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TECHNICAL MANUAL
FOR
DE-211
DATA ELECTRONICS

REVIEWED BY John C Gough
PROJECT ENGINEER

APPROVED BY E. S. Kuns
SECTION MANAGER

AMPEX COMPUTER PRODUCTS DIVISION
P.O. BOX 329, CULVER CITY, CALIF.

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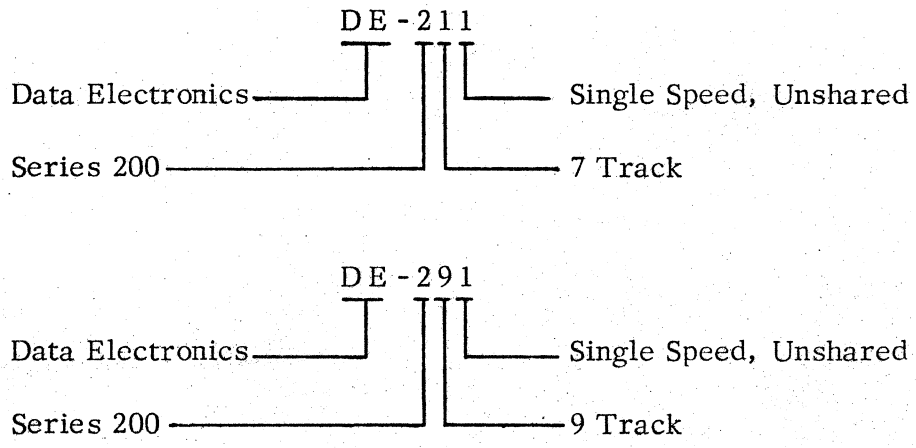
SECTION I
GENERAL DESCRIPTION

1-1. INTRODUCTION.

1-2. SCOPE.

This technical manual describes the installation, operation, theory of operation and maintenance of the DE-211 and the DE-291 Data Electronics.

1-3. MODEL DESIGNATIONS.



1-4. PURPOSE AND BASIC PRINCIPLES.

1-5. PURPOSE.

The Data Electronics card cage is wired, as shown on the Data Electronics Logic Diagram, to accommodate circuit board assemblies which provide the circuitry required to read, write, and check digital data. Seven-track tapes are bilaterally interchangeable with tapes prepared on IBM 729 tape transports. Nine-track tapes are bilaterally interchangeable with tapes prepared per ASCII specifications.

1-6. BASIC PRINCIPLES

The card cage is wired to accommodate circuit boards which will read and write on either 7 or 9 tracks. Wiring is also included to accommodate circuit boards which will perform Vertical Parity Check, and Echo and Rate Checks.

Circuit board assemblies included in the card cage are determined by tape speed, bit packing density, number of tracks, error checking options and bi-directional read capability.

1-7. SPECIAL ADDENDA.

Addenda, which include special logic diagrams, are prepared to document features not included in this manual. Table 1-1 is a partial list of addenda.

TABLE 1-1
PARTIAL ADDENDA LIST

ADDENDUM	DESCRIPTION	LOGIC
3114924	Vertical Parity Generate, 7 Tracks	3114921
3114973	Longitudinal Parity Check	3114904
3114977	Dual Density, Fwd/Stop (Std Levels)	3115496
3115500	LCC Generate, Dual Density	3115776
3115501	Special Neg Levels, Dual Density, Run/Stop	3115445
3115502	Tri-Density, Run/Stop (Std Levels)	3115446
3115503	Read Only, Dual Density, Run/Stop (Std Levels)	3115795
3115530	Special Pos Levels, Dual Density, Run/Stop	3118315
3115758	LCC Generate, Tri-Density	3115757
3115765	Vertical Parity Generate, 9 Tracks	3115766
3118387	Special Pos Levels, Dual Density, Fwd/Stop	3118325
3118390	Special Neg Levels, Tri-Density, Run/Stop	3118323

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. SCOPE.

This section provides information on unpacking, power requirements, installation and cabling. Input signal requirements and output signal characteristics are also described in this section.

2-3. UNPACKING.

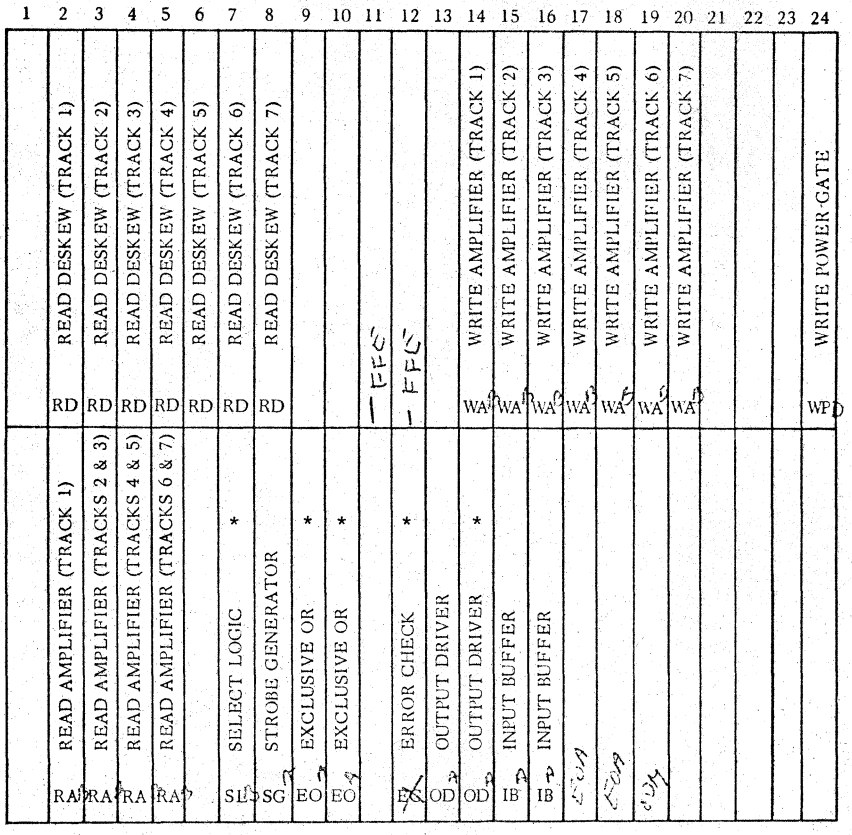
The Data Electronics is installed with the Ampex Tape Transport in the Tape Memory System enclosure. When no enclosure is supplied, the Data Electronics is shipped in custom designed crating. No special unpacking instructions are required. All equipment should be inspected for shipping damage prior to the application of power.

2-4. POWER REQUIREMENTS.

Power for the Data Electronics is supplied by the Ampex Logic Power Supply, which is a separate assembly. The power supply provides three regulated voltage outputs and two unregulated voltage outputs. The power supply requires a maximum input power of 345 watts with all outputs at the full load shown on Table 2-1. If the Ampex Logic Power Supply is not used, provision must be made to supply the voltages listed in Table 2-1 at the required current and regulation.

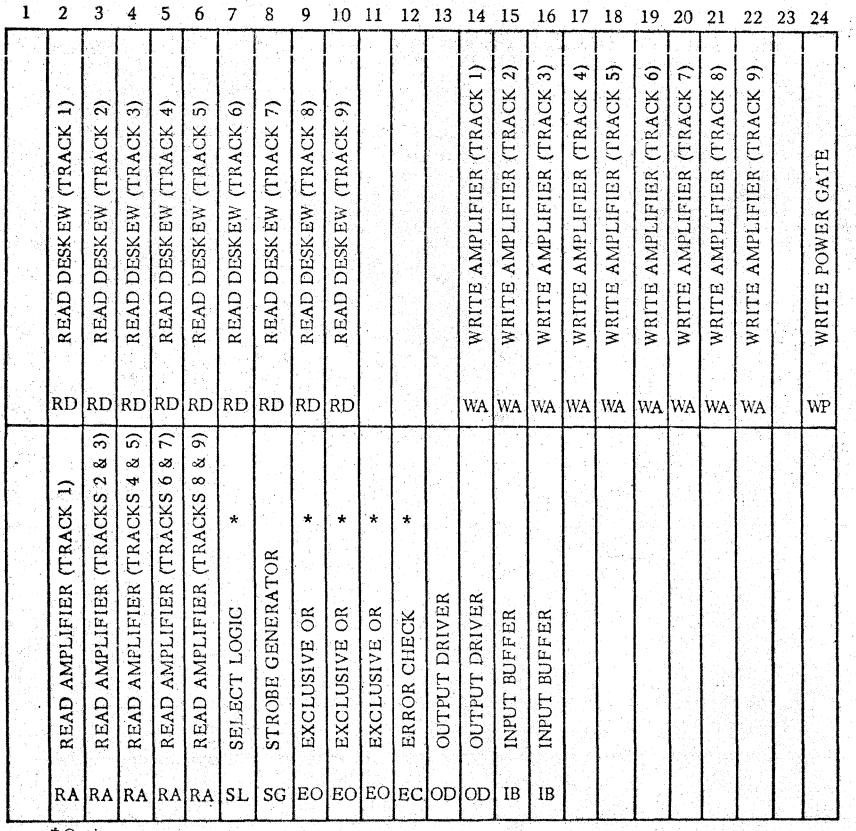
TABLE 2-1
POWER SUPPLY OUTPUT

REGULATED VOLTAGE	CURRENT	REGULATION
+12V	+4.5 Amp	1%
-12V	-5.0 Amp	1%
- 6V	±1.5 Amp	2%
UNREGULATED VOLTAGE	CURRENT	REGULATION
+24V	+0.1 Amp	10%
-24V	-0.1 Amp	10%



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A		READ DESKEW (TRACK 1)	READ DESKEW (TRACK 2)	READ DESKEW (TRACK 3)	READ DESKEW (TRACK 4)	READ DESKEW (TRACK 5)	READ DESKEW (TRACK 6)	READ DESKEW (TRACK 7)						WRITE AMPLIFIER (TRACK 1)	WRITE AMPLIFIER (TRACK 2)	WRITE AMPLIFIER (TRACK 3)	WRITE AMPLIFIER (TRACK 4)	WRITE AMPLIFIER (TRACK 5)	WRITE AMPLIFIER (TRACK 6)	WRITE AMPLIFIER (TRACK 7)				WRITE POWER GATE
		RD	RD	RD	RD	RD	RD	RD						WA	WA	WA	WA	WA	WA	WA				WPD
B		READ AMPLIFIER (TRACK 1)	READ AMPLIFIER (TRACKS 2 & 3)	READ AMPLIFIER (TRACKS 4 & 5)	READ AMPLIFIER (TRACKS 6 & 7)		SELECT LOGIC *	STROBE GENERATOR	EXCLUSIVE OR *	EXCLUSIVE OR *		ERROR CHECK *	OUTPUT DRIVER	OUTPUT DRIVER *	INPUT BUFFER	INPUT BUFFER							
		RA	RA	RA	RA		SL	SG	EO	EO		EC	OD	OD	IB	IB								

7-TRACK
DATA ELECTRONICS
(DE-211)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A		READ DESKEW (TRACK 1)	READ DESKEW (TRACK 2)	READ DESKEW (TRACK 3)	READ DESKEW (TRACK 4)	READ DESKEW (TRACK 5)	READ DESKEW (TRACK 6)	READ DESKEW (TRACK 7)	READ DESKEW (TRACK 8)	READ DESKEW (TRACK 9)				WRITE AMPLIFIER (TRACK 1)	WRITE AMPLIFIER (TRACK 2)	WRITE AMPLIFIER (TRACK 3)	WRITE AMPLIFIER (TRACK 4)	WRITE AMPLIFIER (TRACK 5)	WRITE AMPLIFIER (TRACK 6)	WRITE AMPLIFIER (TRACK 7)	WRITE AMPLIFIER (TRACK 8)	WRITE AMPLIFIER (TRACK 9)		WRITE POWER GATE
		RD	RD	RD	RD	RD	RD	RD	RD	RD				WA	WA	WA	WA	WA	WA	WA	WA	WA		WP
B		READ AMPLIFIER (TRACK 1)	READ AMPLIFIER (TRACKS 2 & 3)	READ AMPLIFIER (TRACKS 4 & 5)	READ AMPLIFIER (TRACKS 6 & 7)	READ AMPLIFIER (TRACKS 8 & 9)	SELECT LOGIC *	STROBE GENERATOR	EXCLUSIVE OR *	EXCLUSIVE OR *	EXCLUSIVE OR *	ERROR CHECK *	OUTPUT DRIVER	OUTPUT DRIVER	INPUT BUFFER	INPUT BUFFER								
		RA	RA	RA	RA	RA	SL	SG	EO	EO	EO	EC	OD	OD	IB	IB								

*Options

9-TRACK
DATA ELECTRONICS
(DE-291)

Figure 2-1
PCB Locations

2-5. INSTALLATION.

Typical Outline and Installation drawings are provided, in the drawing section of this technical manual and in the Tape Transport manuals. Figure 2-1 shows typical printed circuit board assembly (PCBA) locations for 7-track and for 9-track Data Electronics. Mnemonic designations, as shown on the Logic Diagram, are provided. Table 2-2 lists the coded designation which appears on the ejector tab of the PCBA's and provides the part numbers according to basic tape speeds.

2-6. CABLING.

Cabling diagrams for TM-7211, TM-9211 and TM-11211 Tape Memory Systems are supplied in Section VII of this manual. The TM-11211 diagram is also used for TM-12211 systems. Inputs to the system and outputs from the system are connected to the Data Electronics via the connectors on the Input/Output Panel as shown in Tables 2-3 and 2-4, respectively. These inputs and outputs supersede those listed in the Tape Transport manual. Connections from the read heads are shown in Table 2-5 and connections to the write heads in Table 2-6. Table 2-7 lists connections to the Tape Transport. Table 2-8 lists connections to the Logic Power Supply. Tables 2-3 through 2-8 are located at the end of this section.

2-7. INPUT SIGNAL REQUIREMENTS.

2-8. INPUT SIGNAL VOLTAGE LEVELS.

The following signal voltage levels apply to all input signals (the input impedance is 2300 ±115 ohms returned to -3.8 volts.

TRUE Level: -12 (+3, -13) volts

FALSE Level: 0.00 ±1.25 volts

NOTE

When non-standard input levels are provided, special Input Buffer PCBs and wiring changes are required.

2-9. INPUT SIGNAL TIMING.

In the following description of input signal timing, transition times are measured from the 10-percent point to the 90-percent point. Signal duration is measured from the 90-percent point of the leading-edge transition to the 10-percent point of the trailing-edge transition.

TABLE 2-2
PCB PART NUMBERS

CODE	DESCRIPTION	PART NO.
ECC*	Error Check	
	36 ips	3109872-10
	75 ips	3110558-10
	112.5/120/150 ips	3110031-10
EOA**	Exclusive OR	3107274-10
IBA	Input Buffer	3107258-10
ODA	Output Driver	3107259-10
RAB	Read Amplifier	
	36 ips	3107266-10
	75 ips	3109991-10
	112.5/120/150 ips	3110273-10 or 3118138-01
RDB***	Read Deskew (Read Fwd)	
	36 ips	3107269-10
	75 ips	3109475-10
	112.5/120/150 ips	3110004-10
RDC***	Read Deskew (Bidirectional)	
	36 ips	3109932-10
	75 ips	3109935-10
	112.5/120/150 ips	3109936-10
SGA	Strobe Generator	
	36 ips	3107057-10
	75 ips	3109994-10
	112.5/120 ips	3110003-10
	150 ips	3118218-01
SLB***	Select Logic-B	3111157-10
WAB	Write Amplifier	
	36 ips	3112363-10
	75 ips	3109572-10
	112.5/120/150 ips	3110002-10
WPD	Write Power Gate	3107268-10

*The Error Check (ECC) PCB is supplied for the Echo and Rate Check option.
**Two Exclusive OR (EOA) PCBs are supplied for the Vertical Parity Check option.
***Read Deskew (RDB) PCBs are replaced by Bidirectional Read Deskew (RDC) PCBs for bidirectional reading. Select Logic (SLB) is supplied for the bidirectional read option.

2-10. Write Data. (See Figure 2-2.) A minimum interval of 1.5 μsec is required between the 90-percent point of the Write Data leading-edge transition and the 10-percent point of the next Write Strobe leading-edge transition.

A minimum interval of 1.5 μsec is required between the 90-percent point of the Write Strobe trailing-edge transition and the 10-percent of the next Write Data leading-edge transition.

To write a series of ONE's, the Write Data input may be held at the TRUE level for the entire series.

2-11. Write Strobe. (See Figure 2-2.) The Write Strobe leading (and trailing) edge transition time shall not exceed 1.5 μsec.

The Write Strobe TRUE state must coincide with the Write Data TRUE (or FALSE) state for at least 2 μsec.

2-12. Write Reset. The Write Reset leading (and trailing) edge transition time shall not exceed 1.5 μsec.

The Write Reset signal must remain at the TRUE level for at least 1.5 μsec.

The Write Reset signal is used to write the longitudinal check character (LCC) at the end of each block of data. The LCC resets the NRZ1 write register.

A minimum interval of 10^6 μsec/data transfer frequency is required between the 90-percent point of the Write Reset trailing-edge transition and the 10-percent point of the next Write Strobe leading-edge transition.

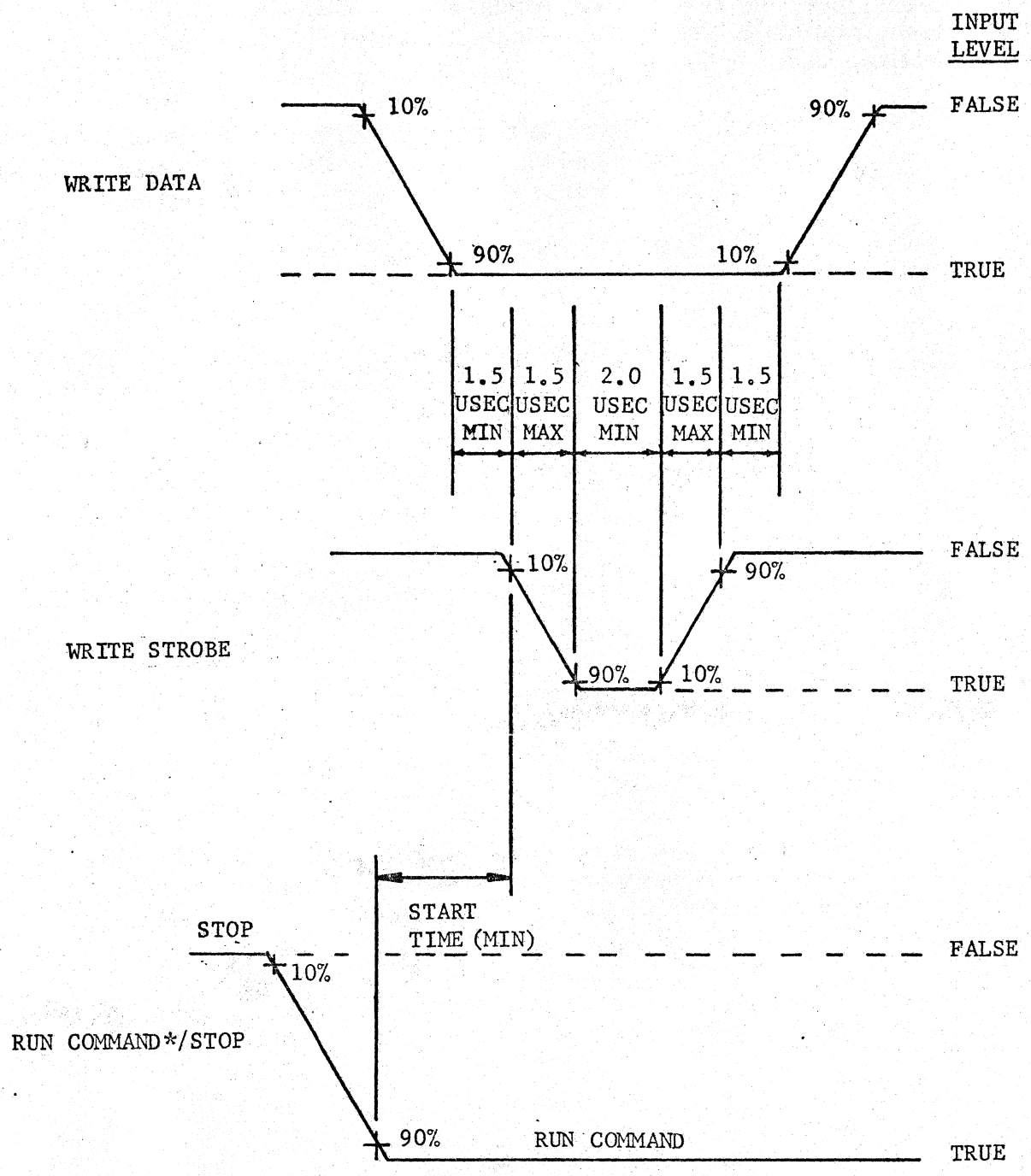
2-13. Write Permit. (See Figure 2-3.) The Write Permit leading (and trailing) edge transition time shall not exceed 5 μsec.

The Write Permit level shall not be changed while the tape is in motion.

CAUTION

Write Permit should be at the FALSE level during Reverse and Rewind operations.

2-14. Read Permit. The Read Permit leading (and trailing) edge transition time shall not exceed 5 μsec.



*Run Command is Run in Fwd/Rev-Run/Stop logic systems and Forward or Reverse in Fwd/Stop-Rev/Stop logic systems.

Figure 2-2
Timing Requirements for Write Data, Write Strobe, and Run/Stop Inputs

2-15. HI/LO Density. The HI/LO Density leading (and trailing) edge transition time shall be 5 μsec maximum. High density is selected by a TRUE level. The high/low density line selects the appropriate timing read circuits.

NOTE

This signal is normally supplied from the tape transport Operator Control Panel.

2-16. Odd/Even Parity. The Odd/Even Parity leading (and trailing) edge transition time shall not exceed 5 μsec. Odd parity is selected by a TRUE level. The Odd/Even Parity line is used to select odd or even Read Vertical Parity check.

2-17. Forward/Reverse. The Forward/Reverse leading (and trailing) edge transition time shall not exceed 5 μsec. (See Figure 2-3A.) The Forward mode is active when this line is at the TRUE level. Forward/Reverse transitions shall not occur while the tape is in motion.

A minimum interval of 5 μsec is required between a Forward/Reverse transition and the Run/Stop transition.

CAUTION

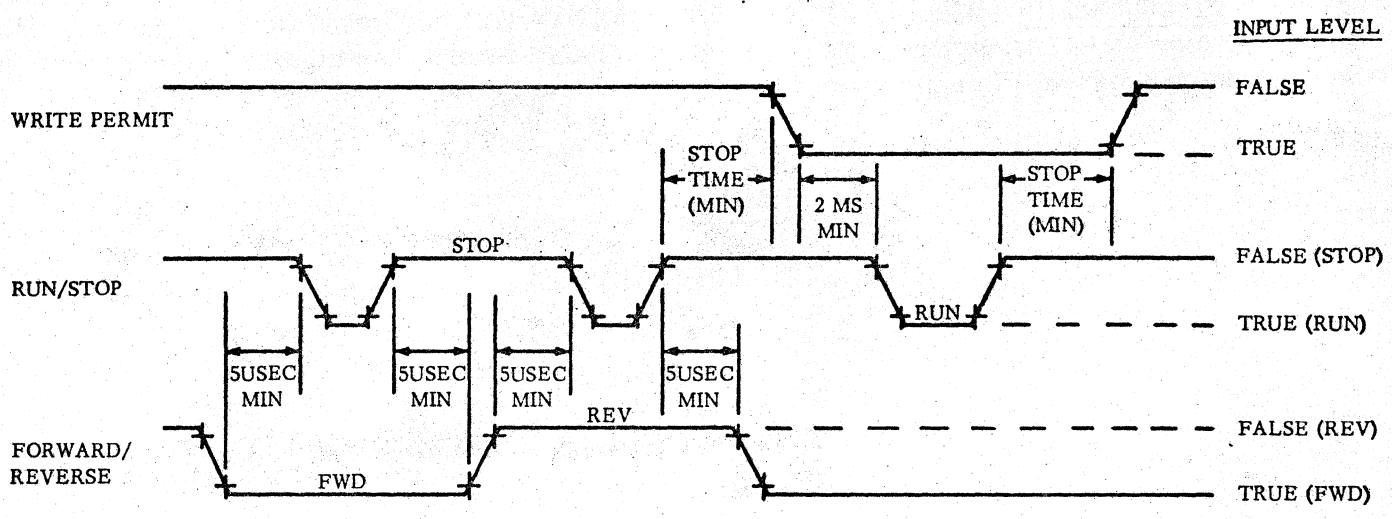
Write Permit should be at the FALSE level when tape is moving in the Reverse direction.

2-18. Run/Stop. The Run/Stop leading (and trailing) edge transition time shall not exceed 5 μsec. (See Figure 2-3B.) A TRUE level on this line sets the transport in the Run mode.

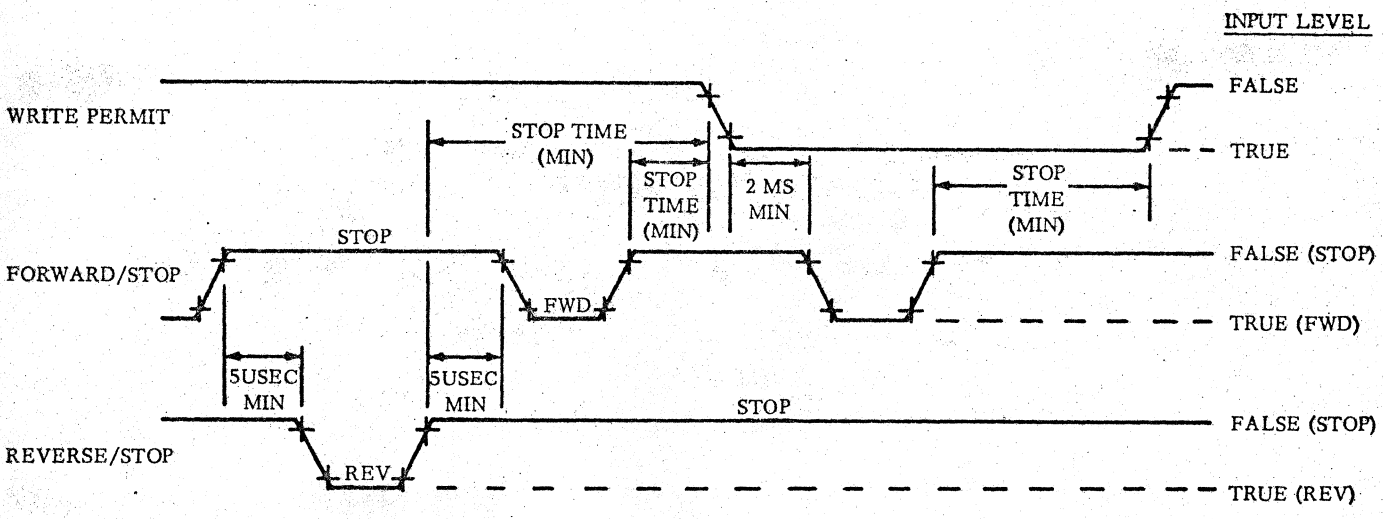
A minimum interval of 5 μsec is required between the Forward/Reverse transition and the Run command.

A minimum interval of 2.0 ms is required between a Write Permit transition and a Run command.

A minimum interval equal to the stop time (to allow tape motion to stop) is required between the 90-percent point of a Stop command transition and a Write Permit transition.



A. Forward/Reverse-Run/Stop Logic



B. Forward/Stop-Reverse/Stop Logic

Figure 2-3
Timing Requirements for Write Permit, Forward/Reverse, Run/Stop, Forward/Stop, and Reverse/Stop Inputs

2-19. Forward/Stop (Option). The Forward/Stop leading (and trailing) edge transition time shall not exceed 5 μsec. (See Figure 2-3B.) The Forward mode is active when this line is at the TRUE level.

A minimum interval of 2.0 ms is required between a Write Permit transition and a Forward command.

A minimum interval equal to the stop time (to allow tape motion to stop) is required between the 90-percent point of a Stop command transition and a Write Permit transition.

2-20. Reverse/Stop (Option). The Reverse/Stop leading (and trailing) edge transition time shall not exceed 5 μsec. (See Figure 2-3B.) The Reverse mode is active when this line is at the TRUE level. A minimum interval equal to the stop time (to allow tape motion to stop) is required between the 90-percent point of a stop command transition and a Write Permit transition.

CAUTION

Write Permit should be at the FALSE level when tape is moving in the Reverse direction.

2-21. Rewind. The Rewind leading (and trailing) edge transition time shall not exceed 5 μsec. The Rewind signal shall remain at the TRUE level for at least 5 μsec. Rewind operation is initiated by the negative-going transition.

2-22. Rewind and Lockout. The Rewind and Lockout leading (and trailing) edge transition time shall not exceed 5 μsec. The Rewind and Lockout signal shall remain at the TRUE level for at least 5 μsec. Rewind and lockout operation is initiated by the negative-going transition.

2-23. OUTPUT SIGNAL CHARACTERISTICS.

2-24. OUTPUT SIGNAL VOLTAGE AND CURRENT LEVELS.

TRUE Level: -11.5 (+2.5, -0.5) volts; 5 ma maximum from the load

FALSE Level: 0.00 ±1.25 volts; 5 ma maximum to the load

NOTE

When non-standard output levels are provided, special Output Driver PCBs and wiring changes are required.

2-25. OUTPUT SIGNAL TIMING.

In the following description of output signal timing, transition times are measured from the 10-percent point to the 90-percent point. Signal duration is measured from the 90-percent point on the leading edge transition to the 10-percent point on the trailing edge transition. Maximum leading edge displacement between Read Data, Read Clock, and Vertical Parity Error outputs is 0.3 μsec maximum.

2-26. Read Data. The Read Data leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.30 μsec. Signal duration is from 0.9 μsec minimum to 1.5 μsec maximum.

2-27. Read Clock. The Read Clock leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.30 μsec. Signal duration is from 0.9 μsec minimum to 1.5 μsec maximum.

2-28. Vertical Parity Error (Option). The Vertical Parity Error leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.30 μsec maximum. Signal duration is from 0.9 μsec minimum to 1.5 μsec maximum.

2-29. Write Check Error (Option). The Write Check Error leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.30 μsec maximum. Signal duration is from 0.5 μsec minimum to 5.3 μsec maximum.

2-30. Write Enable Status. Three lines are provided to indicate the state of the write permit relay on the Data Electronics Write Power Gate PCBA. When a file-protect condition exists, the write permit relay is deenergized and the Write Enable Status (C) line is connected to the Write Enable Status (NC) line. When a write enable condition exists, the write permit relay is energized and the Write Enable Status (C) line is connected to the Write Enable Status (NO) line.

2-31. TAPE TRANSPORT STATUS OUTPUTS.

Tape transport status output levels are -11.5 (+2.5, -0.5) volts (5 ma maximum from the load) and 0.00 ±1.25 volts (5 ma maximum to the load) for TRUE and FALSE, respectively, unless otherwise indicated. The status outputs are active in the remote mode only.

2-32. Beginning-of-Tape (BOT). A TRUE level on the BOT line indicates that the BOT tab is being sensed by the photosense assembly.

2-33. End-of-Tape (EOT). A TRUE level on the EOT line indicates that the EOT tab is being sensed by the photosense assembly.

2-34. High/Low Density Status. The High/Low Density Status line acknowledges the density select level. A TRUE level indicates that high density has been selected. A FALSE level indicates that low density has been selected.

2-35. Ready. A TRUE level on the Ready line indicates that all tape transport interlocks are closed and the transport is ready for remote operation.

2-36. Rewinding. A TRUE level on the Rewinding line indicates that the rewind operation is being performed.

2-37. Unit Select. A TRUE level on the Unit Select line indicates that the tape transport has been selected by a TRUE level at the Select input (when a single tape transport is used, the Select line is returned to -12 volts in the Data Electronics, thus providing a TRUE Select level at all times).

2-38. Select and Remote Indicator. This line is driven by a line driver returned to ground. The line driver must be terminated with an indicator lamp returned to -12 volts (this is normally done by an indicator lamp in the Operator Control Panel of the Tape Transport). When so terminated, the line driver output is 0.0 ±1.5 volts when the Unit Select status line is at the TRUE level; the line driver output is 125 ohms returned to ground when the Unit Select status line is at the FALSE level.

TABLE 2-3
SYSTEM INPUT CONNECTIONS
(FROM CUSTOMER)

INPUT/OUTPUT PANEL CONNECTOR J4 PIN NO.	INPUT SIGNAL	DATA ELECTRONICS CONNECTOR J5 PIN NO.
e	Fwd/Rev (or Rev/Stop)	26
l	Odd/Even Parity	24
f	Rewind Command	28
Z	Rewind and Lockout	27
d	Read Permit	10
Y	Run/Stop (or Fwd/Stop)	25
c	Write Permit	21
X	Write Reset	9
W	Write Strobe	8
C	Write Track 1	1
D	Write Track 2	2
E	Write Track 3	3
F	Write Track 4	4
M	Write Track 5	5
N	Write Track 6	6
P	Write Track 7	7
R	Write Track 8	22
S	Write Track 9	23
G	Spare	31
j	Spare	39
k	Spare	40
A	Ground	11
B	Ground	12
H	Ground	13
J	Ground	14
K	Ground	15
L	Ground	16
T	Ground	17
U	Ground	18
V	Ground	19
a	Ground	35
b	Ground	36
g	Ground	29
h	Ground	30
m	Shield Ground	20

TABLE 2-4
SYSTEM OUTPUT CONNECTIONS
(TO CUSTOMER)

INPUT/OUTPUT PANEL CONNECTOR J5 PIN NO.	OUTPUT SIGNAL	DATA ELECTRONICS CONNECTOR J4 PIN NO.
W	Beginning-of-Tape	21
X	End-of-Tape	22
e	High/Low Density Status	25
R	Read Clock	8
C	Read Track 1	1
D	Read Track 2	2
E	Read Track 3	3
F	Read Track 4	4
M	Read Track 5	5
N	Read Track 6	6
P	Read Track 7	7
G	Read Track 8	9
d	Read Track 9	10
Z	Ready	24
Y	Rewinding	23
k	Unit Select	32
l	Select and Remote Indicator	33
h	Vertical Parity Error	27
c	Write Check Error	29
V	Write Enable Status (C)	38
b	Write Enable Status (NC)	40
a	Write Enable Status (NO)	39
j	Spare	28
f	Spare	26
A	Ground	11
B	Ground	12
H	Ground	13
J	Ground	14
K	Ground	15
L	Ground	16
S	Ground	17
T	Ground	18
U	Ground	19
g	Ground	31
m	Shield Ground	20

TABLE 2-5
DATA ELECTRONICS TO READ HEAD INTERCONNECTIONS

DATA ELECTRONICS J1 PIN NO.	READ HEAD J1 PIN NO.	SIGNAL DESCRIPTION
2	A	Read Track 1
12	D	Read Track 1
23	H	Read Track 2
33	L	Read Track 2
4	P	Read Track 3
14	T	Read Track 3
25	W	Read Track 4
35	Z	Read Track 4
6	a	Read Track 5
16	X	Read Track 5
27	U	Read Track 6
37	R	Read Track 6
8	M	Read Track 7
18	J	Read Track 7
29	E	Read Track 8
39	B	Read Track 8
21	C	Read Track 9
31	F	Read Track 9
9	c	Head Ground
22	--*	Shield Ground

*Shield ground terminated at the read head with lug E1, which is attached to chassis ground near the read head.

TABLE 2-6
DATA ELECTRONICS TO WRITE HEAD INTERCONNECTIONS

DATA ELECTRONICS J7 PIN NO.	WRITE HEAD J2 PIN NO.	SIGNAL DESCRIPTION
2	A	Write Track 1
12	D	Write Track 1
22	--	Shield Ground 1
23	H	Write Track 2
33	L	Write Track 2
13	--	Shield Ground 2
4	P	Write Track 3
14	T	Write Track 3
24	--	Shield Ground 3
25	W	Write Track 4
35	Z	Write Track 4
15	--	Shield Ground 4
6	a	Write Track 5
16	X	Write Track 5
26	--	Shield Ground 5
27	U	Write Track 6
37	R	Write Track 6
17	--	Shield Ground 6
8	M	Write Track 7
18	J	Write Track 7
28	--	Shield Ground 7
29	E	Write Track 8
39	B	Write Track 8
19	--	Shield Ground 8
21	C	Write Track 9
31	F	Write Track 9
11	--	Shield Ground 9
20	b	Erase Head Power
30	d	Erase Head Return
40	--	Shield Ground Erase Head
10	S	Write Power (Head CT)
9	c*	Head Ground
--	--**	Common Shield

*Head ground also terminated at the write head with lug E1, which is attached to chassis ground near the write head.

**Common shield terminated at the write head with lug E2, which is attached to terminal E2 near the write head.

TABLE 2-7
DATA ELECTRONICS TO TAPE TRANSPORT INTERCONNECTIONS

DATA ELECTRONICS J6 PIN NO.	SIGNAL DESCRIPTION	TM-7/TM-9 J10 PIN NO.	TM-11/TM-12 CONTROL ELECTRONICS J4 PIN NO.
6	Beginning-of-Tape (-)	6	11
8	End-of-Tape (-)	8	12
1	Forward/Reverse (-/+)*	1	14
7	High/Low Density (-/+)	7	7
19	High/Low Density Status (-/+)	19	3
10	Ready (-)	10	2
4	Rewind and Lockout (-)	4	9
3	Rewind Command (-)	3	8
9	Rewinding (-)	9	1
2	Run/Stop (-/+)**	2	15
5	Select (-)	5	4
18	Select and Remote Indicator (+)	18	6
14	Unit Select (-)	14	5
15	Write Enable Switch/Relay (C)	15	18
16	Write Enable Switch/Relay (NC)	16	17
17***	Write Enable Switch/Relay (NO)	17	19
11	Ground	11	13
12	Ground	12	16
13	Ground	13	10
20	Shield Ground	20	20

*Reverse/Stop (-/+) when Fwd/Stop-Rev/Stop logic is supplied.
**Forward/Stop (-/+) when Fwd/Stop-Rev/Stop logic is supplied
***Pin 17 of J6 is returned to ground in the Data Electronics

TABLE 2-8
DATA ELECTRONICS TO POWER SUPPLY INTERCONNECTIONS

DATA ELECTRONICS TS1 TERMINAL NO.	LOGIC POWER SUPPLY TS1 TERMINAL NO.	VOLTAGE
1	6	+12 VDC (Regulated)
2	8	Ground
3	10	-6 VDC (Regulated)
4	12	Ground
5	2	-12 VDC (Regulated)
6	4	Ground
7	13	+24 VDC (Unregulated)
8	14	Ground
9	15	-24 VDC (Unregulated)
10	16	Ground

SECTION III
OPERATION

3-1. INTRODUCTION.

This section briefly describes the operation of the Data Electronics.

3-2. OPERATING MODES.

The Data Electronics is capable of operating in three different modes: write check, write only, and read only. The operating mode is determined by the level of the Read Permit and Write Permit input signals.

3-3. WRITE CHECK MODE.

In the Write Check Mode, information is read immediately after it is written. To operate in the Write Check Mode, Write Permit and Read Permit inputs must be TRUE.

3-4. WRITE ONLY MODE.

In the Write Only Mode, information is written but reading does not occur. To operate in the Write Only Mode, Write Permit input must be TRUE and Read Permit input must be FALSE.

3-5. READ ONLY MODE.

In the Read Only Mode, information is read, but writing does not occur. To operate in the Read Only Mode, Read Permit input must be TRUE and Write Permit input must be FALSE.

3-6. WRITE SIGNAL CONDITIONING.

Writing of data is accomplished on seven (or nine) tracks. In the following description of write signal conditioning, the operation of only one track is discussed. Each input signal is conditioned by an input buffer.

3-7. WRITE DATA. (See Figure 3-1.)

Data is written when the Write Data input is strobed through an AND gate by the Write Strobe and fed, via an OR gate, to the Write Deskew single-shot delay. Write Head gap-to-gap static skew is compensated for by the single-shot delay. The deskewed Write Data signal is fed to the write register. Write Permit is comprised of the ANDed Write Permit and Run inputs. The write register controls the direction of current flow in the write head.

3-8. WRITE POWER.

When the Write Permit signal is TRUE and a Write Enable Ring is in place, power is supplied to the Write and Erase Heads through the Write Power Gate.

3-9. WRITE RESET.

The Write Reset signal is ANDed with the Set status output of the NRZ Write Register and is then fed to the NRZ Write Register flip-flops via the OR gate and the single-shot delay. The Write Reset line is used to write the Longitudinal Check Character (LCC) at the end of each block of data. The LCC is used to reset the NRZ register, resulting in an even number of flux reversals (ONEs) in each track of the block.

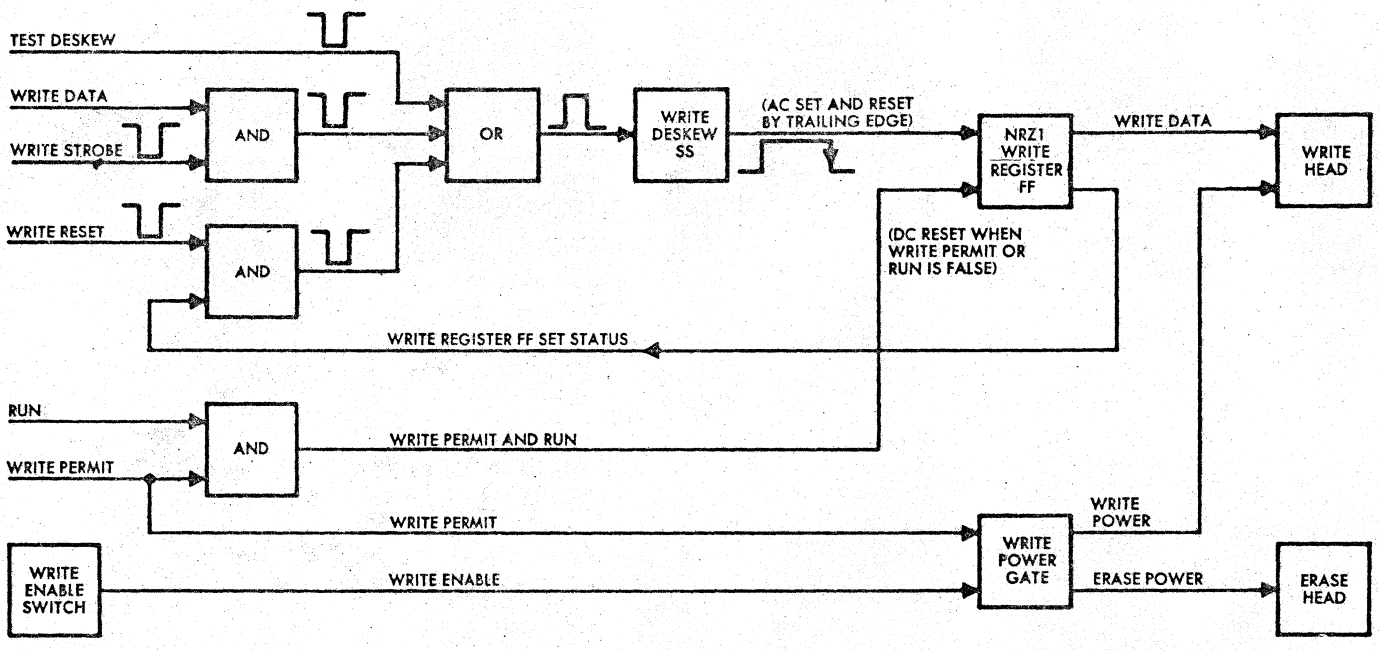


Figure 3-1
Read Signal Conditioning, Block Diagram

3-10. READ SIGNAL CONDITIONING.

Reading of data is accomplished on seven (or nine) tracks. In the following description of read signal conditioning, only one track is discussed.

3-11. READ DATA. (See Figure 3-2.)

The signals from the Read Head are amplified by the Read Amplifier and fed to the peak detector circuit on the Read Deskew PCBA. The peak detector generates positive pulses, corresponding in time to the peaks of the analog Read Head signals. The peak detector clipping level is established as a function of Write Permit.

The Read Data from the peak detector is fed to the Read Deskew single-shot delay. Read head gap-to-gap static skew is compensated for by the single-shot delay. The deskewed Read Data signal is fed to the Read Register. Bi-directional Read Deskew circuits are available as an option.

When a Read Permit signal is present, the Read register assembles the deskewed Read Data signals within each character frame and drives the data output drivers.

3-12. STROBE GENERATION.

The Strobe Generator provides the Strobe signal for the Read Data and Read Parity Error AND gates, and the Read Clock signal to the Read Clock output driver.

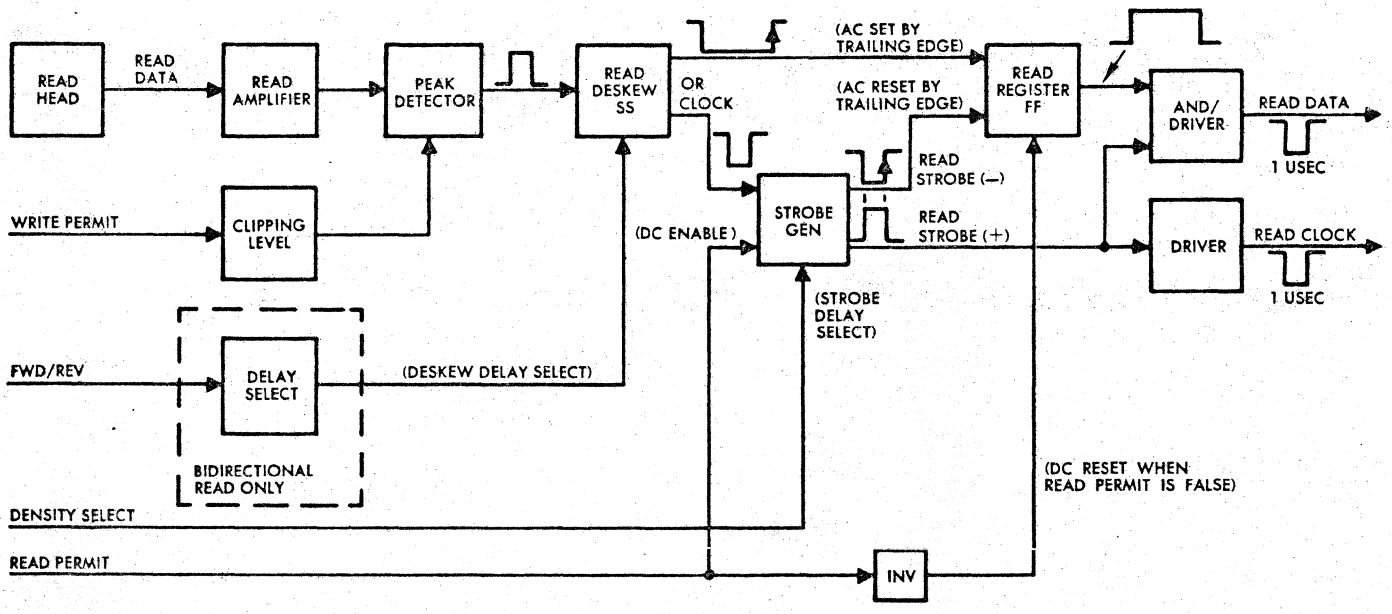


Figure 3-2
Write Signal Conditioning, Block Diagram

3-13. ERROR CHECKING.

3-14. VERTICAL PARITY CHECK.

The vertical parity check circuits generate an Error signal when the parity of the read register does not correspond to the status of the Odd/Even Parity input. In the Read Only Mode, the Error output is provided at the Vertical Parity Error output. In the Write Check Mode, the error indication is provided at the Vertical Parity Error output and at the Write Check Error output

3-15. RATE CHECK.

The rate check circuit generates a Write Check Error output when the time interval between successive characters is below a design threshold.

3-16. ECHO CHECK.

In ORed Clock systems, at least one Write Amplifier flip-flop must change state after each Write Strobe. The echo check circuits generate a Write Check Error output when none of the Write Amplifiers change state after receipt of a Write Strobe.

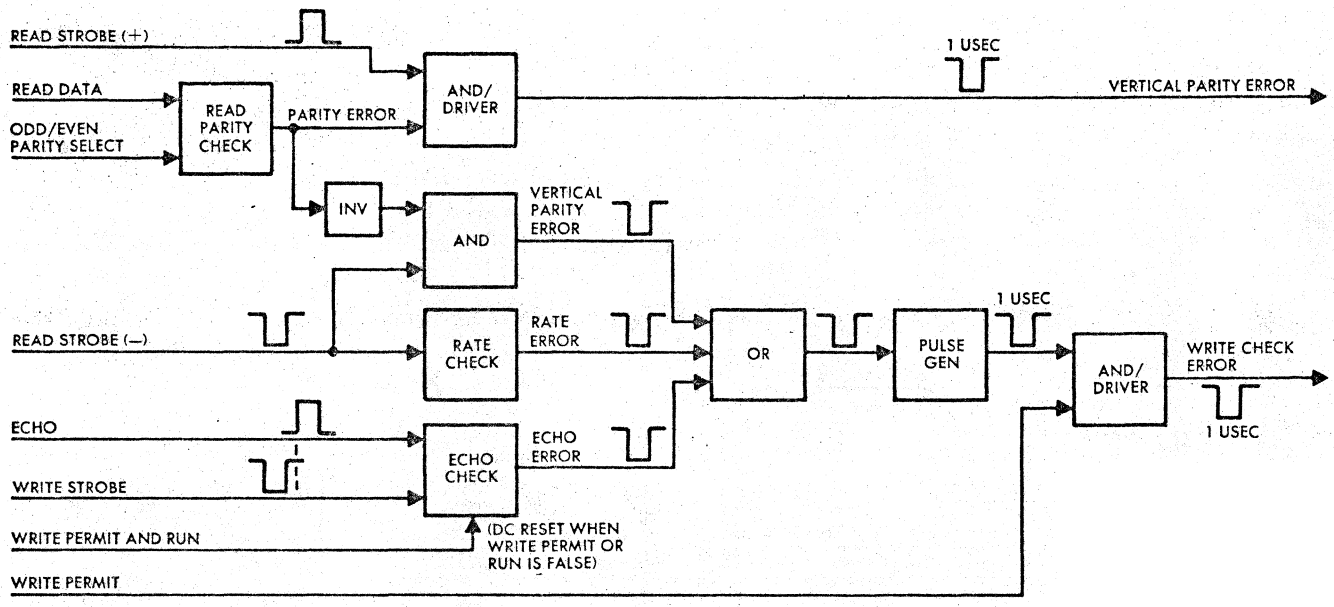


Figure 3-3
Error Check Circuits, Block Diagram

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION.

This section includes the theory of operation of the Data Electronics and an introduction to the graphic symbols used in the logic diagrams.

4-2. LOGIC DIAGRAM.

The Data Electronics logic diagrams in Section VII illustrate the logic functions in the data card cage. Use of the logic diagrams will facilitate the rapid diagnosis and localization of equipment malfunctions.

4-3. LOGIC LEVELS.

Most Data Electronics signals are binary level. Where binary levels are used, one of the two levels is a 0.0 ±0.5 volt level. The second level is generally a -6 volt level. In some circuits, -12 volt, +6 volt, or +12 volt levels are used. When the binary signal levels are 0 and -6 or -12, the 0 volt level is relatively high and is therefore termed positive (+). When the binary signal levels are 0 and +6 or 0 and +12, the 0 volt level is relatively low and is therefore termed negative (-).

Signal callouts in the Data Electronics logic drawing (Section VII) show the TRUE (active state) of the signal. Write Permit (-) indicates that Write Permit is TRUE when the Write Permit signal is relatively low. Read Strobe (+) indicates that Read Strobe is TRUE when the Read Strobe signal is relatively high. Run/Stop (-/+) indicates Run (-) is TRUE when the signal is relatively low and Stop (+) is TRUE when the signal is relatively high.

4-4. LOGIC ELEMENTS.

4-5. Identification. Identification of a logic element is accomplished by the graphic symbol and the notation within the symbol. (See Figure 4-1.) The mnemonic designation identifies the PCB nomenclature. The bottom notation identifies the physical location of the PCB in the card cage.

4-6. State Indicators. A state indicator (small circle) at the input to any logic element indicates that the relatively-low level of the input signal activates the function. A state indicator at the output of any element indicates that the output level of the activated function is relatively low.

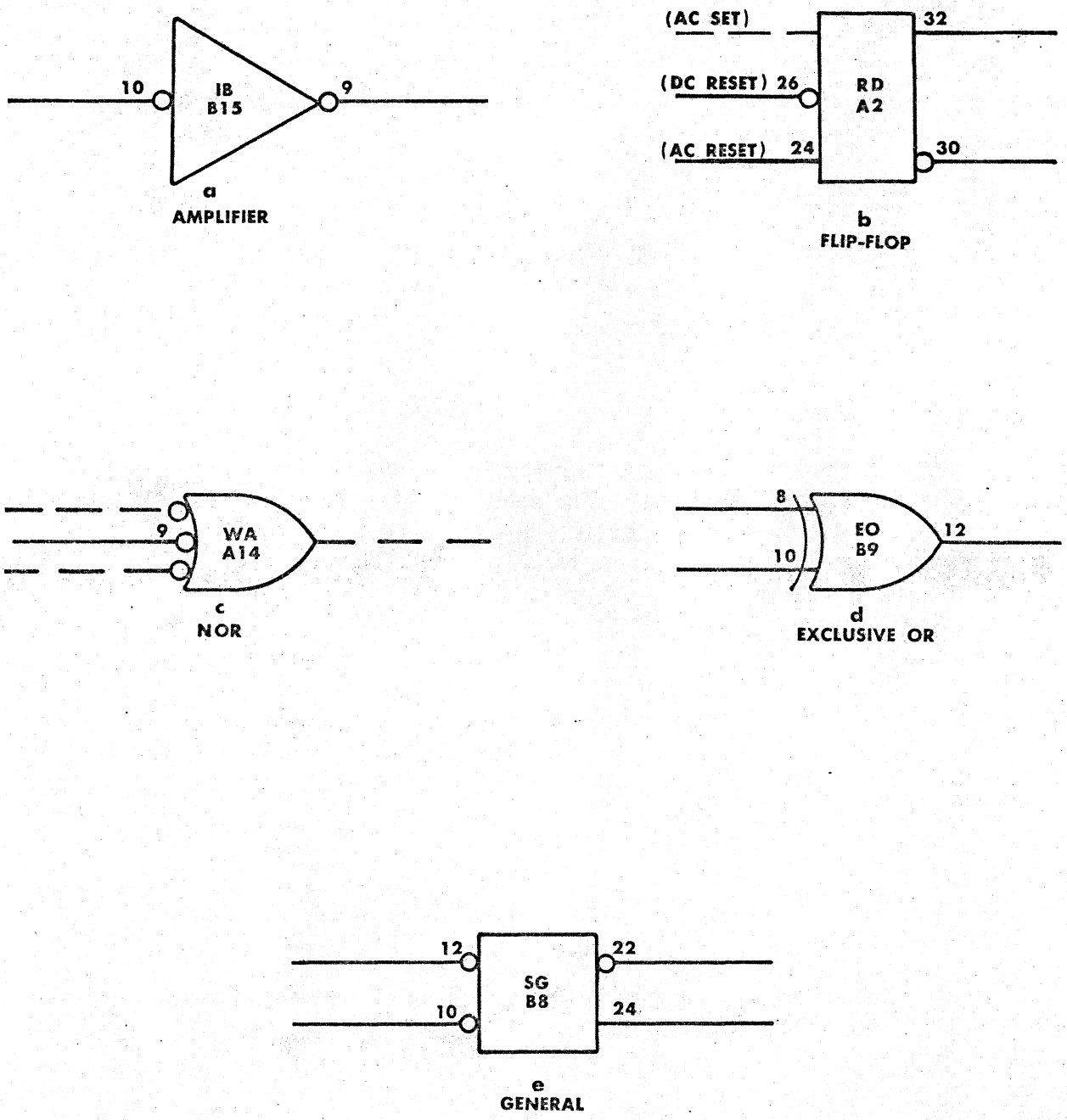


Figure 4-1
Logic Symbols

4-7. SIGNAL FLOW DIRECTION.

Direction of signal flow is indicated by logic symbol orientation. Inputs to a circuit are from the left and outputs are from the right.

4-8. LOGIC SYMBOLS.

4-9. Amplifiers. The triangular symbol represents either a current or a voltage amplifier. The amplifier may have one or more stages and may or may not produce gain or inversion. Figure 4-1a represents an Input Buffer circuit. The presence of state indicators (small circles) at input pin 10 and output pin 9 signifies that inversion has not taken place.

4-10. Flip-Flops. The rectangular symbol, Figure 4-1b, denotes the flip-flop. The flip-flop is a device which stores a single-bit of information. Two or more inputs may be used to Set or Reset the flip-flop to produce two simultaneous outputs, low level and high level. The outputs of the flip-flop are always shown in the set state.

4-11. Gate Circuits. Gate circuits are represented as shown in Figures 4-1c and 4-2 and may have one or more stages that may or may not produce gain or inversion. The presence of state indicators at the inputs or at the single output indicate whether or not inversion has taken place.

A two-input AND gate, Figure 4-2a, signifies that two relatively low levels coincidental at the inputs (pins 11 and 12) will produce a relatively low output. Conversely, Figure 4-2c denotes a two-input AND gate where two relatively high levels present coincidentally at the inputs will produce a relatively high output.

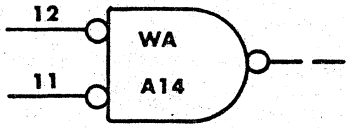
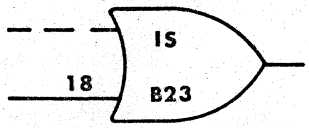
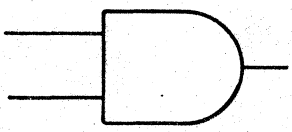
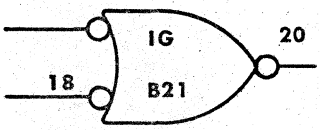
Figure 4-2e represents a two-input NAND (NOT-AND) gate that produces inversion. When two relatively high levels are present coincidentally at the inputs (pins 11 and 12) a relatively low level output is produced. Conversely, in Figure 4-2g, two low levels coincidental at the inputs will produce a relatively high level output from the NAND gate.

Two-input OR gates, Figure 4-2b and 4-2d, produce an output when a signal is present at any of the inputs. In Figure 4-2b, a relatively high level at either of the inputs will produce a high level output. In Figure 4-2d, a relatively low level at either of the inputs will produce a relatively low level output.

In Figures 4-2f and 4-2h, inversion takes place in the two-input NOR (NOT-OR) gates. When a relatively low level is present at any input of the NOR gate, Figure 4-2f, a relatively high level is produced at the output. A relatively high level present at either input of the NOR gate shown in Figure 4-2h will produce a relatively low output from the NOR gate.

LOGIC SYMBOLS

TRUTH TABLES

AND	OR	INPUT 1	INPUT 2	OUTPUT
 a	 b	LOW	LOW	LOW
		LOW	HIGH	HIGH
		HIGH	LOW	HIGH
		HIGH	HIGH	HIGH
 c	 d	LOW	LOW	LOW
		LOW	HIGH	LOW
		HIGH	LOW	LOW
		HIGH	HIGH	HIGH

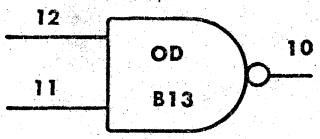
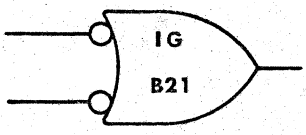
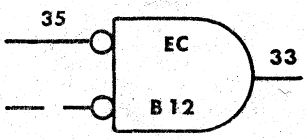
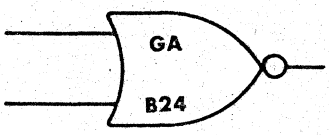
NAND	NOR	INPUT 1	INPUT 2	OUTPUT
 e	 f	LOW	LOW	HIGH
		LOW	HIGH	HIGH
		HIGH	LOW	HIGH
		HIGH	HIGH	LOW
 g	 h	LOW	LOW	HIGH
		LOW	HIGH	LOW
		HIGH	LOW	LOW
		HIGH	HIGH	LOW

Figure 4-2
Gate Circuits

Figure 4-1c represents a three-input NOR gate. A relatively low input at any of the three inputs will cause a relatively high level at the output. The absence of pin numbers and the dashed lines indicate that the preceding and following logical elements are on the same printed circuit board.

3-INPUT NOR GATE TRUTH TABLE

INPUT 1	INPUT 2	INPUT 3	OUTPUT
High	Low	Low	High
High	High	Low	High
High	High	High	Low
Low	High	High	High
Low	Low	High	High
Low	Low	Low	High

4-12. Exclusive OR Gates. Exclusive OR gates are used in the optional error detection circuits. Figure 4-1d represents the Exclusive OR gate. A relatively high level output appears only when the inputs are dissimilar.

EXCLUSIVE OR GATE TRUTH TABLE

INPUT 1	INPUT 2	OUTPUT
High	Low	High
Low	High	High
High	High	Low
Low	Low	Low

4-13. General Circuit Symbols. Rectangular or square symbols denote other circuits. Figure 4-1e represents a Strobe Generator circuit. State indicators denote the relative signal level at the inputs and outputs of the circuit element. Refer to the detailed descriptions of the PCB circuits in Section VI for other circuit designations.

4-14. WRITE LOGICAL SEQUENCE.

4-15. INPUT BUFFERS.

Input buffers are used to provide isolation and supply power gain to the input signals.

4-16. WRITE DATA.

A TRUE (low level) Write Data signal at pin 12 of the write amplifier data input AND gate enables the AND gate. A Write Strobe pulse coincidental with the TRUE Write Data signal produces a negative-going pulse at the output of the AND gate. The negative-going pulse is applied through a NOR gate to the input of the Write Deskew single-shot delay. The positive-going pulse from the NOR gate triggers the single-shot delay, which produces a positive-going pulse. The width of the single-shot delay pulse is adjustable and is set to compensate for the gap-to-gap misalignment (static skew) of the write heads.

The negative-going trailing edge of the single-shot delay pulse triggers the Write Register flip-flop and the flip-flop changes state. When the flip-flop changes state, the direction of current flow through the write head is reversed, which causes the polarity of the head magnetic flux to reverse. The flux polarity change is impressed on the tape and is interpreted as a logical ONE during the read function.

4-17. WRITE RESET.

The Write Reset signal is used to reset the Write Register flip-flops and to generate the LPC character. The Write Register flip-flops are in the reset state at the start of each block of write data. If an odd number of data bits are written on any one track, that Write Register flip-flop is in the set state after the last data bit of the block is written. A low level status signal from the set flip-flop enables the Write Amplifier reset AND gate. The Write Reset pulse produces a negative-going pulse at the output of the reset AND gate. The negative-going pulse is applied through the NOR gate to the input of the Write Deskew single-shot delay and causes a ONE to be written as previously described for the Write Data input. The Write Register flip-flop is then in the reset state.

The reset of the flip-flops generates the LCC which provides an even number of data bits in each track of a data block.

4-18. WRITE REGISTER DC RESET.

The Write Permit signal input is inverted and NANDed with the inverted Run/Stop signal input (or with the inverted Fwd/Stop signal input in Fwd/Stop-Rev/Stop logic systems).

The NAND gate is located on the Strobe Generator PCB. When either the Write Permit signal or the Run/Stop (or Fwd/Stop) signal is at the FALSE (high) level, the output of the NAND gate is at the low level. The low level output from the NAND gate DC resets the Write Register flip-flops and holds the flip-flops in the reset state.

4-19. TEST DESKEW.

A negative-going Test Deskew pulse train applied at Test Point TP1 of the Data Electronics is applied through the Write Amplifier NOR gates to the inputs of the Write Deskew single-shot delays. The pulses cause all ONEs to be written as previously described for the Write Data input. The Test Deskew input is used during off-line Write Deskew adjustment procedures. The Write Reset and the Write Strobe inputs must be FALSE when the Test Deskew input is used.

4-20. WRITE HEAD POWER.

Write Head Power is furnished by the Write Power Gate. When the Write Permit input is at the TRUE level and a write enable ring is in place in the file reel, +10 volt power is supplied to the write heads from the Write Power Gate PCB through pins 28, 29, and 30. The write power relay on the Write Power Gate PCB is energized when the write enable ring is sensed by the write enable switch assembly on the tape transport.

4-21. READ LOGICAL SEQUENCE.

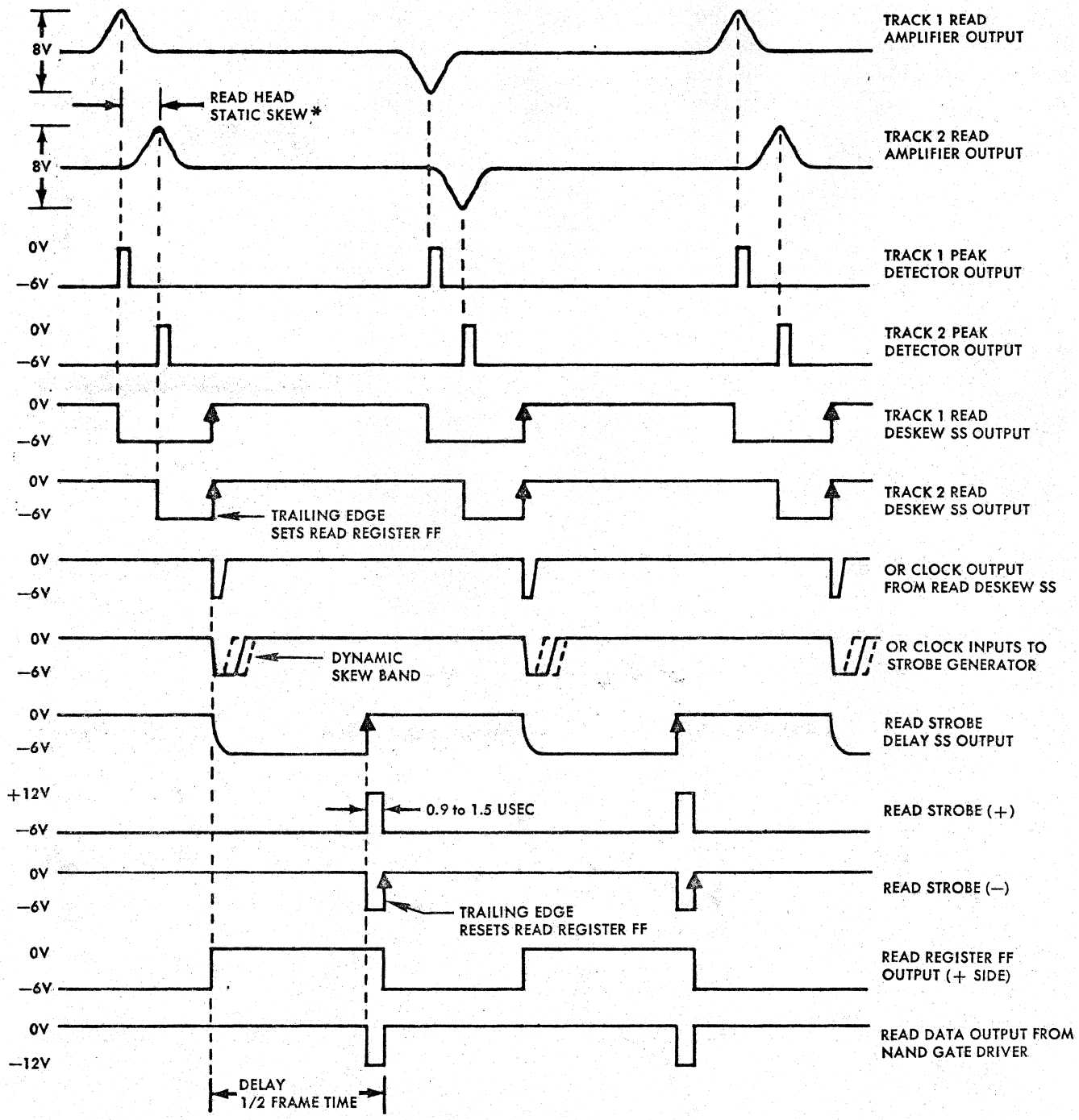
4-22. READ PERMIT.

Read Permit TRUE enables the read strobe generator circuits. Read Permit FALSE DC resets the read register flip-flops and holds the flip-flops in the reset state.

4-23. READ DATA. (See Figure 4-3.)

Flux transitions (written ONEs) on the tape are sensed by the read heads as bipolar analog Read Data signals. The Read Data signals from each read head are amplified in a three-stage differential voltage amplifier on the associated Read Amplifier PCB assembly and then applied to a differential voltage amplifier on the associated Read Deskew PCB assembly.

The differential output from the amplifier on the Read Deskew PCB assembly is clipped in a clipping stage at the input of the peak detector circuit. The clipping level is established by the clipping bias generated on the Strobe Generator PCB assembly and is selected by the Write Permit signal. The clipping bias level is higher when Write Permit is TRUE.



*The read amplifier data outputs are caused by flux reversals on the tape which are sensed by the read heads. Flux reversals on the tracks are written coincidentally; the time displacement shown (read head static skew) is caused by gap-to-gap misalignment of the read heads.

Figure 4-3
Read Deskew Timing

The clipped analog Read Data signal is applied to the peak detector circuit which produces a positive-going pulse at the positive or negative peaks of the signal. The leading edge of the peak detector output pulse is coincident with the detected peak. The positive-going pulse triggers the Read Deskew single-shot delay, which produces a negative-going pulse. The width of the single-shot delay pulse is adjustable and is preset to compensate for the gap-to-gap misalignment (static skew) of the read head. Two pulse widths are set for bidirectional read systems; the forward deskew pulse width is selected when the Forward/Reverse (or Forward/Stop) input is TRUE, the reverse deskew pulse width is selected when the Forward/Reverse (or Forward/Stop) input is FALSE.

The positive-going trailing edge of the single-shot delay pulse sets the Read Register flip-flop and the Read Data output at pin 32 of the Read Deskew PCB goes to the TRUE (high) level. The Read Data output is applied to one input of a NAND gate driver circuit and enables the NAND gate. A Read Strobe (+) pulse coincidental with the TRUE Read Data signal produces a negative-going pulse at the output of the NAND gate driver. The negative-going pulse is a TRUE Read Data output representing a ONE sensed from the tape.

The Read Register flip-flop is reset by the positive-going trailing edge of the Read Strobe (-) pulse.

4-24. READ STROBE.

The Read Strobe (+) and Read Strobe (-) pulses are generated on the Strobe Generator PCB assembly. The positive-going trailing edge of each Read Deskew single-shot delay pulse is coupled through an associated inverter driver stage to produce a negative-going OR Clock pulse. The OR Clock pulses are applied to one common input of an AND gate on the Strobe Generator PCB. The other input to the AND gate is the Read Permit signal. When Read Permit is at the TRUE (low) level, the OR Clock pulses are passed through the AND gate. The first OR Clock pulse through the AND gate triggers the Read Strobe single-shot delay, which produces a negative-going pulse. The width of the single-shot delay pulse is adjustable and is preset to approximately one-half the character frame time, less the read strobe pulse time. Two single-shot delay pulse widths are preset: one for the high density packing rate, the other for the low density packing rate. Selection of the pulse width is accomplished by switching circuits on the Write Power Gate PCB. When the HI/LO Density line is at the low level, the High Density pulse width is selected. When the HI/LO Density line is at the high level, the Low Density pulse width is selected.

The positive-going trailing edge of the Read Strobe single-shot delay pulse is coupled to a pulse generator circuit which then generates the positive-going Read Strobe (+) pulse. The pulse width of the Read Strobe (+) pulse is approximately 1 microsecond. The Read Strobe (+) pulse is inverted through an inverter stage to produce the Read Strobe (-) pulse.

4-25. ERROR CHECK OPTIONS.

Error check options consist of Vertical Parity Check, Rate Check, and Echo Check. (See the Data Electronics Logic Diagram in Section VII.)

4-26. VERTICAL PARITY CHECK.

Vertical Parity is checked during both Read Only and Write Check Modes of operation by a continuous frame-by-frame check of the contents of the read register. A parity-select level from the customer selects either odd or even parity check. Odd parity requires an odd number of logical ONEs be recorded in every character frame. Even parity requires an even number of logical ONEs in every character frame. A Vertical Parity Error exists when an extra (or missing) logical ONE is detected.

Numerical values in parenthesis in the following circuit description refer to 9-track systems. The Odd/Even Parity Select line and the complementary outputs of the Read Register flip-flops are applied to the inputs of the parity checking circuit on the Exclusive OR PCB assembly. Eight Exclusive OR gates are used for 7-track systems, nine for 9-track systems. Each gate compares two inputs and produces a high level output when the logic levels of the inputs are dissimilar. Seven (or nine) Read Data (-) lines from the Read Register flip-flops and the Odd/Even Parity Select line are applied to four (or five) of the Exclusive OR gates. The outputs of the four gates are applied in pairs to the following two Exclusive OR gates, the outputs of which are compared by a single gate. The output of the single gate is compared in a final Exclusive OR gate with a fixed low level input (in 9-track systems, the output of the fifth input Exclusive OR gate is compared with the output of the single gate in the final Exclusive OR gate). The output of the final gate is ANDed with the Read Strobe (+) pulse in a NAND gate driver. If a vertical parity error is sensed, a negative-going Vertical Parity Error pulse is produced at the output of the NAND gate driver and is transmitted to the customer via the system output connector.

4-27. RATE CHECK.

Rate Check is performed only during the Write/Check mode. A Rate error pulse is generated when the interval between successive Read Strobe (-) pulses decreases to

$$0.67 \frac{1}{(\text{tape speed in ips})\ (\text{high bit packing density})}$$

The Rate Check circuit is located on the Error Check PCB and operates in the following manner. (See Figures 4-4 and 4-5.) The Read Strobe (-) pulse triggers single-shot delay A which produces a negative-going pulse. The positive-going trailing edge of the single-shot delay A pulse triggers single-shot delay B, which produces a negative-going pulse. The next arriving Read Strobe (-) pulse retriggers single-shot delay A and also is ANDed with the output of single-shot delay B. If the Read Strobe (-) pulse and the output pulse from single-shot delay B are coincident, a rate error pulse is generated.

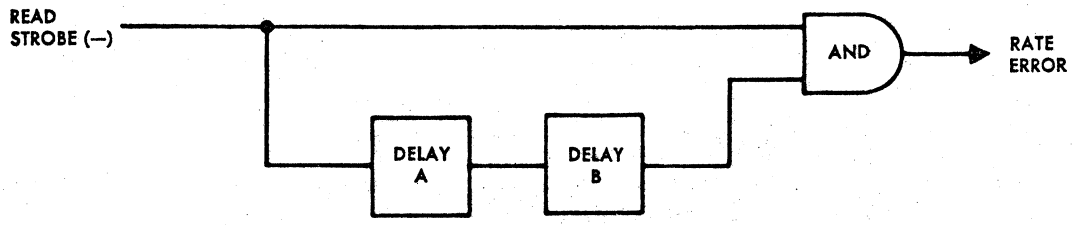


Figure 4-4
Rate Error Check, Block Diagram

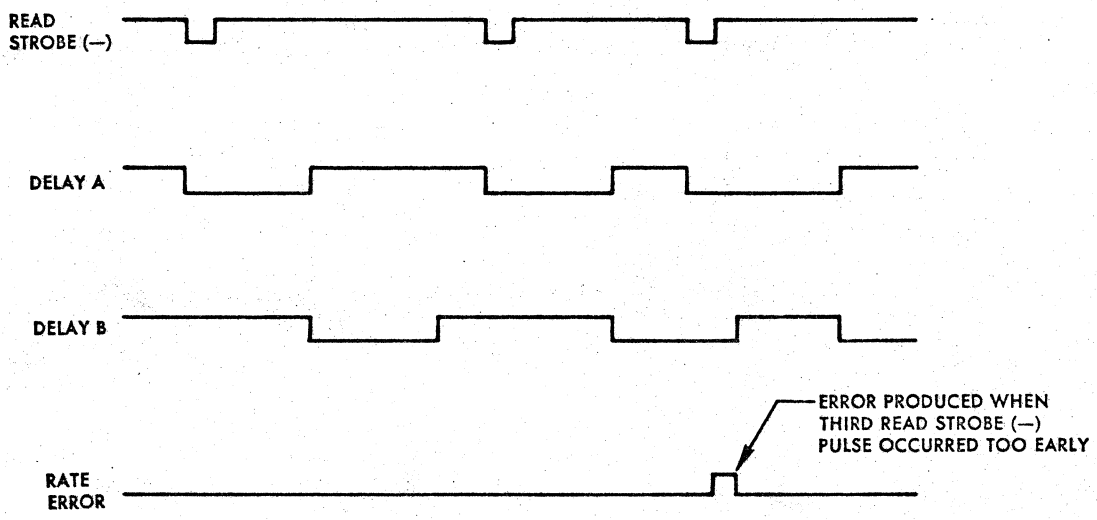


Figure 4-5
Rate Error Timing

4-28. ECHO CHECK.

An Echo output is generated by each Write amplifier whenever the amplifier changes state and reverses the Write head coil current. The Echo output is a positive-going pulse derived from the induced EMF generated by the Write head inductance when the write head coil current reverses.

In ORed Clock systems, the data that is written must cause at least one head driver to change state in each frame. The Echo output of each Write amplifier is ORed with the Echo outputs of all other Write amplifiers to generate an ORed Echo output. The ORed Echo output occurs if any Write amplifier changes state during the frame interval. If no ORed Echo occurs during the frame, a malfunction in the Write circuits is indicated and an Echo error pulse is generated by the Echo Check circuits.

The Echo error pulse is generated in the following manner. (See Figures 4-6 and 4-7.) The Write Strobe triggers the single-shot delay and the leading edge of the single-shot delay pulse sets the flip-flop. The Write Strobe holds the AND gate FALSE for the strobe duration to prevent any output from the AND gate during the period that the single-shot delay and flip-flop are going TRUE. The AND gate is also held FALSE by the single-shot delay pulse for the duration of its delay. The Echo input must occur sometime after the Write Strobe and within the duration of the single-shot output. The Echo input resets the flip-flop. If no Echo input occurs, the flip-flop remains set at the end of the single-shot delay pulse and the output of the AND gate goes TRUE, indicating an Echo Error.

4-29. WRITE/CHECK ERROR.

The Vertical Parity Check output, Rate Check output, and Echo Check output are ORed together. The occurence of any error triggers a pulse generator circuit, which produces a negative-going 1 microsecond error pulse. The error pulse is ANDed with Write Permit. If the Write Permit is TRUE, a negative-going Write Check Error pulse is produced at the output of the AND gate driver and is transmitted to the customer via the system output connector.

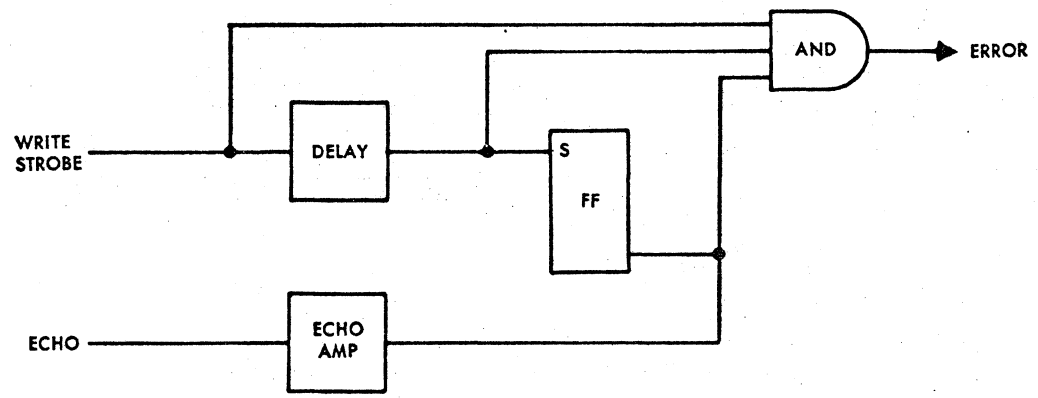


Figure 4-6
Echo Check, Block Diagram

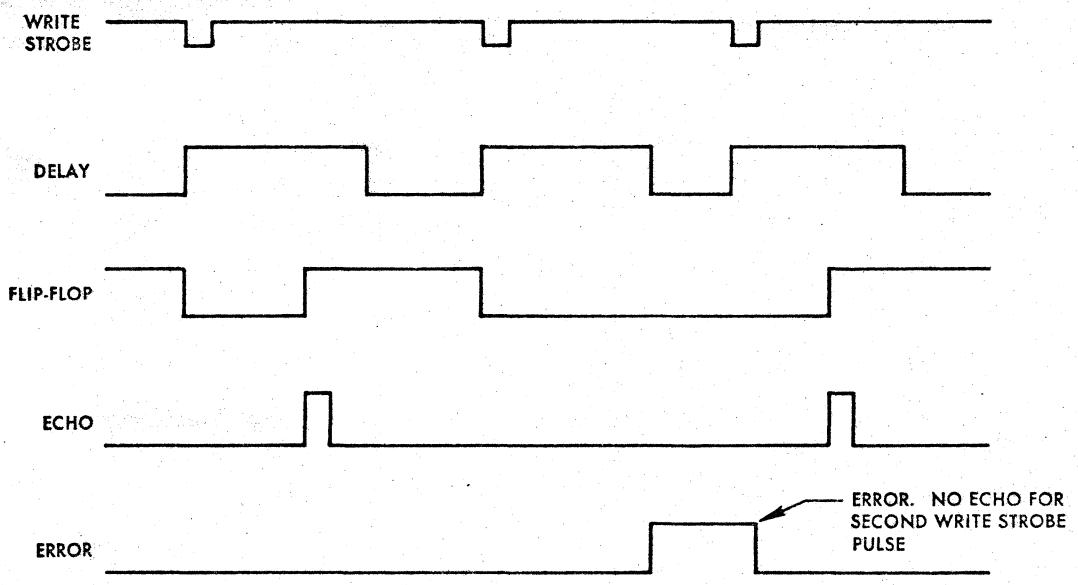


Figure 4-7
Echo Check Timing

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

This section contains adjustment procedures and troubleshooting techniques for the Data Electronics. Tape Transport maintenance is included in the Tape Transport manual.

5-2. TEST EQUIPMENT.

Table 5-1 lists the required test equipment.

TABLE 5-1
REQUIRED TEST EQUIPMENT

EQUIPMENT	RECOMMENDED TYPE OR EQUIVALENT
Digital Voltmeter (DVM)	Digitek 202-B
Master Tape	IBM
Oscilloscope	Tektronix 535
Preamplifier	Tektronix CA
Square Wave Generator	Hewlett-Packard HP-211

5-3. ADJUSTMENT PROCEDURE.

5-4. GENERAL.

Note that adjustments are made by Ampex prior to the shipment of equipment. Verify adjustments when components are either interchanged or replaced. If adjustments are to be made off line, use Alternate Adjustment Procedure. (Refer to paragraph 5-14.)

CAUTION

An insulated-blade screwdriver is recommended for making adjustments to prevent accidental shorting of electrical components.

5-5. SEQUENCE OF ADJUSTMENTS.

Tape transport and power supply adjustments must be verified before Data Electronics adjustments are made. Data Electronics adjustments shall be made in the following sequence.

1. Clipping Level
2. Preliminary Read Amplifier
3. Read Deskew
4. Write Check
5. Read Amplifier
6. Write Deskew
7. Read Strobe
8. Rate Error

5-6. Clipping Level. The bias setting adjustment on the Strobe Generator card determines the clipping level. In the Read Only Mode, the clipping level is at 20 percent. In the Write Check Mode, the clipping level adjustment is at 40 percent. These percentages refer to the base-to-peak amplitude of the signal into the peak detector.

Step 1: Connect voltmeter negative lead to pin B8-32, positive lead to TS1-3 (-6 volts).

Step 2: With power ON, select Remote Mode at the Operator Control Panel (OCP). When the REMOTE switch indicator illuminates, the system is ready for operation. Set Write Permit input to the TRUE level. Adjust potentiometer R9 on the Strobe Generator card (B8) to obtain a reading of 1.4 volts on the voltmeter. (See Figure 5-1.)

Step 3: Set Write Permit input to the FALSE level. Adjust potentiometer R10 on B8 for 0.6 volt on the voltmeter.

5-7. Preliminary Read Amplifier. The Preliminary Read Amplifier adjustment is made using an IBM master tape. A preliminary check of the read amplifier is necessary to ensure sufficient signal is available to properly operate the read deskew amplifier during read deskew adjustments.

CAUTION

Write power must be disabled to prevent accidental erasure of the master tape.

Step 1: Load the master tape without the write enable ring in place. Verify that the FILE PROTECT indicator is illuminated.

Step 2: Connect the oscilloscope vertical input to pin 12 of the track 1 read deskew amplifier (A2). Position the horizontal sweep to 50 μsec/cm.

Step 3: Run the tape forward. The peak-to-peak voltage indicated on the oscilloscope must be 6 to 8 volts. Adjust potentiometer R11 on the read amplifier board if necessary. (Refer to Table 5-3.)

Step 4: Repeat the procedure outlined in Steps 2 and 3 for each of the remaining tracks.

5-8. Read Deskew. The Read Deskew adjustment is made by using the center track as a reference and comparing the track under test with it. The skew correction is accomplished by varying the delay time of a single-shot; the potentiometer of the single-shot is on the Read Deskew board. (See Figure 5-2 and Table 5-2.)

Step 1: Position the potentiometer (R25) on the center track Read Deskew board to its center. (Turn the adjusting screw clockwise until the end of its adjustment is reached, back off the adjusting screw twelve and one-half revolutions.)

Step 2: Connect the oscilloscope inputs A and external sync (-) to pin 34 of the center track (track 4 or track 5). Connect input B to pin 34 of track 1 (A2). Set the oscilloscope controls; Vertical inputs DC, Vertical deflection 2 volts/cm, MODE alternate. Adjust the sweep until a single pulse is displayed over 4 to 6 cm.

Step 3: Load an IBM master tape on the transport and run the tape forward. Adjust potentiometer R25 on Read Deskew A2 until the trailing edge of waveform B most nearly coincides with the trailing edge of waveform A.

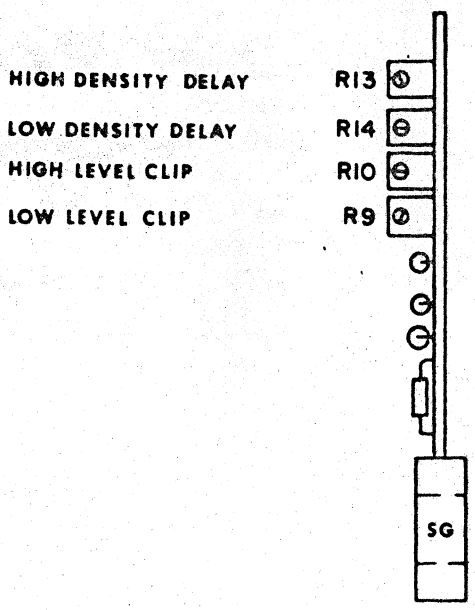


Figure 5-1
Clip Level and Strobe Delay Potentiometers

TABLE 5-2
READ DESKEW PCB

TRACK	LOCATION
1	A2
2	A3
3	A4
4	A5
5	A6
6	A7
7	A8
8	A9*
9	A10*

*9 track system only

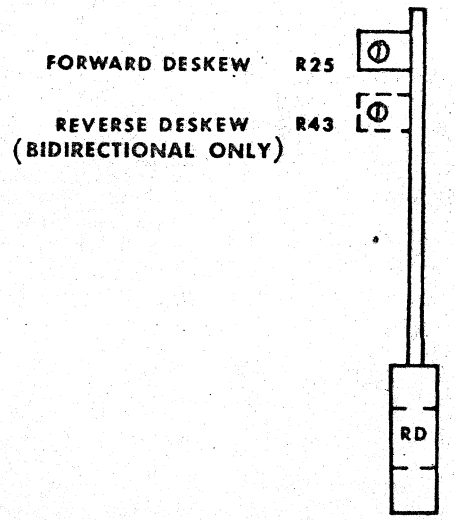


Figure 5-2
Read Deskew Potentiometers

Step 4: Repeat Steps 2 and 3 for each of the remaining tracks.

Step 5: Remove the master tape.

NOTE

When the bidirectional read deskew operation is taken, repeat Steps 1 through 4. To adjust reverse deskew, read the tape in reverse and adjust potentiometer R43 only.

5-9. Write Check. The Write Check procedures are performed with the system performing the write and read function. The write permit and read permit levels must be set TRUE and the transport placed in the Remote Mode of operation. Select high density on the OCP. Verify that the write operation is being performed by checking the write amplifiers.

Step 1: Install the write enable ring. Load a scratch-pad tape on the transport. Set the Write Permit and Read Permit inputs TRUE. Write all ONEs at the high density rate.

Step 2: Connect the oscilloscope input to pin 34 of track 1 of the write amplifier (A-14). A voltage spike of approximately 10 volts should occur for every other current transition through the write head. Repeat for pin 30.

Step 3: Repeat the procedure of Step 2 for the remaining tracks.

5-10. Read Amplifier.

Step 1: Continue to write all ONEs. Connect the oscilloscope input to pin 12 of the read amplifier deskews. (Refer to Table 5-3.)

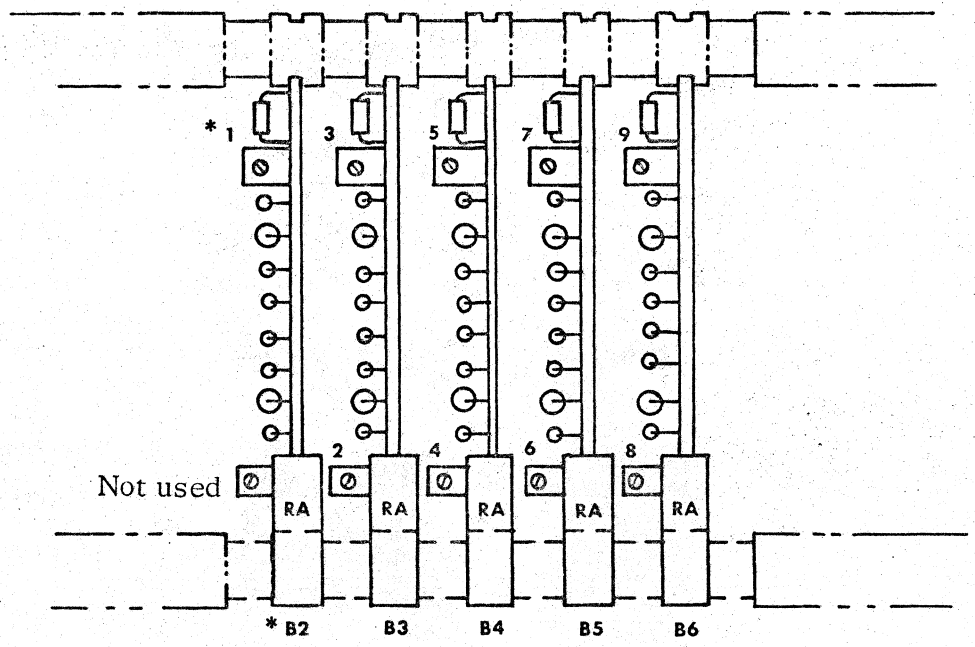
Step 2: Adjust the associated read amplifier gain potentiometer for 8 volts peak-to-peak as indicated on the oscilloscope. (See Figure 5-3.)

Step 3: Repeat the above procedure for the remaining channels.

TABLE 5-3
READ AMPLIFIER ADJUSTMENTS

TRACK	*OSCILLOSCOPE CONNECTION	POTENTIOMETER LOCATION
1	A2-12	B2 Upper
2	A3-12	B3 Lower
3	A4-12	B3 Upper
4	A5-12	B4 Lower
5	A6-12	B4 Upper
6	A7-12	B5 Lower
7	A8-12	B5 Upper
8	A9-12	B6 Lower
9	A10-12	B6 Upper

*Read Amplifier adjustments are observed on Read Deskew PCBs.



*Read Track and PCB Designations for Reference Only

Figure 5-3
Read Amplifier Adjustments

5-11. Write Deskew. Write Deskew adjustment is made by comparing the center track output of the Read Deskew with each of the remaining tracks. The Read Deskew adjustment described in paragraph 5-8 shall have been performed before this adjustment is attempted.

Step 1: Connect oscilloscope inputs A and external sync (-) to pin 34 of the center track read deskew. Connect input B to pin 34 of the track 1 deskew. Set the Horizontal sweep so that a single pulse is displayed over 4 to 6 cm. Set the Vertical MODE to alternate sweeps, Vertical sensitivity to 2 volts/cm.

Step 2: Adjust potentiometer R1 on the center track Write Deskew board (Figure 5-4) to its center position. (Turn the adjusting screw clockwise to the end of its travel, back off twelve and one-half revolutions.)

Step 3: Adjust potentiometer R1 on track 1 Write Deskew until the trailing edge of waveform B most nearly coincides with the trailing edge of waveform A.

Step 4: Repeat the above procedure for each of the remaining tracks. (Refer to Table 5-4.)

TABLE 5-4
WRITE DESKEW PCB

TRACK	LOCATION
1	A2
2	A3
3	A4
4	A5
5	A6
6	A7
7	A8
8	A9*
9	A10*

*9 track system only

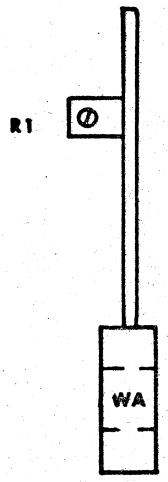


Figure 5-4
Write Deskew Potentiometer

5-12. Read Strobe. The Strobe Generator is adjusted for the proper delay time while writing all ONEs at the required data transfer rate. Table 5-5 lists bit densities and the associated adjustment. See Figure 5-1 for potentiometer location on the PCB.

Step 1: Connect the oscilloscope inputs A and external sync (-) to pin 10, input B to pin 24 of the Strobe Generator (B8). Select high density at OCP.

Step 2: Run the tape forward while writing all ONEs. Adjust potentiometer R13 (B8) for proper delay time. (Refer to Table 5-5 and Figure 5-1.)

Step 3: Select low density input at OCP. Adjust potentiometer R14 for designated delay time. (Refer to Table 5-5 and Figure 5-1.)

TABLE 5-5
READ STROBE ADJUSTMENT

DENSITY	36 IPS	75 IPS	112.5 IPS	120 IPS	150 IPS
200 cpi	69 μsec	33 μsec	22 μsec	20 μsec	16.7 μsec
556 cpi	25 μsec	12 μsec	8 μsec	7 μsec	6 μsec
800 cpi	17 μsec	8 μsec	5.5 μsec	5.2 μsec	4 μsec

5-13. Rate Error. The Error Check PCB is located at B12. The potentiometer controlling the delay time is located on the PCB.

Step 1: Connect input A and the external sync inputs of the oscilloscope to pin 23 of B12. Connect input B to pin 27.

Step 2: Select high density input at the OCP. Write all ONEs. Adjust potentiometer R12 until the trailing edge of the pulse on channel B is delayed from the leading edge of the channel A display by the amount determined from Table 5-6.

TABLE 5-6
RATE ERROR DELAY

DENSITY	36 IPS	75 IPS	112.5 IPS	120 IPS	150 IPS
800 cpi	34 μsec	16 μsec	11 μsec	10 μsec	8 μsec
556 cpi	23 μsec	11 μsec	7.4 μsec	6.9 μsec	5.5 μsec

5-14. ALTERNATE ADJUSTMENT PROCEDURE.

The alternate adjustment procedure may be used to make off-line adjustments. The tape transport must be in the LOCAL mode when making off-line adjustments.

5-15. GENERAL.

The output of a square-wave generator may be applied to test points TP1 and TP2 (TP2 is ground) to write a series of ONEs on all tracks. Verify transport and power supply adjustments. Sequence of off-line adjustments are the same as listed in paragraph 5-5.

CAUTION

To prevent accidental damage to external equipment, disconnect the input at connector J5 of the Data Electronics.

5-16. Clipping Level. The Clipping Level is adjusted in the manner described in paragraph 5-6. The Input Buffer PCB at B16 is extracted from B16 to simulate a Write Permit TRUE signal.

5-17. Read Deskew. The Read Deskew adjustments are as described in paragraph 5-8. For a Read Forward only system, ensure that -12 volts (TRUE) is at pin 21 of the Read Deskew PCB. For bidirectional Read Deskew, connect -12 volts to pin 26 of J5 on the Data Electronics before performing Forward Deskew adjustment. For Reverse Deskew adjustment, remove the -12 volts from pin 26 of J5 and connect 0 volts to pin 26.

CAUTION

Ensure that the square-wave generator is terminated with the correct load resistance.

5-18. Write Check. The Read-after-Write Check and Read Amplifier and Write Deskew adjustments are made in the manner described in paragraphs 5-9, 5-10, and 5-11 with the following exceptions.

Connect a square-wave generator to TP1 and TP2 on the Data Electronics assembly. Simulate Write Permit and Run/Stop TRUE by removing the Input Buffer PCB from B16. Set the frequency of the square-wave generator according to Table 5-6. Adjust the output amplitude for 0 to -12 volts. For a bidirectional read system, connect -12 volts to pin 26 of J5 on the Data Electronics.

5-19. Read Strobe, Rate Error. The Read Strobe and Rate Error adjustments are made in the manner described in paragraphs 5-12 and 5-13 with the following exceptions. The square-wave generator is connected as described in paragraph 5-18. The generator frequencies required to simulate the bit density are listed in Table 5-7.

TABLE 5-7
TEST DESKEW INPUT REQUIREMENT
(SYSTEM DATA TRANSFER RATE)

DENSITY	36 IPS	75 IPS	112.5 IPS	120 IPS	150 IPS
200 cpi	7.2 kc	15 kc	22.5 kc	24 kc	30 kc
556 cpi	20 kc	41.7 kc	62.5 kc	66 kc	83.4 kc
800 cpi	27.8 kc	60 kc	90 kc	96 kc	120 kc

5-20. TROUBLESHOOTING PROCEDURE.

The Data Electronics circuits are on plug-in type printed circuits boards (PCBs). The troubleshooting charts, Tables 5-9 and 5-10, facilitate the isolation of the malfunctioning PCB. The location and function of each PCB is shown in Figure 2-1.

The Theory of Operation in Section IV, the Printed Circuit Descriptions in Section VI, and the logic diagram in Section VII provide the information required for more extensive troubleshooting.

Check the equipment for evidence of damage, that no wires are disconnected and that the PCBs are firmly seated in their proper location.

5-21. PRELIMINARY TESTS.

Establish that the input signals controlling the Data Electronics are as required. Table 5-8 lists the input function, the signal requirement and the test point. These tests are made at the output of the buffer amplifiers. Should the input signals not be as required, the possibility of a malfunctioning Input Buffer card exists. A check may be made by exchanging the card in B16 with B15. Use an oscilloscope to make all tests. Refer to the logic diagram in Section VII while performing all tests.

A write operation cannot be performed unless at least one Write Data input line is TRUE. The input data may be coincident with the Write Strobe pulse or may be held in the TRUE condition by a continuous -9 to -25 volt level. Removing Input Buffer board B15 will have the effect of conditioning tracks 1 through 8 to write all ONEs.

To determine that the write operation is being performed, connect the oscilloscope input lead to pin 24 of any Write Amplifier board, A14 through A22. A 10-volt spike should be present. The repetition rate is a function of the Write Strobe.

The read function is controlled by the read permit level and the strobe generator. Should no data output be present, determine if data is being read by any of the read tracks by checking the OR clock line at the Strobe Generator (B8-10). A negative-going pulse should be observed. The repetition rate will be determined by the data transfer frequency. Should the test confirm that data is being read by the read heads, but no data is being presented to the outputs, investigate the condition of read permit line at pin 9 of the write power gate (A24). The level of read permit at this point must be 0 volts. Should the level not be 0 volts, replace the write power gate. The read strobe and the AC register reset pulses must be present at pins 24 and 22, the read strobe pulse is positive-going, the reset pulse is the inverse of the strobe pulse. Should the signals not be as indicated in the preceding test, replace strobe generator B8.

TABLE 5-8
INPUT SIGNALS

INPUT FUNCTION	TEST POINT	SIGNAL
Write Reset	B16-14	0V
Write Permit	B16-20	-12V
Write Strobe	B16-22	-12V pulses
Read Permit	B16-26	-12V
Run/Stop (or Fwd/Stop)	B16-28	-12V

5-22. TROUBLESHOOTING TABLES.

Troubleshooting Tables 5-9 and 5-10 may be used as a guide to further investigate any malfunction existing in the Data Electronics.

TABLE 5-9
WRITE SECTION TROUBLESHOOTING PROCEDURE

MALFUNCTION	FAILURE INDICATION	REMEDY
1. No head driver output on any track as measured at pins 30 and 34 of PCBs A14 through A22	A. Input Buffer output at B16-20 is at 0 volts	Replace PCB B16
	B. Output of Write Power Gate at pins A24-28, 29, and 30 is at 0 volts	Verify that Write Enable Ring is in place. If ring is in place and the malfunction still exists, replace PCB A24
	C. Write Register Reset output at B8-30 is +12 volts when Write Permit at B8-28 and Run at B8-20 are at -6 to -12 volts	Replace PCB B8
	D. Either a constant 0 volts or a constant -12 volts Write Strobe signal at B16-22	Replace PCB B16
2. No head driver output on a particular track as measured at pins 30 and 34 of PCBs A14 through A22	A. Write Data output from the input buffer of the malfunctioning track remains at 0 volts when ONEs are being written on that track	Replace the PCB corresponding to the malfunctioning track
	B. Input to the Write Amplifier is negative and the Write Strobe is present, but no output at pins 30 and 34 of the Write Amplifier	Replace Write Amplifier PCB associated with the malfunctioning track (A14 through A22)

TABLE 5-10
READ SECTION TROUBLESHOOTING PROCEDURE

MALFUNCTION	FAILURE INDICATION	REMEDY
1. No output on any track as measured at the output of the output drivers	A. Read Permit output at B16 is 0 ±0.5 volts	Replace PCB B16
	B. Read Register DC Reset at A24-9 is at -6 volts	Replace PCB A24
	C. OR Data input at B8-10 remains at a constant -6 volts	One of the Read Deskew Boards A2 through A10 is malfunctioning. Replace malfunctioning PCB.
	D. Read Permit is negative at B8-12 and an OR Data signal is present at B8-10 but no Read Strobe pulse at B8-24 or no Read Register Reset output at B8-22	Replace PCB B8
	E. Read Amplifier output of 6 to 8 volts peak-to-peak at pins 12 and 14 of A2 through A10 but no OR Data output at pin 35 of A2 through A10. Clipping Level input at pins 24 of A2 through A10 at -10 volts or greater	Decrease clipping level (refer to paragraph 5-6). If clipping level will not decrease, replace PCB B8
	F. No Read Register Reset output at B8-22 or no Read Strobe at B8-24 when OR data is present at B8-10. Both High and Low Density Select at B8-34 and B9-35 are at a voltage other than -12 volts	Replace PCB A24.

TABLE 5-10
READ SECTION TROUBLESHOOTING PROCEDURE
(Continued)

MALFUNCTION	FAILURE INDICATION	REMEDY
2. No output from a particular track at the output of the Output Driver	A. No Read Amplifier output at pins 12 and 14 of the Read Deskew boards of the malfunctioning track	Adjust Read Amplifier of malfunctioning track. (Refer to paragraph 5-7.) If malfunction is not corrected, replace Read Amplifier board and adjust. If malfunction still exists, replace Read Deskew board of malfunctioning track
	B. No output at pin 32 of the Read Deskew board of the malfunctioning track, but 6 to 8 volts peak-to-peak measured at pins 12 and 14 of that PCB	Replace Read Deskew PCB of the malfunctioning track
	C. No output signal from the output driver of the malfunctioning track even though both inputs to the output driver are TRUE	Replace PCB B13 or B14

SECTION VI
CIRCUIT DESCRIPTIONS

6-1. INTRODUCTION.

This section contains circuit descriptions of the printed circuit board assemblies. The descriptions are in alphabetical order as shown on Table 6-1. Schematics and assembly drawings are located in Section VII.

TABLE 6-1
LIST OF CIRCUIT DESCRIPTIONS

CIRCUIT DESCRIPTION	SCHEMATIC
Error Check	3109873
Exclusive OR	3104452
Input Buffer	3107038
Output Driver	3107043
Read Amplifier	3107118
Read Deskew	3107253
Read Deskew, Bidirectional	3109930
Select Logic	3111158
Strobe Generator	3107058
Write Amplifier	3112345
Write Power Gate	3107128

1. GENERAL DESCRIPTION.

This card contains the circuits required to perform the Write Check function.

2. THEORY OF OPERATION.

The Write Check function checks the read-after-write data for Parity, Rate and Echo errors. The outputs of the Parity, Rate and Echo check circuits are ORed together such that a Write Check error is generated at the card output if either a Parity, Rate or Echo error is generated.

Parity. The Parity input is ANDed with the Read Register Reset by the AND gate made up of R17 and CR10. The Read Register Reset pulse occurs simultaneously with the Read Clock. The output of the AND gate drives diode CR13, which is an input to the OR gate driving Q6.

Rate Check. The Rate Check circuit checks the period between successive Read Register Reset pulses and generates an output from the AND gate made up of CR11, CR12, and R18 whenever the period between Reset pulses decreases beyond an adjustable threshold. The Rate circuit operates as follows.

A negative Register Reset pulse turns Q1 ON, forcing the single-shot SS-1 (Q2 and Q3) to trigger. At the end of single-shot SS-1's delay, the single-shot SS-2 (Q4 and Q5) is set. The output of SS-2 is ANDed with the next arriving Register Reset pulse. The sum of the delays of SS-1 and SS-2 is adjusted by potentiometer R12 to give a total delay of 0.67 (1/upper Data Transfer frequency). Under normal conditions the next arriving Register Reset pulse will not coincide with the output of SS-2 and the AND gate will give no output. If the tape speed was slow at the time of writing such that the distance between frames was decreased to 0.67 (normal frame time) or less, then coincidence will occur at the AND gate and a Rate Error will be indicated.

Echo Check. The Echo Check circuit verifies that at least one Head Driver changes state after each Write Strobe. The Echo Check circuit operates as follows.

The flip-flop made up of transistors Q16 and Q17 is held reset at all times that the Write Amplifiers are reset. This is done by the Write Register DC Reset input at pin 19. When writing, the Write Register DC Reset is FALSE and the flip-flop is no longer forced reset. The Write Strobe input at pin 11 causes the single-shot (SS-3), made up of Q10 and

2. THEORY OF OPERATION. (Continued)

Q11 to trigger. The output of SS-3 is inverted by the inverter made up by Q12. The flip-flop is set by the single-shot at the moment that the single-shot triggers. The input to the AND gate at CR26 is held FALSE for the duration of the delay of SS-3.

The Echo outputs from the Write Amplifiers arrive at pin 15 before the delay of SS-3 ends, and the first arriving Echo resets the flip-flop. If there is no Echo input after a Write Strobe, the flip-flop remains set and at the end of the delay of SS-3, the flip-flop output coincides with the output of the inverter, made up of Q12, and an Echo Error output is generated by the AND gate.

OR Gate. The outputs from the Parity, Rate and Echo AND gates drive the OR gate made up of CR13, CR14, and CR29. This gate drives the circuit made up of Q6 and Q7 which limits the duration of the Write Check Error output pulse. Resistor R24 and diode CR16 make up an AND gate ANDing the Write Permit with the Write Check Error output. Q8 makes up the inverter that repowers the Write Check output.

3. OPERATIONAL CHARACTERISTICS.

FUNCTION	UP LEVEL	DOWN LEVEL
Write Permit	0 ±0.5 volt	-12 volts
Parity	0 ±0.5 volt	-12 volts
Read Register Reset	0 ±0.5 volt	-6 volts most positive
Write Strobe	0 ±0.5 volt	-6 volts
Write Register DC Reset	+12 volts	Open circuit
Echo	+5 volt transition	
Write Check Error	0 ±0.5 volt	-12 volts

4. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	20 ma
-12 VDC ±3%	78 ma
- 6 VDC ±4%	16 ma

1. GENERAL DESCRIPTION.

This card contains four independent logic elements. Two of the elements require external termination. Each element performs an Exclusive OR function. Electrically, the output assumes UP level only when the polarities of the two inputs are dissimilar.

2. TRUTH TABLE.

INPUT 1	INPUT 2	OUTPUT
-6	-6	-6
-6	0	0
0	-6	0
0	0	-6

3. THEORY OF OPERATION.

Diodes CR1 and CR2 comprise an OR gate. Diodes CR3 and CR4 comprise an AND gate. Transistors Q1 and Q2 are inverters.

Two 0 volt inputs forward bias CR1 and CR2 which conduct and place a positive voltage on the base of Q1 (with respect to the emitter), causing Q1 to cut off. Diodes CR3 and CR4 are back biased and 0 volt appears at the anode of CR6. With Q1 cut off, CR6 is forward biased and conducts, placing 0 volt on the base of Q2. Transistor Q2 is cut off and -6 volts appears at the output.

Zero volt at Input 1 and -6 volts at Input 2 will cause the following sequence of events. Diode CR1 is forward biased and conducts, causing CR2 to be back biased, placing 0 volt on the base of Q1 and causing Q1 to cut off. Diode CR4 is forward biased and conducts, causing CR3 to be back biased and placing -6 volts on the anode of CR6. With Q1 cut off, CR6 is forward biased and conducts, placing -6 volts on the base of Q2. Transistor Q2 conducts and 0 volt appears at the output. When the input voltages are reverse, (-6 volts at Input 1 and 0 volt at Input 2), the circuit action is the same except that diodes CR2 and CR3 conduct and CR1 and CR4 are cut off.

Two -6 volt inputs reverse bias CR1 and CR2 which drives the base of Q1 negative and Q1 conducts. Diodes CR3 and CR4 are forward biased and conduct, placing -6 volts on the anode of CR6. With Q1 conducting and CR6 back biased, the base of Q2 goes positive. Transistor Q2 cuts off and -6 volts appears at the output.

4. OPERATIONAL CHARACTERISTICS

FUNCTION	INPUT		OUTPUT	
	UP LEVEL	DOWN LEVEL	UP LEVEL	DOWN LEVEL
Voltage	0.0V to -0.5V	-5V to -13V	0.0V to 0.5V	-5.7V to -6.7V
Current	5.4 ma max	1 ma max at -6.3V	13.5 ma max	1 ma max
Rise Time			150 ns max*	
Fall Time			1100 ns max*	
Delay	750 ns max** Signal Propagation Delay			

*With 220 pf load returned to ground or 390 pf returned to ground in parallel with 430 ohms returned to -6 volts.

**Total delay of 4 circuits in series.

5. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	11 ma max
-12 VDC ±3%	60 ma max
- 6 VDC ±4%	6.8 ma max

1. GENERAL DESCRIPTION.

This card contains eight identical, independent input buffer circuits. Each circuit provides a non-inverted output and has an input noise rejection of approximately 5 volts.

2. THEORY OF OPERATION.

With 0 volt input, Q1 conducts and -6 volts appears at the collector of Q1. Q2 is driven into saturation by base current via R4. With Q2 conducting, the output is zero.

With -12 volts input, Q1 is reverse biased and cut off. The base of Q2, through R4, goes positive, driving Q2 to cutoff. With Q2 cut off, the output is -12 volts.

3. OPERATIONAL CHARACTERISTICS.

FUNCTION	INPUT		OUTPUT	
	HIGH LEVEL	LOW LEVEL	HIGH LEVEL	LOW LEVEL
Voltage	0.00 ±1.25V	-12 ±12V	0.5V max	-12V thru 2.7K ±10%
Current	2.6 ma max	4.7 ma max	30 ma max	-12V thru 2.7K ±10%
Rise Time			100 ns max	
Fall Time			500 ns max	

4. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	+40 ma max
-12 VDC ±3%	-40 ma max
- 6 VDC ±4%	+56 to -19 ma max

1. GENERAL DESCRIPTION.

Eight identical output driver circuits are mounted on this card. Each circuit provides a two-way gating function.

2. TRUTH TABLE.

INPUT 1	INPUT 2	OUTPUT
HIGH	HIGH	LOW
HIGH	LOW	HIGH
LOW	HIGH	HIGH
LOW	LOW	HIGH

3. THEORY OF OPERATION.

During the following discussion, a 2K output load is assumed. When both inputs are at the high level of zero volts, the input to the base of Q1 becomes positive. Q1 is cut off. When Q1 cuts off, the base of Q2 goes negative. Q2 conducts and functions as an emitter follower until the output reaches approximately -12 volts.

When either one or both inputs are at the low level of -6 volts, the input to the base of Q1 goes negative and Q1 conducts. The base of Q2 goes positive with respect to emitter of Q2 and Q2 cuts off. The output is zero volts.

4. OPERATIONAL CHARACTERISTICS.

FUNCTION	INPUT		OUTPUT	
	HIGH LEVEL	LOW LEVEL	HIGH LEVEL	LOW LEVEL
Voltage	0V to -1V	-5V to -12V	0V to -1V	-12 ±2V
Current	350 μa max	1.5 ma max at -6V	5 ma max	5 ma max

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	5.5 ma max
-12 VDC ±3%	55.0 ma max

1. GENERAL DESCRIPTION.

This card contains two independent and identical circuits. Each circuit is a three-stage, variable gain, linear differential preamplifier.

2. THEORY OF OPERATION.

The inputs to the differential preamplifiers are direct coupled to the Read Heads. The first stage, made up of Q1 and Q2, is a typical differential amplifier. The collectors of Q1 and Q2 are capacitively coupled to the second differential stage, made up of Q3 and Q4. A gain potentiometer, R11, is connected between the collectors of Q3 and Q4 to provide a variable gain adjustment. The second state output is capacitively coupled to the third stage made up of Q5 and Q6. Third stage output of Circuit Number 1 appears at pins 14 and 16. Output of Circuit Number 2 appears at pins 22 and 24.

The differential input impedance is from 7K minimum to 15K maximum across the input terminals. Input voltages are from 12 mv to 24 mv peak-to-peak differentially.

To measure gain, band pass, and output amplitude, the Read Amplifier board must be loaded with the Read Deskew board, assembly 3107252-10. Gain is 310 minimum at the maximum setting of potentiometer R11. Band pass is from 90 cps minimum to 35KC maximum with gain set to maximum. The output amplitude is 3.7 volts peak-to-peak minimum without limiting.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	10 ma max
-12 VDC ±3%	10 ma max

1. GENERAL DESCRIPTION.

This card contains one stage of a differential amplifier, a clipping circuit, a peak detector, a deskew single-shot, and a skew register flip-flop.

2. THEORY OF OPERATION.

The differential input from pins 8 and 10 is applied to the differential amplifier made up of Q1 and Q2. The output of the amplifier is summed with the Clipping Bias input from pin 16, and appears at the bases of Q3 and Q4. Q3 and Q4 form a full-wave rectifier with power gain. The amplitude of the Rectifier output is a function of the Clipping Bias input and appears at the base of emitter follower Q5. Q5 is directly coupled to Q6 and Q7. When the input to Q5 goes positive, Q5 drives the bases of Q6 and Q7 positive. Q6 conducts, charging capacitor C11, and Q7 cuts off. Capacitor C11 reaches maximum charge at the peak of the input waveform at the base of Q6. Following the peak of the waveform, the voltage begins to drop. C11 is charged to the peak voltage and holds the emitter of Q6 to that level. When the voltage at the base of Q6 drops, the base-emitter junction becomes back biased and Q6 cuts off. At the moment Q6 cuts off, the collector of Q6 goes positive, turning on emitter follower Q8. As input to the base of Q7 drops, Q7 begins to conduct and fully discharges C11 when the input waveform reaches zero. The circuit is then prepared for the next positive-going signal. When Q8 conducts, Q9 also conducts, causing Q10 to conduct. When Q10 conducts, a positive signal is fed via CR4 and C12 into the single-shot made up of Q11 and Q12. The output of the single-shot goes negative for the duration of its time delay. The single-shot time delay is dependent on the RC network of C13, R25, and R26. At the end of the time delay, the collector of Q12 goes positive, causing Q13 to conduct. The collector of Q13 goes negative, generating an OR Clock output at pin 35. At the time the collector of Q12 goes positive, the read register flip-flop made up of Q14 and Q15 is set. The flip-flop is later AC reset by a positive-going pulse from AC Reset input, pin 24. The flip-flop may also be forced to reset by a Skew Register DC Reset input from pin 26 through R37. The flip-flop output appears at pins 30 and 32.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	16 ma max
-12 VDC ±3%	40 ma max
- 6 VDC ±4%	80 ma max

1. GENERAL DESCRIPTION.

This card contains one stage of a differential amplifier, a Clipping circuit, a peak detector, a deskew single-shot, and a skew register flip-flop. The deskew single-shot provides two adjustable deskew delays, which are selected by applying +12 volts at one of two inputs.

2. THEORY OF OPERATION.

The Differential input from pins 8 and 10 is applied to the differential amplifier made up of Q1 and Q2. The output of the amplifier is summed with the Clipping Bias input from pin 16, and appears at the bases of Q3 and Q4. Q3 and Q4 form a full-wave rectifier with power gain. The amplitude of the Rectifier output is a function of the Clipping Bias input and appears at the base of emitter follower Q5. Q5 is directly coupled to Q6 and Q7. When the input to Q5 goes positive, Q5 drives the bases of Q6 and Q7 positive. Q6 conducts, charging capacitor C11, and Q7 cuts off. Capacitor C11 reaches maximum charge at the peak of the input waveform at the base of Q6. Following the peak of the waveform, the voltage begins to drop. C11 is charged to the peak voltage and holds the emitter of Q6 to that level. When the voltage at the base of Q6 drops, the base-emitter junction becomes back biased and Q6 cuts off. At the moment Q6 cuts off, the collector of Q6 goes positive, turning on emitter follower Q8. As input to the base of Q7 drops, Q7 begins to conduct and fully discharges C11 when the input waveform reaches zero. The circuit is then prepared for the next positive-going signal. When Q8 conducts, Q9 also conducts, causing Q10 to conduct. When Q10 conducts, a positive signal is fed via CR4 and C12 into the single-shot made up of Q11 and Q12 The output of the single-shot goes negative for the duration of its time delay. The single-shot time delay is dependent on the RC network of C13, R25, and R26 when -12 volts is applied at pin 21, or C13, R43 and R26 when -12 volts is applied at pin 20. Diodes CR16 and CR17 isolate the two inputs. At the end of the time delay, the collector of Q12 goes positive, causing Q13 to conduct. The collector of Q13 goes negative, generating an OR Clock output at pin 35. At the time the collector of Q12 goes positive, the read register flip-flop made up of Q14 and Q15 is set. The flip-flop is later AC reset by a positive-going pulse from AC Reset input, pin 24. The flip-flop may also be forced to reset by a Skew Register DC Reset input from pin 26 through R37. The flip-flop output appears at pins 30 and 32.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	16 ma max
-12 VDC ±3%	40 ma max
- 6 VDC ±4%	80 ma max

1. GENERAL DESCRIPTION.

This card contains six independent circuits as follows: two Input Buffers, one Output Driver, one Inverter, one Hi/Lo Density Select Driver, and one Deskew and Amplifier Select Driver.

2. THEORY OF OPERATION.

Input Buffers. The input to Buffer #1 is at pin 12 and the output is at pin 15. The input to Buffer #2 is at pin 13 and the output is at pin 16. The Input Buffer circuits are identical. Only Input Buffer #1 is described.

With 0 volts input, Q5 conducts and -6 volts appears at the collector of Q5. Q6 is driven into saturation by base current via R14. With Q6 conducting, the output is zero.

With -12 volts input, Q5 is reverse biased and cuts off. The base of Q6, through R14, goes positive, driving Q6 to cutoff. With Q6 cut off, the output is -12 volts.

Output Driver. The Output Driver circuit has two inputs at pins 18 and 19, and an output at pin 17. The theory of operation is as follows.

During the following discussion, a 2K output load is assumed. When both inputs are at the high level of zero volts, the input to the base of Q14 becomes positive. Q14 is cut off. When Q14 cuts off, the base of Q15 goes negative. Q15 conducts and functions as an emitter follower until the output reaches approximately -12 volts.

When either one or both inputs are at the low level of -6 volts, the input to the base of Q14 goes negative and Q14 conducts. The base of Q15 goes positive with respect to emitter of Q15 and Q15 cuts off. Output is zero volts.

Inverter. The Inverter circuit has an input at pin 9 and an output at pin 10. The theory of operation is as follows.

When Read Permit input is -12 volts, Q9 is biased to cutoff and the output is 0 volts. When Read Permit input is 0 volts, Q9 is conducting and the output is -6 volts.

2. THEORY OF OPERATION. (Continued)

Density Select Driver. The Density Select Driver input is at pin 25 and the outputs are at pins 21 and 23. The theory of operation is as follows.

The Density Select Driver input is controlled by a pushbutton on the OCP. When the input at pin 25 is 0 volts (Low Density), Q10 and Q11 are cut off. High Density output at pin 23 is open circuit. Q12 and Q13 are conducting and Low Density output at pin 21 is -12 volts.

When the input at pin 25 is -12 volts (High Density), Q10 and Q11 are conducting. High Density output at pin 23 is -12 volts. Q12 and Q13 are cut off and Low Density output at pin 21 is open circuit.

Deskew and Amplifier Select Driver. The Deskew and Amplifier Select Driver input is at pin 27 and the Deskew Select outputs are at pins 29 and 31, and Amplifier Select outputs are at pins 32 and 33.

The theory of operation is as follows. An input of -12 volts causes Q1 and Q2 to conduct and Q3 and Q4 to cut off. When Q2 is conducting, the outputs at pins 31 and 32 are driven to approximately -12 volts by transistor Q2.

When Q4 is cut off, the output at pin 29 goes to +12 volts and the output at pin 33 is isolated from pin 29 by back biased diode CR5.

An input of 0 volts causes Q1 and Q2 to cut off and Q3 and Q4 to conduct. When Q4 is conducting, the outputs at pins 29 and 33 are driven to approximately -12 volts by transistor Q4. The output at pin 31 goes to +12 volts and the output at pin 32 is isolated from pin 31 by back biased diode CR2.

3. OPERATIONAL CHARACTERISTICS.

CIRCUIT	PARAMETER	INPUT		OUTPUT	
		HIGH LEVEL	LOW LEVEL	HIGH LEVEL	LOW LEVEL
Input Buffer	Voltage	0.00 ±1.25V	-12 ±2V	0.5V max	-12V thru 2.7K ±10%
	Current	2.6 ma max	4.7 ma max	30 ma max	-12V thru 2.7K ±10%
	Rise Time	100 ns		100 ns	
	Fall Time		100 ns		500 ns max
Output Driver	Voltage	0V to -1V	-5V to -12V	0V to -1V	-12 ±2V
	Current	350 μa max	1.5 ma max at -6 volts	5 ma max	5 ma max
Density Select	Voltage	-0.5V most negative	-5.5V least negative	0.3V more positive than -12V supply	Open circuit
Read Permit	Voltage	-0.5V most negative	-5.5V least negative	+0.5V max	-6.0 ±0.5V
Deskew & Amplifier Select	Voltage Deskew	0.00 ±1.25V	-9V to -25V	+12V with no load	-12V
	Voltage Amplifier Select	0.00 ±1.25V	-9V to -25V	0.0 ±0.8V with no load	-12V

1. GENERAL DESCRIPTION.

This card contains four separate circuits. These circuits generate the Read Strobe, AC Read Register Reset signal, a Write Register DC Reset signal, and a Clipping Level output.

2. THEORY OF OPERATION.

Read Strobe and Read Register AC Reset. The Read Strobe circuit generates a Read Strobe and a Read Register AC Reset output at the time of the arrival of the first OR Clock input. The OR Clock (-) and Read Permit (-) inputs are fed to an AND gate comprised of CR1, CR2, and R20. The output of the gate goes negative, driving the base of Q6 negative, and Q6 conducts. The collector of Q6 goes positive, the OR Clock output at pin 14 goes positive, and a positive spike is coupled to the collector of Q7 through diode CR5 and capacitor C6. Q7 is the first transistor in a three-transistor flip-flop made up of Q7, Q8, and Q9. The positive pulse arriving at the collector of Q7 triggers the single-shot and the collector of Q9 goes negative for the duration of the single-shot delay. At the end of the delay, the collector of Q9 goes positive. This positive-going transition is coupled through CR12 and charges C11. When C11 is charged, the base of Q10 goes positive and Q10 cuts off. (Q10 remains cut off until capacitor C11 discharges to a level which causes the base of Q10 to go negative.) The period in which Q10 is cut off is approximately 1.5 μs. While Q10 is cut off, Q11 cuts off, and the collector of Q11 goes positive causing the Read Strobe output at pin 24 to go positive. The collector of Q11 remains positive for the period of time Q10 is cut off. When the collector of Q11 goes positive, Q12 cuts off and the collector of Q12 goes negative. When Q10 conducts, Q11 conducts and the Read Strobe output at pin 24 goes negative. The negative transition of the Read Strobe is the trailing edge of the Read Strobe pulse. When the collector of Q11 goes negative, Q12 conducts and the collector of Q12 goes positive. The positive transition of Q12 is the Read Register AC Reset signal, and appears at pin 22.

The single-shot in the preceding paragraph operates in the following manner. When a positive pulse is coupled into the collector of Q7, this pulse is also seen at the base and emitter of emitter follower Q8 and charges C8. When C8 is charged, the base of Q9 goes positive, and Q9 is cut off. Q7 is forced into conduction and the collector of Q7 drops to ground potential. The emitter of Q8 also falls to approximately ground and completes the charge cycle of C8. Capacitor C8 then begins a slow discharge through R28, R31, and R13 or R14. Resistors R13 and R14 are selected externally to change the time delay range. R13 is selected in high density. R14 is selected in low density. When C8 is discharged to a point where the base of Q9 goes negative, Q9 conducts and the single-shot delay has ended. Emitter follower Q8 totally discharges C8 through diode CR10 and resistors R30 and R29.

2. THEORY OF OPERATION. (Continued)

Write Register DC Reset. The Write Register Reset signal is a composite of the Run and Write Permit input signals. The Run and Write Permit are ANDed in the following manner. The collector of Q2 is normally negative. If Run or Write Permit inputs are positive, the collector of Q2 goes positive. With Write Permit input at pin 28 negative and Run input at pin 20 positive, Q1 is cut off and the collector of Q1 goes positive. Q13 is conducting. The collector of Q13 goes negative. CR19 is back biased and isolates the collector of Q13 from the collector of Q1. Q2 is conducting. The collector of Q2 goes to +12 volts and appears at output pin 30.

With the Run input negative and Write Permit input positive, Q13 is cut off and Q1 is conducting. The collector of Q1 goes negative. Diode CR19 becomes forward biased and lowers the collector voltage of Q13 to -6 volts. Q2 conducts and +12 volts appears at the collector of Q2 and at output pin 30.

With both Run and Write Permit inputs negative, Q1 and Q13 are cut off. The collector of Q13 rises to a value more positive than the emitter of Q2, driving Q2 to cutoff. The output at pin 30 is negative.

Clipping Level. The Clipping Level circuit provides a negative clipping bias voltage for the Read Deskew circuits. This bias voltage may be varied from approximately -6 to -9 volts. In normal operation, a higher clipping level is required in the Write Mode than that used in the Read Mode. The Clipping Level circuit automatically provides a higher clipping level when the circuit is in the Write Mode.

Transistor Q4 functions as an emitter follower and provides a low impedance voltage source to the output at pin 32. Q4 is driven by the voltage divider network comprised of trim pots R9 and R10, resistor R8, and zener diode VR1. A maximum output of approximately -9 volts is required. This output is obtained by placing VR1 in series with -6 volts to give approximately -9 volts between the anode of VR1 and ground.

When Write Permit (-) is TRUE, Q1 is cut off, causing Q3 to be cut off. With Q3 cut off, the voltage at the base of Q4 may be varied from approximately -6 volts to -9 volts by varying trim pot R9. When Write Permit (-) is FALSE, Q1 and Q3 conduct. The collector of Q3 goes to -6 volts. The voltage at the base of Q4 may then be adjusted between -6 volts and the voltage present at the slider of R9.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	86 ma max
-12 VDC ±3%	100 ma max
- 6 VDC ±4%	30 ma max
+24 VDC ±15%	3 ma max

1. GENERAL DESCRIPTION.

This card contains the input gating, deskew single-shot and the write head driver flip-flop.

2. THEORY OF OPERATION.

When Write Data input is coincident with the Write Strobe input for a period of 2 μsec, the Write Data signal is fed through OR diode CR7 to the base of Q2. Transistor Q2 conducts and the collector of Q3 is placed at ground.

Capacitor C7 charges, causing Q4 to cut off and allowing Q3 to conduct. After capacitor C7 discharges, Q4 conducts again. The discharge time of C7 is based on the time constant of C7, R1 (or R2) and R12. The discharge time determines the deskew delay time and can be varied by adjusting potentiometer R2. When the dual speed option is used, potentiometer R1 is used.

With Q4 conducting, Q5 conducts and a negative input is fed to the trigger flip-flop Q7 and Q8. The steering diodes CR18 and CR26 gate the input pulse to the proper transistor, causing the flip-flop to change state.

Assuming the flip-flop is in the reset state, Q6 and Q7 are conducting, Q8 and Q9 are cut off. Diode CR18 is forward biased and CR26 is reverse biased. The collector output of Q6 is at ground and that of Q9 is near +10 volts.

When a negative set pulse arrives at C10 and C11, the pulse through C11 is applied to reverse biased CR26, producing no change. The pulse through C10 is conducted through forward biased CR18 to the base of Q7, cutting Q7 off. When Q7 cuts off, Q6 turns off and opposite state transistors Q8 and Q9 turn on.

When Q8 and Q9 conducts, a ground is provided through the emitter-collector path to output B, pin 30. Simultaneously, the Q6 collector voltage rises to a positive voltage and is applied to output A, pin 34. Each voltage polarity change at the outputs A and B causes a current reversal in the write coil, producing a written ONE on the tape. The positive voltage is also conducted through CR21 to the Echo output, pin 24, for optional Write Check Error usage.

A positive signal at DC Reset input pin 26 causes CR19 to be forward biased, applying a positive potential to the base of Q7. Q7 is forced into conduction. A negative signal at pin 26 causes CR19 to be back biased and disconnects this input.

2. THEORY OF OPERATION. (Continued)

Write Reset input at pin 10 is combined with the Reset output of the flip-flop via Q1 and is handled in the same manner as data, except that a Write Strobe input is not required.

Test Deskew is an input provided for use in the system alignment procedures. Test signals are handled in the same manner as data, except that no other inputs are required.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	14 ma max
-12 VDC ±3%	14 ma max
- 6 VDC ±4%	8 ma max

1. GENERAL DESCRIPTION

This card contains three independent circuits.

The Write Power Gate provides power to the write amplifiers when Write Permit is TRUE and when the Write Enable relay has been energized.

The Read Permit inverter inverts and amplifies the Read Permit signal.

The Density Select driver applies voltage to the density potentiometers located on the Read Deskew Assembly (3107252).

2. THEORY OF OPERATION.

Write Power Gate. When input 1 or 2 is -12 volts, Q1 is biased to cutoff. With Q1 cut off, Q2 is driven into saturation by positive base current through R3. When Q2 conducts, the base of Q3 goes to approximately +3 volts causing Q3 to conduct. With Q3 conducting, the voltage at the base of Q4 goes to approximately +3 volts, causing Q4 to conduct. When Q4 conducts, the output, through pins 7 and 1 of K1, is at +10 volts. Relay K1 is energized when the External File Protect switch is closed.

When input 1 or 2 is 0 volts, Q1 conducts and -6 volts appears at the base of Q3, driving it to cutoff. With Q2 cut off, the base of Q3 goes to +15 volts. As Q3 is conducting, approximately +15 volts appears at the base of Q4, driving it to cutoff. The output is 0 volts.

Read Permit Inverter. When Read Permit input is -12 volts, Q9 is biased to cutoff, and the output is +12 volts. When Read Permit input is 0 volts, Q9 is conducting and the output is -6 volts.

Density Select Driver. The Density Select Driver input is controlled by a pushbutton on the OCP. When input at pin 11 is 0 volts (Low Density), Q5 and Q6 are cut off. High Density output at pin 16 is open circuit. Q7 and Q8 are conducting and Low Density output at pin 17 is -12 volts.

2. THEORY OF OPERATION. (Continued)

Erase Head Driver. Whenever the Write Power Gate is on, current is supplied to the Erase Head through R19. The current is 100 milliamperes nominal.

When input at pin 11 is -12 volts (High Density), Q5 and Q6 are conducting. High Density output at pin 16 is -12 volts. Q7 and Q8 are cut off and Low Density output at pin 17 is open circuit.

3. OPERATIONAL CHARACTERISTICS.

CIRCUIT	INPUT		OUTPUT	
	HIGH LEVEL	LOW LEVEL	HIGH LEVEL	LOW LEVEL
Write Power Gate	0.0V to -0.5V	-5.70V to -12.36V	+11V to +12V	0.0V to -1.5V
Density Select	-0.5V most negative	-5.5V least negative	0.3V more positive than -12V supply	Open circuit
Read Permit	-0.5V most negative	-5.5V least negative	0.5V max	-6.0 ±0.5V
Write Enable Relay	11.64V min at 100 ma max		+11V to +12V	0.0V to -1.5V

4. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	2 ma max
-12 VDC ±3%	103 ma max
- 6 VDC ±4%	13 ma max
+24 VDC ±15%	30 ma max
-24 VDC ±15%	5 ma max

SECTION VII
DRAWINGS

7-1. INTRODUCTION.

Printed circuit board schematics and assembly drawings are included in this section and are located in alphabetical order by the mnemonic code, as shown on Table 7-1.

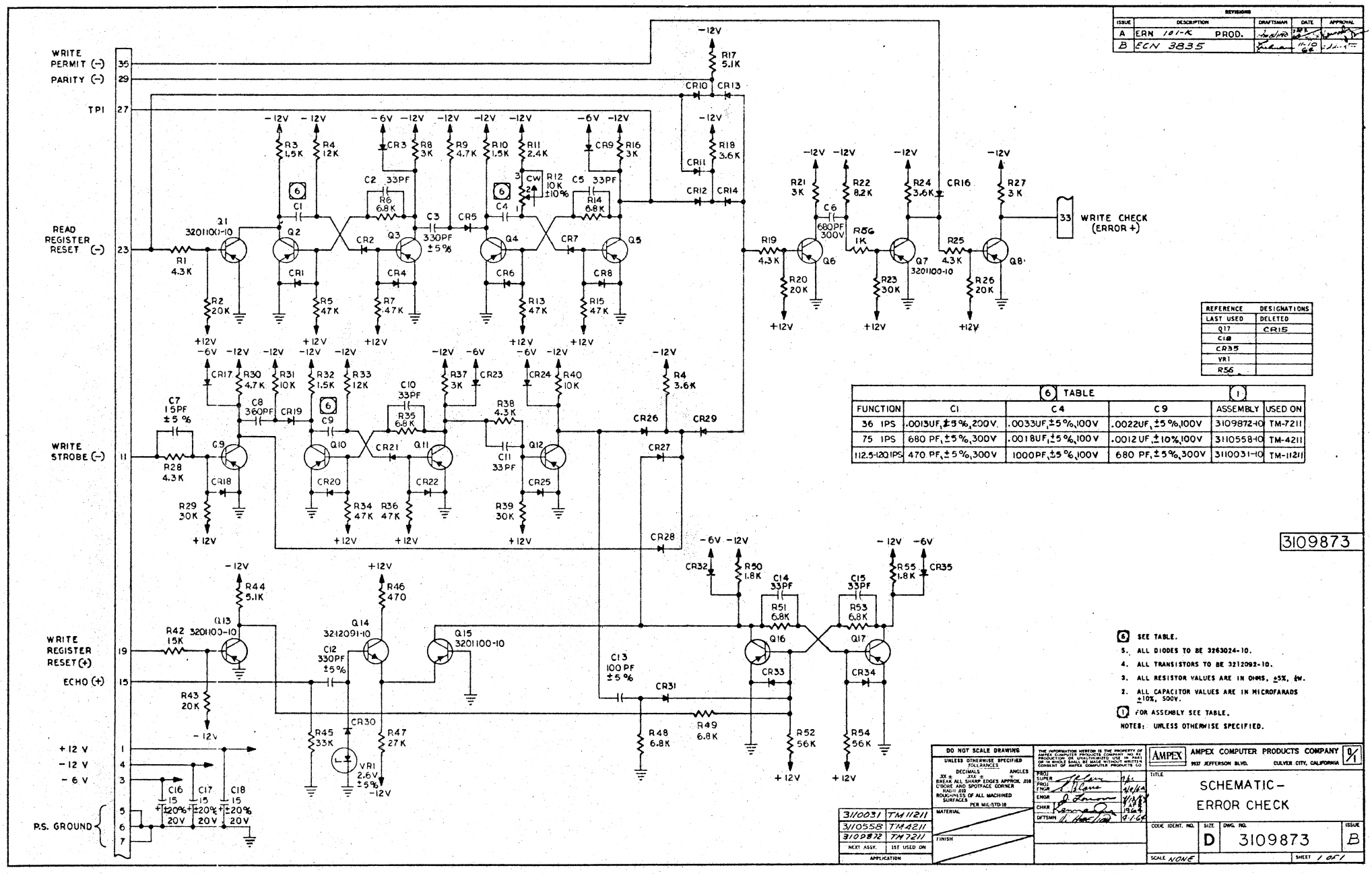
Two sets of logic diagrams are located at the end of this section. Logic Diagram 3112457 is for standard DE-211 (7-track) and DE-291 (9-track) systems which use Forward/Reverse and Run/Stop commands. Logic Diagram 3115496 is for standard systems which use Forward/Stop and Reverse/Stop commands.

TABLE 7-1
LIST OF DRAWINGS

CODE	DESCRIPTION	SCHEMATIC	ASSY DWG
ECC	Error Check	3109873	3109915
EOA	Exclusive OR	3104452	3107274
IBA	Input Buffer	3107038	3107251
ODA	Output Driver	3107043	3107255
RAB	Read Amplifier	3107118	3107270
RDB	Read Deskew	3107253	3107273
RDC	Read Deskew, Bidirectional	3109930	3109933
SGA	Strobe Generator	3107058	3107276
SLB	Select Logic	3111158	3111157
WAB	Write Amplifier	3112345	3112347
WPD	Write Power Gate	3107128	3107272

Logic Diagram DE-211 Data Electronics (Fwd/Rev-Run/Stop) 3112457

Logic Diagram DE-211 Data Electronics (Fwd/Stop-Rev/Stop) 3115496



REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ERN 101-K PROD.			
B	ECN 3835		11/10/66	

REFERENCE DESIGNATIONS	
LAST USED	DELETED
Q17	CR15
C18	
CR35	
VR1	
R56	

(6) TABLE (1)

FUNCTION	C1	C4	C9	ASSEMBLY	USED ON
36 IPS	.0013UF, ±5%, 200V.	.0033UF, ±5%, 100V	.0022UF, ±5%, 100V	3109872-10	TM-7211
75 IPS	680 PF, ±5%, 300V	.0018UF, ±5%, 100V	.0012 UF, ±10%, 100V	3110558-10	TM-4211
112.5-120 IPS	470 PF, ±5%, 300V	1000PF, ±5%, 100V	680 PF, ±5%, 300V	3110031-10	TM-11211

3109873

(6) SEE TABLE.

5. ALL DIODES TO BE 3263024-10.
4. ALL TRANSISTORS TO BE 3212092-10.
3. ALL RESISTOR VALUES ARE IN OHMS, ±5%, ¼W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS ±10%, 500V.

(1) FOR ASSEMBLY SEE TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED.

3110031	TM11211
3110558	TM4211
3109872	TM7211
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .XXX ± ANGLES ±1°
BREAK ALL SHARP EDGES APPROX .010 C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH

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PROJ		
SUPER		
PROJ		
ENGR		4/6/66
ENGR		4/13/66
CHKR		4/14/66
DFTSMN		4/16/66

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

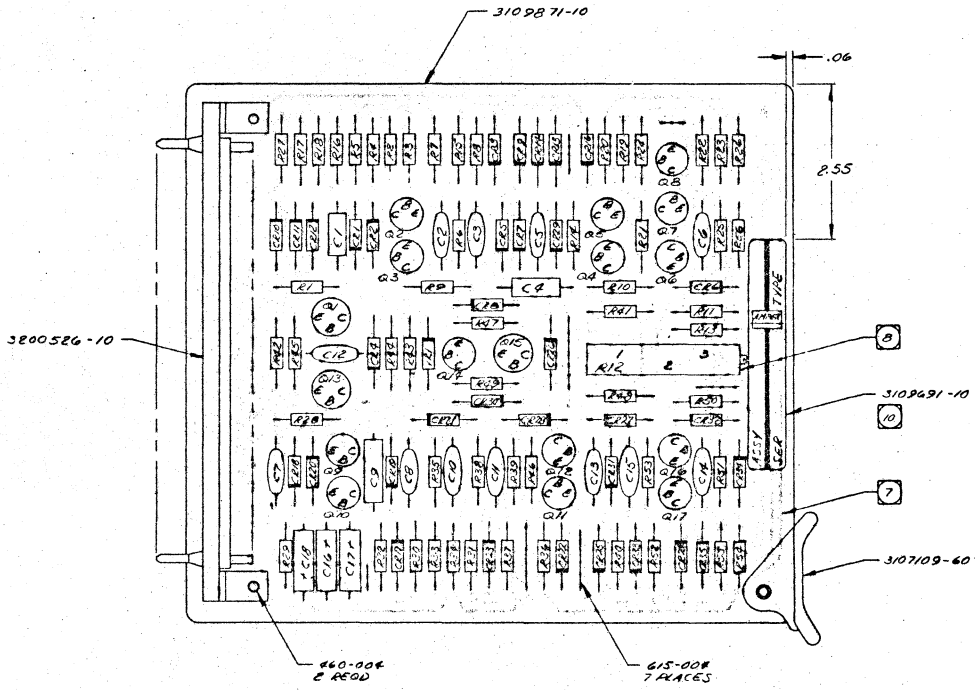
TITLE: SCHEMATIC - ERROR CHECK

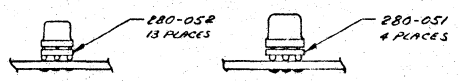
CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3109873	B

SCALE NONE SHEET 1 OF 1

ECC

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 101-K 1H00.			
B	ECN [illegible]			
C	ECN 3835			





TYPICAL TRANSISTOR INSTALLATION

PART NO.	REF DESIGNATION
041-410	R56

PART NO.	REF. DESIGNATIONS
3201100-10	Q1, 13, 15, 7
3212091-10	Q14
3212092-10	Q2,3,4,5,6, 8,9,10,11,12,16,17
3263024-10	CR1 THRU CR14, [illegible]
013-401	VR1
034-177	C13
034-212	C3, 12
034-535	C7
034-491	C2,5,10,11,14,15
034-496	C8
034-519	C6
PART C	C9
PART B	C4
037-990	C16, 17, 18
PART A	C1
041-408	R 31, 40
041-409	R 42
041-411	R6,7,13,15,34,36
041-412	R9, 30
041-413	R6,14,35,48,49,51,53
041-428	R46
041-430	R3, 10, 32
041-434	R50, R55
041-482	R4, R33
041-483	R47
041-495	R22
041-508	R2, 20, 26, 43
041-518	R45
041-519	R52, 54
041-550	R8, 16, 21, 27, 37
041-561	R17, 44
041-570	R11
041-571	R18, 24, 41
041-584	R1,19,25,28,38
041-612	R23, 29, 39
044-197	R12

11. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH. CORP OR EQUIV.
10. MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130. ISSUE LETTER TO BE MARKED IN UPPER RIGHT CORNER OF NAMEPLATE.
9. PART NO. TO BE AS SHOWN ON BILL OF MATERIAL.
8. TRIMPOT NOT TO BE SUBMERGED IN WATER.
7. CIRCUITRY ON FARSIDE.
6. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. HEAVY LINE ON DIODE INDICATES CATHODE.
3. ASSEMBLE PER MANUFACTURING PRACTICES MANUAL.
2. FOR ASSEMBLY SPECIFICATION SEE 3109874.
1. FOR SCHEMATIC SEE 3109873

NOTES:

REFERENCE

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES.
DECIMALS XX ± .03 XXX ± .010 ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010
SCRAPE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES # PER MIL-STD-10
MATERIAL
FINISH

3110031	TM-1121
3110558	TM-4211
3109872	TM-7211
NEXT ASSY	1ST USED ON
APPLICATION	

AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

PROJ		
SUPER PROJ		
ENGR		
ENGR		
CHKR		
DFTSMN		

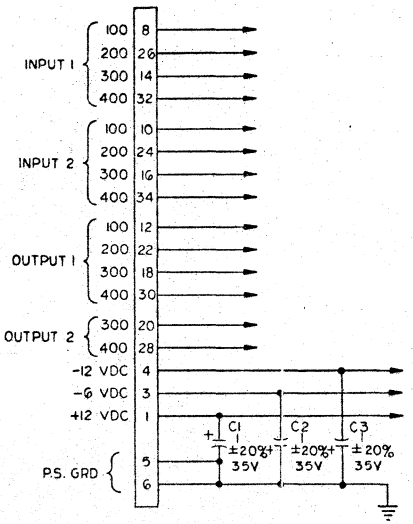
TITLE: CIRCUIT BOARD ASSY-ERROR CHECK

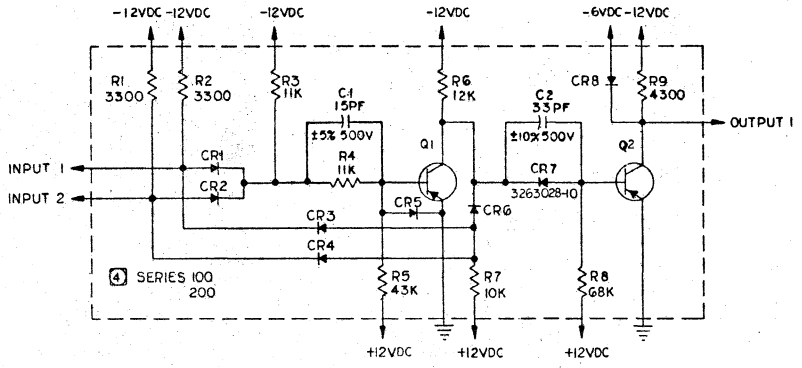
CODE IDENT. NO. | SIZE: D | DWG. NO.: 3109915 | ISSUE: C

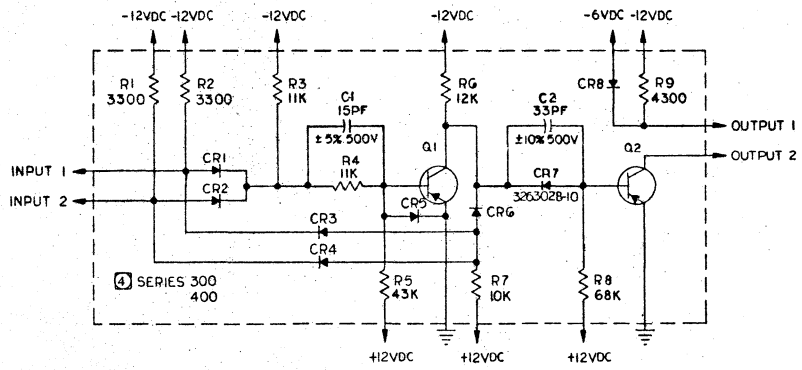
SCALE 2/1

ECC

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	00000-35	MB		
B	ECN 3149 REQ.			







5. ALL TRANSISTORS TO BE 32120192-10.
4. REF DESIGNATIONS ARE ABBREVIATED PER MIL-STD-16. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
3. ALL DIODES TO BE 32G3024-10.
2. ALL RESISTORS IN OHMS ±5%, 1/4W.
1. ALL CAPACITORS IN MICROFARADS

NOTES: UNLESS OTHERWISE SPECIFIED

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES: DECIMALS XX ± .03, .XXX ± .010; ANGLES ± 1°; BREAK ALL SHARP EDGES APPROX. .010; C BORE AND SPOTFACE CORNER RADII .010; ROUGHNESS OF ALL MACHINED SURFACES √ PER MIL STD-10

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PROJ DESIGNER		
PROJ ENGR		
ENGR		
CHKR		10-7-66
DFTSMN		9-26-66

MATERIAL

FINISH

3102978	DE-100
NEXT ASSY.	1ST USED ON
APPLICATION	

AMPEX 9/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC, EXCLUSIVE OR TYPE P

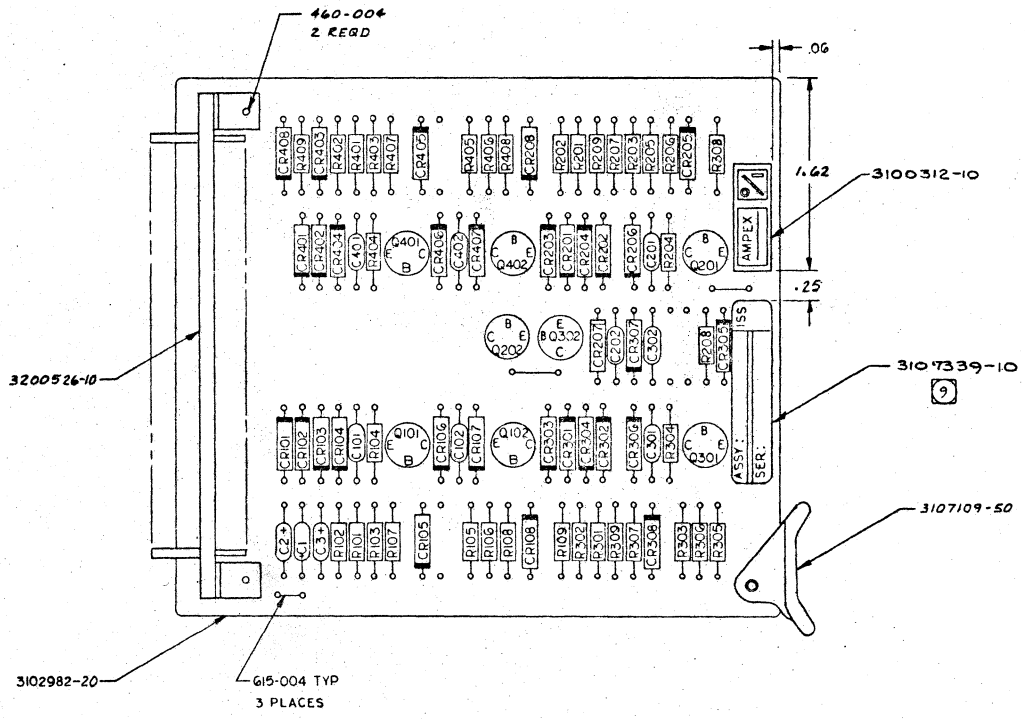
7103-254

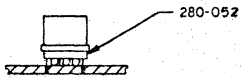
CODE IDENT. NO. | SIZE D | DWG. NO. 3104452 | ISSUE B

SCALE NONE

EOA

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ENGR'G RELEASE PER ECO [illegible]	[illegible]	2 SEPT 66	[illegible]





TYPICAL TRANSISTOR INSTALLATION

PART NO.	QTY.	COMPONENT DESIGNATION
3212092-10	8	Q101,102,201,202,301,302,401,402
3263024-10	28	CR101 THRU 106,108,301 THRU 306, 308,CR201 THRU 206,208,401 THRU 406,408
3263028-10	4	CR107,207,307,407
034-491	4	C102,202,302,402
034-963	4	C101,201,301,401
037-058	3	C1,2,3
041-407	8	R101,102,201,202,301,302,401,402
041-408	4	R107,207,307,407
041-415	4	R108,208,308,408
041-482	4	R106,206,306,406
041-562	4	R105,205,305,405
041-584	4	R109,209,309,409
041-748	8	R103,104,203,204,303,304,403,404

3107274

9 MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

8. PART NO. TO BE 3107274-10.
7. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1815, COLUMBIA TECH. CORP., OR EQUIV.
6. HEAVY LINE ON DIODE INDICATES CATHODE.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
3. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL
2. FOR ASSY SPECIFICATION SEE 3104624.
1. FOR SCHEMATIC SEE 3104452

NOTES:

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES

DECIMALS: .XX ± .03, .XXX ± .010; ANGLES ± 1°; BREAK ALL SHARP EDGES APPROX .010 C'BORE AND SPOTFACE CORNER EACH .010; ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

PROJ		
DSNER		
DRFT		
ENGR		
CHKR		
DFTSMN		

AMPEX 9/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

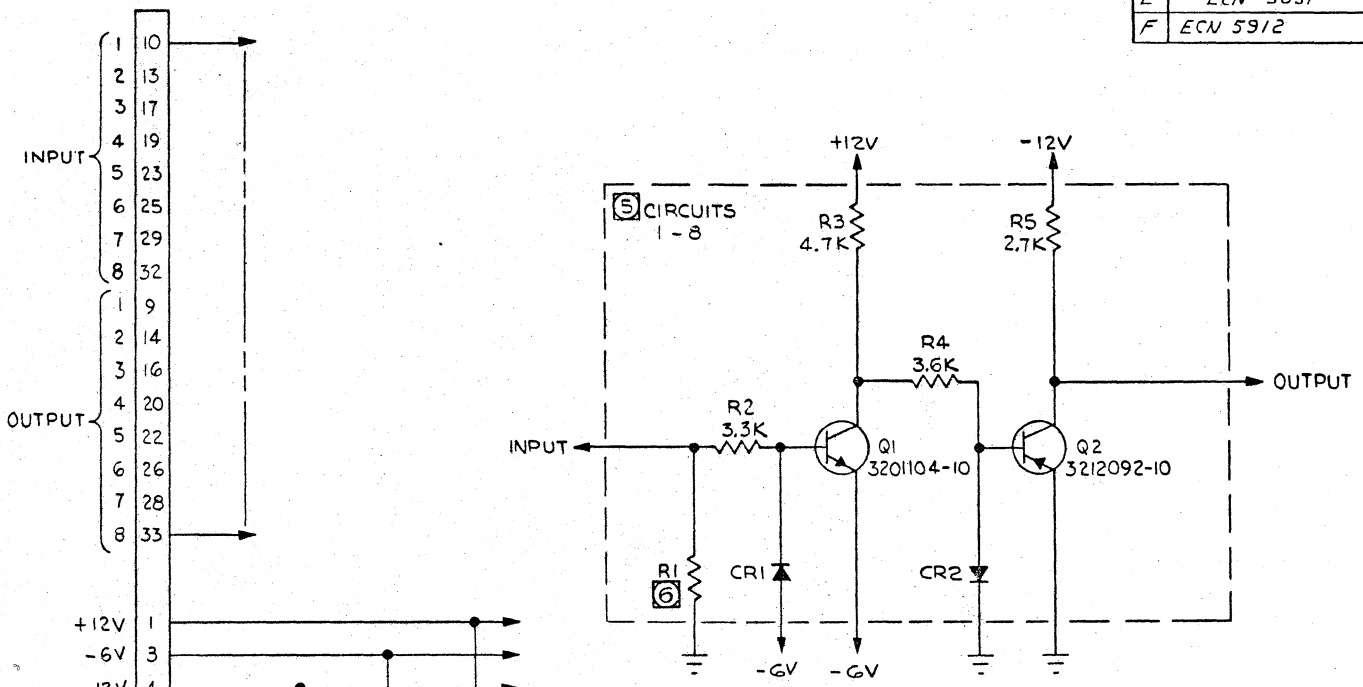
TITLE: CIRCUIT BOARD ASSY - EXCLUSIVE OR TYPE P

MATERIAL			
FINISH	CODE IDENT. NO.	SIZE	DWG. NO.
		D	3107274
SCALE 2/1			ISSUE A

3107280	TM-7211
NEXT ASSY.	1ST USED ON
APPLICATION	

EOA

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
D	ECN 911-AN REDRAW	10-29-63	Jaquith	10 63 29	Allington
E	ECN 5051	4-11-66	L.Co.	4 11 66	Coerper
F	ECN 5912	8/17/66	Aromash	8 18 "	Allington



DWG. NO. 3107038

TABLE I

ASSEMBLY	USED ON	COMPONENT R1	
3107037-10	DE 200	7.5 K	
3107258-10	DE 200	7.5 K	
3118156-01	TM 12211 W/E	36 K	
3118279-01	DE-212 (EAI)	270Ω	

6 SEE TABLE I

5 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE REFERENCE DESIGNATION WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.

4. ALL DIODES TO BE 3263024-10.
3. ALL RESISTOR VALUES ARE IN OHMS 1/4W ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 20V ±20%.
1. FOR ASSEMBLY SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED.

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS TOLERANCES ANGLES
.XX±.03 .XXX±.010 ± ½°
BREAK ALL SHARP EDGES APPROX. .010, C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓
MATERIAL

FINISH

SEE TABLE	——
NEXT ASSY.	1ST USED ON
APPLICATION	

PROJ SUPER	[illegible]	8-15-64
PROJ ENGR	[illegible]	8-15-64
ENGR	[illegible]	8/6-64
CHKR	R.B. Taylor	8-15-63
DFTSMN	J. Edwards	4-6-63

AMPEX COMPUTER PRODUCTS DIVISION
P.O. BOX 329, CULVER CITY, CALIF.

TITLE
SCHEMATIC— INPUT BUFFER

SIZE	CODE IDENT. NO.	DWG. NO.
C	09150	3107038

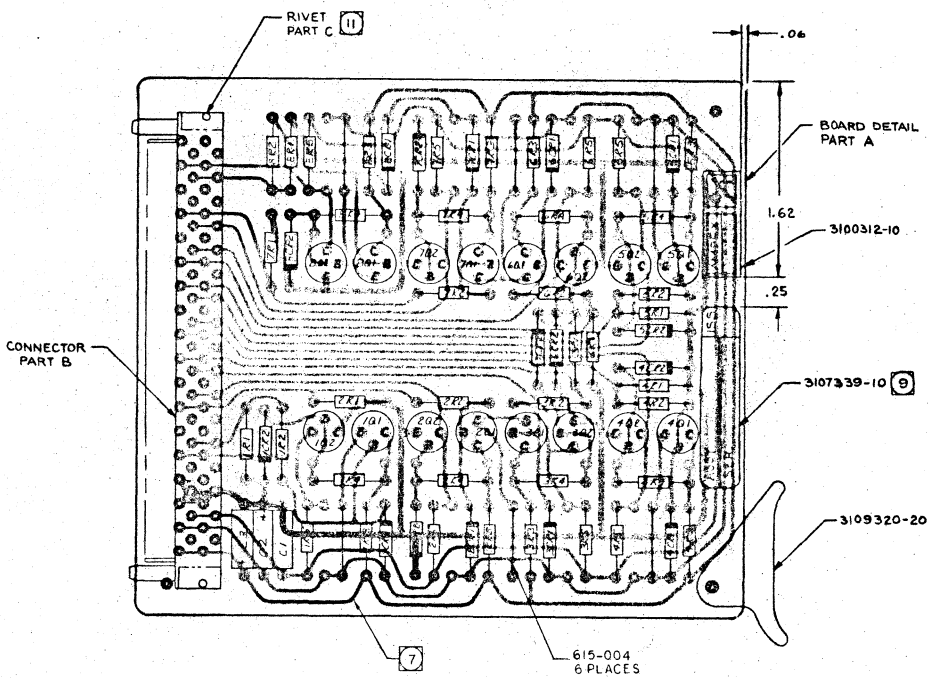
SCALE NONE SHEET 1 OF 1

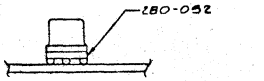
IBA

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-31 DEV. PRO.			
B	ECN 911-76			
C	ECN 911-AN PROD			
D	ECN 5051			
E	ECN 5312			

TABLE I

B/M REFERENCE TABLE		
ASSEMBLY	USED ON	PART D
3107037-10	DE-200	041-520
3107258-10	DE-200	041-520
3118156-01	TM-7213 BTL 168	041-751
3118273-01	DE-212(AN)	041-503





TYPICAL TRANSISTOR INSTALLATION

PART NO.	REFERENCE DESIGNATION
3201104-10	IQ1 THRU BQ1
3212098-10	IQ2 THRU BQ2
3263024-10	ICR1 THRU BCR1, ICR2 THRU BCR2
037-990	C 1,2,3
041-407	IR2 THRU BR2
041-442	IR5 THRU BR5
041-412	IR3 THRU BR3
(12) PART D	IR1 THRU BR1
041-571	IR4 THRU BR4

REFERENCE

(12) INSTALL PART D PER TABLE I.

(11) RIVET, PART C USED ONLY WITH 3200526-10.

10. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE IB15, COLUMBIA TECH CORP OR EQUIV.

(9) MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

8. PART NO. TO BE AS SHOWN ON TABLE I.

(7) CIRCUITRY ON FRESIDE.

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.

4. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL.

3. HEAVY LINE ON DIODE INDICATES CATHODE.

2. FOR PRODUCT SPECIFICATION SEE 3107039.

1. FOR SCHEMATIC SEE 3107038.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	1ST USED ON
3107258	TM7211
3107037	TM7211
3107258	TM7212
3107037	TM5
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS: .01 XX ± .010, .001 XXX ± .005, ANGLES ±1°
BREAK ALL SHARP EDGES APPROX .010
C BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES 125 PER MIL-STD-10
MATERIAL
FINISH

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

PROJ ENGR		
DSGN		
PROJ ENGR		
ENGR		
CHKR		
DFTSMN		

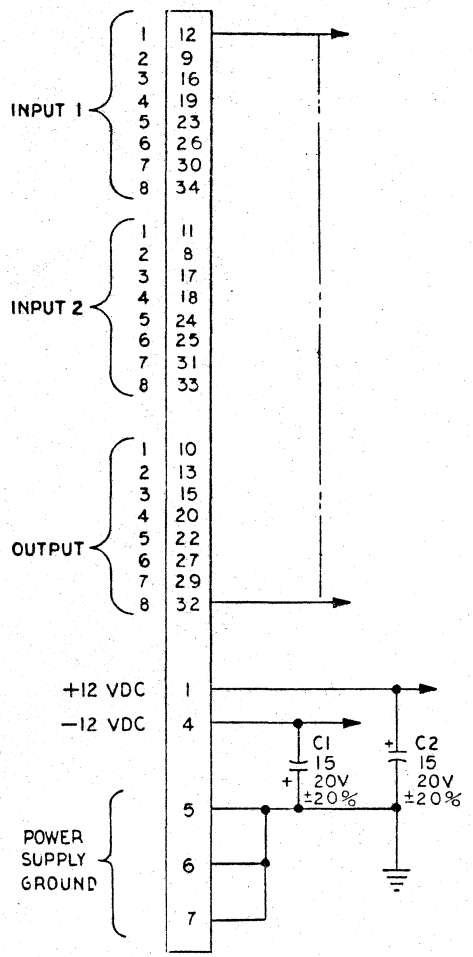
TITLE: CIRCUIT BOARD ASSEMBLY-INPUT BUFFER

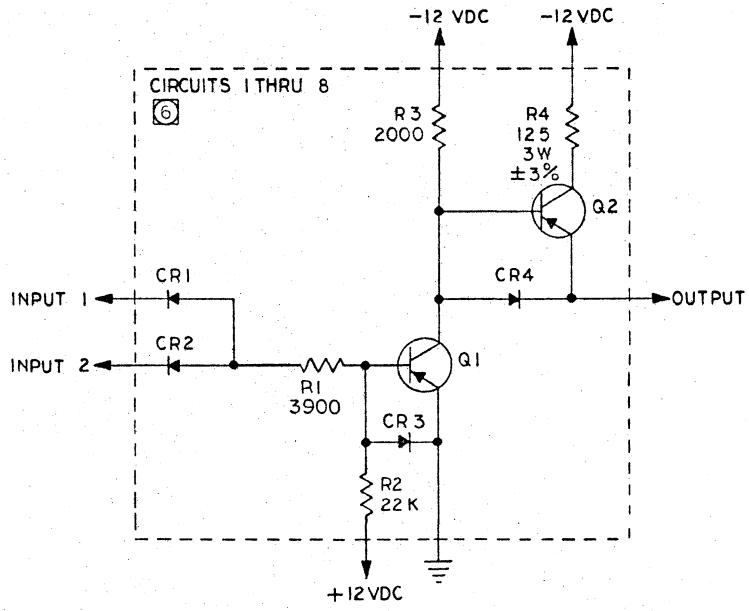
CODE IDENT. NO. | SIZE: D | DWG. NO.: 3107251 | ISSUE: E

SCALE 1/1

IBA

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 800-54 DEV. PRO. (X-C)	B. Hann	8-27-63	
B	ECN 911-31	Gawley	12/9/63	
C	ECN 911-AN PROD.	A Rhoads	3-3-64	





(6) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE DESIGNATING NUMBER WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.

5. ALL DIODES TO BE 3263024-10.

4. ALL TRANSISTORS TO BE 3212092-10.

3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS.

1. FOR ASSEMBLY SEE 3107042, 3107259

NOTES: UNLESS OTHERWISE SPECIFIED

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

3107042	TM-5
3107259	TM 7211
3107042	TM 721
3107259	TM 7212
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS ANGLES
XX ± .03 XXX ± .010 ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES √ PER MIL-STD-10

MATERIAL

FINISH

PROJ SUPER		2/6/64
PROJ ENGR		2/26/64
ENGR		3/6/64
CHKR		3/5/64
DFTSMN	B. Hann	4-22-63

AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

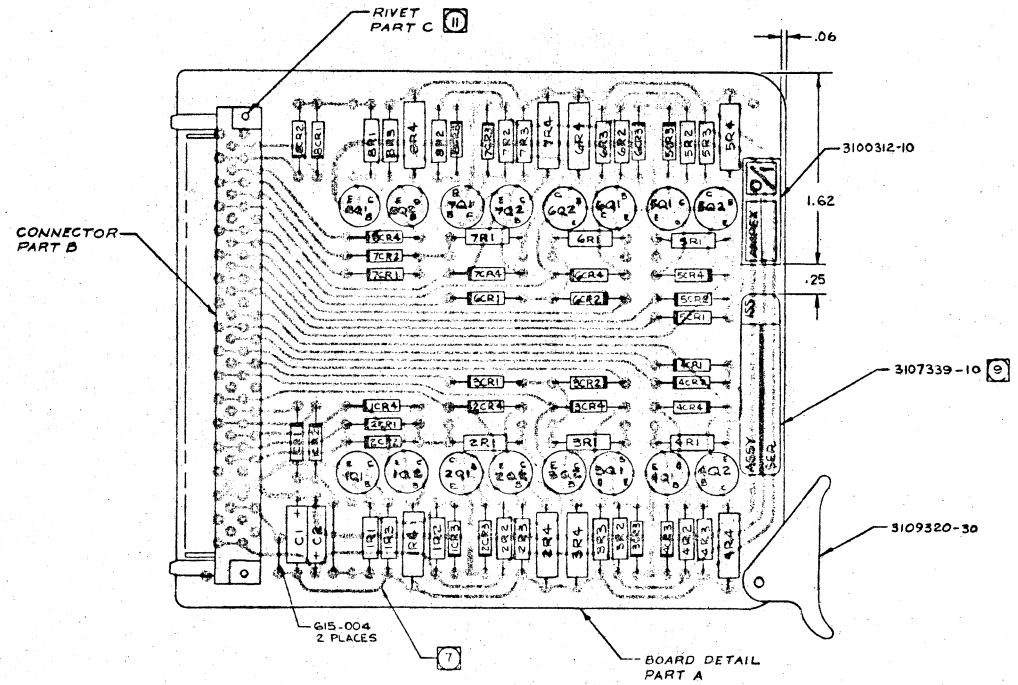
TITLE
SCHEMATIC — OUTPUT DRIVER

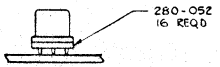
CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	C	3107043	C

SCALE NONE

ODA

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-31 DEV PRO			
B	ECN 911-AN PROD.			





TYPICAL TRANSISTOR INSTALLATION

PART NO.	REFERENCE DESIGNATION
3212092-10	1Q1 THRU 8Q1, 1Q2 THRU 8Q2
3263024-10	1CR1 THRU 8CR1, 1CR2 THRU 8CR2, 1CR3 THRU 8CR3, 1CR4 THRU 8CR4
057-990	C1, C2
041-406	1R2 THRU 8R2
041-511	1R1 THRU 8R1
041-560	1R3 THRU 8R3
047-302	1R4 THRU 8R4

REFERENCE

(11) RIVET, PART C USED ONLY WITH 3200526-10

(10) SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH CORP OR EQUIV.

(9) MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

8. PART NO. TO BE AS SHOWN IN BILL OF MATERIAL

(7) CIRCUITRY ON FARSIDE

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE

5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY

4. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL

3. HEAVY LINE ON DIODE INDICATES CATHODE

2. FOR PRODUCT SPECIFICATION SEE 3107044

1. FOR SCHEMATIC SEE 3107043

NOTES: UNLESS OTHERWISE SPECIFIED

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS: XX ± .03, XXX ± .010, ANGLES ± 1°
BREAK ALL SHARP EDGES APPROX .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES √ PER MIL STD-10

MATERIAL

FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY AND IS NOT TO BE REPRODUCED, USED OR DISCLOSED IN WHOLE OR IN PART WITHOUT THE WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ
SUPVR
PROJ
ENGR
ENGR
CHKR
DFTSMN B. Hinn 4 23 69

AMPEX AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE
CIRCUIT BOARD ASSEMBLY
OUTPUT DRIVER

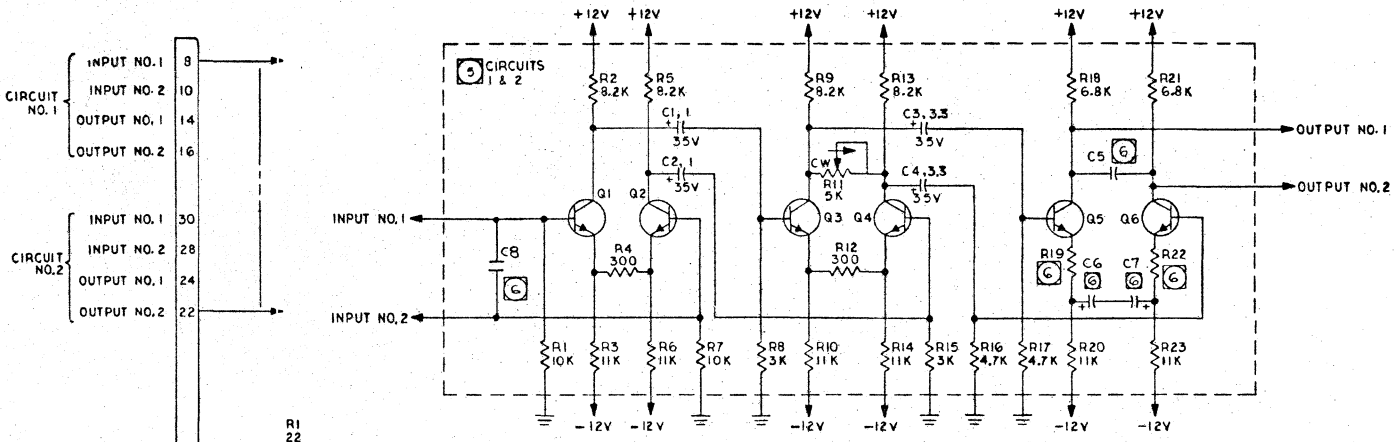
3107042	TM7211
3107259	TM7211
3107259	TM7212
3107042	TM5
NEXT ASSY.	1ST USED ON
APPLICATION	

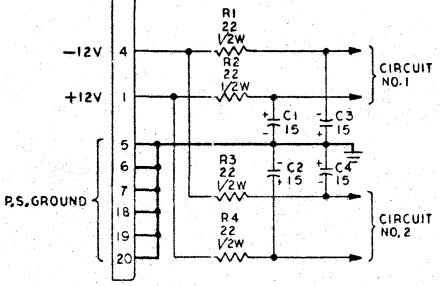
CODE IDENT. NO. | SIZE D | DWG. NO. 3107255 | ISSUE B

SCALE 2/1

ODA

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-17 DEV. PRO(AXCH)		3/3/63	
B	ECN 911-AH PROD.		5-23	
C	ECN 3570		9-20-64	
D	ECN 3963		1-27-65	
E	ECN 4291		5-3-65	
F	ECN 4544		9/9/65	
G	ECN 4657		11/1/65	
H	ECN 4984		3/9/66	
J	ECN 5016		3/24/66	
K	ECN 5086		9/28/66	
L	ECN 7003		9/11/68	





VERSION TABLE							
C6 & C7	FUNCTION	C5	C8	R19 & R22	ASSEMBLY	USED ON
15 μF ±20%, 20V	36 IPS	1000 PF ±5% 100V	OPEN	220 Ω	3107117	TM 7211
15 μF ±20%, 20V	75 IPS	470 PF ±5% 300V	220 PF ±5% 500V	220 Ω	3109991	TM-4211
15 μF ±20%, 20V	112.5-120 IPS	820 PF ±5% 300V	1000 PF ±5% 100V	220 Ω	3110273	TM-11211
15 μF ±20%, 20V	36 IPS	1000 PF ±5% 100V	OPEN	220 Ω	3107266	TM-7211
15 μF ±20%, 20V	7.5 IPS	.0047 μF ±10% 100V	OPEN	100 Ω	3113334	TM-7211
70 μF -15% +25%, 15V	7.5 IPS	.0047 μF ±10% 100V	OPEN	100 Ω	3116066	TM 7211 INTERSTATE
15 μF ±20% 20V	150 IPS	OPEN	OPEN	220 Ω	3116187	TM-12211 AGB
15 μF ±20% 20V	112.5/120/150 IPS	360 PF ±5% 500V	270 PF ±5% 500V	220 Ω	3118138	TM 11211 MANORELL

3107118

6 FOR VALUE SEE VERSION TABLE.

5 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE DESIGNATING NUMBER WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.

4. ALL TRANSISTORS TO BE 3212081-10.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, ± 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 20 V ± 20%.
1. FOR ASSEMBLY SEE TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED..

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .— .XXX ± .— ANGLES ± —
BREAK ALL SHARP EDGES APPROX .010 CHAMF AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH
SEE TABLE
NEXT ASSY | 1ST USED ON
APPLICATION

PROJ
SUPVR
PROJ ENGR
ENGR
CHKR
DFTSMN

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

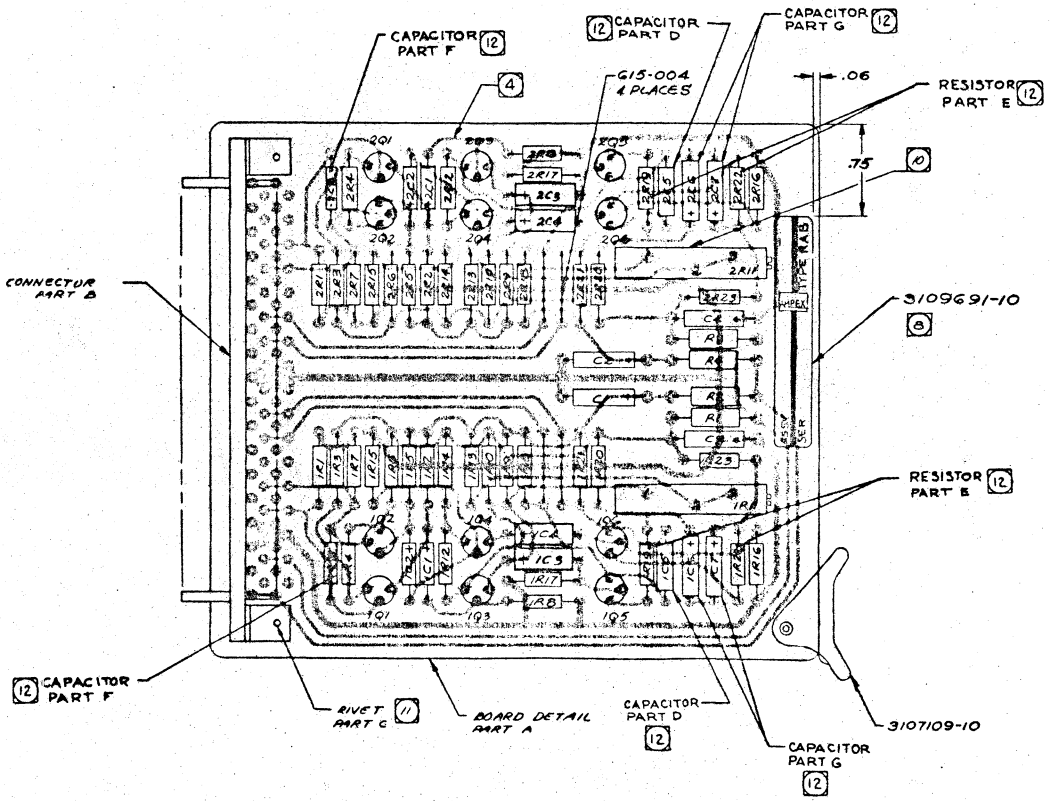
TITLE
SCHEMATIC - READ AMPLIFIER UNSHARED

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107118	L

SCALE NONE SHEET 1 OF 1

RAB

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-47 DEV. PROJECT		1/3/63	
B	ECN 911-AH PROD.		2/5/64	
C	ECN 3744		8/64	
D	ECN 3858		11/64	
E	ECN 3963		12/65	
	ECN 4291		5/66	
G	ECN 4657		11/66	
H	ECN 4984		7/8/66	
J	ECN 5016		7/26/66	
K	ECN 5086		8/8/66	



TYPICAL TRANSISTOR INSTALLATION

TABLE I

ASSEMBLY	USED ON	PART D	PART E	PART F	PART G
3107117-10	TM 7211	034-950	041-416	NOT USED	037-990
3109991-10	TM 4211	034-214	041-416	034-240	037-990
3110273-10	TM 11211	034-283	041-416	034-950	037-990
3107266-10	TM 7211	034-950	041-416	NOT USED	037-990
3113334-10	TM 7211	035-989	041-419	NOT USED	037-990
3116066-10	TM 7211 INTERSTATE	035-989	041-419	NOT USED	037-478
3116187-10	TM 7227 1 (GE)	NOT USED	041-416	NOT USED	037-990
3118138-03	TM 11211 MANDRELL	034-934	041-416	034-319	037-990

PART NO.	REFERENCE DESIGNATION
3212091-10	IQ1 THRU IQ6, 2Q1 THRU 2Q6
PART D	IC5, 2C5
037-994	IC1, IC2, 2C1, 2C2
037-990	C1 THRU C4,
041-408	1R1, 2R1, 1R7, 2R7
041-413	1R18, 2R18, 1R21, 2R21
PART E	1R19, 2R19, 1R22, 2R22
041-550	1R8, 2R8, 1R15, 2R15
041-495	1R2, 2R2, 1R5, 2R5, 1R9, 2R9, 1R13, 2R13
041-421	R1 THRU R4
041-569	1R4, 2R4, 1R12, 2R12
041-748	1R3, 2R3, 1R6, 2R6, 1R10, 2R10, 1R14, 2R14, 1R20, 2R20, 1R23, 2R23
044-366	1R11, 2R11
041-412	1R16, 2R16, 1R17, 2R17
037-176	IC3, IC4, 2C3, 2C4
PART F	IC8, 2C8
PART G	IC6, 2C6, IC7, 2C7

3107270

(10) TRIMPOT NOT TO BE SUBMERGED IN WATER

9 SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH CORP OR EQUIV

(8) MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

7. PART NO. TO BE AS SHOWN IN BILL OF MATERIAL.

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.

(4) CIRCUITRY ON FARSIDE.

3. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL.

2. FOR ASSEMBLY SPECIFICATION SEE 3107119.

1. FOR SCHEMATIC SEE 3107118.

NOTES:

(12) INSTALL PARTS D,E,F

(11) RIVET, PART C USED ONLY WITH 3200626-10.

REFERENCE

273

SEE TABLE	
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES

DECIMALS: XX ± .010, XXX ± .005
ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010 CHORE AND SKIVFACE CORNER RADII .030
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

DRAWN		
SUPER.		
PROJ.		2/6/64
ENGR.		2/6/64
ENGR.		2/6/64
CHKR.		2/6/64
DFTSMN	K. Kirkland	2/6/64

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSEMBLY-READ AMPLIFIER UNSHARED

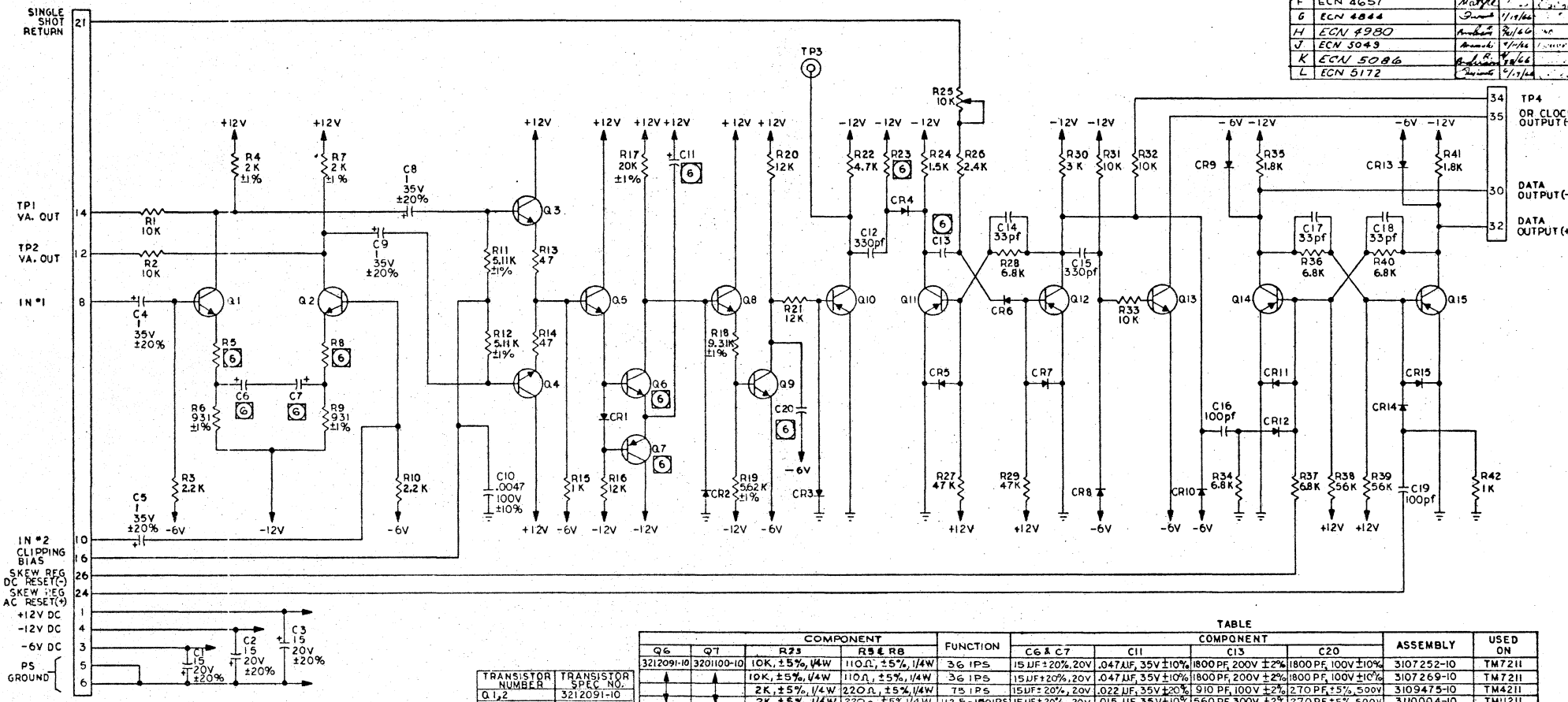
CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107270	K

SCALE 2:1 SHEET 1 OF 1

RAB

REVISIONS				
ISSUE	DESCRIPTIONS	DRAFTSMAN	DATE	APPROVAL
M	ECN 5772	[illegible]	9/1/66	

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	[illegible]	[illegible]		
C	ECN [illegible]	[illegible]		
E	ECN 4612	[illegible]	[illegible]	
F	ECN 4657	[illegible]	[illegible]	
G	ECN 4844	[illegible]	1/19/66	
H	ECN 4980	[illegible]	3/1/66	
J	ECN 5049	[illegible]	4/1/66	
K	ECN 5086	[illegible]	5/6/66	
L	ECN 5172	[illegible]	6/1/66	



TRANSISTOR NUMBER	TRANSISTOR SPEC NO.
Q1,2	3212091-10
Q3,4	3201117-10
Q5	3212098-10
Q8,9,13	3201104-10
Q10,11,12,14,15	3212092-10

TABLE

COMPONENT				FUNCTION	COMPONENT				ASSEMBLY	USED ON
Q6	Q7	R23	R9 & R8		C6 & C7	C11	C13	C20		
3212091-10	3201100-10	10K, ±5%, 1/4W	110Ω, ±5%, 1/4W	36 IPS	15 µF ±20%, 20V	.047 µF, 35V ±10%	1800 PF, 200V ±2%	1800 PF, 100V ±10%	3107252-10	TM7211
↓	↓	10K, ±5%, 1/4W	110Ω, ±5%, 1/4W	36 IPS	15 µF ±20%, 20V	.047 µF, 35V ±10%	1800 PF, 200V ±2%	1800 PF, 100V ±10%	3107269-10	TM7211
↓	↓	2K, ±5%, 1/4W	220Ω, ±5%, 1/4W	75 IPS	15 µF ±20%, 20V	.022 µF, 35V ±20%	910 PF, 100V ±2%	270 PF, ±5%, 500V	3109475-10	TM4211
↓	↓	2K, ±5%, 1/4W	220Ω, ±5%, 1/4W	112.5-150IPS	15 µF ±20%, 20V	.015 µF, 35V ±10%	560 PF, 300V ±2%	270 PF, ±5%, 500V	3110004-10	TM11211
3212091-10	3201100-10	10K, ±5%, 1/4W	110Ω, ±5%, 1/4W	7.5 IPS	15 µF ±20%, 20V	.47 µF, 35V ± 20%	1800 PF, 200V ±2%	.0047 PF 100V ±10%	3113333-10	TM7211
3212081-10	014-364	10K, ± 5%, 1/4W	110Ω, ±5%, 1/4W	7.5 IPS	70 µF -[illegible] %, 15V	.22 µF, 35V, ±10%	.01 UF, 100V ±10%	.0047PF 100V ±10%	3116055-10	TM 4211 INTERSTATE
3212091-10	3201100-10	2K, ±5%, 1/4W	220Ω, ±5%, 1/4W	120 IPS	15 µF, ±20%, 20V	.015 µF, 35 V, ±10%	910 PF, 100V, ±2%	270 PF, ±5%, 500V	3118153-01	TM-11241

6 SEE TABLE.

5. CR3 THRU CR15 TO BE 3263024-10.
4. CR1 AND CR2 TO BE 3263028-10.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 500V.
1. FOR ASSEMBLY SEE TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS ANGLES
.XX ± .02 ±
.XXX ± .010
BREAK ALL SHARP EDGES APPROX .010
CHAMFERS AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES
PER MIL-STD-10

MATERIAL
FINISH

SEE TABLE
NEXT ASSY. | 1ST USED ON
APPLICATION

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PROJ		
SUPER		
PROJ ENGR		
ENGR		
CHKR	K. Brinkman	11-22-67
DFTSMN	J. Kuratani	9/1/68

AMPEX COMPUTER PRODUCTS COMPANY 9/1
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE
SCHEMATIC —
READ DESKEW, UNSHARED

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107253	M

SCALE NONE SHEET 1 OF 1

RDB

TABLE I

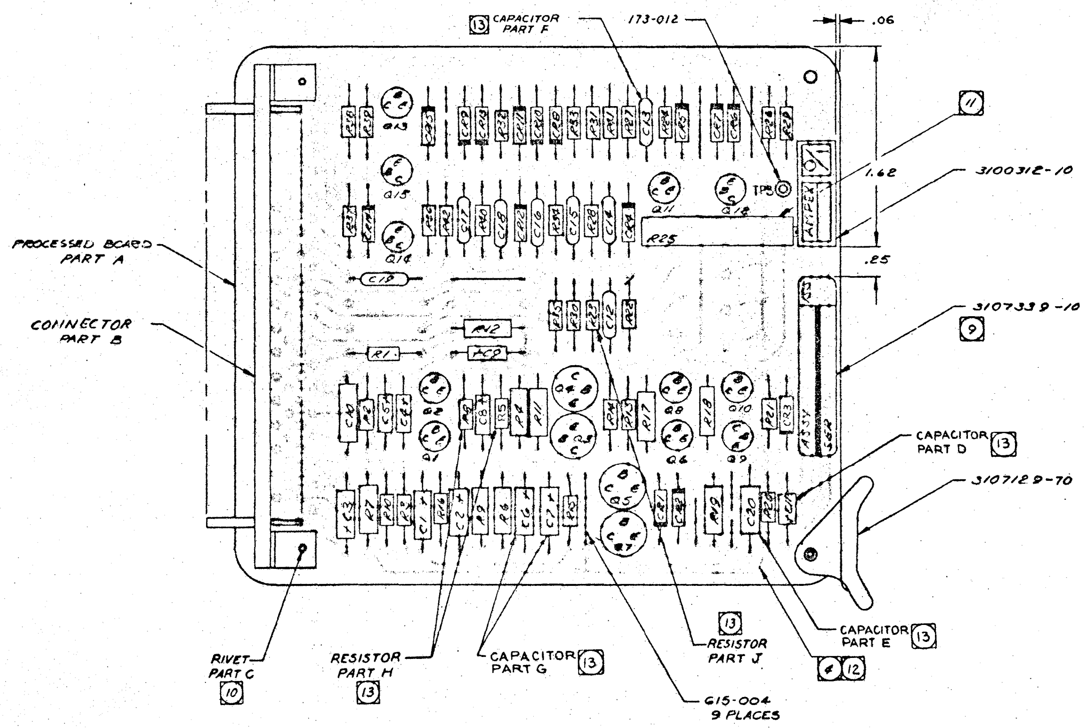
PART K	PART L	ASSEMBLY	FUNCTION	PART D	PART E	PART F	PART G	PART H	PART J
3212091-10	3201100-10	3107252-10	36 IPS	037-273	035-510	033-147	037-990	041-736	041-408
↕	↕	3107269-10	36 IPS	037-273	035-510	033-147	037-990	041-736	041-408
		3109475-10	75 IPS	037-034	034-319	034-278	037-990	041-396	041-560
		3110004-10	112.5-150 IPS	037-344	034-319	034-350	037-990	041-396	041-560
3212091-10	3201100-10	3113333-10	7.5 IPS	037-043	035-989	033-147	037-990	041-736	041-408
3212081-10	014-364	3116055-10	7.5 IPS	037-217	035-989	035-219	037-478	041-736	041-408
3212091-10	3201100-10	3118153-01	120 IPS	037-034	034-319	034-278	037-990	041-396	041-560

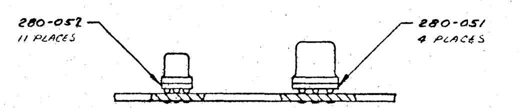
REVISIONS

ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
B	ECN 911-32 REDRAWN			
C	ECN 911-AM PROD.	Matzke		
D				
E	ECN 4612			
F	ECN 4657	Matzke		
G	ECN 4844			
H	ECN 4980			
J	ECN 5049	Aramaki		
K	ECN 5086			
L	ECN 5172		6/17/66	
M	ECN 5772	Aramaki		

PART NO.	REFERENCE DESIGNATIONS
PART J	R23
PART K	Q6

PART NO.	REFERENCE DESIGNATIONS
041-414	R3,10
PART L	Q7
3201104-10	Q8,9,13
3212091-10	Q1,2,
3212092-10	Q10,11,12,14,15
3212098-10	Q5
3201117-10	Q3,4
3263024-10	CR3 THRU CR15
3263028-10	CR1,2
034-417	C16,19
034-491	C14,17,18
034-493	C12,15
PART D	C11
035-989	C10
PART E	C20
PART F	C13
037-990	C1,2,3
041-408	R1,2, 31, 32,33
041-410	R15, 1[illegible]
041-411	R29,27
041-412	R22
041-413	R28,34,36,37,40
041-425	R13,14
041-430	R24
041-434	R35,41
041-482	R16,20,21
048-175	R17
041-519	R38,39
041-550	R30
041-570	R26
037-994	C8,9,4,5
PART H	R5,8
042-429	R19
048-051	R6,9
048-052	R4,7
048-053	R18
042-877	R11,12
044-197	R25
PART G	C6,C7





TYPICAL TRANSISTOR INSTALLATION

REFERENCE

(13) INSTALL PARTS D,E,F,G,H,J,K & L PER TABLE I.
(12) SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH. CORP. OR EQUIVALENT.
(11) TRIMPOT NOT TO BE SUBMERGED IN WATER.
(10) RIVET PART "C" USED ONLY WITH 3200526-10.
(9) MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.
8. PART NO. TO BE AS SHOWN IN BILL OF MATERIAL.
7. HEAVY LINE ON DIODE INDICATES CATHODE.
6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
(4) CIRCUITRY ON FARSIDE.
3. ASSEMBLE PER MANUFACTURING PRACTICES MANUAL.
2. FOR ASSEMBLY SPECIFICATION SEE 3107254.
1. FOR SCHEMATIC SEE 3107253.

NOTES:

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

NEXT ASSY	1ST USED ON
3118153	TM-11241
3116055	TM 7211
3110004	TM 11211
3107269	TM 7211
3107252	TM 7211

APPLICATION

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLLRANCES: DECIMALS XX ± .03 XXX ± .010, ANGLES ± 1/2°. BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII .010. ROUGHNESS OF ALL MACHINED SURFACES √ PER MIL-STD-10.

MATERIAL

FINISH

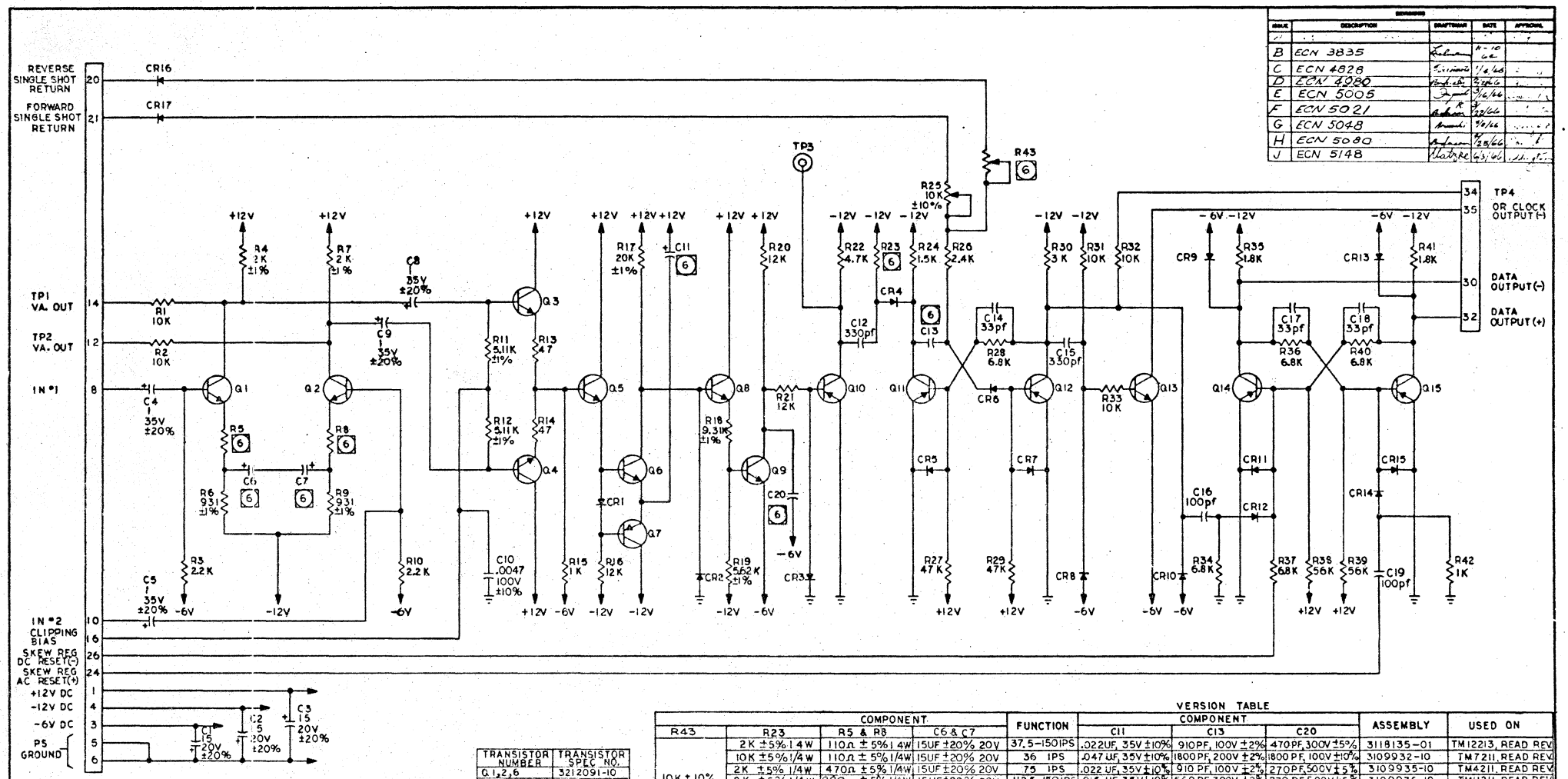
PROJ SUPER / PROJ ENGR / ENGR / CHKR K. BRINKMAN / DFTSMN L. KURATANI 11/7-63

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY - READ DESKEW UNSHARED

CODE INDENT. NO. | SIZE D | DWG. NO. 3107273 | ISSUE M
SCALE 2:1 | SHEET 1 OF 1

RDB



ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
B	ECN 3835		11-10-66	
C	ECN 4828		1/9/67	
D	ECN 4980		2/9/67	
E	ECN 5005		3/6/67	
F	ECN 5021		3/22/67	
G	ECN 5048		4/6/67	
H	ECN 5080		4/28/67	
J	ECN 5148		6/5/67	

TRANSISTOR NUMBER	TRANSISTOR SPEC NO.
Q 1,2,6	3212091-10
Q 3,4	3201117-10
Q 5	3212098-10
Q 7	3201100-10
Q 8,9,13	3201104-10
Q 10,11,12,14,15	3212092-10

VERSION TABLE

R43	COMPONENT R23	R5 & R8	C6 & C7	FUNCTION	COMPONENT C11	C13	C20	ASSEMBLY	USED ON
10K ±10%	2K ±5% 1/4W	110Ω ±5% 1/4W	15UF ±20% 20V	37.5-150IPS	.022UF, 35V ±10%	910PF, 100V ±2%	470PF, 300V ±5%	3118135-01	TM12213, READ REV.
	10K ±5% 1/4W	110Ω ±5% 1/4W	15UF ±20% 20V	36 IPS	.047 UF, 35V ±10%	1800 PF, 200V ±2%	1800 PF, 100V ±10%	3109932-10	TM7211, READ REV.
	2K ±5% 1/4W	470Ω ±5% 1/4W	15UF ±20% 20V	75 IPS	.022 UF, 35V ±10%	910 PF, 100V ±2%	270 PF, 500V ±5%	3109935-10	TM4211, READ REV.
	2K ±5% 1/4W	220Ω ±5% 1/4W	15UF ±20% 20V	112.5-150 IPS	.015 UF, 35V ±10%	560 PF, 300V ±2%	270 PF, 500V ±5%	3109936-10	TM11211, READ REV.
	10K ±5% 1/4W	110Ω ±5% 1/4W	70UF $^{-15\%}_{+20\%}$ 15V	10-100 IPS	.47UF, 35V ±10%	.01UF, 100V ±10%	.0047UF, 100V ±10%	3116107-10	TM7293 READ REV.
	10K ±5% 1/4W	110Ω ±5% 1/4W	15 UF ±20% 20V	30 IPS/1 INCH	.047 UF, 35V, ±10%	.0047 UF, 200V, ±1%	1800 PF, 100V, ±10%	3118154-01	TM 9241 READ REV.
20K ±10%	10K ±5% 1/4W	110Ω ±5% 1/4W	15UF ±20%, 20V	10/20 IPS	.1UF, 35V, ±5%	.0047UF, 200V ±1%	3300PF, 100V ±5%	3118198-01	TM 7293

6 SEE VERSION TABLE.

5. CR3 THRU CR17 TO BE 32630024-10.
4. CR1 AND CR2 TO BE 32630028-10.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 500V.
1. FOR ASSEMBLY SEE VERSION TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC - READ DESKEW, BI-DIRECTION

CODE IDENT. NO. | SIZE D | DWG. NO. 3109930 | ISSUE J

SCALE NONE | SHEET 1 OF 1

RDC

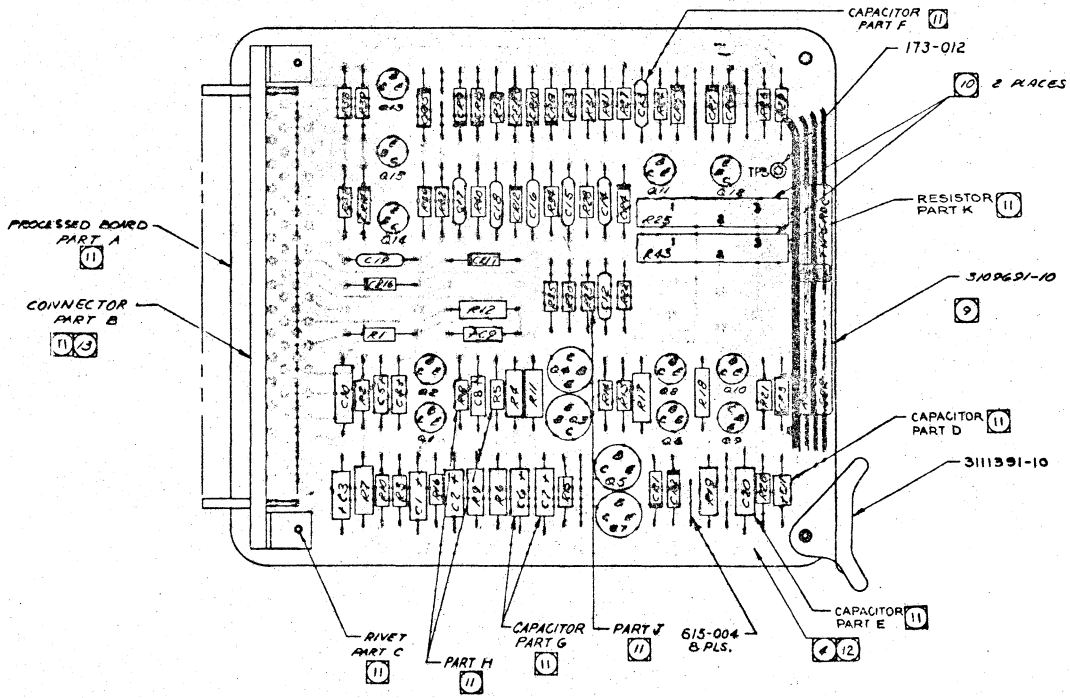
TABLE I

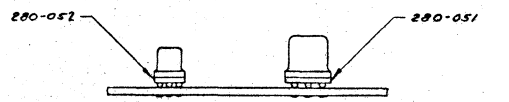
B/M REFERENCE TABLE

ASSEMBLY	FUNCTION	PART A	PART B	PART C	PART D	PART E	PART F	PART G	PART H	PART J	PART K
3109932-10	30 IPS	3107046-20	3200526-10	460-004	037-273	035-510	033-147	037-990	041-736	041-408	044-197
3109935-10	7.5 IPS	3107046-20	3200526-10	460-004	035-839	034-319	034-278	037-990	041-428	041-560	044-197
3109936-10	112.5-150 IPS	3107046-20	3200526-10	460-004	037-344	034-319	034-350	037-990	041-396	041-560	044-197
3116107-10	10-100 IPS	3107046-20	3200526-10	460-004	037-097	035-989	035-219	037-478	041-736	041-408	044-197
3118135-01	37.5-150 IPS	3107046-20	3200526-10	460-004	035-839	034-214	034-278	037-990	041-736	041-560	044-197
3118154-01	30 IPS / 1 INCH	3107046-20	3200526-10	460-004	037-273	035-510	055-128	037-990	041-736	041-408	044-197
3118198-01	10/20 IPS	3107046-20	3200526-10	460-004	037-453	035-422	055-128	037-990	041-736	041-408	044-313

REVISIONS

ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 110-A PROD.			
B	ECN 4392			
C	ECN 3755			
D	ECN 4828			
E	ECN 4980			
F	ECN 5005			
G	ECN 5021			
H	ECN 5048			
J	ECN 5080			
K	ECN 5148			





TYPICAL TRANSISTOR INSTALLATION

PART NO.	REFERENCE DESIGNATION
3201100-10	Q7
3201104-10	Q8,9,13
3212091-10	Q1,2,6
3212092-10	Q10,11,12,14,15
3212098-10	Q5
3201117-10	Q3,Q4
3263024-10	CR3 THRU CR17
3263028-10	CR1, CR2
034-417	C16, C19
034-491	C14, C17, C18
034-493	C12, C15
PART D	C11
041-414	R3, R10
PART K	R43

PART NO.	REFERENCE DESIGNATION
035-989	C10
PART F	C13
PART E	C20
037-990	C1,2,3,6,7
041-408	R1,2, 31,32,33
041-410	R15,42
041-411	R29,27
041-412	R22
041-413	R28,34,36,37,40
041-425	R13,14
041-430	R24
041-434	R35,41
041-482	R16,20,21
048-175	R17
041-519	R38,39
041-550	R30
041-570	R26
037-994	C8,9,4,5
PART H	R5,8
042-429	R19
048-051	R6,9
048-052	R4,7
048-053	R18
042-077	R11,12
044-197	R25
PART G	C6, C7
PART J	R23

REFERENCE

(13) TP1 @ CONNECTOR PIN 14. TP2 @ PIN 12.

(12) SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B1S, COLUMBIA TECH. CORP. OR EQUIVALENT.

(1) INSTALL PARTS A THRU K PER TABLE I.

(10) TRIMPOT NOT TO BE SUBMERGED IN WATER.

(9) MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

8. PART NO. TO BE AS SHOWN ON TABLE.
7. HEAVY LINE ON DIODE INDICATES CATHODE.
6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE
5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
(4) CIRCUITRY ON FARSIDE.
3. ASSEMBLE PER MANUFACTURING PRACTICES MANUAL.
2. FOR ASSEMBLY SPECIFICATION SEE 3107254.
1. FOR SCHEMATIC SEE 3109930.

NOTES:

3118154	TM-3241	DO NOT SCALE DRAWING		REQD	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM
3118135	TM12313	UNLESS OTHERWISE SPECIFIED TOLERANCES				LIST OF MATERIAL			
3116107	TM 7293	DECIMALS XX ± .03 XXX ± .010 BREAK ALL SHARP EDGES APPROX .010 CHAMF AND SPOTFACE CORNER RADII .010 ROUGHNESS OF ALL MACHINED SURFACES 125 PER MIL STD 10	ANGLES ± 1°						
3109935	TM4111 A-E								
3109936	TM4111 A-E								
3109932	TM4114 A-E	MATERIAL							
		FINISH							
NEXT ASSY	1ST USED ON								
APPLICATION									

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY AND IS LOANED SUBJECT TO RETURN UPON DEMAND AND WITH THE UNDERSTANDING THAT IT SHALL NOT BE COPIED OR USED IN WHOLE OR IN PART FOR THE BENEFIT OF ANYONE OTHER THAN AMPEX COMPUTER PRODUCTS CO.

PROJ		
SUPER.		5/4/64
DSGN		5/4/64
ENGR		5/4/64
ENGR		5/4/64
CHKR		5/4/64
DFTSMN		5/4/64

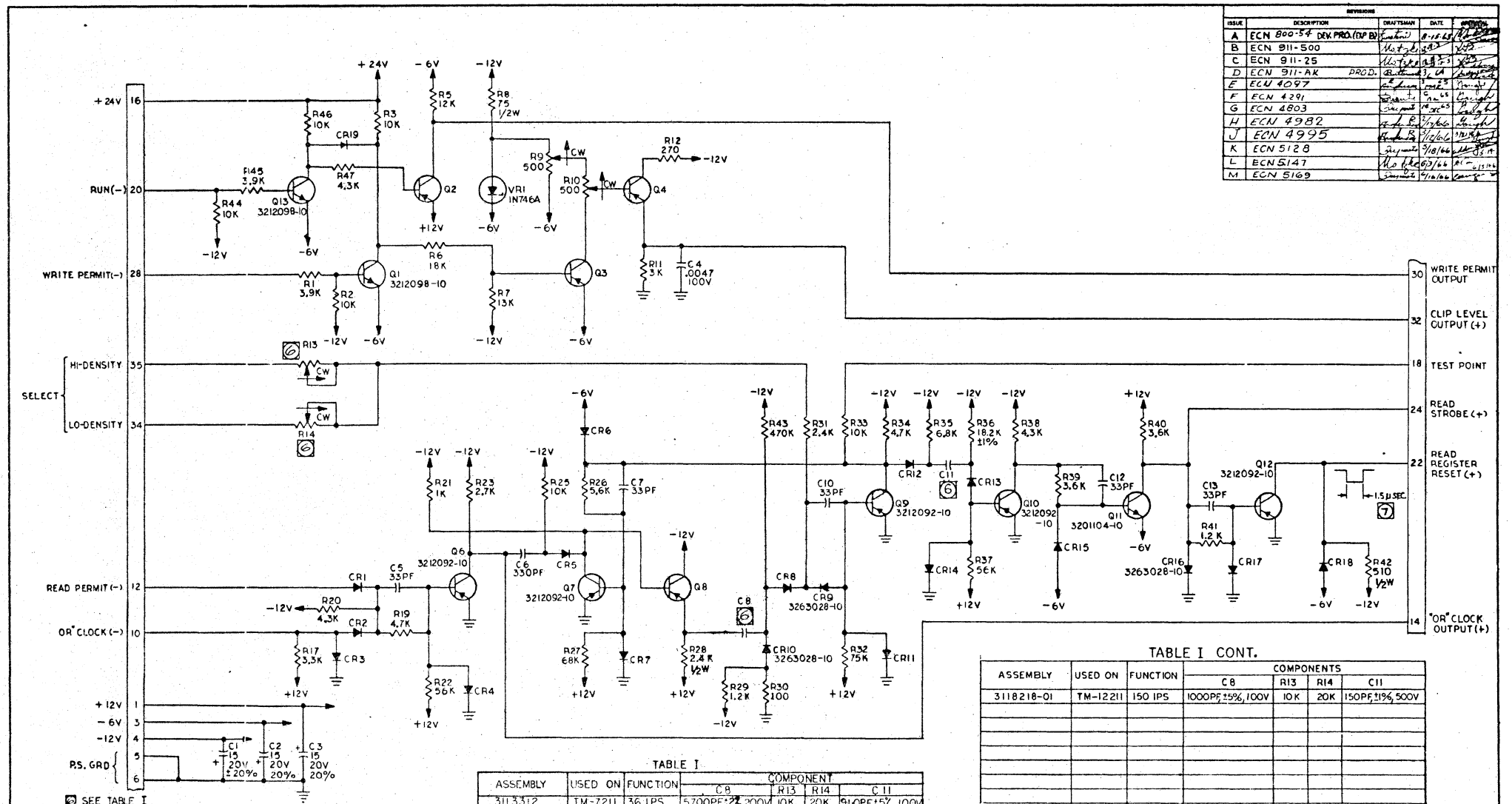
AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY- READ DESKEW, BI-DIRECTION

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3109933	K

SCALE 2:1

RDC



REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVED
A	ECN 800-54 DEV. PROD. (EXP B)		8-15-64	
B	ECN 911-500		10-23-64	
C	ECN 911-25		11-3-64	
D	ECN 911-AK PROD.		3-4-65	
E	ECN 4097		3-22-65	
F	ECN 4291		6-22-65	
G	ECN 4803		12-22-65	
H	ECN 4982		2-16-66	
J	ECN 4995		3-16-66	
K	ECN 5128		5-18-66	
L	ECN 5147		6-3-66	
M	ECN 5169		6-16-66	

TABLE I

ASSEMBLY	USED ON	FUNCTION	COMPONENT C8	R13	R14	C11
3113312	TM-7211	36 IPS	5700PF±2%,200V	10K	20K	910PF±5%,100V
3107057	TM-7211-12	36 IPS	5700PF±2%,200V	10K	20K	150PF±1%,500V
3113186	TM 7211	7.5 IPS	.033±2%, 200V	10K	20K	150PF±1%,500V
3109994	TM 4211	75 IPS	2800PF±2%,200V	10K	20K	150PF±1%,500V
3110003	TM 11211	12.5-120IPS	1800PF±2%,200V	10K	20K	150PF±1%,500V
3107277	TM 7211	36 IPS	5700PF±2%,200V	10K	20K	150PF±1%,500V
3112412	DE 213	75 IPS	.0022±10%, 100V	JUMPER	OPEN	150PF±1%,500V
3113187	TM 7211	15 IPS	.015 ± 2% , 200V	10K	20K	150PF±1%,500V
3116102	TM 7211 INTERMEDIATE	7.5 IPS	.033±2%,200V	10K	20K	620PF±5%,300V
3116164	TM 9241	30 IPS	5700PF±2%,200V	10K	20K	0.02μF±10%,100V
3118123	TM-7293	10/20 IPS	.01 ± 5% 100V	JUMPER	OPEN	620PF±5%,300V
3118189-01	DE-213	2.5/5/6.5 IPS	5700PF±2%,200V	JUMPER	OPEN	150PF±1%,500V

TABLE I CONT.

ASSEMBLY	USED ON	FUNCTION	COMPONENTS C8	R13	R14	C11
3118218-01	TM-12211	150 IPS	1000PF±5%,100V	10K	20K	150PF±1%,500V

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR ASSEMBLY SEE TABLE.
2. SEE TABLE I.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
4. ALL TRANSISTORS TO BE 3201100-10.
5. ALL DIODES TO BE 3263024-10

6. ALL CAPACITOR VALUES ARE IN MICROFARADS, 500V, ±10%.

7. RESET PULSE 8.0μs WIDE ON 3113312; 4.5μs WIDE ON 3116102

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS ANGLES
.XX ± .XXX ± ±
BREAK ALL SHARP EDGES APPROX .010 C'SUNK AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

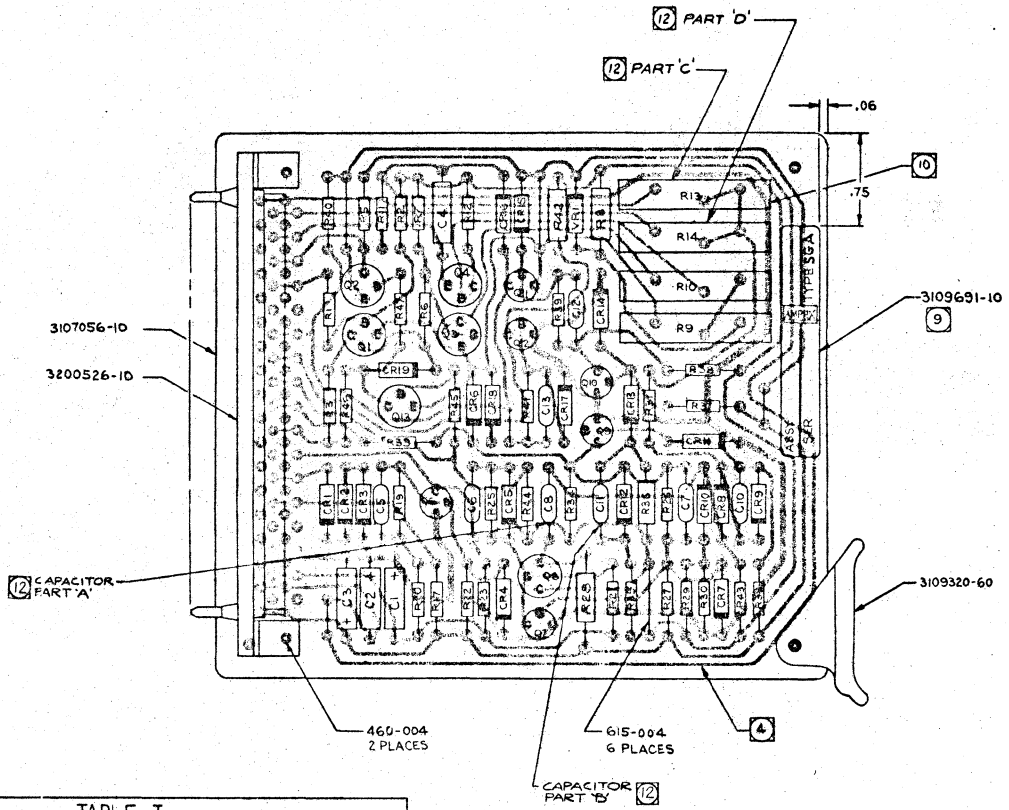
PROJ
SUPER
PROJ
ENGR
CHKR
DFTSMN

TITLE
SCHEMATIC—
STROBE GENERATOR

CODE IDENT. NO. | SIZE D | DWG. NO. 3107058 | ISSUE M
SCALE NONE | SHEET 1 OF 1

SGA

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-AK PROD.			
B	ECN 3849			
C	ECN 4097			
D	ECN 4803			
E	ECN 4982			
F	ECN 5169			
G	ECN 7003	E. REISS		

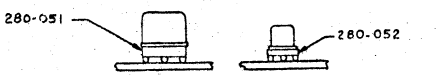


PART NO.	REFERENCE DESIGNATIONS
041-503	R12
041-507	R26
041-511	R1,45
041-512	R43
041-516	R8
041-519	R22,37
041-549	R7
041-550	R11
041-571	R39
041-570	R31
041-571	R40
041-573	R32
041-584	R20,38,47
041-419	R30
042-803	R36
PART C	R13
044-202	R9,10
PART D	R14
041-316	R28
041-440	R29,41
041-409	R42

PART NO.	REFERENCE DESIGNATIONS
3201100-10	Q2,3,4,8
3201104-10	Q11
3212092-10	Q6,7,9,10,12
3212098-10	Q1,13
3263024-10	CR1 THRU 8, CR11 THRU 15, CR17,18,19
3263028-10	CR9,10,16
813-T86	VR1
PART A	C8
034-491	C5,7,10,12,13
034-493	C6
PART B	C11
035-989	C4
037-990	C1,2,3
041-407	R17
041-408	R2,3,25,33,44,46
041-410	R21
041-412	R19,34
041-413	R35
041-415	R27
041-436	R6
041-442	R24
041-482	R5

TABLE I

B/M REFERENCE TABLE					USED ON
ASSY	PART 'A'	PART 'B'	PART 'C'	PART 'D'	
3107057	033-146	034-220	044-197	044-523	TM-7211
3109994	035-832	034-220	↑	↑	TM-4211
3110003	033-147	034-220	↑	↑	TM-11211
3107277	033-146	034-220	↑	↑	TM-7211
3113312	033-146	034-217	↑	↑	TM-7211
3116102	033-276	034-228	↑	↑	TM-7211 INTERSTATE
3116164	033-146	034-988	↑	↑	TM-9241
3118218	034-950	034-220	044-197	044-523	TM-12211
3113186	033-276	034-220	044-197	044-523	EAI-TM-7211



TYPICAL TRANSISTOR INSTALLATION

[12] INSTALL PER TABLE I.

11 SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH. CORP., OR EQUIV.

[10] TRIMPOTS NOT TO BE SUBMERGED IN WATER.

[9] MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

8. PART NO. TO BE AS SHOWN ON B/M.

7. HEAVY LINE ON DIODE INDICATES CATHODE.

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.

[4] CIRCUITRY ON FARSIDE.

3. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL.

12. FOR ASSEMBLY SPECIFICATION SEE 3107059.

1. FOR SCHEMATIC SEE 3107058.

NOTES:

REFERENCE

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES.
DECIMALS: XX ± .03, XXX ± .010
ANGLES: ± 1°
BREAK ALL SHARP EDGES APPROX. .010
C BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES 1 PER MIL STD-10

DRAFTSMAN		
DESIGNER		
PROJ. ENGR	S. BLANC	5/15/63
ENGR		5/15/63
CHKR	C. ANDERSON	5-17-63
CHTSMN	J. BUTTERWORTH	6-14-63

AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSEMBLY-STROBE GENERATOR

SEE TABLE		
NEXT ASSY.	1ST USED ON	
APPLICATION		

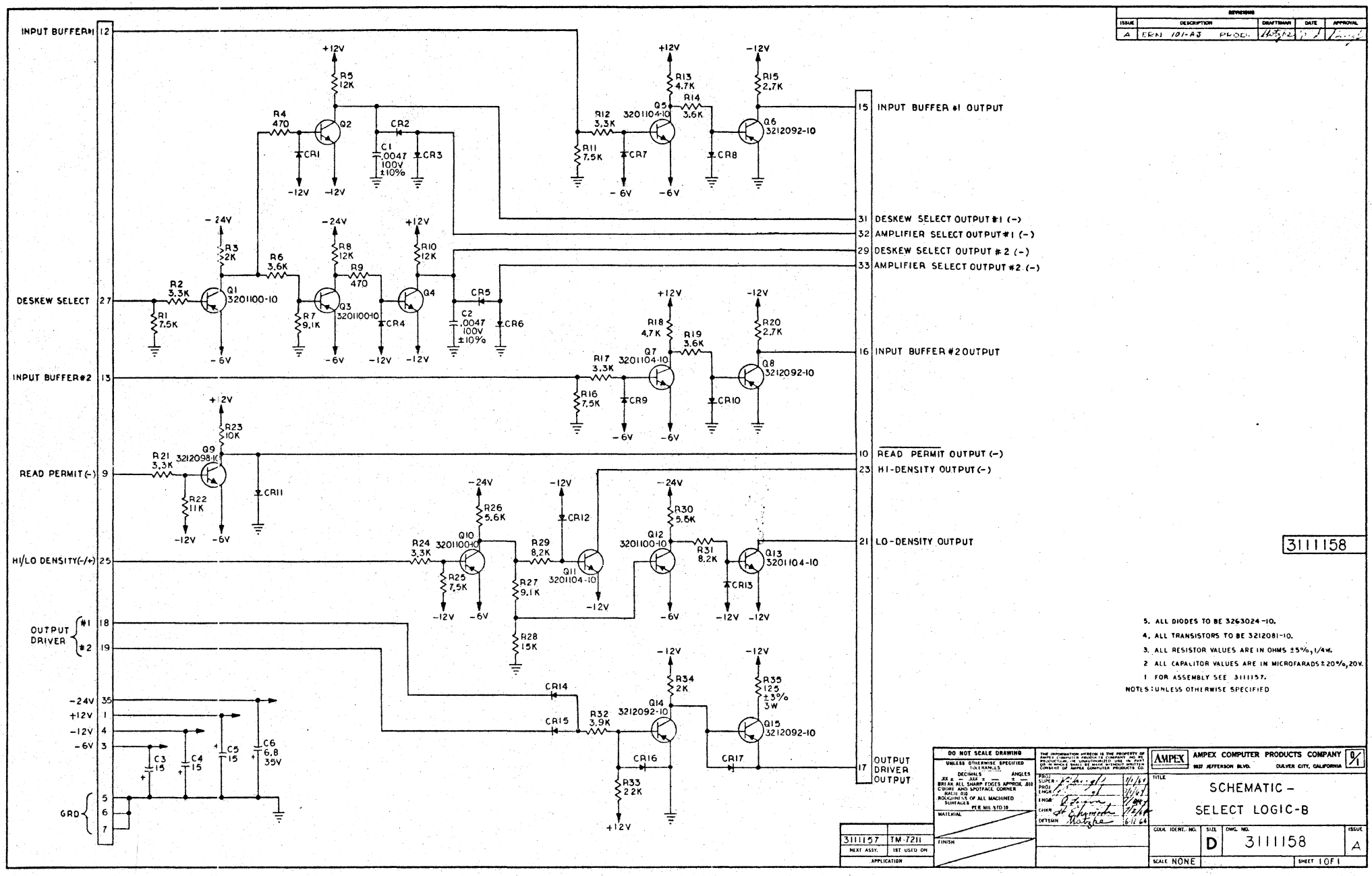
MATERIAL

FINISH

CODE IDENT. NO. | SIZE: D | DWG. NO. 3107276 | ISSUE: G

SCALE 2/1

SGA



REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ERN 101-A3 PROD.			

3111158

5. ALL DIODES TO BE 3263024-10.
4. ALL TRANSISTORS TO BE 3212081-10.
3. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS ±20%, 20V.
1. FOR ASSEMBLY SEE 3111157.

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS ANGLES
.XX ± .01 ± .X ± 1°
BREAK ALL SHARP EDGES APPROX. .010 CROWN AND SPOTFACE CORNER
FINISH PER ROUGHNESS OF ALL MACHINED SURFACES PER MIL STD 10
MATERIAL
FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS CO. AND IS NOT TO BE REPRODUCED OR USED IN WHOLE OR IN PART WITHOUT THE CONSENT OF AMPEX COMPUTER PRODUCTS CO.

DRAWN		
SUPER.		
PROJ.		7/1/64
ENGR		7/1/64
CHKR		7/1/64
DFTSMN	Matzke	6-11-64

3111157	TM-7211
NEXT ASSY.	1ST USED ON
APPLICATION	

AMPEX COMPUTER PRODUCTS COMPANY 9/1
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

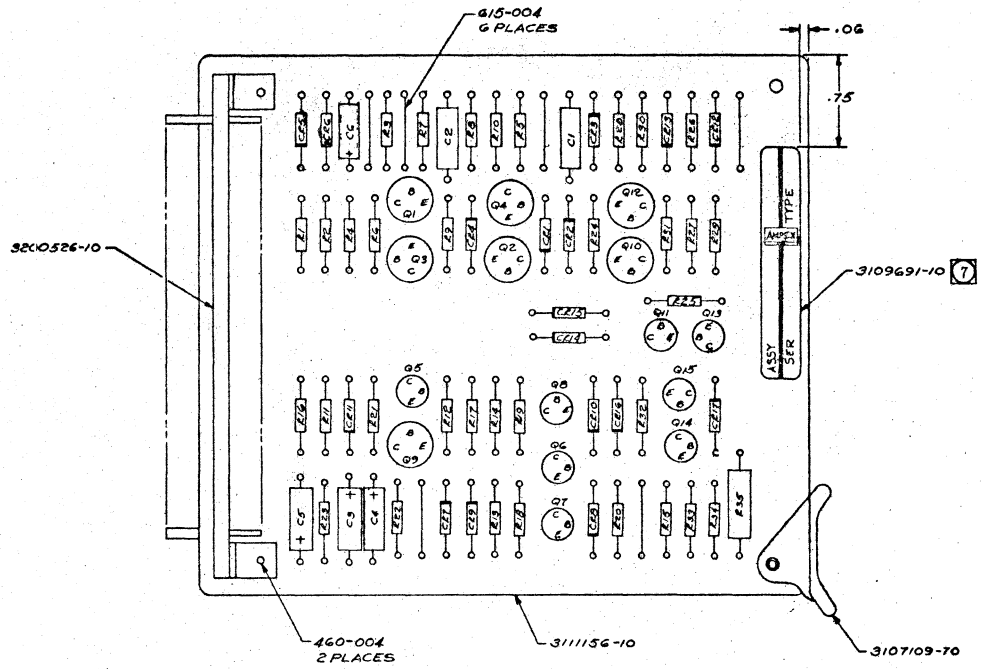
TITLE
SCHEMATIC -
SELECT LOGIC-B

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3111158	A

SCALE NONE SHEET 1 OF 1

SLB

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ERN 101-AJ PROD.		7/1/68	

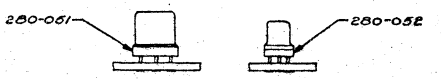


PART NO.	REFERENCE DESIGNATION
3201100-10	Q1,Q3,Q10,Q12
3201104-10	Q5,Q7,Q11,Q13
3212081-10	Q2,Q4
3212092-10	Q6,Q8,Q14,Q15
3212098-10	Q9
3263024-10	CR1 THRU CR17
035-989	C1,C2
037-095	C6
037-990	C3,C4,C5
041-406	R33
041-407	R2,R12,R17,R21,R24
041-408	R23
041-409	R28
041-412	R13,R18
041-428	R4,R9
041-442	R15,R20
041-482	R5,R8,R10
041-495	R29,R31
041-507	R26,R30
041-511	R32
041-514	R7,R27
041-520	R1,R11,R16,R25
041-560	R3,R34
041-571	R6,R14,R19
047-302	R35
041-748	R22

3111157

8. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1815 COLUMBIA TECH. CORP. OR EQUIVALENT.
7. MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.
6. PART NO. TO BE 3111157-10.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. HEAVY LINE ON DIODE INDICATES CATHODE.
3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.
2. FOR ASSEMBLY SPECIFICATION SEE 3111159.
1. FOR SCHEMATIC SEE 3111158.

NOTES:



TYPICAL TRANSISTOR INSTALLATION

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010 C'SKORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
IMPERIAL
METRIC

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. ANY REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ SUPER		7/1/68
PROJ ENGR		7/1/68
ENGR		7/1/68
CHKR		7/1/68
DFTSMN		7/1/68

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

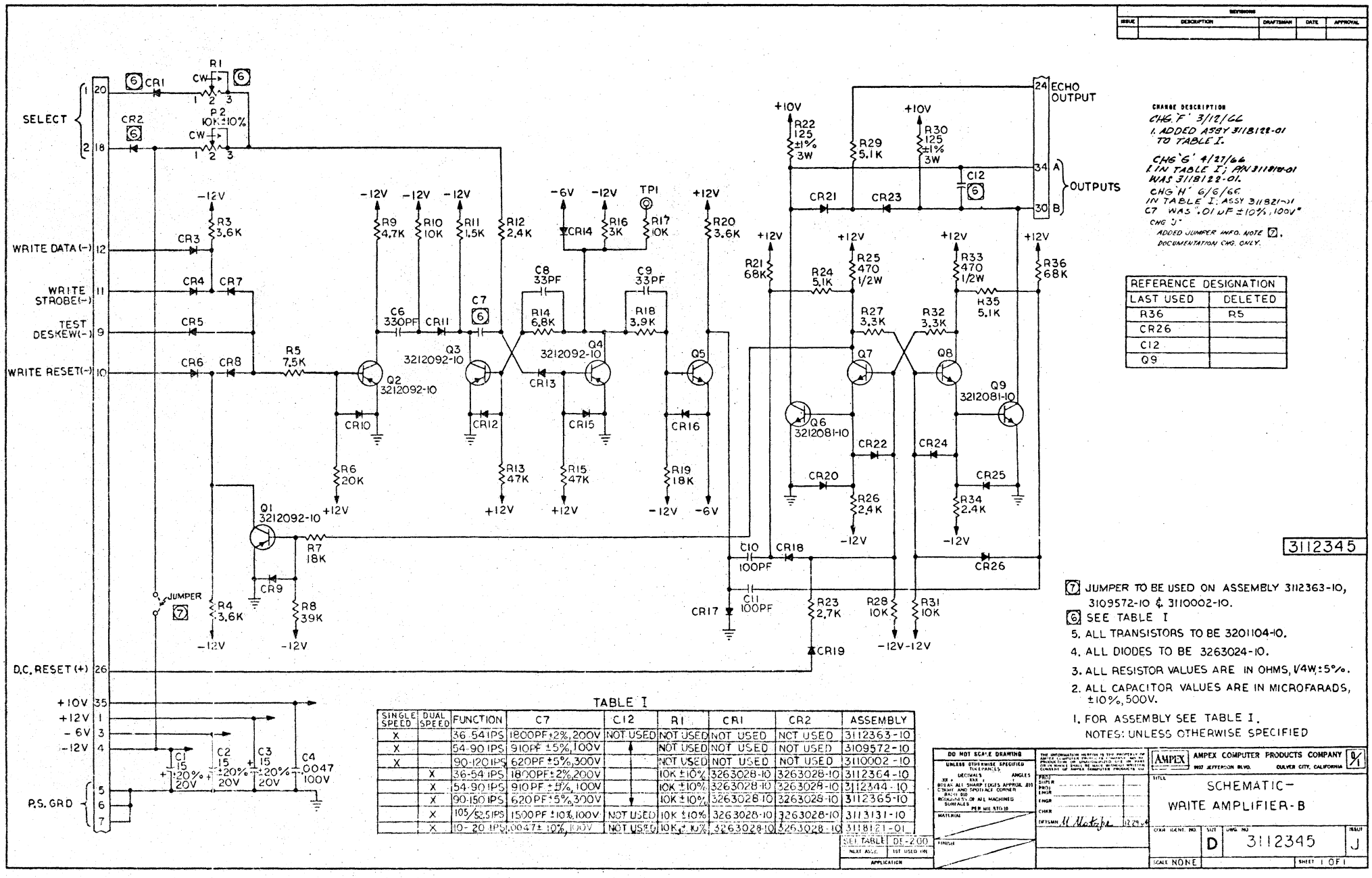
TITLE
CIRCUIT BOARD ASSY-
SELECT LOGIC-B

FINAL APPL.	TM-7611
NEXT ASSY.	1ST USED ON
APPLICATION	

CODE IDENT. NO. | SIZE D | DWG. NO. 3111157 | ISSUE A

SCALE 2/1 SHEET 1 OF 1

SLB



REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL

CHANGE DESCRIPTION

CHG 'F' 3/12/66
1. ADDED ASSY 3118128-01 TO TABLE I.

CHG 'G' 4/27/66
1. IN TABLE I; ASSY 3118128-01 WAS 3118128-01.

CHG 'H' 6/6/66
IN TABLE I: ASSY 3118121-01 C7 WAS ".01 UF ±10%, 100V"

CHG 'J'
ADDED JUMPER INFO. NOTE [7].
DOCUMENTATION CHG. ONLY.

REFERENCE DESIGNATION	
LAST USED	DELETED
R36	R5
CR26	
C12	
Q9	

3112345

[7] JUMPER TO BE USED ON ASSEMBLY 3112363-10, 3109572-10 & 3110002-10.

[6] SEE TABLE I

5. ALL TRANSISTORS TO BE 3201104-10.
4. ALL DIODES TO BE 3263024-10.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 500V.
1. FOR ASSEMBLY SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

TABLE I

SINGLE SPEED	DUAL SPEED	FUNCTION	C7	C12	R1	CR1	CR2	ASSEMBLY
X		36-54 IPS	1800PF±2%, 200V	NOT USED	NOT USED	NOT USED	NOT USED	3112363-10
X		54-90 IPS	910PF ±5%, 100V		NOT USED	NOT USED	NOT USED	3109572-10
X		90-120 IPS	620PF ±5%, 300V		NOT USED	NOT USED	NOT USED	3110002-10
	X	36-54 IPS	1800PF±2%, 200V		10K ±10%	3263028-10	3263028-10	3112364-10
	X	54-90 IPS	910PF ±5%, 100V		10K ±10%	3263028-10	3263028-10	3112344-10
	X	90-150 IPS	620PF ±5%, 300V		10K ±10%	3263028-10	3263028-10	3112365-10
	X	105/52.5 IPS	1500PF ±10%, 100V	NOT USED	10K ±10%	3263028-10	3263028-10	3113131-10
	X	10-20 IPS	.0047± 10%, 100V	NOT USED	10K ±10%	3263028-10	3263028-10	3118121-01

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
TOLERANCES
DECIMALS ANGLES
MATERIAL
FINISH
SEE TABLE DE-200
NEXT ASSY 1ST USED ON
APPLICATION

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX CORPORATION AND SHALL NOT BE REPRODUCED OR USED IN WHOLE OR IN PART WITHOUT WRITTEN PERMISSION OF AMPEX CORPORATION.

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

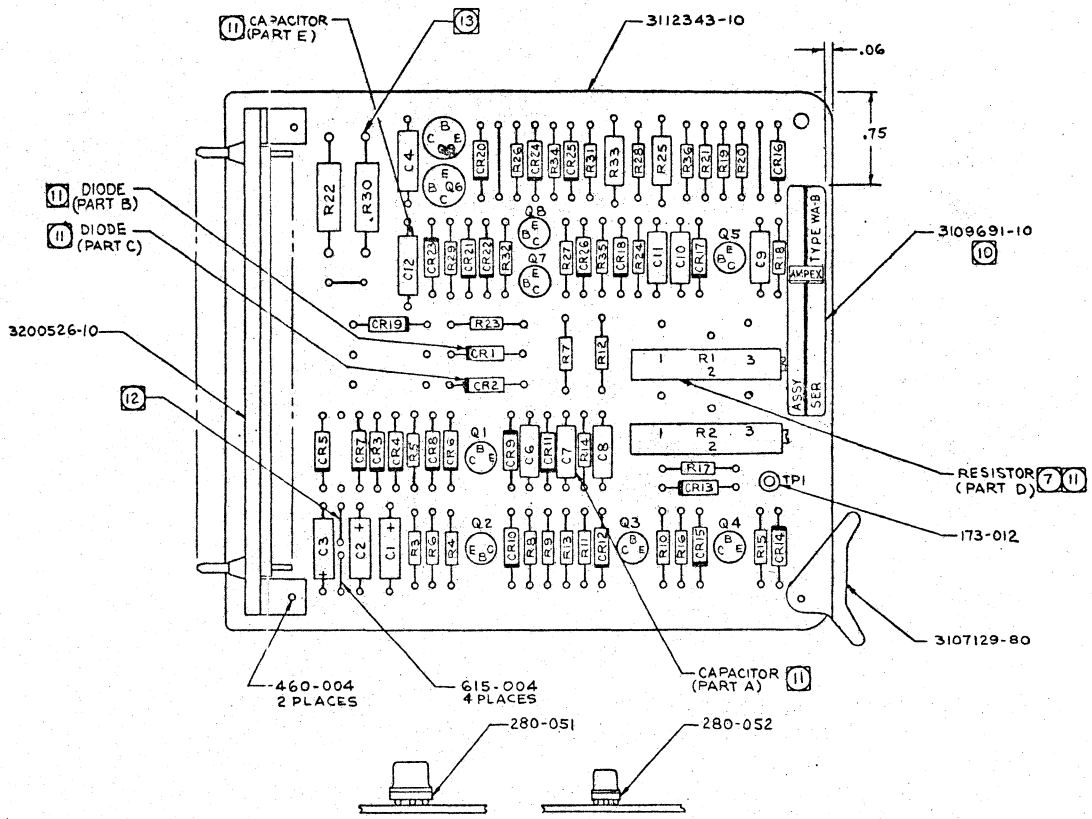
DRAFTSMAN M. Mathys 12-29-65

TITLE
SCHEMATIC-
WRITE AMPLIFIER-B

CAGE IDENT. NO. | SIZE D | DWG. NO. 3112345 | REV J
SCALE NONE | SHEET 1 OF 1

WAB

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
G	ECN 4454 PROD. RELEASE	[illegible]	7/28/65	[illegible]
H	ECN 4522	[illegible]	9/10/65	[illegible]
J	ECN 4995	[illegible]	3/10/66	[illegible]
K	ECN 5084	[illegible]	5/9/66	[illegible]
L	ECN 5151	[illegible]	6/6/66	[illegible]



TYPICAL TRANSISTOR INSTALLATION

PART NO.	REFERENCE DESIGNATION	PART NO.	REFERENCENCE DESIGNATION
041-442	R23	3201104-10	Q5, Q7, Q8
041-443	R8	3212081-10	Q6, Q9
041-511	R18	3212092-10	Q1, Q2, Q3, Q4
041-520	R5	3263024-10	CR3 THRU CR26
041-571	R3, R4, R20	PART B	CR1
041-550	R16	PART A	C7
041-561	R24, R29, R35	034-417	C10, C11
041-570	R12, R26, R34	034-491	C8, C9
041-571	R20	034-493	C6
041-508	R6	035-989	C4
041-415	R21, R36	037-990	C1, C2, C3
044-197	R2	041-336	R25, R33
047-340	R22, R30	041-407	R27, R32
PART C	CR2	041-408	R10, R17, R28, R31
PART D	R1	041-411	R13, R15
PART E	C12	041-412	R9
		041-413	R14
		041-430	R11
		041-436	R19, R7

(13) INSTALL R22 & R30 PER PRODUCTION PRACTICES MANUAL, SECTION 7 HE2-5, FIGURE 10, HIGH WATTAGE RESISTOR SPACING.

(12) INSTALL JUMPER ONLY ON ASSEMBLY 3112363-10, 3109572-10 & 3110002-10.

(11) INSTALL PARTS A,B,C,D,E PER TABLE I.

(10) MARK PART NO. & NAMEPLATE INFORMATION PER MIL-STD-130.

9. PART NO. TO BE AS SHOWN ON TABLE I.
8. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE IB15 COLUMBIA TECH. CORP. OR EQUIV.
(7) TRIMPOTS NOT TO BE SUBMERGED IN WATER.
6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
5. HEAVY LINE ON DIODE INDICATES CATHODE.
4. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.
2. FOR ASSY SPECIFICATION SEE TABLE
1. FOR SCHEMATIC SEE 3112345.

NOTES:

3112347

REFERENCE

TABLE I

B/M REFERENCE TABLE						ASSEMBLY
ASSEMBLY	PART A	PART B	PART C	PART D	PART E	SPECIFICATION
3112363-10	033-147	NOT USED	NOT USED	NOT USED	NOT USED	3112346
3109572-10	034-386	NOT USED	NOT USED	NOT USED	NOT USED	
3110002-10	034-228	NOT USED	NOT USED	NOT USED	NOT USED	
3112364-10	033-147	3263028-10	3263028-10	044-197	NOT USED	
3112344-10	034-386	3263028-10	3263028-10	044-197	NOT USED	
3112365-10	034-228	3263028-10	3263028-10	044-197	NOT USED	
3113131-10	035-509	3263028-10	3263028-10	044-197	NOT USED	3113154
3118121-01	035-989	3263028-10	3263028-10	044-197	NOT USED	3113154

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES

DECIMALS XX ± .03 XXX ± .010 BREAK ALL SHARP EDGES APPROX .010 C'BORE AND SPOTFACE CORNER RAISH 010 ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

ANGLES

MATERIAL

FINISH

SEE TABLE I	DE-200
NEXT ASSY.	1ST USED ON
APPLICATION	

PROJ		
MATER	[illegible]	7/5/65
PHOT	[illegible]	7/9/65
ENGR	[illegible]	7/15/65
ENGR	[illegible]	7/15/65
CHKR	[illegible]	8/9/65
DFTSMN	H. Matzke	8/6/65

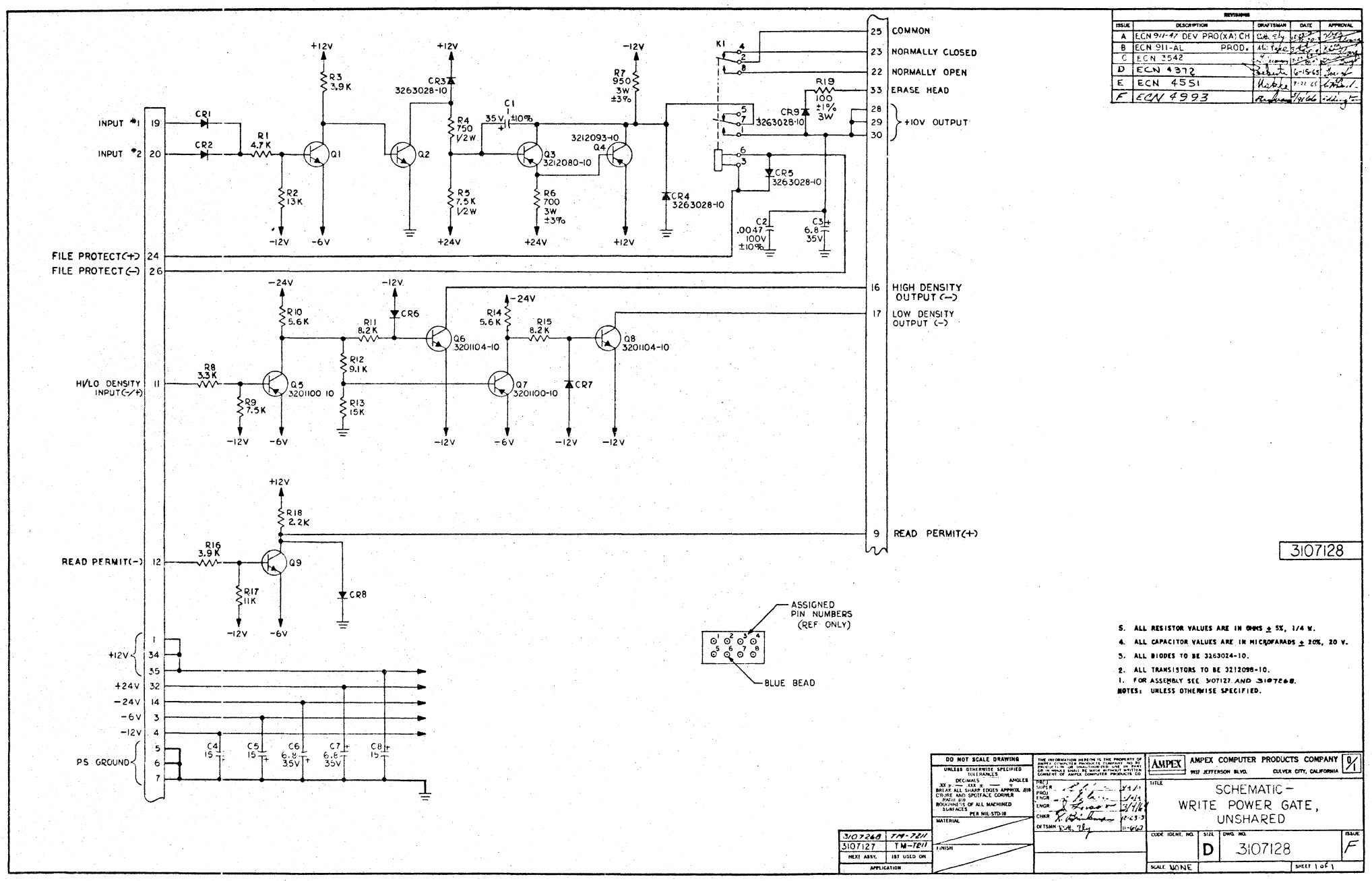
AMPEX AMPEX COMPUTER PRODUCTS COMPANY 9/1
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY- WRITE AMPLIFIER-B

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3112347	L

SCALE 2:1 SHEET 1 OF 1

WAB



REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-17 DEV PRO(XA) CH	[illegible]	[illegible]	[illegible]
B	ECN 911-AL PROD.	[illegible]	[illegible]	[illegible]
C	ECN 3542	[illegible]	[illegible]	[illegible]
D	ECN 4372	[illegible]	6-15-65	[illegible]
E	ECN 4551	[illegible]	[illegible]	[illegible]
F	ECN 4993	[illegible]	9/16/66	[illegible]

3107128

5. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4 W.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS ± 20%, 20 V.
3. ALL DIODES TO BE 3263024-10.
2. ALL TRANSISTORS TO BE 3212098-10.
1. FOR ASSEMBLY SEE 307127 AND 3107268.

NOTES: UNLESS OTHERWISE SPECIFIED.

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .01
ANGLES ±
BREAK ALL SHARP EDGES APPROX .010 CHAMFER AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH

3107268	TM-7211
3107127	TM-7211
NEXT ASSY.	1ST USED ON
APPLICATION	

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PROJ
SUPER
PROJ
ENGR
ENGR
CHKR
DFTSMN

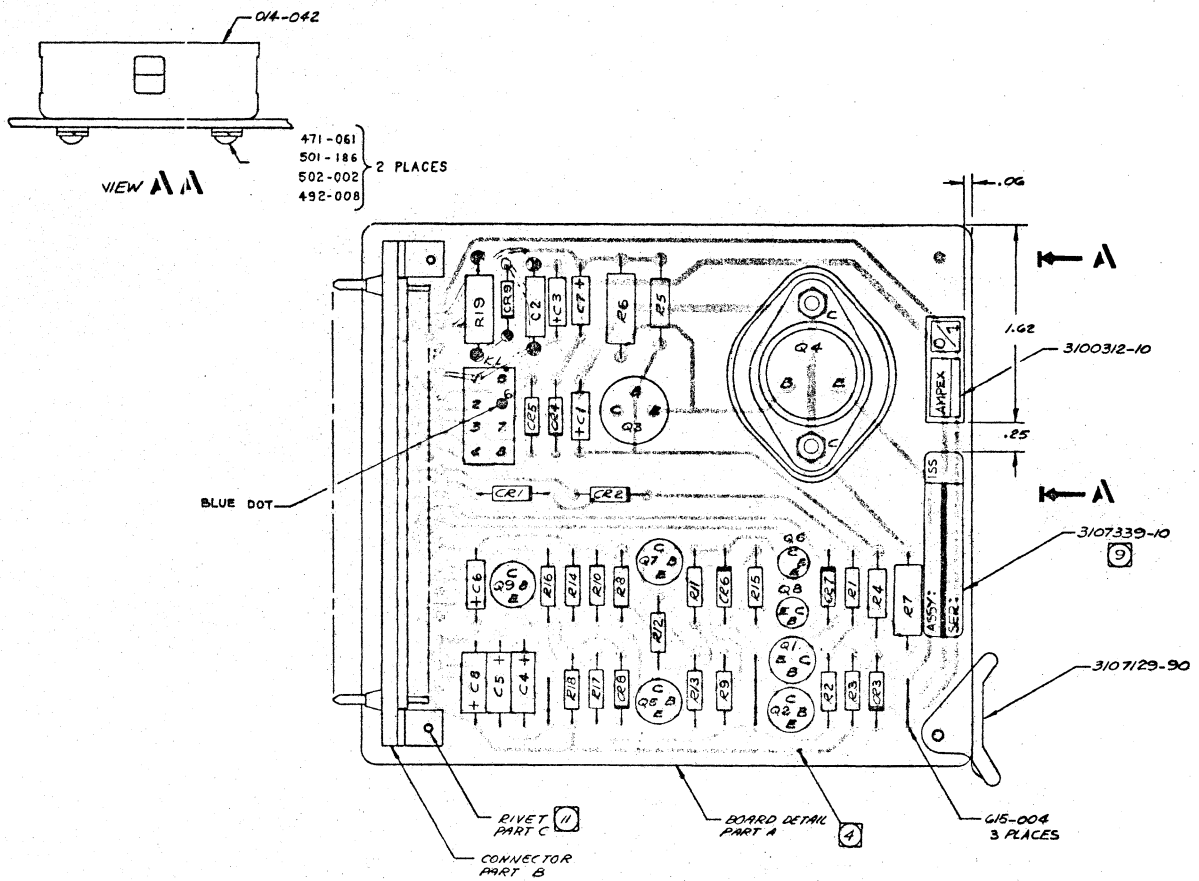
AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

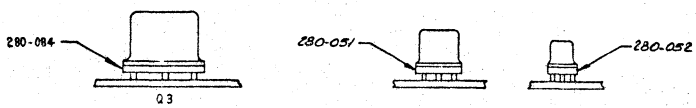
TITLE
SCHEMATIC — WRITE POWER GATE, UNSHARED

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107128	F

SCALE NONE SHEET 1 OF 1

WPD





TYPICAL TRANSISTOR INSTALLATION

REFERENCE

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-AL DEVREQ(X-A)CN			
B	ECN 911-AL PROD.			
C	ECN 3542			
D	ECN 3750			
E	ECN 4312			
F	ECN 4551			
G	ECN 7082			

PART NO.	REFERENCE DESIGNATIONS
3201100-10	Q5,7
3201104-10	Q6,8
3212080-10	Q3
3212093-10	Q4
3212098-10	Q1,2,9
3263024-10	CR1,2,6,7,8
3263028-10	CR3,4,5,9
035-989	C2
037-095	C3,6,7
037-265	C1
037-990	C4,5,8
041-007	R4
041-361	R5
041-407	R8
041-414	R16
041-409	R13
041-412	R1
041-495	R11,15
041-507	R10,14
041-511	R3,16
041-514	R12
041-520	R9
041-549	R2
041-748	R17
047-408	R6
047-632	R7
020-233	K1
047-764	R19

3107272

11. RIVET, PART C USED ONLY WITH 3200526-10.
10. PART NO. TO BE AS SHOWN IN BILL OF MATERIAL.
9. MARK PART NO. AND SERIAL NO. PER MIL-STD-130.
8. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15 COLUMBIA TECH. CORP., OR EQUIVALENT.
7. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
6. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
5. ASSEMBLE PER MANUFACTURING PRACTICES MANUAL.
4. CIRCUITRY ON FAR SIDE.
3. HEAVY LINE ON DIODE INDICATES CATHODE.
2. FOR ASSEMBLY SPECIFICATION SEE 3107121
1. FOR SCHEMATIC SEE 3107128.

NOTES:

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS XX ± .03 XXX ± .010 BREAK ALL SHARP EDGES APPROX .010 C'BORE AND SPOTFACE CORNER RADII .010 SMOOTHNESS OF ALL MACHINED SURFACES 1 PER MIL STD 10
ANGLES ± 1°

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LIST OF MATERIAL

3107268	7M-7211	MATERIAL	
3107127	7M7211		
NEXT ASSY	1ST USED ON	FINISH	
APPLICATION			

PROJ		
SUPER		
PROJ ENGR		
ENGR		
CHKR		
DFTSMN		

AMPEX 01 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

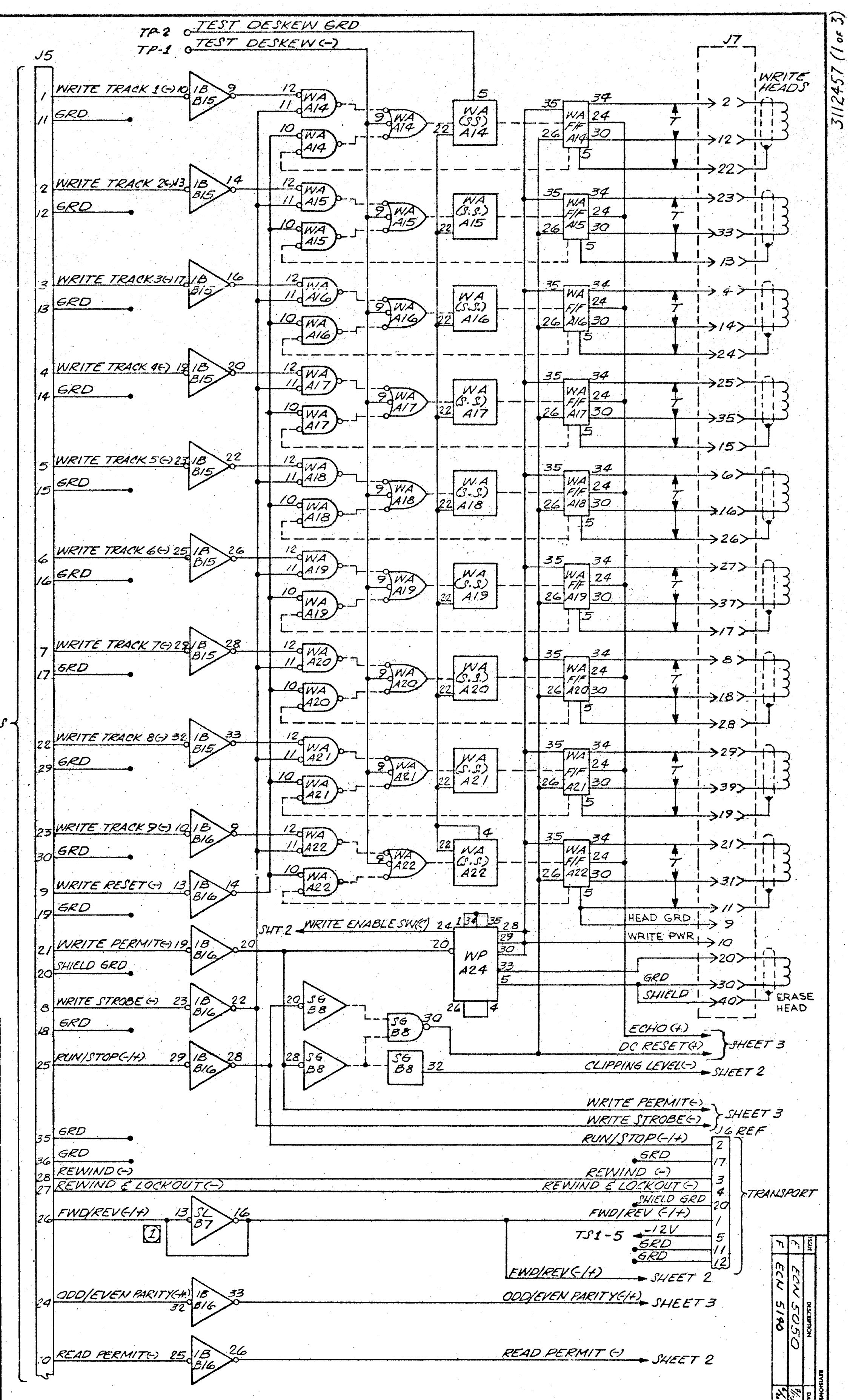
TITLE: CIRCUIT BOARD ASSY-WRITE POWER GATE, UNSHARED

CODE IDENT NO	SIZE	DWG NO.	ISSUE
	D	3107272	G

SCALE 2/1

WPD

311245 7 (1 of 3)



NOTES:

[2] FOR UNSTROBED OUTPUTS REMOVE WIRE FROM B13-31 TO B13-34, ADD WIRE FROM B13-31 TO B13-5.

[1] ON READ FWD ONLY SYSTEMS B7 IS OMITTED & JUMPERS B7-31 TO B7-4 AND B7-13 TO B7-16 ARE ADDED.

REVISIONS				
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	APPROVAL
E	ECN 5050			
F	ECN 5190			

NEXT ASSY.	1ST USED ON
3115770	TM-7211
3112460	TM-7211
APPLICATION	

DO NOT SCALE DRAWING

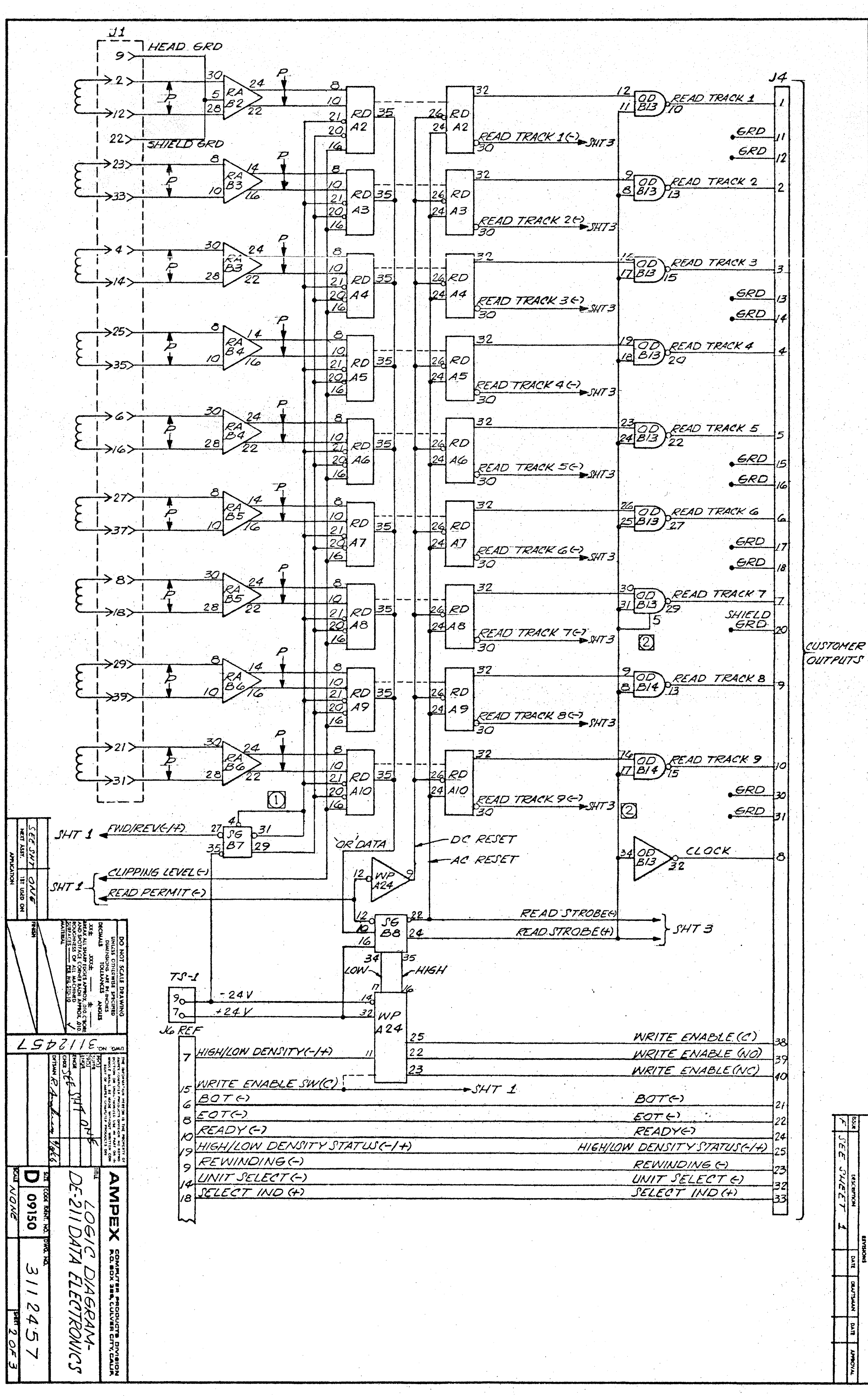
AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE: LOGIC DIAGRAM-DE-211 DATA ELECTRONICS

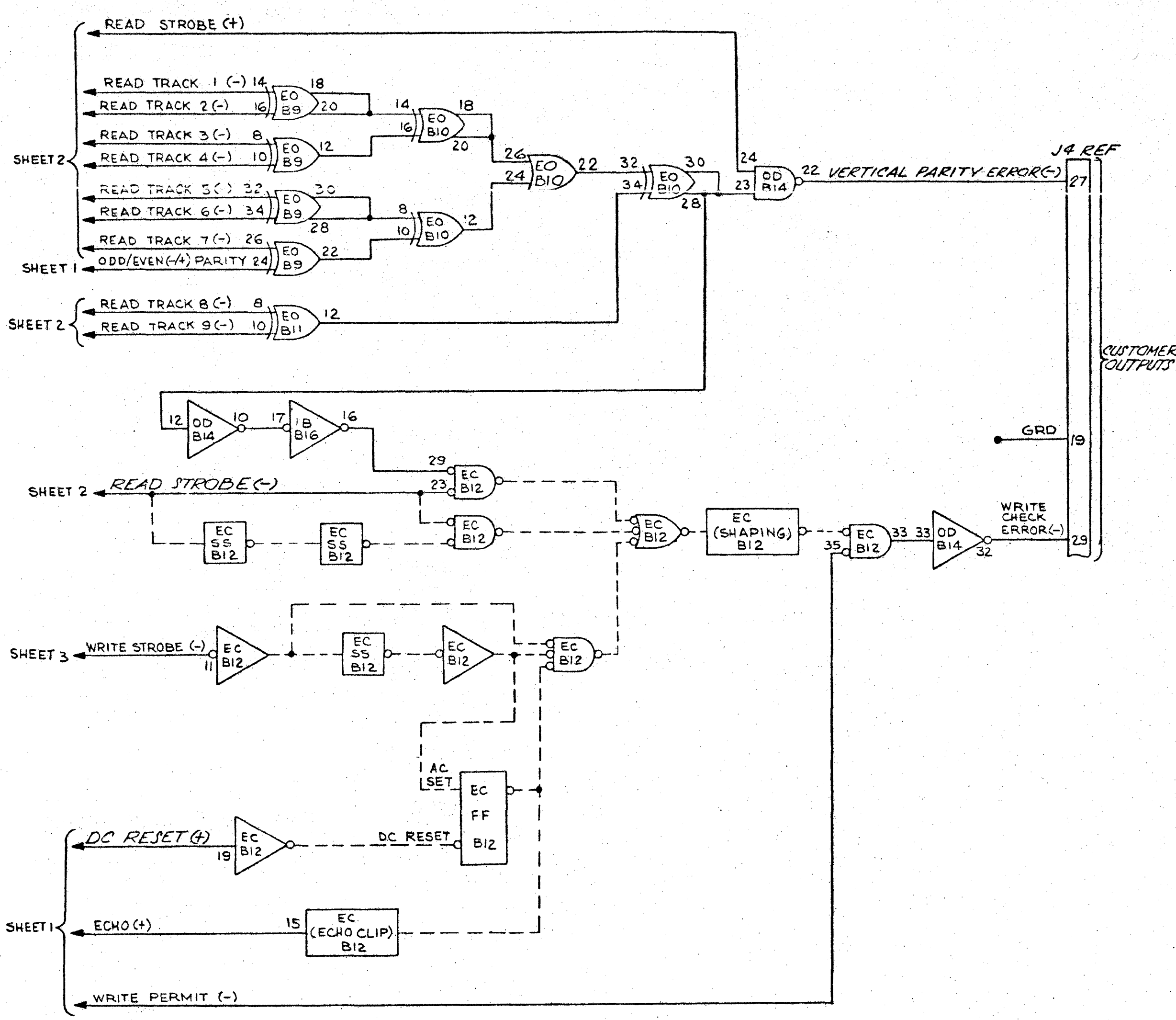
SIZE D | CODE IDENT. NO. 09150 | DWG. NO. 311245 7

SCALE NONE | SHEET 1 OF 3

3112457 (2 of 3)



3112457 (3 of 3)



NEXT ASSY.	1ST USED ON
SEE SHEET I	

APPLICATION

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES

MATERIAL

FINISH

DFTSMN

CHKR SEE SHT 1

ENGR

AMPEX COMPUTER PRODUCTS COMPANY, 9937 JEFFERSON BLVD., CULVER CITY, CALIFORNIA

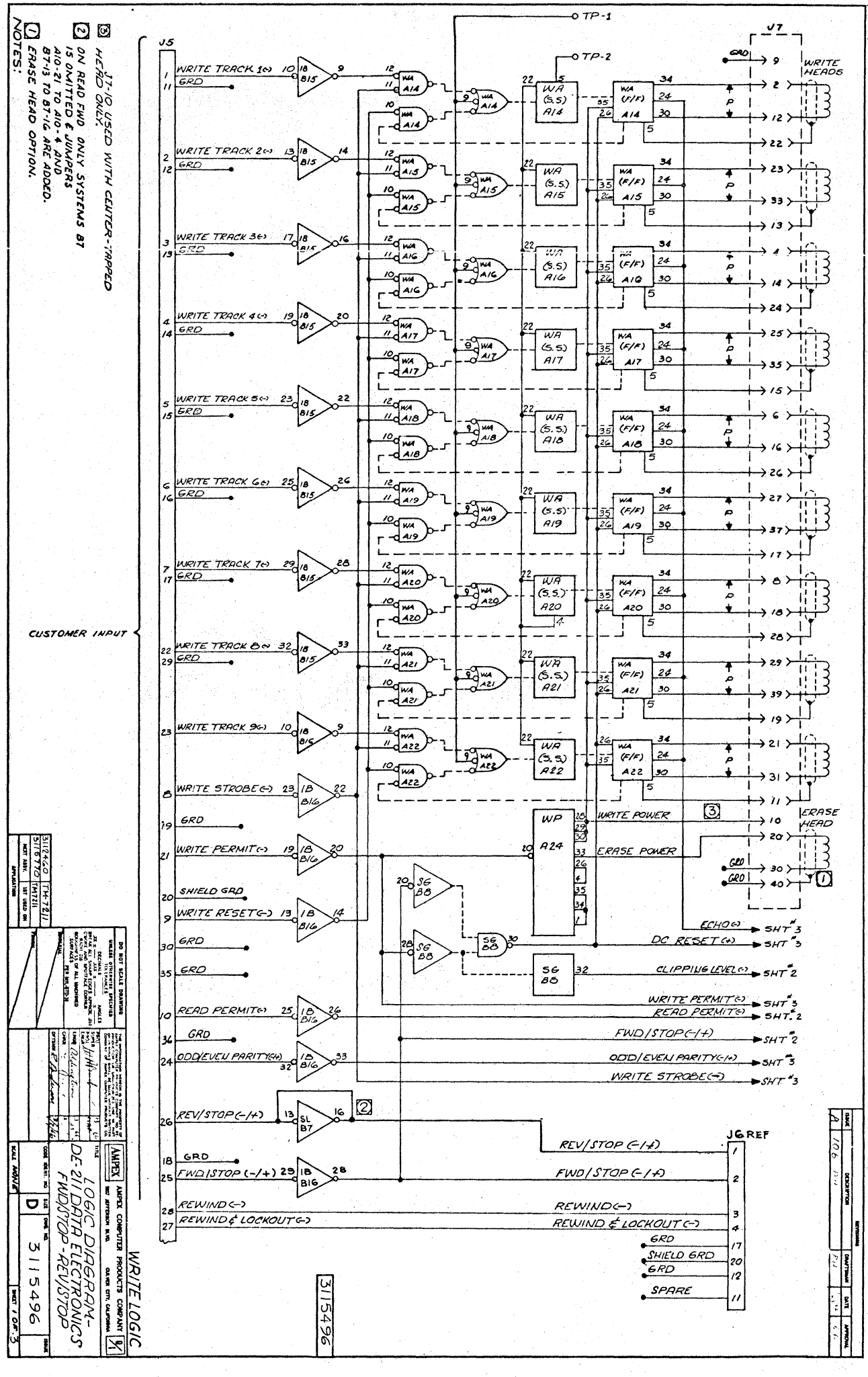
TITLE: ERROR CHECK OPTION — LOGIC DIAGRAM - DE-21 DATA ELECTRONICS

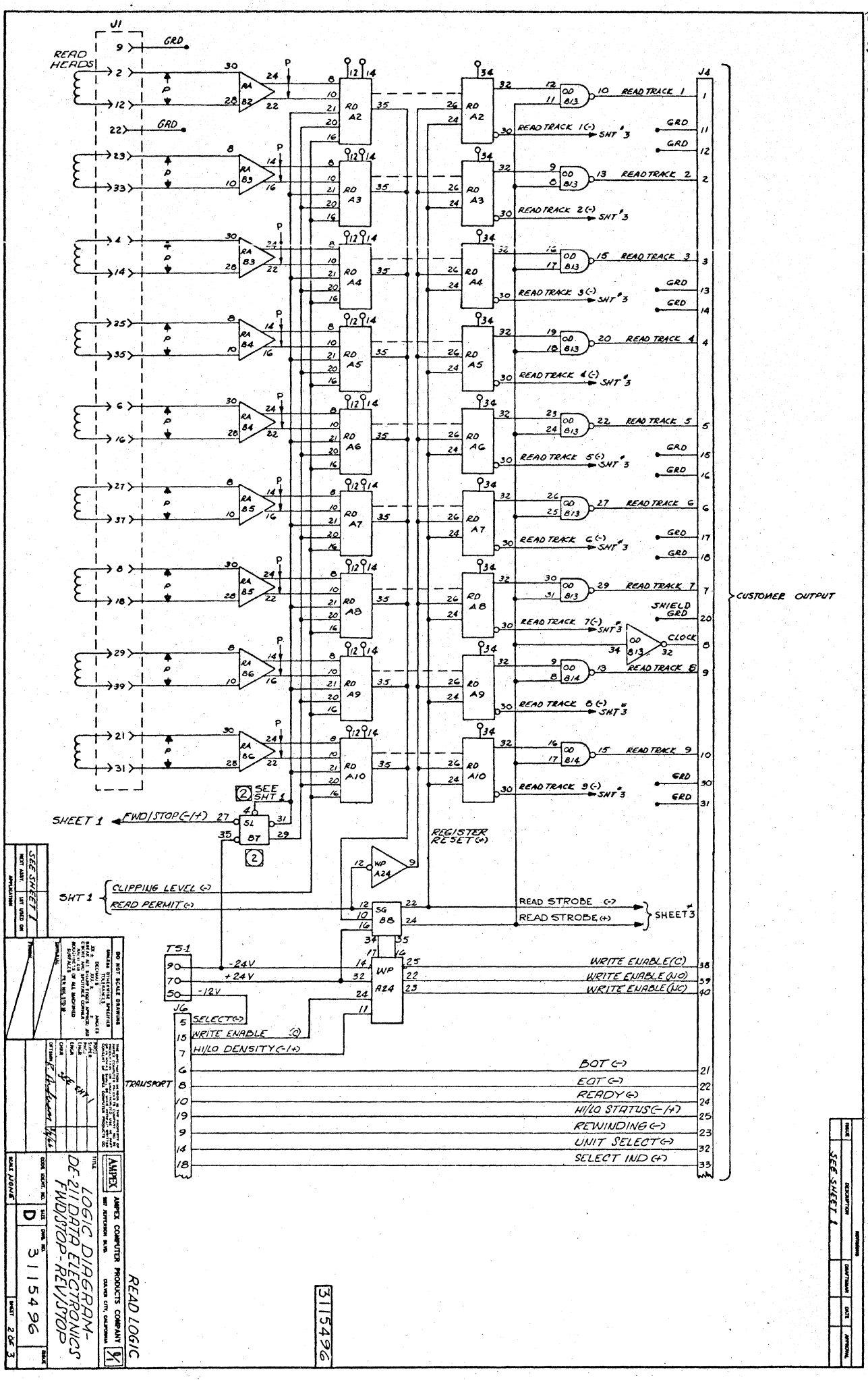
CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3112457	F

SCALE NONE — SHEET 3 OF 3

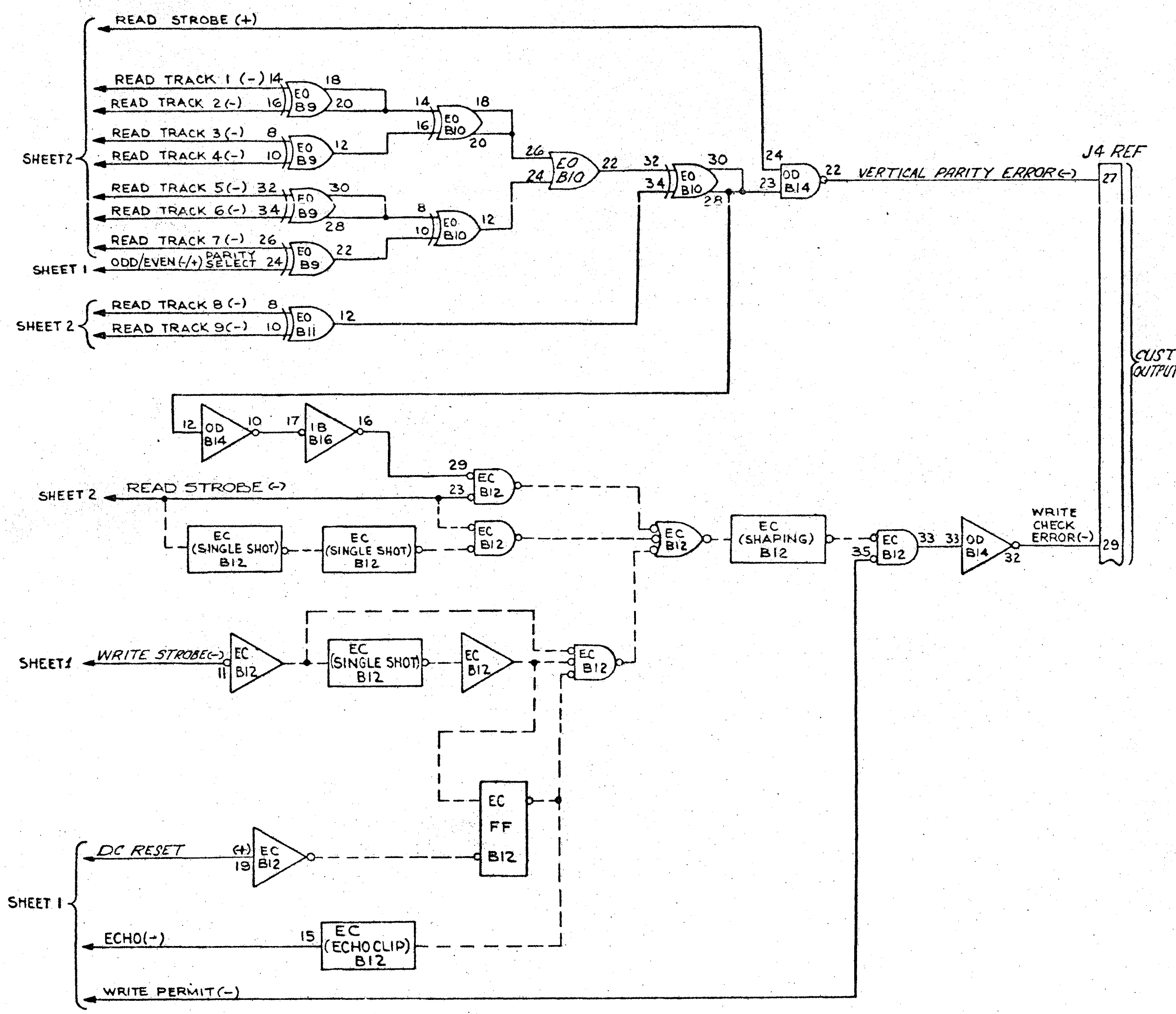
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
F	SEE SHEET 1			

3112457


NOTES:
1. ERASE HEAD OPTION.
2. ON READ FWD ONLY SYSTEMS BT 15 OMITTED & JUMPERS A10-21 TO A10-4 AND BT-13 TO BT-16 ARE ADDED.
3. JT-10 USED WITH CENTER-TAPPED HEAD ONLY.
CUSTOMER INPUT
J5
J7
TP-1
TP-2
WRITE TRACK 1(-)
WRITE TRACK 2(-)
WRITE TRACK 3(-)
WRITE TRACK 4(-)
WRITE TRACK 5(-)
WRITE TRACK 6(-)
WRITE TRACK 7(-)
WRITE TRACK 8(-)
WRITE TRACK 9(-)
WRITE STROBE(-)
WRITE PERMIT(-)
WRITE RESET(-)
READ PERMIT(-)
ODD/EVEN PARITY(+)
REV/STOP(-/+)
FWD/STOP(-/+)
REWIND(-)
REWIND & LOCKOUT(-)
GRD
SHIELD GRD
WRITE HEADS
ERASE HEAD
WRITE POWER
ERASE POWER
ECHO(-)
DC RESET(+)
CLIPPING LEVEL(-)
WRITE PERMIT(-)
READ PERMIT(-)
FWD/STOP(-/+)
ODD/EVEN PARITY(-/+)
WRITE STROBE(-)
J6 REF
SPARE
WRITE LOGIC
LOGIC DIAGRAM-DE-21 DATA ELECTRONICS FWD/STOP-REV/STOP
AMPEX COMPUTER PRODUCTS COMPANY
SCALE NONE
D
3115496
SHEET 1 OF 3
3115496 (1 of 3)


J1
READ HEADS
GRD
RA B2
RA B3
RA B4
RA B5
RA B6
RA B7
RA B8
RA B9
RA B10
RD A2
RD A3
RD A4
RD A5
RD A6
RD A7
RD A8
RD A9
RD A10
SEE SHT 1
SHEET 1
FWD/STOP(-/+)
SL B7
REGISTER RESET(+)
WP A24
SHT 1
CLIPPING LEVEL (-)
READ PERMIT(-)
SG B8
READ STROBE (-)
READ STROBE (+)
SHEET 3
TS-1
-24V
+24V
-12V
J6
SELECT(-)
WRITE ENABLE (-)
HI/LO DENSITY(-/+)
TRANSPORT
WRITE ENABLE(C)
WRITE ENABLE(N/C)
WRITE ENABLE(N/C)
BOT (-)
EOT (-)
READY (-)
HI/LO STATUS(-/+)
REWINDING (-)
UNIT SELECT (-)
SELECT IND (+)
J4
OD B13
OD B14
READ TRACK 1
READ TRACK 1(-)
READ TRACK 2
READ TRACK 2(-)
READ TRACK 3
READ TRACK 3(-)
READ TRACK 4
READ TRACK 4(-)
READ TRACK 5
READ TRACK 5(-)
READ TRACK 6
READ TRACK 6(-)
READ TRACK 7
READ TRACK 7(-)
SHIELD GRD
CLOCK
READ TRACK 8
READ TRACK 8(-)
READ TRACK 9
READ TRACK 9(-)
CUSTOMER OUTPUT
SEE SHEET 1
DO NOT SCALE DRAWING
AMPEX COMPUTER PRODUCTS COMPANY
DE-211 DATA ELECTRONICS FWD/STOP-REV/STOP
LOGIC DIAGRAM-
READ LOGIC
3115496
SIZE D
SHEET 2 OF 3
3115496 (2 of 3)

315496 (3 of 3)



SEE SHEET 1	
NEXT ASSY	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
TOLERANCES
DECIMALS ANGLES
BREAK ALL SHARP EDGES APPROX .010
CHAMFER AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES
PER MIL-STD-10
MATERIAL
FINISH

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM-
DE-211 DATA ELECTRONICS
FWD/STOP-REV/STOP

SIZE	CODE IDENT. NO.	DWG. NO.
D		315496

SCALE NONE — SHEET 3 OF 3

ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
	SEE SHEET 1			

315496