MULTI-USER....

MULTI-PROCESSING....

SUPER SLAVE

TECHNICAL

MANUAL

ADVANCED DIGITAL CORPORATION

12700-B KNOTT AVENUE
GARDEN GROVE, CALIFORNIA 92641
TEL: 714-891-4004 TELEX: 678401 TABIRIN

ADVANCED DIGITAL CORPORATION

September 9, 1983

ATTENTION: ALL CUSTOMERS

SUBJECT: WARRANTY SERVICE RETURNS

Advanced Digital requires an RMA number (return merchandise authorization) on all returned products for warranty service repair.

Any products returned for repair without an RMA number will be returned to the customer.

So please contact our Service Department before sending your product in for repair.

Thank You,

Best Regards,

Al Bagheri
General Manager

AB/ct

INTRODUCTION

ADVANCED DIGITAL is proud to introduce the SUPER SLAVE. The SUPER SLAVE is a Z80 based single board computer designed to be a bus slave in an S100 bus system. The SUPER SLAVE SBC has all the hardware needed to run a single user in an TURBO DOS or MP/M-CP/NOS system with up to 4 serial ports and an external Centronics parallel interface printer all on one board.

The SUPER SLAVE SBC contains :

1) Z-80A cpu (4 MHZ)
2) 64k OR 128k of dynamic memory (bank selectible)
3) 2k or 4k of shadow eprom (2716 or 2732)
4) 4 serial ports (Z80A SIO opt.syncronous)
5) 2 12 bit parallel ports (Z80A PIO)
6) Real time interrupt clock (Hardware divider)

ONE YEAR WARRANTY.

* Note: Items 4 and 5 require external adaptation for RS-232 and Centronics. The adapter boards are 2 x 2" and are called PS NET. They hook up to the back of the main frame with a DB-25 connector.

T A B L E O F C O N T E N T S

1. O V E R V I E W

1.1. The 64k or 128k Dynamic ram

The 64k or 128k ram array can be switched on and off under software control. This allows the CPU to bank switch memory with a specifiable amount of shared memory. The memory has an access time of 200ns. Refresh is done during Z80 M1 cycles and during wait states.

1.2. System Monitor Eprom

The system monitor eprom is switched on during reset. It can be disabled and enabled under software control. It resides when enabled at 0000h to 0FFFh. On power up the prom monitor checks the setting of the sense switch and either tries to load the operating system or goes to the diagnostic monitor which has commands that allow the user to load , examine, goto and test memory. When the prom is disabled it does not use any system address space.

1.3. Serial ports

A Z80A DART is used for the four serial ports , but a Z80A SIO/0 chip can be used in it's place. This allows asyncronous and synchronous serial data communications plus a variety of interrupt modes. Modem control signals are available at each serial connector. There are two software selectible baud rate generators for baud rates of 50 to 19.2k baud.

* Note: The serial ports are TTL and must be connected to external interface boards for RS232 communications. (PS NET/I)

1.4. Parallel ports

A Z80A PIO is used as the parallel port. In the output mode the parallel ports can drive one TTL load .

* Note: The parallel ports need an PS NET interface board for connection to a Centronics compatible parallel printer.

1.5. Real Time Interrupt clock

A hardware divider is used for providing a real time system clock to the board. There are three rates which are generated and can be used for interrupts (244Hz, 122Hz, 61Hz.)

1.6. S100 Bus Interface

The S100 bus interface provides the signals necessary for an 8 bit I/O mapped communications port on the S100 buss and conforms to the IEEE 696 bus specification. Vectored interrupt lines VI0 - VI7 are supported via jumper options.

2. E P R O M

2.1. EPROM and Monitor operation

The onboard EPROM occupies address 0000H-0FFFH. The EPROM is switched on automatically during reset or power on, the EPROM contains SIO initialization code along with a simple debugger and cold start loader. After the operating system is loaded the EPROM can be turned off so that the ram at address 0000H-0FFFH can be accessed. The EPROM can be turned on and off at any time under software control.

2.2. Eprom Enable / Disable

The eprom is switched on by writing the low order bit of port 1FH. An 0 disables the eprom and an 1 enables the eprom. Jumper JPR3 configures the board to accept a 2716 or 2732 EPROM.

* Note: The EPROM is always addressed at 0000H and can not be moved. Since the 2716 EPROM is 2K long it appears twice, 0000H-07FFH and 0800H-0FFFH.

2.3. Monitor Signon

The EPROM contains a simple debugger.
The monitor signs on with :

```
) ADVANCED DIGITAL CORP.
  SUPER SLAVE Running
  Monitor Version 1.2
  Jun - 1982
  Press "H" for help
)
```

2.4. Monitor Commands

The monitor commands are :

DSSSS,QQQQ = Dump memory in hex from SSSS to QQQQ

FSSSS,QQQQ,BB = Fill memory from SSSS to QQQQ with BB

GAAAA = Go to address AAAA

IPP = Input from port P

LAAAA = Load memory starting at AAAA

MSSSS,QQQQ,DDDD = Move starting at S to Q to Addr. D

OPP,DD = Output data D to port P

PSSSS,QQQQ = Print in ascii from SSSS to QQQQ

T = Test Memory

ESC will terminate any command

2.5. Cold Boot Program

```
;
;
;          SLAVE BOOT ROUTINE
;
SLVBOOT::
      LD    BC,SLVBLKL*256+LCSP@          ;SET UP BLOCK TRANS
      LD    HL,SLVBLK
      OUTI                                ;SEND SERVICE REQUEST
      DEC   C                             ;CHANGE PORT
      OTIR                                ;SEND BLOCK MESSAGE
      LD    B,80H                         ;SET UP RECIEVE BLOCK
      LD    HL,1000H
      INIR                                ;GET BLOCK
      JP    1000H                         ;GO TO SLAVE LOADER
;
SLVBLK::
      DB    9                             ;REQUEST SERVICE
      DB    1,4CH,0,0FFH,0FFH
      DB    0FFH,0FFH,0FFH,0FFH,0FFH
;
SLVBLKL EQU     $-SLVBLK                  ;SLAVE BLOCK LENGTH
```

3. I N P U T / O U T P U T P O R T A S S I G M E N T S

Address		Function
00	Read/Write	SIO 1 Channel A Data port
01	Read/Write	SIO 1 Channel A Status/Control Port
02	Read/Write	SIO 1 Channel B Data port
03	Read/Write	SIO 1 Channel B Status/Control Port
04		Unused
05		Unused
06		Unused
07		Unused
08		Unused
09		Unused
0A		Unused
0B		Unused
0C	Read/Write	SIO 2 Channel A Data port
0D	Read/Write	SIO 2 Channel A Status/Control Port
0E	Read/Write	SIO 2 Channel B Data port
0F	Read/Write	SIO 2 Channel B Status/Control Port
10	Write	Baud Rate
11		"
12		"
13		"
14	Read/Write	PIO Channel A Data port
15	Read/Write	PIO Channel B Data port
16	Write	PIO Channel A Control port
17	Write	PIO Channel B Control Port
18	Read/Write	Interrupt controller data port
19	Read/Write	Interrupt command/status port
1A	Read/Write	Interrupt controller data port
1B	Read/Write	Interrupt command/status port
1C		Unused
1D	Write	Memory control port
1E	Read/Write	Master communications port
1F	Read/Write	Master status/command port

All addresses are listed in Hexidecimal.

4. INPUT / OUTPUT PORT DESCRIPTIONS

4.1. Serial Communications Port A --- See Appendex A

00	Read/Write	SIO 1 Channel A Data port
01	Read/Write	SIO 1 Channel A Status/Control Port

4.2. Serial Communications Port B --- See Appendex A

02	Read/Write	SIO 1 Channel B Data port
03	Read/Write	SIO 1 Channel B Status/Control Port

4.3. Serial Communications Port C --- See Appendex A

0C	Read/Write	SIO 2 Channel A Data port
0D	Read/Write	SIO 2 Channel A Status/Control Port

4.4. Serial Communications Port D --- See Appendex A

0E	Read/Write	SIO 2 Channel B Data port
0F	Read/Write	SIO 2 Channel B Status/Control Port

4.5. Baud Rate Select Port

10	Write	Baud Rate Select port

This port programs the two software selectable baud rates for the serial channels. The lower four bits program baud rate A, the upper four bits program baud rate B according to the table below.

Command	Baud Rate	Command	Baud Rate
0	50	8	1800
1	75	9	2000
2	110	A	2400
3	134	B	3600
4	150	C	4800
5	300	D	7200
6	600	E	9600
7	1200	F	19200

(e.g. Output 8EH to Baud Rate Port would select 1200 Baud for Baud Rate B and 9600 Baud for Baud Rate A.)

4.6. Paralled Interface Port A --- See Appendix B

14	Read/Write	PIO Channel A Data port
16	Write	PIO Channel A Control Port

4.7. Parallel Interface Port B --- See Appendix B

15	Read/Write	PIO Channel B Data port
17	Write	PIO Channel B Control Port

4.8. On-Board Memory Control Port

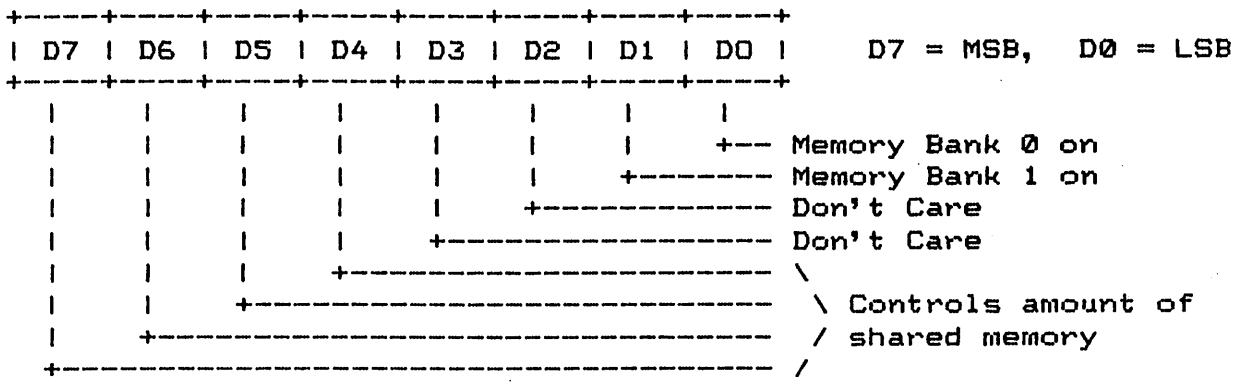
1D	Write	On-Board Memory Control Port

This port controls the onboard memory managment circuit.

Port write :

The two low order bits D0,D1 control which bank is on, D0 for bank 0 and D1 for bank 1.

The four high order bits control how much of bank 0 is shared in both banks in 1k increments from 1k to 16k.



Unswitched memory boundry:

bits 4-7	boundry	bits 4-7	boundry
0	48k	8	56k
1	49k	9	57k
2	50k	A	58K
3	51K	B	59K
4	52K	C	60K
5	53K	D	61K
6	54K	E	62K
7	55K	F	63K

4.9. Master communications port

1E Read/Write Master communications port

This port is a bi-directional interface port to the Master processor. When the slave is in the wait mode a read or write to this port will hold the processor until the master accesses the port from the S100 buss, this waiting along with the syncerr signal gaurantees error free block transfers between the master and the slave. When the slave is not in the wait mode this port can be read from or written to in the normal manner and provides 8 bits of communications with the Master processor.

4.10. Master Status/Command port

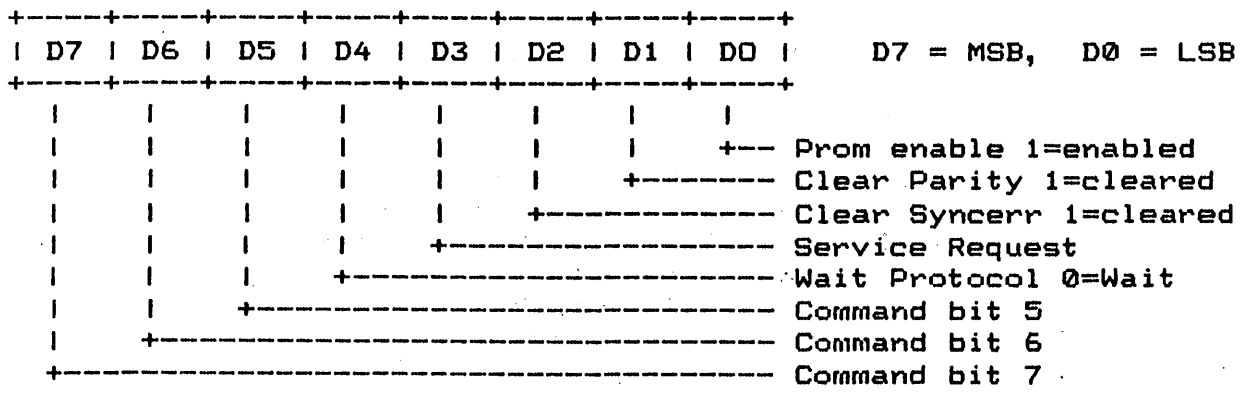
1F Read/Write Master status/command port

This is a bit sensitive port for sending requests to the Master and reading on board status.

For a write:

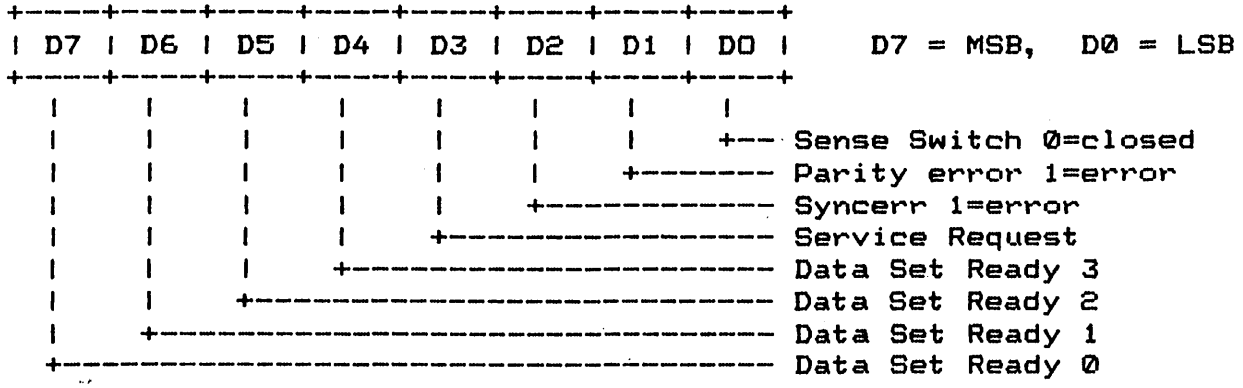
The high order three bits are arbitrary command bits to the master. The next bit sets whether wait state protocol is used or not. Bit 3 is the service request bit to the master processor, Bit 2 clears syncerr status, Bit 1 clears parity errors. Bit 0 enables or disables the on board prom.

Bits 3-7 can be cleared by the master processor.



For a read:

The high order four bits are the Data set ready lines from the four serial channels. Bit 3 is the service request bit, this allows testing to see if the master has responded to the service request. Bit 2 is Syncerr, this indicates if the master accessed the data port when the slave was not in a wait state on the data port. Bit 1 is Parity error. Bit 0 is the sense switch.



5. J U M P E R A R E A D E F I N I T I O N S

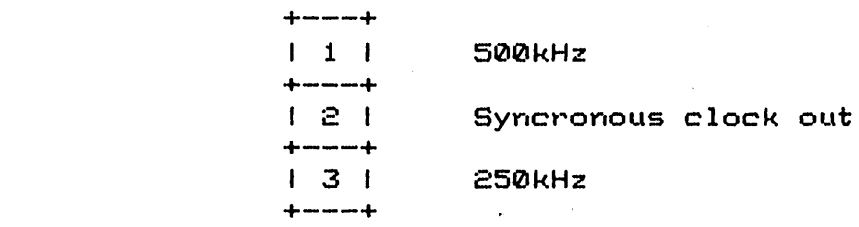
Jumper	Function
A	Syncronous bit rate 250/500kHz
B	Asyncronous/Syncronous clock select
C	External/Internal Tx/Rx clock for SIO channel C
D	External/Internal Tx/Rx clock for SIO channel D
E	External/Internal Tx/Rx clock for SIO channel A
F	External/Internal Tx/Rx clock for SIO channel B
JPR1	External Reset Enable
I	External Reset Select
JPR2	Sense Switch
JPR3	Prom Select
	Interrupt Select

6. J U M P E R D E S C R I P T I O N S

6.1. A Syncronous bit rate 250/500kHz

This jumper determines the syncronous bit rate.

The jumper is located above U1.

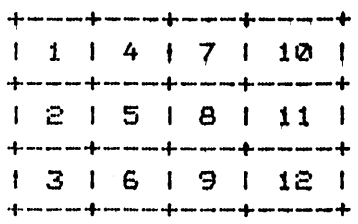


Install Plug between posts 1 & 2 for 500kHz operation.

Install Plug between posts 2 & 3 for 250kHz operation.

6.2. B Asyncronous/Syncronous clock select

This jumper area determines whether the serial ports will get the Syncronous clock or the Asyncronous clock.



Jumpers 1,4,7,10 are the syncronous clock.

Jumpers 3 and 9 are Baud Rate A.

Jumpers 6 and 12 are Baud Rate B.

Jumper 2 is clock for Serial channel A.

Jumper 5 is clock for Serial channel B.

Jumper 8 is clock for Serial channel C.

Jumper 11 is clock for Serial channel D.

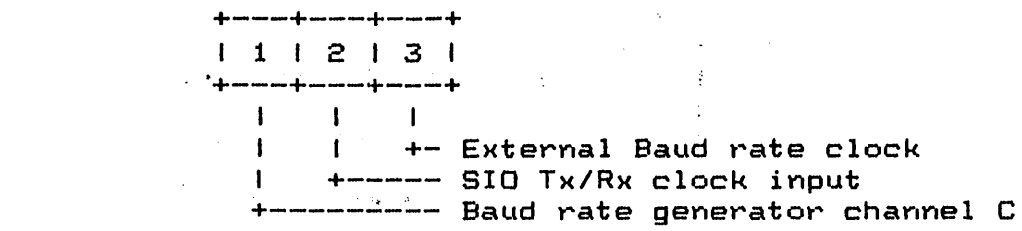
Jumpers from the top row to the middle row will select the syncronous clock for that channel.

Jumpers from the bottom row to the middle row will select the asyncronous clock for that channel.

6.3. C Ext/Int Tx/Rx clock for SIO channel C

Jumper C connects the SIO channel C to either the internal baud rate generator or to the externally generated baud rate for use in sycronous applications.

Jumper C is located above Jumper B.



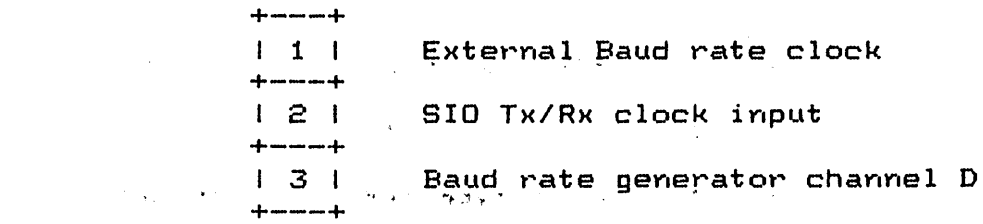
Install Plug between posts 1 & 2 for Baud rate generator.

Install Plug between posts 2 & 3 for external SIO clock.

6.4. D Ext/Int Tx/Rx clock for SIO channel D

Jumper D connects the SIO channel D to either the internal baud rate generator or to the externally generated baud rate for use in sycronous applications.

Jumper D is located next to Jumper B.



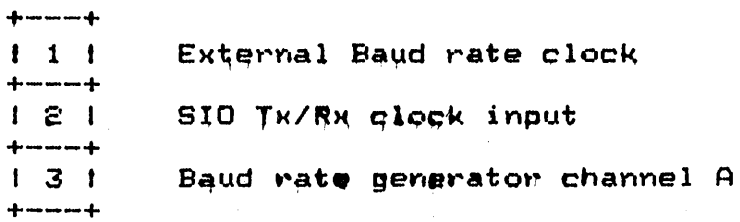
Install Plug between posts 1 & 2 for external SIO clock.

Install Plug between posts 2 & 3 for Baud rate generator.

6.5. E Ext/Int Tx/Rx clock for SIO channel A

Jumper E connects the SIO channel A to either the internal baud rate generator or to the externally generated baud rate for use in sycronous applications.

Jumper E is located next to Jumper D.



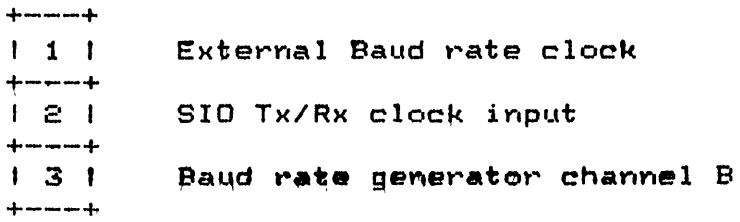
Install Plug between posts 1 & 2 for external SIO clock.

Install Plug between posts 2 & 3 for Baud rate generator.

6.6. F Ext/Int Tx/Rx clock for SIO channel B

Jumper F connects the SIO channel B to either the internal baud rate generator or to the externally generated baud rate for use in sycronous applications.

Jumper F is located next to Jumper E.



Install Plug between posts 1 & 2 for external SIO clock.

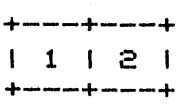
Install Plug between posts 2 & 3 for Baud rate generator.

6.7. JPR1 External Reset Enable

This jumper enables external reset from a terminal which can

control an RS232 line. The PS NET/I board must be jumpered to drive pin 11 of serial A or B connector to control board reset.

This jumper is located above U21.

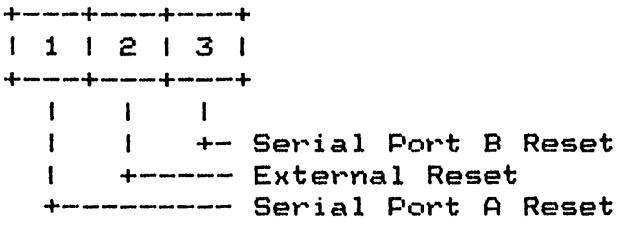


Jumper 1 to 2 to enable external reset.

6.8. I External Reset Select

This jumper selects whether serial port A or serial port B connector has the external reset line connected to it.

This jumper is located between J2 and J3.



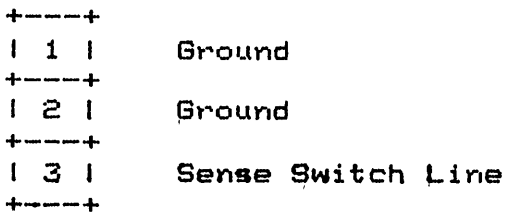
Jumper 1 to 2 to select Reset from Serial Port A.

Jumper 2 to 3 to select Reset from Serial Port B.

6.9. JPR2 Sense Switch

This jumper sets the sense switch either open or closed.

This jumper is located on the right side of U43.



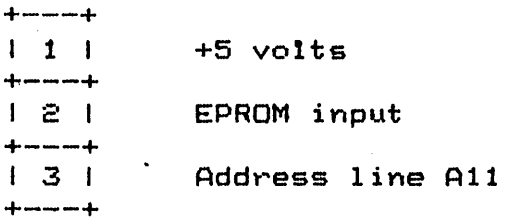
Jumper 1 to 2 to set Sense Switch open.

Jumper 2 to 3 to set Sense Switch closed.

6.10. JPR3 Select 2716 or 2732 EPROM.

Jumper JPR3 configures the board to accept a 2716 or 2732 EPROM.

Jumper JPR3 is located above the Z80 chip.



Install Plug between posts 1 & 2 for a 2716 EPROM.

Install Plug between posts 2 & 3 for a 2732 EPROM.

* Note: The EPROM is always addressed at 0000H and can not be moved. Since the 2716 EPROM is 2K long it appears twice, 0000H-07FFH and 0800H-0FFFH.

6.11. Interrupt Select

This Jumper area selects on board interrupt sources and off board interrupt generators. This area is set up to allow great flexibilty in the selection of interrupt sources for the Super Slave board and to allow the Super Slave to generate interrupts to the S100 bus.

This area is divided into 9 vertical columns each of which

corresponds to an interrupt input to the Super Slave board except for the 9th column which can generate an interrupt to the S100 INT line. The horizontal rows are logical groupings of interrupt sources or destinations.

Row A provides sources which indicate whether the master has read from or written to the Super Slave board.

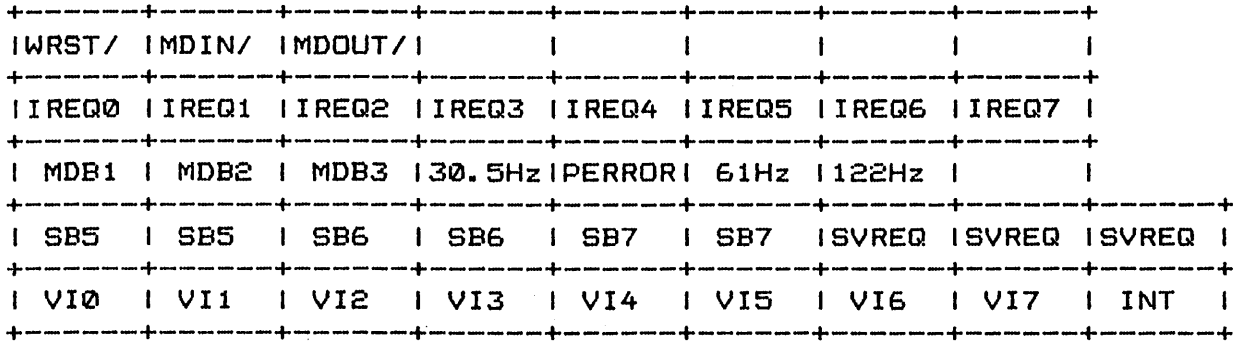
Row B contains the input lines to the 9519 interrupt controller.

Row C provides three master generatable interrupts, the real time clocks, and the parity error signal.

Row D contains signals which can be used as sources for interrupts to the S100 bus.

Row E is the S100 Interrupt lines.

This jumper area is located above switch SW1 and below U13.



The interrupt sources and destinations in this area are arranged so that the most common connections can be made with push on jumpers, but wire wrap wire may be used if necessary.

7. A D D R E S S S W I T C H E S

The address switches control what address on the S100 buss the Super Slave boards I/O ports are to be found. These switches are located in the lower left hand corner of the board below the interrupt jumper area. The address lines A1-A7 correspond to switches S1-S7 (switch S1 is at the right hand end of the switch.) Each switch is set to a low value if it is closed and to a high value if it is open.

Super Slave Address Switch Settings

The table below shows how the 8 dip switch is the set for all the Super Slave boards to be installed in the system. 70-7E hex and 80-8E hex are the most commonly used for slave I/O addressing. The 8 position switch is located on the lower left hand side of the board located next to the +5 volt regulator.

U = up and "1", D = down and "0", I = ignored

8	7	6	5	4	3	2	1	slave address	num.	
I	D	U	U	U	D	D	D	70H	0	#275
I	D	U	U	U	D	D	U	72H	1	#826
I	D	U	U	U	D	U	D	74H	2	#276
I	D	U	U	U	D	U	U	76H	3	#827
I	D	U	U	U	U	D	D	78H	4	#828
I	D	U	U	U	U	D	U	7AH	5	#278
I	D	U	U	U	U	U	D	7CH	6	
I	D	U	U	U	U	U	U	7EH	7	
I	U	D	D	D	D	D	D	80H	8	
I	U	D	D	D	D	D	U	82H	9	
I	U	D	D	D	D	U	D	84H	10	
I	U	D	D	D	D	U	U	86H	11	
I	U	D	D	D	U	D	D	88H	12	
I	U	D	D	D	U	D	U	8AH	13	
I	U	D	D	D	U	U	D	8CH	14	
I	U	D	D	D	U	U	U	8EH	15	

8. EXTERNAL CONNECTOR PIN DEFINITIONS

8.1. Connector P1 = S100 bus connector

PIN#	NAME	PIN #	NAME
1	+8V	51	+8V
2	+16V	52	-16V
3	XRDY	53	GND
4	VI0*	54	SLAVE CLR*
5	VI1*	55-57	DMA0*-DMA2*
6	VI2*	58	SXTRQ*
7	VI3*	59	A19
8	VI4*	60	SIXTN*
9	VI5*	61-64	A20-A23
10	VI6*	65,65	NDEF
11	VI7*	67	PHANTOM*
12	NMI*	68	MWRT
13	PWRFAIL*	69	RFU
14	DMA3*	70	GND
15	A18	71	RFU
16	A17	72	RDY
17	A16	73	INT*
18	SDSB*	74	HOLD*
19	CDSB*	75	RESET*
20	GND	76	PSYNCH
21	NDEF	77	PWR*
22	ADSB*	78	PDBIN
23	DODSB*	79-87	A0-A11
24	0	88-95	DO2-DI0
25	PSTVAL*	96	SINTA
26	PHLDA	97	SWO*
27,28	RFU	98	ERROR*
29-34	A5,A4,A3,A15,A12,A9		
35	DO1/DATA 1	99	POC*
36	DO0/DATA 0	100	GND
37	A10		
38	DO4		
39	DO5		
40-43	DO6,DI2,DI3,DI7		
44	SMI		
45	SOUT		
46	SINP		
47	SMEMR		
48	SHLTA		
49	CLOCK		
50	GND		

8.2. Connector J1 = Serial port Channel A

1	DSR	Data Set Ready
2	DCDA*	Data Carrer Detect Channel A *
3	SYNCA*	Sync Detect
4	RxDA	Receive data
5	CTSA*	Clear to send
6	TxDA	Transmit data
7	RTSA*	Request to send
8	DTRA*	Data terminal ready
9	Tx/RxCA*	Transmitt / receive clock
10	GND	
11	EXRST	External reset
12	+16 VOLTS	
13	-16 VOLTS	
14	+5 VOLTS	

8.3. Connector J2 = Serial port Channel B

1	DSR	Data Set Ready
2	DCDA*	Data Carrer Detect Channel A *
3	SYNCA*	Sync Detect
4	RxDA	Receive data
5	CTSA*	Clear to send
6	TxDA	Transmit data
7	RTSA*	Request to send
8	DTRA*	Data terminal ready
9	Tx/RxCA*	Transmitt / receive clock
10	GND	
11	EXRST	External reset
12	+16 VOLTS	
13	-16 VOLTS	
14	+5 VOLTS	

8.4. Connector J3 = Serial port Channel C

1	DSR	Data Set Ready
2	DCDA*	Data Carrer Detect Channel A *
3	SYNCA*	Sync Detect
4	RxDA	Receive data
5	CTSA*	Clear to send
6	TxDA	Transmit data
7	RTSA*	Request to send
8	DTRA*	Data terminal ready
9	Tx/RxCA*	Transmitt / receive clock
10	GND	
11	N/C	
12	+16 VOLTS	
13	-16 VOLTS	
14	+5 VOLTS	

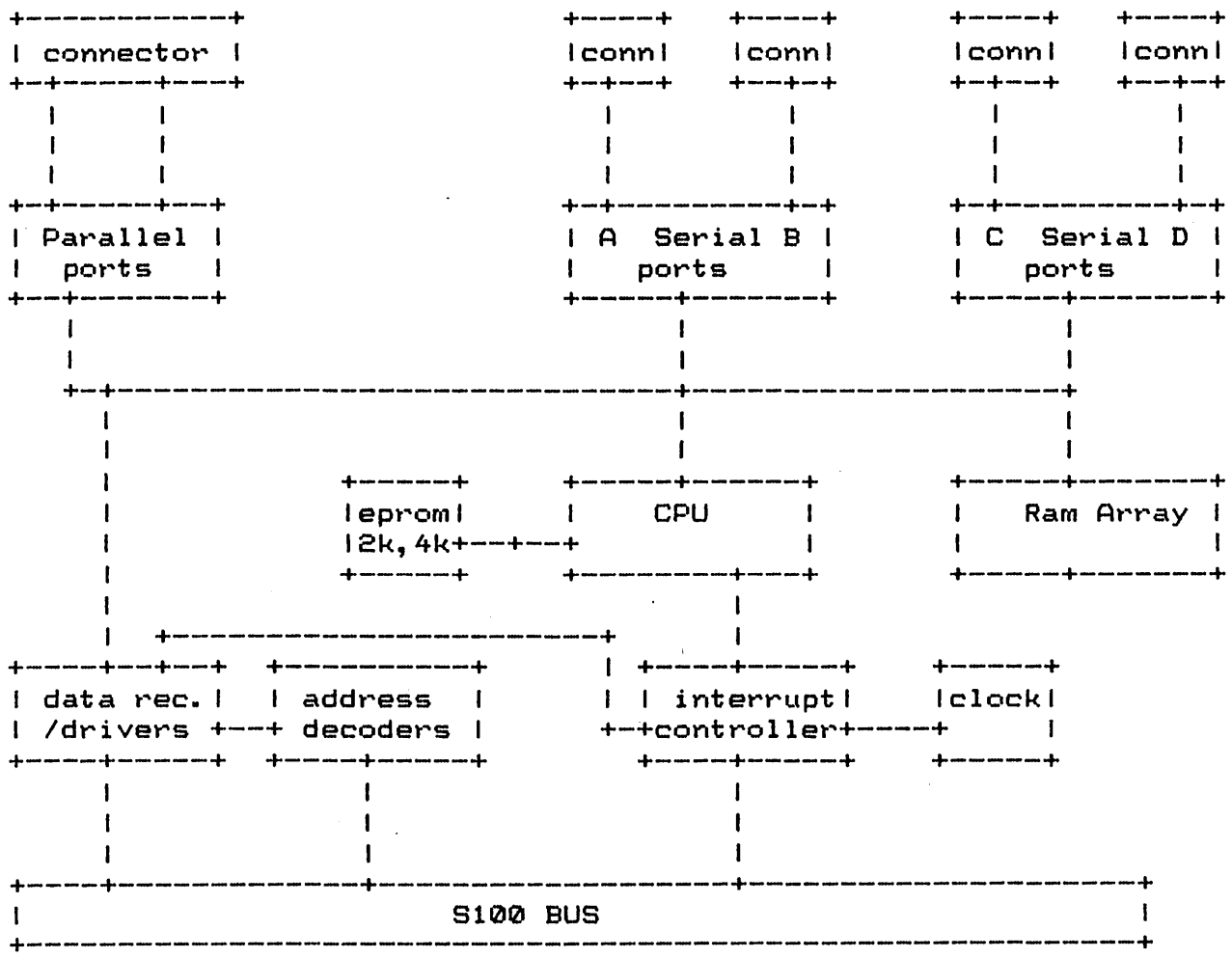
8.5. Connector J4 = Serial port Channel B

1	DSR	Data Set Ready
2	DCDA*	Data Carrer Detect Channel A *
3	SYNCA*	Sync Detect
4	RxDA	Receive data
5	CTSA*	Clear to send
6	TxDA	Transmit data
7	RTSA*	Request to send
8	DTRA*	Data terminal ready
9	Tx/RxCA*	Transmitt / receive clock
10	GND	
11	N/C	
12	+16 VOLTS	
13	-16 VOLTS	
14	+5 VOLTS	

8.6. Connector J5 = Parallel port connector

1	ARDY	PIO Channel A ready signal
2	ARDY RET	ground
3	ASTRB*	PIO Channel A strobe
4	ASTRB RET	ground
5	PA0	PIO Channel A data bit D0
6	PA0 RET	ground
7	PA1	PIO Channel A data bit D1
8	PA1 RET	ground
9	PA2	PIO Channel A data bit D2
10	PA2 RET	ground
11	PA3	PIO Channel A data bit D3
12	PA3 RET	ground
13	PA4	PIO Channel A data bit D4
14	PA4 RET	ground
15	PA5	PIO Channel A data bit D5
16	PA5 RET	ground
17	PA6	PIO Channel A data bit D6
18	PA6 RET	ground
19	PA7	PIO Channel A data bit D7
20	PA7 RET	ground
21	BRDY	PIO Channel B ready signal
22	BRDY RET	ground
23	BSTRB*	PIO Channel B strobe
24	BSTRB RET	ground
25	PB0	PIO Channel B data bit D0
26	PB0 RET	ground
27	PB1	PIO Channel B data bit D1
28	PB1 RET	ground
29	PB2	PIO Channel B data bit D2
30	PB2 RET	ground
31	PB3	PIO Channel B data bit D3
32	PB3 RET	ground
33	PB4	PIO Channel B data bit D4
34	PB4 RET	ground
35	PB5	PIO Channel B data bit D5
36	PB5 RET	ground
37	PB6	PIO Channel B data bit D6
38	PB6 RET	ground
39	PB7	PIO Channel B data bit D7
40	+ 5 VOLTS	

9. B O A R D D I A G R A M



10. F A C T O R Y I N S T A L L E D J U M P E R S

10.1. Factory Installed jumpers

Jumper		
B	2-3	Tx/Rx clock for SIO A asyncronous
B	5-6	Tx/Rx clock for SIO B asyncronous
E	2-3	Tx/Rx clock for SIO A internal
F	2-3	Tx/Rx clock for SIO B internal
JPR2	2-3	Auto boot slave operating system
JPR3	1-2	2716 Eprom

Interrupt area column 0 row B-C MDB1/ to IREQ0

A. Z 8 0 A S I O / D A R T . . . . . .

Z8440
Z80® SIO Serial Input/Output Controller

Zilog

Product Specification

June 1982

Features

- Two independent full-duplex channels, with separate control and status lines for modems or other devices.
- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5 MHz clock (Z-80 SIO), or 0 to 800K bits/second with a 4.0 MHz clock (Z-80A SIO).
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection and flag insertion.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

General Description

The Z-80 SIO Serial Input/Output Controller is a dual-channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA

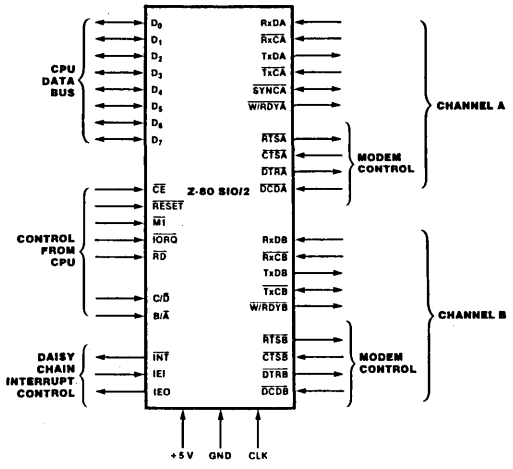


Figure 1. Z-80 SIO/2 Pin Functions

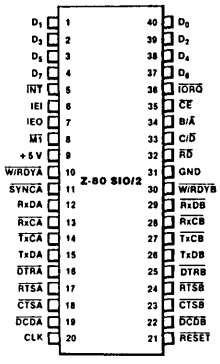


Figure 2. Z-80 SIO/2 Pin Assignments

General Description (Continued)

control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast (or slow) peripheral devices. While designed primarily as a member of the Z-80 family, its versatility makes it well suited to many other CPUs.

The Z-80 SIO is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic or ceramic DIP. It uses a single +5 V power supply and the standard Z-80 family single-phase clock.

Pin Description

Figures 1 through 6 illustrate the three pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- Z-80 SIO/2 lacks $\overline{SYNCB}$
- Z-80 SIO/1 lacks $\overline{DTRB}$
- Z-80 SIO/0 has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The first bonding option above (SIO/2) is the preferred version for most applications. The pin descriptions are as follows:

B/$\overline{A}$. *Channel A Or B Select* (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.

C/$\overline{D}$. *Control Or Data Select* (input, High selects Control). This input defines the type of information transfer performed between the CPU and the SIO. A High at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A Low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low level at this input enables the SIO to accept command or data input from the CPU during a write cycle or to transmit data to the CPU during a read cycle.

CLK. *System Clock* (input). The SIO uses the standard Z-80 System Clock to synchronize internal signals. This is a single-phase clock.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear To Send* (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). The system data bus transfers data and commands between the CPU and the Z-80 SIO. D_0 is the least significant bit.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffer-

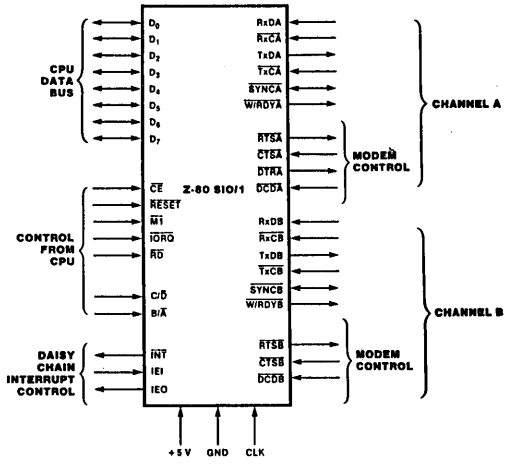


Figure 3. Z-80 SIO/1 Pin Functions

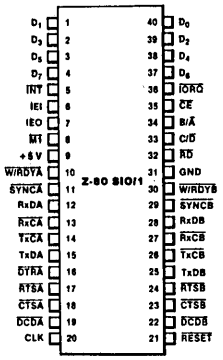


Figure 4. Z-80 SIO/1 Pin Assignments

Pin Description (Continued)

ing does not guarantee a specific noise-level margin.

$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$. *Data Terminal Ready* (outputs, active Low). These outputs follow the state programmed into Z-80 SIO. They can also be programmed as general-purpose outputs.

In the Z-80 SIO/1 bonding option, $\overline{\text{DTRB}}$ is omitted.

IEI. *Interrupt Enable In* (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{\text{INT}}$. *Interrupt Request* (output, open drain, active Low). When the SIO is requesting an interrupt, it pulls $\overline{\text{INT}}$ Low.

$\overline{\text{IORQ}}$. *Input/Output Request* (input from CPU, active Low). $\overline{\text{IORQ}}$ is used in conjunction with B/$\overline{\text{A}}$, C/$\overline{\text{D}}$, $\overline{\text{CE}}$ and $\overline{\text{RD}}$ to transfer commands and data between the CPU and the SIO. When $\overline{\text{CE}}$, $\overline{\text{RD}}$ and $\overline{\text{IORQ}}$ are all active, the channel selected by B/$\overline{\text{A}}$ transfers data to the CPU (a read operation). When $\overline{\text{CE}}$ and $\overline{\text{IORQ}}$ are active but $\overline{\text{RD}}$ is inactive, the channel selected by B/$\overline{\text{A}}$ is written to by the CPU with either data or control information as specified by C/$\overline{\text{D}}$. If $\overline{\text{IORQ}}$ and $\overline{\text{M1}}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{\text{M1}}$. *Machine Cycle* (input from Z-80 CPU, active Low). When $\overline{\text{M1}}$ is active and $\overline{\text{RD}}$ is also active, the Z-80 CPU is fetching an instruction from memory; when $\overline{\text{M1}}$ is active while $\overline{\text{IORQ}}$ is active, the SIO accepts $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z-80 CPU.

$\overline{\text{RxCA}}$, $\overline{\text{RxCB}}$. *Receiver Clocks* (inputs). Receive data is sampled on the rising edge of $\overline{\text{RxC}}$. The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).

In the Z-80 SIO/0 bonding option, $\overline{\text{RxCB}}$ is bonded together with $\overline{\text{TxCB}}$.

$\overline{\text{RD}}$. *Read Cycle Status* (input from CPU, active Low). If $\overline{\text{RD}}$ is active, a memory or I/O read operation is in progress. $\overline{\text{RD}}$ is used with B/$\overline{\text{A}}$, $\overline{\text{CE}}$ and $\overline{\text{IORQ}}$ to transfer data from the SIO to the CPU.

RxDA, RxDB. *Receive Data* (inputs, active High). Serial data at TTL levels.

$\overline{\text{RESET}}$. *Reset* (input, active Low). A Low $\overline{\text{RESET}}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High and disables all interrupts. The control registers must be

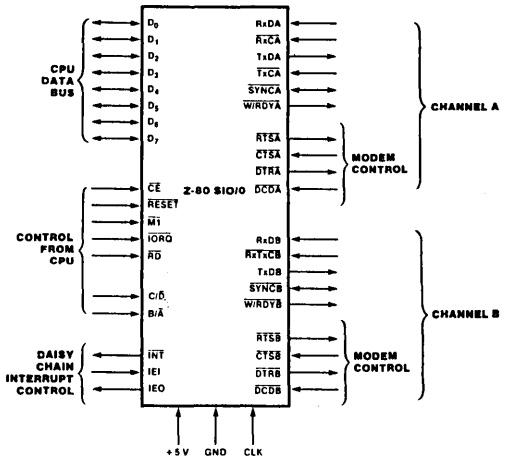


Figure 5. Z-80 SIO/0 Pin Functions

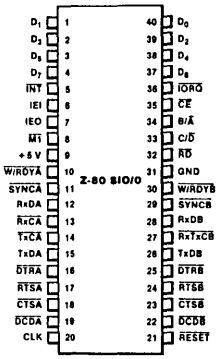


Figure 6. Z-80 SIO/0 Pin Assignments

Pin Description (Continued)

rewritten after the SIO is reset and before data is transmitted or received.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$. *Request To Send* (outputs, active Low). When the RTS bit in Write Register 5 (Figure 14) is set, the $\overline{\text{RTS}}$ output goes Low. When the RTS bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{\text{RTS}}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$. *Synchronization* (inputs/outputs, active Low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 (Figure 13), but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{\text{SYNC}}$ must be driven Low on the second rising edge of $\overline{\text{RxC}}$ after that rising edge of $\overline{\text{RxC}}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{\text{SYNC}}$ input. Once $\overline{\text{SYNC}}$ is forced Low, it should be kept Low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{\text{RxC}}$ that immediately precedes the falling edge of $\overline{\text{SYNC}}$ in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{\text{RxC}}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the Z-80 SIO/2 bonding option, $\overline{\text{SYNCB}}$ is omitted.

$\overline{\text{TxCA}}$, $\overline{\text{TxCB}}$. *Transmitter Clocks* (inputs). In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation.

In the Z-80 SIO/0 bonding option, $\overline{\text{TxCB}}$ is bonded together with $\overline{\text{RxCB}}$.

TxDA, TxDB. *Transmit Data* (outputs, active High). Serial data at TTL levels. TxD changes from the falling edge of $\overline{\text{TxC}}$.

$\overline{\text{W/RDYA}}$, $\overline{\text{W/RDYB}}$. *Wait/Ready A, Wait/Ready B* (outputs, open drain when programmed for Wait function, driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

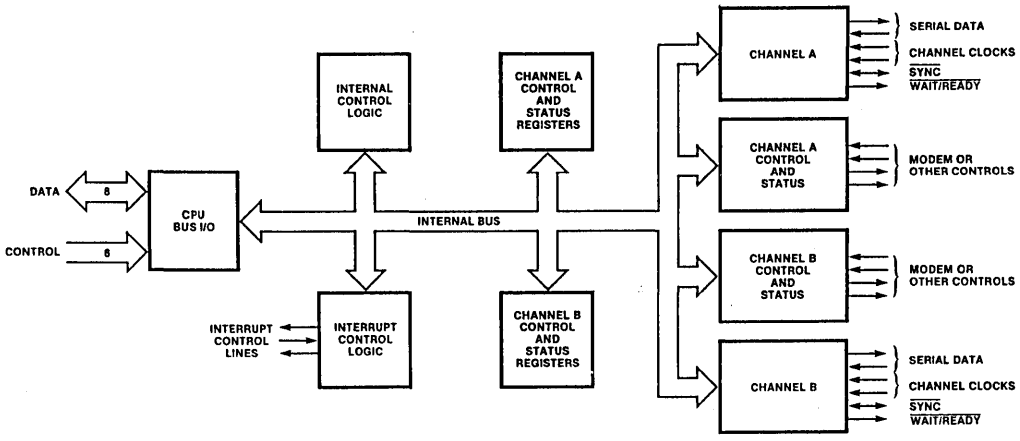


Figure 7. Block Diagram

Functional Description

The functional capabilities of the Z-80 SIO can be described from two different points of view: as a data communications device, it transmits and receives serial data in a wide variety of data-communication protocols; as a Z-80 family peripheral, it interacts with the Z-80 CPU and other peripheral circuits, sharing the data, address and control buses, as well as being a part of the Z-80 interrupt structure. As a peripheral to other microprocessors, the SIO offers valuable features such as non-vectored interrupts, polling and simple handshake capability.

Figure 8 illustrates the conventional devices that the SIO replaces.

The first part of the following discussion covers SIO data-communication capabilities; the second part describes interactions between the CPU and the SIO.

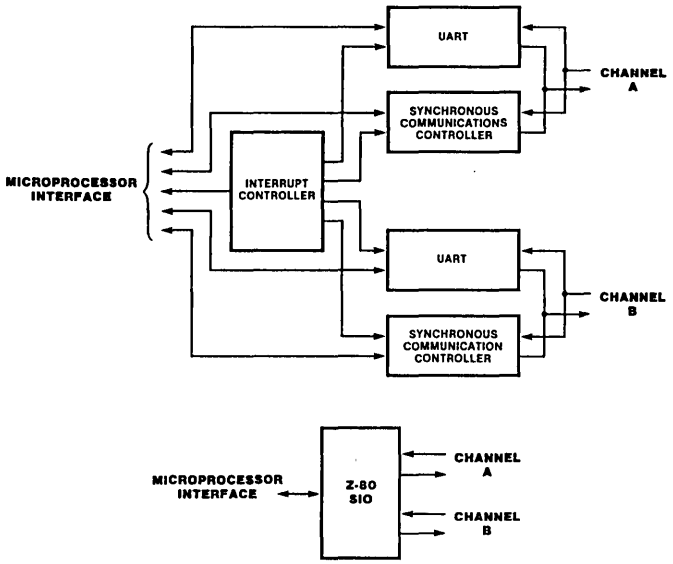


Figure 8. Conventional Devices Replaced by the Z-80 SIO

Data Communication Capabilities

The SIO provides two independent full-duplex channels that can be programmed for use in any common asynchronous or synchronous data-communication protocol. Figure 9 illustrates some of these protocols. The following is a short description of them. A more detailed explanation of these modes can be found in the *Z-80 SIO Technical Manual.*

Asynchronous Modes. Transmission and reception can be done independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 5). If the Low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occurred. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit is begun.

The SIO does not require symmetric transmit and receive clock signals—a feature that allows it to be used with a Z-80 CTC or many other clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32 or 1/64 of the clock rate supplied to the receive and transmit clock inputs.

In asynchronous modes, the $\overline{\text{SYNC}}$ pin may be programmed as an input that can be used for functions such as monitoring a ring indicator.

Synchronous Modes. The SIO supports both byte-oriented and bit-oriented synchronous communication.

Synchronous byte-oriented protocols can be handled in several modes that allow character synchronization with an 8-bit sync character (Monosync), any 16-bit sync pattern (Bisync), or with an external sync signal. Leading sync

Data Communication Capabilities (Continued)

characters can be removed without interrupting the CPU.

Five-, six- or seven-bit sync characters are detected with 8- or 16-bit patterns in the SIO by overlapping the larger pattern across multiple in-coming sync characters, as shown in Figure 10.

CRC checking for synchronous byte-oriented modes is delayed by one character time so the CPU may disable CRC checking on specific characters. This permits implementation of protocols such as IBM Bisync.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. In all non-SDLC modes, the CRC generator is initialized to 0's; in SDLC modes, it is initialized to 1's. The SIO can be used for interfacing to peripherals such as hard-sectored floppy disk, but it cannot generate or check CRC for IBM-compatible soft-sectored disks. The SIO also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows very high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 8- or 16-bit sync characters regardless of the programmed character length.

The SIO supports synchronous bit-oriented protocols such as SDLC and HDLC by performing automatic flag sending, zero insertion and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message the SIO automatically transmits the CRC and trailing flag when the transmit buffer becomes empty. If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. One to eight bits per character can be sent, which allows reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically synchronizes on the leading flag of a frame in SDLC or HDLC, and provides a synchronization signal on the $\overline{\text{SYNC}}$ pin; an interrupt can also be programmed. The receiver can be programmed to search for frames addressed by a single byte to only a specified user-selected address or to a global broadcast address. In this mode, frames that do not match either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For transmitting data, an interrupt on the first received character or on every character can be selected. The receiver automatically deletes all zeroes inserted by the transmitter during character assembly. It also calculates and automatically checks the CRC to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers.

The SIO can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SIO can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SIO then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received.

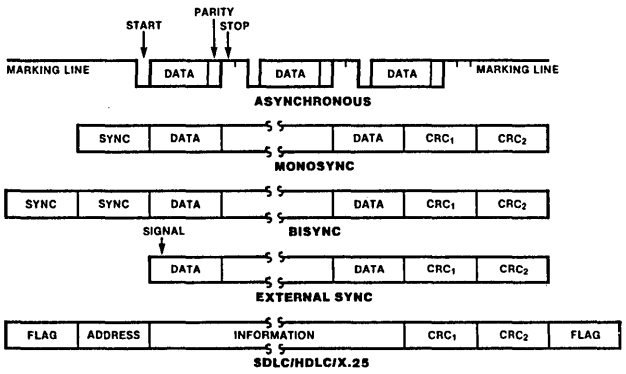


Figure 9. Some Z-80 SIO Protocols

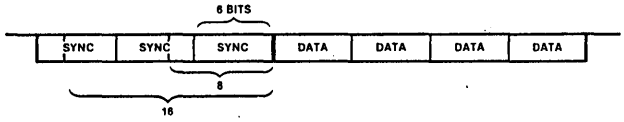


Figure 10.

I/O Interface Capabilities

The SIO offers the choice of polling, interrupt (vectored or non-vectored) and block-transfer modes to transfer data, status and control information to and from the CPU. The block-transfer mode can also be implemented under DMA control.

Polling. Two status registers are updated at appropriate times for each function being performed (for example, CRC error-status valid at the end of a message). When the CPU is operated in a polling fashion, one of the SIO's two status registers is used to indicate whether the SIO has some data or needs some data. Depending on the contents of this register, the CPU will either write data, read data, or just go on. Two bits in the register indicate that a data transfer is needed. In addition, error and other conditions are indicated. The second status register (special receive conditions) does not have to be read in a polling sequence, until a character has been received. All interrupt modes are disabled when operating the device in a polled environment.

Interrupts. The SIO has an elaborate interrupt scheme to provide fast interrupt service in real-time applications. A control register and a status register in Channel B contain the interrupt vector. When programmed to do so, the SIO can modify three bits of the interrupt vector in the status register so that it points directly to one of eight interrupt service routines in memory, thereby servicing conditions in both channels and eliminating most of the needs for a status-analysis routine.

Transmit interrupts, receive interrupts and external/status interrupts are the main sources of interrupts. Each interrupt source is enabled under program control, with Channel A having a higher priority than Channel B, and with receive, transmit and external/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted by the transmit buffer becoming empty. (This implies that the transmitter must have had a data character written into it so it can become empty.) The receiver can interrupt the CPU in one of two ways:

- Interrupt on first received character
- Interrupt on all received characters

Interrupt-on-first-received-character is typically used with the block-transfer mode. Interrupt-on-all-received-characters has the option of modifying the interrupt vector in the event of a parity error. Both of these interrupt modes will also interrupt under special receive conditions on a character or message basis (end-of-frame interrupt in SDLC, for example). This means that the special-receive condition can cause an interrupt only if the interrupt-on-first-received-character or interrupt-on-all-received-characters mode is selected. In interrupt-on-first-received-character, an interrupt can occur from special-receive conditions (except parity error) after the first-received-character interrupt (example: receive-overrun interrupt).

The main function of the external/status interrupt is to monitor the signal transitions of the Clear To Send ($\overline{CTS}$), Data Carrier Detect ($\overline{DCD}$) and Synchronization ($\overline{SYNC}$) pins (Figures 1 through 6). In addition, an external/status interrupt is also caused by a CRC-sending condition or by the detection of a break sequence (asynchronous mode) or abort sequence (SDLC mode) in the data stream. The interrupt caused by the break/abort sequence allows the SIO to interrupt when the break/abort sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the break/abort condition in external logic.

I/O Interface Capabilities (Continued)

In a Z-80 CPU environment (Figure 11), SIO interrupt vectoring is "automatic": the SIO passes its internally-modifiable 8-bit interrupt vector to the CPU, which adds an additional 8 bits from its interrupt-vector (I) register to form the memory address of the interrupt-routine table. This table contains the address of the beginning of the interrupt routine itself. The process entails an indirect transfer of CPU control to the interrupt routine, so that the next instruction executed after an interrupt acknowledge by the CPU is the first instruction of the interrupt routine itself.

CPU/DMA Block Transfer. The SIO's block-transfer mode accommodates both CPU block transfers and DMA controllers (Z-80 DMA or other designs). The block-transfer mode uses the Wait/Ready output signal, which is selected with three bits in an internal control register. The Wait/Ready output signal can be programmed as a $\overline{\text{WAIT}}$ line in the CPU block-transfer mode or as a $\overline{\text{READY}}$ line in the DMA block-transfer mode.

To a DMA controller, the SIO $\overline{\text{READY}}$ output indicates that the SIO is ready to transfer data to or from memory. To the CPU, the $\overline{\text{WAIT}}$ output indicates that the SIO is not ready to transfer data, thereby requesting the CPU to extend the I/O cycle.

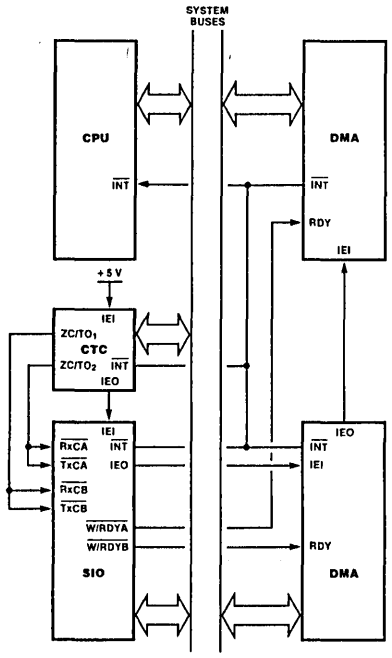


Figure 11. Typical Z-80 Environment

Internal Structure

The internal structure of the device includes a Z-80 CPU interface, internal control and interrupt logic, and two full-duplex channels. Each channel contains its own set of control and status (write and read) registers, and control and status logic that provides the interface to modems or other external devices.

The registers for each channel are designated as follows:

WR0-WR7 — Write Registers 0 through 7
RR0-RR2 — Read Registers 0 through 2

The register group includes five 8-bit control registers, two sync-character registers and two status registers. The interrupt vector is written into an additional 8-bit register (Write Register 2) in Channel B that may be read through another 8-bit register (Read Register 2) in Channel B. The bit assignment and functional grouping of each register is configured to simplify and organize the programming process. Table 1 lists the functions assigned to each read or write register.

Read Register Functions	
RR0	Transmit/Receive buffer status, interrupt status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only)

Write Register Functions	
WR0	Register pointers, CRC initialize, initialization commands for the various modes, etc.
WR1	Transmit/Receive interrupt and data transfer mode definition.
WR2	Interrupt vector (Channel B only)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync character or SDLC address field
WR7	Sync character or SDLC flag

Internal Structure (Continued)

The logic for both channels provides formats, synchronization and validation for data transferred to and from the channel interface. The modem control inputs, Clear To Send ($\overline{CTS}$) and Data Carrier Detect ($\overline{DCD}$), are monitored by the external control and status logic under program control. All external control-and-status-logic signals are general-purpose in nature and can be used for functions other than modem control.

Data Path. The transmit and receive data path illustrated for Channel A in Figure 12 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode and—in asynchronous modes—the character length.

The transmitter has an 8-bit transmit data buffer register that is loaded from the internal data bus, and a 20-bit transmit shift register that can be loaded from the sync-character buffers or from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

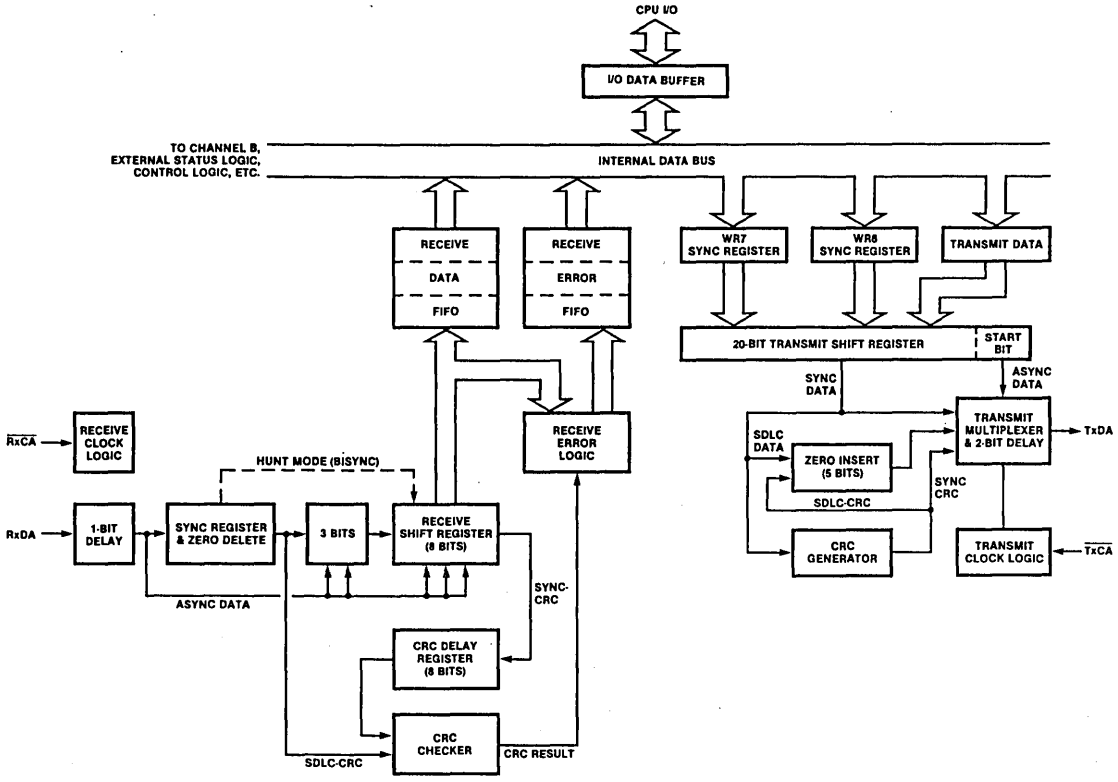


Figure 12. Transmit and Receive Data Path (Channel A)

Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first; then the interrupt mode; and finally, receiver or transmitter enable.

Both channels contain registers that must be programmed via the system program prior to operation. The channel-select input (B/$\overline{A}$) and the control/data input (C/$\overline{D}$) are the command-structure addressing controls, and are normally controlled by the CPU address bus. Figures 15 and 16 illustrate the timing relationships for programming the write registers and transferring data and status.

Read Registers. The SIO contains three read registers for Channel B and two read registers for Channel A (RR0-RR2 in Figure 13) that can be read to obtain the status information; RR2 contains the internally-modifiable interrupt vector and is only in the Channel B register set. The status information includes error conditions, interrupt vector and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing a read instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occurred, all the appropriate error bits can be read from a single register (RR1).

Write Registers. The SIO contains eight write registers for Channel B and seven write registers for Channel A (WR0-WR7 in Figure 14) that are programmed separately to configure the functional personality of the channels; WR2 contains the interrupt vector for both channels and is only in the Channel B register set. With the exception of WR0, programming the write registers requires two bytes. The first byte is to WR0 and contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the SIO.

WR0 is a special case in that all of the basic commands can be written to it with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This implies that a channel reset must not be combined with the pointing to any register.

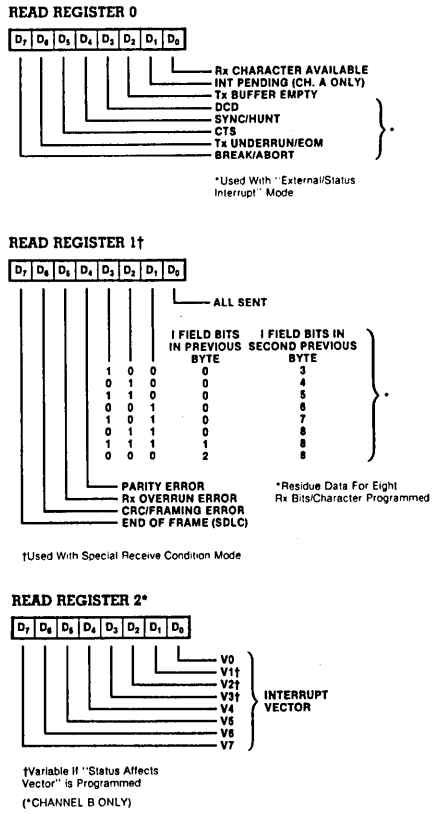


Figure 13. Read Register Bit Functions

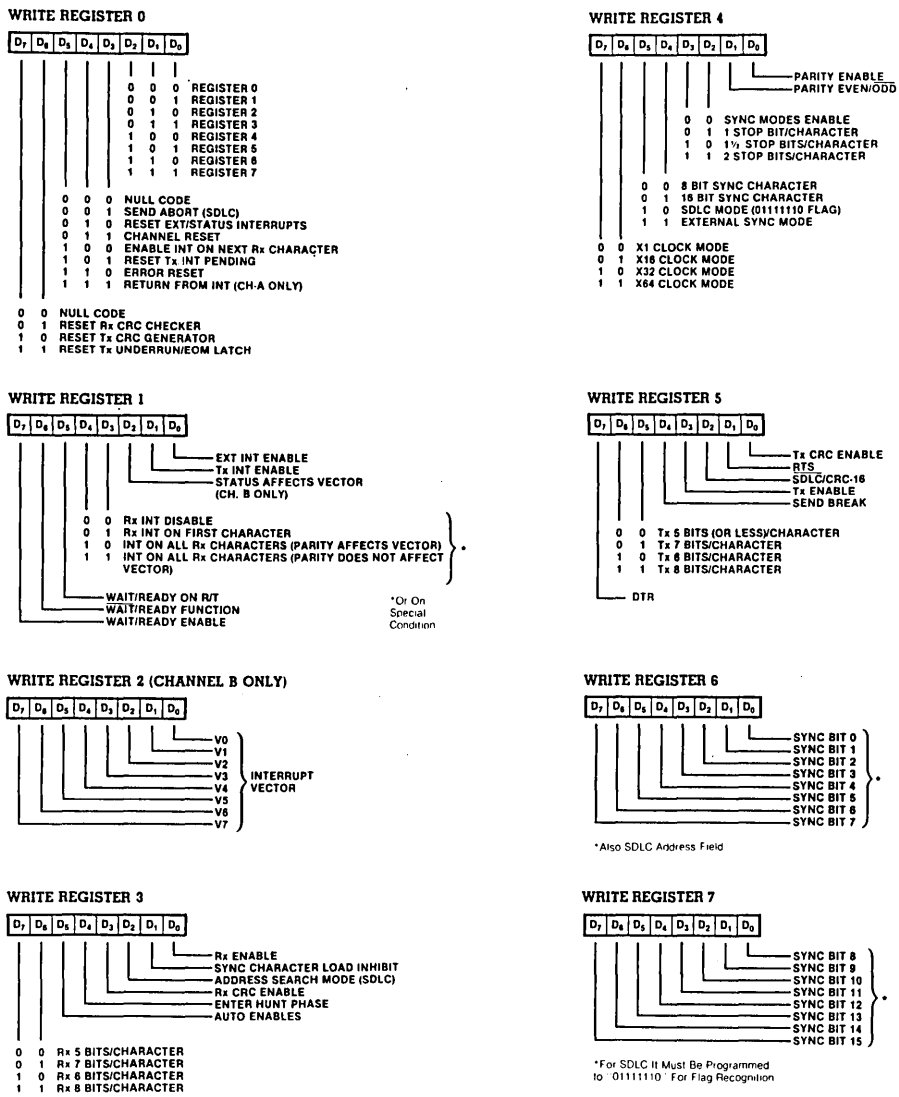


Figure 14. Write Register Bit Functions

Timing

The SIO must have the same clock as the CPU (same phase and frequency relationship, not necessarily the same driver).

Read Cycle. The timing signals generated by a Z-80 CPU input instruction to read a data or status byte from the SIO are illustrated in Figure 15.

Write Cycle. Figure 16 illustrates the timing and data signals generated by a Z-80 CPU output instruction to write a data or control byte into the SIO.

Interrupt-Acknowledge Cycle. After receiving an interrupt-request signal from an SIO ($\overline{INT}$ pulled Low), the Z-80 CPU sends an interrupt-acknowledge sequence ($\overline{M1}$ Low, and $\overline{IORQ}$ Low a few cycles later) as in Figure 17.

The SIO contains an internal daisy-chained interrupt structure for prioritizing nested interrupts for the various functions of its two channels, and this structure can be used within an external user-defined daisy chain that prioritizes several peripheral circuits.

The IEI of the highest-priority device is terminated High. A device that has an interrupt pending or under service forces its IEO Low. For devices with no interrupt pending or under service, IEO = IEI.

To insure stable conditions in the daisy chain, all interrupt status signals are prevented from changing while $\overline{M1}$ is Low. When $\overline{IORQ}$ is Low, the highest priority interrupt requestor (the one with IEI High) places its interrupt vector on the data bus and sets its internal interrupt-under-service latch.

Return From Interrupt Cycle. Figure 18 illustrates the return from interrupt cycle. Normally, the Z-80 CPU issues a RETI (Return From Interrupt) instruction at the end of an interrupt service routine. RETI is a 2-byte opcode (ED-4D) that resets the interrupt-under-service latch in the SIO to terminate the interrupt that has just been processed. This is accomplished by manipulating the daisy chain in the following way.

The normal daisy-chain operation can be used to detect a pending interrupt; however, it cannot distinguish between an interrupt under service and a pending unacknowledged interrupt of a higher priority. Whenever "ED" is decoded, the daisy chain is modified by forcing High the IEO of any interrupt that has not yet been acknowledged. Thus the daisy chain identifies the device presently under service as the only one with an IEI High and an IEO Low. If the next opcode byte is "4D," the interrupt-under-service latch is reset.

The ripple time of the interrupt daisy chain (both the High-to-Low and the Low-to-High transitions) limits the number of devices that can be placed in the daisy chain. Ripple time can be improved with carry-look-ahead, or by extending the interrupt-acknowledge cycle. For further information about techniques for increasing the number of daisy-chained devices, refer to the *Z-80 CPU Product Specification.*

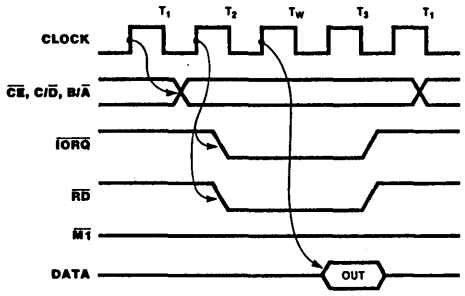


Figure 15. Read Cycle

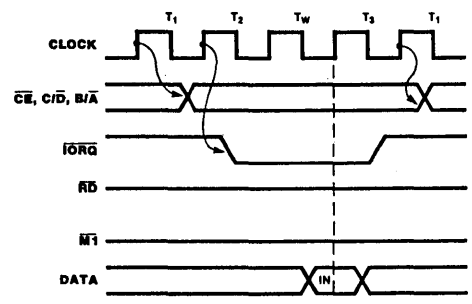


Figure 16. Write Cycle

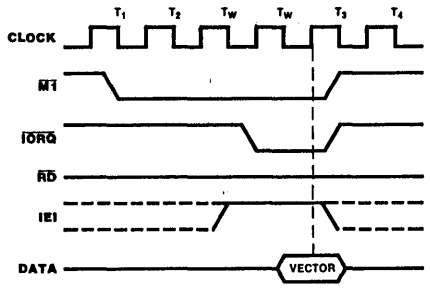


Figure 17. Interrupt Acknowledge Cycle

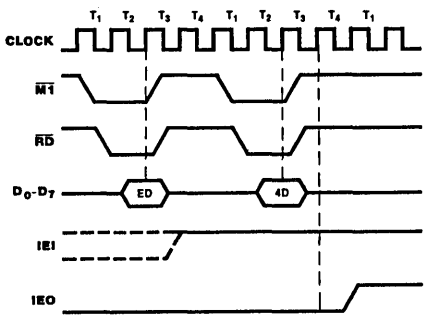


Figure 18. Return from Interrupt Cycle

Absolute Maximum Ratings

Voltages on all inputs and outputs with respect to GND . . . . . -0.3 V to +7.0 V

Operating Ambient Temperature . . . . . As Specified in Ordering Information

Storage Temperature . . . . . -65°C to +150°C

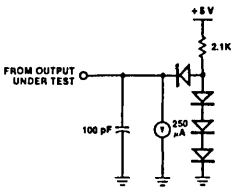
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Test Conditions

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0 V). Positive current flows into the referenced pin. Available operating temperature ranges are:

- S* = 0°C to +70°C, $+4.75\ V \leq V_{CC} \leq +5.25\ V$
- E* = −40°C to +85°C, $+4.75\ V \leq V_{CC} \leq +5.25\ V$
- M* = −55°C to +125°C, $+4.5\ V \leq V_{CC} \leq +5.5\ V$

*See Ordering Information section for package temperature range and product number.



DC Characteristics

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	+0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-0.6	+5.5	V	
V_{IL}	Input Low Voltage	-0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.0	+5.5	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4		V	I_{OH} = -250 µA
I_{LI}	Input Leakage Current	-10	+10	µA	$0 < V_{IN} < V_{CC}$
I_Z	3-State Output/Data Bus Input Leakage Current	-10	+10	µA	$0 < V_{IN} < V_{CC}$
$I_{L(SY)}$	$\overline{SYNC}$ Pin Leakage Current	-40	+10	µA	$0 < V_{IN} < V_{CC}$
I_{CC}	Power Supply Current		100	mA	

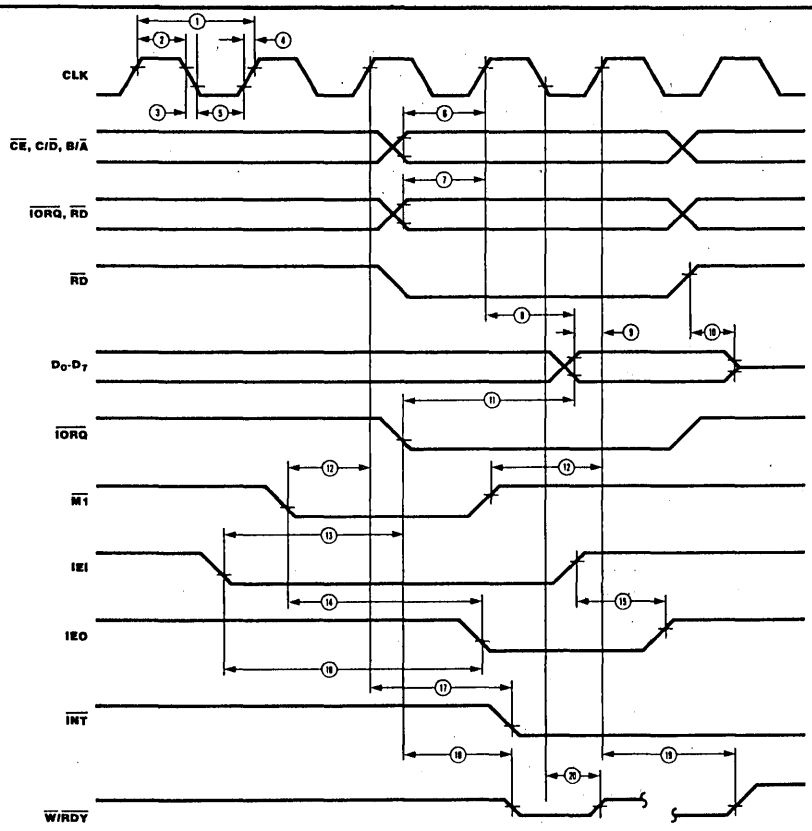
Over specified temperature and voltage range.

Capacitance

Symbol	Parameter	Min	Max	Unit	Test Condition
C	Clock Capacitance		40	pF	Unmeasured
C_{IN}	Input Capacitance		5	pF	pins returned
C_{OUT}	Output Capacitance		10	pF	to ground

Over specified temperature range; f = 1MHz

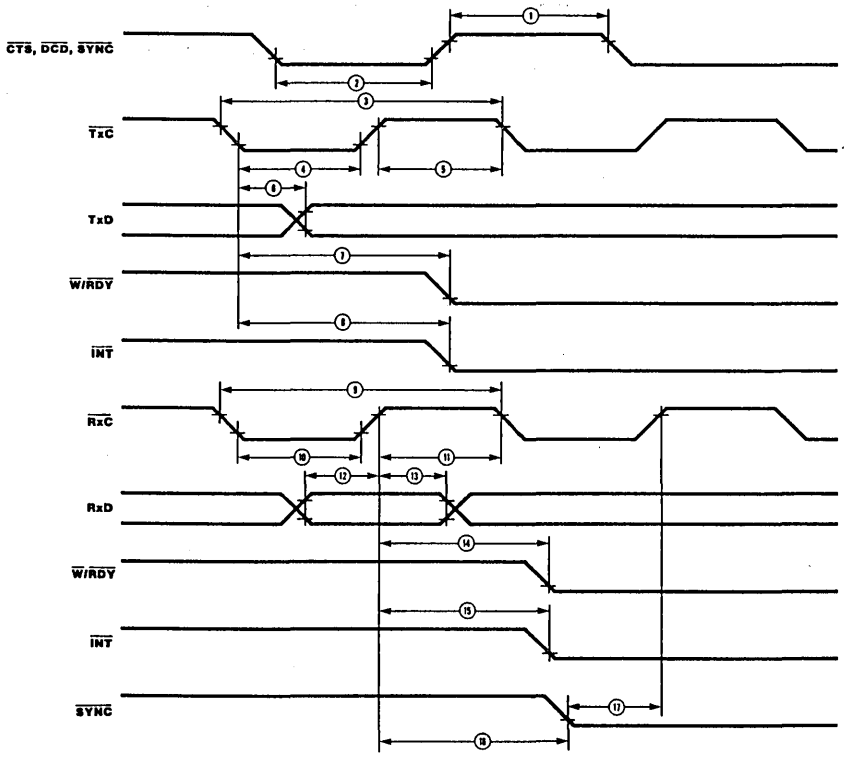
AC Electrical Characteristics



Number	Symbol	Parameter	Z-80 SIO Min	Z-80 SIO Max	Z-80A SIO Min	Z-80A SIO Max	Z-80B SIO*† Min	Z-80B SIO*† Max
1	TcC	Clock Cycle Time	400	4000	250	4000	165	4000
2	TwCh	Clock Width (High)	170	2000	105	2000	70	2000
3	TfC	Clock Fall Time		30		30		15
4	TrC	Clock Rise Time		30		30		15
5	TwCl	Clock Width (Low)	170	2000	105	2000	70	2000
6	TsAD(C)	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to Clock ↑ Setup Time	160		145		60	
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup Time	240		115		60	
8	TdC(DO)	Clock ↑ to Data Out Delay		240		220		150
9	TsDI(C)	Data In to Clock ↑ Setup (Write or $\overline{M1}$ Cycle)	50		50		30	
10	TdRD(DOz)	$\overline{RD}$ ↑ to Data Out Float Delay		230		110		90
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTACK Cycle)		340		160		100
12	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	210		90		75	
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time (INTACK Cycle)	200		140		120	
14	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (interrupt before $\overline{M1}$)		300		190	160	
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		150		100		70
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		150		100		70
17	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		200		200		150
18	TdIO(W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W/RDY}$ ↓ (Delay Wait Mode)		300		210		175
19	TdC(W/RR)	Clock ↑ to $\overline{W/RDY}$ ↑ Delay (Ready Mode)		120		120		100
20	TdC(W/RWz)	Clock ↓ to $\overline{W/RDY}$ Float Delay (Wait Mode)		150		130		110
21	Th	Any unspecified Hold when Setup is specified	0		0		0	

* Z-80 SIO timings are preliminary and subject to change.
† Units in nanoseconds (ns).

AC Electrical Characteristics (Continued)



Number	Symbol	Parameter	Z-80 SIO Min	Z-80 SIO Max	Z-80A SIO Min	Z-80A SIO Max	Z-80B SIO[1] Min	Z-80B SIO[1] Max	Notes†
1	TwPh	Pulse Width (High)	200		200		200		2
2	TwPl	Pulse Width (Low)	200		200		200		2
3	TcTxC	$\overline{TxC}$ Cycle Time	400	∞	400	∞	330	∞	2
4	TwTxCl	$\overline{TxC}$ Width (Low)	180	∞	180	∞	100	∞	2
5	TwTxCh	$\overline{TxC}$ Width (High)	180	∞	180	∞	100	∞	2
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay (x1 Mode)		400		300		220	2
7	TdTxC(W/RRf)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	5	9	5	9	5	9	3
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	5	9	3
9	TcRxC	$\overline{RxC}$ Cycle Time	400	∞	400	∞	330	∞	2
10	TwRxCl	$\overline{RxC}$ Width (Low)	180	∞	180	∞	100	∞	2
11	TwRxCh	$\overline{RxC}$ Width (High)	180	∞	180	∞	100	∞	2
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (x1 Mode)	0		0		0		2
13	ThRxD(RxC)	$\overline{RxC}$ ↑ to RxD Hold Time (x1 Mode)	140		140		100		2
14	TdRxC(W/RRf)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10	13	10	13	10	13	3
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10	13	10	13	10	13	3
16	TdRxC(SYNC)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ ↓ Delay (Output Modes)	4	7	4	7	4	7	3
17	TsSYNC(RxC)	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↑ Setup (External Sync Modes)	-100		-100			100	2

NOTES:
† In all modes, the System Clock rate must be at least five times the maximum data rate.
1. Z-80 SIO timings are preliminary and subject to change.
2. Units in nanoseconds (ns).
3. Units equal to System Clock Periods.

Ordering Information

Product Number	Package/ Temp	Speed	Description
Z8440	CE,CM	2.5 MHz	Z80 SIO/0 (40-pin)
Z8440	CMB,CS	2.5 MHz	Same as above
Z8440	DE,DS	2.5 MHz	Same as above
Z8440	PE,PS	2.5 MHz	Same as above
Z8440A	CE,CM	4.0 MHz	Z80A SIO/0 (40-pin)
Z8440A	CMB,CS	4.0 MHz	Same as above
Z8440A	DE,DS	4.0 MHz	Same as above
Z8440A	PE,PS	4.0 MHz	Same as above
Z8440B	CS	6.0 MHz	Z80B SIO/0 (40-pin)
Z8440B	DS	6.0 MHz	Same as above
Z8440B	PS	6.0 MHz	Same as above
Z8441	CE,CM	2.5 MHz	Z80 SIO/1 (40-pin)
Z8441	CMB,CS	2.5 MHz	Same as above
Z8441	DE,DS	2.5 MHz	Same as above
Z8441	PE,PS	2.5 MHz	Same as above
Z8441A	CE,CM	4.0 MHz	Z80A SIO/1 (40-pin)
Z8441A	CMB,CS	4.0 MHz	Same as above
Z8441A	DE,DS	4.0 MHz	Z80B SIO/1 (40-pin)
Z8441A	PE,PS	4.0 MHz	Same as above
Z8441B	CS	6.0 MHz	Z80B SIO/1 (40-pin)
Z8441B	DS	6.0 MHz	Same as above
Z8441B	PS	6.0 MHz	Same as above
Z8442	CE,CM	2.5 MHz	Z80 SIO/2 (40-pin)
Z8442	CMB,CS	2.5 MHz	Same as above
Z8442	DE,DS	2.5 MHz	Same as above
Z8442	PE,PS	2.5 MHz	Same as above
Z8442A	CE,CM	4.0 MHz	Z80A SIO/2 (40-pin)
Z8442A	CMB,CS	4.0 MHz	Same as above
Z8442A	DE,DS	4.0 MHz	Same as above
Z8442A	PE,PS	4.0 MHz	Same as above
Z8442B	CS	6.0 MHz	Z80B SIO/2 (40-pin)
Z8442B	DS	6.0 MHz	Same as above
Z8442B	PS	6.0 MHz	Same as above

*NOTES: C = Ceramic, D = Cerdip, P = Plastic; E = -40°C to +85°C, M = -55°C to +125°C, MB = -55°C to +125°C with MIL-STD-883 with Class B processing, S = 0°C to +70°C.

B. Z 8 0 A P I O . . . . . .

see Super Quad

C. Z 8 0 A C P U . . . . . .

See Super Quad

D. P A R T S L I S T

LIST OF CHIPS FOR THE SUPER SLAVE...LOCATIONS ...6-29-82..H/A

ITEM	PART NUMBER	LOCATION	QUANTITY USED
1.	74LS00	U4,U9,U26,U36	4
2.	74LS02	U6,U18,U22,U27	4
3.	74S04	U40,U60	2
4.	74LS08	U5,U15	2
5.	74LS10	U10,U25	2
6.	74LS14	U2,U28	2
7.	7416	U21	1
8.	74LS27	U24	1
9.	74LS32	U8,U20	2
10.	74LS85	U33	1
11.	74LS74	U7,U19	2
12.	74LS113	U1,U11	2
13.	74LS138	U34	1
14.	74LS139	U16	1
15.	74F157	U46,U47	2
16.	74LS174	U49	1
17.	74LS175	U17	1
18.	74LS244	U31,U38,U41	3
19.	74LS273	U32	1
20.	74LS373	U37,U42	2
21.	74LS393	U59	1
22.	25LS2521	U29	1
23.	AM9519	U13	1
24.	BR1941	U12	1
25.	CD4020	U3	1

26.	Z80A CPU	U45	1
27.	Z80A DART	U14,U30	2
28.	Z80A PIO	U43	1
29.	2716 EPROM	U44	1
30.	4164 MEMORY	U50-U58,U61-U69	18/9
31.	LM323K(SG323)	VR1	1
32.	16 PIN SWITCH	SW1	1

(R)

E. S C H E M A T I C D I A G R A M

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

PARTS LIST					
QTY REQD	FACS NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING

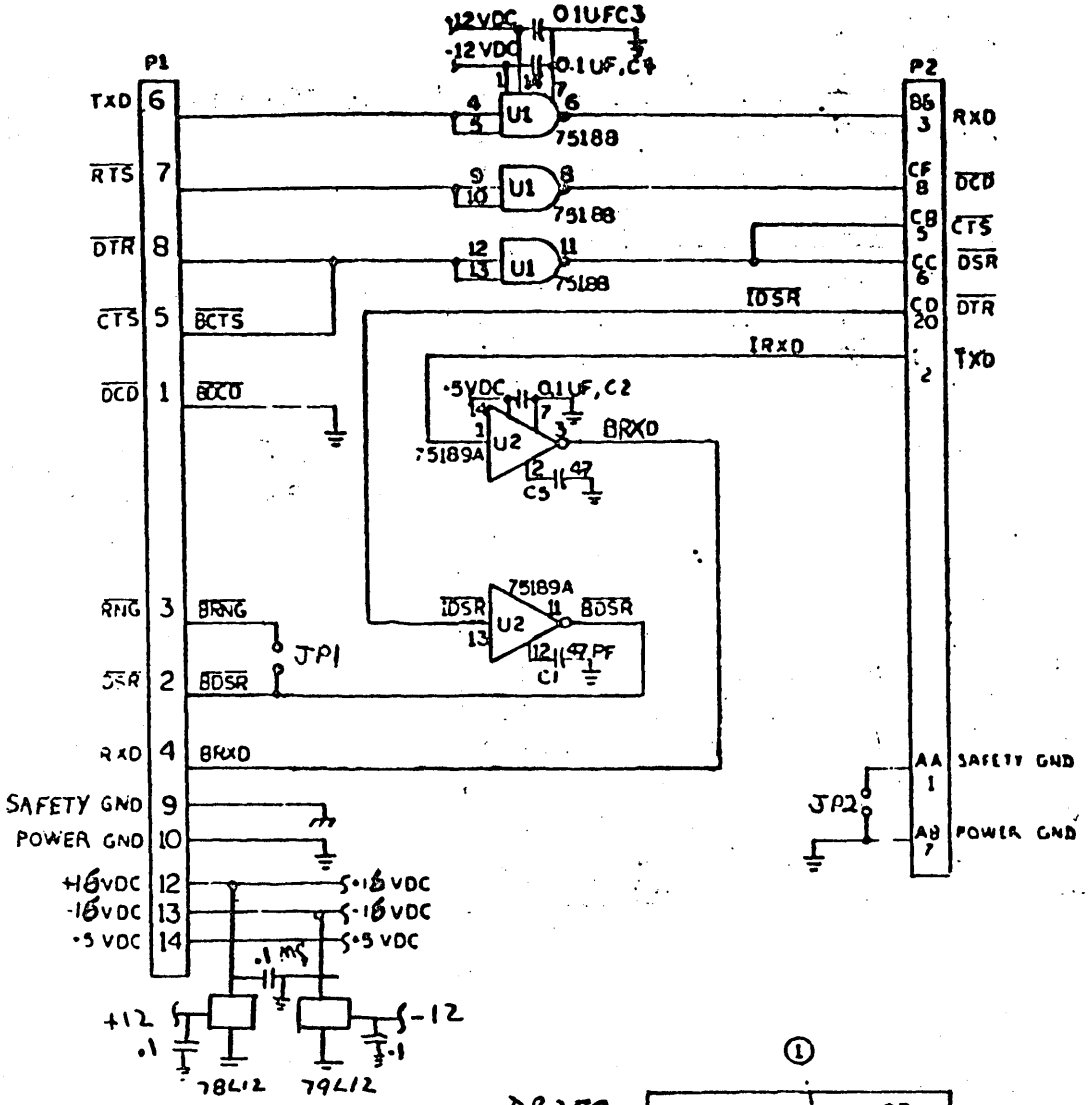
CONTRACT NO.

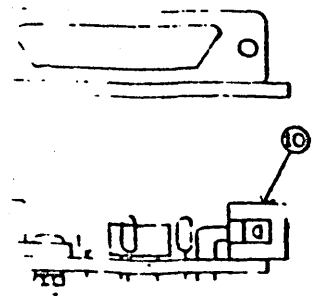
APPROVALS	DATE
DRAWN G.L.	7/1/82
CHECKED H/A	
ISSUED	

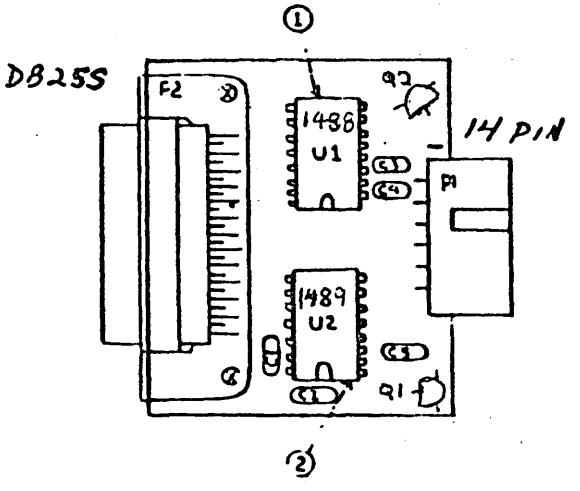
SUPER SLAVE

Advanced Micro Digital Corp.
[illegible] Hunt Ave.
Garden Grove, CA 92641

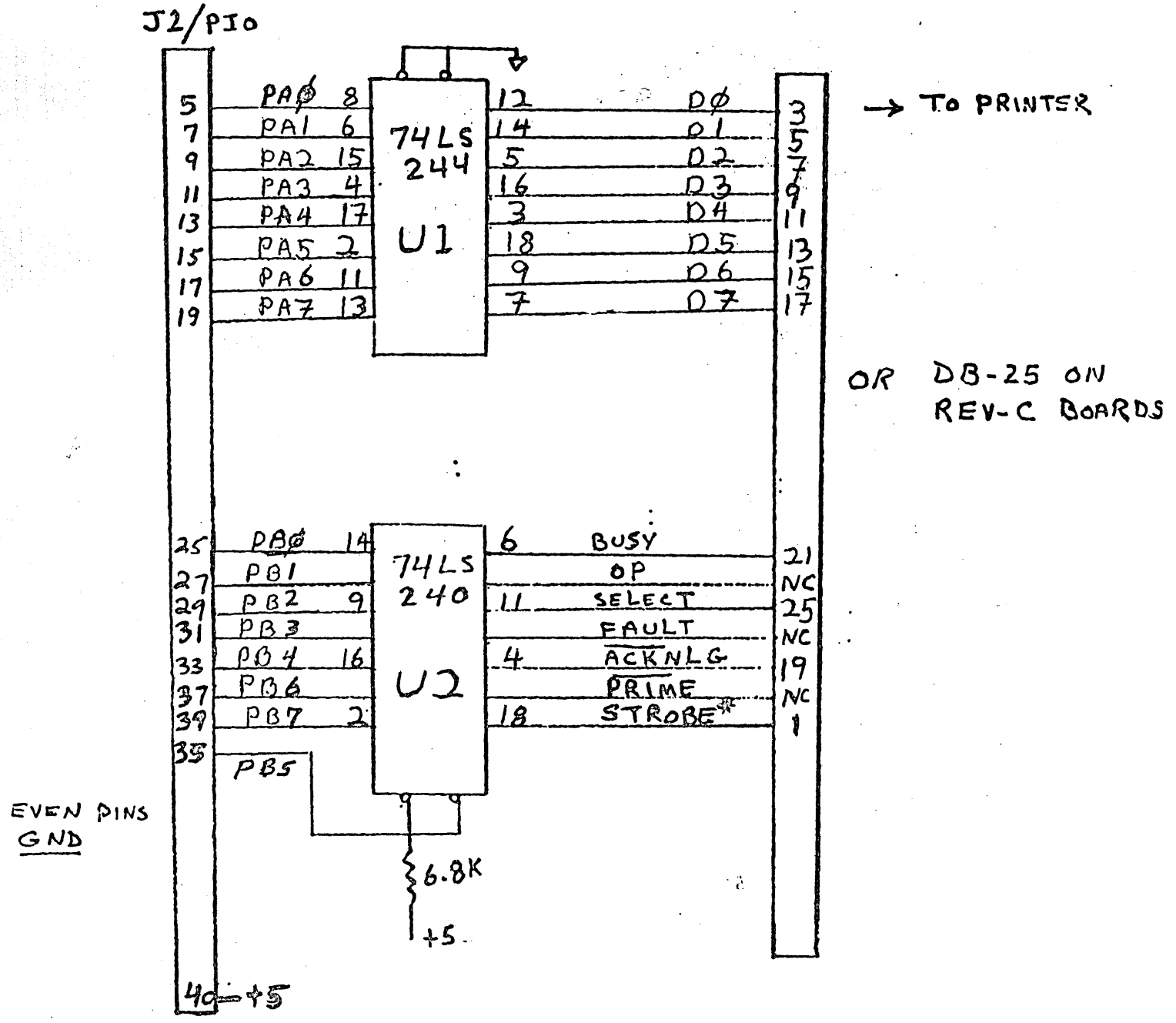
SIZE E | FSCM NO. | DWG. NO. | REV.
SCALE | SHEET







ENG. H/A
10-1-81
PS QUAD/I
ADVANCED MICRO



PSQUAD/PAR

3-25-92