MAGIC
AN ADVANCED COMPUTER FOR SPACEBORNE GUIDANCE SYSTEMS

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Summary

MAGIC is a special purpose digital computer designed specifically to provide the computational capability required in an advanced stellar-inertial guidance system for a rocket-launched space vehicle. The design of MAGIC has been optimized for this particular application but could easily be altered for any similar job. It is a programmable, whole number, binary digital computer with an adequate but not elaborate instruction repertoire. It uses a serial coincident-current, torroidal-core memory with a capacity of 4096 words of 24 bits each. The logic parts of the computer are implemented with Fairchild Micrologic elements, and those parts which could not be implemented with integrated circuits have been constructed of conventional components in welded and encapsulated modules.

Introduction

MAGIC is a miniaturized digital computer designed for use in advanced inertial guidance systems for missile and space applications. As such it is required to operate in real time on a variety of inputs from the rest of the system and must supply a variety of outputs to the rest of the system.

The MAGIC Prototype occupies a volume of .75 cubic feet and weighs 40 pounds. A production model would weigh 35 pounds and have a volume of .64 cubic feet. Power consumption of the total computer is 90 watts with 66 watts required for the Micrologic and 24 watts for the core memory. It is a complete guidance computer with all of the input, output, and computational capabilities required for its integration with an AC Spark Plug advanced inertial platform.

Figure 1 is a photograph of the computer. The cutaway drawing of Figure 2 shows the arrangement of the subassemblies. Next to the memory unit are the two chassis of welded modules, followed by four assemblies of Micrologic. The power supply, shown in Figure 2, is not a part of the prototype, but will be added later.

The computer is designed to operate without performance degradation through all phases of a missile launch. Each of the subassemblies is a sound structural unit, and they form a mutually supporting and very rigid structure when the tie bolts are tightened. Such a package design also provides for easy expansion or contraction of the computer by the addition or subtraction of subassemblies without modification of the basic structure.

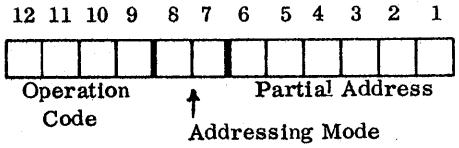
Figure 3 shows a functional block diagram of the important sections of MAGIC and the information flow among them.

MAGIC Instructions

A study made of the set of equations to be solved by MAGIC revealed that less than 20 per cent of core memory would contain data words, and that over 80 per cent of the memory would be required for the program of instructions. An error analysis further suggested that a data word length of 24 bits would be sufficient. For these reasons abbreviated addressing was decided upon so that two instructions could be packed in one word. Thus memory is utilized more efficiently and instruction access time is reduced.

There are four classes of instructions. A brief description and the instruction word format of each class are given below.

1. Arithmetic Class. The arithmetic class of instructions includes the following 70 microsecond operations: Load the A Register, Store, Add, Subtract, Mask with the A Register, and No Operation; and Multiply which requires 258 microseconds and Divide which requires 398. *



Instructions in the arithmetic class have an address which is modified for addressing relatively. Two of the address references are static and two are dynamic. Two mode bits specify which reference is to be used.

*All times include instruction access time and are independent of the operand values.

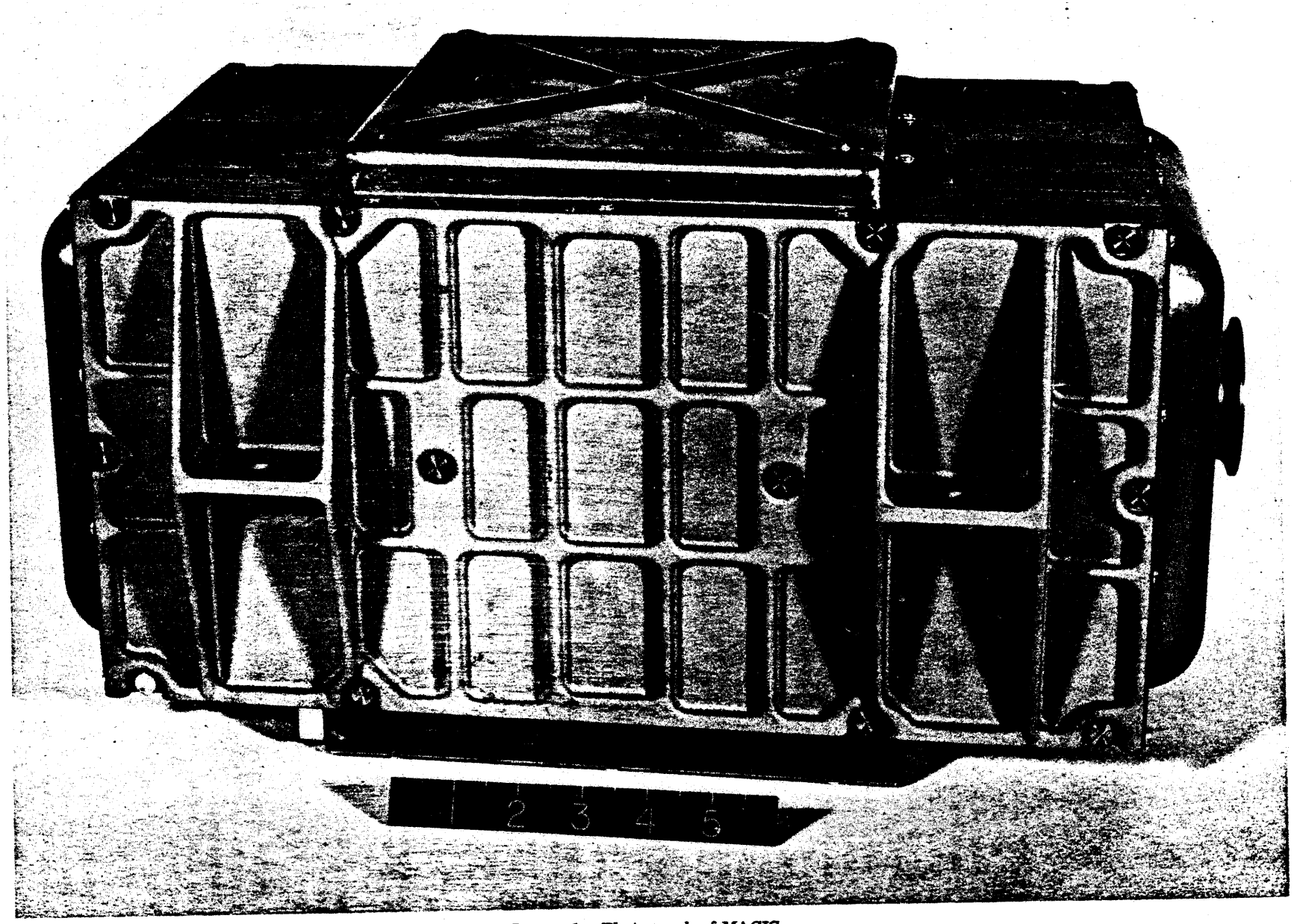


Figure 1. Photograph of MAGIC

glass boards on both the top and bottom of the package. The X and Y drive lines from the storage matrices are soldered to the terminals which are on top of the switch core assemblies.

Welded Electronics

The selection chassis contains the current regulators, current sinks and transistor switches which are associated with the primary circuits of the three switch core matrices. The Memory clock chassis, which is the timing central for the entire computer system, contains the memory sense amplifiers, and the one-shots and buffers of the clock system. Input to the timing chassis is a one megacycle reference signal from the inertial platform. Output of the chassis consists of 24 master digit times and 7 master clock pulses. All of these circuits are constructed of reasonably conventional components welded together in cordwood fashion. The individual modules are encapsulated in a microballoon-filled epoxy, and contained in an aluminum can. The can is, in turn, fastened to a magnesium heat sink. Circuit and package designs have been combined to limit the junction temperature rise of the semiconductors to $30^{\circ}C$, maximum.

Micrologic Circuits

In MAGIC all logic functions have been implemented using Fairchild Micrologic elements.[2,3,4] These elements represent the first of a number of approaches to integrated circuits to become available in production quantities. Elements in this class offer important advantages of reliability, physical size, and economics.

The Micrologic element is fundamentally a complex semiconductor device fabricated with the same techniques that have been proven in transistor manufacturing. As explained below, there are six different types of elements, each capable of implementing a particular logic function using direct-coupled transistor logic circuits. Each Micrologic element consists of from one to five DCTL NOR Gates; the circuit components--resistors and silicon planar transistors -- are diffused into a single die of silicon, and metal interconnections are deposited on top of the chip. The device is then packaged in a multi-lead TO-5 transistor can.

Connections from the element to the leads of the package are made by means of thermocompression ball bonds. A conventional cap is welded onto the header to form a hermetically sealed package.

The most fundamental logic function implemented is a three-input NOR gate and is called a G element for short. Since the NOR function is a complete logical set in itself, it is theoretically sufficient to implement all logic without the use of any other element. However, more complex circuits are desirable in any practical system.

The Flip-Flop is a static storage element, complete with means for setting it to either the ZERO or ONE state; it is called an F element for short.

The Half Shift Register (or S Element) is basically a flip-flop with gating circuits adequate to transfer information into the flip-flop under control of a single clock signal.

The Buffer (B element) acts simply as a power amplifier when the output from a Micrologic element is required to drive many other Micrologic elements.

The Half-Adder (H element) generates both the exclusive OR of its inputs, and the AND of two of its inputs.

The final Micrologic element is the Counter Adapter (C element) which provides gating in binary counter stages.

A summary of Micrologic utilizations in MAGIC is as follows:

116 B's, 7 C's, 82 F's, 1187 G's, 80 H's, and 626 S's for a total of 2,098 elements.

The number of C and H elements in the system is much smaller than would be the case if MAGIC were being designed today. The reason for this is simple. In 1961 when the purchase order for Micrologic was placed, there was some doubt as to the availability of these devices. Therefore, the logic mechanization of most of the computer was done using the gate as the only logic module.

Micrologic Interconnection

In Micrologic elements, as in all direct-coupled transistor logic circuits, the signal swing is equal to the difference between the "ON" base voltage and the saturated collector voltage. This difference is never larger than a volt, and tends to zero at high temperatures. This causes some anxiety about reliability in a sizeable operating system due to externally induced and self-induced noises. A careful study led to the conclusion that, although the problem is a real one, certain packaging considerations can relieve it to some extent.

Figure 7 illustrates the construction technique used for the Micrologic parts of MAGIC. The elements are carried on multilayer etched circuit boards which are cemented to magnesium frames. The circuit layer closest to the Micrologic cans is a continuous

sheet for the +3V power. Next is a ground plane, followed by three circuit layers.

The ground plane serves two useful purposes. First it provides a low impedance ground reference for every Micrologic circuit. Secondly, the proximity of the signal conductors to the ground plane reduces the self - and mutual-inductance effects of these wires. The logic boards were made large enough to accomodate all the circuits required for sizeable units of the computer in order to minimize the number of signal wires which have to pass through the edge connector since they must depart slightly from the ground plane at that point.

The operating experience with the computer to date indicates that the noise problems are not as severe as anticipated, and that the means used to minimize the noise generation have been quite effective.

In the prototype, about half the wiring is contained in the etched circuits. The remainder is hand wired. In a production computer, all of the wiring would be etched.

Micrologic elements do not lend themselves easily to providing output signals directly across the interface, and low-level input signals might be susceptible to noise and cross talk difficulties. Therefore, special circuits of conventional components have been utilized for output and input isolation of the Micrologic. These circuits are mounted on the etched cards with the Micrologic and can be seen in Figure 7. The plastic blocks contain resistor-diode networks which give input signal level shifts and provide some noise threshhold beyond that inherent in the Micrologic. Three small transistors can also be seen. They are driven directly at Micrologic signal level and provide power gain and isolation for driving signals out of the computer.

Component Count

The following list is a complete count of the electronic components in MAGIC:

Ferrite storage Cores	98,304
Ferrite Switch Cores	768
Micrologic Elements	2,098
Transistors	495
Diodes	2,475
Resistors	1,623
Capacitors	265
Transformers	72

Conclusions

The original design goals for MAGIC have been exceeded insofar as the power, weight, and volume are concerned. Early indications are that the expected reliability figure may be achievable, but only time can tell the true story. The computer has clocked 400 hours of operating time since the first stored program was run. During this time there have been no spontaneous component failures of any kind.

Acknowledgment

It would be impractical to list by name all the devoted individuals in both the El Segundo and Milwaukee facilities of AC Spark Plug who have made a substantial contribution to the MAGIC project. The list would be enormous. Suffice it to say that the authors extend a most grateful acknowledgment to each and every magician.

References

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2. Norman, R., Last, J., and Haas, I., Solid State Micrologic Elements presented at Solid State Circuits Conference, February 1960.

3. Farina, D., Nall, J., and Anderson, R., Application of Micrologic Elements presented at National Electronics Conference, October 1960.

4. Norman, R. H., and Anderson, R. C., Testing Micrologic Elements presented at WJCC, Los Angeles, May 1961.

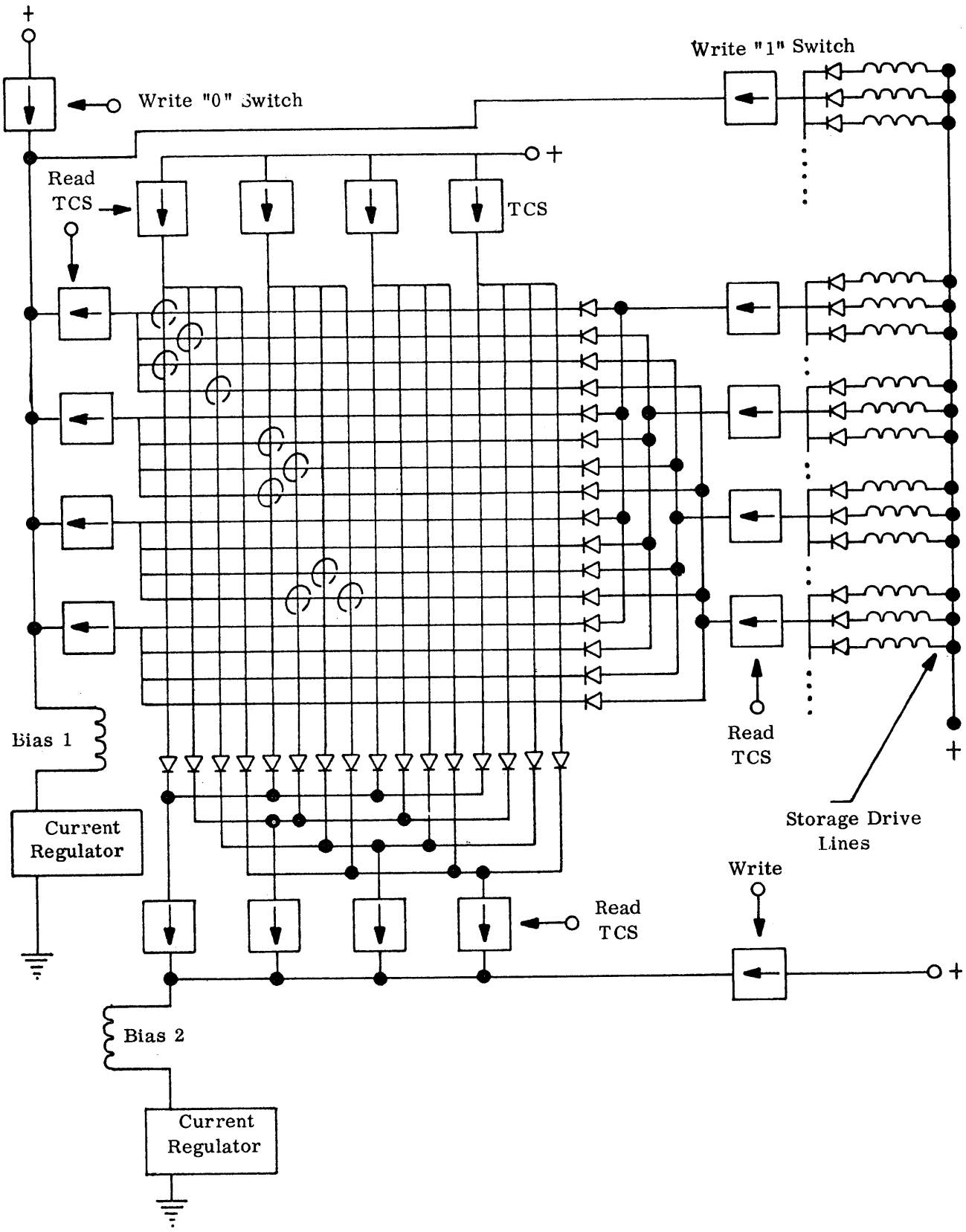


Figure 5. Switch Core Matrix

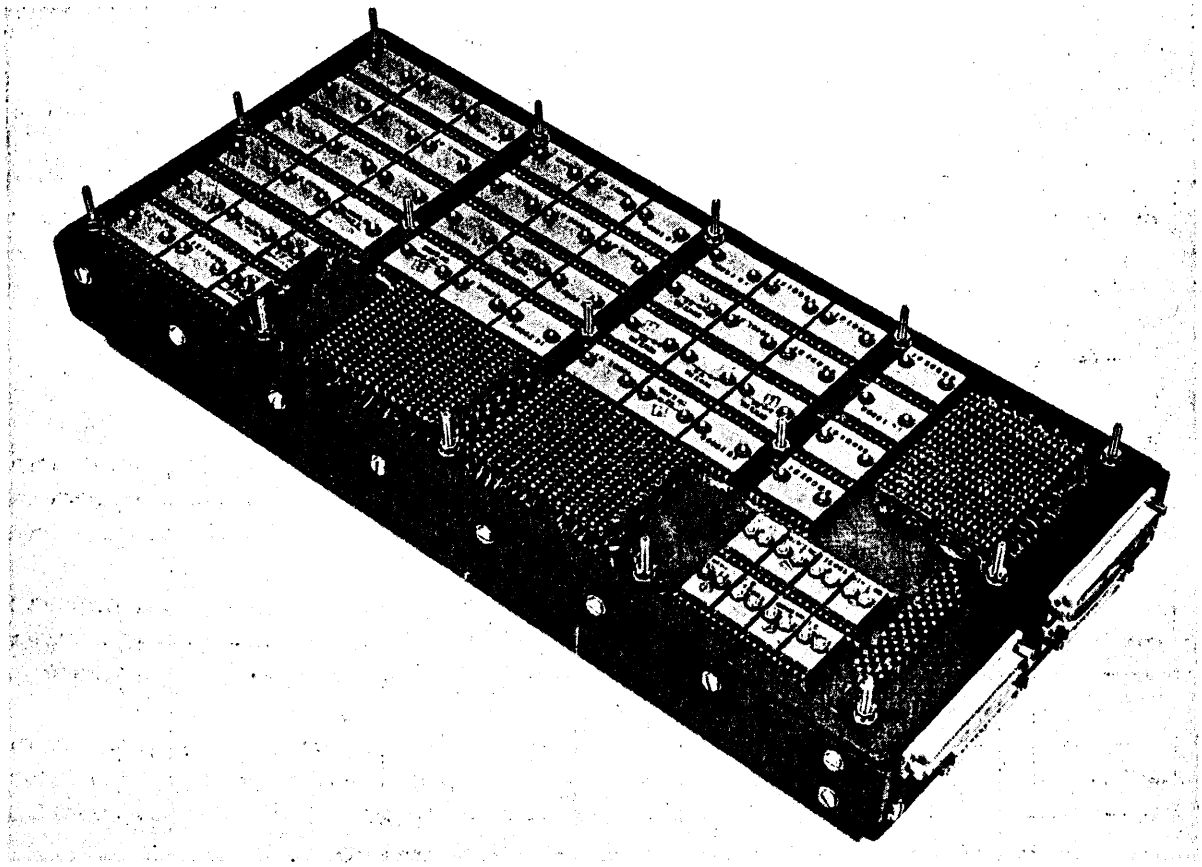


Figure 6. Magnetic Memory Package

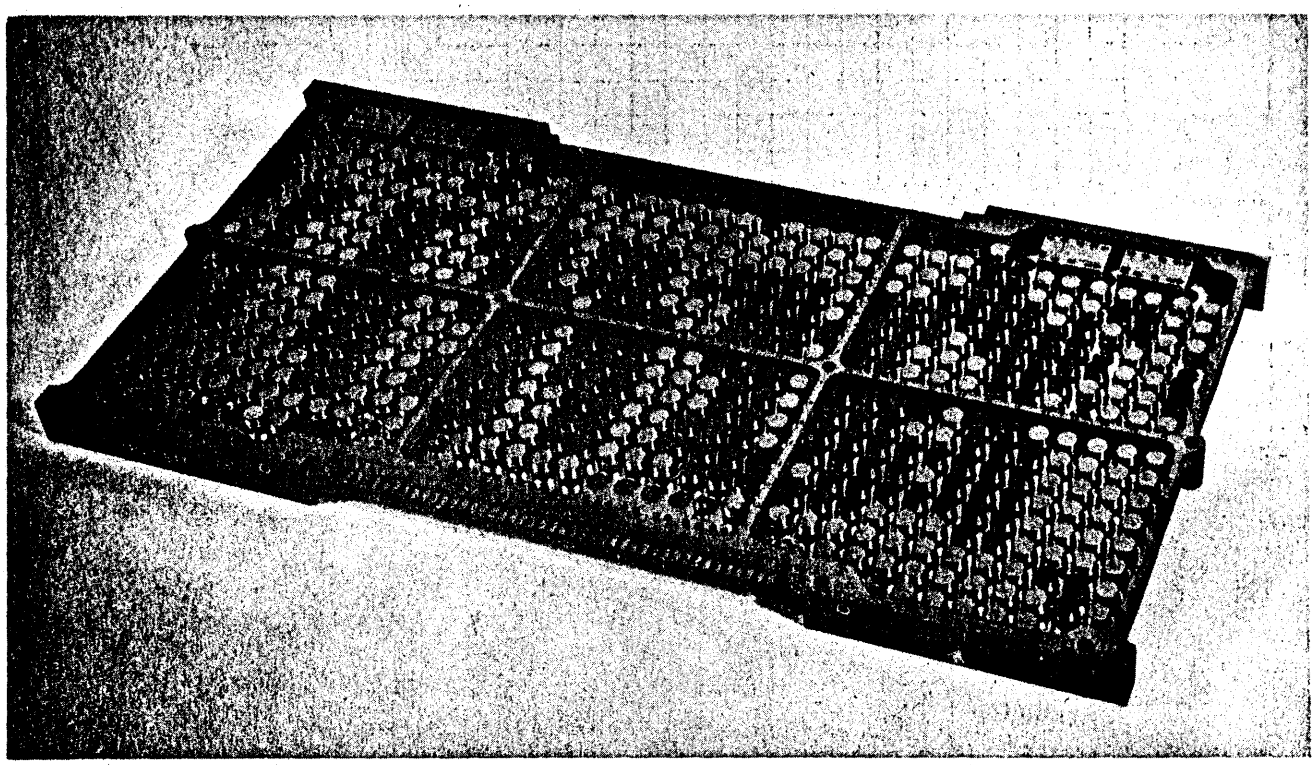


Figure 7. Micrologic Board

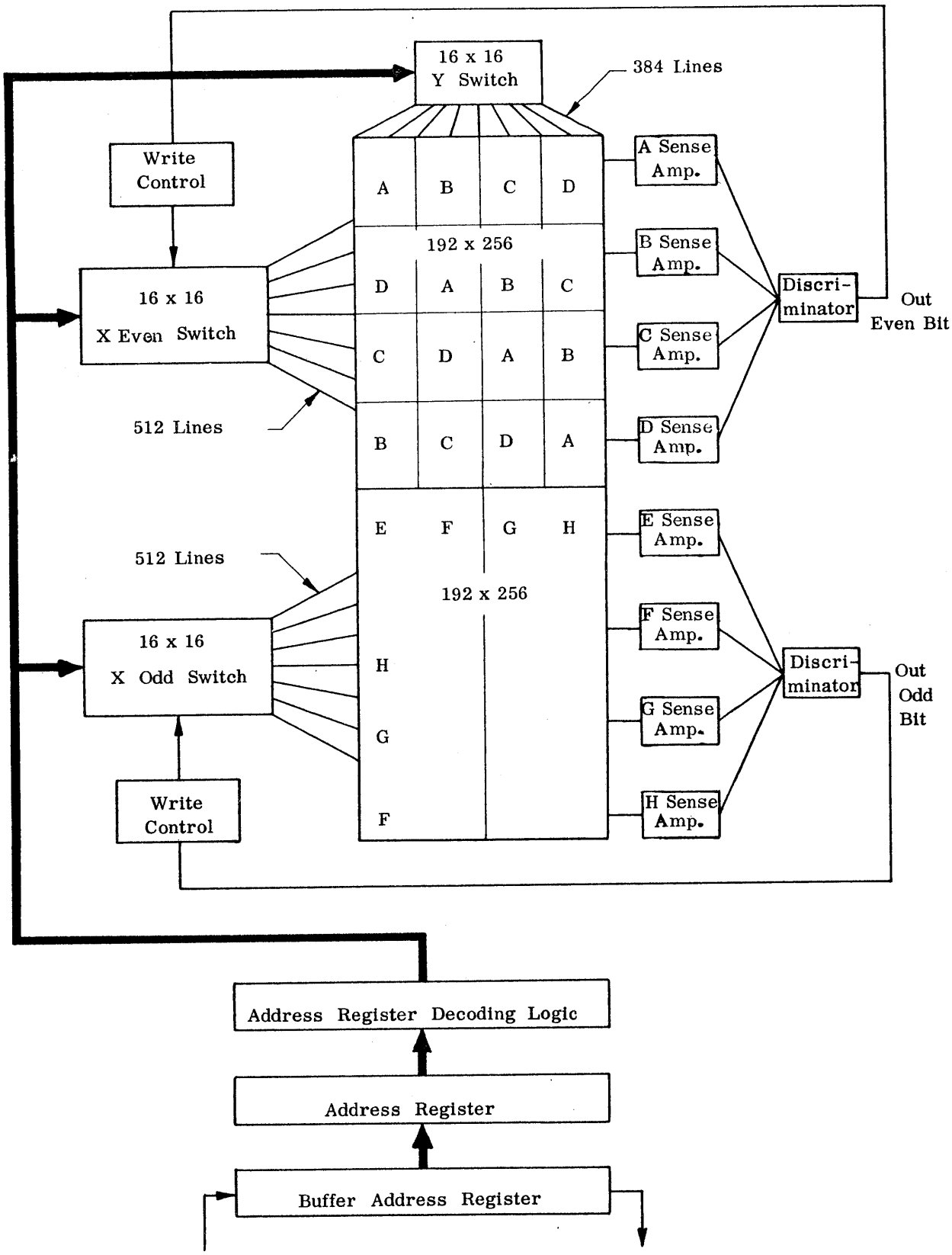


Figure 4. Memory Schematic

are read and written two at a time, and the storage array is divided into two halves. If a number (N) is represented in the usual two's complement format of

$N = -A_0 2^0 + A_1 2^{-1} + A_2 2^{-2} + \ldots A_{23} 2^{-23}$, then

the bits which represent the even-numbered coefficients A_0, A_2, etc., are stored in one half of the memory and the odd-numbered bits are stored in the other half. Both halves share the same Y drive lines but have separate X drive lines. The Y switch matrix must always generate both read and write current pulses. The two X switches always generate read current pulses, but they are individually controlled by separate writing circuits. If a "1" is to be written into a core in one half, the X write current is enabled in that half. If a "0" is to be written into that core, the write cycle is inhibited. This allows the memory system to operate with only double coincidence of currents in the storage cores. This contrasts with the usual parallel coincident current memory in which currents flow in X and Y and digit-plane windings, yielding triple coincidence in the cores during writing. The individual tolerances of these currents must be accounted for in determining the operating margins of the memory system. The total allowable variation is determined by the storage core characteristics. In a double coincidence system the allowable current variations will be greater than can be allowed in a triple coincidence system.

The use of two wires in each selection direction through the storage cores allows the output from one current generator to be steered through one winding for read and the other for write, guaranteeing that a symmetrical drive condition will exist in the storage core. If two drive lines are not used in each direction, it is necessary to have positive and negative currents generated by separate circuits, and the individual tolerances of these circuits must be accounted for in the overall system performance. Using double coincidence, a five wire system, in conjunction with temperature compensation of the current sources, allows satisfactory drive current margins for reliable operation over a temperature range of $0^{\circ}C$ to $70^{\circ}C$.

Each half of the memory consists of sixteen 48 x 64 (3072) core mats. Each mat is linked by one sense winding. The sense windings of four of these mats selected diagonally across the half memory are mixed together through resistor networks at the inputs of a single sense amplifier. Four amplifiers are therefore required for each half of the memory. The four sense amplifiers are coupled to a circuit which is a level discriminator and an OR network. The output of the discriminator is used directly to set the Micrologic memory output register.

Switch Core Matrices

Figure 5 shows the primary selection windings of a switch core matrix. Two bias windings link every core in the matrix. The cores are normally biased off with one unit of drive current. Activation of a pair of transistor current switches at each end of the row and column windings allows currents to flow in the switch matrix. One unit of current cancels the bias, and the second unit of current causes one core to switch. When the core switches, the voltage generated in one of its two secondary circuits causes the read current to be steered into a drive line of the memory. When the switch core's drive currents are removed, the bias resets the core, inducing a voltage in the write secondary winding of that core. If a "1" is to be written, the current is steered by that secondary to the proper X drive line. If a "0" is to be written, the current is prevented from going through the write secondary, and is shunted away to the power supply.

It is interesting to note at this point that the address of the storage core which is to be written into had been stored in the selected switch core during the read cycle. Therefore, the information in the memory address register is not needed during the write cycle and it can be changed in preparation for the next read cycle.

The X and Y switches are similar except that on 64 of the Y switch cores no secondary windings are used since only 384 outputs are required for the Y lines of the storage matrix.

The memory operates on a four microsecond read/write cycle. Twelve cycles are required to read out a 24 bit word. Twelve bits of address are supplied by the instruction processor at the beginning of each word time. The bit counter of four stages is effectively included as part of the address register. The entire register is automatically sequenced to access the bits of the computer word which follow the first bit.

Memory Packaging

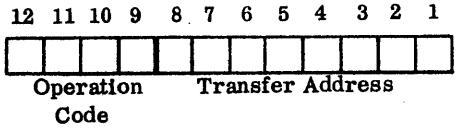
The magnetic package for the MAGIC memory is shown in Figure 6. The 50 mil cores are strung on four epoxy-glass frames which contain 24,576 cores each in eight mats of 48 x 64 cores. Internal to each frame the wiring is continuous with solder joints occurring only around the periphery of the frame. Once strung, the frame is glued to an aluminum plate and the cores are potted in silicone rubber. A special treatment is given the aluminum to insure that the silicone rubber will adhere firmly to the plate. Four such plates are required for all the storage cores. The four frames are interconnected and then folded up. In Figure 6 the storage matrices are not visible. The X and Y switch cores and their associated primary and secondary diodes are mounted on large epoxy-

The two fixed references which are added to the address field to generate an effective address are 3968 and 4032. The address field is considered to contain a positive partial address in the range 0 through 63, providing a stationary block of 128 words, any one of which may be randomly accessed.

The two dynamic references for addressing are the bias register and the instruction counter. The address field, when used for dynamic addressing, is considered to have a sign and five magnitude bits, providing a range of -32 through +31 about the reference. The address field is added to the contents of either the bias register or the instruction counter to obtain the effective address. The instruction counter as a modifiable source is extremely useful for building up short iterative program sequences such as subroutines. Whatever data is required in the sequence can usually be "carried" within the specified addressing range of the instructions. The bias register is used as a reference more often for addressing the portion of memory set aside for data in tabular form, or data used by several separate parts of the program.

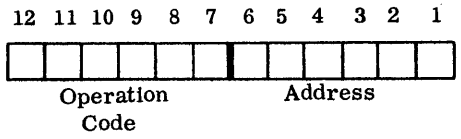
2. Transfer Class. Transfer instructions normally require 164 microseconds for execution. The types of transfers are the following: Unconditional Transfer, Unconditional Transfer and Trap Present Address, Transfer on Minus A register, and Jump on Minus A register.

The conditional jump is a 70 microsecond instruction which permits short transfers, forward or backward, relative to the setting of the instruction counter. The jump range is -128 to +127, and the instruction counter receives the sum of the jump address and the previous instruction counter contents.

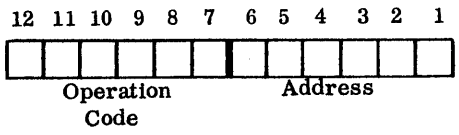


Instructions of the transfer class have two parts, the operation field and the indirect address field. In all of these instructions except the Conditional Jump, the eight bit address field denotes which one of 256 words of a transfer table in core memory contains the address of the next instruction to be executed. During the execution of a transfer the low order twelve bits of the word in the transfer table are used as the address, to replace the contents of the instruction counter, and the high order twelve bits are sent to the bias register. The transfer table occupies locations 000 through 255. Included is a "trap address" feature that saves the contents of the instruction counter and the bias register. If the computer is not in the interrupt mode, these quantities are stored in memory cell 0000. If the computer is in the interrupt mode, the register contents are stored at 0001. The bias register contents go into the most significant half and the instruction counter contents into the least significant half of the word in memory.

3. Input-Output Class. The input-output class of instructions provides the means of communicating with the outside world. In these instructions the address specifies the register or device which will send data to or receive data from the A register. The types of inputs and outputs will be treated in more detail later.



4. Miscellaneous Class. The miscellaneous class of instructions includes the shift instructions in which the address field is used to specify the shift constant. These instructions are short and permit shifting the entire range of the A and B registers in 70 microseconds. Also included are instructions to exchange the contents of the A and B registers, and to set the bias register. In the latter operation, since the bias register can hold twelve bits, the address part of the instruction is placed in the most significant half of the bias register and the least significant half of the register is zeroed.



An interesting and worthwhile by-product of the method of addressing used in MAGIC is the practicality of increasing core memory capacity without changing the addressing structure of the instructions.

Interrupt

External interrupt is included in the instruction processor design for priority control. Its purpose is to interrupt the normal sequence of program instructions upon one of the following conditions:

1) When time is the criterion for executing certain critical program phases. These are usually in the form of subroutines.

2) When, owing to the asynchronous nature of input-output devices, it becomes necessary to transfer data from or to the computer.

3) When a discrete signal is received.

Interrupt can be from only one source at a time, with a program option to acknowledge it or not. When an external interrupt is received, the instruction processor forces a direct transfer of control to memory location 0002, and executes the instruction pair found there. If one of these instructions is a transfer, the interrupt will be effective; if not, it will be ignored. If it is ignored, the cost is simply two instruction periods with all register contents preserved.

Arithmetic Unit

Three Micrologic shift registers - A, B, and M - are used to perform the standard arithmetic and shift operations, and to provide communication with the Input-Output Unit. Within the Arithmetic Unit, information flow is two bits at a time. A two-bit serial adder/subtractor is the basic arithmetic element. All numbers range between minus one and plus one, with negative numbers represented in two's complement form.

During operations which communicate with the memory the arithmetic registers shift at a 250 kc clock rate. During multiply, divide, and shift instructions the registers run at a one megacycle clock rate.

The information in the A register at the start of an addition (subtraction) is the augend (minuend). The sum (difference) is generated serially in the A register using as the adden (subtrahend) the information read serially out of memory two bits at a time.

Multiplication takes five word times. During the first word time, the contents of the A register are shifted into the B register and used as the multiplier. At the same time, the multiplicand as specified by the address field of the instruction is shifted serially from memory into the M register. During the second, third, fourth, and part of the fifth word times, the double-length product is formed in the A and B registers. The sign of the B register is made to agree with the sign of the A register.

The non-restoring division process takes eight word times. [1] It uses the pair of signed numbers in the A and B registers as the double-length dividend. During the first word time, the divisor, as specified by the address field of the instruction, is shifted serially from memory into the M register. During the next six word times the quotient is formed in the B register. A residue is left in the A register. During the eighth word time the contents of the A and B registers are exchanged so that the quotient is available in the A register.

Input-Output Processing Units

The Input-Output Processing Units will be different for each particular application of the computer. A variety of digital inputs and outputs and analog-digital converters may be involved. However, the philosophy in MAGIC is to use as little special equipment as possible for the many functions which must be performed. Serial shift registers operating at one megacycle are used to process the data received at the interface. Many registers share the same adder and the registers themselves are time-shared, holding different functions during different modes of operation. One serial channel is provided to and from the memory and arithmetic unit via the A register. It is felt that this philosophy will lead to the maximum scope of application for MAGIC, since guidance system instruments and actuators are becoming increasingly digital in character.

The present machine includes input facilities for the following types of signals:

1) Phase-shifted square waves derived from synchro-resolvers for shaft-position encoding.

2) Pulses representing incremental changes in physical quantities.

3) Discrete levels indicating the status of various parts of the system.

4) Inputs from a separate console unit for ground operation and manual control.

MAGIC provides facilities for the following kinds of output signals:

1) Constant frequency pulses for incremental actuation of stepper motors.

2) Discrete levels to control the operation of other parts of the system.

3) Proportional analog voltages.

4) Outputs to a separate console for program control and monitoring.

Memory

Figure 4 shows a schematic representation of the memory system. Storage is provided by an array of 192 x 512 torroidal ferrite cores. Drive currents for these cores are steered through the appropriate X and Y lines by means of three 16 x 16 switch core matrices. Each 50 mil storage core has five wires through it; a read and a write wire for each of the X and Y selection directions, and a sense winding. Bits

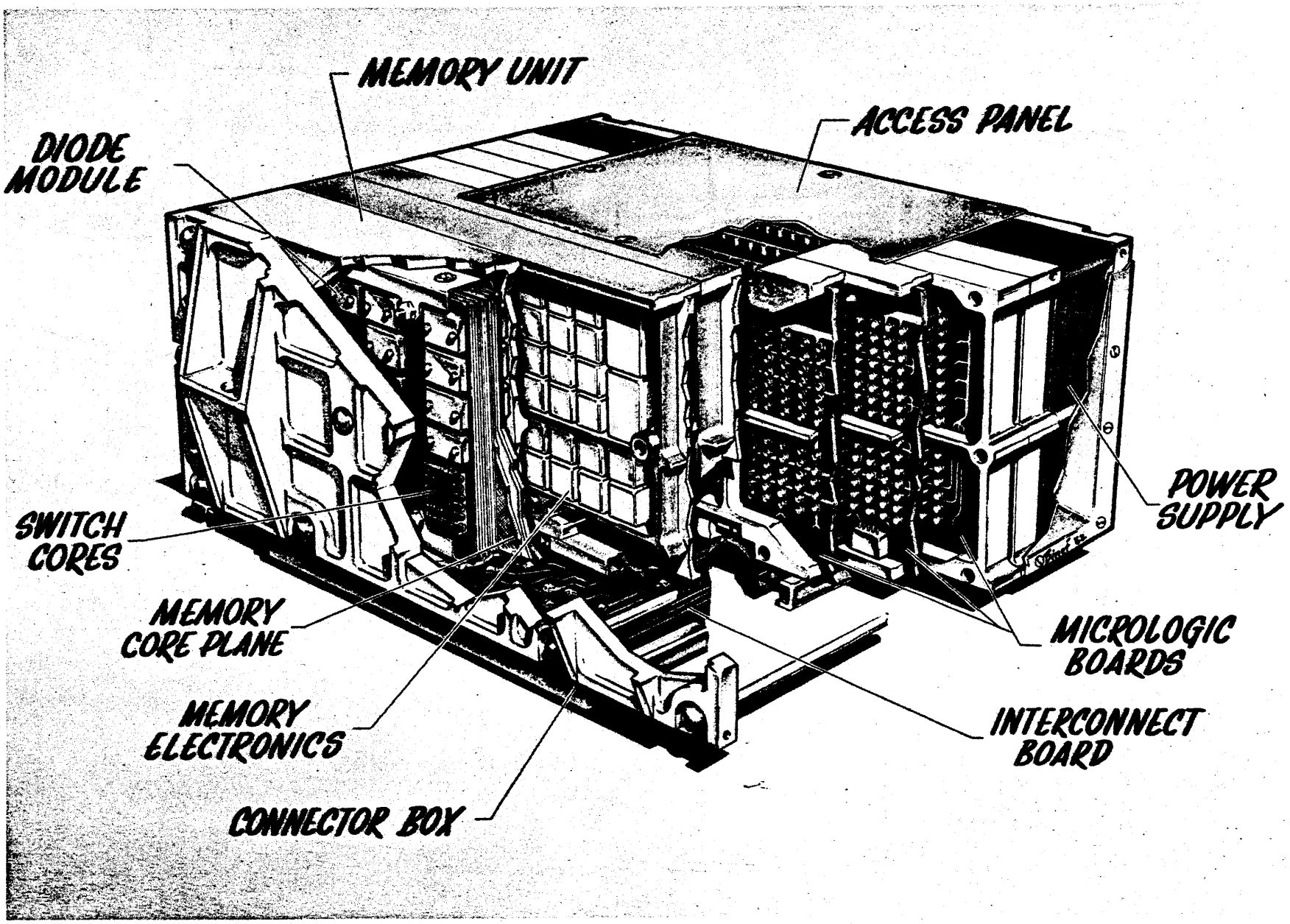


Figure 2. Artist's Cutaway of MAGIC

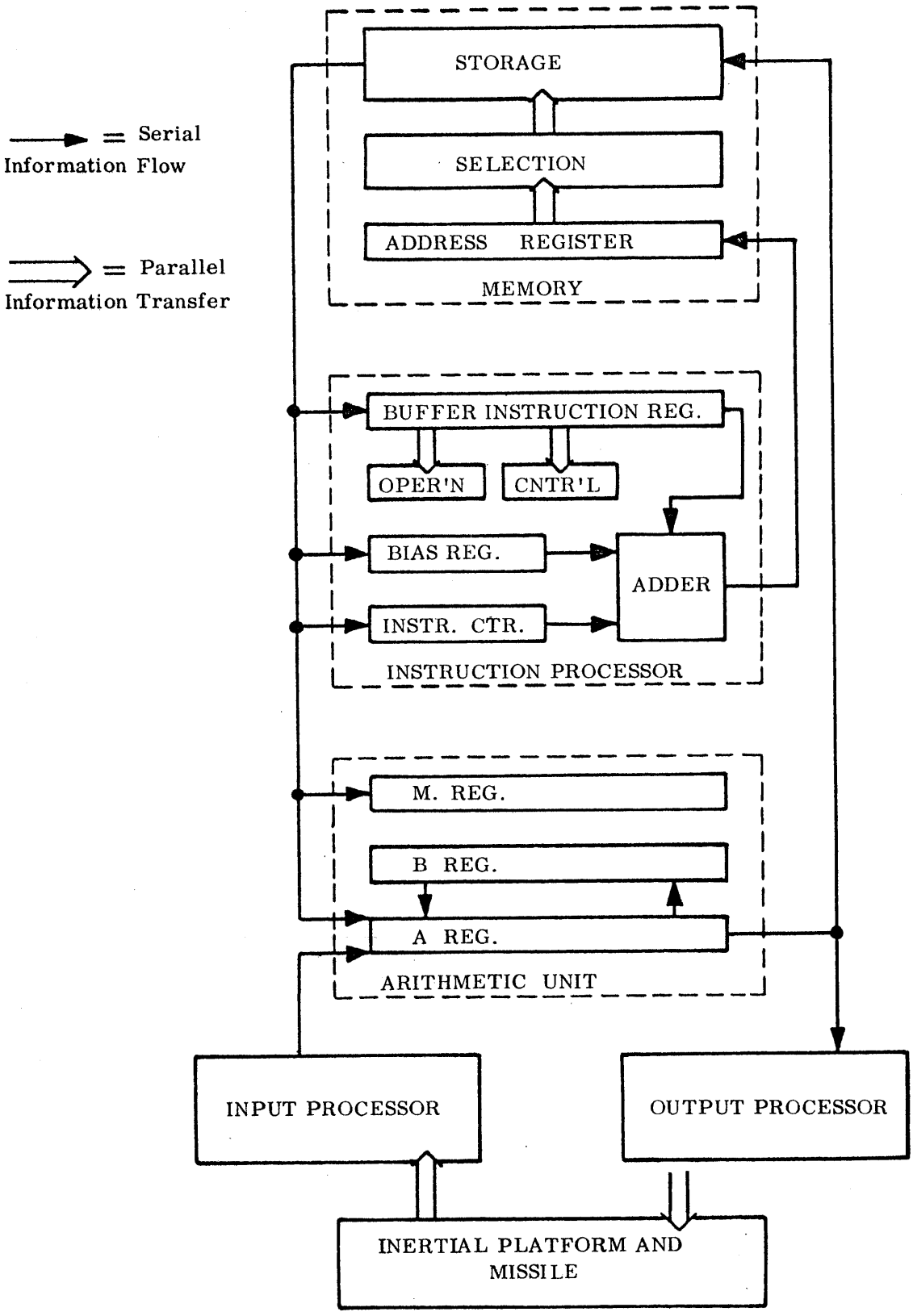


Figure 3. MAGIC Organization