NS11-04/34
INSTALLATION GUIDE

National Semiconductor
Memory Systems

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	APPROVED	DATE	DESCRIPTION	REV
		Sh Stern	6-23-78	PDD 2766	A

NS11-04/34
INSTALLATION GUIDE

REV																													
SHEET																													
REVISION STATUS OF SHEETS	REV																												
	SHEET																												

BY	DATE	TEST ENGR	DATE
CHK Sh Stern	6-23-78	DIR OF ENG	
PROD ENGR			8/7/78
PROJ ENGR		MANUF TEST	

TITLE NS11-04/34
INSTALLATION GUIDE

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara Calif. 95051

SIZE	DWG NO	REV
A	420103803	001

SCALE | SHEET 1 OF 13

I. GENERAL

The National Semiconductor Memory Systems Model NS 11-04/34 Memory Systems is designed to operate in Digital Equipment Corporations PDP 11/04* and PDP 11/34* Series Computers. The card is directly plug compatable into the following DEC backplanes:

a. DD11-DK (slots 3-8)
b. DD11-PK (slots 3-8)
c. DD11-CK (slots 2,3)

The NS 11-04/34 is completely compatable with the PDP 11/04/34 computers and all standard DEC peripheral devices. It can be utilized in both parity (M7850 installed) and non-parity systems. For installation in backplanes not listed above, the subject backplane connector pin assignments must be compatable with the NS 11-04/34 pin assignments as listed in table 1.

The memory is ready for installation upon receipt; however, the memory size and address switches and the option jumpers MUST be checked before the card is installed.

> **CAUTION**
>
> TURN OFF ALL SYSTEM POWER BEFORE INSERTING OR REMOVING A CARD.

II. OPTION JUMPER CONNECTIONS

The NS 11-04/34 options can be broken down as follows:

a. Modified or Standard UNIBUS compatability.
b. Parity or non-parity.
c. +15V or +20V input.

The configuration of each system is identified by a dash number. The dash number will be marked on each unit next to location D1 on side 1 (the component side). Table 2 identifies the option jumpers required for each dash number. Figure 1 locates each wire wrap jumper location. NOTE: There will be only ONE wire wrap connection per jumper location. Insure that the jumper location posts are not bent or touching.

*Trade mark of the Digital Equipment Corporation.

III. SWITCH SETTINGS

Switch S1 located at position E24 is an 8-position DIP switch used to set the I/O space and the initial address of the NS-11 Memory module. The three (3) low-order positions are used for I/O space, and the five (5) high-order positions are used for address selection.

A. I/O Space (S1-1, S1-2, S1-3). By convention, PDP-11 systems reserve the upper 4K addresses for I/O devices, thus limiting main memory to 28K of 32K possible addresses, or 124K of a possible 128K with memory management.

In some systems, fewer I/O device addresses are required and additional usable main memory is desired. The NS 11-04/34 permits memory expansion of 1K or 2K by setting S1-1, S1-2, and S1-3 according to the following table:

Reserved I/O Space	Usable Memory	S1 Switch Setting* 1	2	3
4K	28K/124K	Off	Off	On
2K	30K/126K	Off	On	On
1K	31K/127K	On	On	On

*Off = Open, On = Closed

B. Switch S2 located at D23 is used in conjunction with memory card depopulation. For a 32K card, switch positions 1-8 will be ON (CLOSED). For a 16K memory, S2-1 thru S2-4 will be ON, and S2-5 thru S2-8 will be OFF.

C. Initial Address (S1-4 thru S1-8). The NS 11-04/34 can be set to any starting address (in 4K increments) by setting switches 4,5,6,7 and 8 according to the following table:

Initial Address		Switch Setting				
32K Memory Card	16K Memory Card	8	7	6	5	4
0-32K	0-16K	Off	Off	Off	Off	Off
4-36	4-20	Off	Off	Off	Off	On
8-40	8-24	Off	Off	Off	On	Off
12-44	12-28	Off	Off	Off	On	On
16-48	16-32	Off	Off	On	Off	Off
20-52	20-36	Off	Off	On	Off	On
24-56	24-40	Off	Off	On	On	Off

Initial Address		Switch Setting				
32K Memory Card	16K Memory Card	8	7	6	5	4
28-60	28-44	Off	Off	On	On	On
32-64	32-48	Off	On	Off	Off	Off
36-68	36-52	Off	On	Off	Off	On
40-72	40-56	Off	On	Off	On	Off
44-76	44-60	Off	On	Off	On	On
48-80	48-64	Off	On	On	Off	Off
52-84	52-68	Off	On	On	Off	On
56-88	56-72	Off	On	On	On	Off
60-92	60-76	Off	On	On	On	On
64-96	64-80	On	Off	Off	Off	Off
68-100	68-84	On	Off	Off	Off	On
72-104	72-88	On	Off	Off	On	Off
76-108	76-92	On	Off	Off	On	On
80-112	80-96	On	Off	On	Off	Off
84-116	84-100	On	Off	On	Off	On
88-120	88-104	On	Off	On	On	Off
92-124	92-108	On	Off	On	On	On
96-124*	96-112	On	On	Off	Off	Off
100-124*	100-116	On	On	Off	Off	On
104-124*	104-120	On	On	Off	On	Off
108-124*	108-124	On	On	Off	On	On

*Not used

IV. INSTALLATION AND MAINTENANCE

The NS 11-04/34 was designed and built to best commercial workmanship standards and will withstand all normal shock and vibration encountered in shipping and installation. While not fragile, the unit should be handled with reasonable care to avoid damage.

A. Installation

1. Verify that the system is performing properly by running the appropriate memory diagnostics BEFORE any changes to the CPU configuration are made.

2. Carefully unpack and check container and unit for shipping damage. If damage has occurred, immediately notify the carrier and National Semiconductor, Computer Products Division.

3. Verify that jumper connections and switch settings are correct according to the Memory Configuration, starting address, and tables shown above.

4. TURN OFF CPU POWER.

5. Carefully slide the Memory System into the selected slot. Be sure that the component side faces the correct direction, that the board is aligned in the card guides. Insert and remove slowly so contact is not made with adjacent boards. When the memory has engaged the connectors, press firmly on the card and seat it by exerting equal pressure on the two ejectors.

6. Replace any cables, covers, panels, etc., which were moved during installation. Turn on CPU power.

7. Correct memory operation is verified by running one of the memory diagnostic routines. Instructions are contained in the processor reference manuals.

B. Maintenance

If operational difficulties are encountered, perform one or more of the following simplified procedures:

1. Check the memory installation. It must be installed facing the correct direction. Memory components are facing the same direction as the CPU board components.

2. Remove memory and visually inspect. Wipe edge connector with clean cloth.

3. Recheck the jumper connections and switch settings.

4. Reinstall memory, carefully seating module in the chassis connectors.

5. Using the peripheral equipment, interrogate various address areas of the memory. This will assure the module is fully operational.

6. When possible, switch with another module known to be operating properly. Use the results to determine whether the problem is in the module or in the processor interface.

The memory elements are all mounted in sockets, and the peripheral devices are in common use, so that repairs can be effected on-site, if desired. Tables IV and V identify the Memory Component locations as a function of Bit, Address, and Address drivers.

TABLE 1

NS 11-04/34 PIN ASSIGNMENTS

CONNECTOR A		
PIN	SIDE 1	SIDE 2
A	INIT L	
B		
C	DO0 L	OV
D	DO2 L	DO1 L
E	DO4 L	DO3 L
F	DO6 L	DO5 L
H	DO8 L	DO7 L
J	D10 L	DO9 L
K	D12 L	D11 L
L	D14 L	D13 L
M	PA L (1)	D15 L
N	PAR P1 (1)	PB L (1)
P	PAR P0 (1)	
R	+15V (1)	
S		
T	OV	
U		
V		+20V (1)

CONNECTOR B		
PIN	SIDE 1	SIDE 2
A		+5V
B		
C		OV
D		
E	SSYN INT L	PAR DET
F		DC LO
H	A01 L	A00 L
J	A03 L	A02 L
K	A05 L	A04 L
L	A07 L	A06 L
M	A09 L	A08 L
N	A11 L	A10 L
P	A13 L	A12 L
R	A15 L	A14 L
S	A17 L	A16 L
T	OV	C1 L
U	SSYN L	C0 L
V	MSYN L	

CONNECTORS C, D, E AND F

The following pins are tied together for GRANT CONTINUITY: CA1-CB1, DK2-DL2, DM2-DN2, DP2-DR2, DS2-DT2, and DR1-DS1.
Pin A2 is +5, C2 and T1 are OV on all connectors.
Pin CU1 is +15V (1)

(1) Jumper connection, See Table 2.

TABLE 2

NS 11-04/34 TABULATION TABLE

DASH NO.	UNIBUS TYPE	PARITY	BACKPLANE VOLTAGE	MEMORY SIZE	JUMPERS (1) INSTALLED
-037	MODIFIED	YES	+15V	16K x 18	A,B,C,D,E,H,J
-038	MODIFIED	NO	+15V	16K x 16	A,B,C,D,E,H,J
-039	MODIFIED	YES	+20V	16K x 18	A,B,C,G,H,J
-040	MODIFIED	NO	+20V	16K x 16	A,B,C,G,H,J
-041	STANDARD	YES	+15V	16K x 18	A,B,E,F,K,L
-042	STANDARD	NO	+15V	16K x 16	A,B,E,F
-043	MODIFIED	YES	+15V	32K x 18	A,B,C,D,E,H,J
-044	MODIFIED	NO	+15V	32K x 16	A,B,C,D,E,H,J
-045	MODIFIED	YES	+20V	32K x 18	A,B,C,G,H,J
-046	MODIFIED	NO	+20V	32K x 16	A,B,C,G,H,J
-047	STANDARD	YES	+15V	32K x 18	A,B,E,F,K,L
-048	STANDARD	NO	+15V	32K x 16	A,B,E,F
-049	MODIFIED	YES	+15V	16K x 18	A,C,D,E,H,J,P
-050	MODIFIED	NO	+15V	16K x 16	A,C,D,E,H,J,P
-051	MODIFIED	YES	+20V	16K x 18	A,C,G,H,J,P
-052	MODIFIED	NO	+20V	16K x 16	A,C,G,H,J,P
-053	STANDARD	YES	+15V	16K x 18	A,E,F,K,L,P
-054	STANDARD	NO	+15V	16K x 16	A,E,F,P
-055	MODIFIED	YES	+15V	32K x 18	A,C,D,E,H,J,P
-056	MODIFIED	NO	+15V	32K x 16	A,C,D,E,H,J,P
-057	MODIFIED	YES	+20V	32K x 18	A,C,G,H,J,P
-058	MODIFIED	NO	+20V	32K x 16	A,C,G,H,J,P
-059	STANDARD	YES	+15V	32K x 18	A,E,F,K,L,P
-060	STANDARD	NO	+15V	32K x 16	A,E,F,P

(1) Refer to Jumper Designator Chart (Table 3) and Jumper Connection Location Diagram (Figure 1).

TABLE 3

JUMPER DESIGNATION CHART

JUMPER (1)	DESIGNATION	FUNCTION
#19 to #20	A	+12 Reg. Out
#21 to #22	B	-5 Reg. Out
#3 to #4	C	-Parity Detect
#17 to #18	D	+15 in @ AR1
#13 to #14	E	+15 input to Regulators
#16 to #17	F	+15 in @ CU1
#14 to #15	G	+20 in @ AV2
#8 to #9	H	PO L
#11 to #12	J	P1 L
#7 to #8	K	PA L
#10 to #11	L	PB L
#2 to #6	P	OV

(1) See Figure 1 for Jumper Connection Locations.

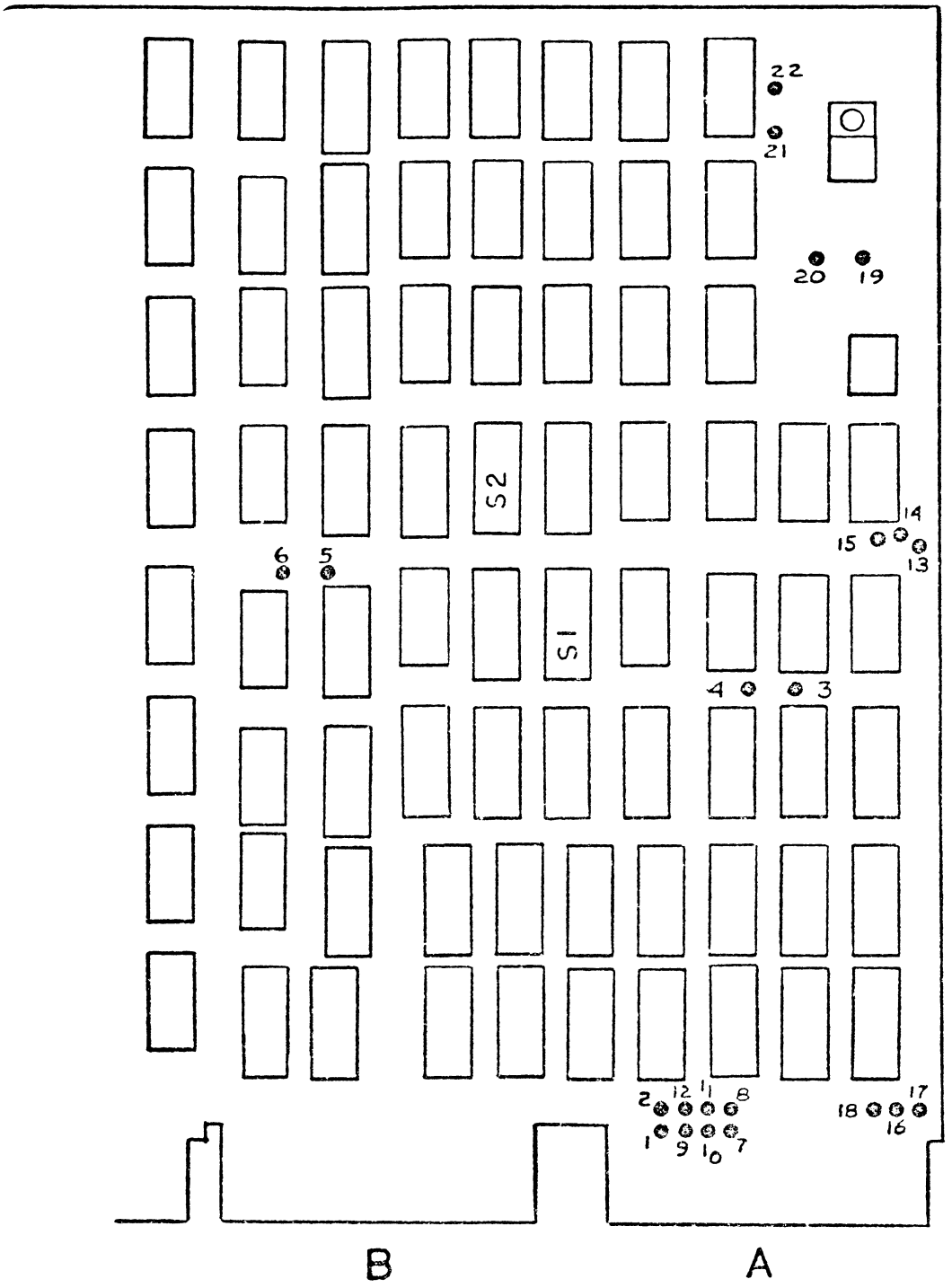


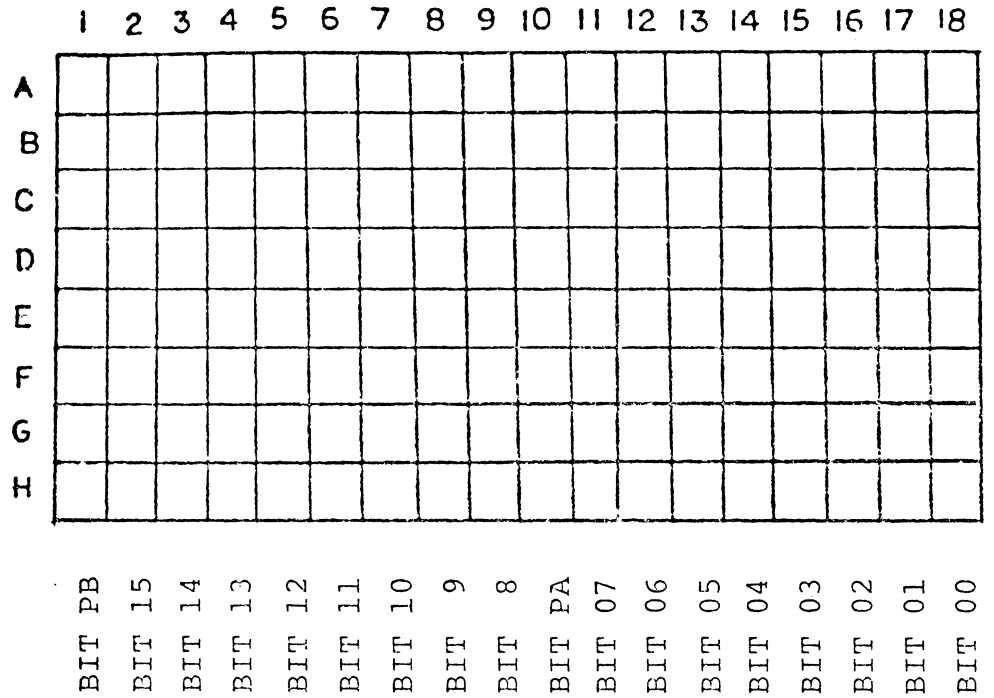
FIGURE 1

OPTION JUMPER CONNECTIONS

National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara Calif. 95051	SIZE A	DWG NO 420103803	REV
	SCALE	SHEET 10 OF 13	

TABLE IV

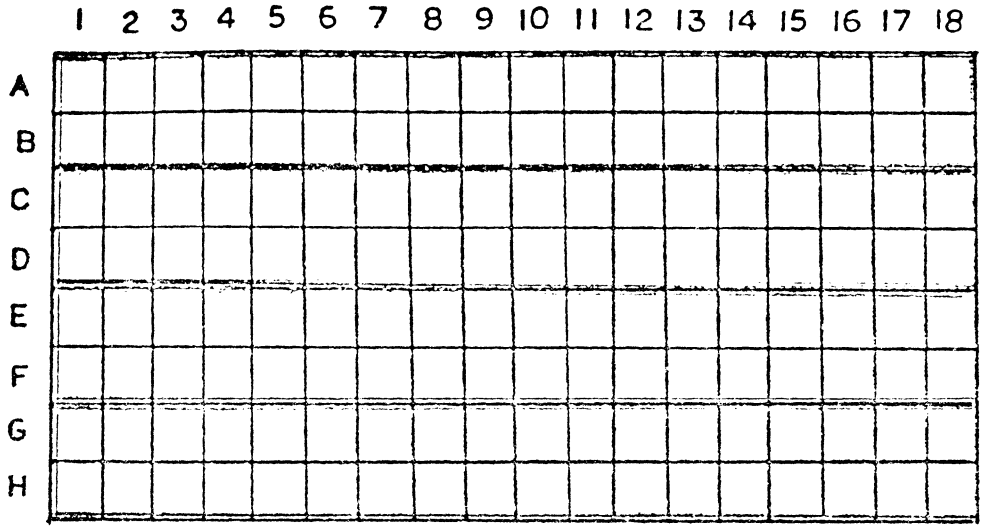
MEMORY COMPONENT BIT AND ROW ADDRESS LOCATOR



ROW	MEMORY SYSTEM ADDRESS RANGE
A	0-4K $(0 - 17777)_8$
B	4-8K $(20000 - 37777)_8$
C	8-12K $(40000 - 57777)_8$
D	12-16K $(60000 - 77777)_8$
E	16-20K $(100000 - 117777)_8$
F	20-24K $(120000 - 137777)_8$
G	24-28K $(140000 - 157777)_8$
H	28-32K $(160000 - 177777)_8$

TABLE V

MEMORY COMPONENT ADDRESS DRIVER LOCATOR



ADDRESS	ADDRESS DRIVER			
	ROW A,B	ROW C,D	ROW E,F	ROW G,H
A00	A19-6	C19-6	E19-6	G19-6
A01	B19-8	D19-8	F19-8	H19-8
A02	B19-10	D19-10	F19-10	H19-10
A03	A19-10	C19-10	E19-10	G19-10
A04	A19-8	C19-8	E19-8	G19-8
A05	B19-6	D19-6	F19-6	H19-6
A06	B19-4	D19-4	F19-4	H19-4
A07	B19-12	D19-12	F19-12	H19-12
A08	B19-2	D19-2	F19-2	H19-2
A09	A19-2	C19-2	E19-2	G19-2
A10	A19-12	C19-12	E19-12	G19-12
A11	A19-4	C19-4	E19-4	G19-4

TABLE VI

DECIMAL WORD TO OCTAL BYTE CONVERSION

DECIMAL WORD	OCTAL BYTE
4096 (4K)	0020000
8192 (8K)	0040000
12288 (12K)	0060000
16384 (16K)	0100000
20480 (20K)	0120000
24576 (24K)	0140000
28672 (28K)	0160000
32768 (32K)	0200000
36864 (36K)	0220000
40960 (40K)	0240000
45056 (44K)	0260000
49152 (48K)	0300000
53248 (52K)	0320000
57344 (56K)	0340000
61440 (60K)	0360000
65536 (64K)	0400000
69632 (68K)	0420000
73728 (72K)	0440000
77824 (76K)	0460000
81920 (80K)	0500000
86016 (84K)	0520000
90112 (88K)	0540000
94208 (92K)	0560000
98304 (96K)	0600000
102400 (100K)	0620000
106496 (104K)	0640000
110592 (108K)	0660000
114688 (112K)	0700000
118784 (116K)	0720000
122880 (120K)	0740000
126976 (124K)	0760000
131072 (128K)	1000000

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	10/5	PDD 1653	

FRONT

1	A	2	
BUSINITL	A	+5V	(4)
(4) INTR	B	0V	(4)
BUSD00L	C	0V	
BUSD02L	D	BUSD01L	
BUSD04L	E	BUSD03L	
BUSD06L	F	BUSD05L	
BUSD08L	H	BUSD07L	
BUSD10L	J	BUSD09L	
BUSD12L	K	BUSD11L	
BUSD14L	L	BUSD13L	
BUSDPAL	M	BUSD15L	
PARP1	N	BUSDPBL	
PARP0	P	BBSYL	
0V/+15V	R	SACKL	
(4) 0V/-15V	S	NPRL	(4)
0V	T	BR7L	
(4) NPG/+20V	U	BR6L	
DATIP CLR	V	+20V	

1	B	2	
BG6H	A	+5V	
(4) BG5H	B	0V	(4)
BR5L	C	0V	
0V/+5V	D	BR4L	(4)
SSYN INTL	E	PARDET	
(4) ACLOL	F	DCLO	
BUSA01L	H	BUSA00L	
BUSA03L	J	BUSA02L	
BUSA05L	K	BUSA04L	
BUSA07L	L	BUSA06L	
BUSA09L	M	BUSA08L	
BUSA11L	N	BUSA10L	
BUSA13L	P	BUSA12L	
BUSA15L	R	BUSA14L	
BUSA17L	S	BUSA16L	
0V	T	BUS C1L	
BUS SSYNL	U	BUS C0L	
BUS MSYNL	V	0V/-5V	(4)

1	C, D, E, F	2	
(5)	A	+5V	
	B	0V	
	C		
	D		
	E		
	F		
	H		
	J		
	K		
	L		
	M		
	N		(3)
	P		
	R		
(3)	S		
0V	T		
+15V	U		
	V		

(6)

TABULATION TABLE (10)

DASH NO.	PART NO.	SIZE	UNIBUS	VOLTAGE	PARITY	LOCATIONS NOT INST.	QTY	JUMPER INSTALLATIONS	SWITCH NO.	POSITION ON	POSITION OFF	CONT NO.
-037	870101870	16K X 18 (7)	MODIFIED	+15V	PARITY	E1 - E18 F1 - F18 G1 - G18 H1 - H18 FOR NON PARITY ADD A10, B10, C10, D10, A1, B1, C1, D1	7. 80 (NON PARITY)	E2-10, E3-4, E8-9, E11-12, E13-14, E16-17, E19-20, E21-22	1 THRU 8		X	PDD 1653
-038	870101870	16K X 16 (7)	BOTH	+15V	NON-PARITY			E13-14, E16-17, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-039	870101870	16K X 18 (7)	MODIFIED	+20V	PARITY			E2-10, E3-4, E8-9, E11-12, E13-14, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-040	870101870	16K X 16 (7)	MODIFIED	+20V	NON-PARITY			E14-15, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-041	870101870	16K X 18 (7)	STANDARD	+15V	PARITY			E1-2, E7-8, E10-11, E13-14, E16-17, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-042	870101870	16K X 18 (7)	STANDARD (NOT EXIST)	+20V	PARITY			E1-2, E7-8, E10-11, E14-15, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-043	870101870	32K X 18 (8)	MODIFIED	+15V	PARITY	FOR NON PARITY A10, B10, C10 D10, E10, F10 G10, H10 A1, B1, C1, D1 E1,F1,G1,H1	16.	E2-10, E3-4, E8-9, E11-12, E13-14, E16-17, E19-20, E21-22	1 THRU 8		X	PDD 1653
-044	870101870	32K X 16 (8)	BOTH	+15V	NON-PARITY			E13-14, E16-17, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-045	870101870	32K X 18 (8)	MODIFIED	+20V	PARITY			E2-10, E3-4, E8-9, E11-12, E13-14, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-046	870101870	32K X 16 (8)	MODIFIED	+20V	NON-PARITY			E14-15, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-047	870101870	32K X 18 (8)	STANDARD	+15V	PARITY			E1-2, E7-8, E10-11, E13-14, E16-17, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-048	870101870	32K X 18 (8)	STANDARD (NOT EXIST)	+20V	PARITY			E1-2, E7-8, E10-11, E14-15, E19-20, E21-22.	1 THRU 8		X	PDD 1653
-100	870101870	32K X 18 (8)	BASIC BOARD FOR TESTING PURPOSES					E2-10, E3-4, E8-9, E11-12, E13-14, E18-20, E15-22.	1 THRU 8		X	PDD 1653

CAUTION: DO NOT INSTALL JUMPERS FOR BOTH +15V AND +20V, AS THEY MAY DAMAGE LOWER SUPPLY.

ADDRESS SELECT AND I/O SPACE TABLE (8)

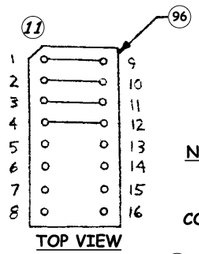
MEMORY BANK 32K SYS	MEMORY BANK 16K SYS	SWITCH 8	7	6	5	4
0-32 K	0-16 K	OFF	OFF	OFF	OFF	OFF
4-36	4-20	OFF	OFF	OFF	OFF	ON
8-40	8-24	OFF	OFF	OFF	ON	OFF
12-44	12-28	OFF	OFF	OFF	ON	ON
16-48	16-32	OFF	OFF	ON	OFF	OFF
20-52	20-36	OFF	OFF	ON	OFF	ON
24-56	24-40	OFF	OFF	ON	ON	OFF
28-60	28-44	OFF	OFF	ON	ON	ON
32-64	32-48	OFF	ON	OFF	OFF	OFF
36-68	36-52	OFF	ON	OFF	OFF	ON
40-72	40-56	OFF	ON	OFF	ON	OFF
44-76	44-60	OFF	ON	OFF	ON	ON
48-80	48-64	OFF	ON	ON	OFF	OFF
52-84	52-68	OFF	ON	ON	OFF	ON
56-88	56-72	OFF	ON	ON	ON	OFF
60-92	60-76	OFF	ON	ON	ON	ON
64-96	64-80	ON	OFF	OFF	OFF	OFF
68-100	68-84	ON	OFF	OFF	OFF	ON
72-104	72-88	ON	OFF	OFF	ON	OFF
76-108	76-92	ON	OFF	OFF	ON	ON
80-112	80-96	ON	OFF	ON	OFF	OFF
84-116	84-100	ON	OFF	ON	OFF	ON
88-120	88-104	ON	OFF	ON	ON	OFF
92-124	92-108	ON	OFF	ON	ON	ON
96-128	96-112	ON	ON	OFF	OFF	OFF
100-124*	100-116	ON	ON	OFF	OFF	ON
104-124*	104-120	ON	ON	OFF	ON	OFF
108-124*	108-124	ON	ON	OFF	ON	ON
112-124*	112-124	ON	ON	ON	OFF	OFF
116-124**	116-124**	ON	ON	ON	OFF	ON
120-124**	120-124**	ON	ON	ON	ON	OFF

	IOSPACE	SWITCH 1	2	3
WITH MEMORY MANAGEMENT	4K	OFF	OFF	ON
	2K	OFF	ON	ON
	1K	ON	ON	ON
WITHOUT MEMORY MANAGEMENT	4K	OFF	OFF	OFF
	2K	OFF	ON	OFF
	1K	ON	ON	OFF

(9)

** NOT USED WITH 32K UNIT
* NOT USED

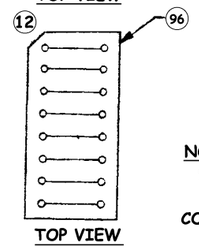
(11)



TOP VIEW

NOTE: INSTALL ITEM 95 AFTER WIRING INSTALL IN 16K CONFIGURATION ONLY

(12)



TOP VIEW

NOTE: INSTALL ITEM 95 AFTER WIRING INSTALL IN 32K CONFIGURATION ONLY

(13) SWITCHES ARE ALWAYS SET IN OFF POSITION FOR SHIPPING. IF ANY OF THE FOLLOWING THREE CONFIGURATIONS ARE REQUESTED, CONFIGURATION MANAGEMENT MUST EB NOTIFIED:
1. ADDRESS RANGE OF MEMORY
2. MEMORY MANAGEMENT PRESENT (NOT PRESENT)
3. RESERVED I/O SPACE

(12) SEE DETAIL

(11) SEE DETAIL

(10) JUMPERS ARE SHOWN AFTER TESTING.

(9) SWITCH 3: MUST BE ON WHEN MEMORY MANAGEMENT IS INBSTALLED; MUST BE OFF WHEN MEMORY MANAGEMENT IS NOT INSTALLED.

(8) REFER TO ADDRESS SELECT TABLE.

7

(6) REFER TO TABULATION TABLE FOR JUMPER INFORMATION.

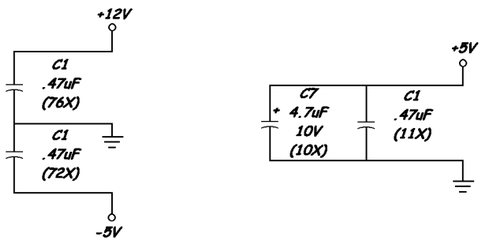
(5) ON CONNECTOR "C" ONLY PIN A IS CONENCTED TO B ON FRONT SIDE.

(4) SIGNALS ASSIGNED IN UNIBUS BUT ARE NOT USED IN THIS MEMORY.

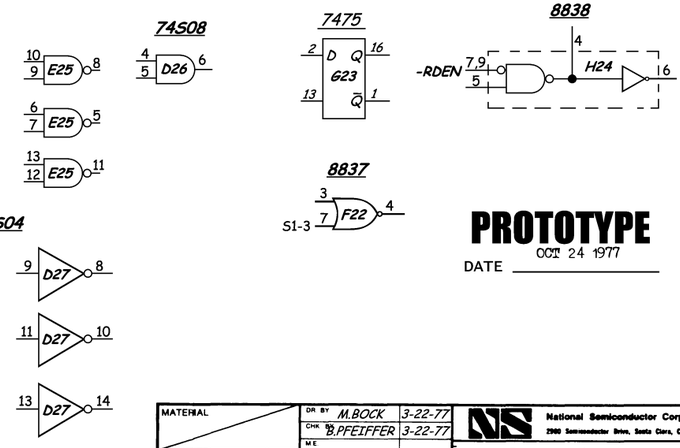
(3) ON CONNECTOR "D" ONLY PIN K IS CONNECTED TO L, M TO N, P TO R, AND S TO T ON BACKSIDE (2); R TO S ON FRONT SIDE (1).

2. ALL 14 PIN IC'S HAVE PIN 7 AT GROUND AND PIN 14 AT +5V, ALL 16 PIN IC'S HAVE PIN 8 AT GROUND AND PIN 16 AT +5V, EXCEPT: 7475 - PIN 12 GROUND, PIN 5 +5V.

1. ALL RESTISTANCES ARE IN OHMS, CAPACITANCE IN MICROFARADS.
NOTES: (UNLESS OTHERWISE SPECIFIED.)



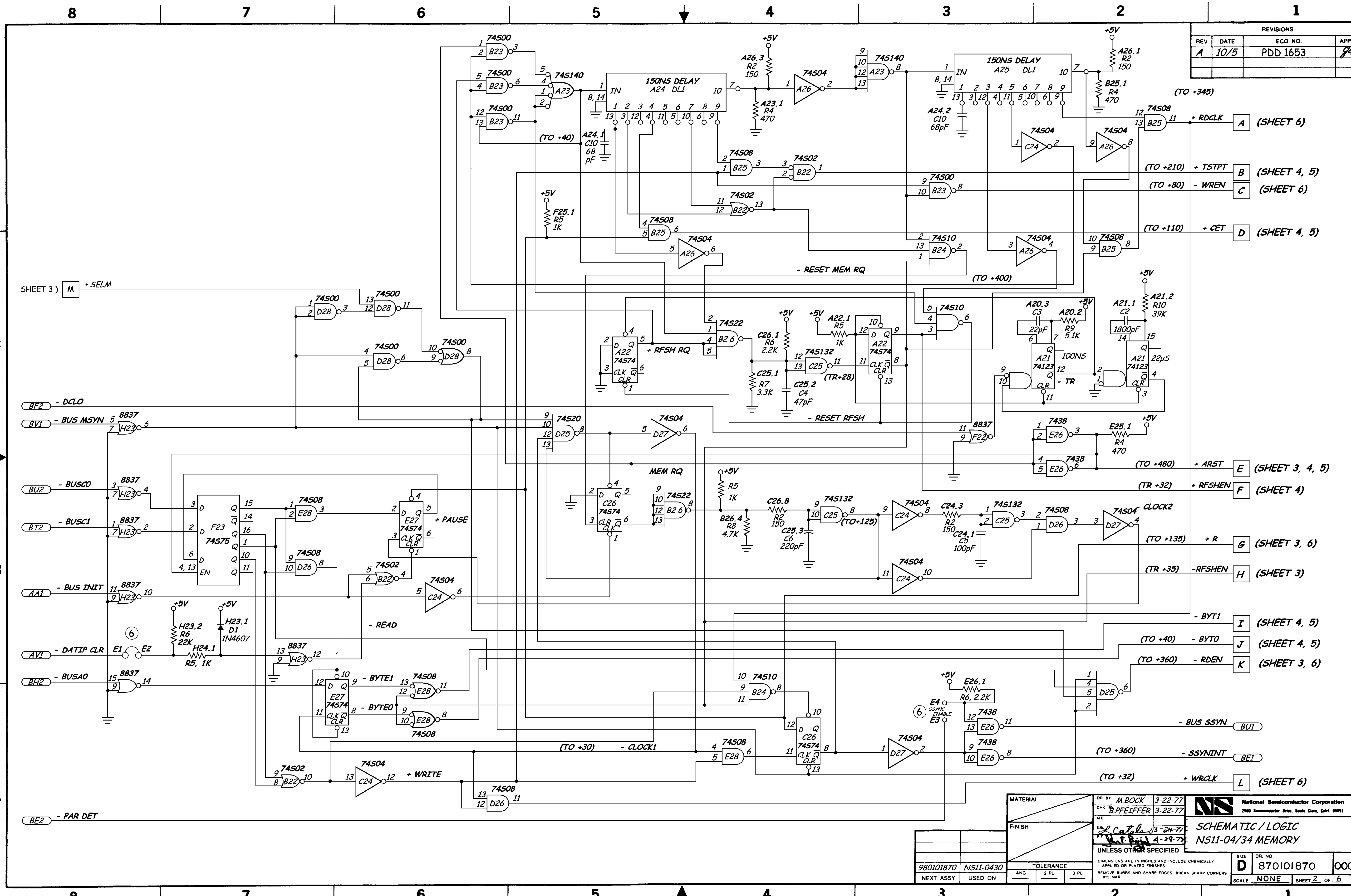
NOT USED

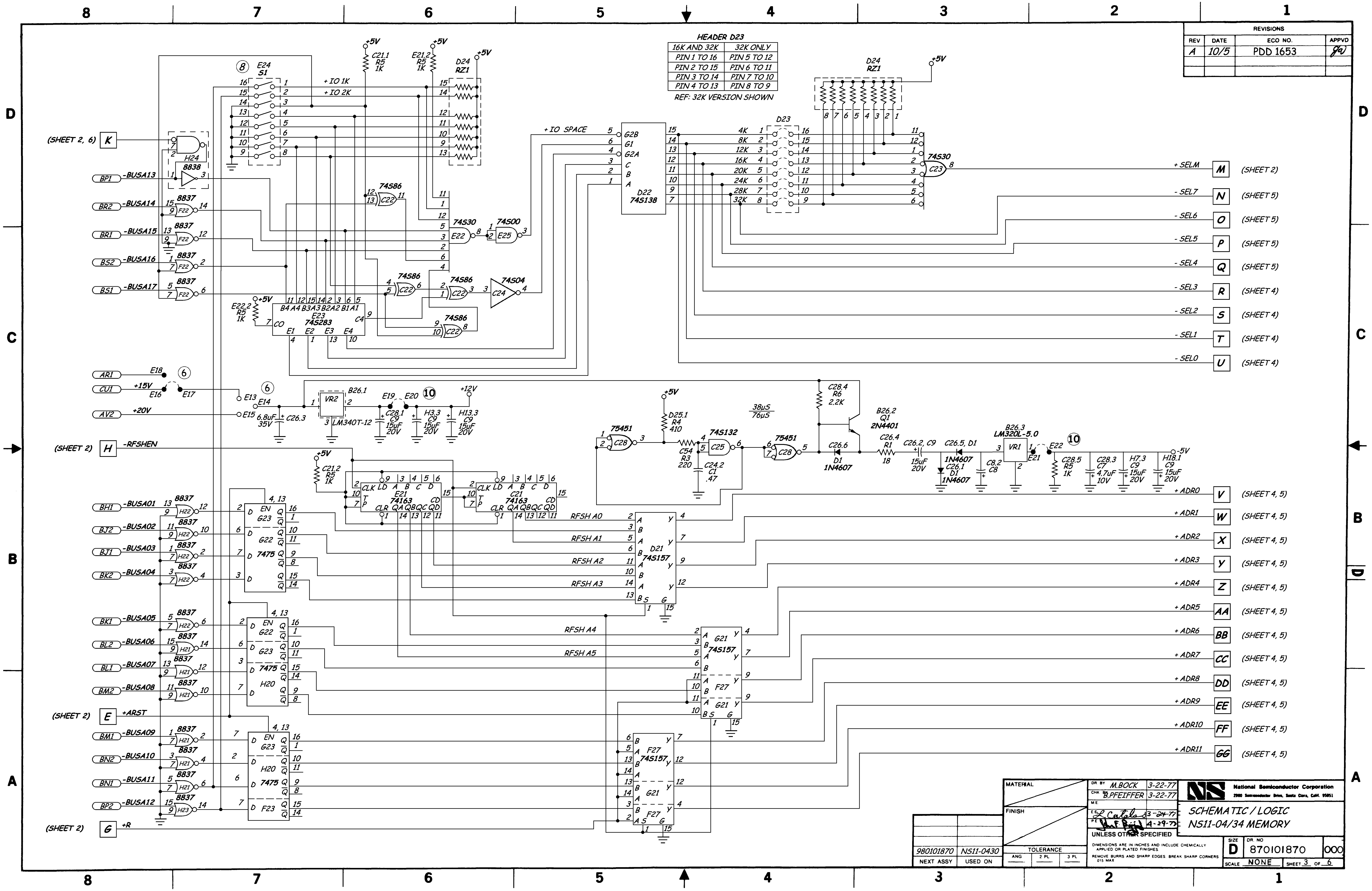


PROTOTYPE
DATE OCT 24 1977

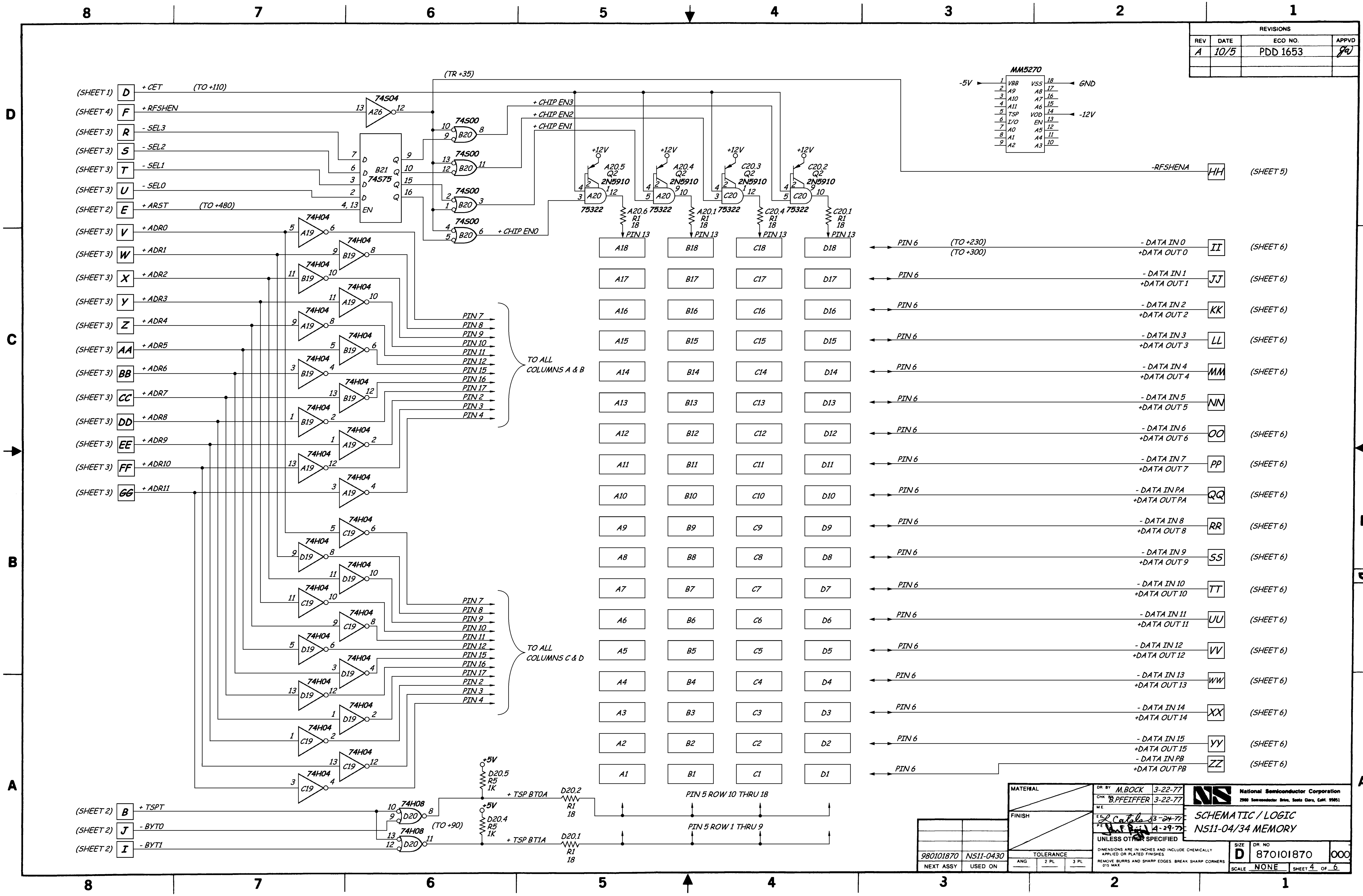
MATERIAL	DR BY M.BOCK 3-22-77	National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH	CHK B.PFEIFFER 3-22-77	SCHEMATIC / LOGIC
	ME	N511-04/34 MEMORY
	ENG [illegible] 3-24-77	
	PROJ [illegible] 4-29-77	
980101870 N511-0430	UNLESS OTHERWISE SPECIFIED	SIZE D DR NO 870101870 000
NEXT ASSY USED ON	TOLERANCE ANG 2 PL 3 PL	SCALE NONE SHEET 1 OF 6

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX

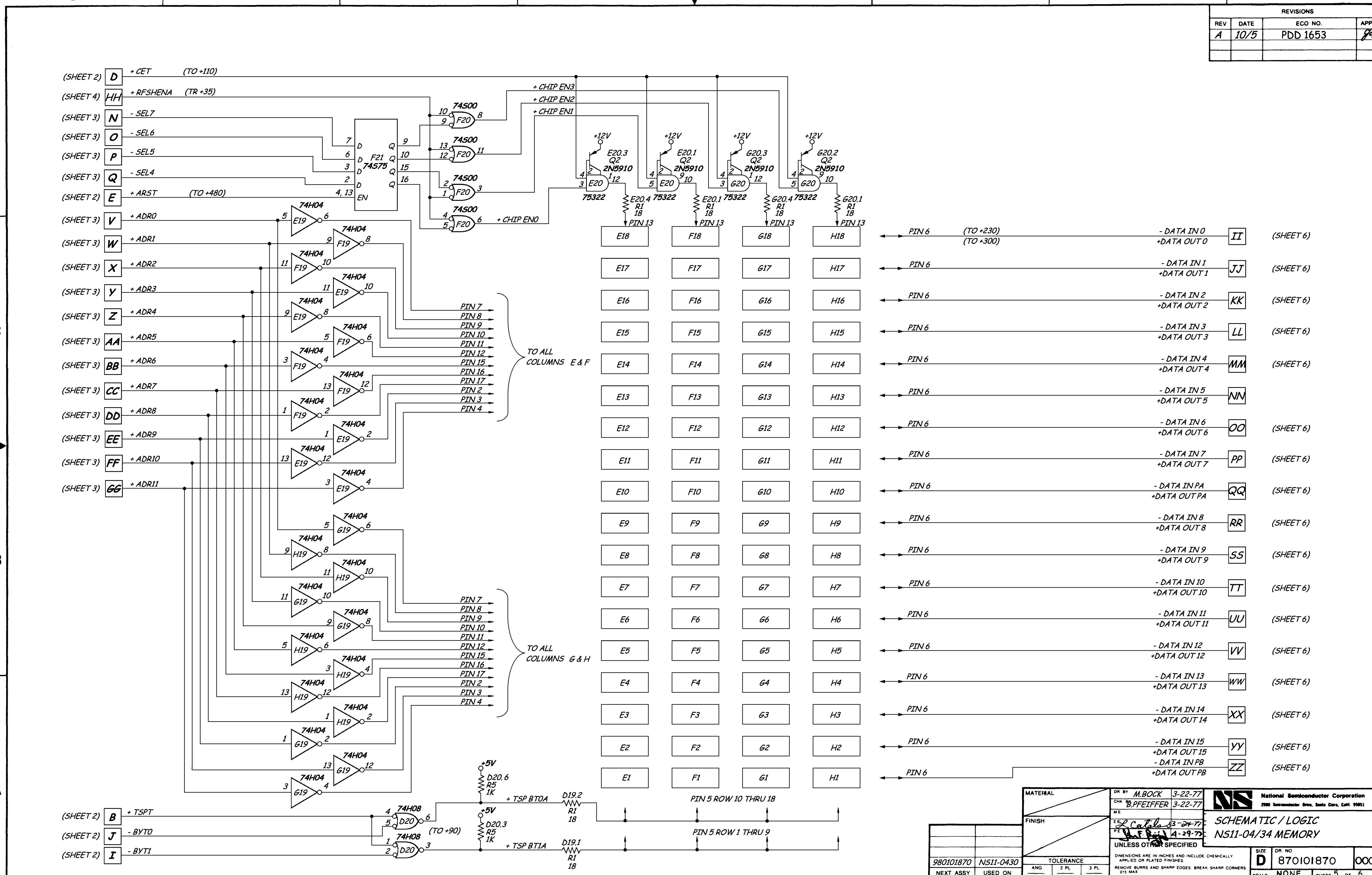

REVISIONS
REV | DATE | ECO NO. | APPVD
A | 10/5 | PDD 1653
150NS DELAY A24 DL1
150NS DELAY A25 DL1
- RESET MEM RQ
+ RFSH RQ
- RESET RFSH
MEM RQ
+ PAUSE
- READ
- BYTE1
- BYTE0
+ WRITE
- CLOCK1
CLOCK2
SHEET 3) M + SELM
BF2 - DCLO
BV1 - BUS MSYN
BU2 - BUSC0
BT2 - BUSC1
AA1 - BUS INIT
AV1 - DATIP CLR
BH2 - BUSA0
BE2 - PAR DET
(TO +345) + RDCLK A (SHEET 6)
(TO +210) + TSTPT B (SHEET 4, 5)
(TO +80) - WREN C (SHEET 6)
(TO +110) + CET D (SHEET 4, 5)
(TO +480) + ARST E (SHEET 3, 4, 5)
(TR +32) + RFSHEN F (SHEET 4)
(TO +135) + R G (SHEET 3, 6)
(TR +35) -RFSHEN H (SHEET 3)
- BYT1 I (SHEET 4, 5)
(TO +40) - BYT0 J (SHEET 4, 5)
(TO +360) - RDEN K (SHEET 3, 6)
- BUS SSYN BU1
(TO +360) - SSYNINT BE1
(TO +32) + WRCLK L (SHEET 6)
MATERIAL
FINISH
DR BY M.BOCK 3-22-77
CHK B.PFEIFFER 3-22-77
National Semiconductor Corporation
SCHEMATIC / LOGIC
NS11-04/34 MEMORY
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX
TOLERANCE
980101870 NS11-0430
NEXT ASSY USED ON
SIZE D DR NO 870101870 000
SCALE NONE SHEET 2 OF 6



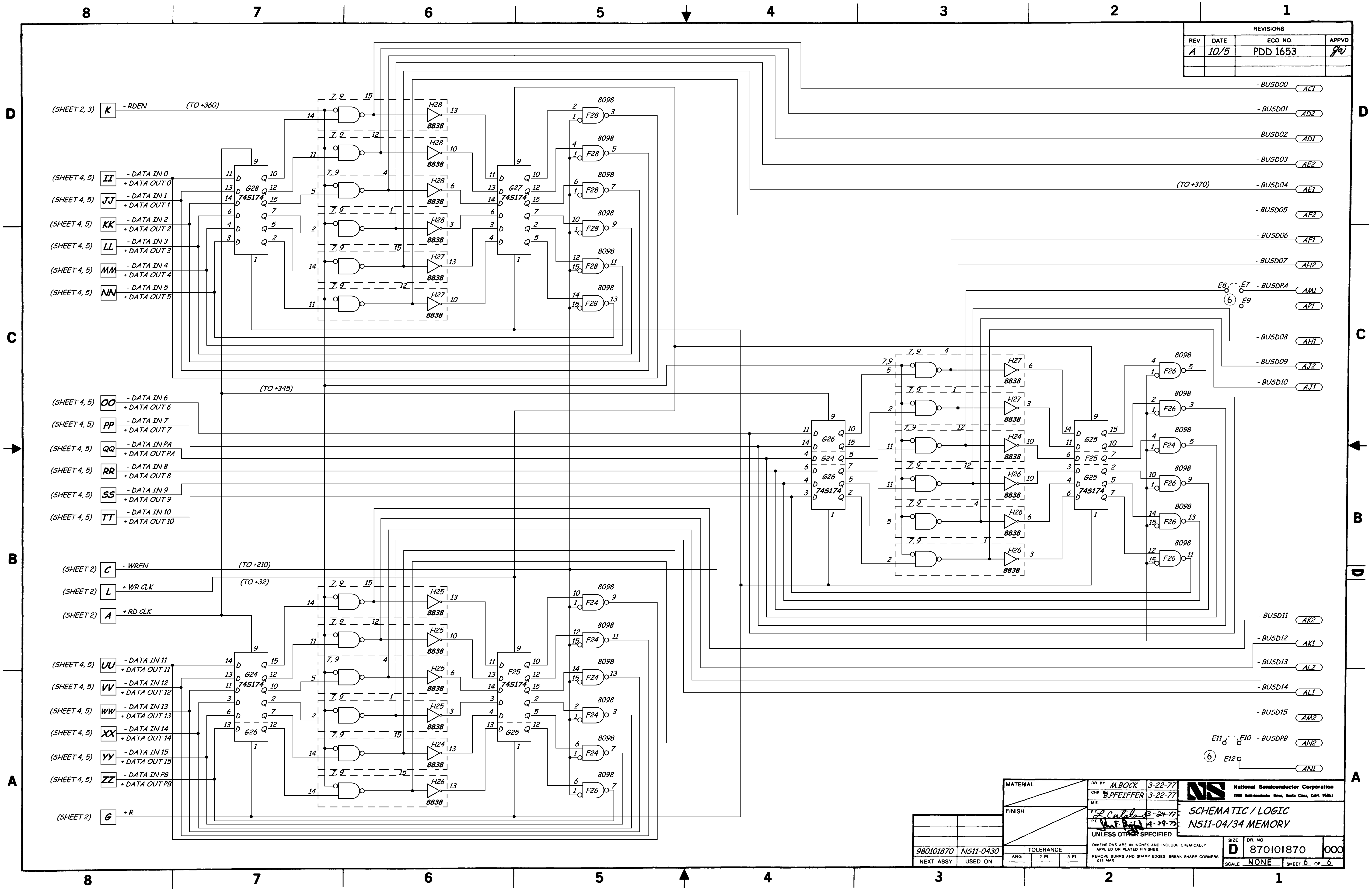
REVISIONS
REV | DATE | ECO NO. | APPVD
A | 10/5 | PDD 1653
HEADER D23
16K AND 32K | 32K ONLY
PIN 1 TO 16 | PIN 5 TO 12
PIN 2 TO 15 | PIN 6 TO 11
PIN 3 TO 14 | PIN 7 TO 10
PIN 4 TO 13 | PIN 8 TO 9
REF: 32K VERSION SHOWN
(SHEET 2, 6) K
BP1 -BUSA13
BR2 -BUSA14
BR1 -BUSA15
BS2 -BUSA16
BS1 -BUSA17
E24 S1
+IO 1K
+IO 2K
D24 RZ1
74S86
74S30
74S00
74S138
D22
+IO SPACE
74S283
E23
74S04
D23
4K 8K 12K 16K 20K 24K 28K 32K
+SELM M (SHEET 2)
-SEL7 N (SHEET 5)
-SEL6 O (SHEET 5)
-SEL5 P (SHEET 5)
-SEL4 Q (SHEET 5)
-SEL3 R (SHEET 4)
-SEL2 S (SHEET 4)
-SEL1 T (SHEET 4)
-SEL0 U (SHEET 4)
AR1 CU1 AV2
+15V +20V +12V
VR2 LM340T-12
(SHEET 2) H -RFSHEN
75451 74S132
38uS 76uS
Q1 2N4401
D1 1N4607
VR1 LM320L-5.0
-5V
74163 E21 C21
74S157 D21 G21 F27
7475 G23 G22 H20 F23
RFSH A0 RFSH A1 RFSH A2 RFSH A3 RFSH A4 RFSH A5
BH1 -BUSA01
BJ2 -BUSA02
BJ1 -BUSA03
BK2 -BUSA04
BK1 -BUSA05
BL2 -BUSA06
BL1 -BUSA07
BM2 -BUSA08
(SHEET 2) E +ARST
BM1 -BUSA09
BN2 -BUSA10
BN1 -BUSA11
BP2 -BUSA12
(SHEET 2) G +R
8837
+ADR0 V (SHEET 4, 5)
+ADR1 W (SHEET 4, 5)
+ADR2 X (SHEET 4, 5)
+ADR3 Y (SHEET 4, 5)
+ADR4 Z (SHEET 4, 5)
+ADR5 AA (SHEET 4, 5)
+ADR6 BB (SHEET 4, 5)
+ADR7 CC (SHEET 4, 5)
+ADR8 DD (SHEET 4, 5)
+ADR9 EE (SHEET 4, 5)
+ADR10 FF (SHEET 4, 5)
+ADR11 GG (SHEET 4, 5)
980101870 | NS11-0430
NEXT ASSY | USED ON
MATERIAL
FINISH
TOLERANCE
DR BY M.BOCK 3-22-77
CHK B.PFEIFFER 3-22-77
UNLESS OTHER SPECIFIED
National Semiconductor Corporation
SCHEMATIC / LOGIC
NS11-04/34 MEMORY
SIZE D DR NO 870101870 000
SCALE NONE SHEET 3 OF 6



REVISIONS
REV A | DATE 10/5 | ECO NO. PDD 1653
MM5270
-5V
GND
-12V
(SHEET 1) D +CET (TO +110)
(SHEET 4) F +RFSHEN
(SHEET 3) R -SEL3
(SHEET 3) S -SEL2
(SHEET 3) T -SEL1
(SHEET 3) U -SEL0
(SHEET 2) E +ARST (TO +480)
(TR +35)
74S04 A26
74S00 B20
74S75 B21
+CHIP EN3
+CHIP EN2
+CHIP EN1
+CHIP EN0
+12V
A20.5 Q2 2N5910
A20.4 Q2 2N5910
C20.3 Q2 2N5910
C20.2 Q2 2N5910
75322
A20.6 R1 18
A20.1 R1 18
C20.4 R1 18
C20.1 R1 18
PIN 13
-RFSHENA HH (SHEET 5)
(SHEET 3) V +ADR0
(SHEET 3) W +ADR1
(SHEET 3) X +ADR2
(SHEET 3) Y +ADR3
(SHEET 3) Z +ADR4
(SHEET 3) AA +ADR5
(SHEET 3) BB +ADR6
(SHEET 3) CC +ADR7
(SHEET 3) DD +ADR8
(SHEET 3) EE +ADR9
(SHEET 3) FF +ADR10
(SHEET 3) GG +ADR11
74H04
TO ALL COLUMNS A & B
TO ALL COLUMNS C & D
PIN 7 PIN 8 PIN 9 PIN 10 PIN 11 PIN 12 PIN 15 PIN 16 PIN 17 PIN 2 PIN 3 PIN 4
PIN 6 (TO +230) (TO +300)
-DATA IN 0 +DATA OUT 0 II (SHEET 6)
-DATA IN 1 +DATA OUT 1 JJ (SHEET 6)
-DATA IN 2 +DATA OUT 2 KK (SHEET 6)
-DATA IN 3 +DATA OUT 3 LL (SHEET 6)
-DATA IN 4 +DATA OUT 4 MM (SHEET 6)
-DATA IN 5 +DATA OUT 5 NN
-DATA IN 6 +DATA OUT 6 OO (SHEET 6)
-DATA IN 7 +DATA OUT 7 PP (SHEET 6)
-DATA IN PA +DATA OUT PA QQ (SHEET 6)
-DATA IN 8 +DATA OUT 8 RR (SHEET 6)
-DATA IN 9 +DATA OUT 9 SS (SHEET 6)
-DATA IN 10 +DATA OUT 10 TT (SHEET 6)
-DATA IN 11 +DATA OUT 11 UU (SHEET 6)
-DATA IN 12 +DATA OUT 12 VV (SHEET 6)
-DATA IN 13 +DATA OUT 13 WW (SHEET 6)
-DATA IN 14 +DATA OUT 14 XX (SHEET 6)
-DATA IN 15 +DATA OUT 15 YY (SHEET 6)
-DATA IN PB +DATA OUT PB ZZ (SHEET 6)
(SHEET 2) B +TSPT
(SHEET 2) J -BYT0
(SHEET 2) I -BYT1
74H08 D20
(TO +90)
+5V D20.5 R5 1K
+5V D20.4 R5 1K
+TSP BT0A D20.2 R1 18
+TSP BT1A D20.1 R1 18
PIN 5 ROW 10 THRU 18
PIN 5 ROW 1 THRU 9
MATERIAL
FINISH
TOLERANCE
980101870 | N511-0430
NEXT ASSY | USED ON
DR BY M.BOCK 3-22-77
CHK B.PFEIFFER 3-22-77
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051
SCHEMATIC / LOGIC
NS11-04/34 MEMORY
UNLESS OTHERWISE SPECIFIED
SIZE D DR NO 870101870
SCALE NONE SHEET 4 OF 6



REVISIONS
REV | DATE | ECO NO. | APPVD
A | 10/5 | PDD 1653
(SHEET 2) D +CET (TO +110)
(SHEET 4) HH +RFSHENA (TR +35)
(SHEET 3) N -SEL7
(SHEET 3) O -SEL6
(SHEET 3) P -SEL5
(SHEET 3) Q -SEL4
(SHEET 2) E +ARST (TO +480)
(SHEET 3) V +ADR0
(SHEET 3) W +ADR1
(SHEET 3) X +ADR2
(SHEET 3) Y +ADR3
(SHEET 3) Z +ADR4
(SHEET 3) AA +ADR5
(SHEET 3) BB +ADR6
(SHEET 3) CC +ADR7
(SHEET 3) DD +ADR8
(SHEET 3) EE +ADR9
(SHEET 3) FF +ADR10
(SHEET 3) GG +ADR11
F21 74S75
74S00
+CHIP EN3
+CHIP EN2
+CHIP EN1
+CHIP EN0
+12V
Q2 2N5910
75322
R1 18
PIN 13
74H04
TO ALL COLUMNS E & F
TO ALL COLUMNS G & H
PIN 6 (TO +230) (TO +300)
-DATA IN 0 +DATA OUT 0 II (SHEET 6)
-DATA IN 1 +DATA OUT 1 JJ (SHEET 6)
-DATA IN 2 +DATA OUT 2 KK (SHEET 6)
-DATA IN 3 +DATA OUT 3 LL (SHEET 6)
-DATA IN 4 +DATA OUT 4 MM (SHEET 6)
-DATA IN 5 +DATA OUT 5 NN
-DATA IN 6 +DATA OUT 6 OO (SHEET 6)
-DATA IN 7 +DATA OUT 7 PP (SHEET 6)
-DATA IN PA +DATA OUT PA QQ (SHEET 6)
-DATA IN 8 +DATA OUT 8 RR (SHEET 6)
-DATA IN 9 +DATA OUT 9 SS (SHEET 6)
-DATA IN 10 +DATA OUT 10 TT (SHEET 6)
-DATA IN 11 +DATA OUT 11 UU (SHEET 6)
-DATA IN 12 +DATA OUT 12 VV (SHEET 6)
-DATA IN 13 +DATA OUT 13 WW (SHEET 6)
-DATA IN 14 +DATA OUT 14 XX (SHEET 6)
-DATA IN 15 +DATA OUT 15 YY (SHEET 6)
-DATA IN PB +DATA OUT PB ZZ (SHEET 6)
(SHEET 2) B +TSPT
(SHEET 2) J -BYT0
(SHEET 2) I -BYT1
74H08 D20 (TO +90)
+5V D20.6 R5 1K
+5V D20.3 R5 1K
+TSP BT0A D19.2 R1 18
+TSP BT1A D19.1 R1 18
PIN 5 ROW 10 THRU 18
PIN 5 ROW 1 THRU 9
980101870 NS11-0430
NEXT ASSY USED ON
MATERIAL
FINISH
TOLERANCE
DR BY M.BOCK 3-22-77
CHK B.PFEIFFER 3-22-77
National Semiconductor Corporation
SCHEMATIC / LOGIC
NS11-04/34 MEMORY
UNLESS OTHERWISE SPECIFIED
SIZE D DR NO 870101870 000
SCALE NONE SHEET 5 OF 6



REVISIONS
REV | DATE | ECO NO. | APPVD
A | 10/5 | PDD 1653
(SHEET 2, 3) K - RDEN (TO +360)
(SHEET 4, 5) II - DATA IN 0 + DATA OUT 0
(SHEET 4, 5) JJ - DATA IN 1 + DATA OUT 1
(SHEET 4, 5) KK - DATA IN 2 + DATA OUT 2
(SHEET 4, 5) LL - DATA IN 3 + DATA OUT 3
(SHEET 4, 5) MM - DATA IN 4 + DATA OUT 4
(SHEET 4, 5) NN - DATA IN 5 + DATA OUT 5
(TO +345)
(SHEET 4, 5) OO - DATA IN 6 + DATA OUT 6
(SHEET 4, 5) PP - DATA IN 7 + DATA OUT 7
(SHEET 4, 5) QQ - DATA IN PA + DATA OUT PA
(SHEET 4, 5) RR - DATA IN 8 + DATA OUT 8
(SHEET 4, 5) SS - DATA IN 9 + DATA OUT 9
(SHEET 4, 5) TT - DATA IN 10 + DATA OUT 10
(SHEET 2) C - WREN (TO +210)
(SHEET 2) L + WR CLK (TO +32)
(SHEET 2) A + RD CLK
(SHEET 4, 5) UU - DATA IN 11 + DATA OUT 11
(SHEET 4, 5) VV - DATA IN 12 + DATA OUT 12
(SHEET 4, 5) WW - DATA IN 13 + DATA OUT 13
(SHEET 4, 5) XX - DATA IN 14 + DATA OUT 14
(SHEET 4, 5) YY - DATA IN 15 + DATA OUT 15
(SHEET 4, 5) ZZ - DATA IN PB + DATA OUT PB
(SHEET 2) G + R
G28 74S174
G27 74S174
G26 G24 G26 74S174
G25 F25 G25 74S174
G24 74S174 G26
F25 74S174 G25
8838
8098
- BUSD00 AC1
- BUSD01 AD2
- BUSD02 AD1
- BUSD03 AE2
(TO +370) - BUSD04 AE1
- BUSD05 AF2
- BUSD06 AF1
- BUSD07 AH2
E8 E7 - BUSDPA AM1
6 E9 AP1
- BUSD08 AH1
- BUSD09 AJ2
- BUSD10 AJ1
- BUSD11 AK2
- BUSD12 AK1
- BUSD13 AL2
- BUSD14 AL1
- BUSD15 AM2
E11 E10 - BUSDPB AN2
6 E12 AN1
MATERIAL
FINISH
DR BY M.BOCK 3-22-77
CHK B.PFEIFFER 3-22-77
3-24-77
4-29-77
UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX
TOLERANCE ANG 2 PL 3 PL
980101870 NS11-0430
NEXT ASSY USED ON
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051
SCHEMATIC / LOGIC
NS11-04/34 MEMORY
SIZE D DR NO 870101870 000
SCALE NONE SHEET 6 OF 6