

# MEMOREX

**677-01 DEC and 677-51 DEC  
Disc Storage Drives  
Technical Manual**

677-01/51.20-01  
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# SECTION 1 GENERAL INFORMATION

## 1.1 INTRODUCTION

Memorex 677 Series Disc Storage Drives are high-capacity, direct-access data storage devices featuring fast access and simplicity in design and packaging, proven to provide high reliability and ease of maintenance. Particular 677 Series drives are customized to fill the needs of original equipment manufacturers. Two such drives, supplied to Digital Equipment Corporation (DEC), are addressed in this manual. They are:

### 1.1.1 Product Definition

The 677-51 DEC and 677-01 DEC are derivatives of the 670 and 675, Memorex's third and fourth generation drives, respectively. Major components in either DEC drive are the same as those in the 670, with refinements as incorporated since the first 670 was delivered in October of 1972. Components in the 677-01 DEC drive which are sensitive to a doubling of data capacity to 200 megabytes are the same as those in the 675, with

<u>Memorex Designation</u>	<u>DEC Designation</u>	<u>Approximate Data Capacity</u>	<u>Average Access Time</u>
• 677-01 DEC Disc Storage Drive	RP06 Disc Pack Drive	200 megabytes	28.5 msec
• 677-51 DEC Disc Storage Drive	RP05 Disc Pack Drive	100 megabytes	28.5 msec

The two drives above are packaged as one spindle per drive. The data storage media used is the 200-megabyte Memorex Mark XI Disc Pack (equivalent to IBM 336-11) or the 100-megabyte Memorex Mark X Disc Pack (equivalent to IBM 3336). Except for DEC logo identifications, the two drives above look alike (Figure 1-1).

Each drive is supplied in one of two power configurations. Model A configurations (677-01A DEC and 677-51A DEC) operate from domestic power sources. Model B configurations operate from other power sources. Power conversion at the user site is possible.

Field conversion to double the approximate data capacity (going from a -51 DEC drive to a -01 DEC drive) is possible.

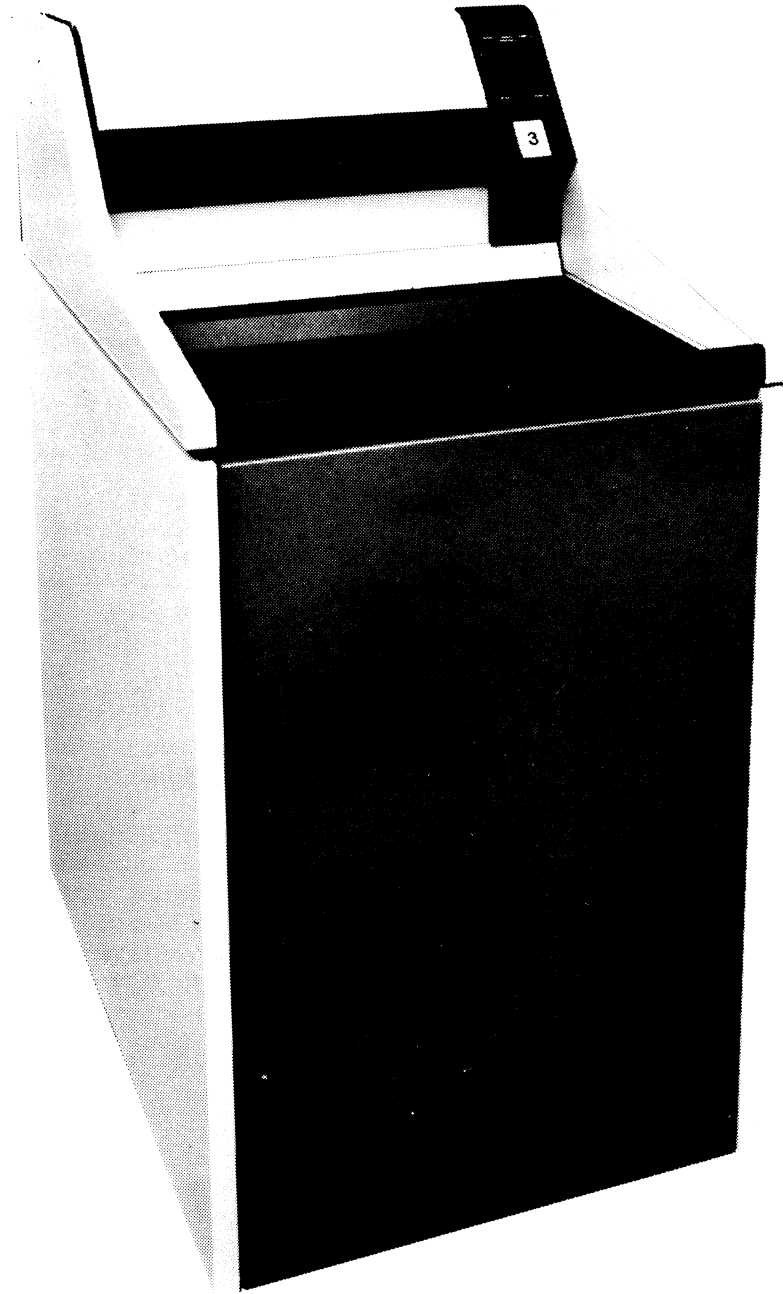
Control logic for either DEC drive is contained in an external attachment. It is designated the Device Control Logic (DCL) and is supplied and integrated with a drive by the user.

Each DEC drive (excluding DCL) is a recognized component of Underwriters Laboratories.

refinements as incorporated since the first 675 was delivered in October of 1974.

Any 677-XY ("X" designates maximum data capacity, "Y" designates a particular OEM) consists of customized features, integrated with a residual core of hardware and logic which provide fundamental drive capabilities. The "residual core" consists of major components in the drive's servo system, read/write system, spindle control system, and power system. The approach used in structuring any 677-XY drive has two principal objectives:

1. To maximize the latitude provided OEM's for customization, to insure drive compliance with OEM system compatibility, performance, and operating requirements.
2. To insure drive compliance with Memorex standards for high reliability, proven maintainability, and effective physical design—all as derived from manufacturing experience (18,000 drives) and operating experience (90 million online hours) with the core of hardware and logic which are common to all state-of-the-art Memorex drives.



**FIGURE 1-1. MEMOREX 677-01/51 DEC DISC STORAGE DRIVE**

The customized features in any 677-XY address:

- Either one or two spindles per drive
- Overall performance (either column below):

<b>Approx. data capacity per spindle:</b>	
200 megabytes	100 megabytes
<b>Average access time:</b>	
28.5 msec	28.5 msec
<b>Data transfer rate:</b>	
806 kilobytes/sec	806 kilobytes/sec
- Media compatibility (same column below):

<b>Memorex media:</b>	
Mark XI Disc Pack	Mark X Disc Pack
<b>IBM media:</b>	
3336-11 Disc Pack	3336 Disc Pack
- Interface lines
- Receiver and driver circuits
- Dual port capability
- Logical address plugs
- Console indicators and diagnostic display
- Automatic restart after ac power drop
- Dynamic braking of pack rotation
- 50 Hz power
- Rotational position sensing
- Address mark
- Pad to index after write address mark
- VFO/precompensated data conditioning
- 1 to 128 programmable sector divider
- Reading of registers
- Multiplex interface
- External cables and configuration
- Appearance group (covers and company logo)

In addition to customizing the drive itself as indicated above, the Memorex 800 Disc Storage Subsystem Tester can be customized to execute OEM diagnostic programs for testing 677-XY offline, and this has been accomplished for the 677-01 DEC and 677-51 DEC.

Special maintenance tools, in addition to the tester mentioned above, and conversion kits (power and data capacity) are also available.

## 1.1.2 Manual Purpose and Intended Use

This manual is the single authoritative reference for technical information on the 677-01 and 677-51 DEC drives that are provided by Memorex, with one exception: the *Illustrated Parts Catalog* is provided separately as Publication No. 677-01.23-00.

### NOTE

This manual, in its entirety, is applicable only to 677-01 DEC and 677-51 DEC. Applicability of particular paragraphs to any 677-XY (existing or planned) can be ascertained by applying the information in paragraph 1.1.1, recognizing at the outset that no other distinction is made in succeeding paragraphs between customized and standardized features.

Information in this manual is intended for use by Digital Equipment Corporation, in preparing documentation for installing, operating, servicing, and troubleshooting customer EDP systems which contain Memorex drives. Within the general framework of providing drive inputs to this system documentation, scope of coverage in this manual is unlimited. The format used is described as follows (refer to Table of Contents):

- Information is presented in a way that recognizes drive involvement with the rest of the system, thereby easing the transition from "drive inputs" to "system documentation." For example, drive installation procedures contain indications of when the drive is ready for DCL attachment, cabling, or system verification testing.
- Different audiences are recognized. For example, paragraph 2.4 is dedicated to operator information. Searching through other paragraphs for drive inputs to a "system operator's guide" is probably unnecessary.
- As the required number of drives are produced, nonfunctional refinements may be incorporated; this possibility is recognized in the manual. To lessen the probable impact on system documentation due to engineering changes in the drive, operating principles and

theory are described in functional terms. The result is a decreased probability of issuing manual updates, and consequently of changing system documentation to reflect the updates.

- Performance requirements are presented to support and extend the descriptions of system operating principles and theory—and also to make available, for possible customer use, a basis for designing tests of the drive at either the system or component level. Of course, performance testing of the drive after delivery is totally customer discretionary, but the requirements themselves relate directly to what systems do for the drive, and this is vital to understanding the operating principles and theory applied.

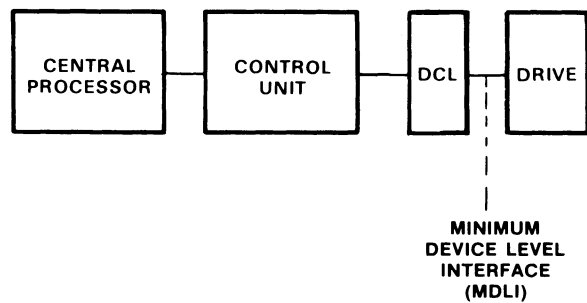
### 1.1.3 Drive Functions and Applications

The 677-01 DEC or 677-51 DEC drive is used as an input/output device in the data processing system shown in Figure 1-2. The system is configured using OEM control units and drive attachments to process sequential and randomly organized files using disc storage. Data is either read from a recording surface on the disc pack and sent to the system, or written on a disc surface for retrieval at a later time. The pack serves as permanent or temporary information storage media which can be written on by one drive, removed and stored, and then installed on the same or another drive with no degradation in data recovery or loss of pack compatibility. The drive rotates the pack at 3600 rpm, selects one of 19 read/write heads for an operation, positions the heads to the selected track on the disc surface, and allows the system to synchronize the data transfer. **The data transfer between drive and system occurs under control of an OEM device packaged as an external attachment to the drive.** The mechanical and electrical characteristics of the drive are customized to satisfy OEM interface specifications. Once the drive is installed into the system, routine operation of the drive is fully automated, requiring Operator intervention simply for an exchange of disc packs.

The name designated by DEC for the interface control attachment is **Device Control Logic (DCL)**. A DCL is physically attachable to a drive, and is attached to serve as the drive's port of com-

munication with the system. It is supplied by DEC, which also supplies information needed for DCL installation and servicing.

The sketch below defines the MDLI used as a reference point in discussing the system.



As indicated above, a drive transfers data to the system through the MDLI to its attached DCL.

The 800 Disc Storage Subsystem Tester (Figure 1-3) permits drive testing concurrently with system operation. The Tester attaches to the MDLI to perform microdiagnostics testing the key functional areas within a drive. The routines programmed into this tester are described in Appendix A.

Figure 1-4 illustrates drive external cabling for the example case of a system having four drives. All drive signal inputs and outputs are transmitted in dedicated lines, contained in Cables A and B (DCL commands of the drive) and Cables C and D (drive responses to commands). Regarding ac power connections, wall power is supplied to one drive in a grouping of three drives. For four to six attached drives, two wall power connections are required.

Two models of each drive, accommodating 60 Hz and 50 Hz operation at specified voltages, are supplied. Conversion between models in the field is straightforward (replacement of spindle motor assembly and belts and moving connections only).



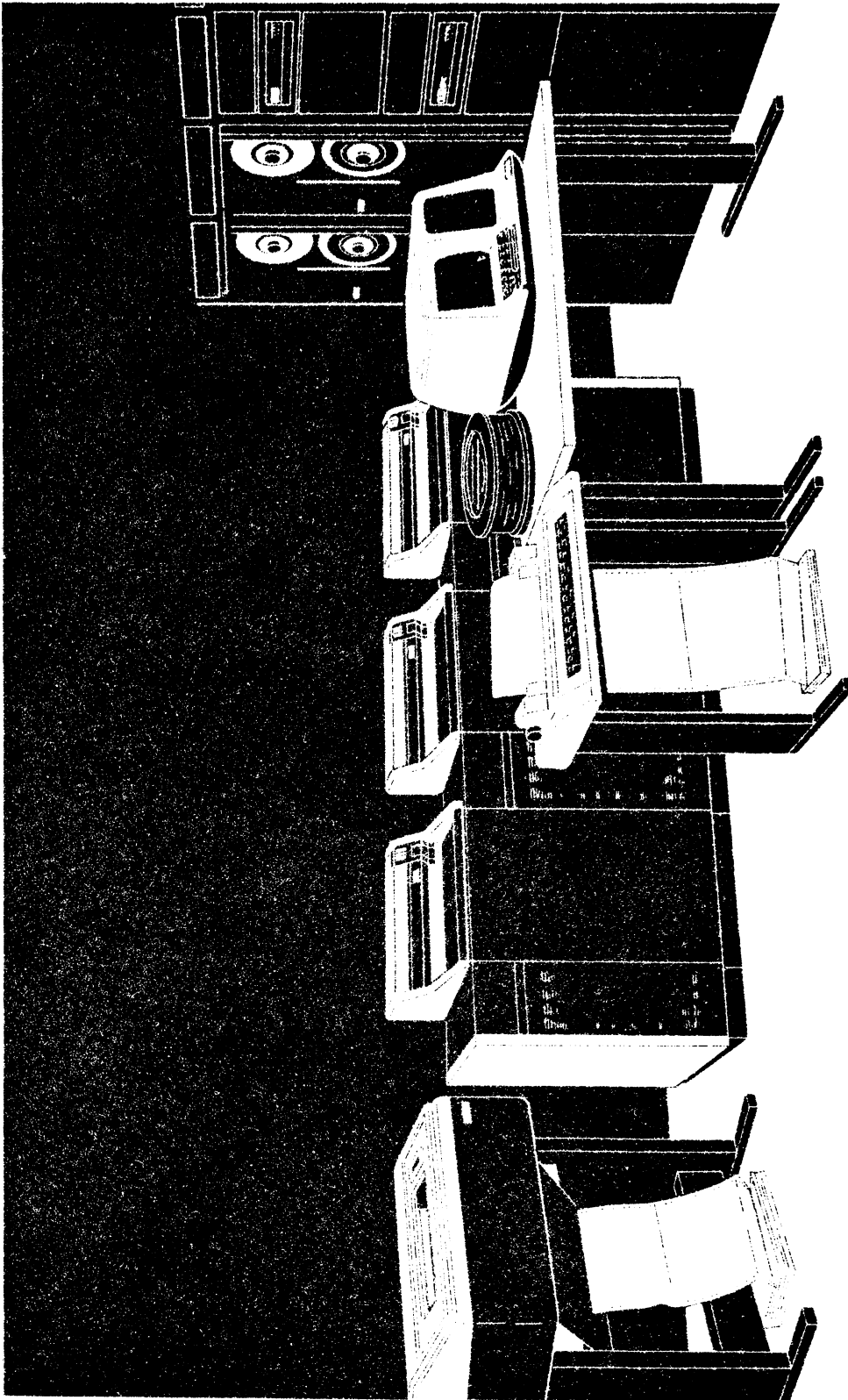
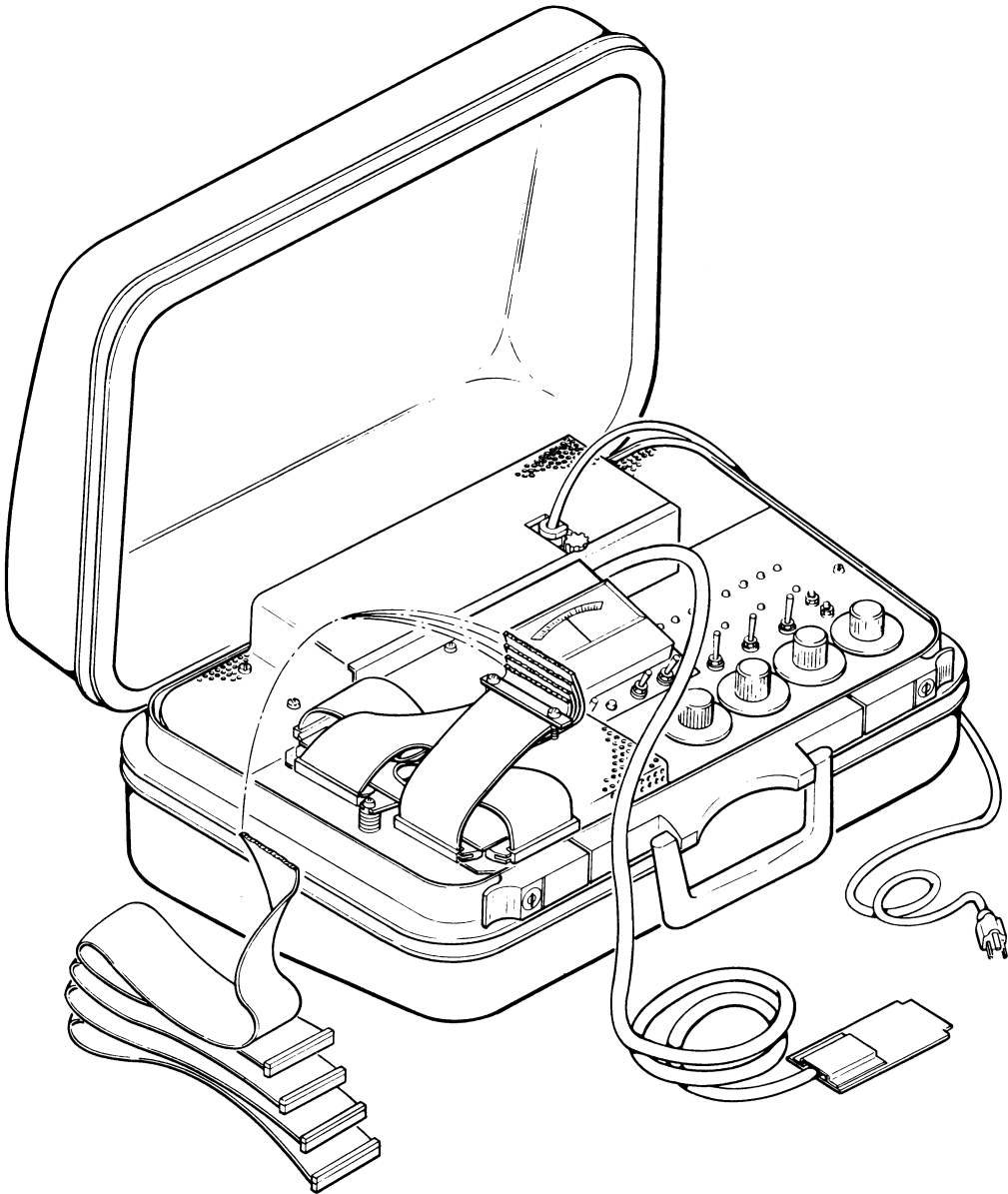


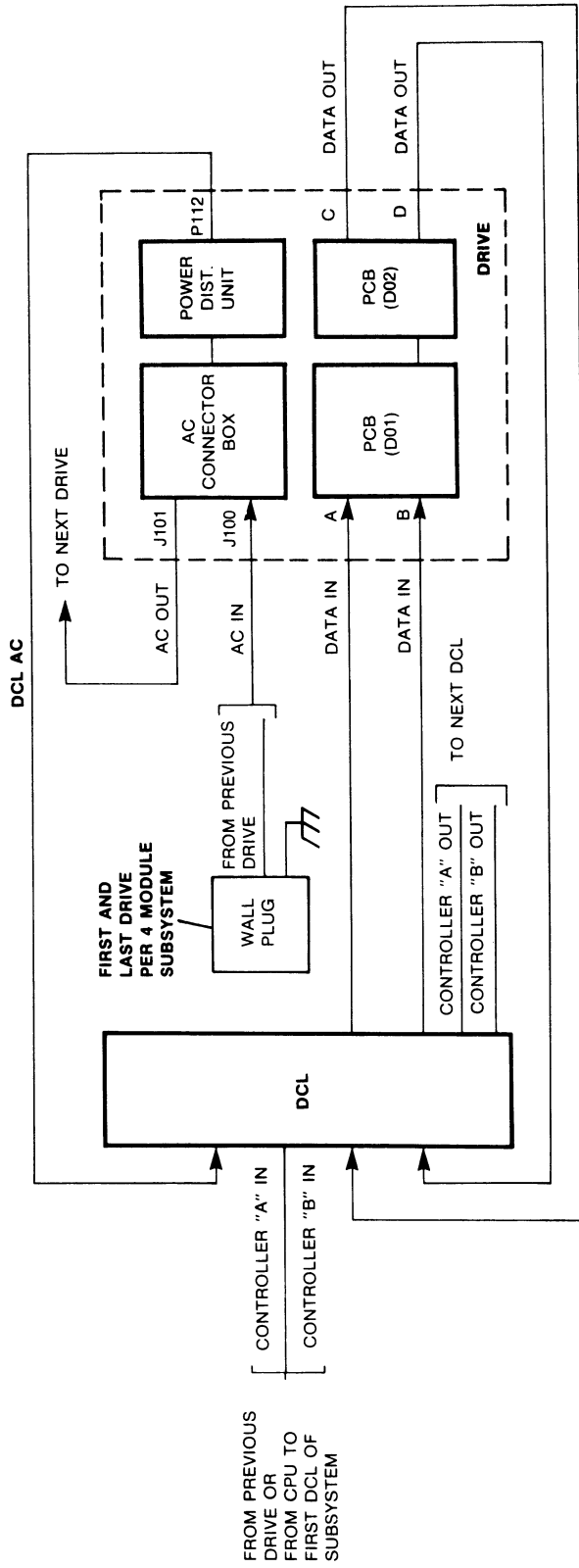
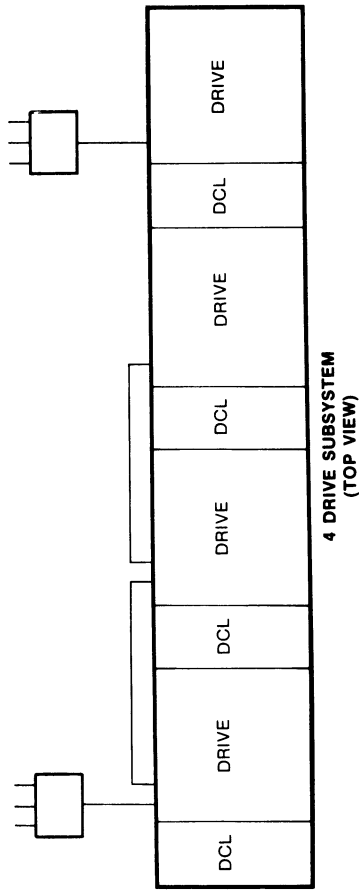
FIGURE 1-2. EXAMPLE OF A DATA PROCESSING SYSTEM



**FIGURE 1-3. MEMOREX 800 DISC STORAGE SUBSYSTEM TESTER**

QTY*	NAME	CONNECTION
4	DCL AC	DRIVE TO DCL**
2	AC IN	WALL TO DRIVE
2	AC OUT	DRIVE TO DRIVE
4	CABLE A	DCL TO DRIVE
4	CABLE B	DCL TO DRIVE
4	CABLE C	DRIVE TO DCL
4	CABLE D	DRIVE TO DCL
1***	CONTROLLER	CPU TO DCL
3	CONTROLLER	DCL TO DCL

\* FOR A 4-DRIVE SYSTEM  
 \*\* MEMOREX SUPPLIED  
 \*\*\* 2 FOR CONTROLLERS "A" AND "B" ACTIVE



**FIGURE 1-4. TYPICAL DRIVE EXTERNAL CABLING**

### 1.1.4 Disc Pack

The Memorex Mark X or XI Disc Pack (Figure 1-5) is a compact disc assembly weighing 20 pounds. Protective discs are located at the top and bottom of the disc array to minimize possible physical damage that might result from handling. A two-piece cover has a shock absorbing bumper strip for additional pack protection. Specifications for the Memorex packs equal or exceed those for equivalent capacity IBM packs.

The assembly contains 10 recording discs. A total of 19 surfaces are recording surfaces; the 20th surface contains prerecorded track-following (servo) and sector-timing data.

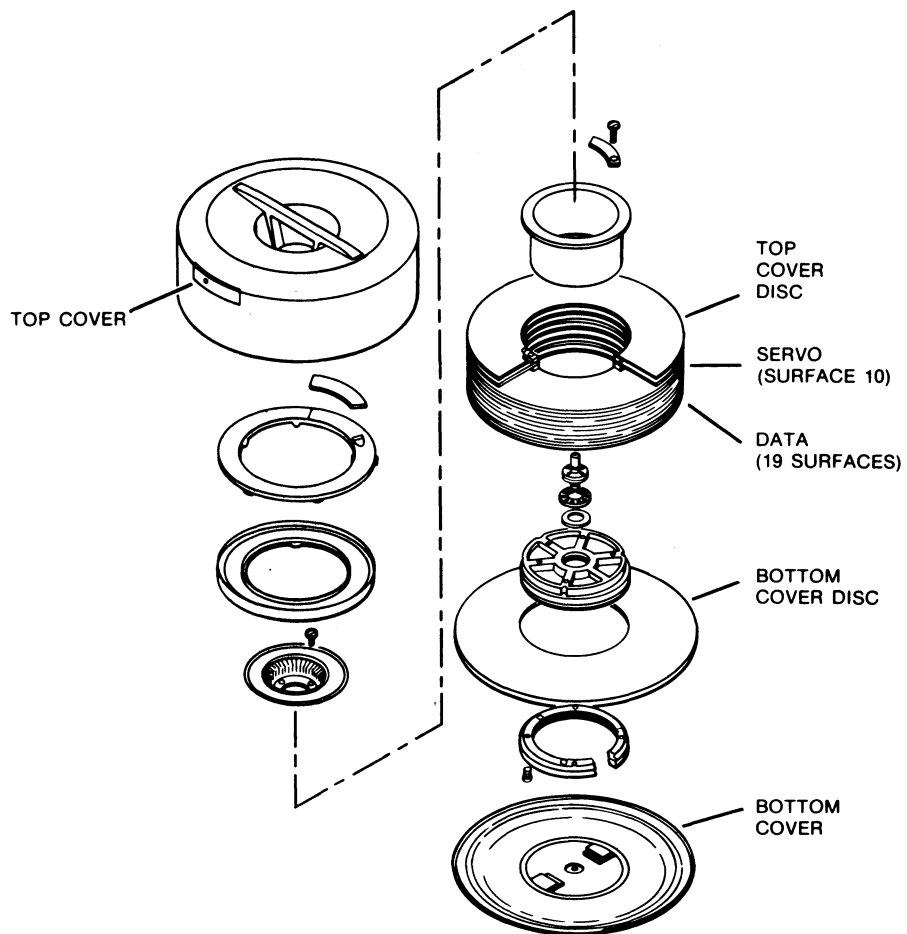
Installation of the disc pack is accomplished by simply sliding the drive's glass access door with a slight lifting action toward the rear of the drive, mounting the pack on the spindle in the conventional manner, and closing the access door.

### 1.1.5 Hardware Orientation

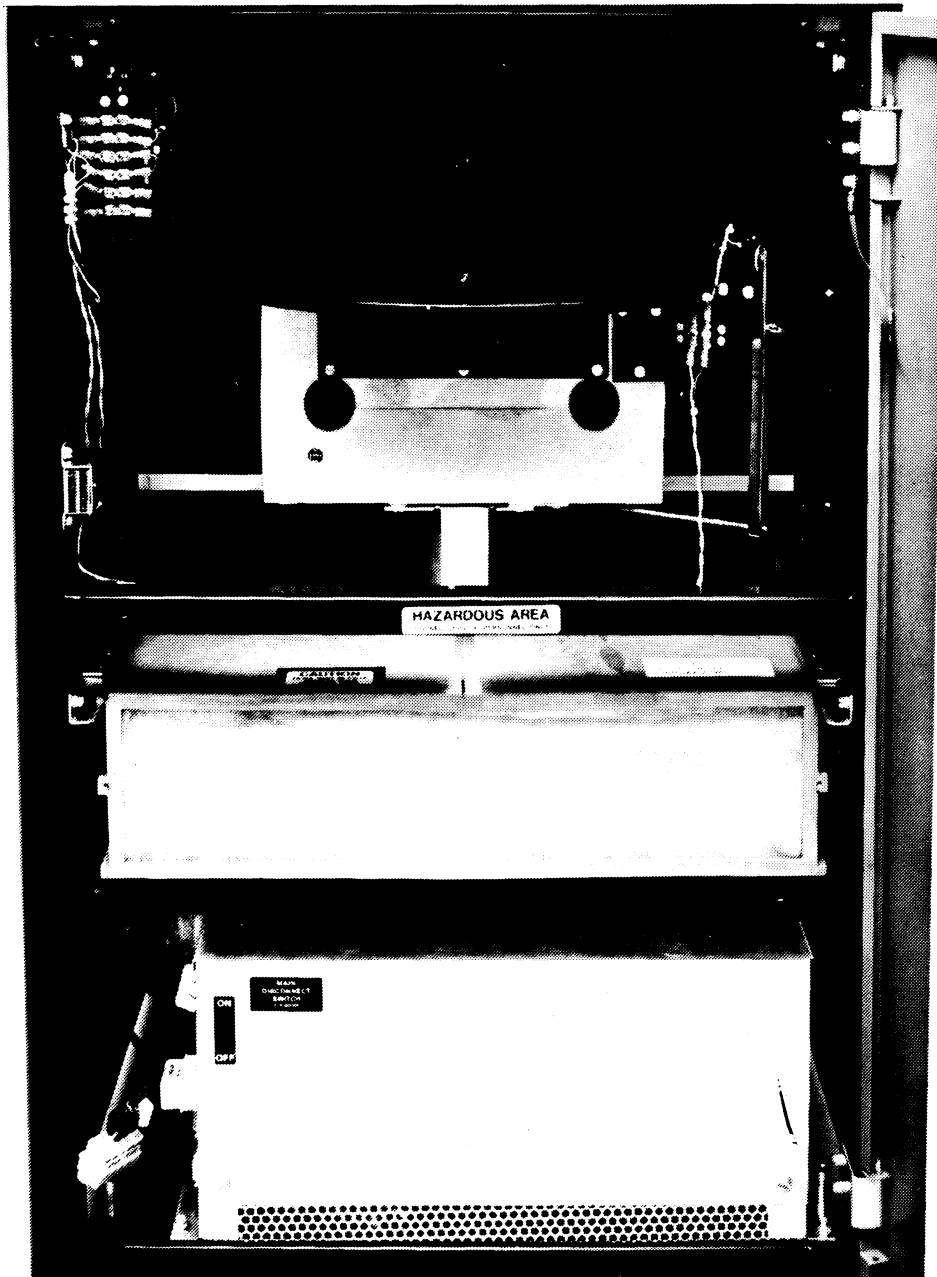
Major assemblies of the drive are shown in Figures 1-6 to 1-10.

The drive can be divided into a number of hardware groups. They are:

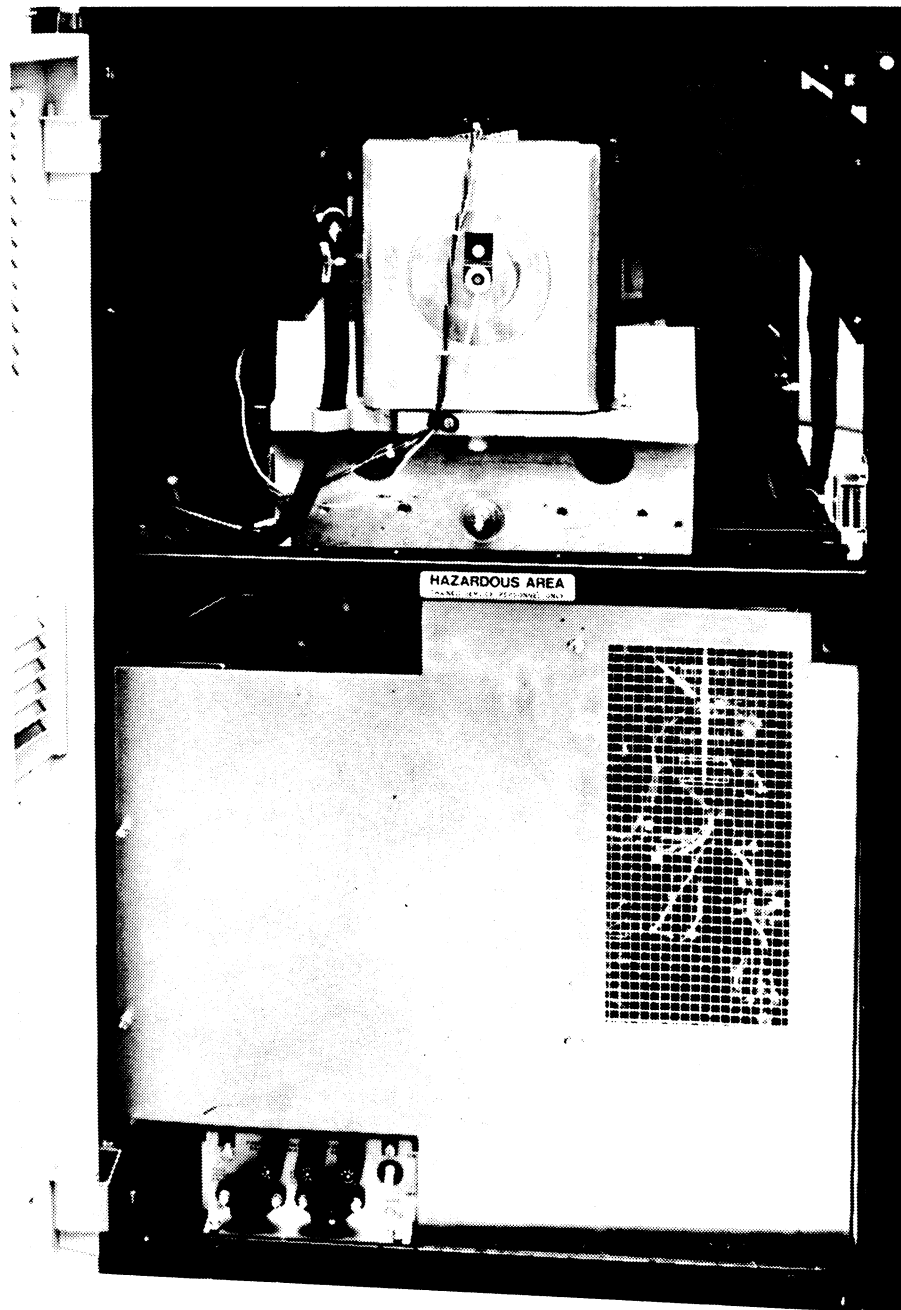
- Operator Control System, containing the specified controls and indicators for routine operation of the drive by nontechnical personnel.
- DCL (Device Control Logic) Support System, which receives a specified set of commands and data to be recorded on the disc pack, and sends specified responses to these commands and data retrieved from the pack to the DCL.
- Pack Access System, providing access to the pack area for loading and unloading disc packs. It consists of a sliding access door assembly and a door lock mechanism.
- Servo System, consisting of servo electronics, linear positioning motor assembly, and carriage assembly. Access to a data cylinder in the disc pack is achieved by the positioning motor; it controls motion of the carriage on which the read/write heads and servo head are attached. The servo electronics position and lock the carriage on the desired cylinder by reading information prerecorded on the disc pack at the factory. This information is read by the servo head. Once the desired cylinder has been reached and the Servo System has locked on the servo track, any read/write head may be electronically selected and the data recorded or retrieved from the pack.
- Read/Write System, consisting of read/write circuitry and read/write heads. The system accepts decoded control signals to provide the head select, read, and write functions. Including the servo head, there are a total of 20 heads, 10 mounted on each side of the T-block. Each head is contained in a head/arm assembly which fits into precision slots in the T-block and is held in place by screws.
- Spindle Control System, consisting of motor control circuitry, drive motor, and spindle. The disc pack attaches to the precision ball-bearing spindle assembly that is belt driven by the one-HP drive motor at 3600 rpm. The drive motor assembly is spring loaded with sufficient belt tension to achieve start and stop requirements. Fast stopping times are achieved by a dynamic braking system that utilizes the electromagnetic properties of the motor. The spindle assembly has a static brake mechanism which senses correct positioning of the disc pack and inhibits drive operation if the pack is not correctly positioned. The motor control circuits provide up- and down-sequencing control.
- Airflow and Filtration System, which is a patented absolute-filter system, moves filtered air throughout the shroud assembly and carriage way, and cools the linear positioning motor assembly. The spinning disc pack itself is used to pump filtered air through the drive. A wind tunnel guides the cooling air around and through the linear positioning motor assembly, and then out of the drive through the rear cover. It slides towards the rear to provide easy access to the heads for servicing. The fundamental design of the system allows for more effective air sealing, greatly reducing the chances of contamination.
- Power System, consisting of the power distribution unit and dc power supply. The power distribution unit distributes filtered ac power to the drive and dc power supply. The dc power supply provides all dc voltages needed for drive operation.



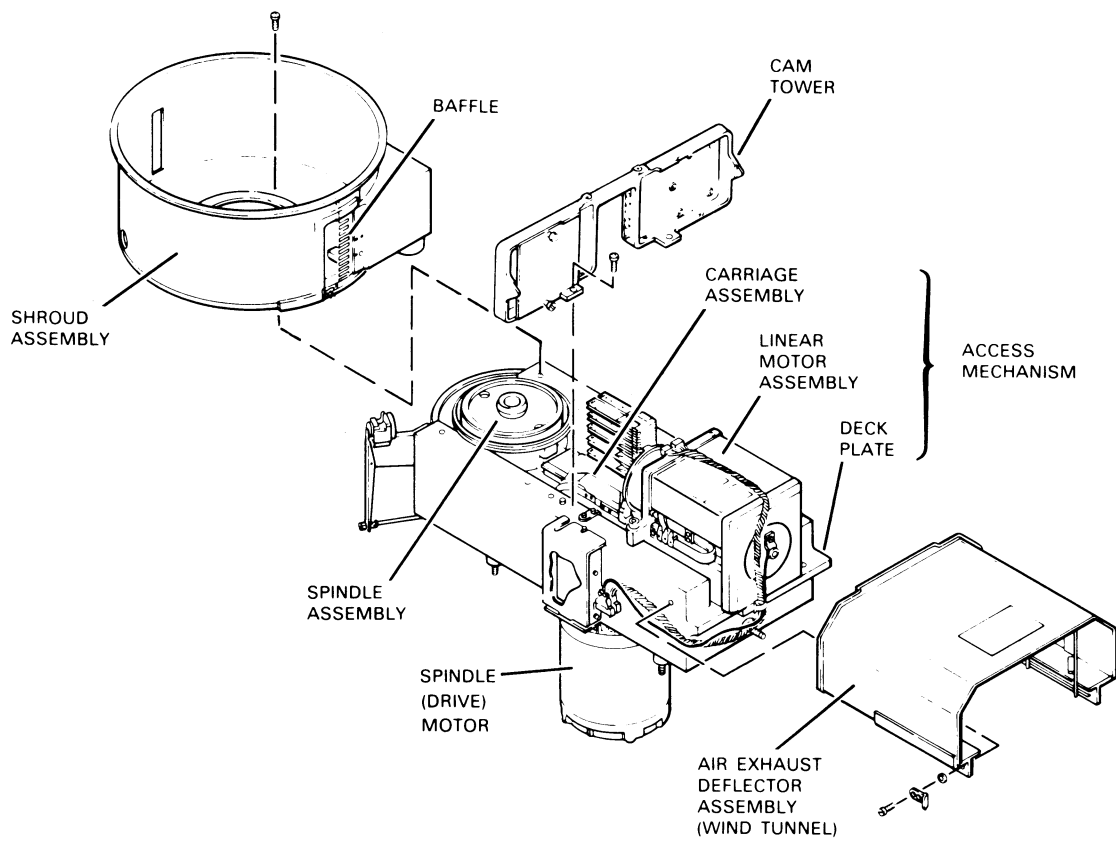
**FIGURE 1-5. MARK X OR MARK XI DISC PACK**



**FIGURE 1-6. DRIVE FRONT VIEW**

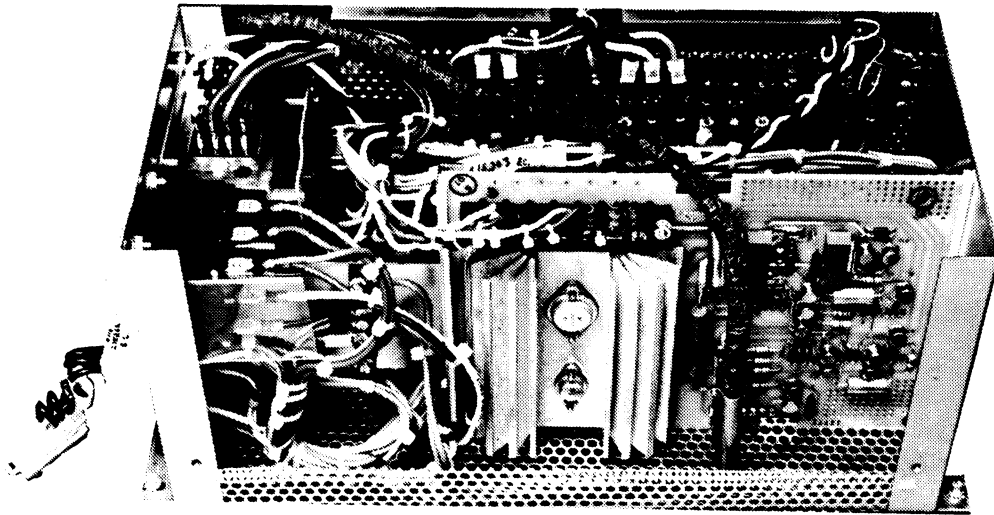


**FIGURE 1-7. DRIVE REAR VIEW**

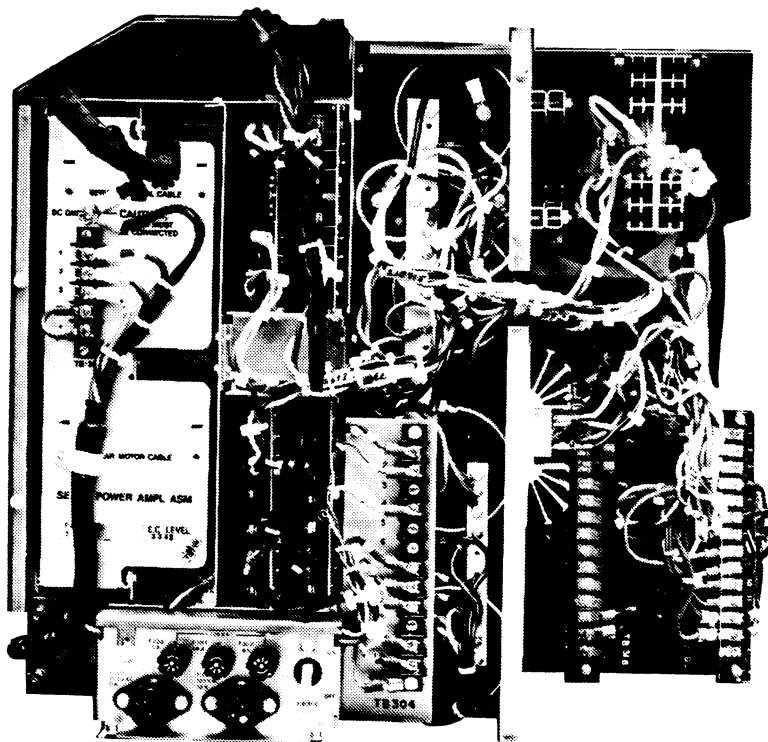


**FIGURE 1-8. DECK PLATE**





**FIGURE 1-9. POWER DISTRIBUTION UNIT**



**FIGURE 1-10. POWER SUPPLY**

## 1.1.6 Basic Drive Operations

The basic drive operations are head position, read, and write. Head position operations are head load, recalibrate, seek, offset seek, retract, and emergency retract.

**Head Load.** When the START switch on the drive's operator panel is depressed (assuming that the drive is installed in the system and power is applied), power is supplied to the spindle and the pack begins rotating. When the pack is up to speed (3600 rpm), the heads are positioned to Cylinder 000 in a head load sequence and the drive sends a signal to the system indicating it is ready. The ready state occurs approximately 20 seconds after the START switch is depressed, and is indicated to the drive user by lighting READY on the drive's display panel. At this time the drive is ready to receive a command to seek a specified cylinder, select a specified head, and read or write.

**Recalibrate.** A recalibrate operation causes the heads to be positioned at Cylinder 000. A recalibrate can be initiated by a system command, an operator inserting the logical address plug, or a seek incomplete condition (see paragraph below).

**Seek.** A seek operation causes the heads to be positioned at the desired cylinder and is initiated by a system command. If the heads fail to position at the proper cylinder, a seek incomplete status is sent to the system and a recalibrate operation is initiated.

**Offset Seek.** An offset seek operation is initiated by a system command and causes the heads to move a nominal distance away from the data track centerline to aid in recovering data after a read error has been made.

**Retract.** A retract operation is initiated when the drive is stopped, and causes the heads to be lifted from their flying position immediately above the disc surface and to be retracted from the pack to allow pack removal.

**Emergency Retract.** An emergency retract operation is used to remove the heads from the pack if the retract operation fails, or if there is a power or power supply failure.

**Write.** Writing is performed by a magnetic recording head which flies over a rotating disc in the prescribed cylinder location. The control unit

sends a serial stream of data to the drive to be MFM-encoded into clock or data pulses and recorded on a data track as magnetic flux reversals. The data remains on the disc surface where it can be read at any time until recorded over by new data. The disc pack containing this data can be removed from the drive and stored, and then installed in the same or another drive for reading or additional writing of data.

**Read.** The same head is used to write the data as used to read it. The magnetic flux changes recorded on the disc surface cause current reversals in the head's coils. The current reversals are converted to an output signal which is fed into the data separator (VFO). The VFO separates clock from data, generates serial data to the control unit, and provides a clock pulse to strobe the data.

## 1.2 DRIVE SPECIFICATIONS

### 1.2.1 General Drive Specifications

Table 1-1 summarizes general specifications for the 677-01A and B and 677-51A and B. This table provides, primarily, a single reference source of the major performance and operating features of the drive (both models), its physical characteristics, the numbering conventions adopted (heads, cylinders, surfaces), and the power and environmental requirements of the user site.

Referring to each specification for access time in Table 1-1 (first paragraph), access time is defined as the time interval between true transitions of SEEK START and READY.

The CONTROL A/B switch (Table 1-1) in the operator control panel is a three-position switch. When switched to the center position, the DCL is permitted to communicate with either port. When switched up or down, communication in one port is enabled and the other is disabled.

### 1.2.2 Error Rates

A seek error, defined as an incomplete seek or a seek to a wrong cylinder, occurs less than one in  $10^6$  random seeks (average).

**TABLE 1-1. GENERAL SPECIFICATIONS**

**DATA RETRIEVAL TIMES**

Average Latency Time .....	8.33 msec
Maximum Access Time, Track-toTrack* .....	6 msec
Maximum Access Time, Track 000 to Track 814* .....	53 msec
Average Access Time** .....	28.5 msec
Nominal Data Transfer Rate .....	806,000 bytes/sec

**DISC PACK CHARACTERISTICS**

Number of Recording Discs .....	10
Number of Recording Surfaces .....	19
Surface Numbering Scheme, Uppermost to Lowermost Surface .....	Surface 00 to 19
Servo Surface .....	Surface 10
Servo Format .....	Ref: Figure 1-11
Index Pattern .....	111110101101
Encoding Scheme .....	MFM
Track Density (677-01) .....	370 tracks/inch
Track Density (677-51) .....	192 tracks/inch
Tracks per Surface (677-01) .....	815
Tracks per Surface (677-51) .....	411
Bit Density, Outermost Track .....	2660 bits/inch
Bit Density, Innermost Track .....	4040 bits/inch
Rotational Speed .....	3600 rpm
Coating Material (Memorex Mark X or XI) .....	Oriented pfizer iron oxide
Approximate Weight .....	20 lbs.

**HEADS**

Number of Heads .....	20
Servo Head .....	Not addressable
Nominal Track Spacing Center-to-Center (677-01) .....	2.7 mils
Nominal Track Spacing Center-to-Center (677-51) .....	5.2 mils

**INFORMATION STORAGE CAPACITIES**

Track Capacity .....	13,440 bytes
Cylinder Capacity (bytes available to a single access) .....	255,360 bytes
Disc Pack Capacity (including alternate cylinders) .....	208,118,400 bytes (677-01 drive) 104,952,960 bytes (677-51 drive)

**DIMENSIONS AND WEIGHT**

Width (excluding DCL attachment) .....	22 inches
Depth .....	32 inches
Overall Height .....	47 inches
Pack Access Height (top of sliding door) .....	35 inches
Weight .....	550 lbs.

\* This figure does not include average latency time of 8.33 msec due to rotation.

\*\* Average access time =  $\frac{\text{time excluding latency to do all possible combinations of seeks}}{\text{number of seek combinations possible}}$

**TABLE 1-1. GENERAL SPECIFICATIONS (Continued)**

**SERVICE CLEARANCE**

Front .....	41 inches
Rear .....	45 inches
Sides .....	4 inches

**OPERATOR CONTROLS**

Switches .....	START/STOP WRITE PROTECT CONTROL A/CONTROL B Logical Address Plug Lamp Test
----------------	---

Indicators .....	START CONTROL A/B READY UNSAFE STANDBY WRITE PROTECT DOOR LOCKED
------------------	--

START/STOP TIME .....	20 sec
-----------------------	--------

**POWER REQUIREMENTS**

Model A:	
Frequency .....	60 ± 1.0 Hz
Voltage .....	208/230/240 Vac ± 10%
Phase and Configuration .....	3-phase + ground, Delta
Model B:	
Frequency .....	50 ± 1.0 Hz
Voltage .....	220/380/398/416 Vac ± 10%
Phase and Configuration, 220 Vac .....	3-phase + ground, Delta
Phase and Configuration, 380/398/416 Vac .....	3-phase + neutral, Wye
Model A/B:	
Maximum Run Current (excluding DCL) .....	10 amps/phase
Maximum Start Current .....	40 amps/phase
Number of Drives on One AC Cable String .....	2 drives
Maximum Phase Current Unbalance on Two Drives .....	70%
AC Line Filtering .....	self contained
DC Power Supply .....	self contained

MAXIMUM HEAT DISSIPATION .....	4450 Btu/hour
--------------------------------	---------------

INTERNAL AIR FLOW .....	550 CFM
-------------------------	---------

**OPERATING ENVIRONMENTAL CONDITIONS**

Temperature:	
Range .....	60° to 90° F
Optimum .....	75° F
Allowed Variation .....	5° F/hour

**TABLE 1-1. GENERAL SPECIFICATIONS (Continued)**

Relative Humidity:	
Range .....	20% to 80%
Optimum .....	50%
Allowed Variation .....	10%/hour and no condensation
Maximum Wet Bulb .....	78° F
Transient Line Noise Tolerance .....	250V peak for 100 nsec
(no irrecoverable data errors)	into 100 ohm load
AC Power Dropout Tolerance .....	10 msec
(continued operation while writing)	

**NONOPERATING ENVIRONMENTAL CONDITIONS**

Temperature:	
Range .....	50° to 110° F
Allowed Variation .....	10° F/hour and no condensation
Relative Humidity:	
Range .....	8% to 85%
Allowed Variation .....	No condensation
Maximum Wet Bulb .....	78° F

**SHIPPING ENVIRONMENTAL CONDITIONS**

Temperature:	
Range .....	-50° to 114° F
Allowed Variation .....	15° F/hour and no condensation
Relative Humidity:	
Range .....	5% to 90%
Allowed Variation .....	No condensation
Shock Tolerance, Free-Fall Drops of Packaged Drive .....	Flat on any side from 12-inch height; on any edge from 24-inch height
Vibration Tolerance of Package Drive .....	1.3g over the range 2 to 5 Hz, per ASTM D-999-63T

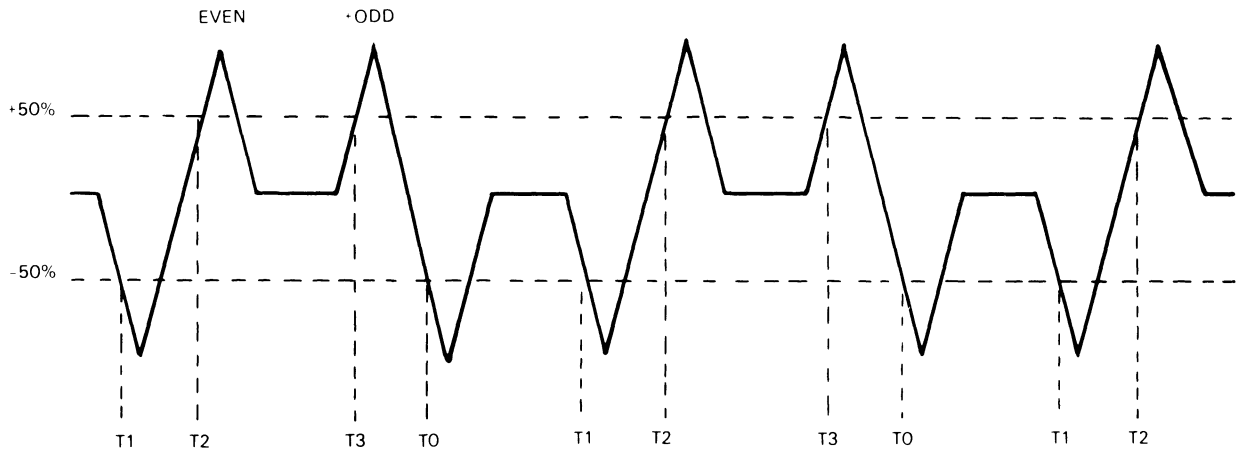
One drive performance parameter is specified by the Read Error Rate, which depends on whether the error is correctable or uncorrectable. The specification for read errors follows.

a. The Read Error Rate is determined for interchanged written media using Memorex Mark XI Disc Packs and drives aligned with Memorex CE Disc Packs.

b. Error detection and correction capabilities external to the drive must be capable of detecting and correcting burst errors of 11 bits or less in length within the record being read.

c. When a data error occurs, the customer's control unit must reorient on the failing record and retry the read operation up to 16 times. If the error persists, after 16 retries at nominal head position, the control unit must attempt to recover the data by offset operation and error correction. The retry sequence must be two retries, each at offsets of:

<u>677-01</u>	<u>677-51</u>
+200 microinches	+ 400 microinches
-200 microinches	- 400 microinches
+400 microinches	+ 800 microinches
-400 microinches	- 800 microinches
+600 microinches	+1200 microinches
-600 microinches	-1200 microinches



INTERVAL	TIME (NSEC)
T0 to T0	2480
T0 to T2	1240
T1 to T1	2480
T1 to T2	360 (Track 404)*
	360 (Track 808)
T1 to T2	250 (Track 000)
T3 to T0	360 (Track 404)*
	360 (Track 808)
T3 to T0	250 (Track 000)

\*100 Megabyte Drives

**FIGURE 1-11. SERVO DATA FORMAT**

- d. Correctable errors per items (a,b,c) do not occur at a rate greater than once in every  $10^9$  bits transferred.
- e. Uncorrectable/unrecoverable errors per items (a,b,c) do not occur at a rate greater than once in every  $10^{12}$  bits transferred.
- f. Error rates specified in items (d,e) exclude errors due to defects in a disc pack.

Following an initial test/debug period of 90 days, and before the period at which the drive approaches its end of life, the average Mean Time Between Failure (MTBF) of a population of 18 drives or more, distributed over 5 or more customer sites, is 2500 power-on hours. This statistical MTBF is based on performance of all recommended PM procedures as scheduled. Each drive must operate a minimum time period equal to the stated MTBF for the statistic to be meaningful.

### 1.2.3 PM Time and MTBF

Actual maintenance time spent by trained field engineers in performing the recommended preventive maintenance (PM) on a population of drives is estimated at 1 manhour per 200 operating hours per spindle.

### 1.2.4 Response to Brownouts

Redundant power monitoring circuits in the drive detect a loss of ac power (such as brownouts). If it occurs, heads are retracted from the pack at a controlled velocity with a clearance adequate to retain their sensitive calibrations and alignments with respect to the disc surfaces. The drive will withstand up to 10 msec ac supply dropout without loss of any recorded data or interruption to normal operation.

## 1.3 INTERFACE SPECIFICATIONS

Interface specifications are presented in paragraphs 1.3.1 (electrical) and 1.3.2 (mechanical). They address the principle items of drive customization for the OEM. Field engineers can skip over these paragraphs, and return to them as referenced in succeeding paragraphs.

The term "interface specifications" is generally used, but its specific meaning for this manual should be discussed to assure a common understanding. A discussion follows:

- The "interface" referred to is the internal/external interface relative to the drive. Three distinct interfaces are involved: between drive and DCL, drive and operator (human interface), and drive and user site. Their commonality is OEM customization, most extensive (relative to the drive) for the first interface mentioned and least for the last mentioned.
- The "specifications" referred to are drive design requirements and conventions which establish compatibility between both sides of each interface. Specifications containing data of special significance to technical readers are provided in this manual.
- Many "interface specifications" have significance when installing, operating, and servicing the drive. Regarding a particular interface specification, **who** needs to know (site planners, operators, instructors, and/or field engineers), **when** it is applied in the field (for installation, operation, and/or servicing), and **what** functional unit of the drive is being addressed (servo system, power system, etc.) have several appropriate combinations, depending on the item specified. For this reason, the interface specifications which follow are organized into general categories of electrical and mechanical types. This organization avoids repetition of information relating to specific subjects as addressed in later sections—and which, by referencing, will return field engineers here.

### 1.3.1 Electrical Interface Specification

#### 1.3.1.1 Command Summary

The drive contains logic to execute the following system commands:

- **Seek Go**, which specifies the start of seek motion, head to be used, cylinder difference, and direction

- **Seek Offset**, which specifies the start of offset motion, offset value, and direction
- **Write**, which specifies a write operation
- **Read**, which specifies a read operation
- **Recalibrate**, which specifies repositioning the heads to Cylinder 000
- **Device Initialize**, which specifies resetting of all safety latches
- **Device in Standby**, which specifies standby sequencing
- **Offset Reset**, which specifies resetting an offset operation by repositioning the heads over track centers.

#### 1.3.1.2 DCL to Drive Lines

Commands are provided via dedicated input lines contained in interface Cables A and B, connecting the DCL with the drive's Input PCB (logic gate position D01). Table 1-2 tabulates the names given to signals in these lines and their pin assignments. Each signal is described in the following paragraphs.

- **SEEK DIRECTION LEVEL** indicates the direction of the seek. The signal being true specifies a reverse seek (motion away from spindle). A false condition specifies a forward seek (motion towards spindle).
- **Cylinder Difference/Offset Lines (10)** indicate, for a seek operation, the number of cylinders to be traversed. The seek direction is given by the condition of **SEEK DIRECTION LEVEL**. For an offset operation, these lines indicate the amount and direction of head offset. The condition of **OFFSET MODE LEVEL** determines whether the operation is a seek or offset operation. Definitions of the 10 lines are:

Bit	Seek Operation	Offset Operation
1	DIFF=1	25 MICROINCHES
2	DIFF=2	50 MICROINCHES
4	DIFF=4	100 MICROINCHES
8	DIFF=8	200 MICROINCHES
16	DIFF=16	400 MICROINCHES
32	DIFF=32	800 MICROINCHES*
64	DIFF=64	(not used)
128	DIFF=128	REVERSE DIRECTION
256	DIFF=256	(not used)
512*	DIFF=512*	(not used)

\*Not used in 100 MB drive.

**TABLE 1-2. INPUT INTERFACE LINES**

Input Lines (36), MDLI to Drive PCB D01

—Pin Number and Signal—		—Pin Number and Signal—	
B40	-SEEK DIRECTION LEVEL	A19	-CAR 256
A24	-DIFF 1/OFFSET 25 $\mu$ IN	B18	-CAR 512
A26	-DIFF 2/OFFSET 50 $\mu$ IN	A01	-HEAD 1
A28	-DIFF 4/OFFSET 100 $\mu$ IN	A03	-HEAD 2
A30	-DIFF 8/OFFSET 200 $\mu$ IN	A05	-HEAD 4
A32	-DIFF 16/OFFSET 400 $\mu$ IN	A07	-HEAD 8
A34	-DIFF 32 /OFFSET 800 $\mu$ IN (100 MB)	A09	-HEAD 16
A36	-DIFF 64	B15	-WRITE COMMAND LEVEL
A38	-DIFF 128/OFFSET REV	B06	-WRITE STROBE
A40	-DIFF 256	B07	+WRITE STROBE
A11	-DIFF 512	B11	-READ COMMAND LEVEL
B38	-SEEK/OFFSET GO PULSE	B01	-READ/WRITE DATA
B36	-OFFSET MODE LEVEL	B02	+READ/WRITE DATA
B34	-OFFSET RESET PULSE	B09	-PORT A LAMP
B32	-RECALIBRATE	B13	-PORT B LAMP
B30	-DEVICE INITIALIZE PULSE	B24	-CONTROLLED GROUND
B28	-DEVICE IN STANDBY	B22	-SEQUENCE PICK IN
A17	-CAR 128	B20	+SEQUENCE ENABLE

- SEEK/OFFSET GO PULSE true causes the drive to start a seek or offset operation, providing FILE READY LEVEL true exists at the interface. The condition of OFFSET MODE LEVEL determines whether a seek or offset operation is started.
- OFFSET MODE LEVEL true/false indicates an offset/seek operation, respectively. For an offset operation (signal is true), it is set true prior to receiving SEEK/OFFSET GO PULSE true, and held true for the duration of the operation. Going false indicates completion of the offset operation, which occurs following the trailing edge of OFFSET RESET PULSE.

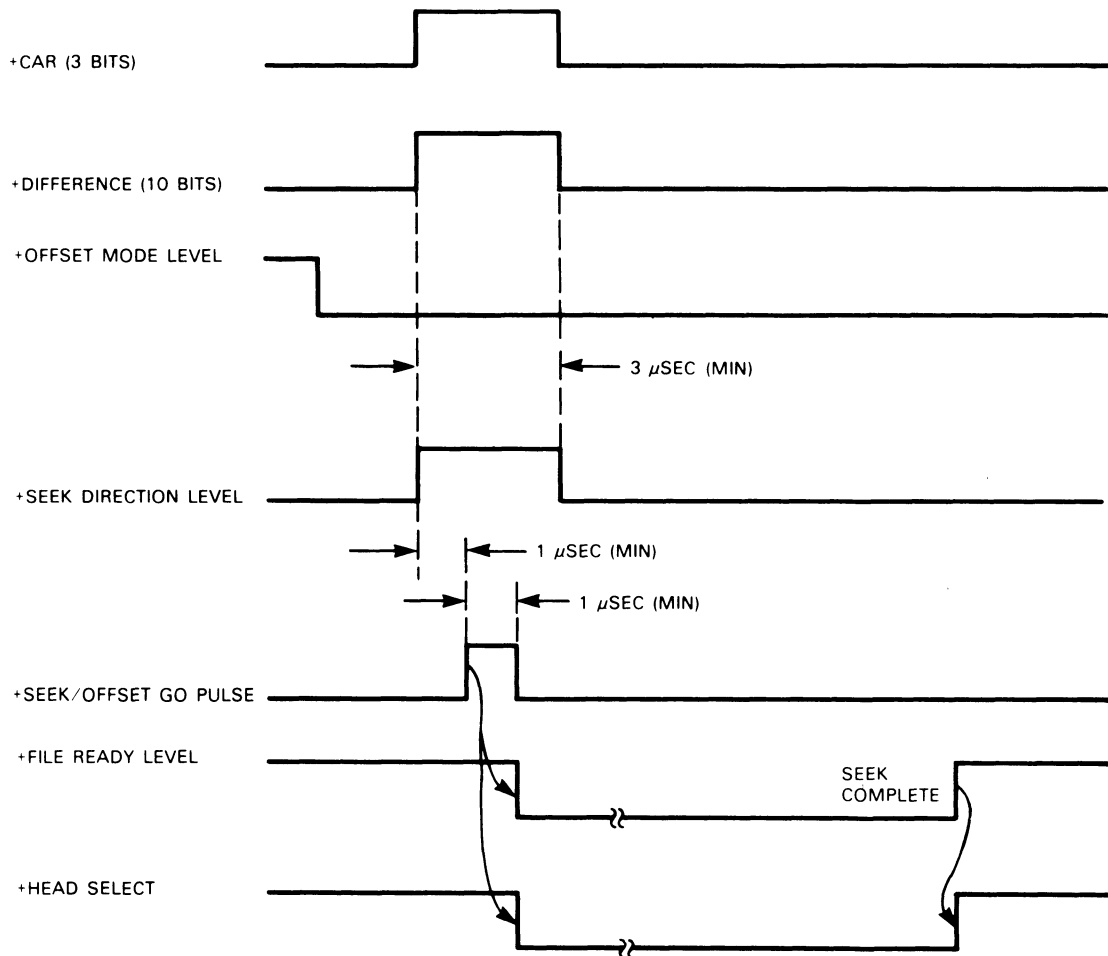
**NOTES**

1. For a seek operation (OFFSET MODE LEVEL is false), the seek argument is loaded into the drive logic when SEEK/OFFSET GO PULSE is true. The Cylinder

Difference/Offset Lines are loaded into the drive's difference counter, SEEK DIRECTION LEVEL is loaded into the reverse latch, and cylinder address is loaded into the cylinder address register. Drive internal logic initiates a SEEK START signal to begin traversal of the number of cylinders contained in the difference counter. Refer to Figure 1-12 for timing information.

2. For an offset operation (OFFSET MODE LEVEL is true), the offset argument is loaded into the drive logic when SEEK/OFFSET GO PULSE is true. The Cylinder Difference/Offset Lines are loaded into the offset register (difference counter is used), and the heads offset in the direction and amount stored in the offset register





- Notes:**
1. All signals shown are issued as commands to the drive, except FILE READY LEVEL and HEAD SELECT which are generated in the drive.
  2. FILE READY LEVEL is a required response of the drive to commands (sent to the interface). HEAD SELECT is not a required response (used by drive internal logic only).

**FIGURE 1-12. SEEK TIMING**

(difference counter). When the heads reach the specified offset position, the drive logic sends OFFSET READY LEVEL true to the interface. OFFSET READY LEVEL goes false if: a command to reposition the heads over track centers (OFFSET RESET PULSE) or to start a seek/offset operation (SEEK/OFFSET GO PULSE) is received while the heads are held offset. Refer to Figure 1-13 for timing information.

- OFFSET RESET PULSE true causes the heads, if offset from track centers (OFFSET MODE LEVEL is true), to reposition over track centers.
- RECALIBRATE true initiates a seek to Cylinder 000 (home position). Completion of the recalibrate operation is indicated by the drive sending FILE READY LEVEL true to the interface. Refer to Figure 1-14 for timing information.
- DEVICE INITIALIZE PULSE true resets all appropriate drive registers, including error registers. If START/STOP switch is in neutral position, DEVICE INITIALIZE PULSE true generates a start condition providing no abnormal stop conditions are present.

#### NOTE

Registers are also reset by the drive (internally) as described below.

- a. If the drive detects an invalid/missing index pulse (INDEX ERROR is true), INDEX ERROR is reset by the next valid index pulse.
  - b. If the drive detects an abnormal stop condition (ABNORMAL STOP is true), the abnormal stop register is reset when the Start/Stop switch on the operator panel is positioned to Start, providing the abnormal stop condition has disappeared.
  - c. SEEK INCOMPLETE is reset internally when the recalibrate initiated by the drive is complete.
- DEVICE IN STANDBY true causes the following events to occur in progressive order, while main power to the drive is maintained (refer to Figure 1-14):

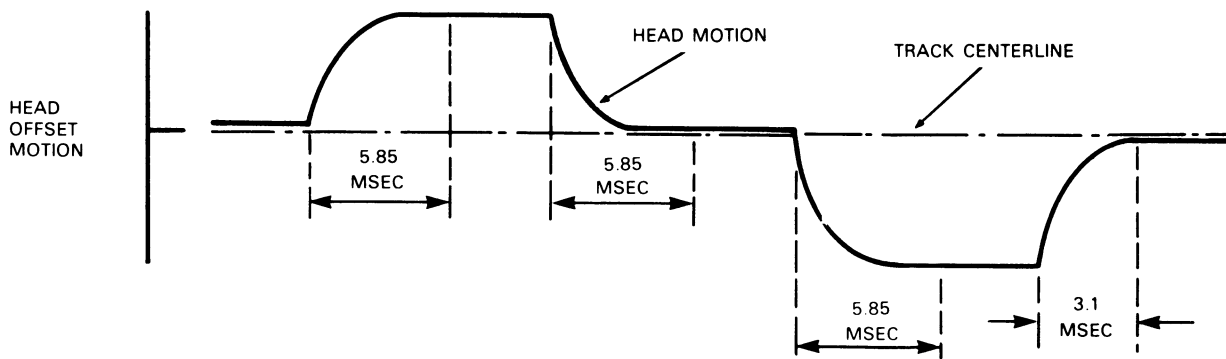
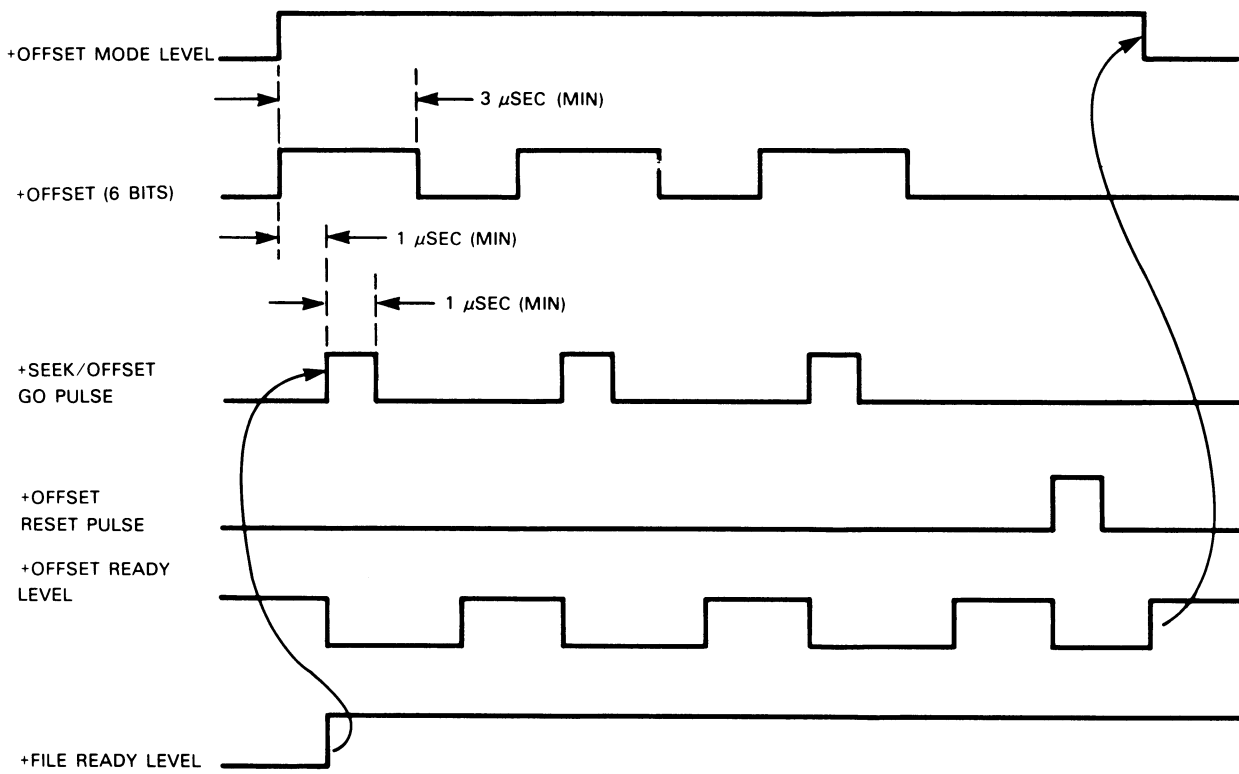
- a. Standby Latch in the drive is set and the Standby indicator in the operator panel is illuminated.
- b. Reverse motion to retract the heads from the pack is started.
- c. Indications that the heads are not loaded and the drive is not ready to execute a command are sent to the interface (ON LINE and FILE READY LEVEL are false), and illumination of the Ready indicator in the operator panel is extinguished.
- d. When the heads are fully retracted from the pack, an indication is sent to the interface (HEADS RETRACTED is true).
- e. Dynamic braking is applied to stop pack rotation.

When the drive is in the Standby mode, starting the drive is accomplished by pressing the momentary Start/Stop switch providing:

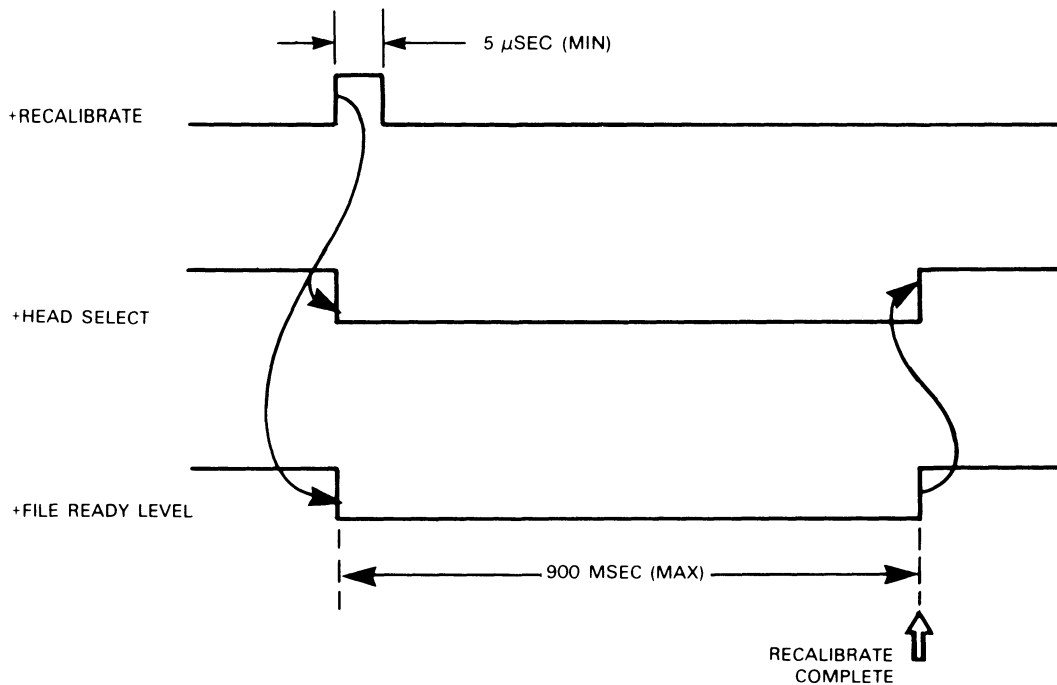
- a. Conditions permitting the start of a power-up sequence exist while no other drive is in process of powering up (CONTROLLED GROUND, SEQUENCE PICK IN, and SEQUENCE ENABLE are true).
- b. The disc pack is in place and the pack access door is closed.

With conditions a and b above satisfied, pressing the Start/Stop switch extinguishes the Standby indicator and causes sequencing to the "file ready" state.

- Cylinder Address Lines (3) transmit the high order address of the cylinder location which is used to program the optimum write current for the cylinder being written on. (Inside cylinders, having a smaller radius and higher bit density, require a lower write current.)
- Head Select Levels are 5 latched lines which contain the address of the desired head. The Head Select Levels must be valid for the duration of data transfer. The servo head is not addressable. Refer to Table 1-1 for the head numbering scheme used.
- WRITE COMMAND LEVEL true enables the write circuitry. Writing is accomplished using the head addressed by the Head Select Levels.



**FIGURE 1-13. OFFSET TIMING**



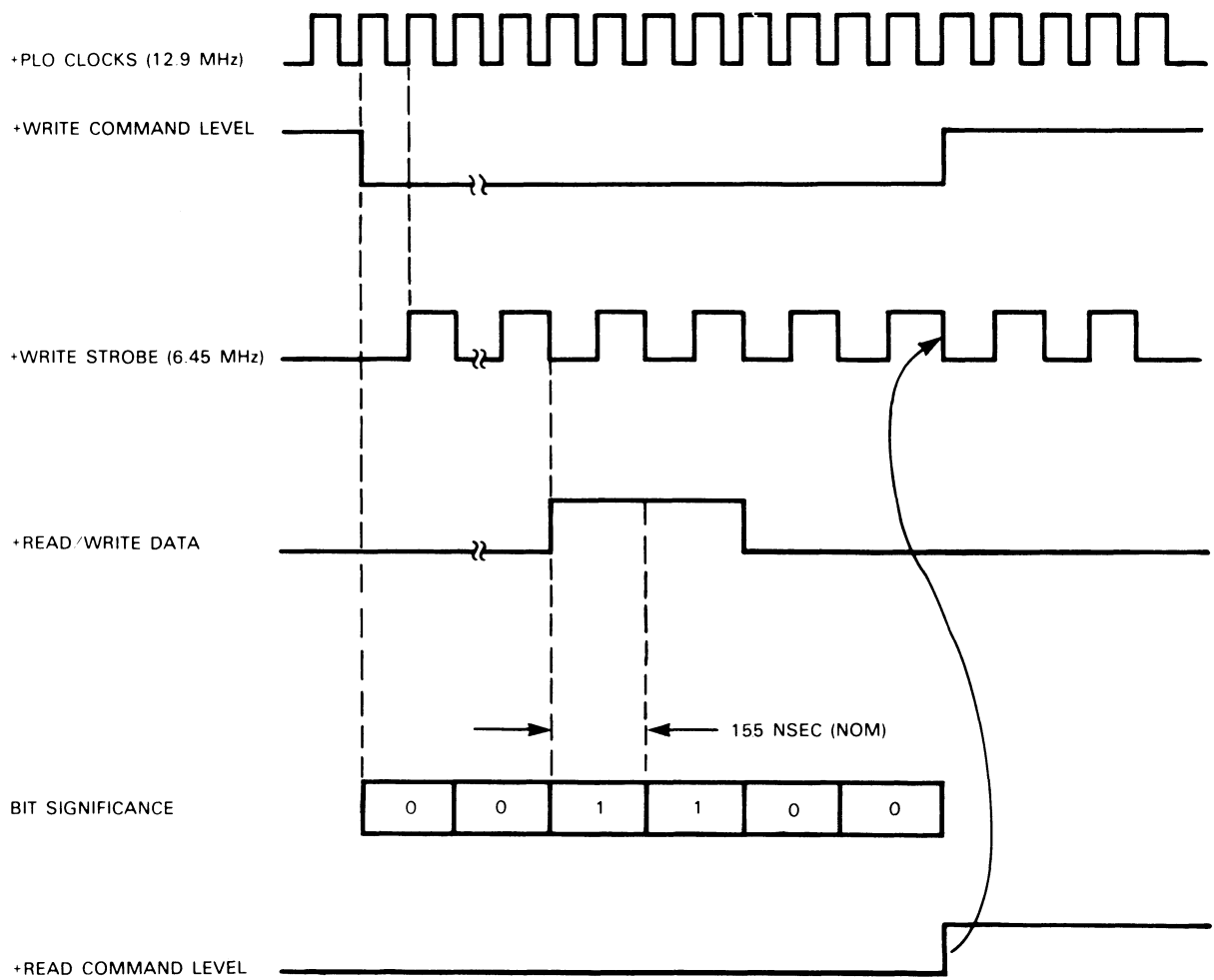
**FIGURE 1-14. RECALIBRATE TIMING**

- WRITE STROBE is a nominal 6.45 mHz signal used to clock write data transmitted to the drive for recording on the pack. It is derived from the PLO CLOCKS signal which is phase locked to the servo data prerecorded in the pack. Refer to Figure 1-15 for write data timing information.
- READ COMMAND LEVEL true enables the read circuitry. It is set true only in a valid data area. Reading is accomplished using the head addressed by the Head Select Levels.
- READ/WRITE DATA is a bidirectional line that transfers serial (NRZ) read or write data, depending on whether READ COMMAND LEVEL or WRITE COMMAND LEVEL is true. Refer to Figure 1-16 for read data timing information.
- PORT A LAMP true causes the CONTROL A lamp to illuminate. PORT B LAMP true causes the CONTROL B lamp to illuminate.
- CONTROLLED GROUND true allows the drive to load the heads. The false condition causes the heads to retract from the pack.

- SEQUENCE PICK IN true enables power-up sequencing in the drive, providing SEQUENCE ENABLE is true. Refer to Figure 1-17 for sequence timing information.
- SEQUENCE ENABLE is false (grounded) in the drive powering up, and becomes true when pack upspeed is reached. This signal is transmitted to each attached drive (through DCL cables) to insure that two or more drives do not require spindle motor surge current simultaneously.

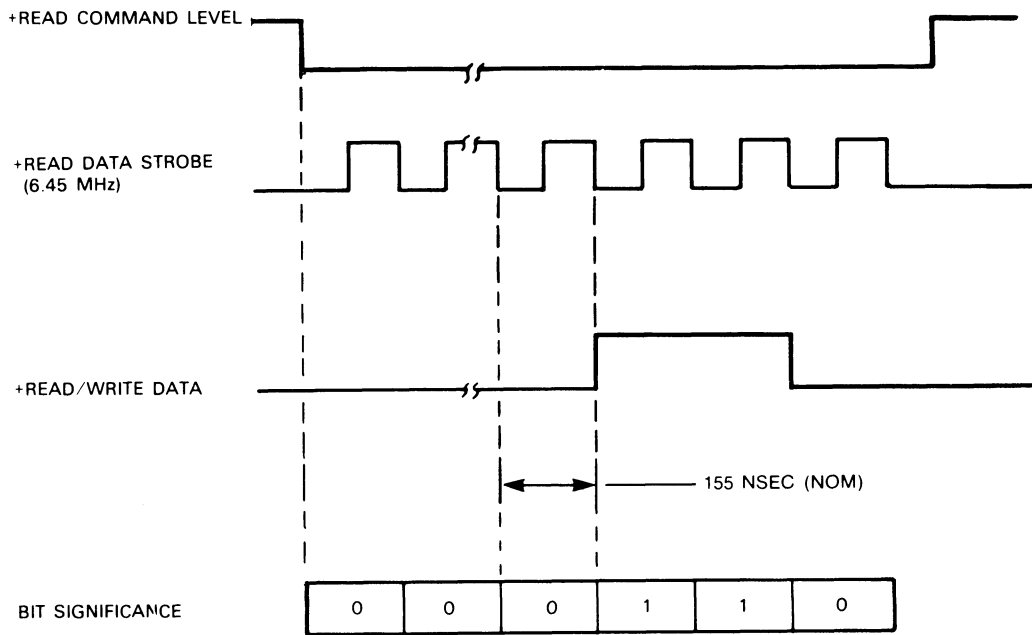
### 1.3.1.3 Drive to DCL Lines

Dedicated output lines are contained in interface Cables C and D, connecting the drive's Output PCB (logic gate position D02) with the MDLI. The signals in these output lines are required responses of the drive to system commands received in the input lines (described in paragraph 1.3.1.2). Table 1-3 tabulates both the names given by Memorex to the output signals and their individual pin assignments.



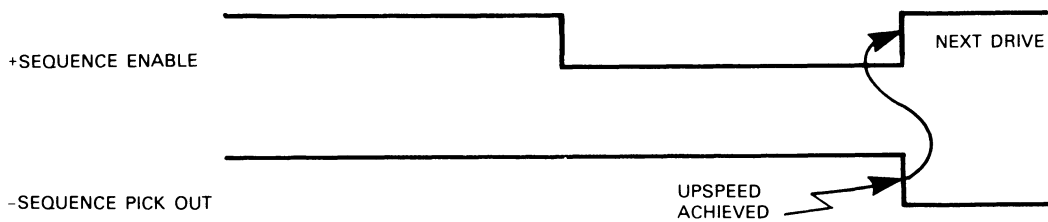
- Notes:**
1. Data level changes on the negative edge of WRITE STROBE.
  2. Data is good at the positive edge of WRITE STROBE.

**FIGURE 1-15. WRITE DATA TIMING**



- Notes:**
1. Data level changes on the negative edge of READ DATA STROBE.
  2. Data is good at the positive edge of READ DATA STROBE.

**FIGURE 1-16. READ DATA TIMING**



**FIGURE 1-17. POWER SEQUENCE TIMING**

**TABLE 1-3. OUTPUT INTERFACE LINES**

Output Lines (50), Drive PCB D02 to MDLI

—Pin Number and Signal—		—Pin Number and Signal—	
D11	-READ DATA STROBE	C15	-NO HEAD SELECT
D12	+READ DATA STROBE	C14	-HEADS UNSAFE
D08	-PLO CLOCKS	C13	-PLO UNSAFE
D09	+PLO CLOCKS	C03	-INDEX ERROR
C40	-OFFSET READY LEVEL	D28	-RESET REGS
C38	-FILE READY LEVEL	C12	-DC UNSAFE
D01	-INDEX PULSE	D38	-VELOCITY SERVO ENABLE
D02	+INDEX PULSE	D34	-DIFF LESS THAN 32
D05	-SECTOR CLOCK	D24	-COARSE TRACK
D06	+SECTOR CLOCK	D22	-ON TRACK
C36	-WRITE PROTECT LEVEL	D20	-SERVO DATA
C33	-PLUG ENABLE	D32	-SIGN
C32	-PORT A LOCKED	C01	-35V REGULATOR FAIL
C30	-PORT B LOCKED	C02	-READ AND WRITE
D36	-ON LINE	C09	-WRITE AND OFFSET
C28	-SEQUENCE PICK OUT	D18	-SEEK INCOMPLETE
C26	-WRITE CURRENT UNSAFE	D16	-UNSAFE
C25	-CURRENT SINK FAILURE	D14	-OFF CYLINDER
C24	-WRITE SELECT UNSAFE	C04	-ABNORMAL STOP
C23	-CURRENT SW UNSAFE	C06	-LOGICAL ADDRESS 4
C21	-DC WRITE UNSAFE	C08	-LOGICAL ADDRESS 2
C20	-TRANSITIONS DET FAIL	C10	-LOGICAL ADDRESS 1
C19	-TRANSITIONS UNSAFE	D26	-DIFF=0
C18	-AC WRITE UNSAFE	D30	-STOP VELOCITY
C17	-WRITE READY UNSAFE		
C16	-MULTI HEAD SELECT		

Signals in the output interface lines are described in the following paragraphs.

- READ DATA STROBE allows the DCL to strobe serial read data (from the bidirectional READ/WRITE DATA line described in paragraph 1.3.1.2) during a read command operation (duration of READ COMMAND LEVEL true). Figure 1-16 shows read data timing requirements.
- PLO CLOCKS generates the WRITE STROBE signal (described in paragraph 1.3.1.2) when writing (duration of WRITE COMMAND LEVEL true). It is a 1.9 megapulses/second signal which is phase locked to the servo data prerecorded in the disc pack. Refer to Figure 1-15 for write data timing information.
- OFFSET READY LEVEL true indicates the heads are located at the specified offset position. This signal goes false if: a command to

reposition the heads over track centers (OFFSET RESET PULSE is true) or to start a seek/offset operation (SEEK/OFFSET GO PULSE is true) is received while the heads are held offset (OFFSET READY LEVEL is true).

- FILE READY LEVEL true signifies the drive is ready to execute a command. The true condition occurs at the completion of power-up sequencing (which includes a head load), a normal (programmed) seek operation, or a recalibrate operation.
- INDEX PULSE true occurs at pack index, which means once every pack revolution ( $16.67 \pm 0.33$  milliseconds). Duration of INDEX PULSE true is  $620 \pm 100$  nanoseconds.
- SECTOR CLOCK is a 620 nsec clock with a nominal period of  $1.24 \mu\text{sec}$  and a total of 13,440 clock pulses per revolution.
- WRITE PROTECT LEVEL true indicates write operations of the drive are inhibited (control panel Write-Protect switch is manually set to Write Protect).
- PLUG ENABLE true occurs when the drive's Logical Address Plug is inserted into the operator panel.
- PORT A LOCKED true indicates the CONTROL A/CONTROL B switch in the drive's operator panel is in the CONTROL A position.
- PORT B LOCKED true indicates the CONTROL A/CONTROL B switch in the drive's operator panel is in the CONTROL B position.
- ON LINE true indicates read/write heads are loaded and the servo head is reading positioning data from the pack, or, a recalibrate operation is in process and the logical address plug is inserted.
- SEQUENCE PICK OUT is the SEQUENCE PICK IN signal when the drive's dc power is off, or when the drive is not performing a power-up sequence. This signal is false (open) during a power-up sequence and follows SEQUENCE PICK IN when the drive is up to speed. See Figure 1-17 for timing.
- WRITE CURRENT UNSAFE true indicates detection by the drive of write current without the presence of a write command. It causes deselection of heads and disabling of read/write capabilities.
- CURRENT SINK FAILURE true indicates detection by the drive of a nonoperative current sink at the end of a write command. It causes deselection of heads and disabling of read/write capabilities.
- WRITE SELECT UNSAFE true indicates detection by the drive of both write current sources—one for even numbered heads and the other for odd numbered heads—being active simultaneously. It causes deselection of heads and disabling of read/write capabilities.
- CURRENT SWITCH UNSAFE true indicates detection of a wrong write current for the selected cylinder during a write operation. It causes deselection of heads and disabling of read/write capabilities.
- DC WRITE UNSAFE true indicates detection of any one of the following unsafe conditions in the drive:
  - a. Write current with no write gate (WRITE CURRENT UNSAFE is true)
  - b. Transistor used to short write current to ground not turned on within the prescribed time (CURRENT SINK FAILURE is true)
  - c. Both write current sources on (WRITE SELECT UNSAFE is true)
  - d. Wrong write current (CURRENT SWITCH UNSAFE is true)
- TRANSITIONS DETECTOR FAILURE true indicates detection of write transitions without the presence of a write command. It causes deselection of heads and disabling of read/write capabilities.
- TRANSITIONS UNSAFE true indicates no write transitions during a write operation. It causes deselection of heads and disabling of read/write capabilities.
- AC WRITE UNSAFE true indicates detection of either TRANSITIONS DETECTOR FAILURE true or TRANSITIONS UNSAFE true (as a summary bit).



- WRITE READY UNSAFE true indicates the presence of a write command while the heads are not on cylinder. It causes deselection of heads and disabling of read/write capabilities.
- MULTIPLE HEAD SELECT true indicates selection of more than one head. It causes deselection of heads and disabling of read/write capabilities.
- NO HEAD SELECT true indicates no head being selected when a read or write command is present. It causes disabling of read/write capabilities.
- HEADS UNSAFE true indicates detection of either MULTIPLE HEAD SELECT true or NO HEAD SELECT true (as a summary bit).
- PLO UNSAFE true indicates detection of a loss of synchronization of the read/write PLO. It causes deselection of heads and disabling of read/write capabilities.
- INDEX ERROR true indicates detection of a missing or invalid index pulse. It goes false when the next valid index pulse is detected.
- RESET REGISTERS is true when a head load, unload, or a rezero is in progress.
- DC UNSAFE true indicates detection of dc power supply outputs which are not within the acceptable tolerance range. In such case, this line is grounded by a relay contact.
- VELOCITY SERVO ENABLE true indicates current to the linear positioning motor is programmed by the servo in the velocity mode.
- DIFF LESS THAN 32 true indicates the content of the difference register is less than 32.
- COARSE TRACK true indicates the servo head is within 432 microinches of cylinder center in the 200 MB drive or within 832 microinches of cylinder center in the 100 MB drive, or the servo head is not over servo data.
- ON TRACK true indicates the servo head is within 136 microinches of cylinder center in the 200 MB drive or within 262 microinches of cylinder center in the 100 MB drive, or the servo head is not over servo data.
- SERVO DATA true indicates the servo head is positioned over servo data.
- SIGN is generated by the drive's Head Alignment Unit (special FE test equipment) to indicate the direction of head misalignment when valid data is present. During the alignment procedure, SIGN true means the read/write data head is behind the servo head (offset away from spindle centerline). SIGN false means it is ahead of the servo head (offset towards spindle centerline). A true/false condition of this signal is indicated by a right/left deflection, respectively, in the Head Alignment Unit's indicator display. An indication of zero in the display would mean the head is in perfect alignment. The amount of deflection in the display indicates the number of microinches of misalignment (in either direction). The Head Alignment Unit also contains a light indicator which illuminates if invalid data is present.
- 35V REGULATOR FAIL true indicates detection of a failure in the regulator that controls the write current sources during a write operation. It causes deselection of heads and disabling of read/write capabilities.
- READ AND WRITE true indicates detection of both a read and write command simultaneously. It causes deselection of heads and disabling of read/write capabilities.
- WRITE AND OFFSET true indicates detection of a write command while a programmed offset is active. It causes deselection of heads and disabling of read/write capabilities.
- SEEK INCOMPLETE true indicates failure to complete a seek within 100 msec, or a recalibrate or head load operation within 750 msec.
- UNSAFE true indicates detection of any unsafe condition except SEEK INCOMPLETE or OFF CYLINDER (as a summary bit).
- OFF CYLINDER true indicates the loss of coarse track when ready and not in offset mode.
- ABNORMAL STOP true indicates detection by safety circuits of a condition that may impair mechanical or data integrity. Conditions causing ABNORMAL STOP to be latched true are:

- a. Loss of emergency retract power
  - b. An attempted head launch during powering up before upspeed is attained
  - c. Servo failure to perform a normal retraction of the heads
  - d. Failure to attain upspeed within 21.7 seconds after the start of a power-up sequence
  - e. An unsuccessful recalibrate operation, performed automatically after a seek incomplete condition occurred
  - f. Heads being retracted during a seek operation
- Logical Address Lines contain the binary decode of the Logical Address Plug.
  - DIFF=0 true indicates the content of the difference register equals zero.
  - STOP VELOCITY true indicates a carriage velocity less than 0.5 inch/second.

#### 1.3.1.4 Sequencing

Power up/down sequencing of the drive is the joint function of the drive and DCL, and can be enabled or disabled by either control unit (CU) attached to the DCL. The drive provides the logic and safety interlocks for its operation, and supplies the DCL with a sequence pick return line. In the following paragraphs, the interface signals involved in power sequencing, and the conditions that must be satisfied to initiate a power-up or power-down sequence, are described.

##### Interface signals:

- SEQUENCE ENABLE is false (grounded) in the drive powering up. It becomes true when pack upspeed is attained, then is sent to the remaining drives to allow another to sequence up. The false condition assures no multiple sequencing.
- SEQUENCE PICK IN true initiates power-up sequencing in a drive, provided SEQUENCE ENABLE is also true. SEQUENCE PICK OUT follows SEQUENCE PICK IN except when the drive's spindle is coming up to speed, at which time it is false. SEQUENCE PICK OUT becomes SEQUENCE PICK IN to the next drive on a string.
- Detection of a CU (#1 or #2) or DCL power failure is represented by an open contact in the CU or DCL +5-volt switch (CONTROLLED GROUND is false). For the case of an open contact in one CU switch, all drives are forced to retract heads if their panel switches are set to allow communication with that particular CU only. For the case of contact closure in both CU's and an open contact in one particular DCL, only the one drive attached to the DCL is forced to retract heads.

**Power-up sequencing conditions.** As described above, SEQUENCE PICK IN and SEQUENCE ENABLE must be true to initiate powering up. The following safety and interlock conditions within the drive must also be satisfied to initiate powering up:

- Drive is powered on (ac voltage is present and Start/Stop switch is in Start).
- If the drive is in standby mode (the Standby indicator is illuminated), the Start/Stop switch is pressed once.
- No abnormal stop conditions are present in the drive (ABNORMAL STOP is false).
- Pack access door is fully closed, a pack is inserted, and its cover is removed, all of which are indicated by signals used internally within the drive only.

**Power-down sequencing conditions.** A powering down of a drive is initiated in three ways: by placing the drive in standby, by placing the drive's Start/Stop switch in the Stop position (normal operation), or by the drive's detecting an abnormal stop condition. For the case of normal powering down, the drive retracts heads, ac power to the spindle motor is cut, and, after time delays have expired, the drive picks the dynamic brake relay and current. Braking brings the spindle to a full stop in approximately 20 seconds. At approximately 19 seconds, the door is unlocked to allow access to the almost-stopped pack. For the case of abnormal stop powering down, the presence within the drive of any one of six abnormal stop

conditions initiates a power-down sequence. The six conditions are identified in paragraph 1.3.1.3, under the description of the ABNORMAL STOP signal. Each is indicated if present by a signal used internally within the drive only.

#### NOTE

Except as specified for power sequencing, random or inadvertent operation of the Start/Stop switch in a drive is not related (does not interfere) with the operation of other drives.

### 1.3.1.5 Line Drivers and Receivers

Power sequencing signals described in the previous paragraph are transmitted with single-ended type SN7438 line drivers and SN7404 line receivers.

The following signals are transmitted with differential-type SN75113 line drivers and SN75107 line receivers (refer to Figure 1-18):

- READ/WRITE DATA (bi-directional)
- WRITE STROBE
- READ DATA STROBE
- PLO CLOCKS
- SECTOR CLOCK
- INDEX PULSE

The "remaining" drive signals—meaning input/output signals not covered above—are transmitted with single-ended type SN7438 line drivers and SN7404 line receivers as shown in Figure 1-19. Referring to this figure, the line receiver in the drive for each input signal is terminated to an equivalent of 80 ohms in the manner shown. The line receiver in the DCL for each output signal should be similarly terminated.

### 1.3.1.6 AC Power

Figure 1-20 shows ac power distribution inside the drive. Referring to the figure, wall power is received at AC IN connector J100. RFI filtering is accomplished by the three-phase RFI filter across the line at its input, and line-to-line filters at certain points of distribution. The ac to the drive dc power supply, power supply fan, and spindle motor is filtered twice. The ac to the logic fans and DCL (dc power supply) is filtered once. Filtered ac to the DCL is provided at DCL AC connector J111. The

circuit breaker and power conversion plug are provided before load distribution to either DCL or drive components; they are discussed below.

CB100 (Figure 1-20) is the drive's main circuit breaker. When switched off, no power is supplied to any component of the drive. It must be off during replacement of printed circuit boards (PCBs). With CB100 off, inserting or removing PCBs does not introduce noise pulses on the interface cables. When switched on, power is applied to all components of the drive requiring power.

#### NOTE

If a complete loss of ac (power blackout) occurs, heads are automatically retracted from the disc pack. The pack can be removed before power is restored by following the instructions given in paragraph 2.4.5.2.

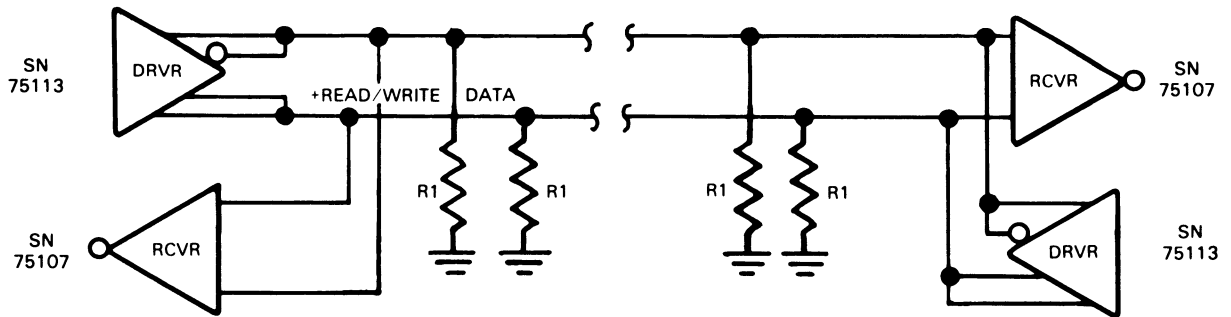
The ac distribution circuitry allows for easy modification to accommodate power sources available worldwide. In the United States, 208/230 Vac appears from line to line ("delta" load). This is the case assumed in Figure 1-20; neutral is not used. In other world locations, 220/230/240 Vac from line to line, or 380/398/416 Vac from line to neutral ("wye" or "star with neutral" load) may be the case—and the only case where neutral is used. By using the power conversion plug appropriately, as specified on the plug itself, the drive loads may be shifted from a delta load to a wye load.

#### NOTE

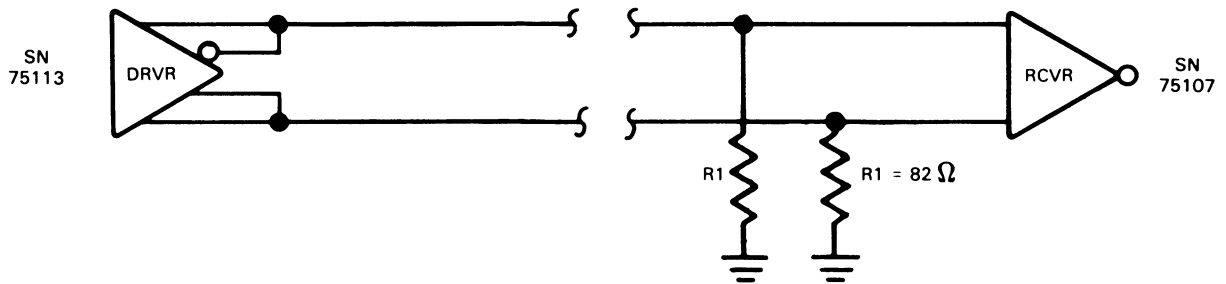
Although the power conversion plug accommodates power source voltage variations, frequency differences necessitate a Spindle Control System in the drive that is customized for either 60 Hz or 50 Hz operation. Field conversion (page 4-35) requires a motor change. Each model of the drive is designed for operation at an exclusive frequency, either 60 Hz (drive Model A) or 50 Hz (drive Model B).

Allowable tolerances of the possible source voltages and frequencies are specified in Table 1-1.

Line current requirements under different machine conditions and input voltages are tabulated in Table 1-4.

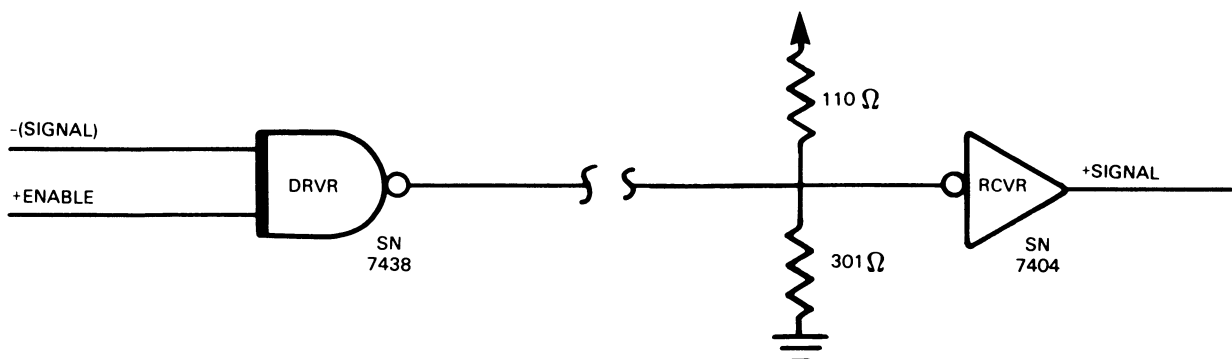


(a) Bidirectional Driver/Receiver Configuration

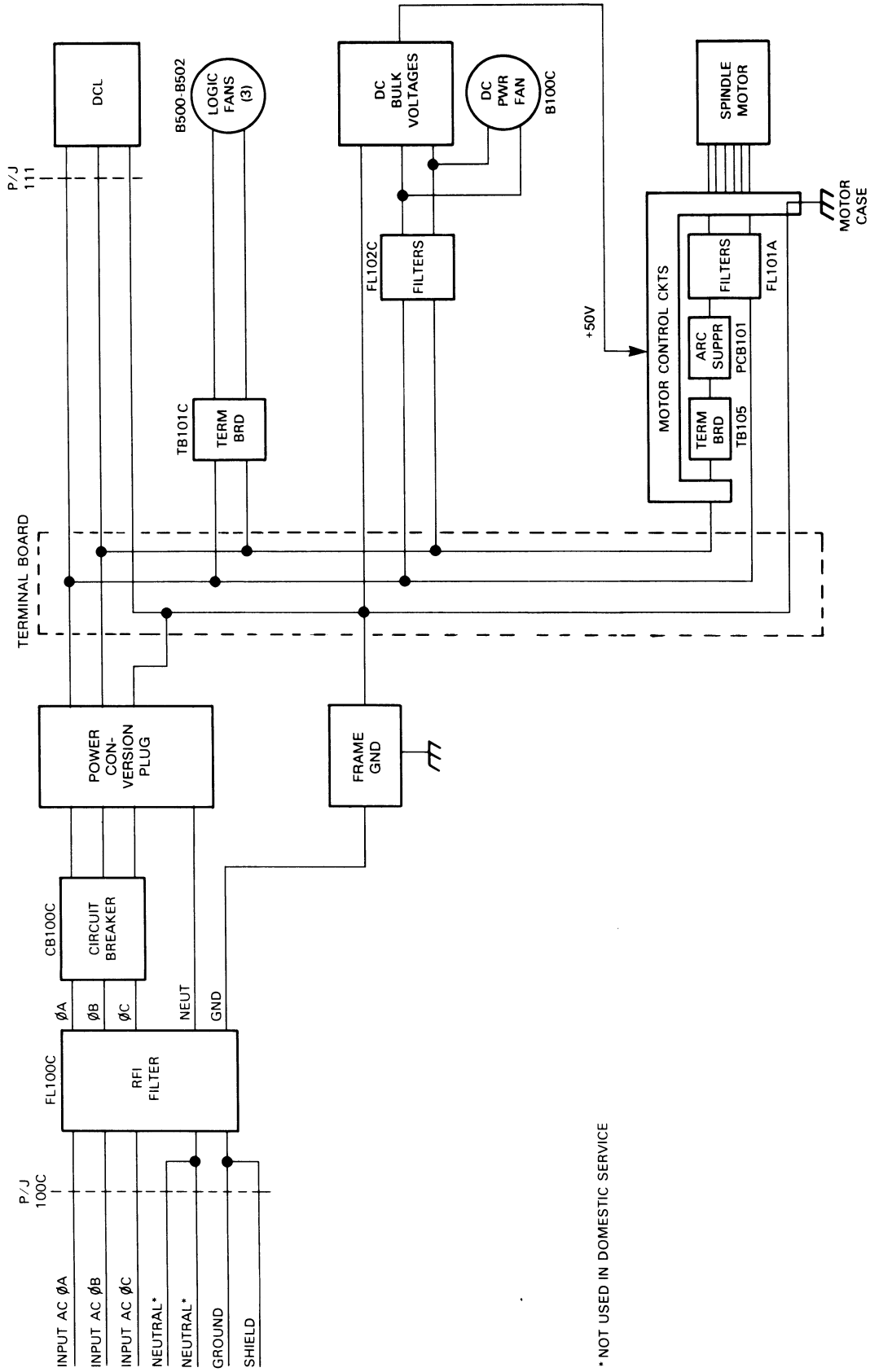


(b) Unidirectional Driver/Receiver Configuration

**FIGURE 1-18. DIFFERENTIAL LINE DRIVERS AND RECEIVERS**



**FIGURE 1-19. SINGLE-ENDED LINE DRIVERS AND RECEIVERS**



\* NOT USED IN DOMESTIC SERVICE

FIGURE 1-20. AC POWER DISTRIBUTION

**TABLE 1-4. 677-01/51 LINE CURRENT REQUIREMENTS**

	Source	Vac	Status	Maximum RMS Current (amps)		
				Phase A	Phase B	Phase C
SINGLE DRIVE	208	208	Motor Off	1.0	2.5	1.5
		208	Drive Seeking	7.0	3.0	5.5
		208	Start Up	31.0	2.5	30.0
	60 Hz DELTA CONNECTED	230	Motor Off	1.0	3.0	1.5
		230	Drive Seeking	8.5	4.5	6.0
		230	Start Up	30.0	2.5	31.0
	240	240	Motor Off	1.0	2.5	2.0
		240	Drive Seeking	8.5	4.5	6.0
		240	Start Up	33.0	2.5	36.5
	50 Hz DELTA CONNECTED	220	Motor Off	1.0	4.5	1.0
		220	Drive Seeking	9.5	3.5	7.0
		220	Start Up	26.5	3.5	25.5
	380	380	Motor Off	2.0	1.0	0
		380	Drive Seeking	3.0	1.0	7.0
		380	Start Up	2.0	1.0	25.5
50 Hz WYE CONNECTED	398	Motor Off	2.0	1.0	0	
	398	Drive Seeking	3.0	1.0	7.5	
	398	Start Up	2.0	1.0	25.5	
416	416	Motor Off	2.0	1.0	0	
	416	Drive Seeking	3.0	1.0	8.0	
	416	Start Up	2.0	1.0	29.0	
2 DRIVES CONNECTED ON SAME POWER STRING*	208	208	Motor Off	8.5	4.5	6.5
		208	Drive Seeking	10.5	8.5	10.0
		208	Start Up	8.5	30.0	32.0
	60 Hz DELTA CONNECTED	230	Motor Off	11.0	6.5	6.5
		230	Drive Seeking	12.0	10.0	10.5
		230	Start Up	12.0	30.0	31.0
	240	240	Motor Off	11.0	6.5	7.0
		240	Drive Seeking	12.0	9.5	11.0
		240	Start Up	11.0	33.0	37.0
	50 Hz DELTA CONNECTED	220	Motor Off	11.0	10.0	4.5
		220	Drive Seeking	13.5	10.0	12.5
		220	Start Up	9.0	33.0	30.0
	380	380	Motor Off	3.0	4.0	7.0
		380	Drive Seeking	4.5	4.5	13.5
		380	Start Up	3.0	4.0	32.5
50 Hz WYE CONNECTED	398	Motor Off	3.0	4.0	7.5	
	398	Drive Seeking	4.5	4.5	13.5	
	398	Start Up	3.0	4.0	33.0	
416	416	Motor Off	3.0	4.0	8.0	
	416	Drive Seeking	4.5	4.5	14.5	
	416	Start Up	3.0	4.0	37.0	

\* One drive under test—the other on line and random seeking

Grounding is discussed in paragraph 1.3.1.7.

AC power connector types, locations, designations, and pin assignments are specified in paragraph 1.3.2.

### 1.3.1.7 Grounding

Frame (chassis) ground is a 0.380 tinned area near the RFI filter used as a common terminal for all ac grounds; it is designated FRAME GRD and shown in Figure 1-20. By using central grounding, frame current is virtually eliminated.

Drive to DCL frame ground is provided by the OEM using the shield in the ac power cable and green chassis wire from DCL to drive chassis.

Drive to DCL dc ground (system ground) is provided by the OEM. According to OEM specifications, system ground is tied to frame ground in the control unit(s), at a common point to prevent ground loops, using the shield in the drive's output signal cables. System ground is not tied to frame ground in the drive.

#### NOTE

For personnel safety when a drive is to be operated without signal cables, the OEM provides a jumper, which should be used at all times, to connect the system/frame dc common ground in the control unit with frame ground in the drive. Physical specifications of the ground wire used are given in paragraph 1.3.2.

For added safety and to reduce RFI, each cover on a drive is connected to frame ground.

Grounding requirements, satisfied at the factory and applicable to customer installation and maintenance of the drive, are:

- With all side covers installed on the drive and all external connections removed from the drive, logic ground is isolated from frame ground by 2.0 megohms or greater. Logic ground is present at TB500-13 (see paragraph 3.9.3) and all PCBs in the Logic File at pins L1 and L40.
- Resistance between deck plate and logic ground is 0.01 ohm or less.

- Resistance between deck plate and the rotating spindle is 10 ohms or less.
- Resistance between deck plate and each head/arm assembly is 0.1 ohm or less.

### 1.3.1.8 Termination Requirement

All signal lines must be terminated at both ends. Impedances at the drive ends and impedances which must be provided by DEC at the DCL ends are discussed in paragraph 1.3.1.5.

## 1.3.2 Mechanical Interface Specifications

### 1.3.2.1 Connector Locations

External cable connectors are located as shown in Figure 1-21.

### 1.3.2.2 AC Power Connections

The drive has three ac power connections; they are:

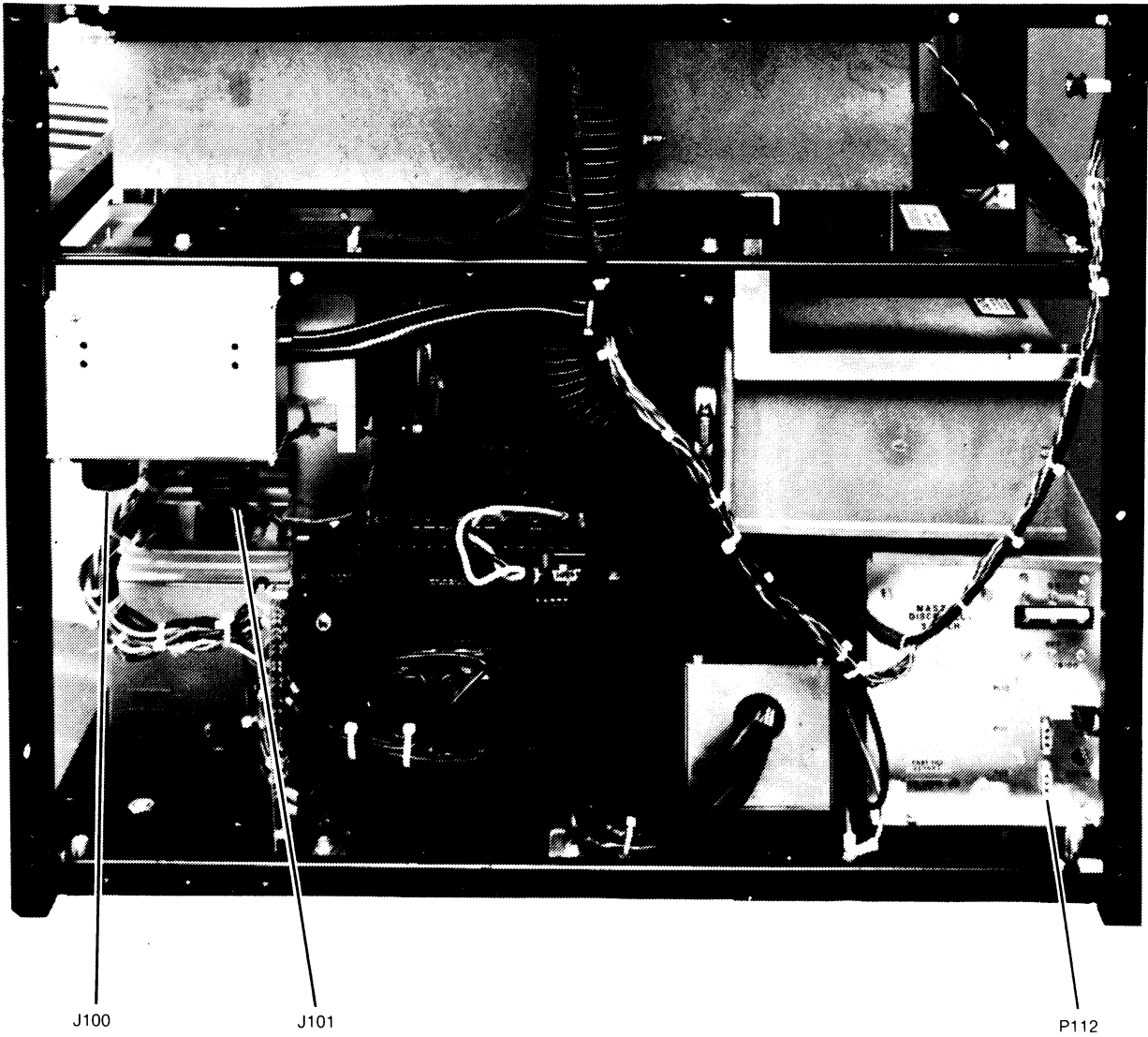
<u>Service</u>	<u>Name</u>	<u>Designation</u>
Facility Power Source to Drive	AC IN	J100
Drive to Drive	AC OUT	J101
Drive to DCL	DCL AC	P112

Connector pin assignments are listed in Table 1-5.

### 1.3.2.3 Signal Connections

MDLI signal inputs are transferred by the DCL to the drive using cables designated as Cable A and Cable B. They are received by the drive at its Input PCB, designated IPUT and located in logic gate position D01. Pin assignments are listed in Table 1-2. All cable conductors not listed in the table are grounds.

Drive signal outputs are transferred by the DCL to the MDLI using cables designated as Cable C and Cable D. They are sent by the drive from its Output PCB, designated OPUT and located in logic gate position D02. Pin assignments are listed in Table 1-3. All cable conductors not listed in the table are grounds.



**FIGURE 1-21. EXTERNAL CABLE CONNECTORS**



**TABLE 1-5. AC CONNECTOR PIN ASSIGNMENTS**

(a) **AC IN Pin Assignments:**

Pin	Drive 60 Hz Model A	Drive 50 Hz Model B
A	Phase A	Phase A
B	Phase B	Phase B
C	Phase C	Phase C
D	Not used	Neutral
E	Not used	Not used
F	Not used	Not used
G	Chassis Gnd	Chassis Gnd

(b) **AC OUT Pin Assignments:**

A	Phase B	Phase B
B	Phase A	Phase A
C	Phase C	Phase C
D	Not used	Neutral
E	Not used	Not used
F	Not used	Not used
G	Chassis Gnd	Chassis Gnd

(c) **DCL AC Pin Assignments:**

1	Phase 1
2	Phase 2
3	Ground

**1.3.2.4 Ground Connection**

The DCL to drive dc ground wire (discussed in paragraph 1.3.1.8) is provided by DEC. The point of connection at the drive is indicated in Figure 1-22.

**Switches**

CONTROL A/  
CONTROL B  
Logical Address Plug  
Lamp Test

**Indicators**

CONTROL A and  
CONTROL B  
READY  
UNSAFE  
STANDBY  
DOOR LOCKED

**1.3.2.5 Termination**

The DCL connected to a drive must electrically terminate the drive signal lines. The required terminator is supplied by DEC.

Operating controls (left column above) consist of four switches and one removable plug. All indicators (right column above) illuminate white, in English words. The mechanical (physical) functions of all controls and indicators are described in paragraph 2.4.

**1.3.2.6 Controls and Indicators**

The control switches and display indicators provided are:

Logical requirements for starting and stopping the drive are discussed in paragraph 1.3.1.4.

**Switches**

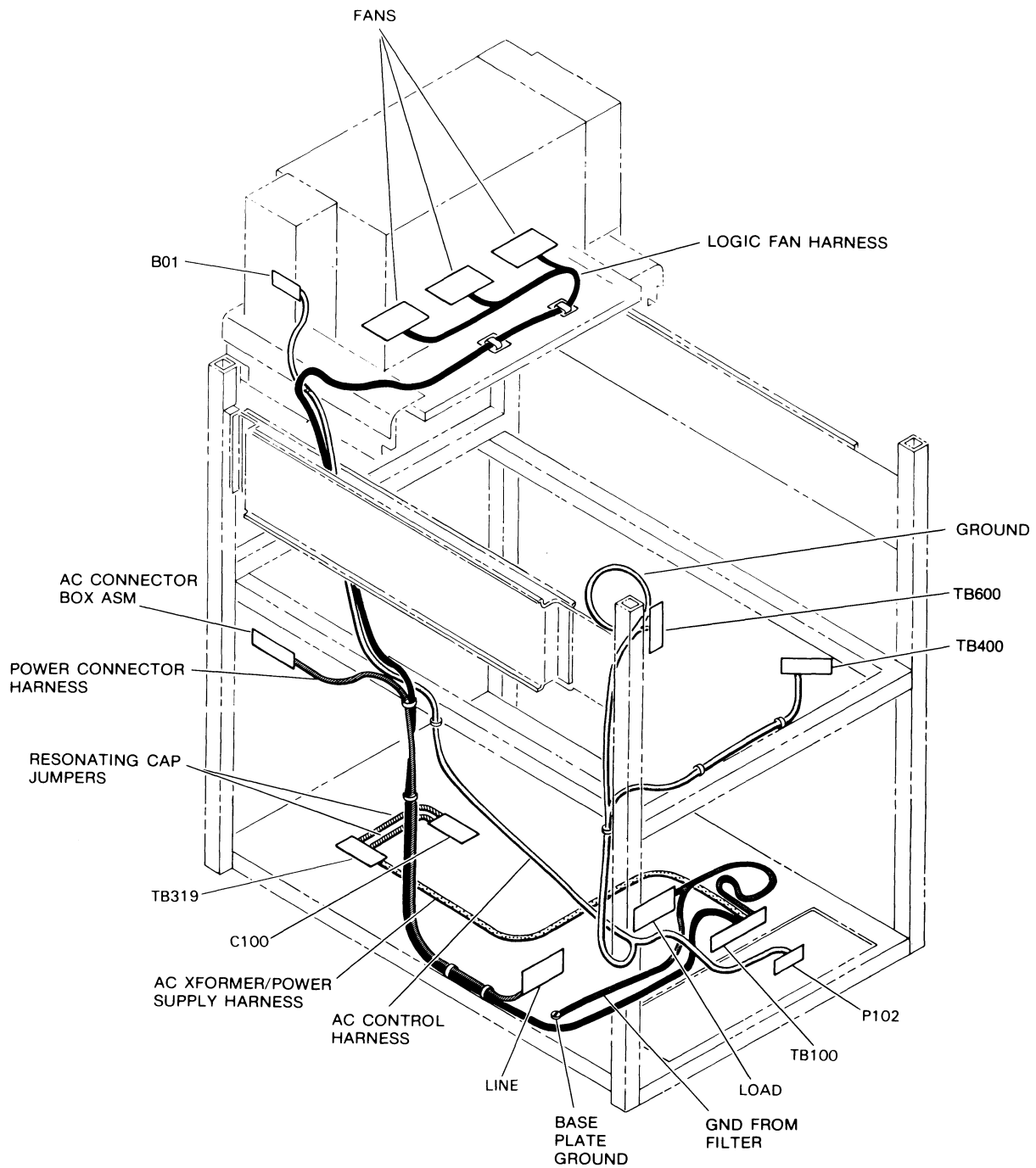
START/STOP  
WRITE PROTECT

**Indicators**

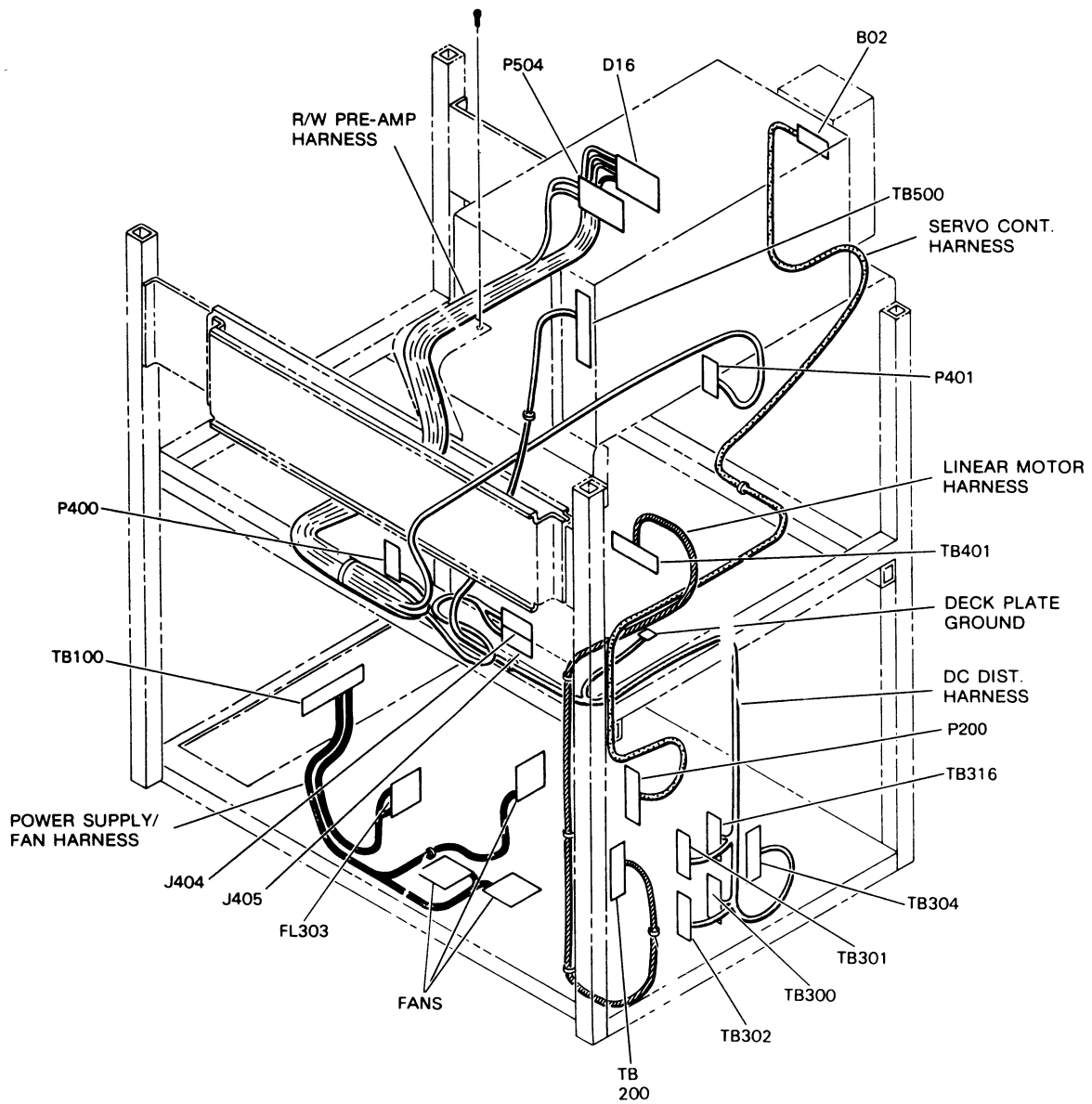
START  
WRITE PROTECT

**1.3.2.7 Cable Routing and Terminal Board Locations**

Drive internal cable routing and terminal board locations are shown in Figure 1-22 (two parts).



**FIGURE 1-22. CABLE ROUTING AND TERMINAL BOARD LOCATIONS (PART 1 OF 2)**



**FIGURE 1-22. CABLE ROUTING AND TERMINAL BOARD LOCATIONS (PART 2 OF 2)**



## SECTION 2 INSTALLATION AND OPERATION

### 2.1 SCOPE AND INTENDED USE

This section contains procedures for installing and operating the 677-01 DEC or 677-51 DEC Disc Storage Drive. It is intended as source material on the drive, to be used by the OEM in developing procedures for system installation and operation.

Memorex recognizes the OEM responsibility for drive installation as an integrated part of system installation, diagnostic verification of the total installation, and personnel assignments for system operation including those for the drive. It is also recognized that drive inputs are required to implement this responsibility; this section responds to the requirement.

The procedures in this section must be examined for agreement with OEM standard practices and supplemented to account for the system involvement with the drive. For example:

- Drive installation procedures exclude coverage of DCL attachment to the drive, and DCL/drive internal and external cabling. These exclusions are necessary because the DCL and all cables are OEM supplied and installed. However, the procedures include indications of when the drive is ready for DCL attachment and cabling.
- System diagnostics must be run on each drive installed. This final step in the installation procedures must be OEM specified and conducted to assure operational status of the drive (as well as the rest of the system). System verification testing will demonstrate correct drive installation and no internal damage to the drive during shipment.
- Drive operating procedures include suggested responses by the operator to abnormal conditions. Although considered suitable to Memorex end users, they should be confirmed as suitable to OEM customer operators.

Whenever the procedures in this section differ from the OEM's standard installation or operating practices, follow the standard practices to obtain the same desired results.

### 2.2 SPECIAL TOOLS AND TEST EQUIPMENT

The following special tools and test equipment (or their OEM equivalents) are needed to perform the installation procedures in paragraph 2.3:

Description	Memorex Part Number
• Digital Voltmeter	203154
• Crescent Wrench (10 inch)	203164
• PCB Extender	011086
• Head Alignment Kit	215970
• CE Disc Pack	320100 (100 MB)
• CE Disc Pack	335001 (200 MB)
• Oscilloscope	Tektronix 453, or equivalent
• 800 Disc Storage Subsystem Tester	215900
• 800 Disc Storage Subsystem Tester	215935 (OPT. head alignment tool available)

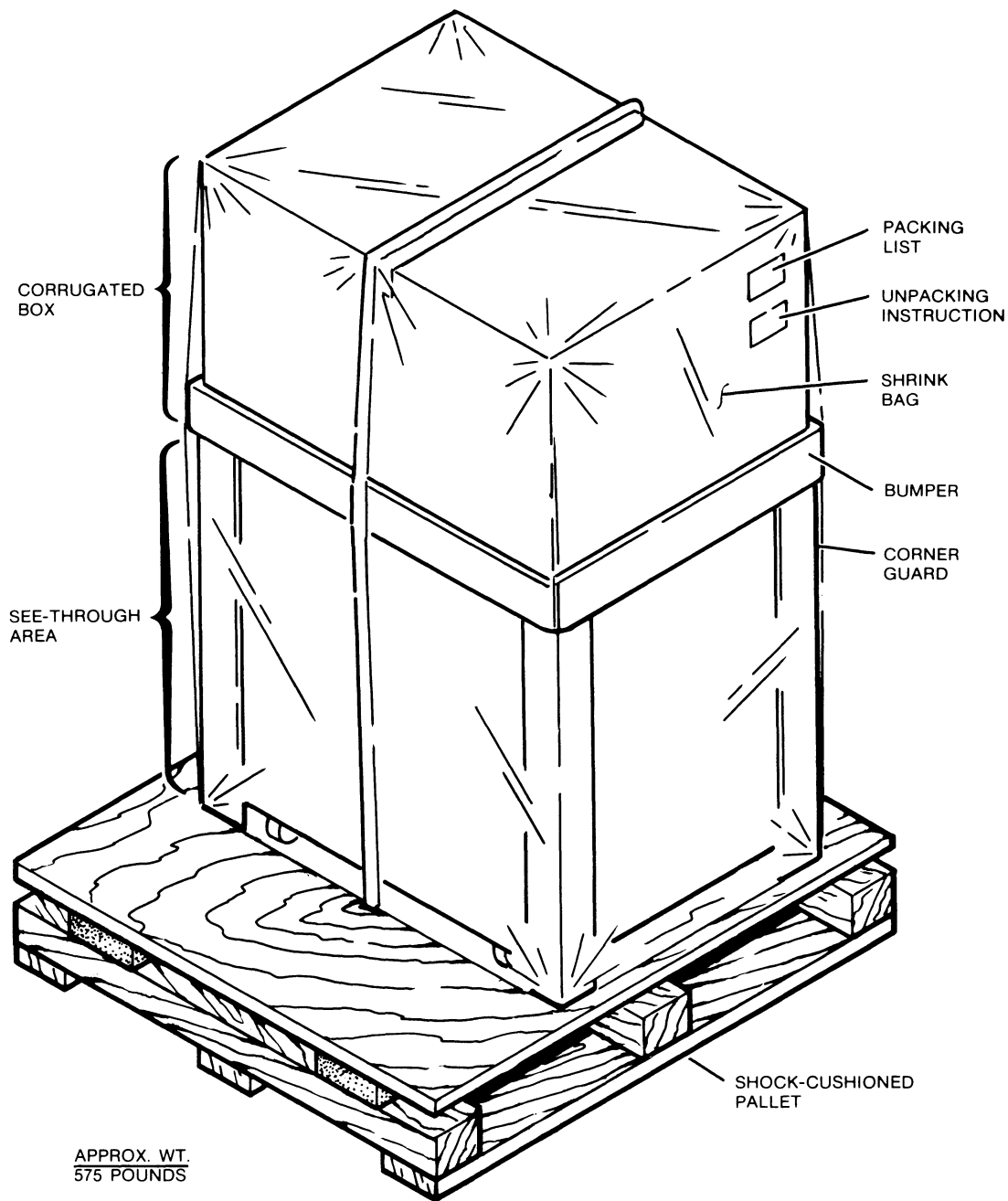
### 2.3 INSTALLATION

#### 2.3.1 Unloading and Moving

A drive is shipped by van or air freight carrier. It is packaged for shipment in accordance with EDP-industry standards and OEM packaging specifications.

The shipping container is shown in Figure 2-1. As indicated in this figure, the container is completely encased in a tight fitting polyethylene bag ("shrink" bag). Side panels on the drive are visible by looking through the transparent bag. Upon delivery, immediately check for panel dents, marks, or scratches. If damage is noted, contact the carrier to make a physical examination of damage. The carrier is required to complete and sign a damage report form.

The shipping container has a shock cushioned pallet (Figure 2-1). A hand-lift truck should be used for removing the container from the carrier and placing it near its operating position. The container must not be laid on its end or side. Tipping or tilting is permissible. Sudden shifts in direction, stops, or dropping must be avoided.



**FIGURE 2-1. SHIPPING CONTAINER**

## 2.3.2 Unpacking

The shipping container provides protection against moisture, dust, and contact damage. To ensure drive preservation, the container should be left unopened as long as possible.

As indicated in Figure 2-1, an envelope containing unpacking instructions is secured to the outside of the shrink bag. These unpacking instructions must be followed to remove all external shipping materials from the drive in a controlled manner, allowing for reuse of materials (except the shrink bag) at some later time for repacking.

For reference purposes only, an exploded view of package installation is shown in Figure 2-2.

## 2.3.3 Mechanical Preparation

### CAUTION

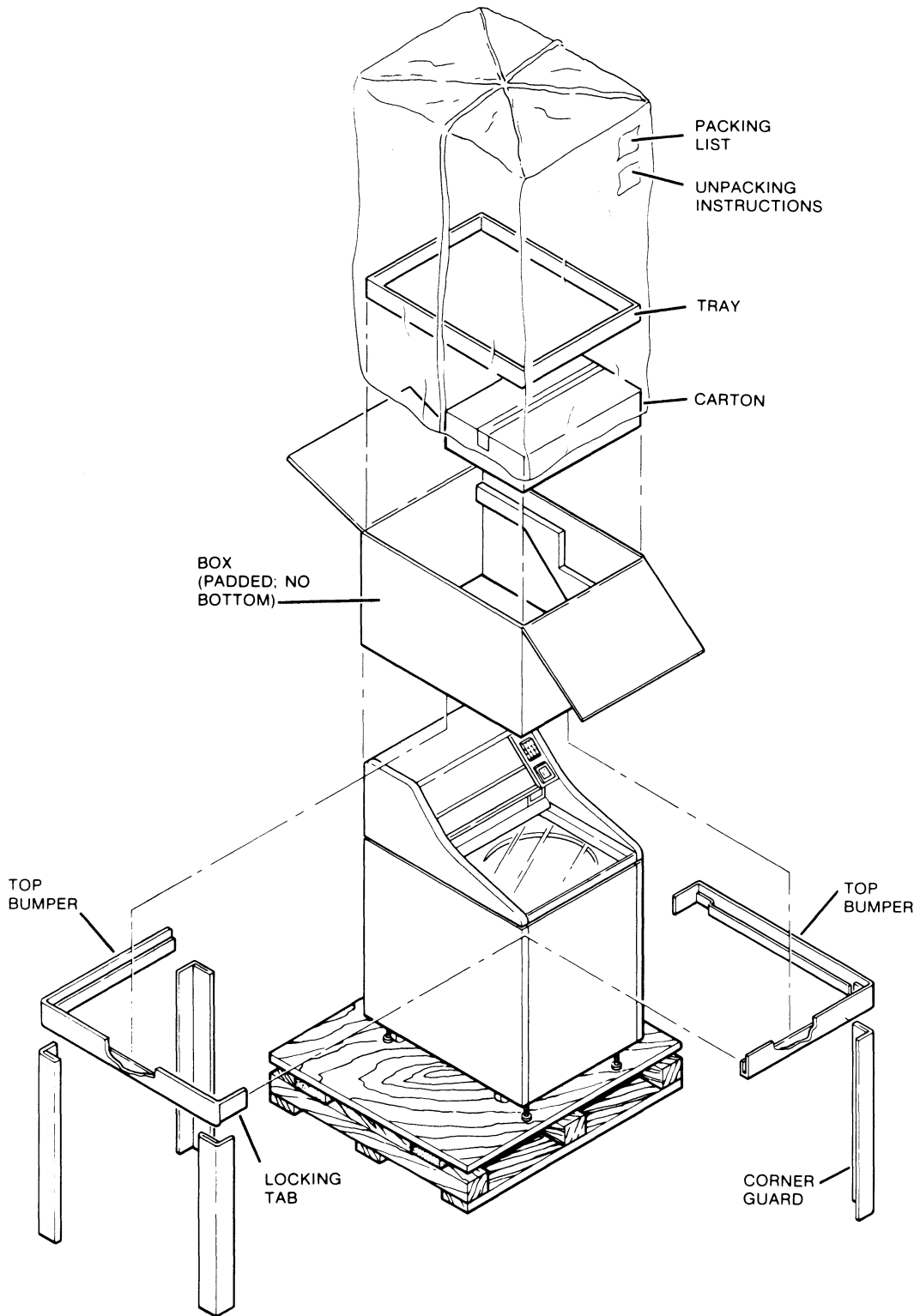
Never place heavy items (shipping box, disc pack, etc.) on top of glass door.

1. Roll the drive to its preassigned floor location.
2. Remove the front and rear covers and set aside. Each cover is removed by opening the cover, pulling the quick-disconnect ground lug (near top hinge), and lifting the cover off its hinges.
3. Remove the side cover and set aside. The cover is removed by slowly raising the cover until the brackets disengage, then removing the ground lug.
4. Inspect interior of drive for loose connections on terminal boards and frame grounds.

## 2.3.4 Shipping Hardware Removal

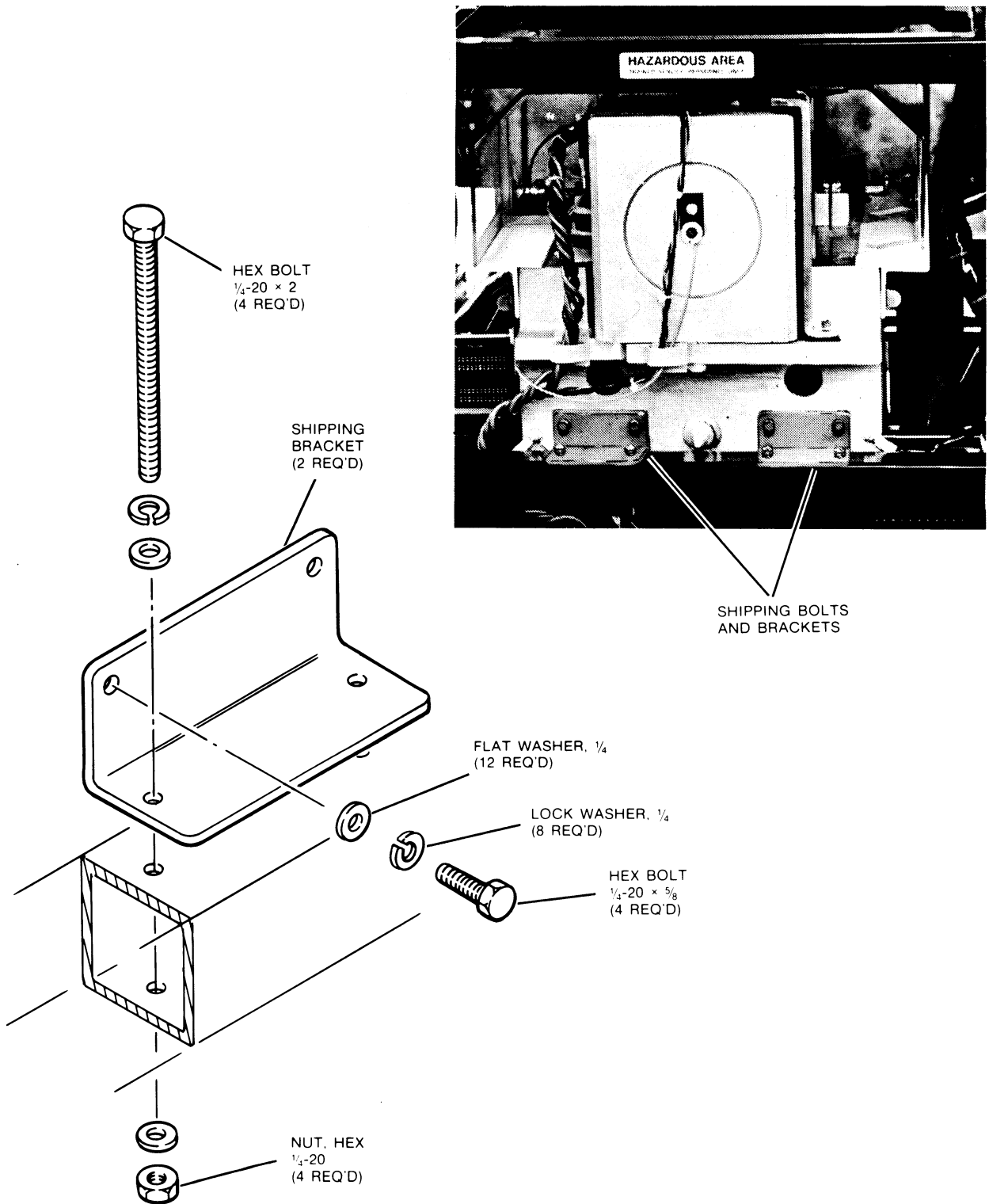
For protection against vibration and shock loading during transportation, the interior of the drive contains shipping hardware which must be removed. If the drive is operated with shipping hardware in place, **serious equipment damage can occur**. Do not reverse and reinstall shipping brackets; remove them completely. Retain all shipping hardware removed for future use. Remove the shipping hardware as follows:

1. Remove two brackets from rear of the deck plate and frame (see Figure 2-3).
2. Provide room for accessing other shipping hardware (Steps 3 and 4 below) by removing the absolute filter (Figure 2-4). To remove the filter, reach through the left side of the drive with a screwdriver and remove the hose clamp at the rear of the filter, then slide the filter out.
3. Remove two bolt/washer/spacer sets from the area between the frame and deck plate (see Figure 2-5).
4. Remove the heavy support bar by pushing out from the side (see Figure 2-5).
5. Replace the absolute filter. Clamp the hose to the rear of the filter.
6. Remove the tape that is wrapped around the disc pack locking rod and the slotted post (see Figure 2-4).
7. Remove two strips of tape securing the wind tunnel (plastic deflector) to the deck plate. To access the wind tunnel, swing open the drive's rear cover.
8. Remove shipping block on linear motor (see Figure 2-6).

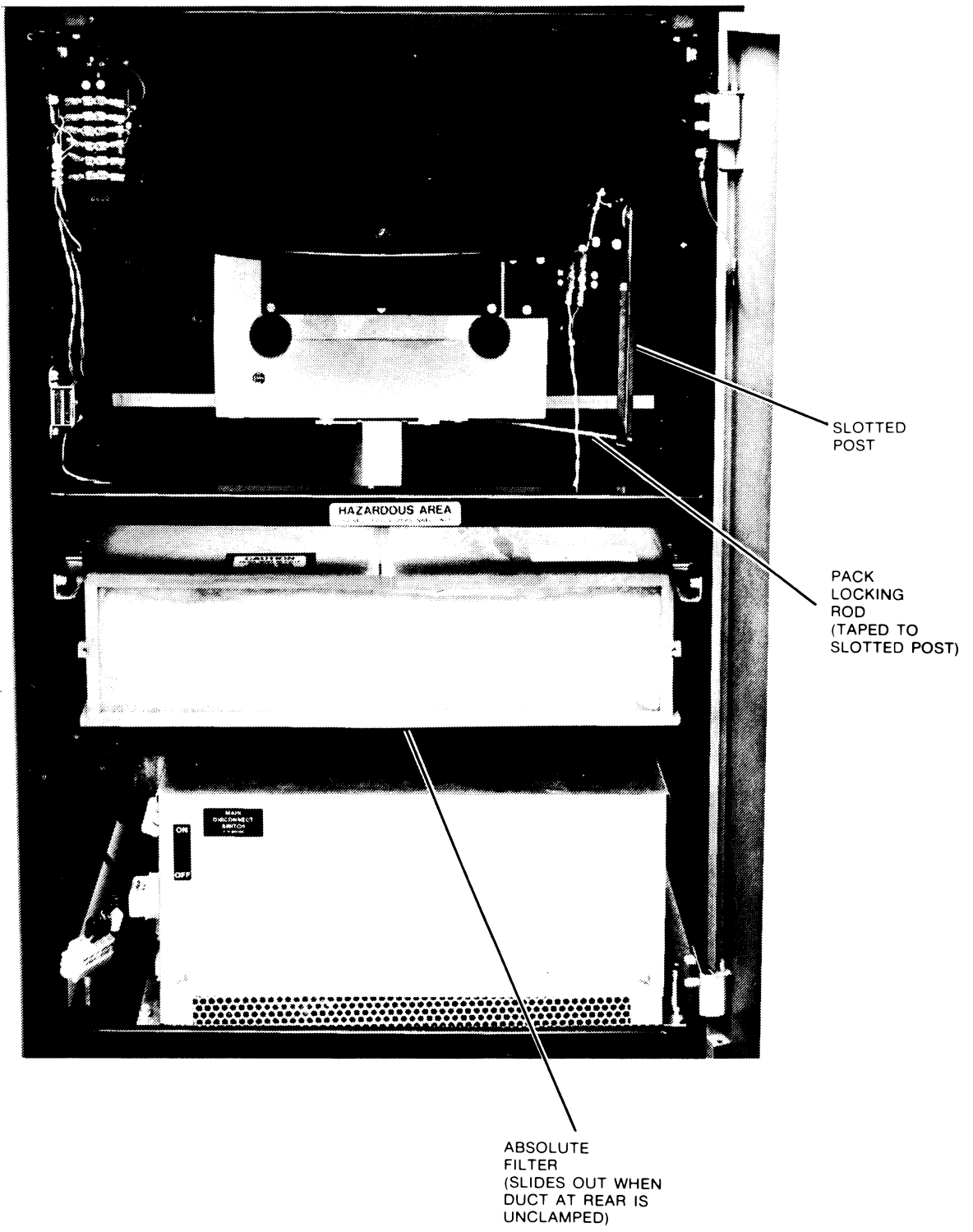


**FIGURE 2-2. SHIPPING CONTAINER DESIGN**

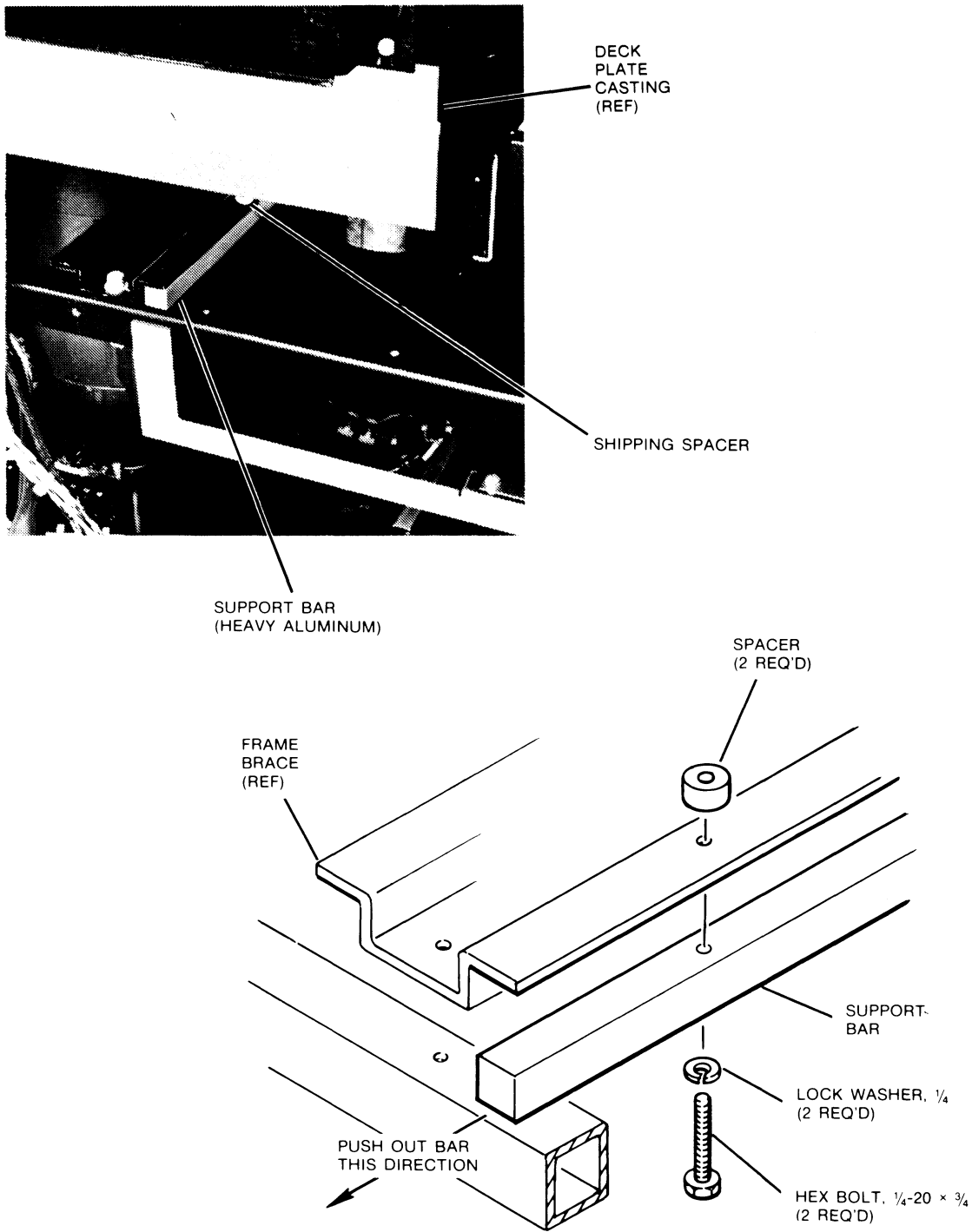




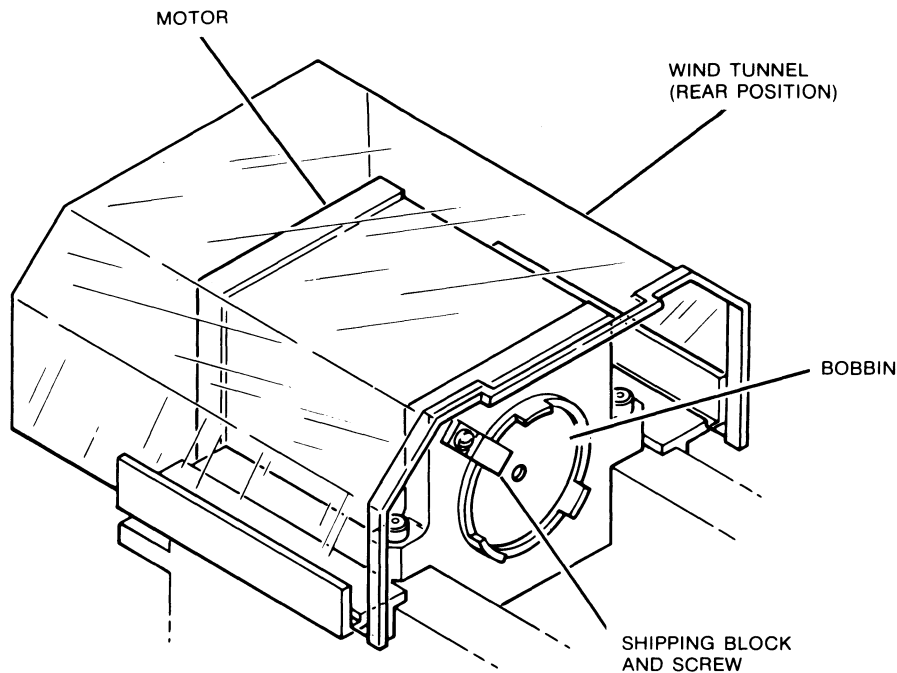
**FIGURE 2-3. SHIPPING BRACKETS**



**FIGURE 2-4. ABSOLUTE FILTER AND PACK LOCKING ROD**



**FIGURE 2-5. SHIPPING SPACERS AND SUPPORT BAR**



**FIGURE 2-6. LINEAR MOTOR SHIPPING BLOCK**

### 2.3.5 Terminal Board Checks

Check terminal boards and associated connectors, cables, and hardware for tightness (no loose connections) and broken components or wires, as follows:

1. For access into the power supply, its cover must be removed by loosening two screws (in open slotted holes) down the left side, removing two screws down the center, then pulling out.
2. Check TB304 located on the front of the power supply, at the rear of the drive (see Figure 2-7).
3. Check four regulator PCBs, located in the power supply (see Figure 2-7).
4. Check TB200 on the servo power amplifier (see Figure 2-7).
5. Check terminal boards in the power distribution unit, located at the front of the drive (see Figure 2-8). To access into the PDU, its cover must be removed by removing two screws and lifting

out; the cover's rear edge has a plastic lip that slides under a bracket in the housing.

6. Replace PDU cover removed in Step 5.

### 2.3.6 Power Configuration Check

#### 2.3.6.1 60 Hz Drive

1. Verify that the Power Conversion Plug Assembly P/N 215766 (shown in Figure 2-8 and in *Illustrated Parts Catalog*, Figure 2-83) has the PHASE TO PHASE connector installed (shown as P110 in *Logic Manual*, page ZA100) regardless whether source is WYE or DELTA.
2. Determine the phase-to-phase voltage of the power source, and move power supply leads to appropriate terminals of TB319 on transformer (refer to *Logic Manual*, page ZD100).
3. Replace power supply cover removed in paragraph 2.3.5, Step 1. **Do not use excessive force on the self-tapping screws.**

### 2.3.6.2 50 Hz Drive

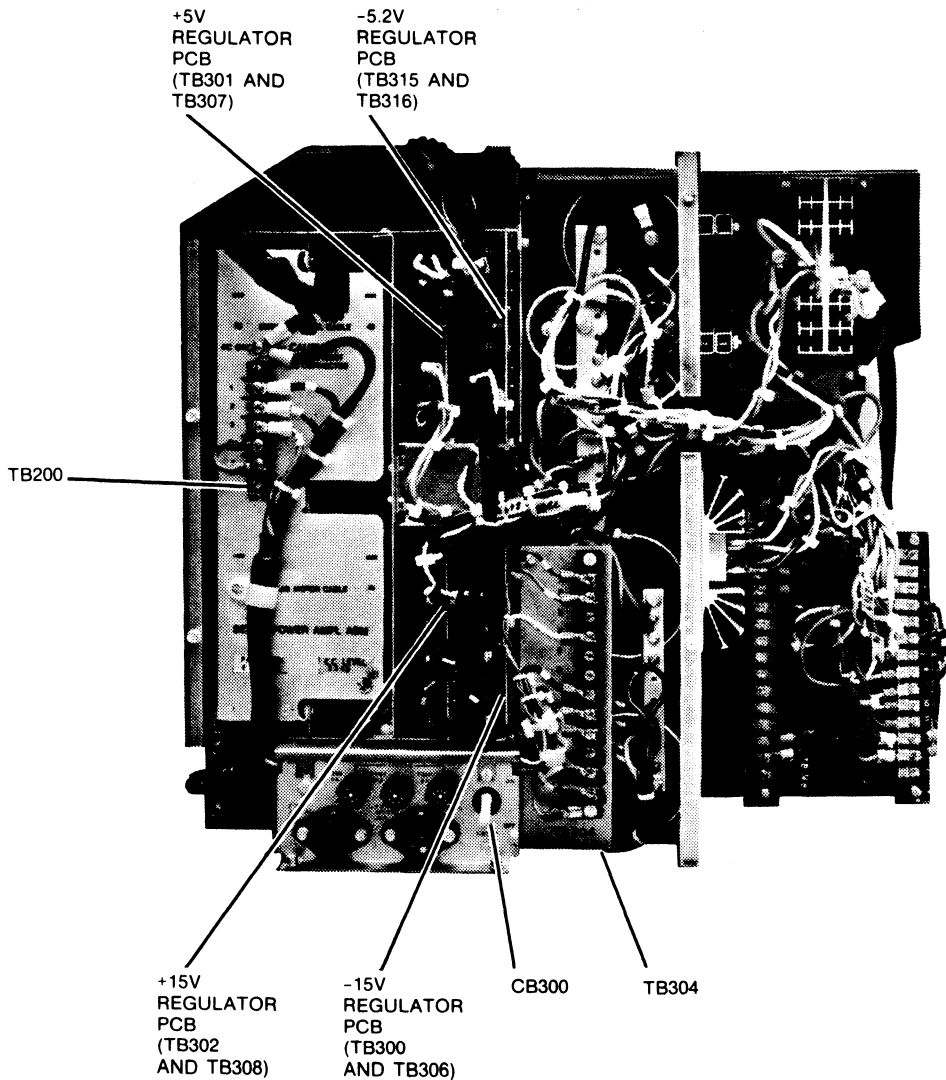
1. Determine if power source is WYE or DELTA configured. Locate the Power Conversion Plug Assembly P/N 215766 (shown in Figure 2-8 and in *Illustrated Parts Catalog*, Figure 2-83). If source is DELTA, install the PHASE TO PHASE plug. If source is WYE, install the PHASE TO NEUTRAL plug. (Refer to P110 in *Logic Manual*, page ZA100.)
2. Determine the phase-to-phase voltage of power source if DELTA configured, or the phase-to-neutral voltage if WYE configured, and move

power supply leads to appropriate terminals of TB319 on transformer (refer to *Logic Manual*, page ZD100).

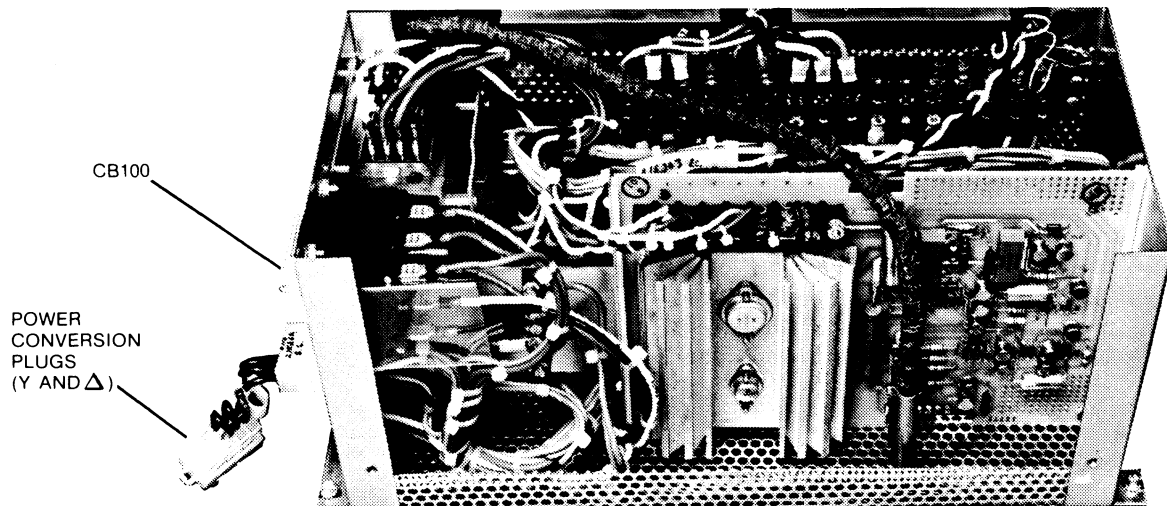
3. Replace power supply cover removed in paragraph 2.3.5, Step 1. **Do not use excessive force on the self-tapping screws.**

### 2.3.7 Grounding Check

Verify greater than two megohms resistance between the ground terminal on TB304 (Figure 2-7) and the frame.



**FIGURE 2-7. REAR VIEW, POWER SUPPLY COVER OFF**



**FIGURE 2-8. FRONT VIEW, PDU COVER OFF**

### 2.3.8 Prepower Checks

Before power is applied to a drive, the power source voltage should be checked against specifications (Table 1-1).

#### NOTE

At this stage in the installation procedure, the following activities should be performed using OEM supplied procedures:

- a. Connection of cables between drive and DCL; bolting the two units together; and installing a cover (previously on a drive) onto the DCL as shown in Figure 2-9.
- b. Installation of all system cables.

### 2.3.9 Power On Checks

When prepower checks are completed and units in the system are interconnected, perform ac and dc power checks for the drives.

Perform ac power checks as follows:

1. Set CB100 on the PDU to ON (see Figure 2-8).
2. Verify that three fans, located under the logic gate, are operating.

3. Repeat Steps 1 and 2 above for each drive.

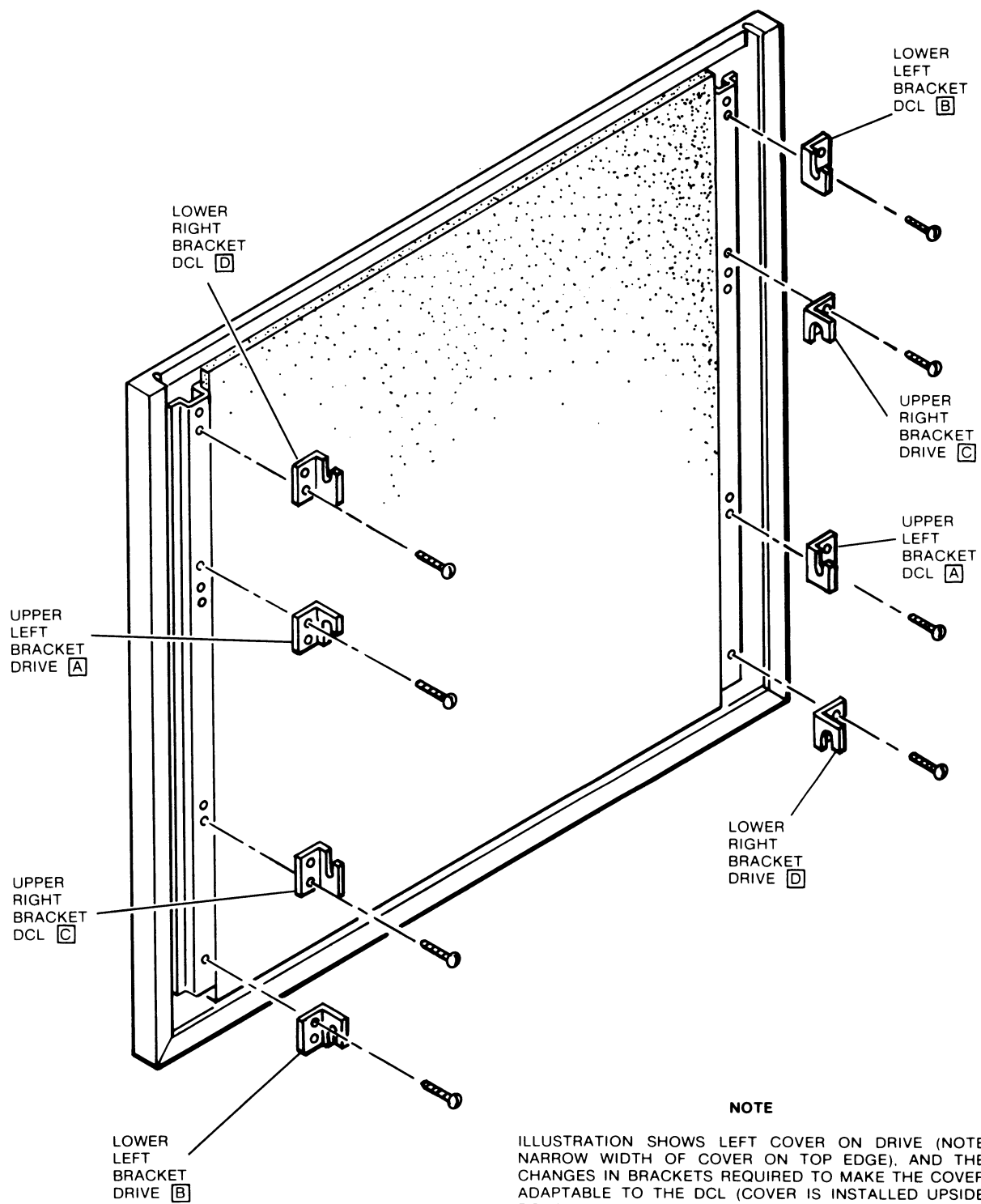
Perform dc power checks as follows:

1. Set CB300 on the power supply to ON (see Figure 2-7).
2. Momentarily press LAMP TEST on the operator panel. Verify that all indicators are illuminated.   
*OF LOGIC AREA*
3. Using a digital voltmeter, measure voltages at the back panel and compare against specifications below. With one exception (noted below), the measurement locations are etched onto the back panel itself, using their nominal voltage values. If necessary, adjust these voltages as instructed in paragraph 4.5.3.

Minimum	Nominal	Maximum	
+ 4.9	+ 5	+ 5.2	
- 5.3	- 5.2*	- 5.1	
+14.7	+15	+15.3	
-15.3	-15	-14.7	
+19.0	+24	+29.0	} Not Adjustable
> +45.0	+50	+55.0	
- TB304-1 (FUSED +50V)			

\*At TB500A terminal #3, not marked as - 5.2

4. Repeat Steps 1 through 3 above for each drive.



**FIGURE 2-9. CONVERTING DRIVE COVER TO DCL COVER**

### 2.3.10 Readiness Tests

Prepare for readiness testing and conduct the tests as follows:

1. Inspect and clean (as required) all heads in the drive. Refer to paragraph 4.6.1 for the procedure to be used.
2. Mount a scratch disc pack on the drive. Remove the Logical Address Plug from the operator panel (see NOTE below). Press START/STOP switch to START. Allow the drive to come up to speed and purge for 5 minutes. With LAP removed and without a first launch, hand load heads very carefully. Check for binding or unusual noise that may indicate head-to-disc interference (HDI); refer to paragraph 2.4.5.3 for clues on HDI detection. If HDI is present, turn the drive off and investigate the problem. Install any numbered LAP; this will allow the heads to launch to Track 000. Remove and reinstall LAP. Drive should do a rezero. Otherwise, leave power on and proceed to Step 3 below.

#### NOTE

Logical address plugs on 677-01 DEC drives are removable by simply pulling out. Before plugs on 677-51 DEC drives can be removed in similar fashion, clips at the rear of the plugs (preventing their removal) must be disengaged.

3. Verify the capability of the drive to execute a seek operation. If the Memorex offline tester is to be used, refer to its User's Guide manual for instructions.
4. Perform the head alignment procedure using the offline tester (see Note c below if tester not available). Before starting head alignment, be sure to allow 30 minutes for thermal stabilization of drive and pack.
5. Repeat Steps 1 through 4 above for each drive.

#### NOTE

At this stage in the installation procedure, the following activities should be performed using DEC supplied procedures:

- a. Verification of correct system cabling and signal termination in the DCL.

- b. System diagnostics, verifying the presence of an operational condition in each drive.

- c. System head alignment procedure using system diagnostics.

### 2.3.11 Leveling

Lower the four leveling jacks under each drive (and the leveling jacks under its attached DCL) such that all units are parallel to the floor, giving a uniform appearance upon sighting down the front and rear top edges of adjacent drives. Tighten the lock nuts on all leveling jacks.

### 2.3.12 Covers and Kickplates

1. Install front and rear covers on each drive.
2. For the one DCL at the left, and the one drive at the right, install a side cover (see Figure 2-9) and a kickplate (using two #8 screws each).

#### NOTE

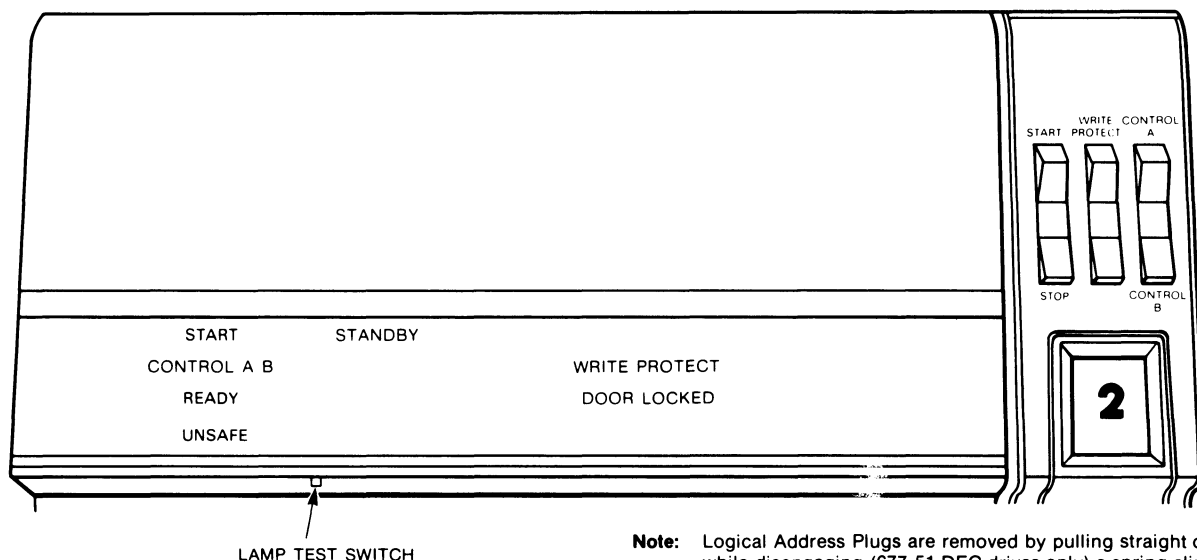
When the steps given in paragraphs 2.3.1 through 2.3.12 - supplemented by DEC procedures as indicated by the notes within these paragraphs, have all been successfully completed, the drives in the system are ready for operational use.

## 2.4 OPERATION

### 2.4.1 User Information

All controls and indicators needed for efficient operation of the drive are located in a single panel designed for use by nontechnical personnel. Names of individual controls (OEM specified) are descriptive of their functions and are printed onto the panel. Indicators illuminate white with English words (OEM specified) that identify the condition existing in the drive. One indicator, the word UNSAFE, will illuminate when a malfunction is present. The normal response is to position the START/STOP switch to STOP and request maintenance.





**FIGURE 2-10. OPERATOR PANEL**

## 2.4.2 Operator Controls

Functions of individual controls in the drive's Operator Panel (Figure 2-10) are described below.

- **START/STOP.** This is a three-position rocker switch. When pressed to the START position and released, the switch returns to its center position. When pressed to the STOP position, it remains in the STOP position. With the pack access door closed and all interlocks satisfied, pressing the switch to START locks the pack access door and initiates a drive power-up sequence. When the pack reaches operating speed, the heads are extended and loaded. When the switch is pressed to STOP, the carriage moves in a reverse direction to pull the heads out of the pack area. Electrodynamic braking power is applied to stop pack rotation, and when stopped the pack access door is unlocked. Starting or stopping time is approximately 20 seconds. When pressed to the START position, STANDBY will be reset if it was true (see STANDBY description in paragraph 2.4.3). If left in the center position and sequence conditions are satisfied, the drive will initiate a power-up sequence when ac power is applied or restored.
- **WRITE PROTECT.** With this two-position rocker switch in the WRITE PROTECT position,

data stored on a disc pack is protected against accidental over-write. The normal position is off. With the switch in the WRITE PROTECT position, the write function of the drive is inhibited, providing the drive was not writing at the time the switch was engaged. If the switch is engaged while the drive is writing, the inhibit function will operate after the drive stops writing. With the switch in the off position, the reading or writing function of the drive is permitted. If both functions are commanded simultaneously, heads are deselected and both reading and writing are disabled.

- **CONTROL A/CONTROL B.** CONTROL A forces the PORT A LOCKED line on the MDLI to a true level. CONTROL B forces the PORT B LOCKED line to a true level. In the center position, both lines are false.
- **Logical Address Plug.** This removable plug permits changing the logical address of a drive by simply changing the plug. Recabling is not necessary. Plugs are factory configured to designate the individual drives in the system (maximum of 9 plugs including 1 service). Plugs are labeled to indicate drive designations ("0" through "7" and "S"). Two identical plugs are not used on drives attached to the same controller.

- **Lamp Test.** This momentary switch provides illumination of all panel indicators for checking purposes.

### 2.4.3 Operator Displays

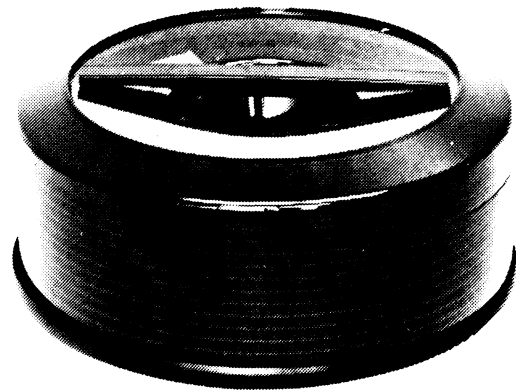
Functions of individual indicators in the drive's Operator Panel (Figure 2-10) are described below.

- **START.** This word illuminates when the START/STOP switch is set to START and all start conditions are satisfied, and remains illuminated until the drive is stopped.
- **CONTROL A/B.** This word and letters A and B illuminate to indicate the state of the PORT A LAMP and PORT B LAMP lines.
- **READY.** This word illuminates when the drive is on line.
- **UNSAFE.** This word illuminates to indicate a drive malfunction that requires the attention of service personnel. Illumination occurs when either an abnormal-stop or read/write safety error occurs.
- **STANDBY.** This word illuminates to indicate the drive is in the standby mode. Illumination appears when a command to place the drive in standby mode is implemented in the drive circuitry. When in the standby mode, starting the drive is accomplished by setting the START/STOP switch to START, which starts the drive providing: conditions permitting the initiation of a power-up sequence exist while no other drive is in process of powering up, and a disc pack is installed and the access door closed. With these starting conditions satisfied, pressing START causes STANDBY to disappear.
- **WRITE PROTECT.** These words illuminate when the WRITE PROTECT switch is in the WRITE PROTECT position.
- **DOOR LOCKED.** These words illuminate to indicate the pack access door is seated and locked closed. For personnel safety, pack rotation can begin only when this indicator is illuminated. If the door is forced open during drive operation, pack rotation will commence stopping and the heads will be retracted out of the pack automatically. Normal sequence down will take place under this condition.

## 2.4.4 Normal Operating Procedures

### 2.4.4.1 Handling the Disc Pack

The Memorex disc pack (Figure 2-11) is protected during shipping by a special plastic foam container. When the pack is received, examine the container for damage. If the condition appears acceptable, remove the pack and store the container for later use. If the container or pack is damaged, retain the combination in an "as received" condition and notify Memorex.



**FIGURE 2-11. MARK X OR XI DISC PACK**

A two-piece plastic cover protects the disc pack from dust and moisture when the pack is stored. The top section of the cover contains a handle for carrying the pack. This top cover is never left on a pack that is installed into a drive.

When transporting disc packs:

1. Be sure the pack is securely fastened in its two-piece cover.
2. Use only the specially designed shipping container.
3. Handle the pack only with its top cover on. If the pack is accidentally dropped or receives a sharp impact of any kind, have it inspected by service personnel before using.

For identification purposes, a plastic labeling surface is placed on the center area of the disc pack. When labeling:

1. Use a pen or felt-tip marker that does not produce residue. DO NOT use a lead pencil. Microscopic lead particles can damage disc surfaces and heads.
2. Write on the label before it is applied to the disc pack.
3. Place the label only on the center area.
4. Use a new label if changes are necessary. NEVER ERASE a label that is on a pack. Microscopic eraser particles can damage surfaces and heads.
5. Removal or placement of labels can be done only when the pack is installed. DO NOT attempt to remove the top cover when the pack is not installed onto the drive's spindle.

To ensure maximum disc pack life and reliability:

1. Each pack should rest flat on a shelf when storing, not on edge or another pack.
2. Store in a computer room environment. If a pack must be stored in a different environment, allow two hours for temperature adjustment within the computer room before using.

#### **2.4.4.2 Disc Pack Installation and Removal**

A disc pack can be installed when main power to the drive is off, or provided the spindle is stopped.

1. If the spindle in the drive is stopped (both START and READY not illuminated), go directly to Step 4; otherwise perform Steps 2 and 3 before Step 4.
2. Press the START/STOP switch to the STOP position. This event will cause the START illumination to disappear.
3. Wait approximately 20 seconds, until the DOOR LOCKED illumination disappears, indicating the spindle dynamic braking is complete and the pack access door is unlocked.
4. Open the glass access door by sliding it all the way to the rear of the drive.

5. Remove pack (if present) by performing Steps 14 through 16.
6. Remove the bottom cover of the disc pack to be installed by pressing the two handles on the bottom cover together.
7. Place the disc pack, together with its top cover, on the spindle carefully and slowly.
8. Turn the handle on the top cover in a clockwise direction until it comes to a full stop.
9. Lift the top cover straight up from the pack, carefully to avoid hitting the edges of the discs.
10. Place the top cover on the bottom cover to create a positive dust seal, and store.

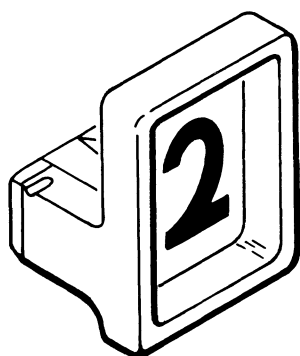
#### **NOTE**

Without the disc pack inside, the top and bottom covers are not attachable together.

11. Close the glass access door by sliding it all the way to the front of the drive. The access door should always be left closed to prevent contamination.
12. To remove a disc pack, perform Steps 13 through 17.
13. Make sure spindle is stopped. Open the glass access door by sliding it all the way to the rear of the drive.
14. Lower the top cover straight down over the pack, carefully to avoid hitting the edges of the discs. Turn the handle on the top cover in a counterclockwise direction two full turns.
15. Using the handle, remove the pack from the drive.
16. Immediately attach the bottom cover to the pack, and store.
17. Close the glass access door by sliding it all the way to the front of the drive. The access door should always be left closed to prevent contamination.

### 2.4.4.3 Drive Address Assignment

1. The Logical Address Plug determines the drive's assigned address.
2. To change the address, verify the system is idle before removal of the Logical Address Plug.
3. Remove the Logical Address Plug (Figure 2-12) from the drive's Operator Panel.
4. Insert the appropriately-numbered Logical Address Plug into the panel's plug socket by simply pushing straight in.



**FIGURE 2-12. LOGICAL ADDRESS PLUG**

### 2.4.4.4 Spindle Motor Start/Stop

To start the drive spindle motor, press the START/STOP switch to START. The drive will sequence to the ready state approximately 20 seconds later, at which time the word READY illuminates. The information below covers both the actual starting procedure and the prerequisites to starting.

1. Be sure a Logical Address Plug is installed, a disc pack is installed, and the glass access door is closed.
2. Verify all indicators light by pushing the Lamp Test switch. This also indicates main power is applied to the drive. If an unsafe condition has been detected (UNSAFE is illuminated), go to paragraph 2.4.5.1 to clear this condition, and if cleared go to Step 3. If the unsafe condition persists, request maintenance.
3. Press the START/STOP switch to the START position. When pressed, the following events occur: START illuminates, pack begins rotating, and DOOR LOCKED illuminates. If DOOR LOCKED does not illuminate, close the door fully.
4. Wait approximately 20 seconds until the word READY illuminates. It indicates the drive is started and ready to execute commands. START and DOOR LOCKED will remain illuminated.

To stop the drive spindle motor, press the START/STOP switch to STOP. When pressed, the READY and START lamps are extinguished and the drive retracts heads. The DOOR LOCKED illumination disappears approximately 20 seconds later, when the motor-down sequence is completed.

### NOTES

- a. When the START/STOP switch is set to STOP, dynamic braking power is applied to the spindle motor. Approximately 20 seconds later the door is unlocked (and the DOOR LOCKED lamp is extinguished) to allow pack removal.
- b. The system can stop the drive motor by issuing a command to place the drive in standby mode. Whether stopped by system or Operator, the resulting status of indicators is the same, with the exception that the system illuminates STANDBY.

## 2.4.5 User Responses to Abnormal Conditions

### 2.4.5.1 Clearing an Unsafe Condition

If a sequence malfunction occurs during a start operation, an unsafe condition will occur (UNSAFE is illuminated) and the drive will automatically perform an abnormal stop sequence. At the end of the stop sequence, the spindle should come to a complete stop. To restart the drive, clear the unsafe condition by pressing START. UNSAFE should disappear; if not, service personnel should be advised that the drive cannot be restarted. If UNSAFE disappears the drive will then perform its normal starting sequence. If UNSAFE reoccurs, the abnormal stop sequence will perform again automatically; in this event press STOP and advise service personnel.

#### NOTE

Anytime the stop sequence malfunctions, as indicated when the spindle does not stop at the end of the sequence, advise service personnel and do not attempt other operations. If it is necessary to remove ac power from the drive, **first** manually unload the heads.

### 2.4.5.2 Removing a Pack With No Drive Power

To remove a pack from a drive with no ac power applied:

1. Verify that the spindle is stopped and the heads are retracted.
2. Pull open the drive's front cover. Referring to Figure 2-13, locate the door lock override mechanism; it is an arm protruding from the door lock solenoid. Press the mechanism downward, and while holding down, push the door and start sliding it toward the rear. Release the mechanism and push the access door all the way back.
3. Remove the pack using the normal pack removal procedure (paragraph 2.4.4.2, Steps 13 through 17).

4. Close the drive's front cover.

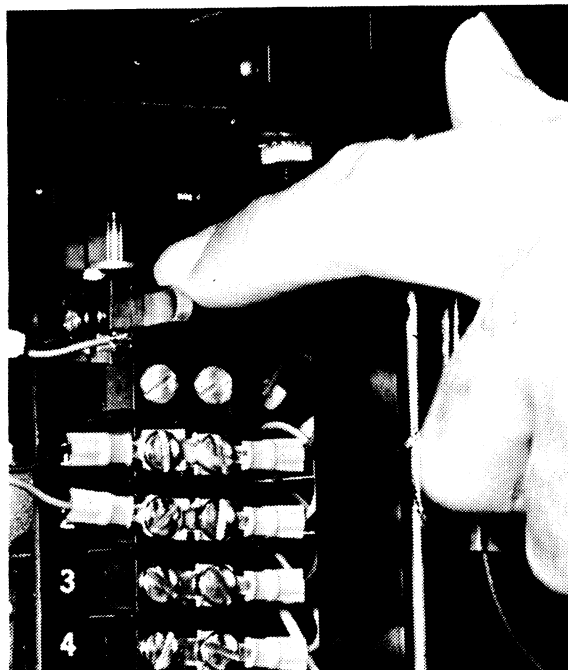


FIGURE 2-13. DOOR LOCK OVERRIDE MECHANISM

### 2.4.5.3 Detecting Head-to-Disc Interference

HDI results from head contact with a disc surface. Usually a foreign particle in the air stream or a protrusion from the disc surface causes the head to break through the air "bearing" and abrade the disc surface. If the problem is not totally corrected, it will have a propagation effect from pack to pack and, in turn, drive to drive. Try to recognize the following symptoms of HDI:

1. Sudden hard read errors.
2. Black contamination on flying surface of any head.
3. UNSAFE during a write operation.

4. Uncommon noise from the disc, characterized by audible tinkling, zinging, or scratching sounds. If allowed to continue, the noise will progress to a screech.

If any symptom above is exhibited:

1. Stop the drive immediately and contact service personnel.
2. Unless absolutely necessary, do not remove the suspected pack from the drive.

#### **CAUTION**

- a. If the suspected pack is replaced with another pack and the drive operated, or the suspected pack is used in another drive, damage to either the second drive or the substituted pack will occur.**
- b. All packs and drives being used when HDI symptoms are exhibited must be checked for HDI by service personnel.**

## **2.5 REMOVAL**

### **2.5.1 Preparation**

To remove the drives from a system installation:

1. Stop the drives and remove the disc packs.
2. Switch all circuit breakers on the drives and attached DCLs to OFF.

3. Disconnect all external cables to the drives.
4. Remove all kickplates, and raise all leveling jacks on the drives.

### **2.5.2 Shipping Hardware Installation**

Prepare for packaging as follows:

1. Install two shipping bracket assemblies (see Figure 2-3). Shipping bracket is Memorex ID/N 500200058.
2. Unclamp the hose from the air duct behind the filter, then remove the filter by sliding out.
3. Install two spacers per deck plate (see Figure 2-5). Spacer is Memorex ID/N 500200563.
4. Install the support bar (see Figure 2-5). Support bar is Memorex ID/N 500200541.
5. Replace the filter and attach the air hose with the clamp.
6. Secure with tape (half-inch filament reinforced tape) all areas where tape was removed during unpacking.

The drives are now ready to be moved from the computer room floor and packaged for shipment using DEC packaging procedures. Except for the shrink bag, all external packaging materials used in delivering the drives are reuseable.

## SECTION 3 PRINCIPLES OF OPERATION

### 3.1 CONTENTS AND INTENDED USE

SECTION 3 contains descriptions of major elements in the 677 OEM Disc Storage Drive, explaining operating principles and theory as applied in the drive to satisfy functional requirements. These descriptions are intended for use as instructional material.

SECTION 3 is one source of information useful in failure analysis; additional sources are contained in the appendices and VOLUME II of this manual.

SECTION 3 contains descriptions of the major electronic, electrical, and mechanical elements in the drive, explaining their operating principles and theory. These descriptions are organized in a way that emphasizes the functional approach used, as discussed below.

- The drive's major elements are grouped into "systems." Each system is identified by "top level" functions which reflect fundamental capabilities. Examples are: Operator Control System, Servo System, DCL Support System, and Read/Write System. Elements in a particular system are selected on the basis that they operate to support the designated system functions.
- Once a system is defined, it is explained in terms of what it does for the user, not just for the drive.

- At this point in the description of a system, its elements are described separately. "Second level" block diagrams of logic and other pictorial information are used extensively. For the case of system elements which are PCBs, the diagrams provided are correlated directly with individual Memorex Engineering Logic Diagrams in VOLUME II of this manual which can be used to obtain "third level" details.
- As the functional descriptions proceed through two levels of detail, the major performance requirements satisfied at the factory are presented to support and extend the descriptions. When requirements of signal lines are presented, signal PCB/pin locations are given.
- Conventional logic standards, abbreviations, and symbology are used throughout.

Figure 3-1 identifies the systems in the drive, and the elements assigned to each system.

#### NOTE

The equipment used by Memorex in PCB acceptance testing includes: Tektronix Type 454 scope, General Radio Model 1192 frequency counter, 0.1% digital voltmeter, Lambda Type LPD 422 FM power supplies, Wavetek Model 144 function generator, and North Hills Electronics Model 0300 BB differential wideband transformer. Scope probes are 10:1 attenuation with 7 pf maximum for all measurements.

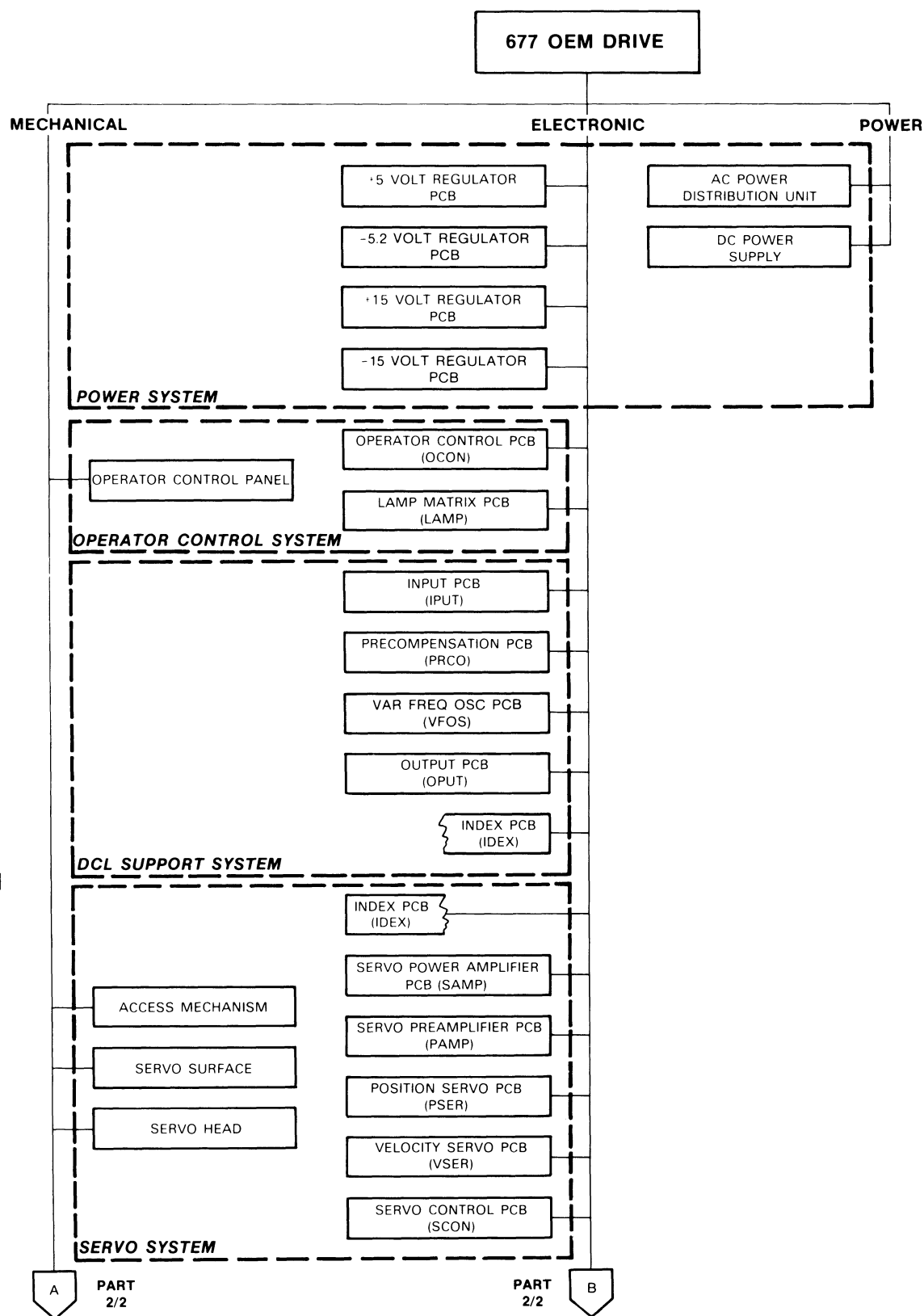
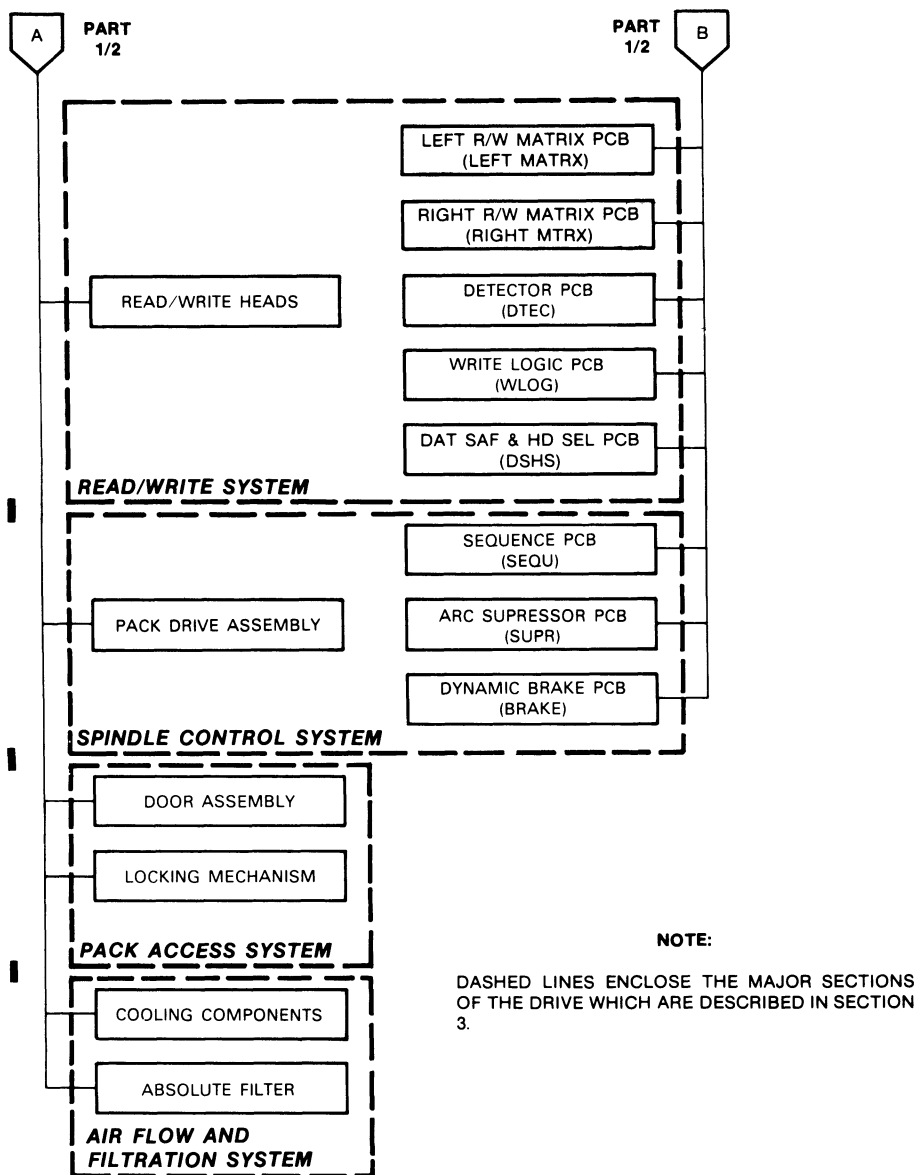


FIGURE 3-1. BREAKDOWN INTO SYSTEMS (Part 1 of 2)





PADDLE BOARDS				PCB POSITION																			
				D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20
A01	A02	A03	A04																				
B01	B02	B03	B04	INPUT	OPUT	PRCO	INDX	VFO	NOT USED	NOT USED	NOT USED	NOT USED	SEQU	SVTL	NOT USED	NOT USED	VSER	PSER	READ/WRITE CABLE	WLOG	LINA	DTEC	DSHS
C01	C02	C03	C04																			NOT USED	OCON

FIGURE 3-1. BREAKDOWN INTO SYSTEMS (Part 2 of 2)

## 3.2 OPERATOR CONTROL SYSTEM

### 3.2.1 System Description

The Operator Control System serves as the operator's interface with the drive and the DCL. It provides the mechanisms for controlling the drive, verifying normal operation, displaying drive status and commands issued by the DCL, and transmitting operating conditions set manually by the operator to using circuitry in the drive.

To provide the functions indicated above, the system uses a modularized operator control panel and associated circuitry, each of which is discussed below.

The control panel contains three switches, seven indicators, and one removable plug. The three switches enable starting/stopping the drive, reading only or reading and writing, and communicating with a predesignated control unit connected to the drive via the DCL. The removable plug is inserted into the panel to establish the drive's logical address. User information on the panel, operating procedures normally used, and suggested operator responses to abnormal conditions, can be found in Section 2.4. Further treatment of the panel is not needed in this manual.

### 3.2.2 Operator Control PCB

OCON circuitry and functions provided are described below, addressing the block diagram of OCON logic shown in Figure 3-2.

#### 3.2.2.1 LAP Plug Enabling

When the operator inserts a Logical Address Plug into its receptacle in the control panel, appropriate address switches (fixed by the plug's rear configuration) and an enable switch (located at the rear of the address switches) are engaged. Insertion generates ENABLE SW true and signals containing the binary decode of drive address (LAP 1,2,4). These signals are sent to the OPUT PCB, as shown in Figure 3-2.

#### 3.2.2.2 Generating Control A and Control B

Control A and Control B switch is sent to the OPUT PCB as Port A Locked and Port B Locked.

#### 3.2.2.3 Transmitting Display Commands

OCON transmits to LAMP a total of eight display indicators; they are listed in paragraph 3.2.3.

### 3.2.3 Lamp Matrix PCB

LAMP contains lamp drivers and indicator lamps that display drive operating and inhibit conditions in the control panel. Figure 3-3 shows the signals sent by OCON to the LAMP drivers, and the display lamps which can be illuminated. Sources of these signals are listed below.

- READY LAMP is generated by the On Line Latch on the OPUT PCB. The two signals READY LAMP and ON LINE are the same, as shown in Figure 3-2.
- START LAMP is generated by the Start Latch in OPUT (Figure 3-18), which verifies that start conditions are satisfied.
- STANDBY LAMP is generated by the Standby Latch in OPUT (Figure 3-18), which verifies that standby conditions are satisfied.
- WRITE PROTECT LAMP is an output from the SEQU PCB which indicates the status of the WRITE PROTECT SW.
- DOOR LOCKED LAMP is a register output of SEQU from the input signal DOOR LOCKED SW.
- UNSAFE LAMP is an output from OPUT logic which checks for the existence of any unsafe conditions in the drive.
- PORT A LAMP and PORT B LAMP are DCL commands, transmitted via IPUT and OCON. If both are true, both the "A" and "B" display lamps are illuminated.
- PORT LAMP is the Ored result of PORT A LAMP and PORT B LAMP, either of which being true causes illumination of the word CONTROL in the control panel.

## 3.2.4 System Performance Requirements

### 3.2.4.1 Addressing

Logical address requirements are (refer to Figure 3-2):

- a. If Logical Address Plug 0-7 is inserted into the operator control panel, PLUG ENABLE SW (D22-R18) is true.
- b. If Logical Address Plug 1, 3, 5, or 7 is inserted into the panel, LAP 1 SW (D22-R27) is true.
- c. If Logical Address Plug 2, 3, 6, or 7 is inserted into the panel, LAP 2 SW (D22-R33) is true.
- d. If Logical Address Plug 4, 5, 6, or 7 is inserted into the panel, LAP 4 SW (D22-R31) is true.

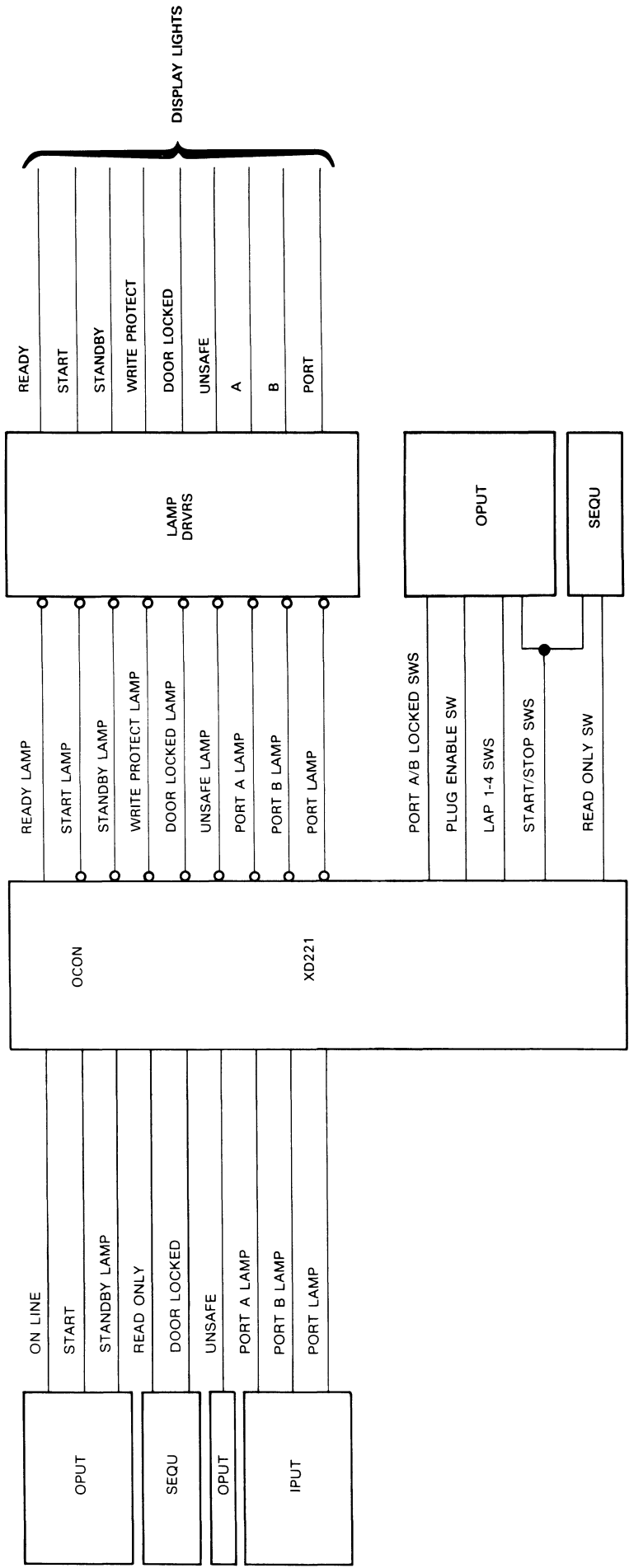


FIGURE 3-2. OPERATOR CONTROL AND LAMP MATRIX PCB

**BLANK**

### 3.3 DCL SUPPORT SYSTEM

#### 3.3.1 System Description

The DCL Support System serves as the drive's interface with the customer's Device Control Logic attachment (the DCL). This system receives commands and write data from the DCL, and sends drive responses to these commands and read data to the DCL. It also transfers command indicators between the DCL and operator control panel.

The commands received by the system, and the responses required of the system, are customer specified. They are defined in paragraph 1.3.1.

The DCL Support System uses a bidirectional data bus to receive write data and send read data. It compensates for variations in disc speed when writing, and standardizes the data and clock pulses when reading. If a DCL write command is issued and accepted as valid, the write data received is precompensated and transferred to write logic which is phase locked to servo data (and thus the disc speed), and recorded providing no unsafe condition exists. If a DCL read command is issued and accepted as valid, raw data from the disc is transferred to the system, conditioned as clocked read data, and sent to the DCL. To implement commands and provide read/write data conditioning, the system receives drive status/inhibit/unsafe indications from servo, spindle control, and read/write logic in the drive—and operates on these indications using the commands issued by the DCL and control panel. Output signals from the system are fed back to the same systems of logic, to support servoing, spindle control, and reading or writing, and to illuminate control panel lamps. Sources of inputs to the DCL Support System, and destinations of outputs from the system, are indicated in Table 3-1.

To provide the data handling and command processing functions discussed above, the DCL Support System uses four PCBs and part of the circuitry contained in a fifth PCB. Their names, individual functions, and general characteristics are indicated below.

- **IPUT (Input PCB).** IPUT receives, from the DCL, all commands of the drive and the data to be recorded in the disc pack—and sends data retrieved from the pack to the DCL. No manipulation is performed on approximately half of the commands received; they are distributed only to the using logic located elsewhere in the drive. The rest of the commands received are used to generate summary indications of the seek/offset argument, a drive general reset indication, head position error-correction

indications, and seek/offset/rezero enabling signals, the uses of which are more closely associated with the servoing function than with IPUT's principal functions to receive and distribute commands and provide a two-way path for data.

- **PRCO (Precompensation PCB).** PRCO encodes the write data received from the DCL (via IPUT) and precompensates for expected bit shift in the data prior to writing. Only one output signal is used in the logic; others are test points.

**TABLE 3-1. DCL SUPPORT SYSTEM INPUT SOURCES AND OUTPUT DESTINATIONS**

Input Sources	Output Destinations
Device Control Logic	Device Control Logic
Operator Control System	Operator Control System
• OCON (Operator Control PCB)	• OCON
Servo System	Servo System
• PSER (Position Servo PCB)	• PSER
• INDX (Index PCB)	• PAMP (Servo Preamplifier PCB)
• SVTL (Servo Control PCB)	• SVTL
• VSER (Velocity Servo PCB)	• VSER
Spindle Control System	Spindle Control System
• SEQU (Sequence PCB)	• SEQU
Read/Write System	Read/Write System
• DSHS (Data Safety and Head Select PCB)	• DSHS
• VFO (Variable Frequency Oscillator PCB)	• WLOG (Write Logic PCB)
• MTRX (Left and Right Read/Write Matrix PCB)	• PRCO (Precompensation PCB)
• LINA (Linear Amplifier PCB)	• VFO
• DETC (Detector PCB)	

- **VFOS (Variable Frequency Oscillator PCB).** VFOS can be divided into two functional units: oscillator and driver. The oscillator decodes raw data written on the disc in MFV code into standard format, and generates a clocking signal used to develop a read strobe. The driver converts the encoded TTL write data to differential ECL write data. The oscillator is used when reading but is kept running when writing, and the driver is used only when writing; they operate independently of each other.
- **Circuits in INDX (Index PCB).** Decoding index, which is the primary function of the Index PCB, is associated with servoing and for this reason Index PCB is designated part of the Servo System. However, secondary functions have been assigned to support the DCL Support System. The Phase Locked Oscillator (PLO) circuit generates the clock output which drives the oscillator in VFOS, and the divided output that is used in PRCO for write precompensation—and certain other outputs used to decode index. A power monitoring circuit generates an indicator of unsafe voltage which, if true, resets the oscillator in VFOS.
- **OPUT (Output PCB).** Except for read data, OPUT sends directly to the DCL all drive responses to the DCL commands received. In addition to this almost-dedicated function of responding to commands, OPUT generates indications of drive operating levels which can mean the drive is unsafe for operation, is either started or being started, or is in standby mode.

The following paragraphs describe the circuitry contained in the DCL Support System. Included in the description that follows are summary statements on PRCO, VFOS, and PLO performance requirements, to support and extend the circuit descriptions.

### 3.3.2 Input PCB

INPUT circuitry and functions provided are described below, addressing the block diagram of INPUT logic shown in Figure 3-3.

#### 3.3.2.1 Providing Seek Go Instructions

INPUT enables the drive to implement a DCL command to start seek motion, and transmits the head to be used, cylinder difference, and direction to the Servo System. The start of seek motion is initiated by SEEK START true, which is a latched condition caused by:

- DCL sending OFFSET MODE LEVEL false and SEEK/OFFSET GO PULSE true.
- Servo System sending indications that the drive is ready to receive commands (READY is true) and that the content of the difference register is zero (DIFF=0 is true).

The head to be used is designated in the HEAD SELECT lines. INPUT transmits the information in these lines to the head select decoder in DSHS. Cylinder difference (in DIFF/OFFSET lines) is loaded into difference counters, and seek direction and cylinder address (in CAR lines) are loaded into the reverse/cylinder register. If SEEK DIRECTION LEVEL (from the DCL) is true, the seek is in the reverse direction (REVERSE is true). SEEK START being true enables the Servo System to begin traversal of the number of cylinders contained in the difference counters. The present difference count, and summary data on the different count, are transmitted by INPUT to using elements of the Servo System, and/or the DCL via OPUT. The summary data consists of DIFF LESS THAN 32 and HIGH ORDER DIFF — and an indicator used for programming an access velocity of 4 inches/second (PGM DIFF 2); their uses by the Servo System are described in paragraph 3.4.

#### 3.3.2.2 Providing Seek Offset Instructions

INPUT enables the drive to implement a DCL command to start offset motion, and transfers the offset value and direction to the Servo System. Offset motion is initiated by OFFSET START true, which is a latched condition caused by:

- DCL sending OFFSET MODE LEVEL true and SEEK/OFFSET GO PULSE true.
- Servo System sending an indication that the drive is ready to receive commands (READY is true).

The offset value and direction are specified by the DCL in the DIFF/OFFSET lines, which are loaded into an "offset register" (difference counters are used) and sent to using elements of the Servo System as DIFF REG 1 → 128. OFFSET START being true enables the Servo System to offset in the direction and amount stored in the offset registers (difference counters).

When the heads reach the specified offset position and the drive is ready to receive commands, OPUT sends OFFSET READY LEVEL true to the DCL.

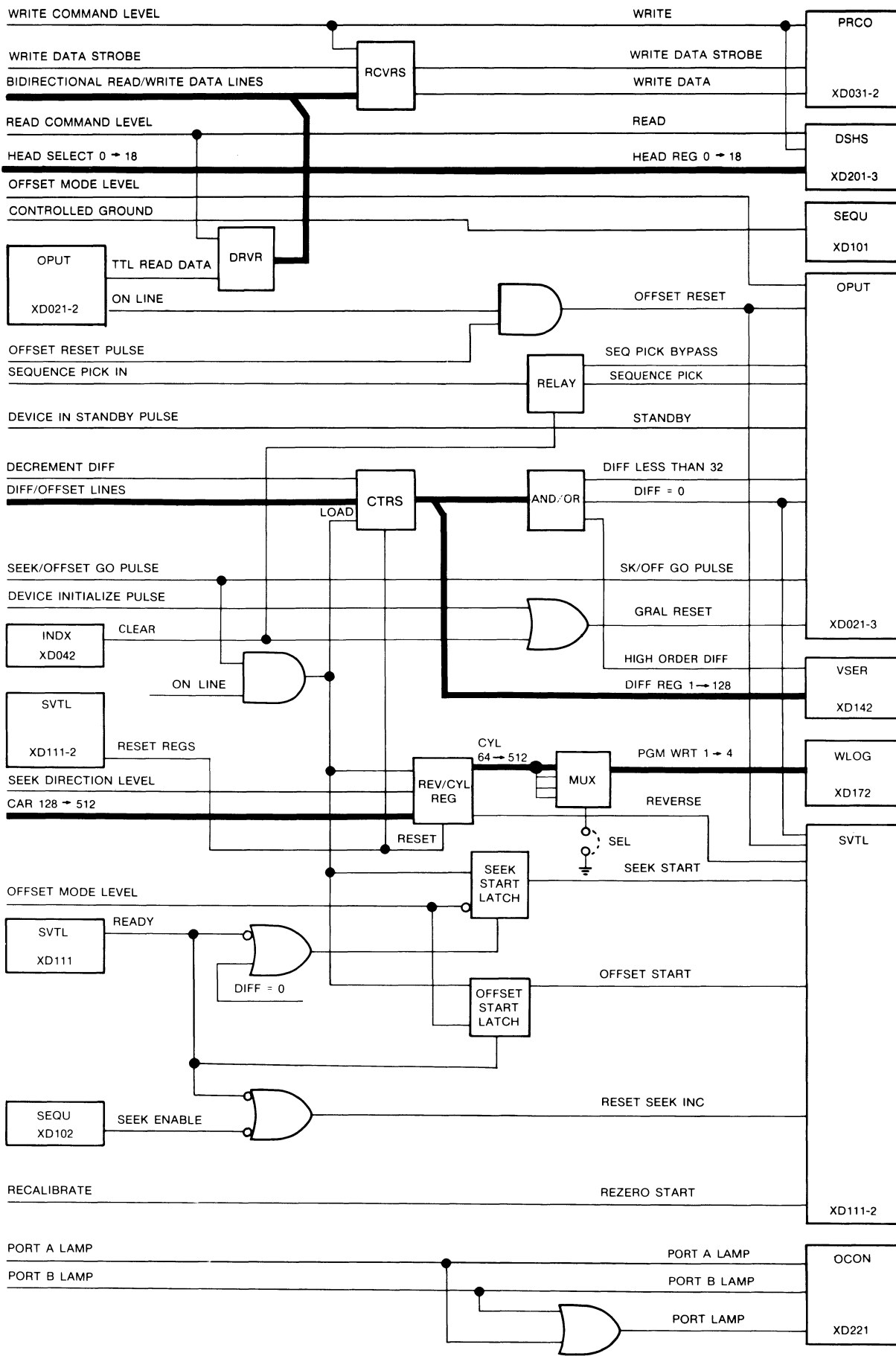


FIGURE 3-3. INPUT PCB

### 3.3.2.3 Providing Write Operation Instructions

IPUT receives the DCL's write command (WRITE COMMAND LEVEL), the serial NRZ write data (WRITE DATA), and the 6.45 mHz signal needed to clock the data for recording in the pack (WRITE DATA STROBE)—and sends them to PRCO for development of encoded write data. The receivers used are customer specified. WRITE is also sent to Read/Write System logic in DSHS, which polls for unsafe conditions in the drive.

### 3.3.2.4 Transmitting Read Data

IPUT receives, from OPUT, data retrieved from the pack (TTL READ DATA) and transmits the data to the DCL in the bidirectional data bus. The differential line driver used is customer specified.

### 3.3.2.5 Transmitting Recalibrate Command

IPUT receives the DCL command to seek Cylinder 000 (RECALIBRATE) and sends it to servo control logic as REZERO START.

### 3.3.2.6 Initializing the Drive

IPUT receives the DCL command to reset all safety latches (DEVICE INITIALIZE PULSE) and sends it to the off cylinder latch in OPUT as a general reset indication (GRAL RESET).

A general reset can also be indicated by the Servo System (CLEAR signal indicated by Index PCB).

### 3.3.2.7 Placing Drive in Standby Mode

IPUT receives the DCL command to execute standby sequencing (STANDBY) and transmits it to OPUT, where it is used to illuminate the control panel's standby indicator and to sequence down the drive.

### 3.3.2.8 Resetting an Offset Operation

IPUT receives the DCL command to reposition the heads over track centers, providing the heads are held offset when the command is received (OFFSET RESET PULSE). If held offset (OFFSET MODE LEVEL is true), the command is transmitted to the offset ready latch in OPUT and servo control logic in the Servo System.

### 3.3.2.9 Port Enabling

IPUT receives DCL commands which specify the communication path(s) to be used (PORT A LAMP or PORT B LAMP), and sends them to the Operator Control System for illumination of the corresponding control panel indicators.

### 3.3.2.10 Providing Power Sequencing Instructions

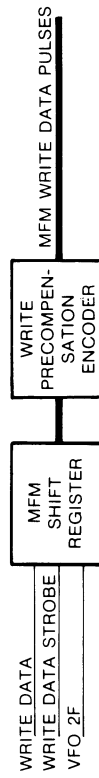
IPUT receives DCL commands which enable power sequencing in the drive (SEQUENCE PICK IN and SEQUENCE ENABLE), and sends them to OPUT for checking that start conditions are satisfied.

The interface signals involved in power sequencing, and the conditions that must be satisfied to initiate a power up or down sequence, are discussed in paragraph 1.3.1.4.

## 3.3.3 Precompensation PCB (Refer to Logic page XD031-2).

### 3.3.3.1 Encoding and Precompensating Data

PRCO PCB (Precompensation) contains circuitry which can be portrayed as follows:



PRCO logic takes WRITE DATA level (NRZ, non-return to zero) with WRITE DATA STROBE from DCL (received via IPUT) and synchronizes write data with VFO 2F timing signal. PRCO also codes write data in modified frequency modulation (MFM) form, and precompensates it allowing for the bit shift that is inherent when writing high density data. (See Figure 3-4.)

- The VFO 2F timing signal originates from VFO PCB and is phase-locked to PLO 2F A clock during write operation. The PLO 2F A clock is also phase-locked to servo (clock) pulses pre-recorded in the servo disc. In order to compensate for variations in disc speed, the VFO 2F is used for write timing signal. This enables bits to be written at a constant density.



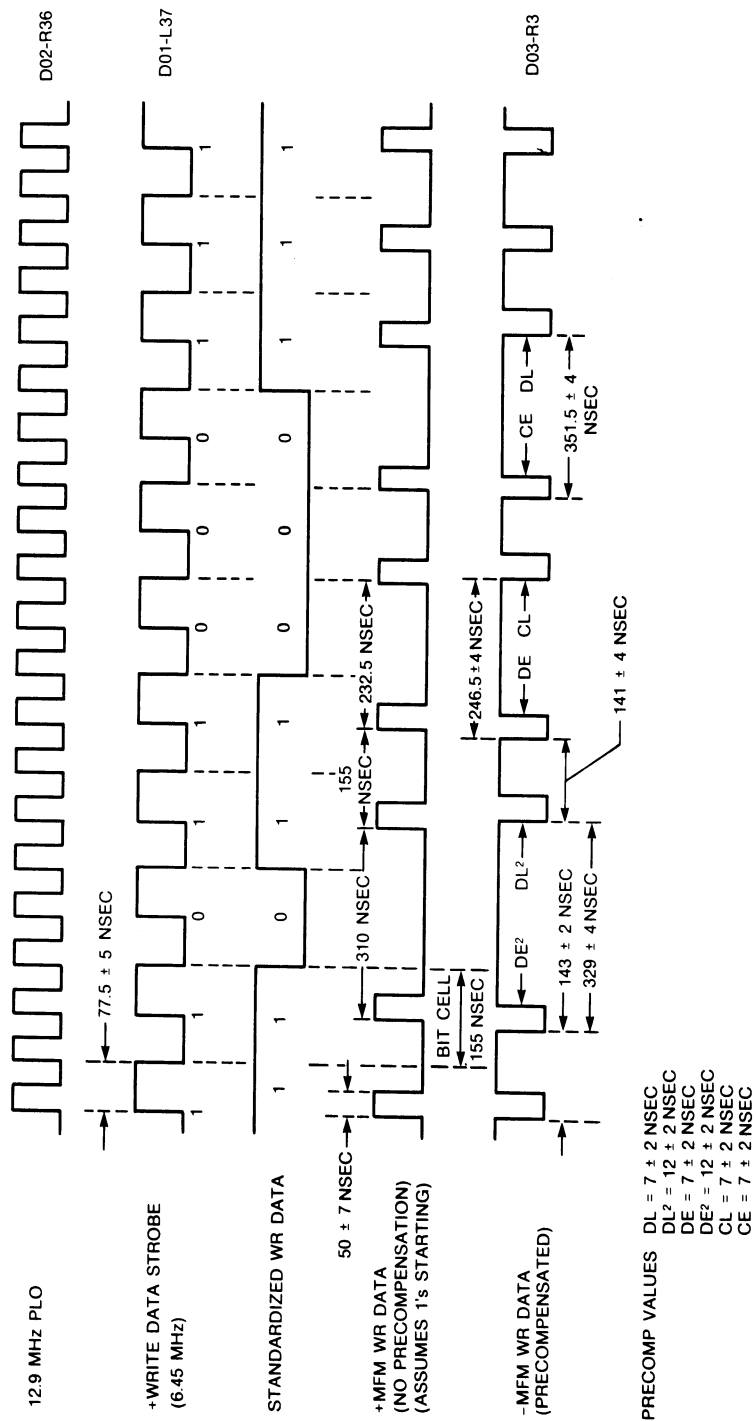


FIGURE 3-4. WRITE DATA TIMING

- The MFM recording technique (Figure 3-4) records a clock pulse between two consecutive missing data bits only. The clock pulse is then inserted midway between the two missing data bits. The timing relationship, therefore, between the clock and data pulses is always one and one-half cell time, or 232.5 nanoseconds. The normal time between two consecutive data bits is one cell time (155 nanoseconds). The maximum time between data bits is two cell time (310 nanoseconds).

- To compensate for bit shift in readback signal, the bits to be written are shifted opposite in time for their MFM-encoded positions so that the bit shift when writing will move the bit (Data or Clock pulse) into the desired location. Also taken into account is the fact that not all bit shifts are equal. The amount of bit shift depends on the density of the transitions preceding and following the shifted bit.

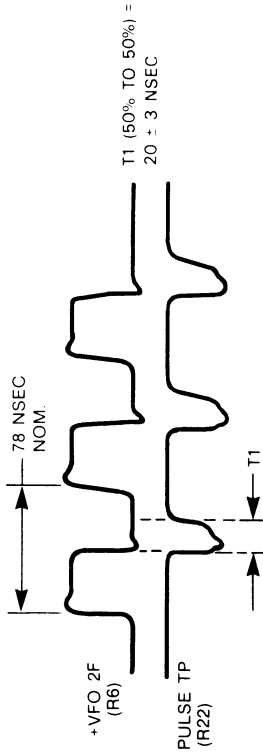
- PRCO circuit is activated by WRITE (or WRITE COMMAND from the DCL). The MFM WRITE DATA is sent to Write Logic (WLOG PCB) via VFO PCB, and is the only output from PRCO. Other output pins are used for test purposes.

- The block diagram of PRCO logic is shown in Figure 3-7.

### 3.3.3.2 Write Precompensation Requirements

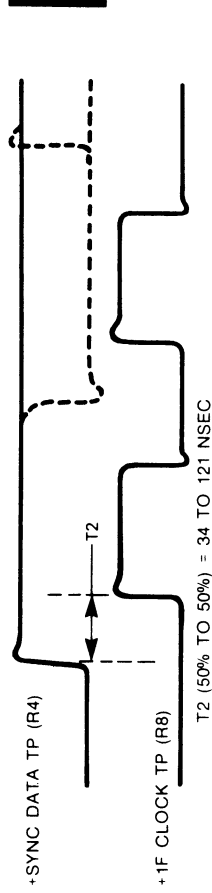
To satisfy PRCO performance specifications, timing requirements of DCL input signals to PRCO exist, and PRCO output signals are factory adjusted to eliminate any write precompensation error. Input requirements are summarized in paragraph 3.3.3.3. Output requirements, met at the factory, are summarized below for descriptive purposes and possible customer use in precompensation checking. Refer to the block diagram of PRCO test points in Figure 3-7. Only inputs  $\pm$  VFO 2F are ECL levels; all other input and output signals, including Test Points, are TTL levels.

**2F Pulse Timing.** The  $-2F$  PULSE TP (pin R22) signals must be negative going and must appear on the negative transitions of  $+VFO$  2F (pin R6). Width should be  $20 \pm 3$  nsec. These performance requirements are shown in Figure 3-5.



**FIGURE 3-5. 2F PULSE TIMING**

**1F Clock Timing.** The input sync circuit is adjusted by delay line ID such that the leading edge of  $+1F$  CLOCK TP (pin R8) is at least 34 nsec from any transition of  $+SYNC$  DATA TP (pin R4). These performance requirements are shown in Figure 3-6.



**FIGURE 3-6. 1F CLOCK TIMING**

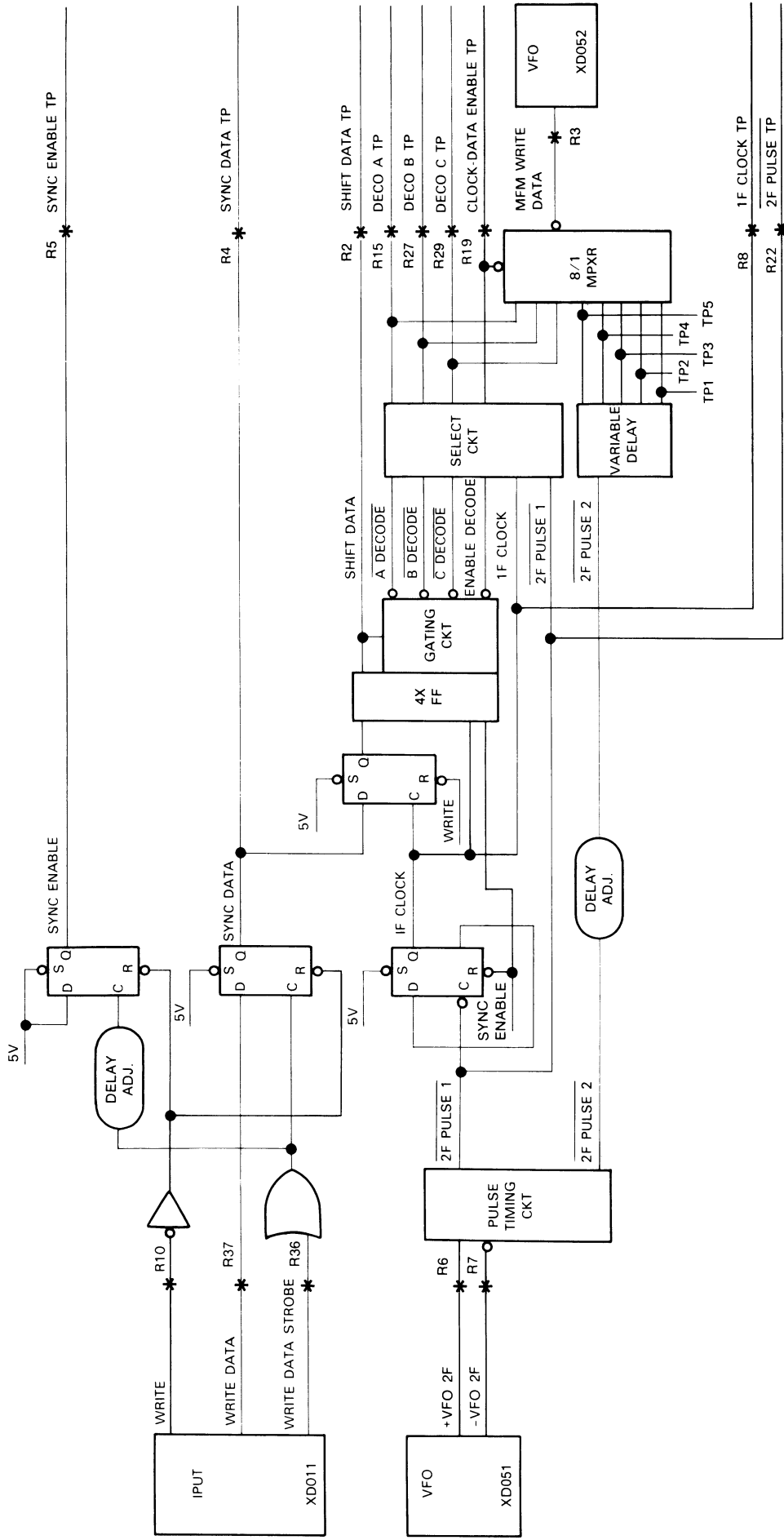
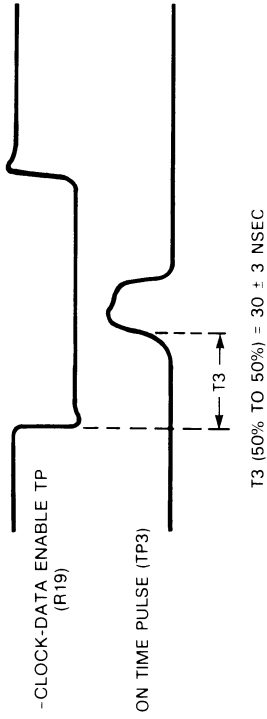


FIGURE 3-7. PRECOMPENSATION PCB (PRCO PCB, D03 LOCATION)

**On Time Pulse Timing.** The on time pulse (shown in Figure 3-7 as TP3) is adjusted such that its leading edge occurs  $30 \pm 3$  nsec after the trailing edge of -CLOCK-DATA ENABLE TP (pin R19). Figure 3-8 shows this requirement.



**FIGURE 3-8. ON TIME PULSE TIMING**

**Precompensation Delay Line Timing.** Refer to test points TP1 through TP5 shown in Figure 3-7. The pulses at TP1/2/4/5 must have the following timing relationships between their leading edges and the leading edge of the on time pulse at TP3:

- TP1.  $12 \pm 2$  nsec before TP3
- TP2.  $7 \pm 1$  nsec before TP3
- TP4.  $7 \pm 1$  nsec after TP3
- TP5.  $12 \pm 2$  nsec after TP3

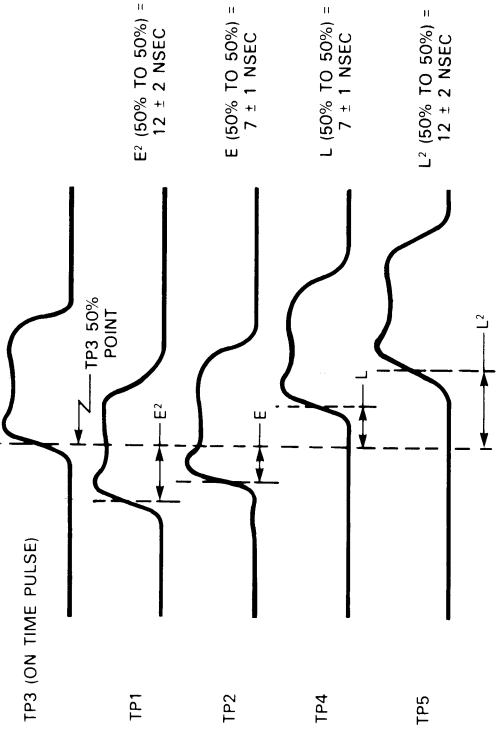
The performance requirements stated above are shown in Figure 3-9.

**MFM Write Data Pulse Timing.** The required pulse width of -MFM WRITE DATA (pin R3) is  $35 \pm 15$  nsec, as shown in Figure 3-10.

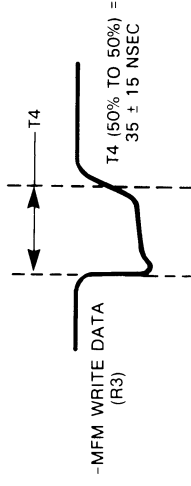
### 3.3.3.3 Signal Input Requirements

Timing requirements of inputs to PRCO are summarized below for reference purposes.

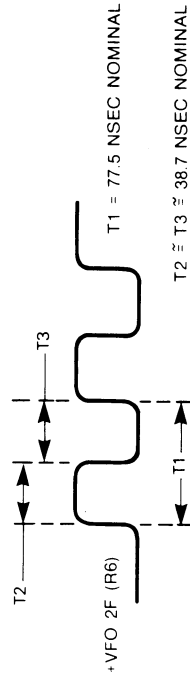
**±VFO 2F Timing.** The ±VFO 2F (pins R6/R7) signals are a 12.9 MHz (Nominal) square wave, as shown in Figure 3-11. Note that the -VFO 2F signal is the inverted signal of +VFO 2F.



**FIGURE 3-9. DELAY LINE TIMING**



**FIGURE 3-10. MFM WRITE DATA TIMING**



**FIGURE 3-11. ±VFO 2F TIMING**

**Write Data Strobe Timing.** The +WRITE DATA STROBE (pin R36) is a 6.45 MHz (Nominal) square wave indirectly derived from +PLO 2F A on INDEX PCB (D04). The phase relationship of this signal and +VFO 2F can be variable over 180 degrees of WRITE DATA STROBE as long as it is constant for any one write operation.

**Write Data Timing.** The +WRITE DATA (pin R3) signal being high represents a "1"—low represents a "0." The level may change depending on the incoming data from the DCL, but only at the time of the negative going edge of +WRITE DATA STROBE as shown in Figure 3-12.

**Write Command Implementation.** The -WRITE (pin R10) signal low activates the PRCO circuitry. A -WRITE high will reset and stop all PRCO operations.

**Address Mark Implementation (Optional).** If -AM at pin R13 is low for a few microseconds, it will inhibit MFM WRITE DATA output during that interval, and will write an Address Mark gap on a disc pack.

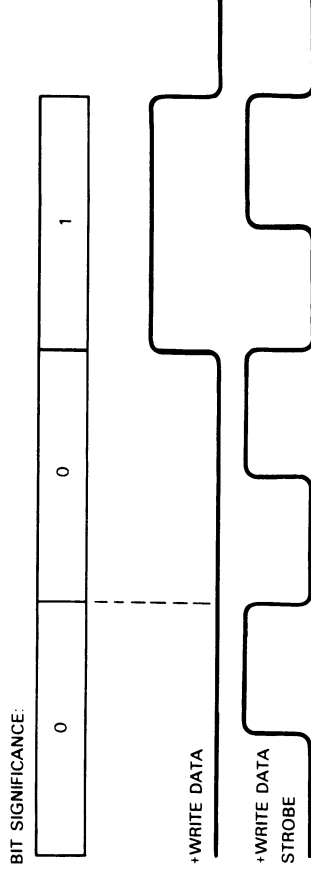


FIGURE 3-12. CHANGING STATES OF WRITE DATA

### 3.3.4 Variable Frequency Oscillator PCB

(Refer to Logic page XD051-2.)

#### 3.3.4.1 Decoding Raw Data and Generating VFO Clock

VFO has two functions related to read operations. The first is to decode raw data written in MFM code on the disc and send it to OPUT in shift register form, which is the standard NRZ format (non-return to zero), as ST DATA. It

is used by OPUT to generate TTL READ DATA which is transmitted to the DCL in IPUT's bidirectional data bus. The second function is to generate VFO CLOCK and send it to OPUT, which generates TTL READ STROBE that is also sent to the DCL.

The block diagram of VFO logic in Figure 3-13 illustrates how the two functions discussed above (and a third function, discussed in paragraph 3.3.4.2) are provided. The generation of ST DATA and VFO CLOCK is described below, addressing the using blocks in Figure 3-13.

**Receivers.** Raw data or PLO 2F A clock input is sent to one of two line receivers and connected as differential twisted pairs.

**Electronic Switch.** If READ is true, the switch connects the RAW DATA to the input of the Phase Detector. If READ is false, the switch connects PLO 2F A to the input of Phase Detector.

**Phase Detector.** This circuit generates output current which is proportional to the phase difference between the outputs of Electronic Switch and Voltage Controlled Oscillator.

**Filter.** The Filter converts the Phase Detector's output current into voltage. It ensures the phase locked loop (PLL) stability.

**Voltage Controlled Oscillator.** VCO generates a square wave with frequency proportional to Filter's output voltage.

**Fast T Control.** This circuit generates a signal (FAST T) for fast phase locked loop response.

**Phase Equalizer.** This is a squelching circuit which stops the VCO at every transition of -READ and starts the VCO in phase with RAW DATA or PLO 2F A.

**Data Separator.** This circuit generates the data window and separates the data bits from the clock bits.

**Shift Register.** The Shift Register converts the separated data (raw data without the clock bits) into "shift register" format (standard NRZ format).

**Reset Circuit.** This circuit resets the VFO after power to the drive is switched on, or when Switch S1 is pressed.

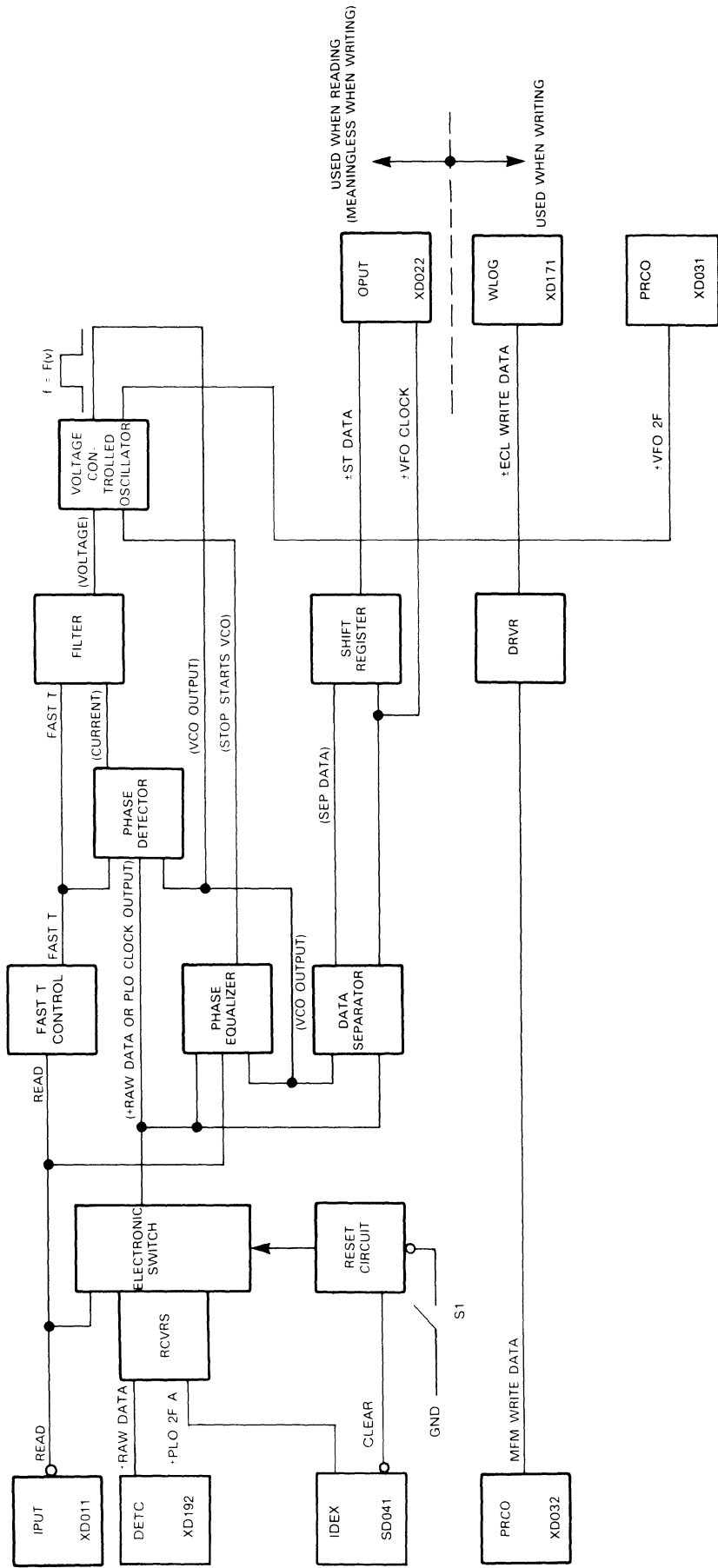


FIGURE 3-13. VARIABLE FREQUENCY OSCILLATOR PCB (VFO)

### 3.3.4.2 Converting Write Data and Generating VFO 2F

VFO has two functions related to write operations, as described below.

**Driver.** The Driver shown in Figure 3-13 is used when writing to convert the TTL write data (MFM WRITE DATA) to ECL differential write data (ECL WRITE DATA), and to transmit the converted data on a twisted pair line to write logic. Its operation is entirely independent of the VFO. For example, during a write operation the  $\pm$ ST DATA output of the VFO is meaningless.

**Write Timing Signal.** During a write operation, VFO is phase locked to  $\pm$ PLO 2F A inputs, and generates write timing signals  $\pm$ VFO 2F which reflect variations in disc speed and are sent to Write Precompensation PCB (PRCO).

### 3.3.4.3 VFO Performance Requirements

VFO performance requirements are summarized below.

#### Input Requirements:

- $\pm$ RAW DATA signals at pins D05-L37/R37 are readback MFM pulses with a nominal pulse width of 55 nsec, and are at ECL levels. An ECL ZERO level is defined as  $-0.80V$  to  $-1.40V$ , and an ECL ONE level is  $-1.50V$  to  $-1.90V$ .
- $\pm$ PLO 2F A signals at pins D05-L36/R36 are pulses at ECL levels with a pulse repetition rate of 12.9 MHz nominal (or a period of 78 nsec nominal).
- $-$ MFM WRITE DATA signal at D05-R5 is MFM Write data pulses at TTL logic levels.
- READ (D05-R19) and CLEAR (D05-L26) are TTL logic levels.

#### Output Requirements:

- All output signals are ECL levels. VFO waveform is shown in Figure 3-15.
- $\pm$ VFO 2F signals at pins D05-R6/R7 have a pulse repetition rate of 12.9 MHz nominal (or a period of 78 nsec nominal).

- $\pm$ VFO CLOCK signals at pins D05-L4/R4 have a pulse repetition rate of 6.45 MHz nominal (or a period of 155 nsec nominal).
- $\pm$ ST DATA signals at pins D05-R11/R12 are a decoded read data in non-return to zero form (NRZ) with  $\pm$ VFO CLOCK as its strobe timing.
- $\pm$ ECL WRITE DATA signals at pins D05-L3/R3 are MFM write data pulses at ECL levels.

#### Test Point Requirements

- Performing a write operation on an entire cylinder, DC ERROR at TP8 shall be  $-2.60V \pm 0.15V$ . The time interval between  $+FAST T$  (TP7) and  $-READ$  (TP3 or pin D05-R19) falling edges is  $3.8 \pm 0.6 \mu\text{sec}$ .
- Data Separator waveforms are shown in Figure 3-14 for an "all ones" bit pattern read back from a disc pack.

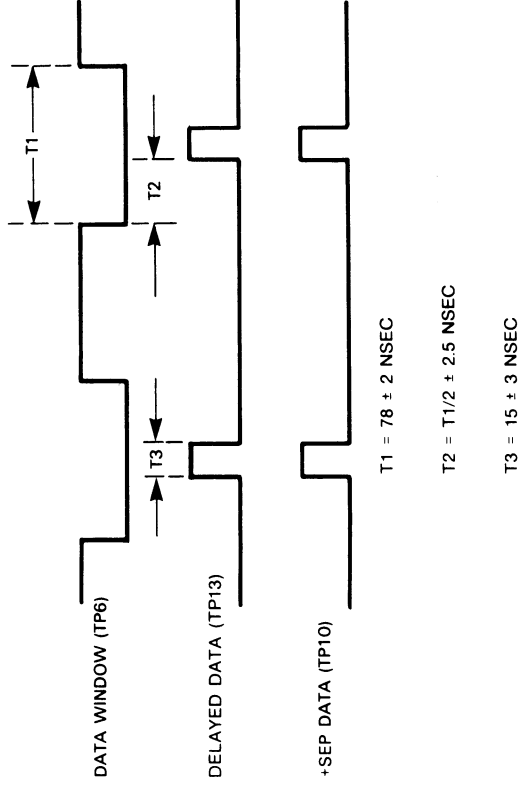


FIGURE 3-14. DATA SEPARATOR RESPONSE

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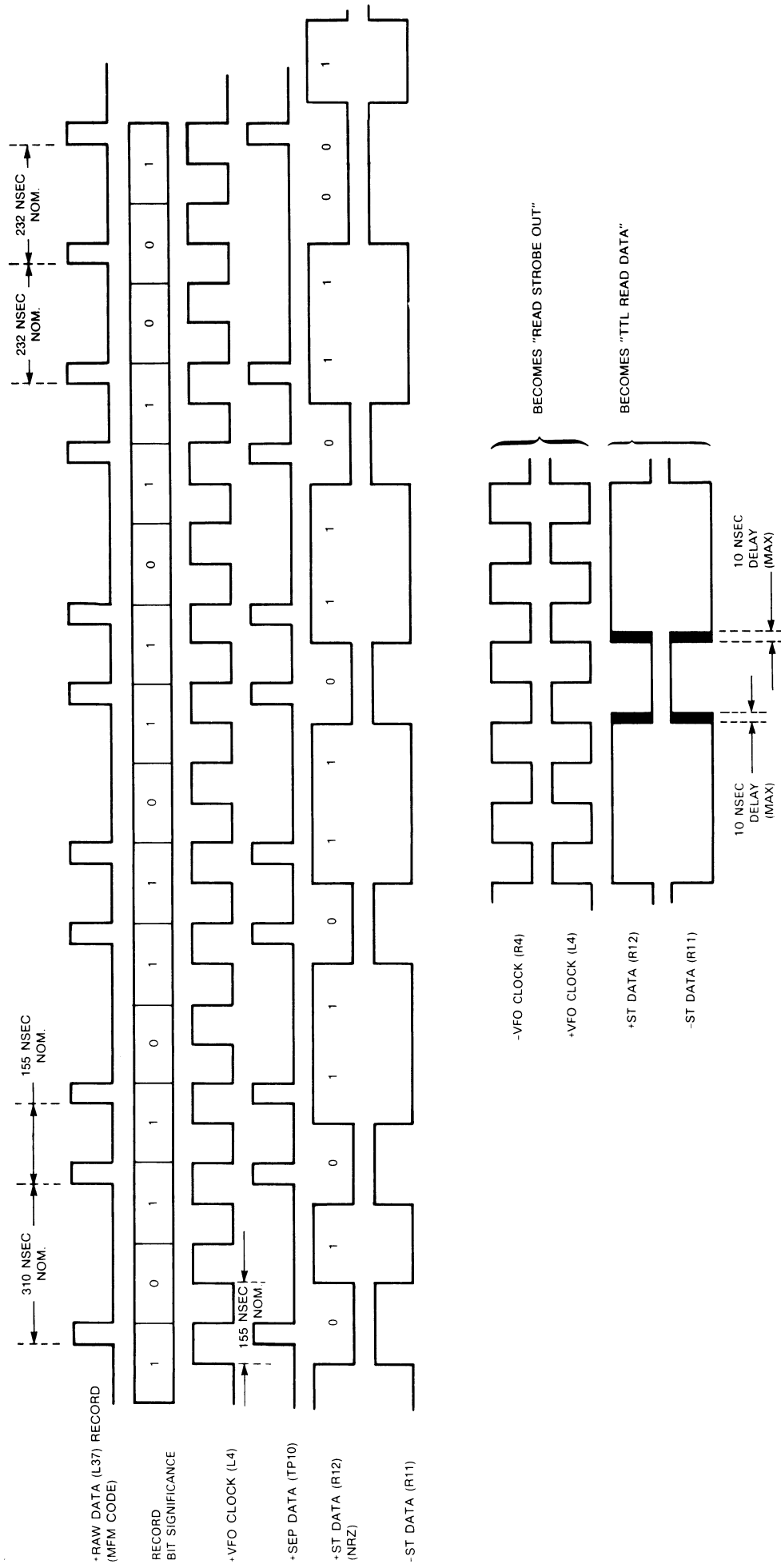


FIGURE 3-15. VFO OUTPUTS (D05)

### 3.3.5 Related Circuitry

The Index PCB, which has the primary function of decoding index (and therefore is designated as part of the Servo System), contains circuits that support data precompensation and VFO operation when writing. Functions provided by these circuits are identified below.

#### 3.3.5.1 Generating PLO Clock Outputs

The Index PCB contains the Phase Locked Oscillator (PLO). Figure 3-16 shows PLO input sources and output destinations. As shown in the figure, PLO generates the clock output that drives the oscillator in VFOS during write operations (PLO 2F A).

#### 3.3.5.2 Monitoring Regulated Power Supplies

Index PCB contains a circuit that monitors regulated power supplies in the drive, and generates an indicator of unsafe voltage (CLEAR) if any voltage is not within a specified range. CLEAR being true resets the oscillator in VFOS, as shown in Figure 3-13.

#### 3.3.5.3 PLO Performance Requirements

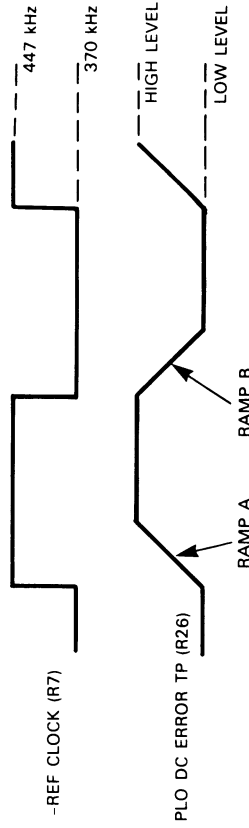
PLO output requirements are summarized below.

**DC Error.** With a square wave switching from  $370 \pm 2$  kHz to  $470 \pm 2$  kHz rate applied to -REF CLOCK (pin R7), PLO DC ERROR TP (pin R26) satisfies the requirements of Figure 3-17.

**Power Monitoring.** A total of five requirements are met. First, -POWER FAIL TP (pin R33) is greater than 5V if all specifications in Table 3-2a are satisfied. Secondly, the same signal is less than 0.4V if any specification in Table 3-3b is satisfied. Third, -CLEAR (pin R29) switches from 0 to 5V within  $1 \pm 0.5$  sec after -POWER FAIL TP switches from  $< 0.4V$  to  $> 5V$ . Fourth, -CLEAR does not switch to 0V if -POWER FAIL TP is  $< 0.4V$  for 80  $\mu$ sec or less. Fifth, -CLEAR switches to 0V if -POWER FAIL TP is  $< 0.4V$  for 500  $\mu$ sec or longer.

**TABLE 3-2. POWER MONITOR SPECIFICATIONS**

- a. R1 and R40 =  $+5.0 \pm 0.25V$   
 R16 =  $+15.0 \pm 0.75V$   
 R38 = -  $5.2 \pm 0.26V$   
 R25 =  $-15.0 \pm 0.75V$   
 L10 =  $+24 \pm 5V$
- b. R1 and R40 =  $+4.45V$  or less, OR  $+5.55V$  or greater  
 R16 =  $+13.35V$  or less, OR  $+16.65V$  or greater  
 R38 = -  $5.77V$  or less, OR  $-4.63V$  or greater  
 R25 =  $-16.65V$  or less, OR  $-13.35V$  or greater



1. HIGH LEVEL must be  $+10v$  or less.
2. LOW LEVEL must be  $-10v$  or greater.
3. RAMP A requirements are:  
 Slope =  $+1.7 + 0.5v/msec$   
 Duration =  $4.0 + 2.0 msec$   
 Damping factor =  $0.7 + 0.1$
4. RAMP B requirements are:  
 Slope =  $-1.7 + 0.5v/msec$   
 Duration =  $4.0 + 2.0 msec$   
 Damping factor =  $0.7 + 0.1$

**FIGURE 3-17. PLO DC ERROR RESPONSE**

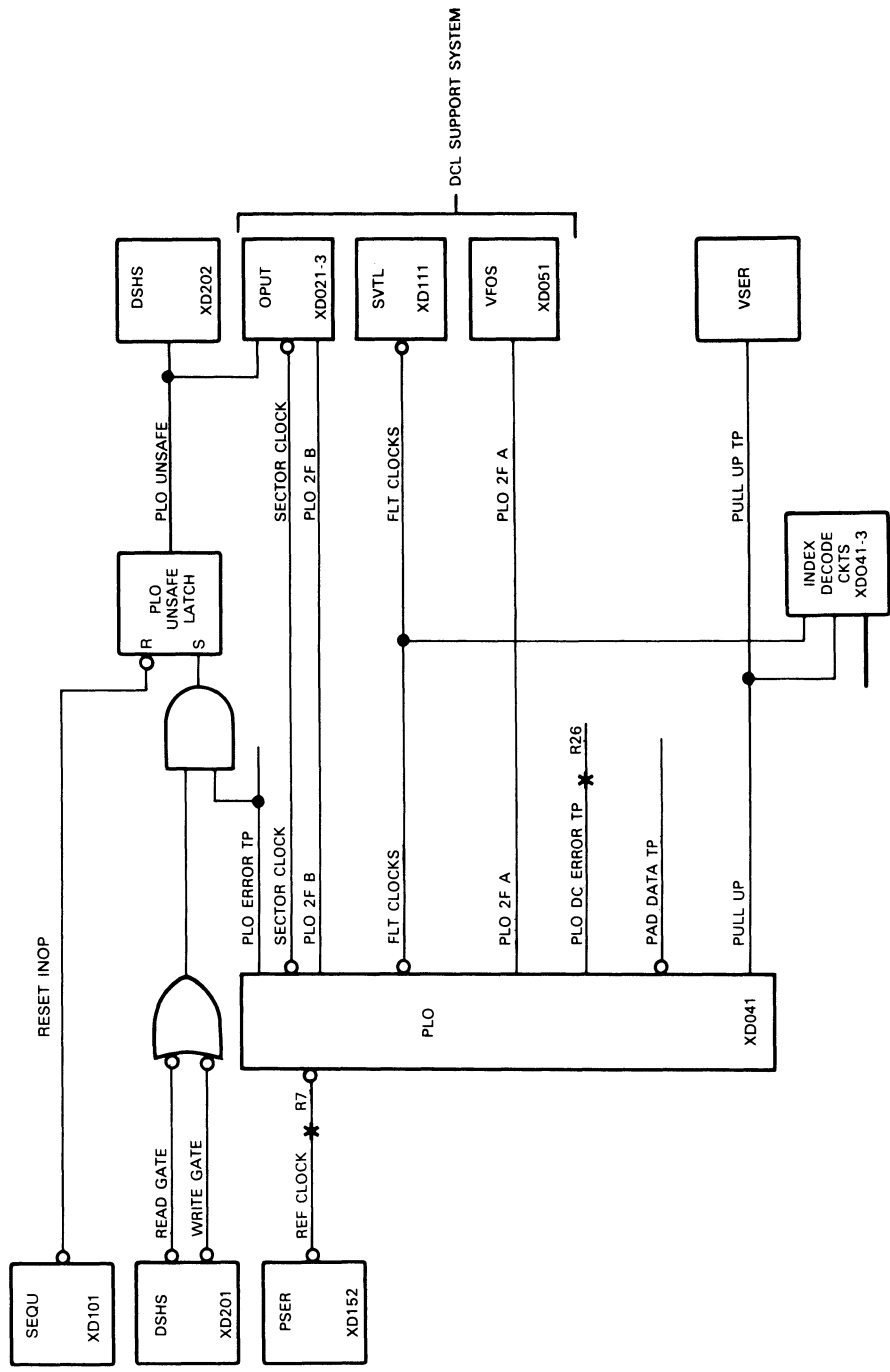


FIGURE 3-16. PLO INPUTS AND OUTPUTS

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### 3.3.6 Output PCB

OPUT circuitry and functions provided are described below, addressing the block diagrams of OPUT logic presented as Figure 3-18. This figure is divided into parts, depending on output destinations. Parts 1 and 2 address outputs transmitted directly to the DCL. Part 3 addresses outputs transmitted to other elements of logic internal to the drive.

#### 3.3.6.1 Responding to DCL Commands

OPUT sends to the DCL all drive responses to the DCL commands received, with one exception: read data is transmitted by OPUT to IPUT for transmission to the DCL over IPUT's bidirectional data bus. All responses are customer specified. They are defined in paragraph 1.3.1.3. All line drivers used are also customer specified; they are identified in paragraph 1.3.1.5.

Parts 1 and 2 of Figure 3-18 represents OPUT logic used to generate outputs supplied directly to the DCL. As shown, over half of these outputs are direct transmissions of inputs received. However, to satisfy customer requirements some signals change names even though no manipulation is performed (such as HEADS LOADED to SERVO DATA and READ ONLY to WRITE PROTECT). The rest of the outputs supplied directly to the DCL are summarized below.

**Latched Conditions.** OFFSET READY LEVEL is latched true when commands indicating an offset operation (ANDed result of SK/OFF GO PULSE true and OFF MODE LEVEL true) are received, executed (READY is true), and not reset (OFFSET RESET is false)—and regulated dc voltages are within acceptable ranges (CLEAR is false). If off cylinder is indicated, SEEK INCOMPLETE true is generated. At pack index (INDEX is true), INDEX PULSE true is generated in sync with sector clock.

**Unsafe Summary Indicators.** ORing eight of the possible indicators of an unsafe condition in the drive provides three summary indicators, as shown in the bottom area of Part 2. All of the unsafe indicators are shown in Part 3.

**Other.** PLO and VFO clock outputs are converted from ECL levels to TTL levels (TTL PLO CLOCKS and TTL READ STROBE, respectively). If an index error is detected when the DCL issues a write command (WRITE is true), INDEX ERROR true is generated. If OFFSET READY LEVEL is false, or the drive's Servo System is ready to receive commands (READY is true), FILE READY LEVEL true is generated.

#### 3.3.6.2 Transmitting Read Data

OPUT receives, from VFOS, read data in standard shift register format and sends TTL READ DATA to IPUT for transmittal to the DCL, as shown in Part 3.

#### 3.3.6.3 Indicating an Unsafe Drive

As shown in Part 3, indicators of an unsafe drive are ORed. Any indicator being true generates UNSAFE true which is sent to the drive's interface with the Head Alignment Unit (maintenance tool) and control panel to illuminate the unsafe lamp.

#### 3.3.6.4 Providing Start, Standby, and Unsafe Lamp Indications

If the conditions shown in Part 3 are satisfied, start, standby, or an unsafe indication is supplied to control panel lamps.

#### 3.3.6.5 Generating On Line

Refer to the On Line Latch in Part 1. If the LAP plug is inserted (PLUG ENABLE is true) and servo data is being sensed (SERVO DATA is true), the drive is on line (ON LINE is true) because the heads are loaded (servo head is reading positioning data from the pack), or, a recalibrate operation is in process. If the plug is removed, or the loss of servo data is detected at any time except during a recalibrate operation, the On Line Latch is reset.

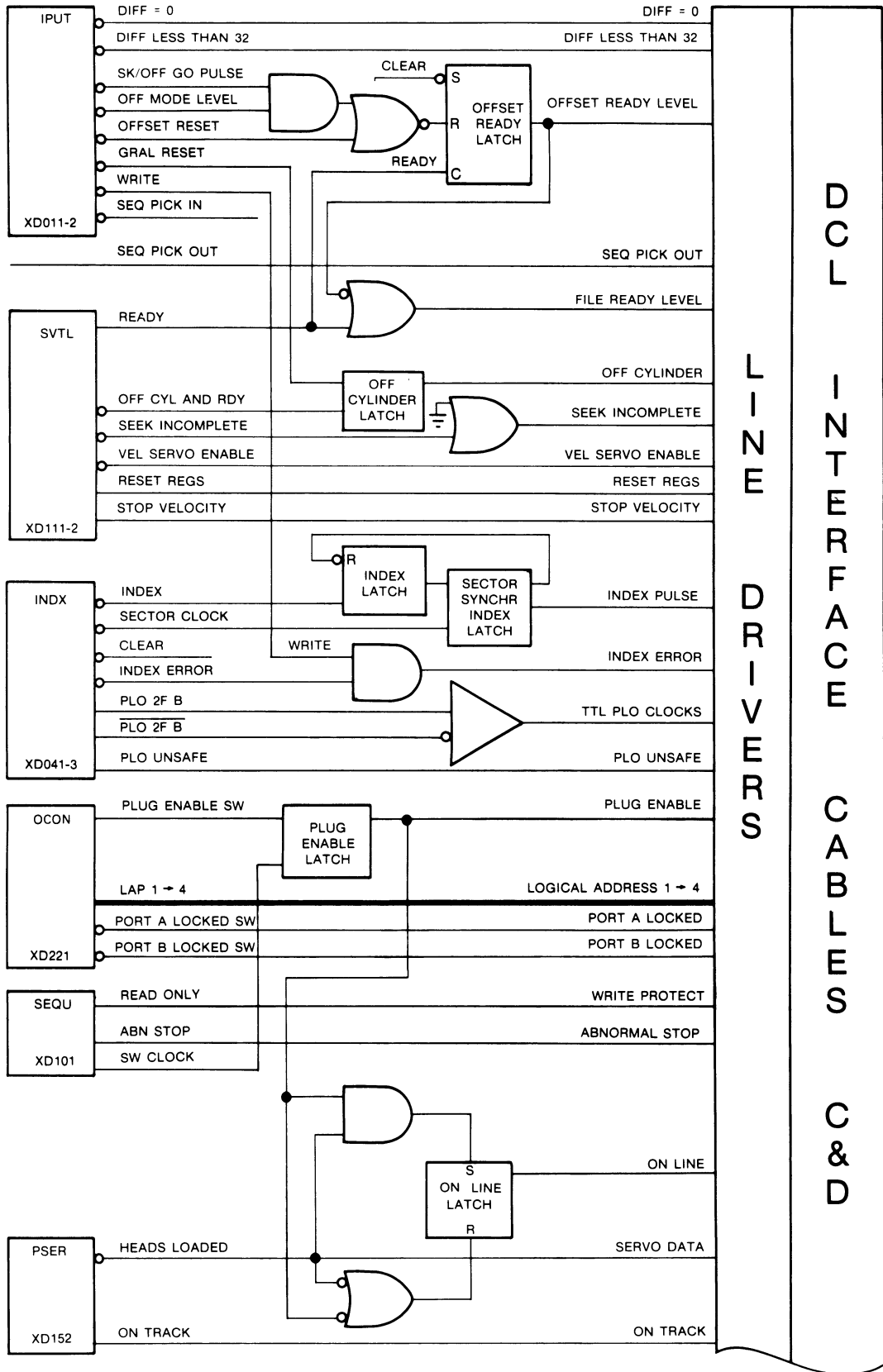


FIGURE 3-18. OUTPUT PCB (Part 1 of 3)

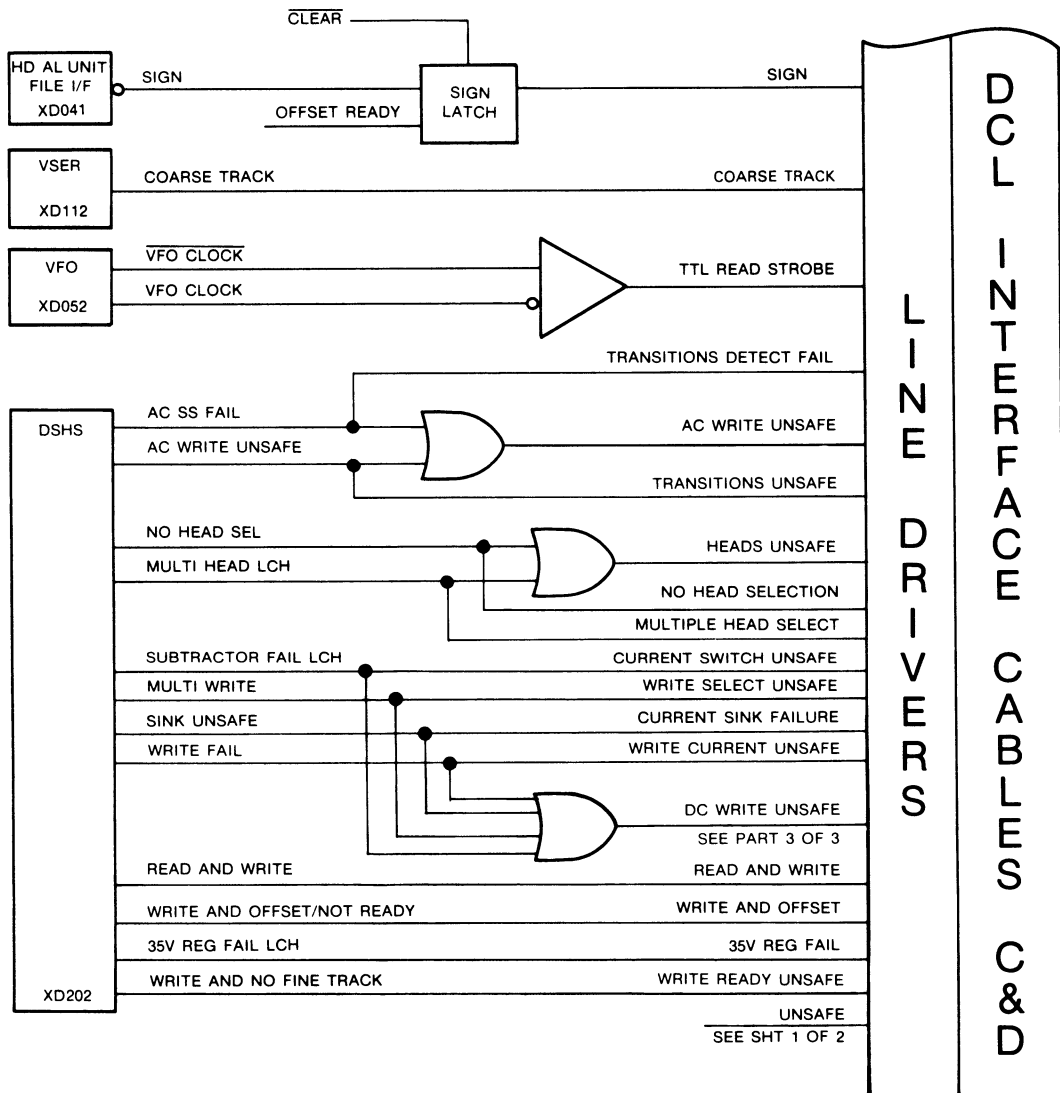


FIGURE 3-18. OUTPUT PCB (Part 2 of 3)

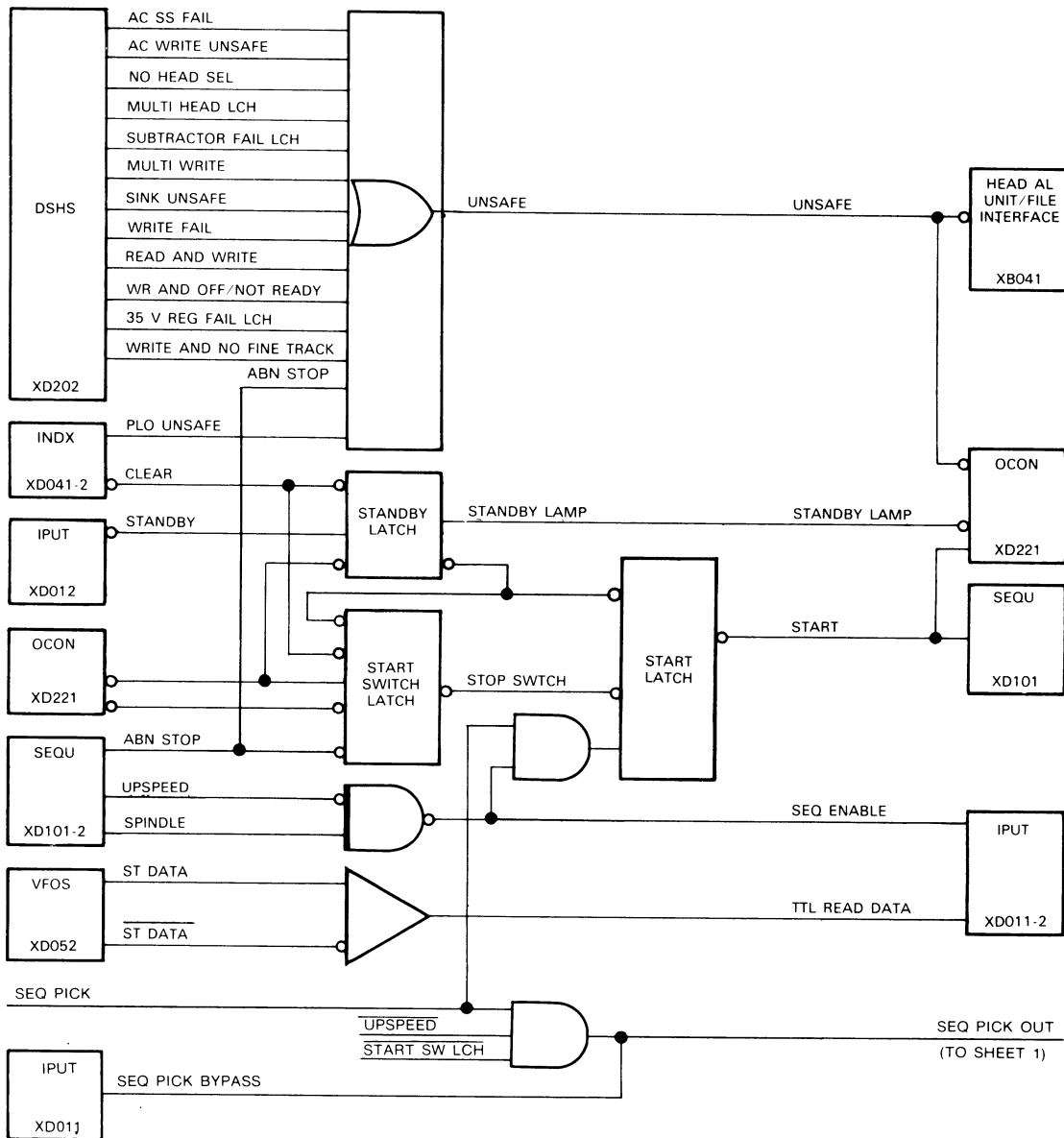


FIGURE 3-18. OUTPUT PCB (Part 3 of 3)



### 3.4 SERVO SYSTEM

#### 3.4.1 System Description

The Servo System is used to move the read/write heads over a preselected cylinder and to maintain accurate head positioning. These functions support the drive's fundamental capability of providing the DCL with direct access to any cylinder in the disc pack with an average access time of 28.5 msec.

The disc pack, containing 20 disc surfaces, has 815 cylinder locations. One head and one surface are used exclusively for servo information. The Servo System positions the 19 read/write heads over any one of the 815 cylinders. Positioning is normally over the cylinder's center. However, data error recovery is made possible by the added capability to track-follow a specified number of microinches on either or both sides of cylinder center in an attempt to recover the data.

The system uses an access mechanism and servo circuits to determine the current cylinder location, compute an optimized velocity schedule as a function of the difference between current and desired locations, move the heads through the disc pack, and control head acceleration and deceleration. Once having reached the desired location, track following the "proper" position (on or off cylinder center) is maintained. Since the system **constantly** determines the current location, it is characterized as a closed-loop system. Referring to the sketch below, the motor circuit controls direction and amount of current applied is controlled by an error-correction circuit which constantly monitors the current head location.

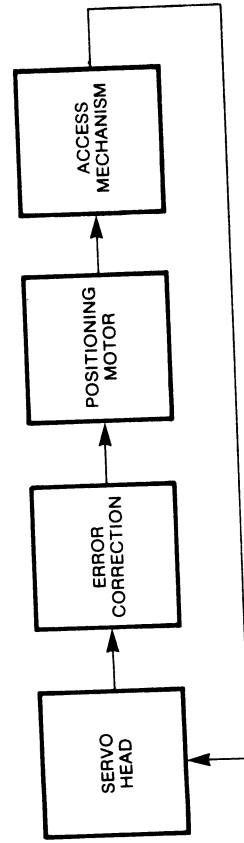


FIGURE 3-19. CLOSED-LOOP SERVO SYSTEM PHILOSOPHY

Three operating modes of the system exist. By definition, the "velocity control" mode exists when access motion (seeking, rezeroing) or head motion (loading, unloading) is occurring. The "position control" mode exists when track following (cylinder center or offset position). The "emergency retract" mode exists when the system is responding to detection of a serious malfunction.

Figure 3-20 is a simplified representation of the system. Referring to this figure, a voice coil motor (VCM) and a bearing-supported carriage position the heads over a cylinder. The VCM moves the carriage. The direction of movement and velocity of the carriage are controlled by the direction and amount of current in the voice coil. The heads and coil are mounted on the carriage. Movement of the carriage causes the heads to move within the disc pack, or to be retracted from the disc pack. Servo circuits provide the methods of controlling and monitoring head positioning. By monitoring servo information from the pack, these circuits change head positioning by controlling current in the VCM. When seeking, the number of cylinders to be traversed is loaded into a difference counter. As the heads move toward the desired cylinder, the difference count is decremented each time the servo head passes a cylinder location. In these ways, the VCM, carriage, servo circuits, servo head, and servo surface work together to allow direct access to any data record for reading, or any cylinder location for writing.

As discussed in the paragraphs above, three operating modes of the system exist, and the system contains a VCM and carriage ("access mechanism"), servo head and servo surface, and servo circuits. These operating modes and elements of the system are described in the rest of this section, as follows:

- **Operating Modes.** The three operating modes of the system are described in paragraph 3.4.2. They classify the types of mechanical action performed and control signals used when the system is operating in fundamentally different ways. Referencing a particular mode is helpful in communicating information about the system.
- **Access Mechanism.** Paragraph 3.4.3 reviews the mechanics of accessing and the components used.
- **Servo Surface.** Paragraph 3.4.4 summarizes the disc format used and how servo information is detected.
- **Servo Head.** Paragraph 3.4.5 discusses the manner used by the servo head to accomplish a track-follow operation in the Position Control mode, and make corrections for head position error.

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- **Servo Circuits.** Paragraph 3.4.6 presents an overview of the system of logic heretofore called the servo circuits. Paragraphs 3.4.7 through 3.4.12 describe the major elements of this system of logic, addressing the operating principles used.

- **Servo Operation Timing Diagrams and Waveforms:** Paragraph 3.4.13 contains timing diagrams of load heads, retract, recalibrate, track follow, and seek operations—and reference waveforms taken at test points within the servo circuits. The timing diagrams represent a “quicklook” summary of the self-controlled operations of the system. The waveforms are useful in system performance checking.

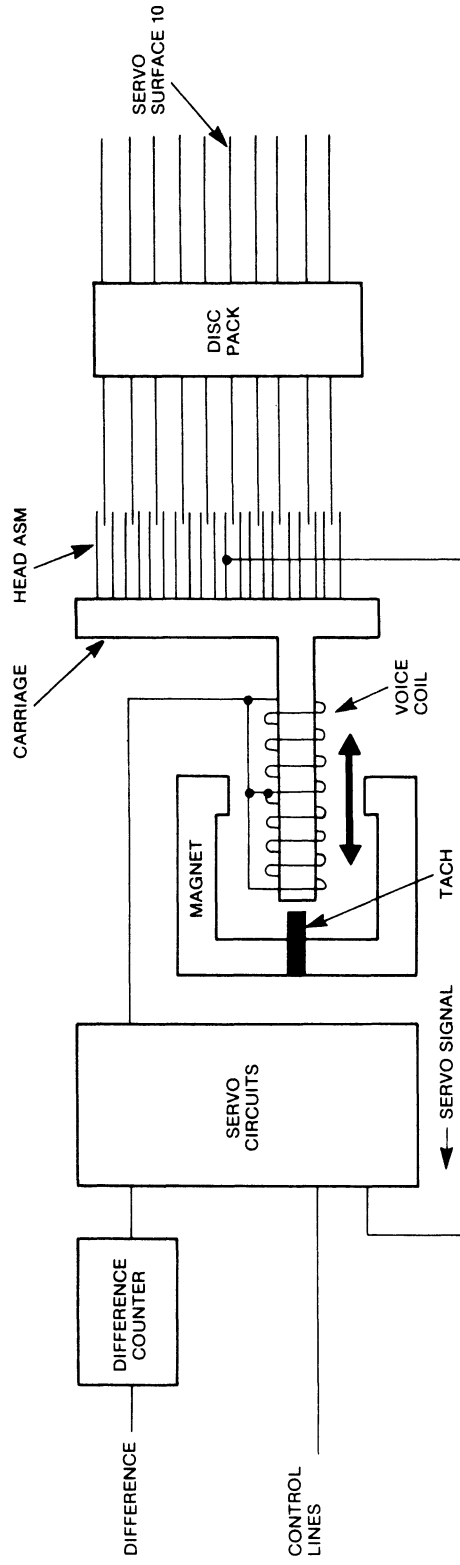


FIGURE 3-20. SERVO SYSTEM BASIC ELEMENTS

### 3.4.2 Servo Operating Modes

A description of the three Servo System operating modes is presented below, addressing the positioning operations possible in each mode and when/how/why each operation is normally performed.

#### 3.4.2.1 Velocity Control Mode

A total of four positioning operations can occur while the system operates in the Velocity Control mode; they are:

**Load Heads.** To perform a load-heads operation, the heads are loaded/positioned into "flying" attitude above the disc surface after the discs reach the required rotational speed. The sketch below shows the orientation of mechanical components when heads are loaded. Referring to this sketch, heads are attached to arms which are screwed to the T-block, and the T-block is mounted on the carriage. As shown, any head-arm assembly is not contacting a cam surface when heads are loaded. Heads are loaded when the drive is powered up or restarted by the operator following a disc pack change. In either case, the following events occur to load heads: forward current is applied to the VCM, heads are cammed down to flying position as they move forward into the disc pack, and forward motion continues until the heads are over Cylinder 000. When heads are loaded, the Servo System switches to the Position Control mode.

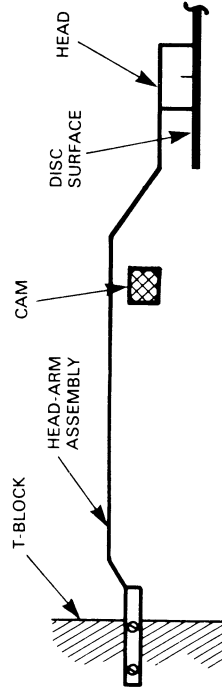


FIGURE 3-21. LOADED HEADS

**Retract.** To perform a retract operation, heads are unloaded and then retracted from the pack. The sketch below shows orientation of mechanical components when heads are unloaded. As shown, the bend in any head-arm assembly is contacting a cam surface when heads are unloaded.

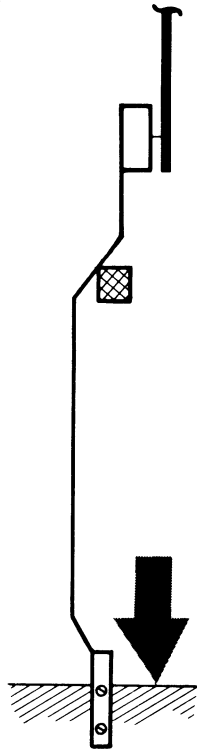


FIGURE 3-22. UNLOADED HEADS

The sketch below shows component orientation when heads are retracted. As shown, any head is moved completely away from a disc surface when heads are retracted.

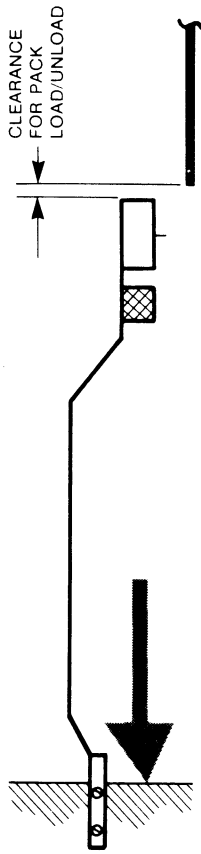


FIGURE 3-23. RETRACTED HEADS

Heads are unloaded and retracted when the drive is powered down by the operator to allow a disc pack change, or stopped by servo circuits when failures occur. In either case, the following events occur to unload and retract heads; reverse current is applied to the VCM to retract the carriage, and heads are cammed away from disc surfaces as the heads move in reverse out of the pack.

**Recalibrate.** To perform a recalibrate operation, the heads retract until they are no longer over data, then seek to cylinder 000. It is used when the DCL sends a RECALIBRATE command, normally after a seek error to reestablish a known head location, or after the operator reinserts the logical address plug. In either case, the following events occur to recalibrate the system: reverse current is applied to the VCM to drive the carriage out of the cylinder area, and then forward current is applied until heads are positioned over cylinder 000. When the system is recalibrated, it switches to the Position Control mode.

**Seek.** To perform a seek operation, the heads are moved to a new cylinder location. It is used for reading and writing data at a DCL-selected location in the pack. The system begins a seek operation when the seek argument (cylinder difference and direction of travel) and the initiating SEEK command are received. The following events occur during a seek operation: proper current is applied to the VCM to move heads to the new cylinder, difference amount is decremented as each cylinder is passed, and carriage speed is controlled to cause heads to stop at the new cylinder location (difference = 0). The sketch below makes a significant point about seek operations. Referring to this sketch, 10 is assumed as placed in the difference counter to move the heads from cylinder 120 to cylinder 130. Notice that the signal DIFF=0 becomes true approximately one track from the terminal position (cylinder 129).

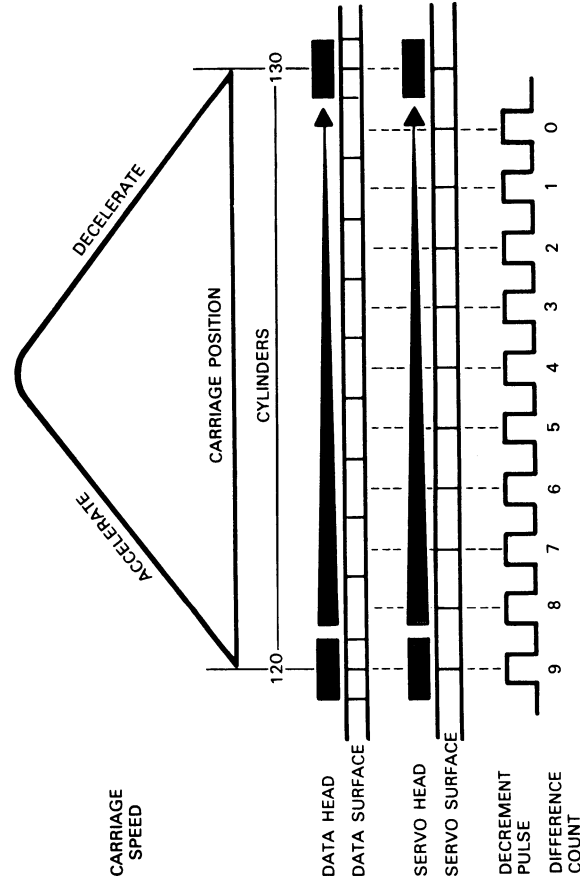


FIGURE 3-24. SIMPLIFIED SEEK OPERATION

### 3.4.2.2 Position Control Mode

Before entering the Position Control mode, the system must first operate in the Velocity Control mode to load and position the heads over the selected cylinder.

The system operates in the Position Control mode to maintain proper positioning of the heads. "Maintaining proper positioning of the heads" means operating the system such that the heads are tracking/following either the centerline of the cylinder or a location offset from the centerline by a specified number of microinches, whichever is specified in information supplied by the DCL.

Two head positioning operations can occur while the system operates in the Position Control mode; they are:

**Track Follow.** In a track-follow operation, the data heads are track following the data cylinder center. This location is, by definition, coincident with the border in a servo track between odd servo data and even servo data, as shown below.

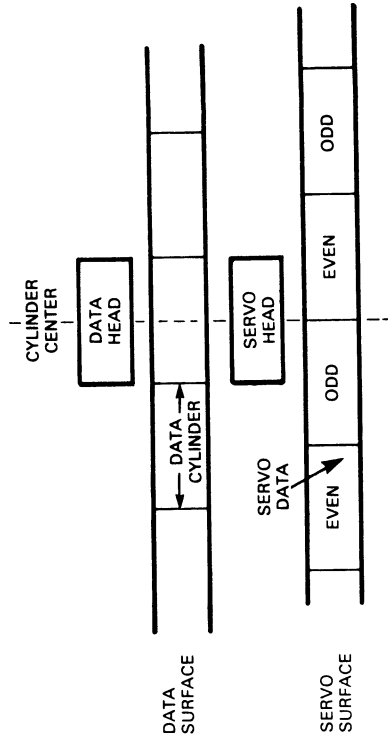


FIGURE 3-25. DEFINITION OF CYLINDER CENTER

Track following the cylinder center is accomplished by the servo head. It contains a read element spanning across one track width. Signals from the two adjoining bands of odd servo data and even servo data are sensed by the read element. To maintain read/write heads over cylinder centers, the system nulls the odd and even data signals by changing current applied to the VCM. See paragraph 3.4.4 for a full description of the head position error-correction process.

**Offset.** In an offset operation, the data heads are track following a predetermined number of microinches (proportional to position signal amplitude) off either side of the cylinder center (offset). Performing this operation is useful during error recovery and head alignment verification procedures. For example, if data errors are experienced, the heads can be offset to both sides in an attempt to recover the data.

To initiate an offset operation, the DCL sends amount-of-offset information and an OFFSET START command to the drive. The drive induces into the servo circuits an "error" voltage which is proportional to the required amount of offset. The data heads track follow off cylinder center by an amount and direction proportional to the amplitude and polarity of the error voltage.

### 3.4.2.3 Emergency Retract Mode

Only one positioning operation can occur in this mode, this being an emergency-retract operation.

In the emergency-retract operation/mode, the heads are unloaded and retracted from the pack whenever a serious malfunction warrants such action. Examples are logic voltage failure, retract failure, overcurrent failure, and supply voltage failure. During this operation, heads are cammed away from the disc surfaces as the heads move in reverse out of the pack.

Unlike the "normal" retract operation in the Velocity Control mode, the emergency-retract operation cannot be initiated by either the host computer or DCL.

### 3.4.3 Access Mechanism

The access mechanism, consisting of the VCM (Voice Coil Motor) and carriage assembly, is used to position the read/write heads over a preselected cylinder. The VCM and carriage assembly are part of the drive's deck plate, shown in Figure 3-26. Referring to this figure, the heads are screwed to the T-block, the T-block is mounted on the carriage, and the carriage is moved by the VCM along the carriage way. The carriage travels on tri-point bearing surfaces along hardened rails of the carriage way. The direction of movement and velocity of the carriage are controlled by the direction and amount of current in the VCM coil. The coil is also mounted on the carriage, and is provided with current through the flex conductors mounted at the side of the VCM.

The read/write heads and the servo head are mounted on precision stainless steel arms. As discussed in paragraph 3.4.2.1, heads are cammed away from the disc surfaces as they move in reverse out of the pack, or cammed down to flying position as they move forward into the disc pack. All heads are similarly constructed. See paragraph 3.5 (Read/Write System) for a mechanical description of the heads.

The tachometer assembly consists of a magnetized rod, attached to the back of the T-block, and a tachometer coil. As the carriage moves back and forth, the signal generated within the coil corresponds to the speed at which the rod is traveling. This signal is fed to the servo electronics to control the speed during seek operations.

A continuous seeking operation causes the coil to rise in temperature. For this reason a continuous stream of cool air is circulated through and around the coil. This air stream is generated by pack rotation and is guided around the entire motor area. For details of the cooling provisions built into the drive, see paragraph 3.8 (Airflow and Filtration System).

The carriage, T-block, carriage way, tachometer rod, tachometer coil, and motor assembly are precision aligned at the factory. Clearances are maintained between the stationary section and the moving or suspended sections. Field adjustments are possible using precision tools which are available. Adjustment procedures are included in Section 4.0 (Maintenance).

See the 677 OEM *Illustrated Parts Catalog* for a breakdown of parts in the access mechanism, tabulated in the recommended order of disassembly down to available field replaceable units, and information on the required maintenance tools.

### 3.4.4 Servo Surface

Using a sketch of segments of the servo surface and the recording surface located directly underneath, Figure 3-27 presents salient points of the servo disc format. This figure is self-explanatory and should be understood before proceeding.

### 3.4.5 Servo Head

The paragraphs below describe how signals from the servo head enable the system to accomplish proper positioning of the read/write heads. The description focuses on the basic concept of Even Servo Data bordering on Odd Servo Data. As shown in Figure 3-27, this border is the common centerline of data tracks in the cylinder located directly above and below in the disc pack.

#### 3.4.5.1 Servo Carrier

Signals from the two adjoining bands of Even Servo Data and Odd Servo Data are termed E and O, respectively. The servo head contains a read element spanning across one track width. Therefore, if the head is centered over Even Servo Data, the peaks (positive or negative) in the E wavetrain are equal to 100% of maximum E. At the same time, the peaks (negative or positive) in the O wavetrain are equal to approximately 100% of maximum O.

The combination of E and O signals from the adjoining servo bands constitutes a servo carrier containing information on the magnitude and direction of off-track. This means that for a given carrier, the head is either centered, off-track on one side of the border, or off-track on the other side.

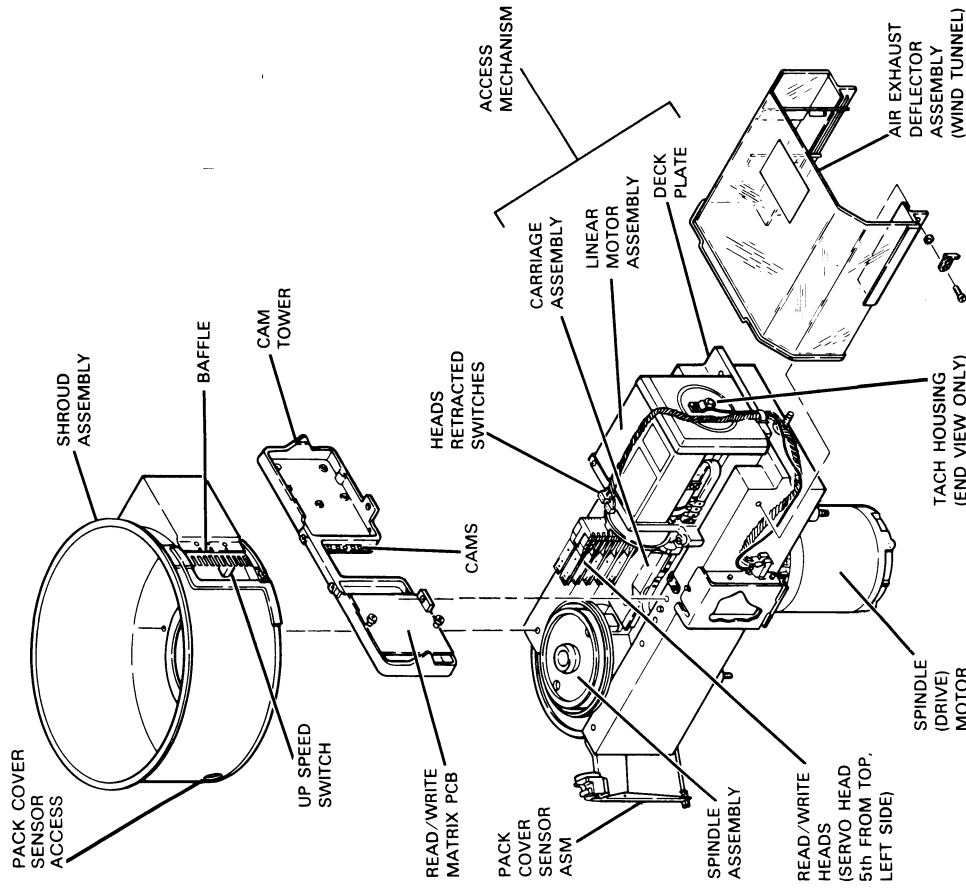


FIGURE 3-26. MAJOR COMPONENTS OF DECK PLATE

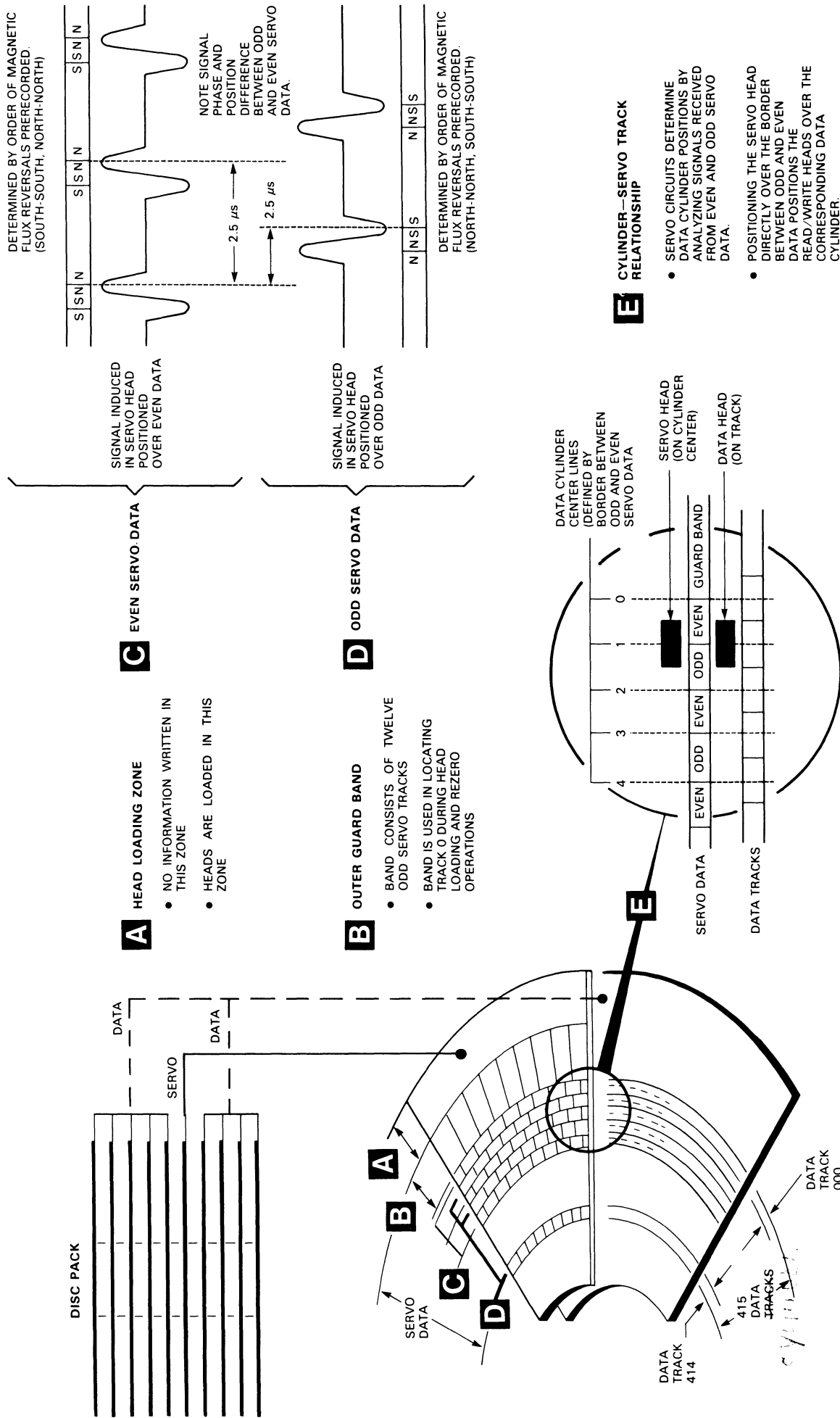


FIGURE 3-27. SERVO SURFACE FORMAT



### 3.4.5.2 Carrier Amplitude

The sketch below portrays Even Servo Data and Odd Servo Data on the rotating servo surface. An example servo head path is superimposed over the data.

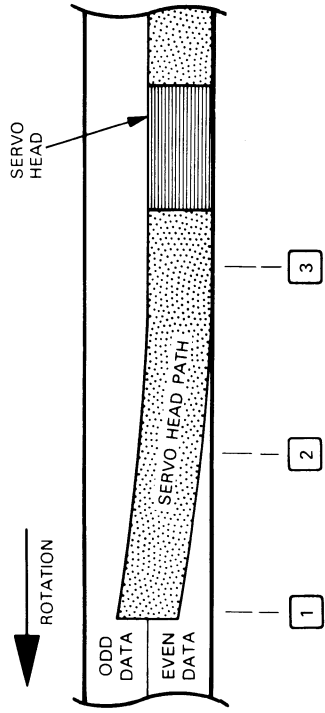


FIGURE 3-28. EXAMPLE SERVO HEAD PATH

At point 1 in the head path shown above, the servo head is centered over the border between even and odd data. The E and O signals (at the output of the servo preamp), in terms of percent of maximum signal amplitude, are shown in the illustration below.

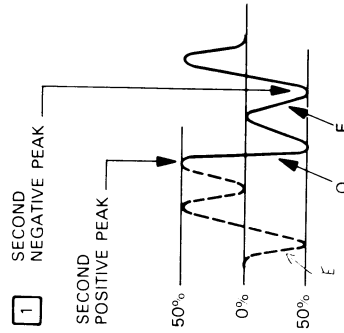


FIGURE 3-29. CARRIER SIGNAL FROM CENTERED SERVO HEAD

As shown above, the amplitudes at the SECOND POSITIVE PEAK and SECOND NEGATIVE PEAK are each 50% of maximum. The position servo sums algebraically the two second-peak amplitudes. The result being zero at point 1 means the head is located over track center.

The E and O signals at points 2 and 3 are illustrated below.

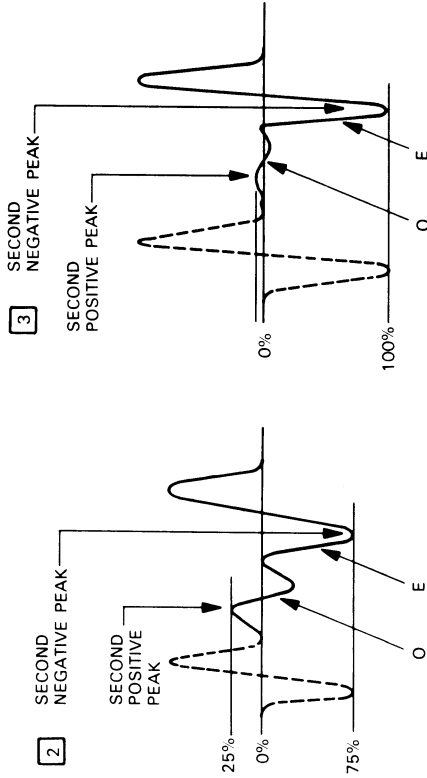


FIGURE 3-30. CARRIER SIGNAL FROM OFFSET SERVO HEAD

Point 2 portrays the offset condition wherein  $\frac{1}{4}$  of odd data and  $\frac{3}{4}$  of even data are covered by the servo head. Point 3 portrays the offset condition wherein only even data is covered by the servo head. Referring to the two illustrations above, note the following: the amplitude of a servo head signal (E or O) is proportional to the amount of servo head gap over the corresponding servo data.

### 3.4.5.3 Head Position Error

The servo carrier is sent to the position servo (one element of the servo circuits) which produces a demodulated position signal that is proportional to the amount of off track. The position signal error is proportional to the algebraic sum of SECOND POSITIVE PEAK and SECOND NEGATIVE PEAK amplitudes. The position signal amplitude indicates the amount of off track. Its polarity indicates the direction of the off track. Error correction is described in the following paragraph.

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### 3.4.5.4 Error Correction

A positive position error voltage results in head movement towards the spindle. A negative position error voltage results in head movement away from the spindle. Depending on the condition of the signal POS CYL EVEN (supplied by Input PCB), the servo attempts to move the heads to even cylinder centers or odd cylinder centers.

The servo attempts to null (eliminate) the position error signal by centering the heads over a selected cylinder location. Data used to control head movement is obtained first by demodulating the servo carrier by producing a position error signal. Its amplitude and polarity determine the amount and direction of head position correction. Current to the VCM is monitored and adjusted as needed to move the heads to the correct null position.

Consider the case of Odd Servo Data such as is written in the outer guard band area (refer to Figure 3-27). Now, suppose the heads were initially positioned at Cyl 000 Center and were pushed off track past the Cyl 001 Center when POS CYL EVEN is true (see Figure 3-31). For these suppositions, the position error signal sensed by the servo head would be as shown in waveform 2 below. The essential point of this example is that the servo system would not be able to locate the heads at the Cyl 001 Center because the direction forces ("F" in the waveform) would be in the direction of cylinders 000 and 002. Point "P" in the waveform is the stable null position for the Cyl 000 Center for the true condition of POS CYL EVEN. This condition inverts the servo carrier. The demodulated, noninverted signal carrier (for CYL EVEN false) is portrayed in waveform 1 below.

While viewing the directions of forces (arrows) at cylinder centers in the illustration above, note the following:

- For POS CYL EVEN false, positioning the head at the centers of Cylinders 000 or 002 would constitute an unstable positioning mode. Positioning at 001 or 003 would constitute a stable positioning mode.
- For POS CYL EVEN true, the reverse situation exists.

The signal POS CYL EVEN is an input to the servo preamplifier. Inverting or not inverting this signal allows the heads to be positioned at both odd and even cylinder locations.

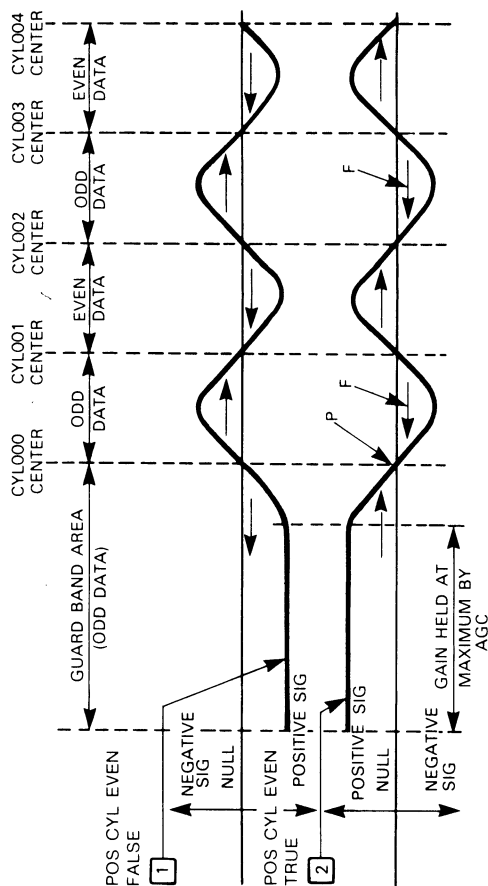


FIGURE 3-31. HEAD POSITION ERROR CORRECTION

Inverting the servo carrier results in an opposite polarity position error voltage to provide the correction forces in the opposite direction. This change in force direction can be seen by comparing waveforms 1 and 2 in the illustration above.

### 3.4.6 Servo Circuits

Servo circuits maintain proper cylinder positioning and head positioning during normal drive operation, and accomplish emergency head retraction from the pack if a serious drive malfunction is detected. To provide these functions, the servo circuits receive the servo head signal and tach output from the access mechanism, and outputs from every system in the drive which contains electronic circuitry (Operator Control System, DCL Support System, Read/Write System, Spindle Control System, and Power System). These systems receive inputs generated by the servo circuits. Figure 3-32 shows the inputs received by elements of the servo circuits (six PCBs), and the outputs transmitted to PCBs outside the Servo System.

Servo circuits are contained in six PCBs. They are: SVTL (Servo Control), VSER (Velocity Control), PAMP (Servo Preamplifier), PSER (Position Control), IDEX (Index), and SAMP (Servo Power Amplifier). Individual functions are indicated in their names. Figure 3-33 shows these PCBs, addressing the signals which they generate for use internally.

In the following paragraphs, each one of the six PCBs containing servo circuits is described individually. Use Figures 3-32 and 3-33 to retain PCB orientation with the Servo System; the combination of these figures amounts to a complete system block diagram (which is not provided in one page because of the number of interfacing signals involved).

### 3.4.7 Servo Power Amplifier PCB

SAMP provides current to drive the VCM. It operates in one of three system operating modes described in paragraph 3.4.2 (Position Control, Velocity Control, and Emergency Retract modes), each as discussed below.

SAMP controls current to the VCM through five transistor switches when operating in the Position Control or Velocity Control modes. These switches are named Upper Center Tap, Upper Forward, Upper Reverse, Lower Forward, and Lower Reverse. Figure 3-34 shows the control of these switches. Referring to the figure, the analog signals LIN DRIVE FWD and LIN DRIVE REV provide forward or reverse current proportional to the position error when LIN AMP ENABLE is true. MINUS FWD DRIVE and MINUS REV DRIVE are logic signals; their duty cycle is proportional to the velocity error when operating in the Velocity Control mode.

#### 3.4.7.1 Operating in the Position Control Mode

Referring to Figure 3-35 for operation in the Position Control mode, SAMP uses the Upper Center Tap switch with the Lower Forward and Lower Reverse switches operating in their linear region. Current flows through the center tap, to one of the two lower switches which is regulated by LIN DRIVE FWD or LIN DRIVE REV. These switches are disabled if retract power is received before upspeed is achieved. When disabled, current cannot flow through either side of the amplifier bridge because the base drives for the lower switches are clamped.

SAMP contains discrete components which provide safety against short circuiting the power supply due to both lower switches conducting simultaneously.

#### 3.4.7.2 Operating in the Velocity Control Mode

In the Velocity Control mode, SAMP operates as indicated in Figure 3-36 (forward drive state) or Figure 3-37 (reverse drive state). Referring to either figure, SAMP operates in this mode as a high current switch. The Center Tap is not used. The operating state, either forward (toward spindle) or reverse (away from spindle), is determined by the MINUS FWD DRIVE and MINUS REV DRIVE inputs. In the forward drive state (Figure 3-36), the Upper Forward and Lower Forward switches in the VCM are used. In the reverse drive state (Figure 3-37), the Upper Reverse and Lower Reverse switches are used.

#### NOTE

The portrayal, in Figures 3-36 and 3-37, of forward drive and reverse drive being independently executed has been allowed for instructional purposes only. During operation in the Velocity Control mode, the servo controls velocity as described in paragraph 3.4.7.2 and Figure 3-44.

#### 3.4.7.3 Operating in the Emergency Retract Mode

In the Emergency Retract mode, SAMP operates as indicated in Figure 3-38. Referring to this figure, the Emergency Retract Power Amp is activated when operation in the Emergency Retract mode is initiated. It turns on and off to maintain necessary velocity control during retraction.

The following conditions will initiate an emergency retract operation:

- An elapsed time of 640 msec after initiation of the RETRACT HDS signal and the carriage is not in the fully retracted position.
- CLEAR is true, which indicates either the loss of dc voltage or loss of voltage regulation.
- Servo current greater than 8 amps for an uninterrupted period of 975 msec.
- Loss of 50 Vdc with the heads not retracted.

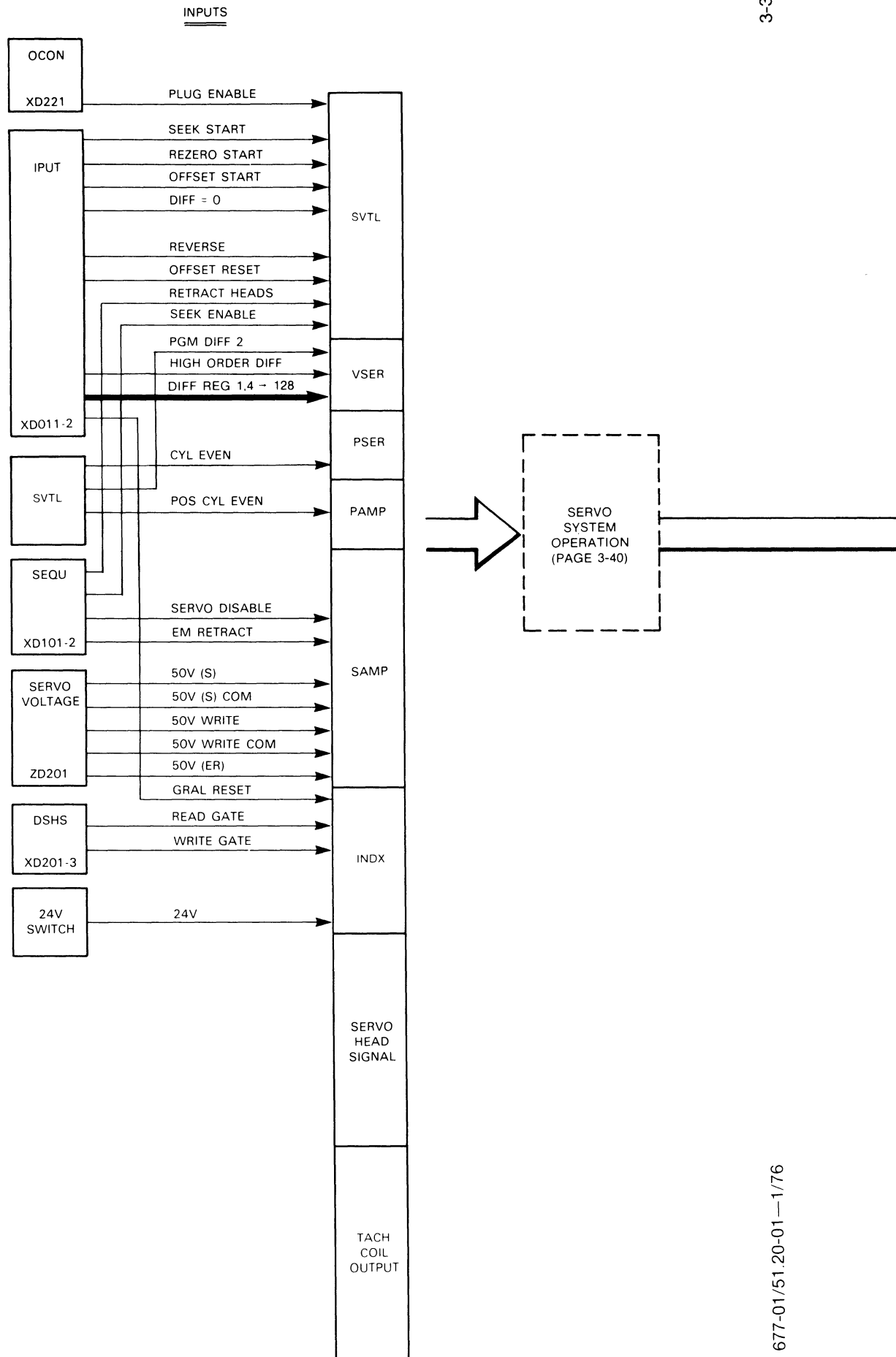


FIGURE 3-32. SERVO SYSTEM INPUTS AND OUTPUTS (Part 1 of 2)

OUTPUTS

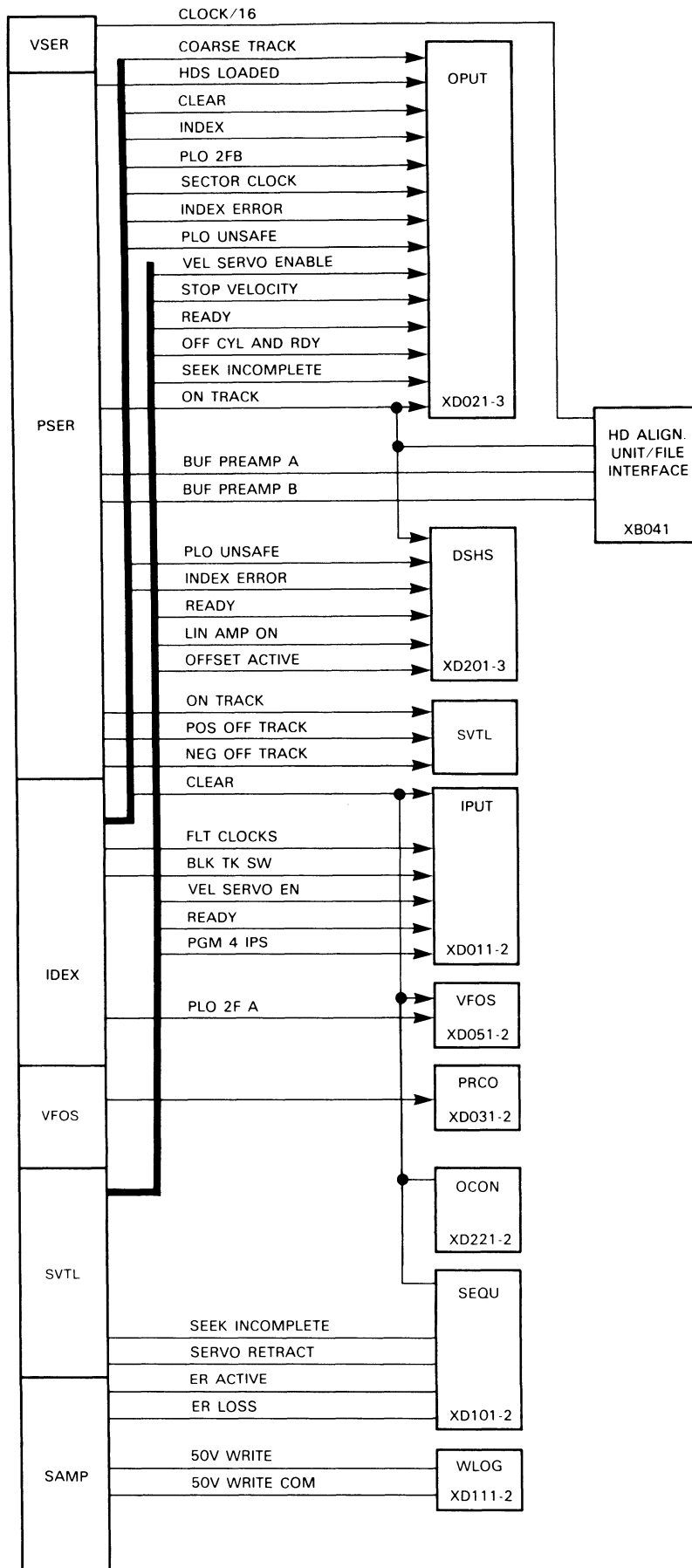


FIGURE 3-32. SERVO SYSTEM INPUTS AND OUTPUTS (Part 2 of 2)

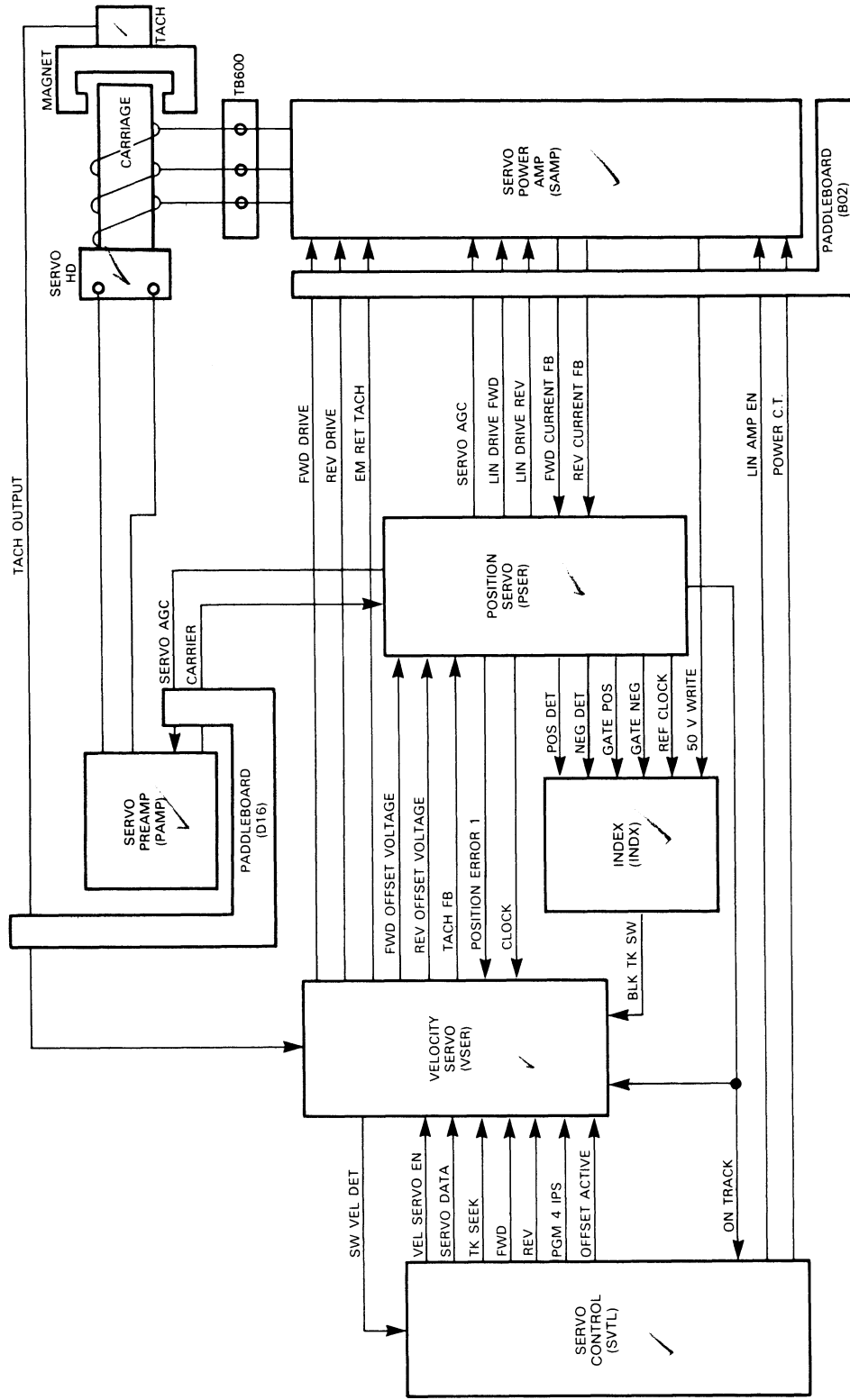


FIGURE 3-33. SERVO SYSTEM INTERNAL OPERATION

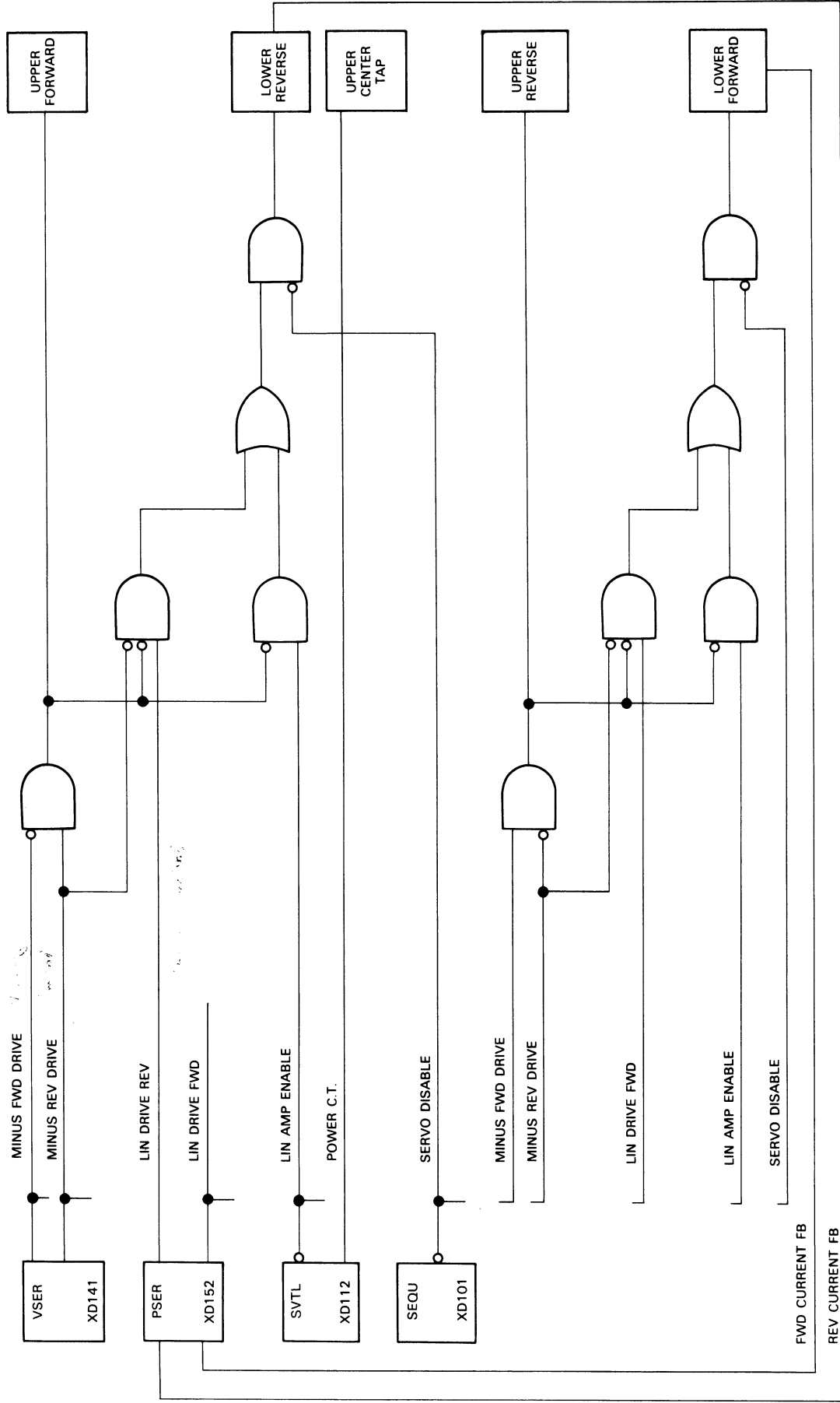


FIGURE 3-34. SERVO POWER AMPLIFIER PCB NORMAL OPERATION

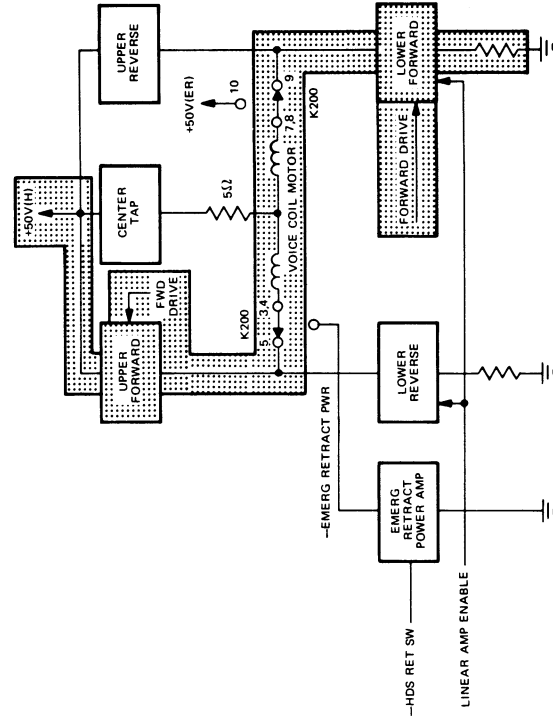


FIGURE 3-35. POWER AMP IN POSITION CONTROL MODE

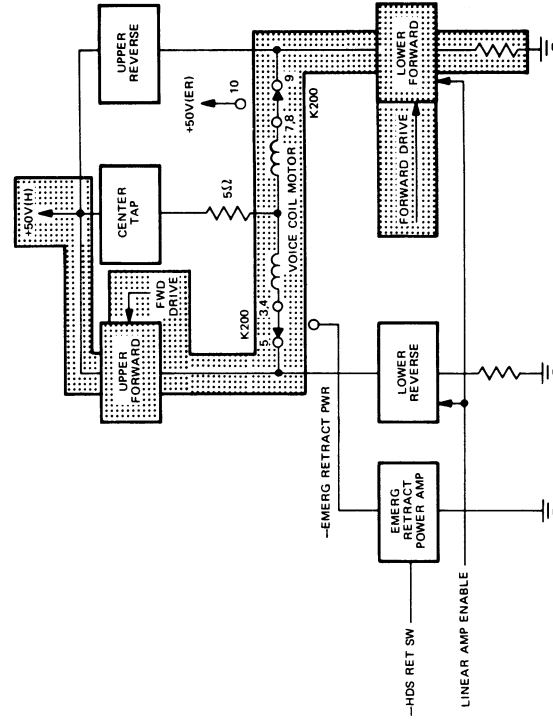


FIGURE 3-36. POWER AMP IN VELOCITY CONTROL MODE, FORWARD



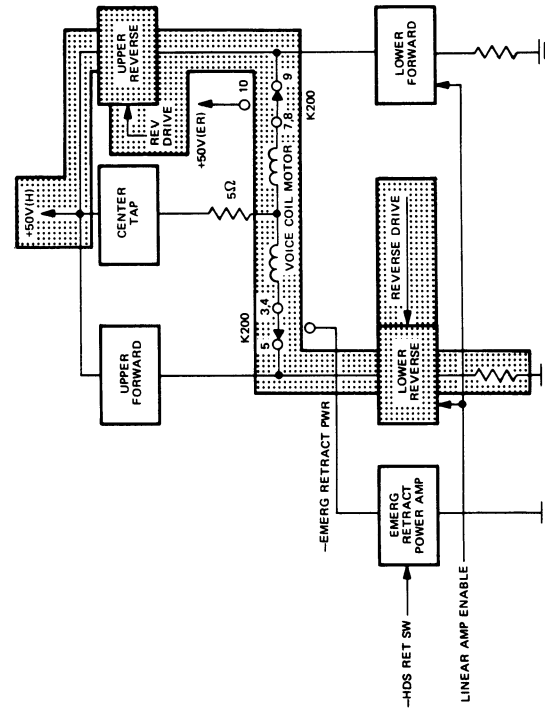
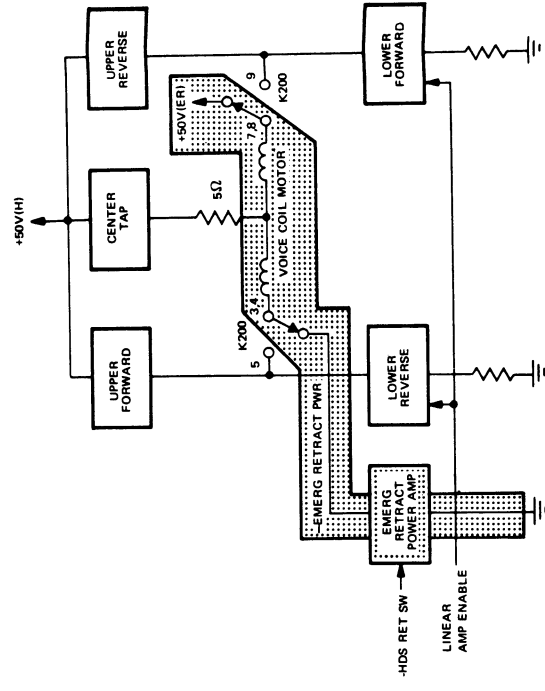


FIGURE 3-37. POWER AMP IN VELOCITY CONTROL MODE, REVERSE

FIGURE 3-38. POWER AMP IN EMERGENCY RETRACT MODE

Figure 3-39 shows the circuitry used to execute an emergency retract operation. It is described below.

- Operation begins when transferring the relay K200, and applying Retract Power to retract the heads.
- Retract Power Amp is a high current switch that allows current to flow through the bobbin for carriage retraction. When fully retracted, HDS RET SW being true turns the Retract Power Amp off.
- EM RETRACT TACH signal is used by Emergency Retract Speed Control, which compares this signal with an internal reference voltage. The comparison results in turning the Retract Power Amp on and off to control current in the bobbin. Controlling this current controls the speed of carriage retraction.

### 3.4.8 Servo Preamplifier PCB

PAMP is described below, addressing the area in Figure 3-40 within the dashed block.

#### 3.4.8.1 Reading Servo Head Signal and Adjusting Gain

PAMP reads directly and amplifies the signal from the servo head and adjusts gain to maintain a uniform output voltage on all tracks. Refer to Figure 3-40. Preamp sends the head signal to AGC Amp for gain control. The gain-adjusted and amplified signal is sent, through Line Driver, to the carrier amp in the position servo for further amplification. For an on-track condition, carrier amp output is held constant using the SERVO AGC signal provided by AGC detector to AGC Amp.

#### 3.4.8.2 Inverting or Noninverting the Head Signal

Referring to Figure 3-40, Track Switch receives the POS CYL EVEN input and, depending on the state of this signal, inverts or noninverts the head signal as described in paragraph 3.4.5.4.

### 3.4.9 Position Servo PCB

PSER processes the servo head signal (preamp output) to determine and control head positioning relative to track center, and provides position indications and repositioning current to interfacing PCBs in the Servo System. It also provides on-track and heads-loaded indications to circuits outside the Servo System for verifying data safety and responding to DCL commands for status information. Functions provided by PSER are described below, addressing the block diagram in Figure 3-40.

#### 3.4.9.1 Track Following

In a track-follow operation, the desired data head position is over track center. Referring to Figure 3-40, the existing head position is indicated in a dc position error signal (POSITION SIGNAL). The amplitude and polarity of the Position error determines the amount and direction of the required head positioning adjustment. Track Detector output signals are used for track counting and R/W in-ops.

Data Head Deviation	Position Signal	Head Correction
None	0	None
Toward spindle	-	Reverse
Away from spindle	+	Forward

POSITION SIGNAL is generated and used as follows (refer to Figure 3-40):

- Carrier Amp provides the amplified servo head signal to Positive Detector, Negative Detector, and a Servo Clock. They provide the gates for entry of the head signal to the peak detectors.
- Positive Peak Detector and Negative Peak Detector detect the second positive peaks and second negative peaks of the head signal (respectively). These gated peaks charge capacitors to dc values proportional to the amplitudes of the second-positive and second-negative peaks.
- Summing Amp takes the dc values from the detectors and sums them together to provide the dc position error signal (POSITION SIGNAL). This signal is sent to Track Detector which provides logic levels indicating the head positioning, and to the Compensation Amp.

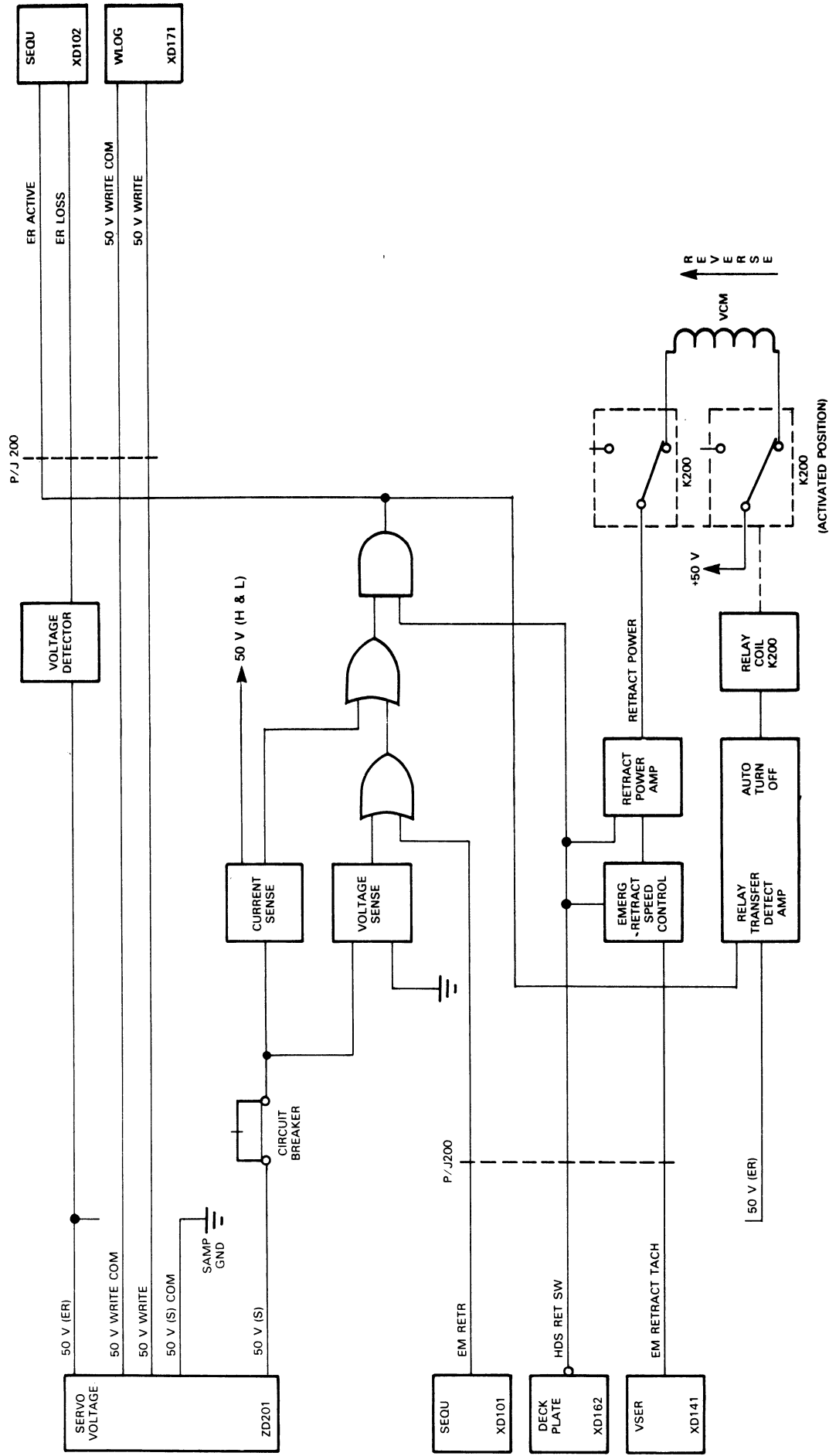


FIGURE 3-39. SERVO POWER AMPLIFIER PCB, EMERGENCY RETRACT OPERATION

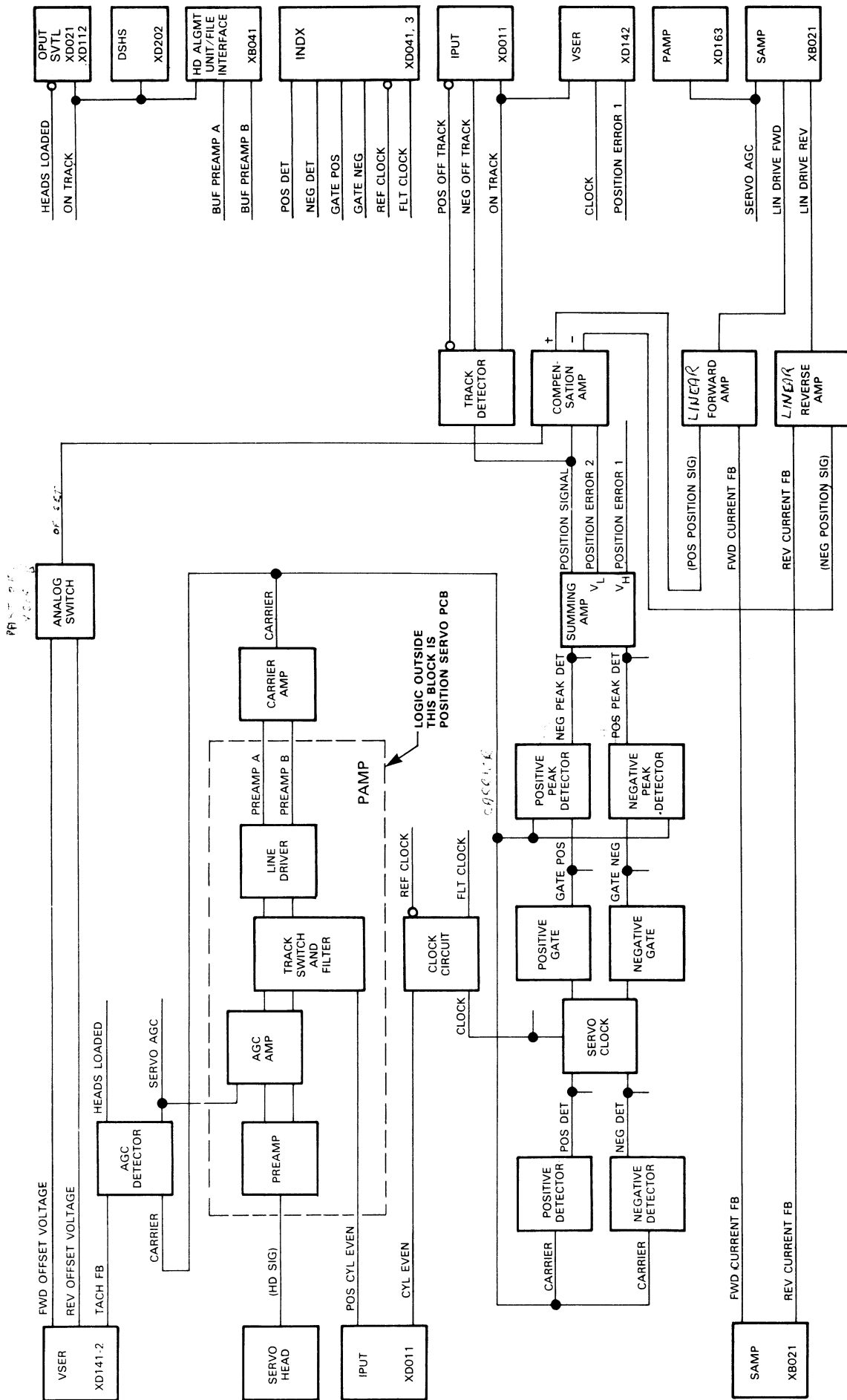


FIGURE 3-40. SERVO PREAMPLIFIER PCB AND POSITION SERVO PCB

- Comp Amp provides frequency compensation which adjusts and stabilizes the response of the overall servo system. To clarify the relationship between Comp Amp, Summing Amp, and the detectors, consider the following example. Suppose the servo head is displaced from track center in a forward (toward spindle) direction. For this condition, Summing Amp would develop a negative position signal. This signal conditions Comp Amp to initiate reverse current in the VCM to make the heads move away from the spindle.

- Depending on polarity, the position signal is processed by Forward Amp or Reverse Amp. These amplifiers, in conjunction with the Servo Power Amp (SAMP), control current to the VCM as a function of position error. SAMP drivers provide forward or reverse current through the VCM, and current feedback (FWD CURRENT FB and REV CURRENT FB) to Forward Amp and Reverse Amp.

### 3.4.9.2 Offset Track Following

The capability of track following a predetermined number of microinches (proportional to position signal amplitude) off either side of track center (offset) is useful during error recovery and head alignment operations. For example, if data errors are experienced, the heads can be offset to either side in an attempt to recover the data.

Offset is accomplished by summing a voltage, proportional to the amount of offset desired, into Comp Amp along with the position error signal. This causes the compensating circuits to react as though the heads were at track center when in reality they are actually offset slightly. When the offset value (FWD or REV OFFSET VOLTAGE) is summed with the actual position signal, the position servo attempts to zero the summed signal by moving the heads. For example, suppose a reverse offset operation is desired. For this condition, REV OFFSET VOLTAGE is sent to Comp Amp through the Analog Switch; FWD OFFSET VOLTAGE is not active. This causes the head to move in reverse, to track-follow off track to the point where the position signal has an amplitude and polarity that cancels the REV OFFSET VOLTAGE input.

During an offset operation, the direction and amount of offset is controlled by a value placed in the difference counter, as shown below.

Difference Counter Position	Offset Information
128	Reverse (Not 128 is Forward)
64	(not used)
32	800 microinches
	(100 Megabyte drive only)
16	400 microinches
8	200 microinches
4	100 microinches
2	50 microinches
1	25 microinches

For example, to perform a 325 microinch offset in the reverse direction, cylinder difference/offset lines from the DCL to the drive would turn on difference counter positions 128, 8, 4, and 1.

### 3.4.9.3 Developing Index and Supporting Data Timing

The Servo Clock shown in Figure 3-40 is an oscillator phase-locked to the servo carrier by POS DET and NEG DET signals. Its primary function is to gate the "proper" peaks from the carrier into the two peak detectors. These signal outputs are shown in the figure as GATE POS and GATE NEG. They are used in head positioning, as described in the two preceding paragraphs, and to support index detection and write data timing as discussed below.

Index is a fixed pattern of missing servo pulses. This pattern is illustrated in Figure 3-41. Index detection circuits in the Index PCB monitor the POS DET, NEG DET, GATE POS, GATE NEG, and REF CLOCK outputs to detect index.



FIGURE 3-41. INDEX PATTERN

Since the Servo Clock is generated by the carrier that is written on the disc, the frequency of the clock output pulses is directly proportional to disc rotational speed. Therefore, the Servo Clock outputs are additionally used by the DCL to synchronize the timing of data written in the pack.

#### 3.4.9.4 Supporting Velocity Control

The CLOCK signal from Servo Clock, the high-voltage position error signal from Summing Amp (POSITION ERROR 1), and the ON TRACK signal from Track Detector, are transmitted to VSER, which controls carriage velocity as described in paragraph 3.4.10.1.

#### 3.4.9.5 PSER Performance Requirements

**Regulated Voltages.** Voltage at D15-TP11/R14 equals  $+11.4 \text{ Vdc} \pm 10\%$ . Voltage at D15-TP12/R31 equals  $-5.6 \text{ Vdc} \pm 10\%$ .

### 3.4.10 Velocity Servo PCB

VSER supports system operation in the Velocity Control mode by controlling carriage velocity. The logic used is described below, addressing the block diagram in Figure 3-42.

- When conditioned by TK SEEK true, Analog Gate 1 gates the high-voltage position error signal (POSITION ERROR 1) to the inverting or noninverting pin of the Velocity Scheduler as programmed velocity for the last  $\frac{3}{4}$  track of the seek after difference counter has already gone to zero. For FWD true, the error signal is gated to the noninverting pin.
- DAC produces an analog current proportional to the binary value in the difference counter. This current is an input to the Velocity Scheduler.
- Velocity Scheduler converts the received current to a scheduled velocity curve. The method used is described in paragraph 3.4.10.1.
- Analog Gate 2 gates the forward or reverse program velocity signal to the inverting or noninverting pin of the Velocity Error Amp.
- Velocity Error Amp compares voltages proportional to the scheduled and actual carriage velocities, and sends the result to the Pulse Width

Modulator. It converts the voltage difference to logic signals FWD DRIVE and REV DRIVE. The conversion is accomplished as described in paragraph 3.4.10.2.

- Triangle Generator converts "divided by 16" clock pulses (CLOCK/16) to a triangle waveform (SAWTOOTH). It is used by the Pulse Width Modulator, as described in paragraph 3.4.10.2.
- Tach Buffer Amp amplifies the tach output, which is proportional to actual velocity.
- Velocity Detector sends an indication to the servo control logic when actual velocity is 0.5 in/sec or less.

Specific functions provided by VSER are described in the following paragraphs.

#### 3.4.10.1 Scheduling of Seek Velocity

The Velocity Scheduler (Figure 3-42) generates a desired velocity curve during a seek operation in the Velocity Control mode. It operates to position the carriage to the desired track in the shortest time. The method of operation is described below, addressing Figure 3-43.

- Actual Carriage Velocity is monitored using the tachometer. Tach output is proportional to this velocity.
- Actual Carriage Velocity is compared with the Ideal Scheduled Velocity curve. This curve corresponds to a specific number of tracks that remain to be moved (difference count).
- Scheduled Velocity curve is a modified analog conversion of the value in the difference counter.
- The carriage is made to follow the Scheduled Velocity curve by controlling current in the VCM.

During acceleration, full current is applied to the VCM, and the output of the Velocity Error Amp (Figure 3-42) goes to saturation. The Velocity Scheduler's output is a function of the difference count (input) and is clamped to approximately  $-9\text{v}$  whenever the count is greater than 80. This clamping action limits velocity.

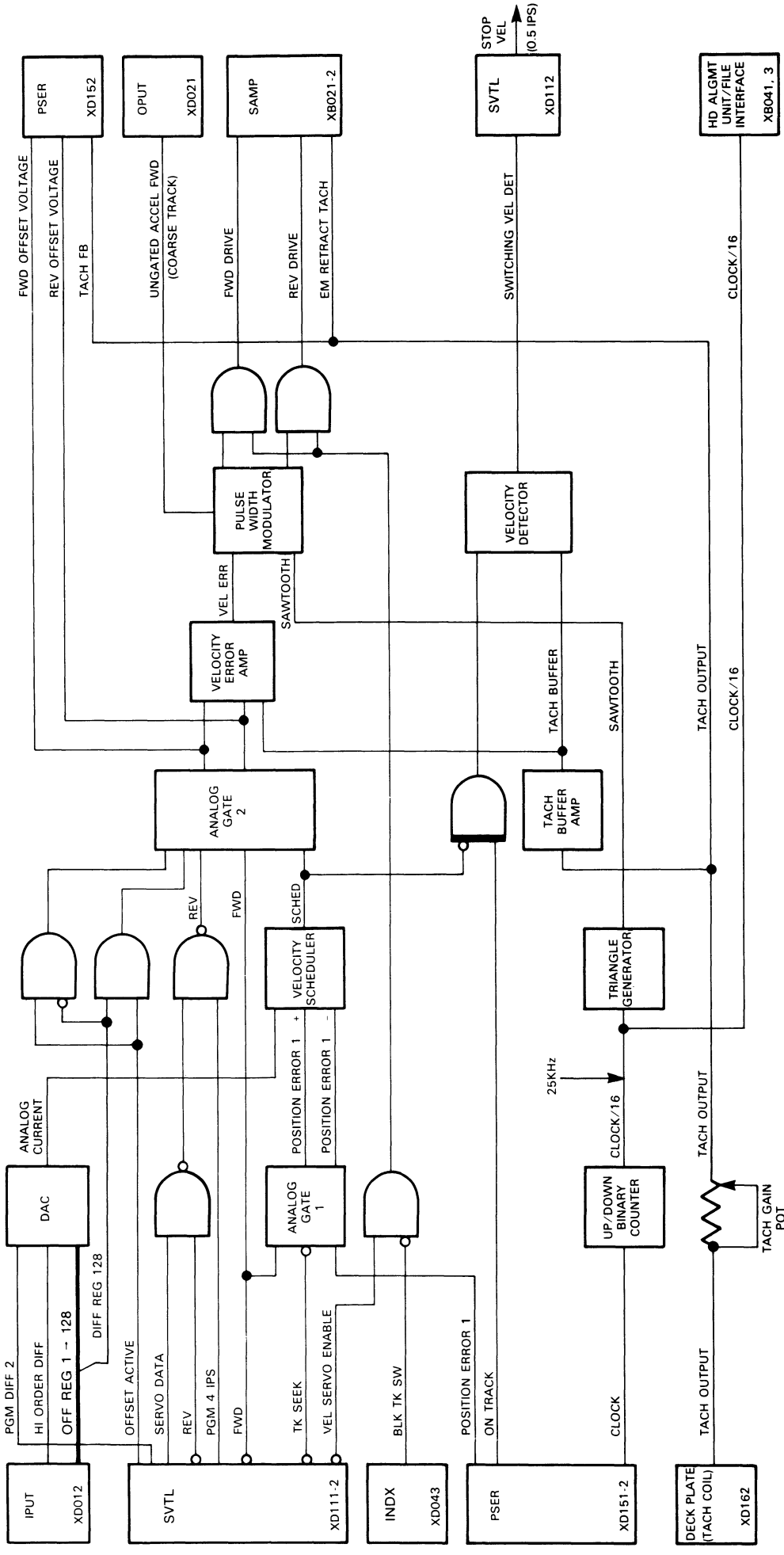


FIGURE 3-42. VELOCITY SERVO PCB

### 3.4.10.2 Providing Linear Power Control

Scheduled velocity (forward and reverse voltages) and actual velocity (amplified tach output) are sent to the Velocity Error Amp which determines the velocity difference (velocity error voltage). When the velocity difference is approximately 1 in/sec, voltages to the servo power amp (logic conversions FWD DRIVE and REV DRIVE) become pulse-width modulated. At this point, VSER enters a linear power control state. Velocity control during this state, and just before entering this state, is described below.

Referring to Figure 3-44, VELOCITY ERROR is compared with the 25 kHz SAWTOOTH. When the error is approximately 1 in/sec, a Pulse Width Modulator generates the modulated signals which gate voltages across the VCM. These signals cause the VCM to be pulsed with a duty cycle dependent on the velocity error, as shown in Figure 3-44. Notice in the figure the period of no modulation when the error is greater than 1 in/sec.

### 3.4.10.3 Terminating Velocity Control

The Velocity Detector (Figure 3-42) output is sent to servo control circuitry. It terminates operation in the Velocity Control mode and goes into the position mode (VEL SERVO ENABLE is false) when the absolute velocity is detected at less than 0.1 in/sec by the Velocity Detector.

### 3.4.10.4 Transmitting Offset Value

If servo control circuitry indicates an offset operation (OFFSET ACTIVE is true), the desired amount of offset is contained in the difference counter and the state of DIFF REG 128 indicates the direction of offset. As shown in Figure 3-42, the offset amount and direction are sent to Analog Gate 2, which gates the offset information (as FWD and REV OFFSET VOLTAGE) to the position servo for offset head positioning.

### 3.4.10.5 Responding to a DCL Command

If the Pulse Width Modulator (Figure 3-42) indicates an ungated accelerate forward condition of the carriage is underway, this condition is indicated to OPUT which sends the indication to the DCL as the signal COARSE TRACK.

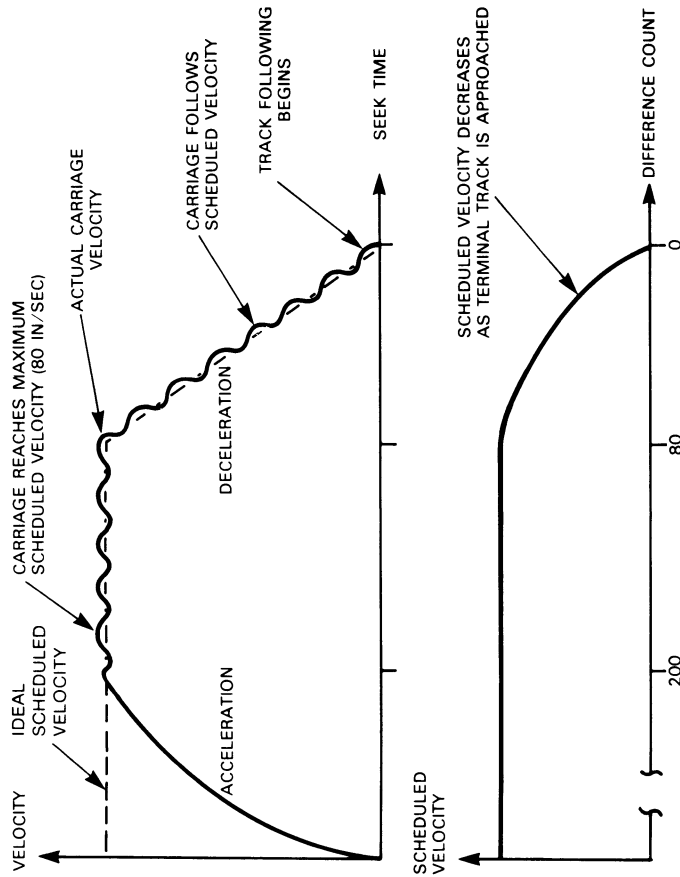


FIGURE 3-43. SCHEDULING SEEK VELOCITY



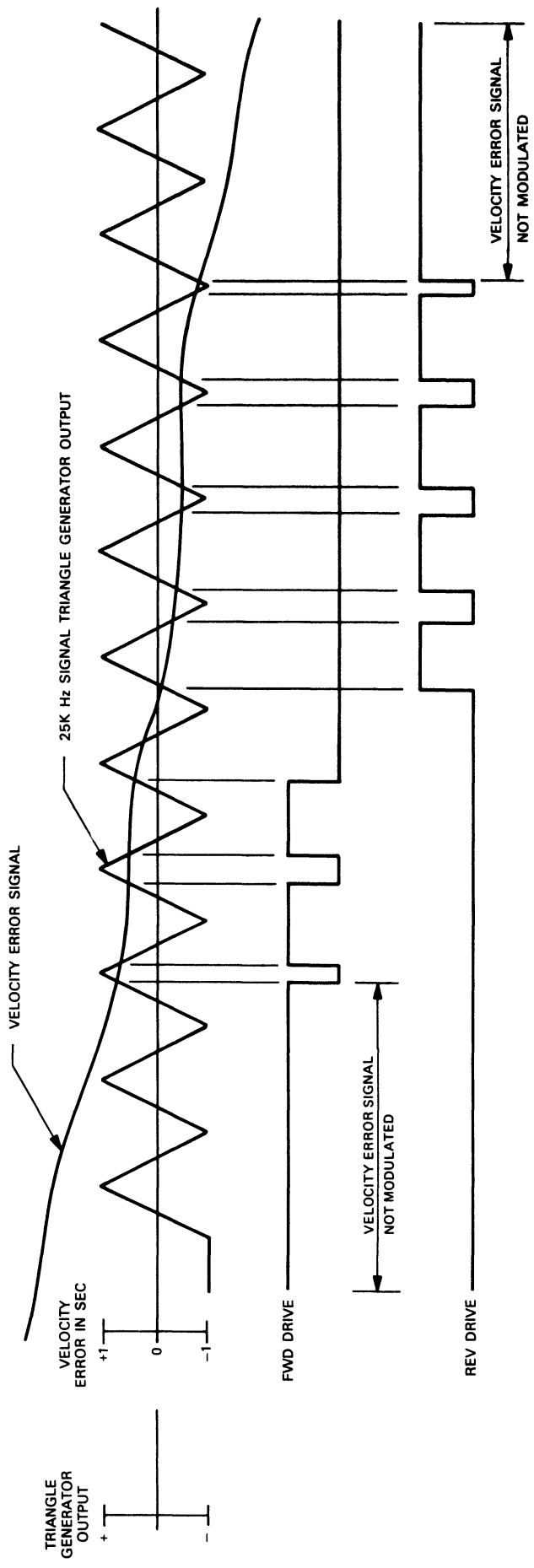


FIGURE 3-44. PULSE WIDTH MODULATION

### 3.4.11 Index PCB

INDEX detects pack index, and provides outputs used in data precompensation and VFO operation, as described below.

#### 3.4.11.1 Detecting Index

Index is a fixed pattern of gaps in the servo data. Each gap consists of two missing dipulses. Referring to the timing chart in Figure 3-45 and the logic block diagram in Figure 3-46, index is detected as follows:

- Gaps are detected by two latches that comprise the Gap Detector. Both are reset by the NORed result of POS DET and NEG DET, and clocked by the ORed result of GATE POS and GATE NEG. If the first latch is set, the second is set. A positive output from the second latch indicates detection of two missing dipulses, which defines a single index gap.
- When an index gap is detected, a zero is shifted into a 6-bit Shift Register.
- The index pattern is decoded (INDEX is true) by Index Decode in the index window. If not decoded in the index window, or if decoded outside the index window, INDEX ERROR is generated.

#### 3.4.11.2 Block TK SW

Block TK SW is used to prevent inverting the output of the Servo Preamp (controlled by the cylinder even latch on the SVTL PCB) and to prevent current switching in the velocity mode during the time the index gaps are being detected by the servo head.

#### 3.4.11.3 Generating PLO Outputs

PLO and Clock Circuits (Figure 3-46) generate outputs used in write precompensation and VFO operation, as described in paragraph 3.3.5.1.

#### 3.4.11.4 Checking for Power Failure

Power Fail Logic (Figure 3-46) generates an indication of unsafe voltage if present, as described in paragraph 3.3.5.2.

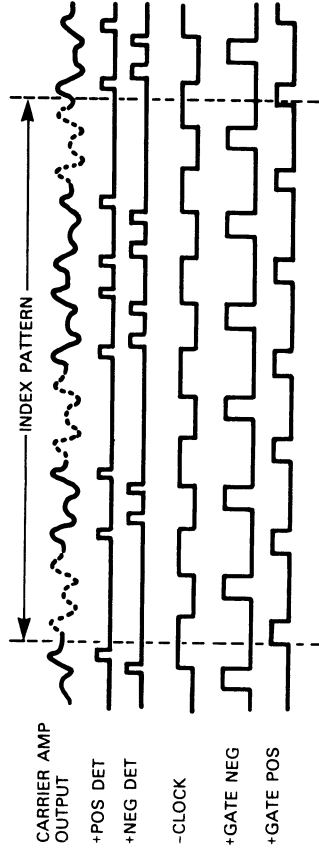


FIGURE 3-45. SERVO CLOCKING FOR INDEX

#### 3.4.11.5 INDEX Performance Requirements

Index requirements are presented below (refer to figure 3-46).

- When either on track or seeking between tracks using a standard disc pack, INDEX is detected and INDEX ERROR is false.
- INDEX is true every  $16.67 \pm 0.33$  msec. Duration of INDEX true is  $620 \pm 100$  nsec.
- SECTOR CLOCK true has a nominal period of  $1.24 \mu\text{sec}$ , and occurs 13,440 times between true transitions of INDEX.
- INDEX ERROR is true when the heads are retracted.
- If INDEX does not occur during INDEX WINDOW TP, or occurs outside of INDEX WINDOW TP, INDEX ERROR becomes true and remains true until INDEX occurs during INDEX WINDOW TP.



### 3.4.12 Servo Control PCB

Using indicators of Servo System status, control panel status, and DCL commands of the drive, SVTL provides for a logical progression of servoing events as needed to control system operations. It enables seek or recalibrate operations and the servo power amp, detects an incomplete seek or servo error, permits velocity or position control, terminates velocity control, and, depending on system status, either initiates, delays, or resets the system ready-to-operate indication. In addition, SVTL sends system status indicators to data safety circuits (DSHS), spindle control circuits (SEQU), and the DCL (via OPUT).

Figure 3-47 shows the sources of inputs to SVTL (left side of figure), destinations of outputs generated (right side), and SVTL logic divided into nine functional segments (middle portion of figure). Dividing the logic into segments, each defining a particular control state of the system, provides the basis used to organize the description of SVTL which follows. This figure allows orientation to the servo control states, and provides a single reference for all SVTL inputs and outputs.

As shown in Figure 3-47, segments of logic receive inputs from external and internal sources, the latter including timers in most cases. Six timers are used; they are described in Figure 3-48. All are retriggerable one shots. Since a false-to-true transition in the input logic to each one shot restarts its timing cycle, input conditions cannot be ignored (may change) during timeout of any one shot. Addressing changing conditions in the design allows servoing in the shortest time. (For this reason, mechanical events occurring at the end of the six timeout periods, while the system progresses from one control state to another, are variable to the degree that a discussion would have little general value.)

In the following paragraphs, each segment of logic shown in Figure 3-47 is described, addressing the outputs generated (except timer outputs, which are addressed above) while the system progresses from one control state to another.

#### 3.4.12.1 Enabling Servo Logic

Seek Enable Logic (Figure 3-47) generates SERVO LOGIC ENABLE, which must be true to enable all other segments of servo control logic to operate.

As shown in Figure 3-49, SERVO LOGIC ENABLE is latched true when the drive is prepared for normal operation (SEEK ENABLE is true), and Timers T2 and T6 have been tested.

The system can arrive at a disable state from any other state by dropping SEEK ENABLE. It can leave the disable state only by the logic raising SEEK ENABLE. When raised, the system enters a test state. At this time, T1, T2, and T6 are started. After T2 and T6 have timed out, correct timer operation is assured.

#### 3.4.12.2 Enabling Rezeroing

Rezero Logic generates D0 REZERO, which must be true to enable a recalibrate operation. Referring to Figure 3-47, this operation can be executed by enabling the power amp, enabling the velocity servo, and completing a seek to track 000.

As shown in Figure 3-49, D0 REZERO is latched true when a head load is initiated, the LAP plug is removed and replaced, a rezero start is received, or a servo error is detected.

#### 3.4.12.3 Enabling Velocity Control

Velocity Servo Enable Logic (Figure 3-47) generates VELOCITY ENABLE.

As shown in Figure 3-50, D0 REZERO being true starts T1 and T2, setting the Velocity Enable latch. VELOCITY ENABLE is latched true when T6 is additionally started (servo logic is enabled), provided the difference count is not zero and the latch is not reset by STOP VELOCITY.

VELOCITY ENABLE may be true with heads retracted or extended.

#### 3.4.12.4 Stopping Velocity Control

Velocity Stop Logic (Figure 3-47) generates STOP VELOCITY, which becomes true when the carriage has effectively stopped, and stopping terminates the Velocity Control mode.

Refer to Figure 3-50. Unless blocked by T3 or T4, STOP VELOCITY is latched true when carriage motion is so slow (0.5 in/sec) that switching to the Position Control mode is indicated (SW VEL DET is true).

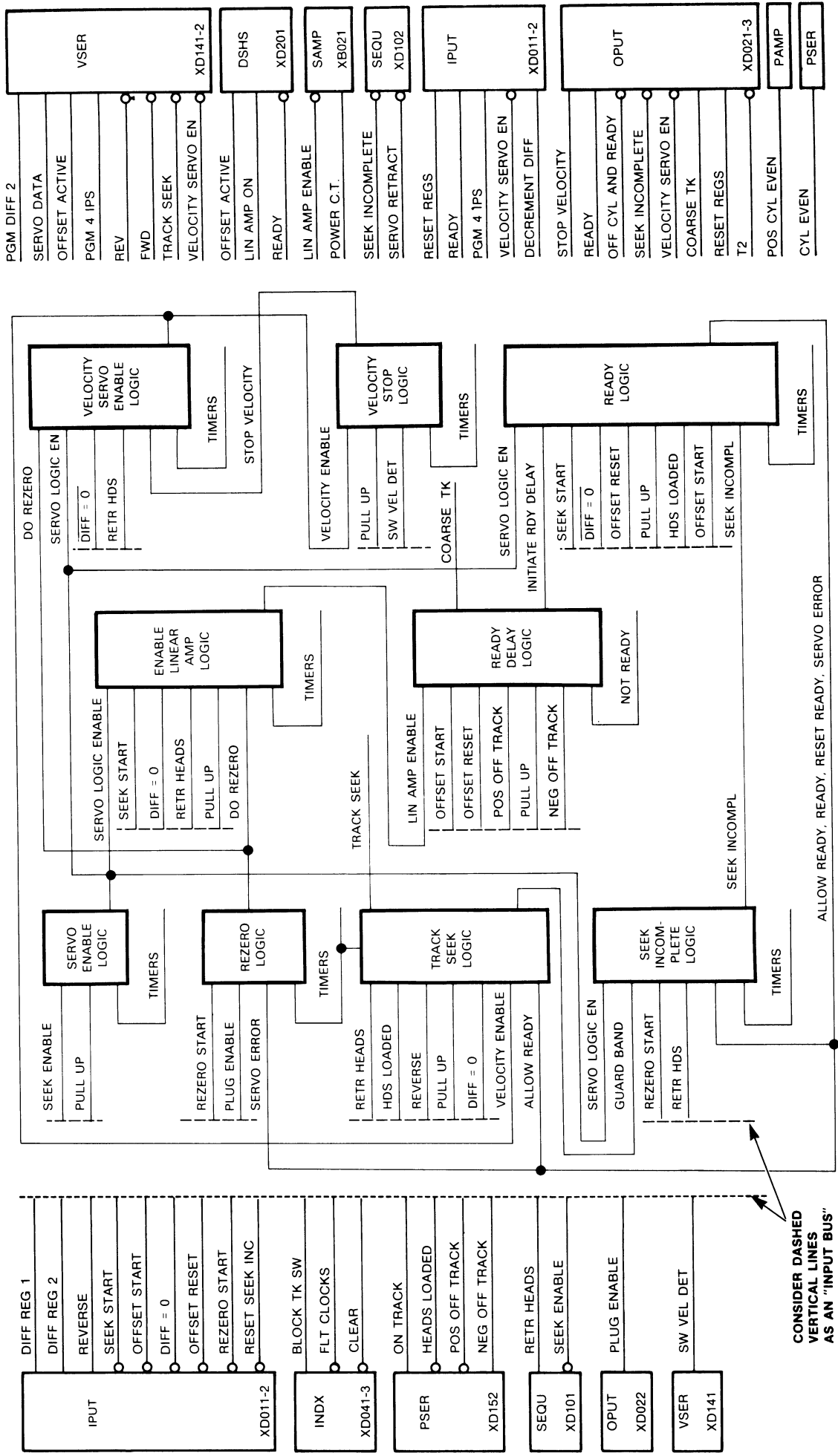


FIGURE 3-47. SVTL FUNCTIONS, INPUT SIGNALS USED, AND OUTPUTS GENERATED

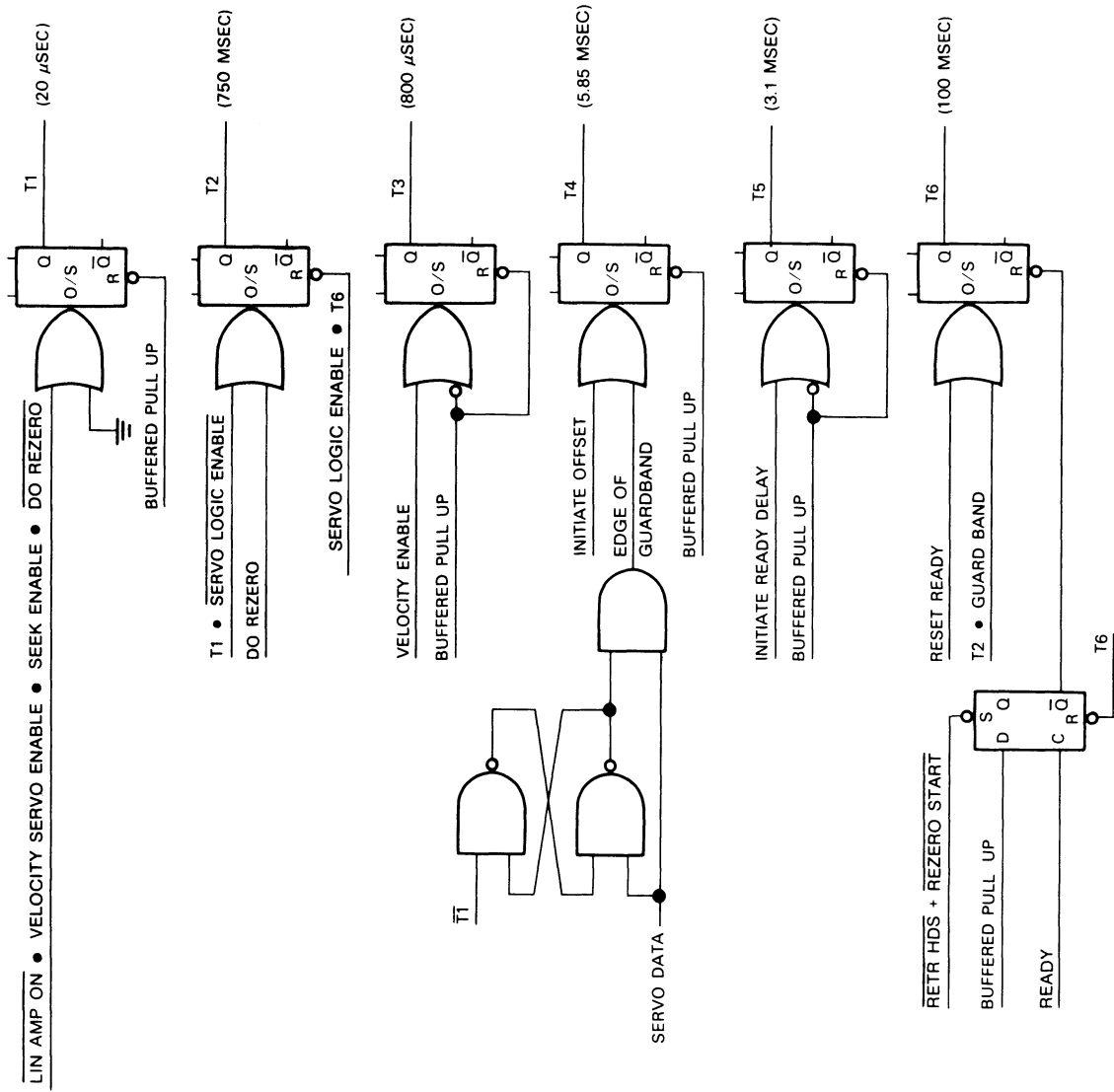


FIGURE 3-48. SVTL ONE SHOTS

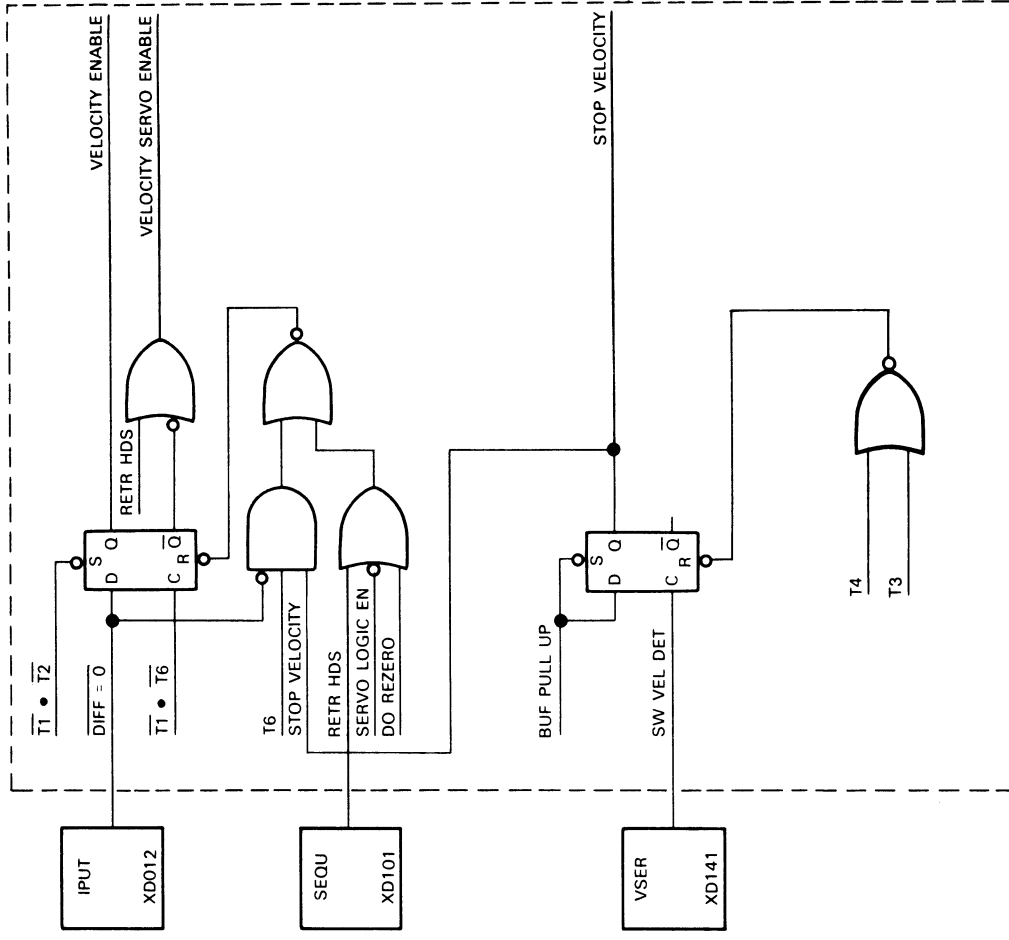


FIGURE 3-50. VELOCITY ENABLE AND STOP VELOCITY

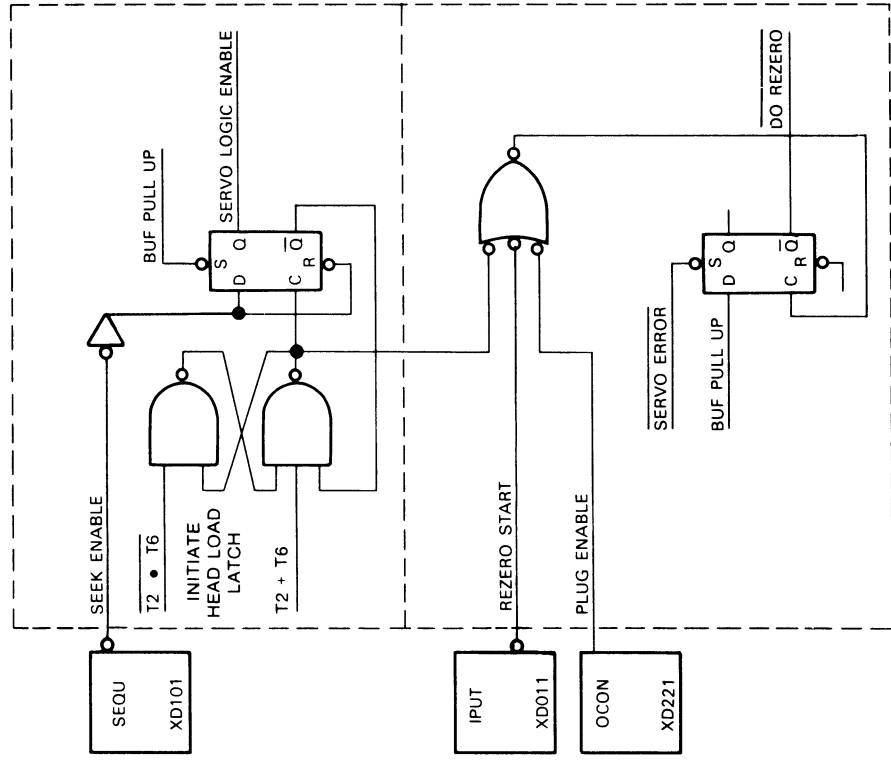


FIGURE 3-49. SERVO LOGIC ENABLE AND DO REZERO

### 3.4.12.5 Enabling Power Amp

Enable Linear (Power) Amp Logic generates LIN AMP ENABLE, which must be true as one indication the system is ready to seek (Figure 3-47).

Referring to Figure 3-51, LIN AMP ENABLE is latched true when T1 times out, provided the latch is not reset.

### 3.4.12.6 Delaying Ready

Ready Delay Logic (Figure 3-47) generates INITIATE RDY DELAY, which must become true to provide the time period needed for head settling.

STOP VELOCITY being true sets T1, and when timed out the system is in the Position Control mode. Referring to Figure 3-51, COARSE TRACK becomes true when the carriage has positioned the heads near track center. This signal being true allows INITIATE READY DELAY becoming true, provided the linear amp is on and the system is not already in the ready state (READY is false).

### 3.4.12.7 Allowing Ready

Ready Logic (Figure 3-47) generates READY, which must be true to enable seeking in the Velocity Control mode.

Referring to Figure 3-51, READY is latched true when T5 (the initiate ready delay) times out, provided T6 has not timed out and the latch is not reset by one of the five reset conditions shown in the figure. How each reset condition is generated is shown in this figure (or Figure 3-52), except for OFFSET START; it takes the logic from the ready state for 5.85 msec (T4) to allow time for offset positioning by the programmed amount.

### 3.4.12.8 Enabling a Seek

Track Seek Logic (Figure 3-47) generates TRACK SEEK, which must be true to condition the analog gate in the velocity servo which gates the position error signal to the velocity scheduler.

Referring to Figure 3-52 (lower right area), initiating a track seek is allowed (TRACK SEEK is true) before T6 times out, provided the velocity servo is enabled (VELOCITY ENABLE is true) and the difference count is zero (DIFF=0 is true). Major events leading to initiation of a track seek during a rezero are (refer to lower half of figure):

- When VELOCITY ENABLE is true, the logic checks for servo data to determine whether the heads are loaded. If servo data is detected (meaning heads loaded), the carriage moves in reverse direction (REV is true) at 4 in/sec (PGM 4 IPS is true).
- The carriage moves forward until servo data is detected. T4 being set also provides a needed delay prior to going into the guard band state (GUARD BAND is true).
- After entering the guard band, T6 is started and T2 is reset. (As indicated in Figure 3-51, T6 does not go false before the logic allows entering the ready state.) With T6 and VELOCITY ENABLE true, the logic enters the track seek state provided the difference count is zero.

### 3.4.12.9 Detecting an Incomplete Seek

Seek Incomplete Logic (Figure 3-47) generates SEEK INCOMPLETE. If a seek failure occurs, it must be detected and this signal made true.

Referring to Figure 3-52 (upper half), if T2 times out before starting T6 or T6 times out before allowing ready, the logic enters the seek incomplete state.

#### NOTE

Two consecutive SEEK INCOMPLETES will cause a servo retract.

## 3.4.13 Timing Diagrams

Figures 3-53 through 3-56 present timing diagrams of retract, load heads, recalibrate, track follow, and seek operations of the Servo System. They contain references to locations where signals can be monitored. These timing diagrams represent a "quicklook" summary of the signals generated and decisions made by the system as it executes particular self-controlled operations, and are useful in classroom instruction on the system and debugging servo problems.

Figure 3-57 shows the location of certain test points in the system. Each test point is flagged using a letter. Waveforms photographed at these test points are reproduced in Figure 3-58; each is identified by a letter-to-waveform key and the PCB/pin location of the test point. These waveforms are useful in system performance checking.



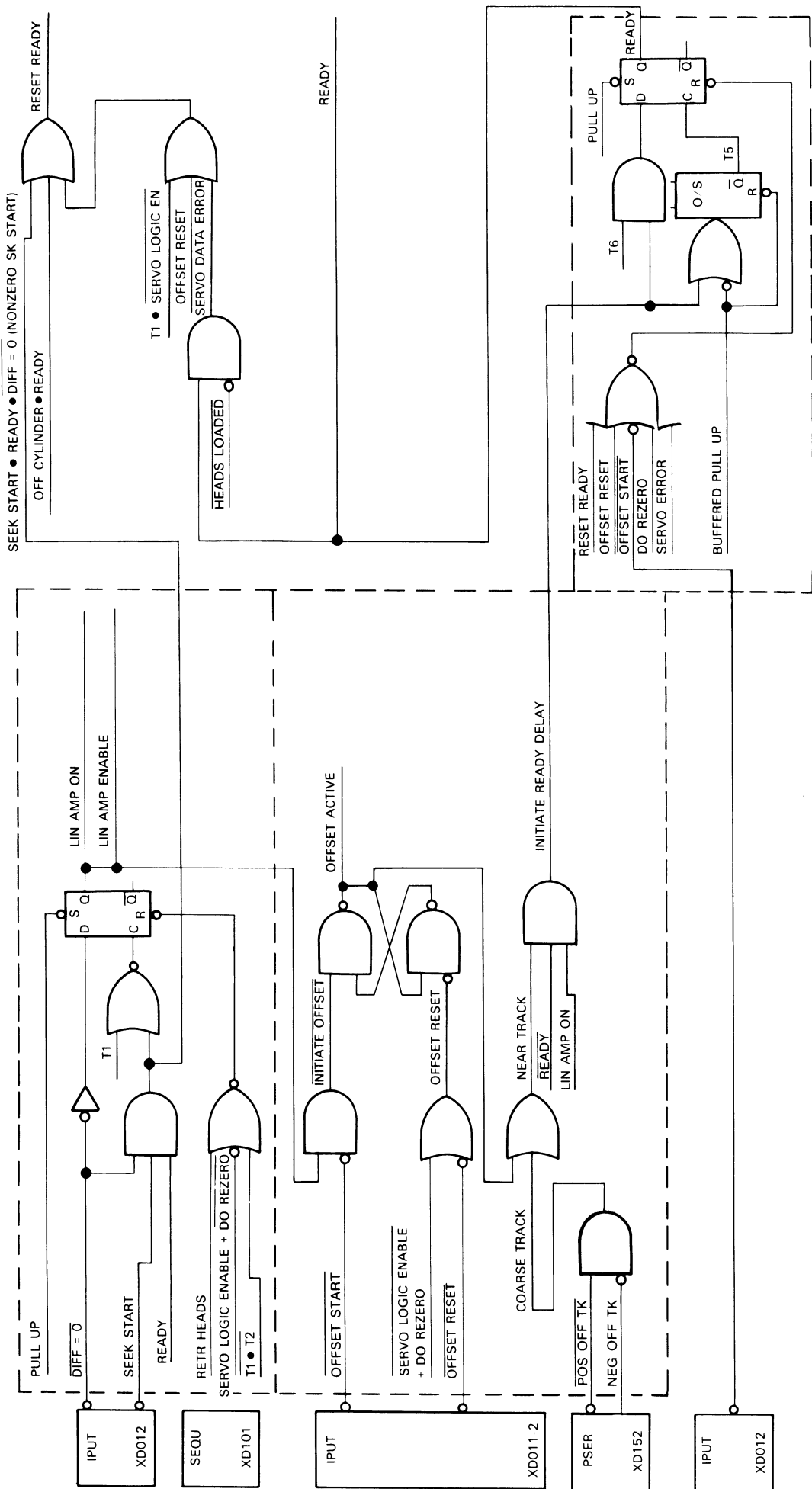


FIGURE 3-51. AMP ENABLE, READY DELAY, ALLOW READY AND READY

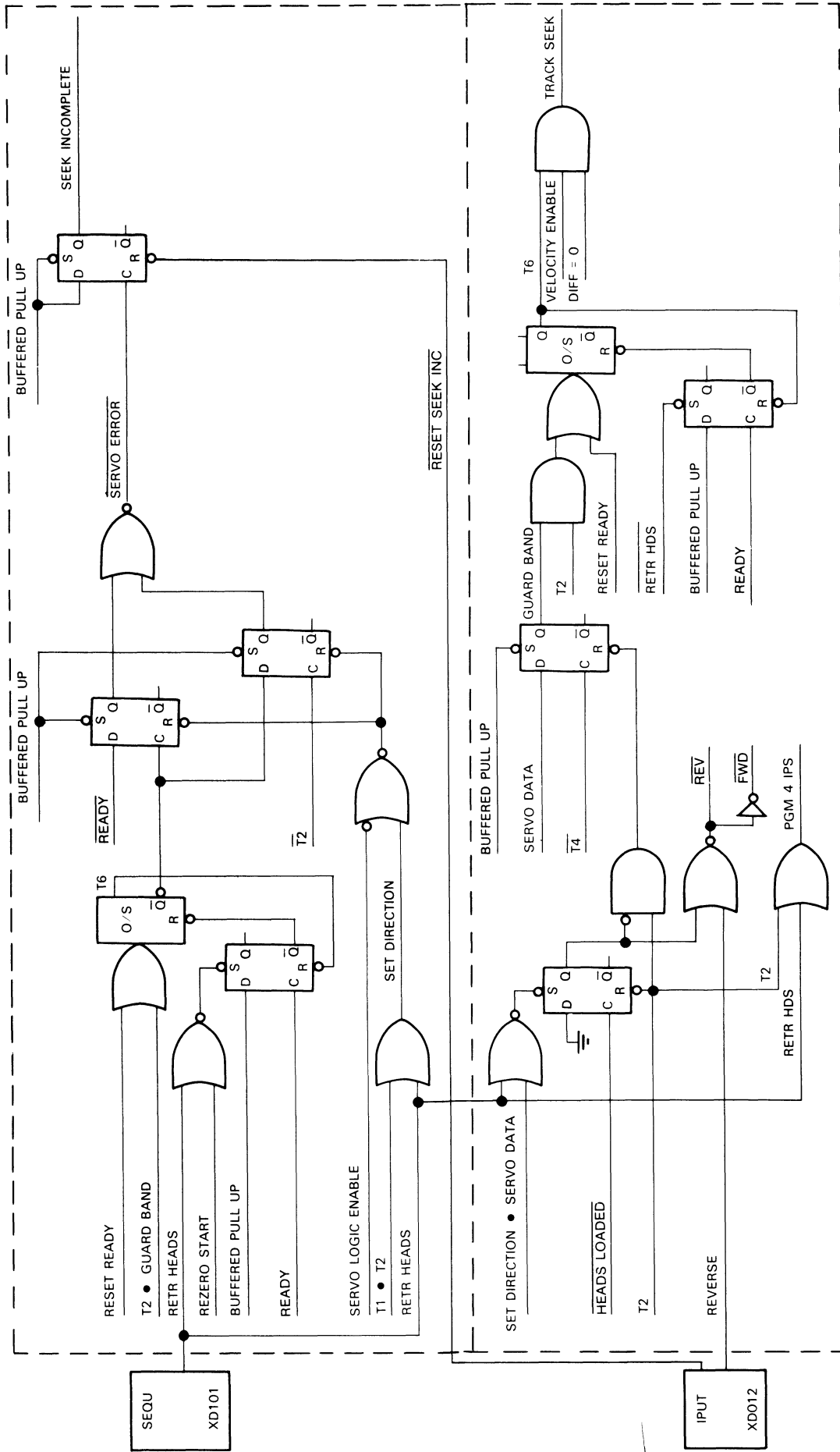


FIGURE 3-52. TRACK SEEK AND SEEK INCOMPLETE

SEE PAGE 3-64  
FOR EXPLANATION

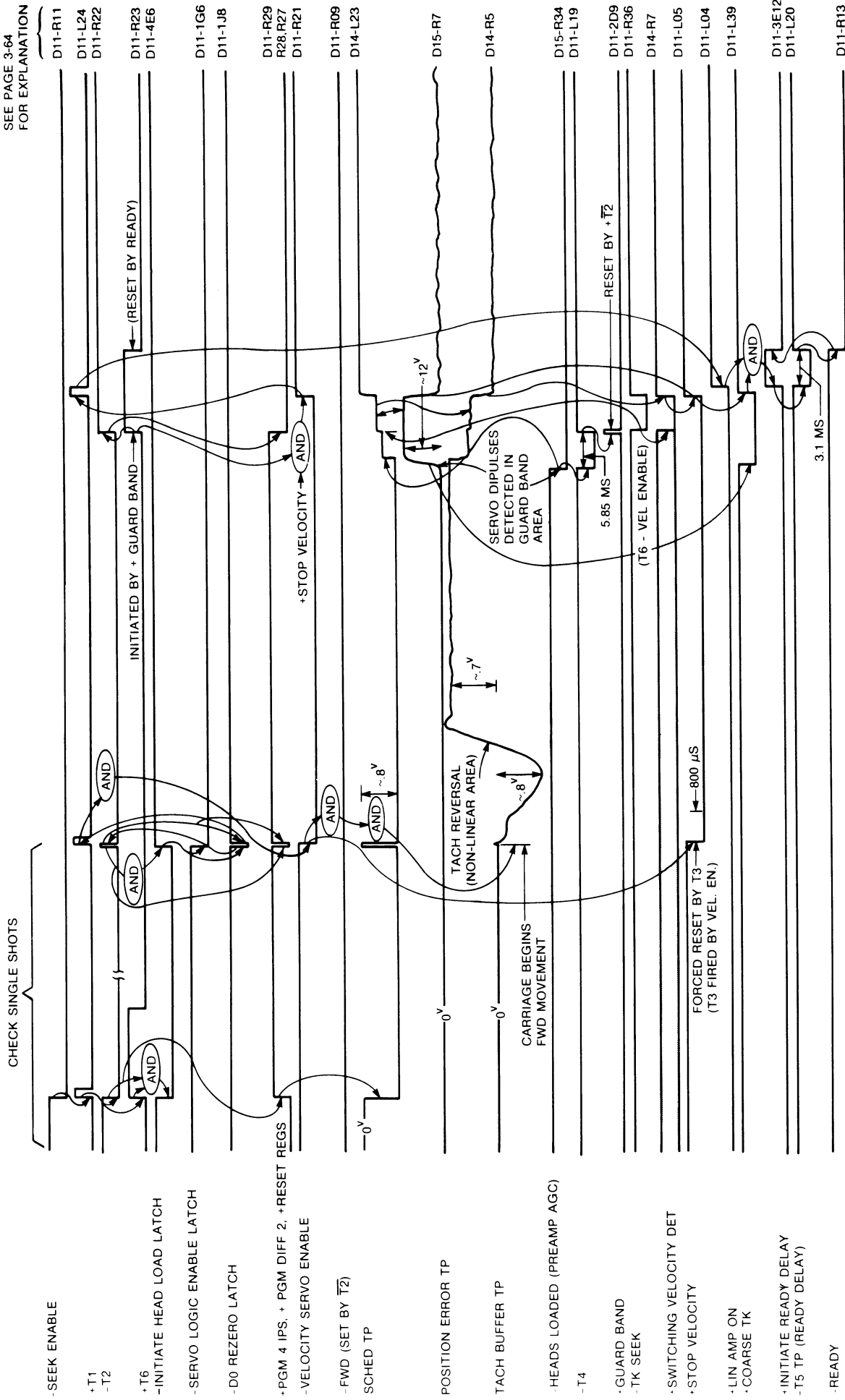


FIGURE 3-53. 677 SERVO TIMING DIAGRAM—HEAD LOAD

SEE PAGE 3-64  
FOR EXPLANATION

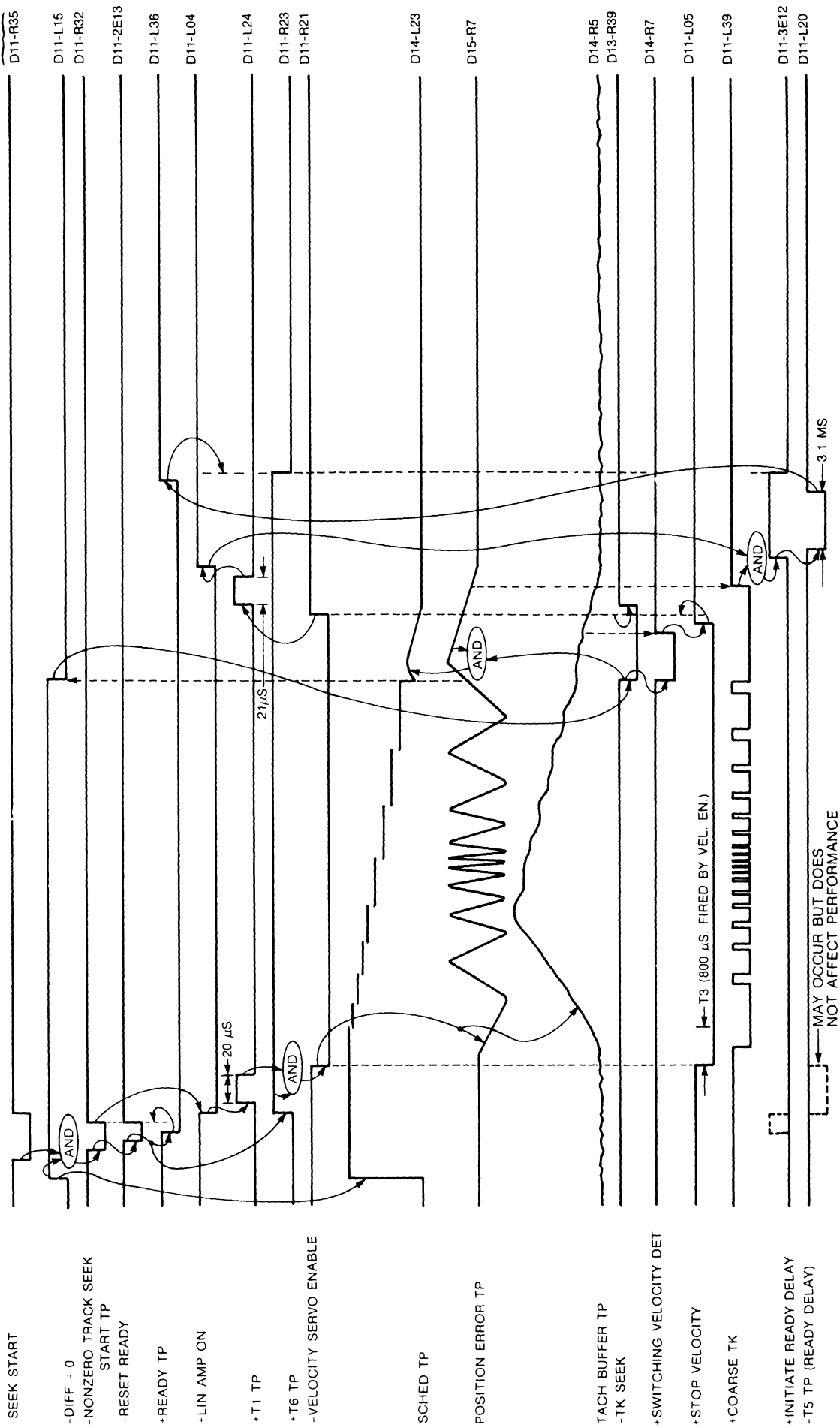
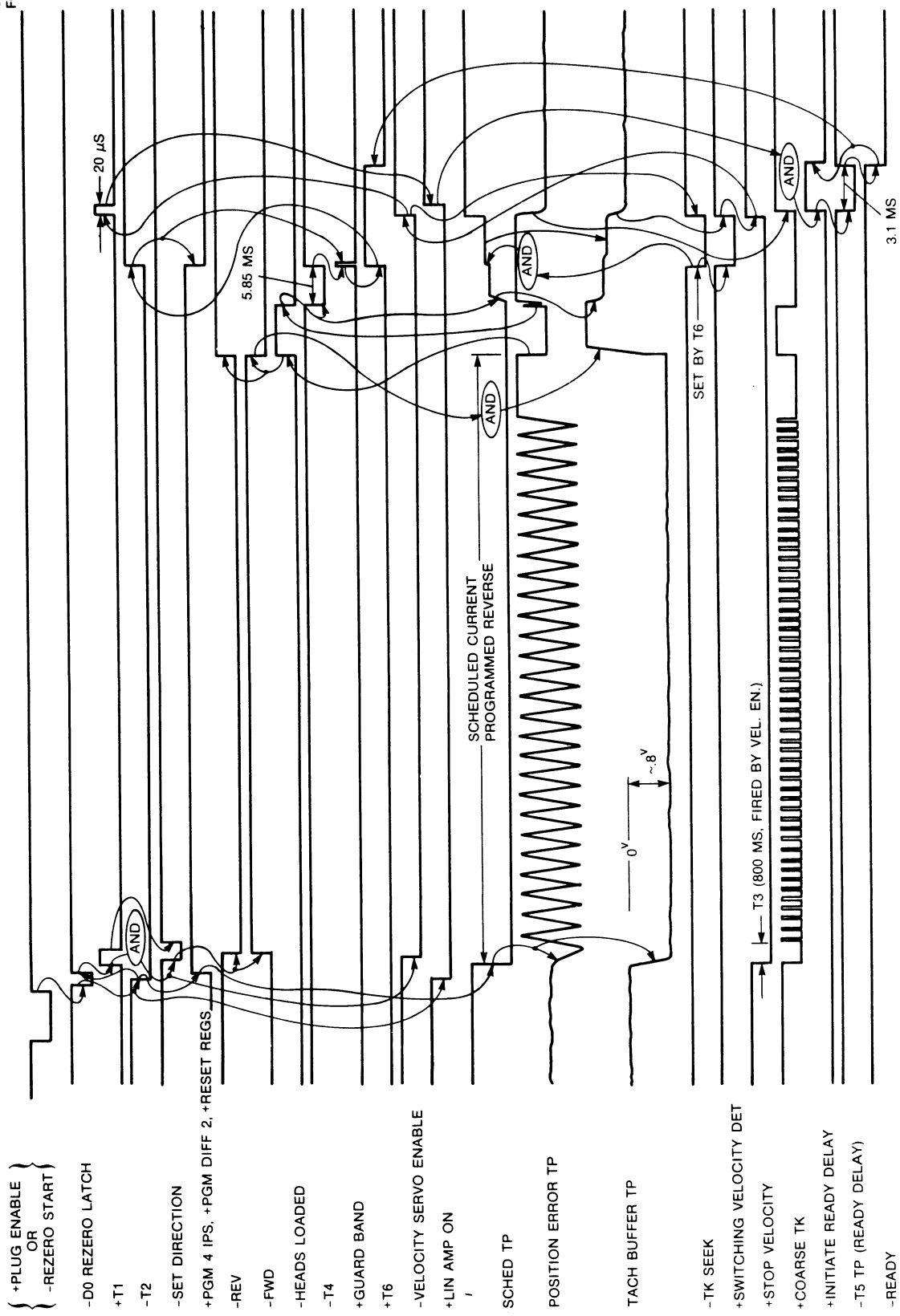


FIGURE 3-54. 677 SERVO TIMING DIAGRAM—18 CYLINDER FORWARD SEEK

SEE PAGE 3-64  
FOR EXPLANATION  
D11-R39,L38



{ +PLUG ENABLE  
OR  
-REZERO START }

- D0 REZERO LATCH
- +T1
- T2
- SET DIRECTION
- +PGM 4 IPS, +PGM DIFF 2, +RESET REGS
- REV
- FWD
- HEADS LOADED
- T4
- +GUARD BAND
- +T6
- VELOCITY SERVO ENABLE
- +LIN AMP ON
- SCHED TP
- POSITION ERROR TP
- TACH BUFFER TP
- TK SEEK
- +SWITCHING VELOCITY DET
- +STOP VELOCITY
- +COARSE TK
- +INITIATE READY DELAY
- T5 TP (READY DELAY)
- READY

- D11-IJ8
- D11-L24
- D11-R22
- D11-ID4
- D11-R29,R28,R27
- D11-R05
- D11-R09
- D11-L37
- D11-L19
- D11-2D9
- D11-R23
- D11-R21
- D11-L04
- D14-L23
- D15-R7
- D14-R5
- D11-R36
- D14-R7
- D11-L05
- D11-L39
- D11-3E12
- D11-L20
- D11-R13

FIGURE 3-55. 677 SERVO TIMING DIAGRAM—REZERO FROM TRACK 53

LETTER/NUMBER COMBINATION BEFORE THE DASH INDICATES PCB ROW/SLOT LOCATION IN LOGIC GATE (SEE PAGE 3-3).

LETTER/NUMBER COMBINATION AFTER THE DASH INDICATES SIGNAL LOCATION ON THE PCB.

- IF THE LETTER IS "L" OR "R," THE COMBINATION INDICATES AN I/O PIN (LEFT OR RIGHT SIDE OF PCB, PIN 1 THROUGH 40).
- FOR OTHER LETTERS, THE COMBINATION INDICATES AN IC PIN. THE FIRST NUMBER-LETTER IS THE X-Y COORDINATE LOCATION OF THE IC ON THE PCB (QUADRANT GIVEN BY NUMBER 1 THROUGH 5 AND LETTER A THROUGH H). THE LAST NUMBER IS THE IC PIN NUMBER (REFER TO LOGIC MANUAL).

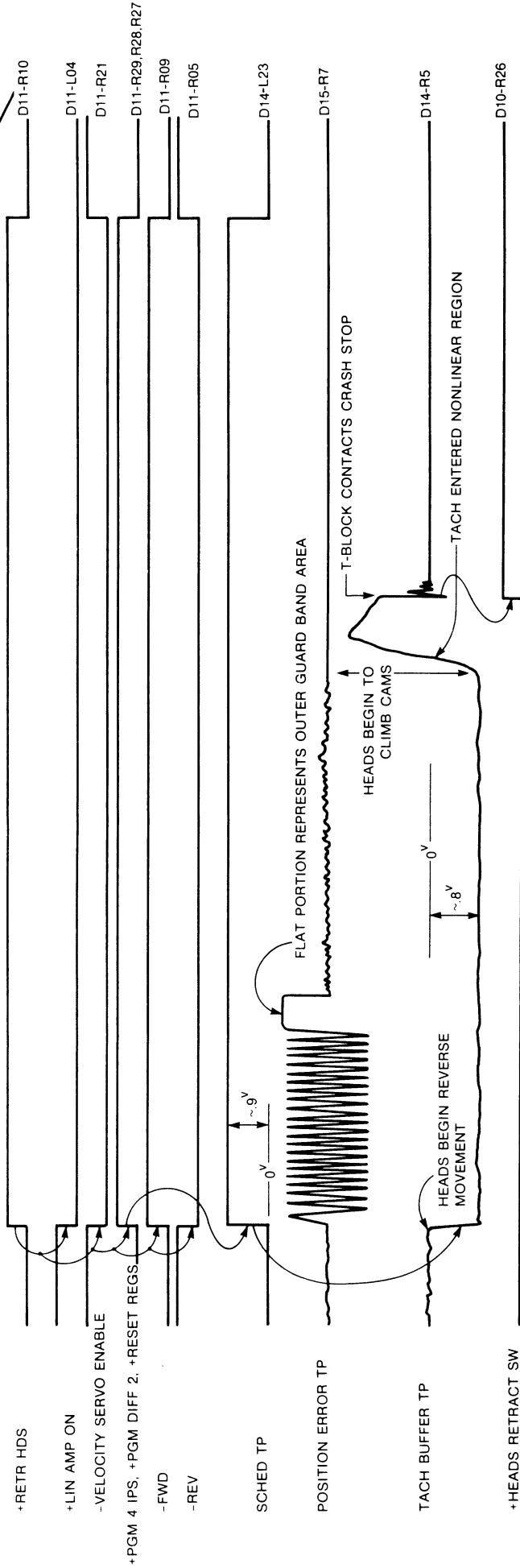


FIGURE 3-56. 677 SERVO TIMING DIAGRAM—RETRACT FROM TRACK 42

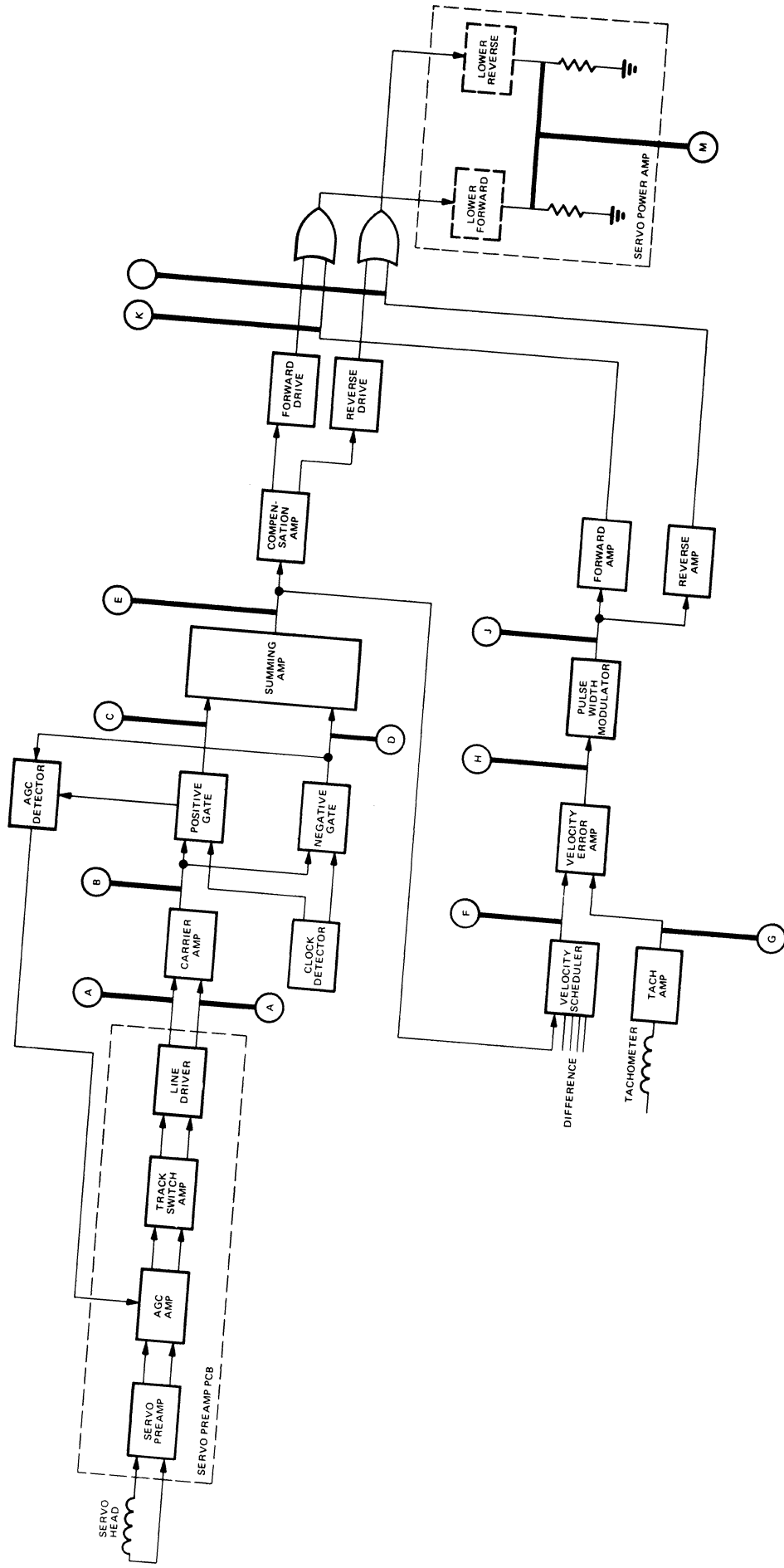
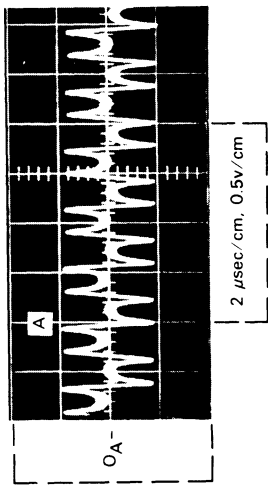


FIGURE 3-57. SERVO SYSTEM TEST POINTS

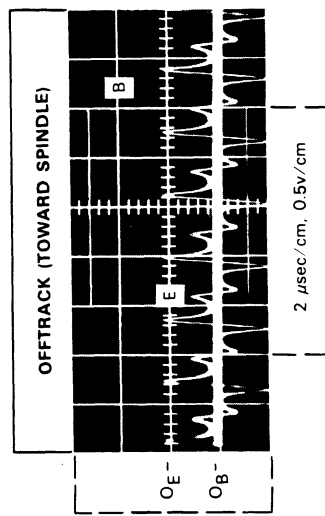
### TRACK FOLLOWING

The waveforms on this page are for Normal and Offset Track Following operations.

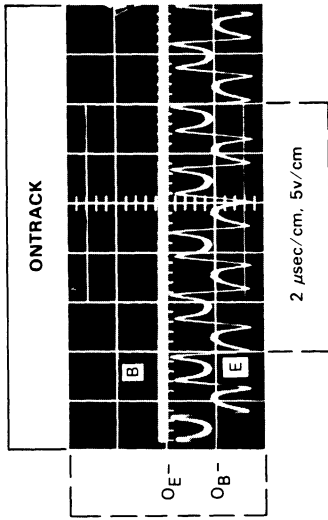
The SERVO HEAD signal at the output of the Pre-Amp (D15 L36/L38) scaped differentially is shown below. Amplitude varies with servo head location. The ontrack condition is shown.



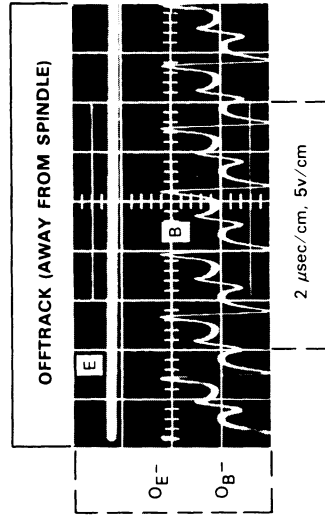
The two signal waveforms shown below apply to a Head Offtrack, Toward Spindle condition. "B" is the Carriage Amp output (D15 R36) that amplifies the SERVO HEAD signal for use by the Peak Detectors and Servo Clock. "E" is the position error (D15 R7).



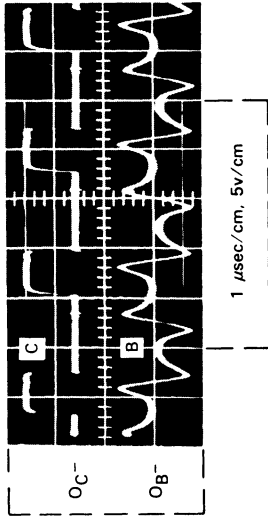
"B" and "E" are shown below for the Head Ontrack condition.



"B" and "E" are shown below for the Head Offtrack (away from spindle) condition.



"C" shown below is GATE POSITIVE (D15 R33). It gates the second-positive peaks into the Positive Peak Detector. As previously identified, "B" is the Carrier Amp output.



"D" shown below is GATE NEGATIVE (D15 R35). It gates second-negative peaks into the Negative Peak Detector. As previously identified, "B" is the Carrier Amp output.

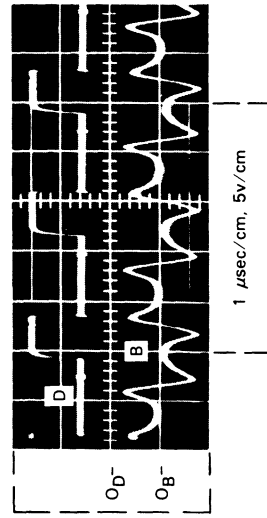


FIGURE 3-58. SERVO SYSTEM WAVEFORMS (Part 1 of 6) — TRACK FOLLOWING

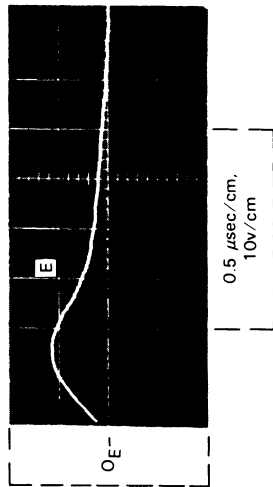


### SERVO SEEK WAVEFORMS

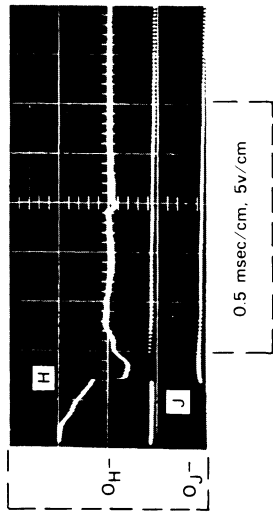
The Seek waveforms shown on this page and the following pages were photographed while performing forward seeks, and while syncing the scope on -FWD (D14 R24).

#### ONE-TRACK SEEK FORWARD

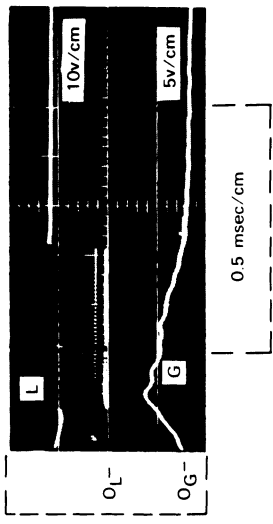
The position signal at the output of the summing Amplifier (D15 R7) is shown below. A 0 volt signal indicates the center of a cylinder location.



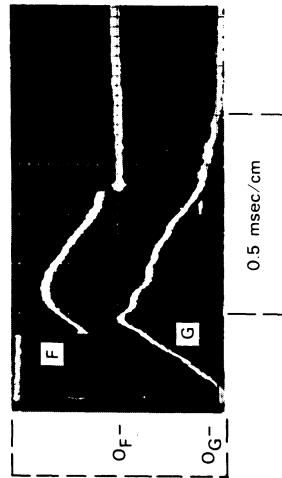
"H" shown below is the velocity error (D14 R11). It is the output of the Velocity Error Amp which reflects the difference between actual velocity (tach) and desired velocity (curve). "J" is UNGATED ACCELERATE FWD (D14 R14). It is generated by comparing Velocity Error to 25 KHz sawtooth.



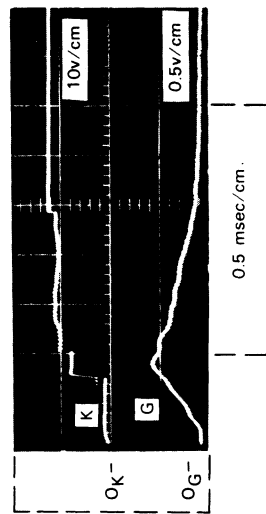
"L" shown below is MINUS REV DRIVE (D14 R21). It gates reverse current to the VCM during a Seek operation. Decelerate current is pulsed to the VCM. As previously identified, "G" shown below is the Tach Buffer output.



"F" shown below is the Velocity Schedule curve (D14 L23). It is the output of the Velocity Scheduler. "G" shown below is the Tach Buffer output (D14 R5). It is the output of the Tach Amplifier, and is shown inverted to aid comparison with the Velocity Schedule curve.



"K" shown below is -FWD DRIVE (D14 R13). It gates forward current to the VCM during a Seek operation. "G" shown below is Tach Buffer output (D14 R5). It is the signal at the output of the Tach Amplifier, and is shown inverted. "G" is proportional to Carriage Velocity.



"M" shown below is a voltage signal that is proportional to the VCM current during a Seek operation. Current is pulsed during decelerate time. "M" results when the following signals are scoped differentially.

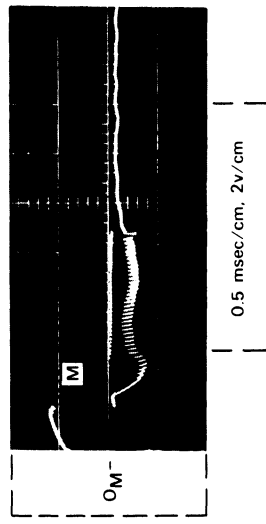
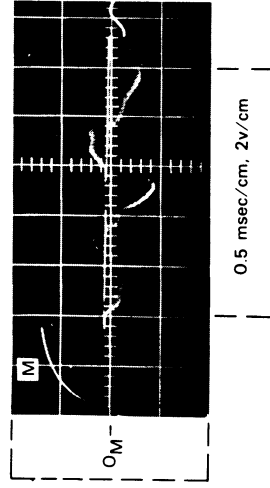
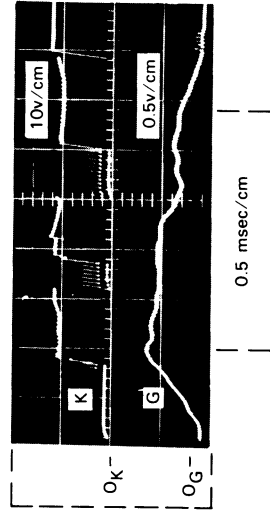
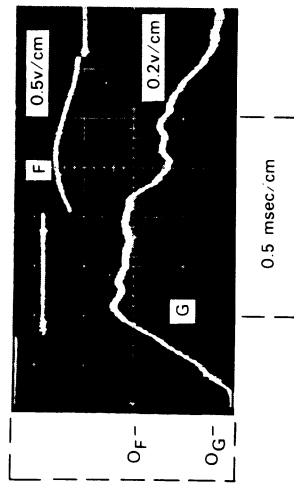
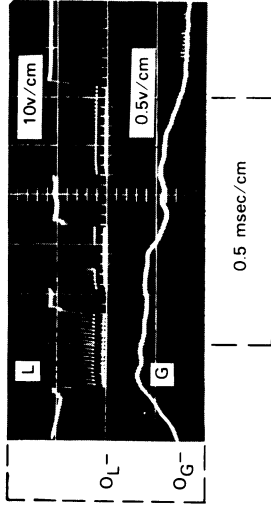
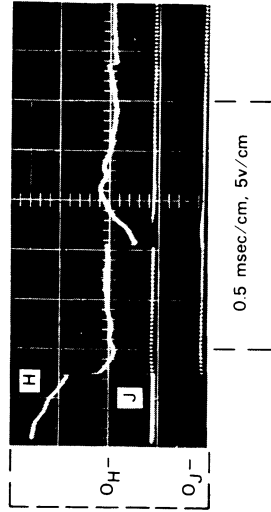
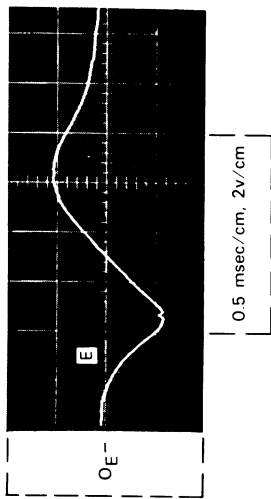


FIGURE 3-58. SERVO SYSTEM WAVEFORMS (Part 2 of 6) — ONE TRACK SEEK FORWARD

**TWO-TRACK SEEK FORWARD**

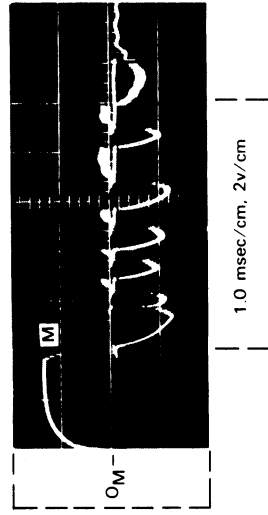
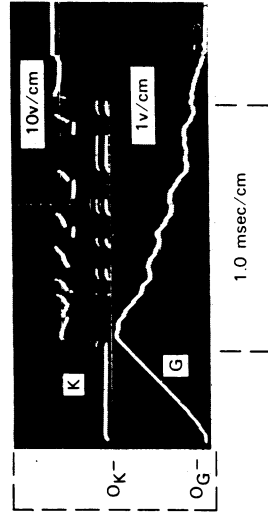
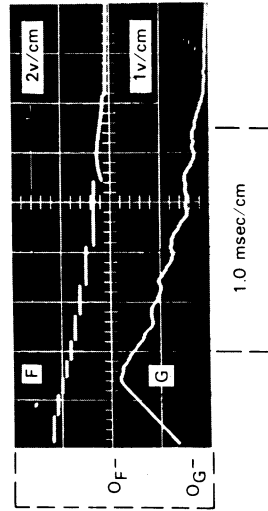
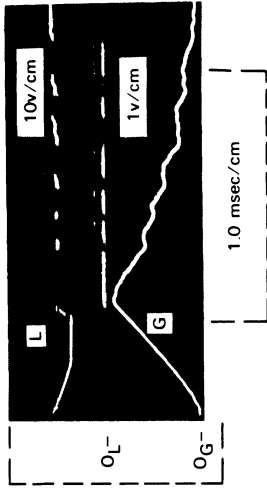
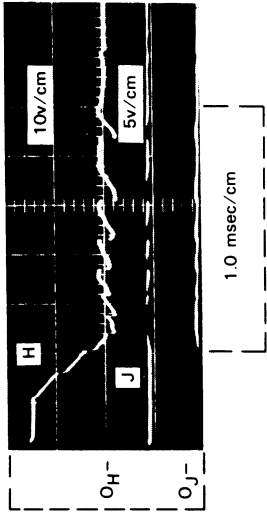
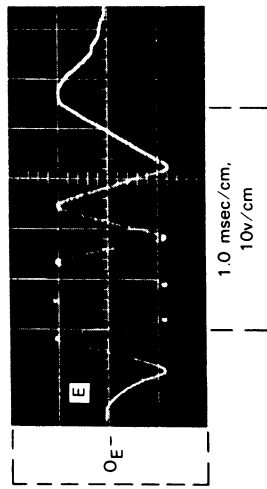
The following six photos show signal waveforms taken during a Two-Track Seek. Their sequence of presentation, and the particular signals shown on each photo, are the same as those previously presented for a One-Track Seek.



**FIGURE 3-58. SERVO SYSTEM WAVEFORMS (Part 3 of 6) — TWO TRACK SEEK FORWARD**

**TEN-TRACK SEEK FORWARD**

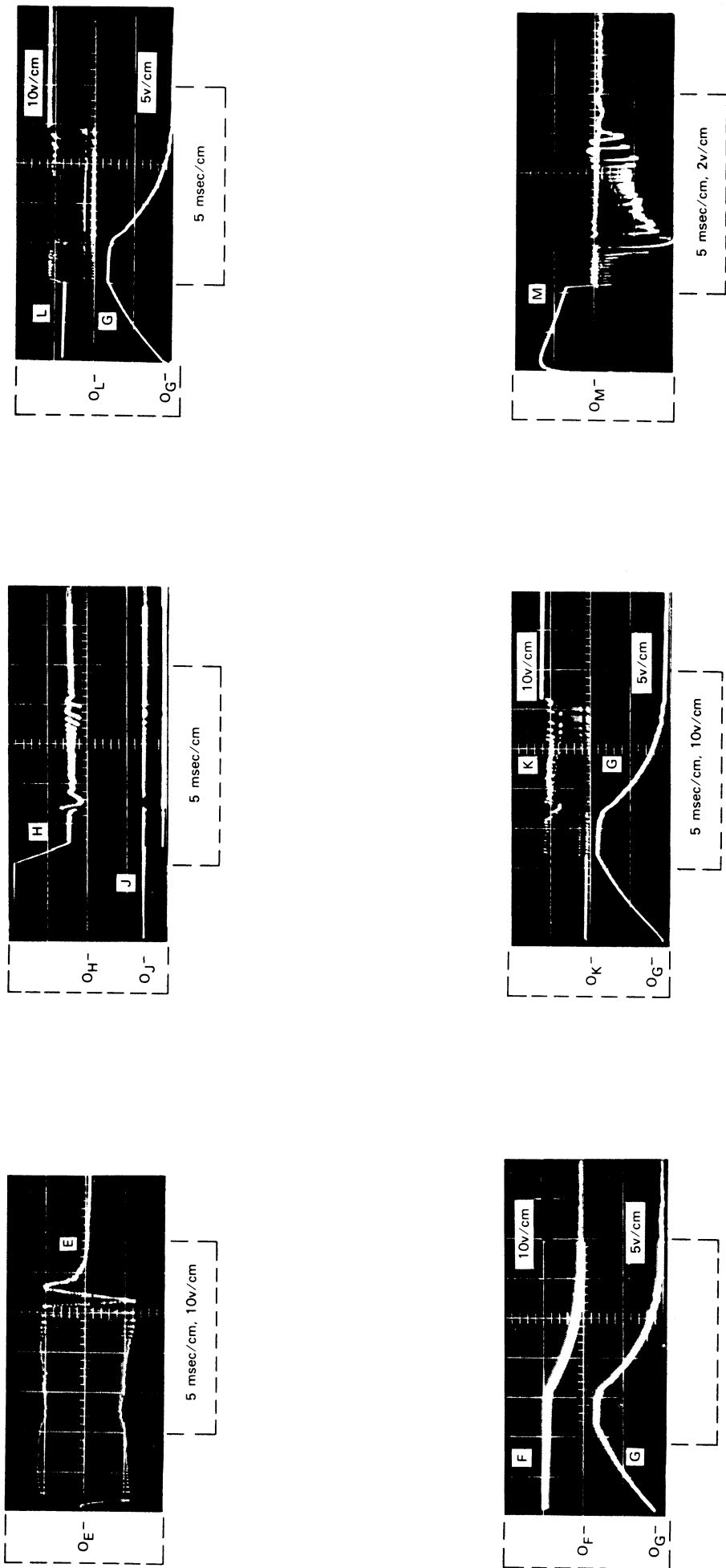
The following six photos show signal waveforms taken during a Ten-Track Seek. Their sequence of presentation, and the particular signals shown on each photo, are the same as those previously presented for both a One- and Two- Track Seek.



**FIGURE 3-58. SERVO SYSTEM WAVEFORMS (Part 4 of 6) — TEN TRACK SEEK FORWARD**

**TWO HUNDRED-TRACK SEEK FORWARD**

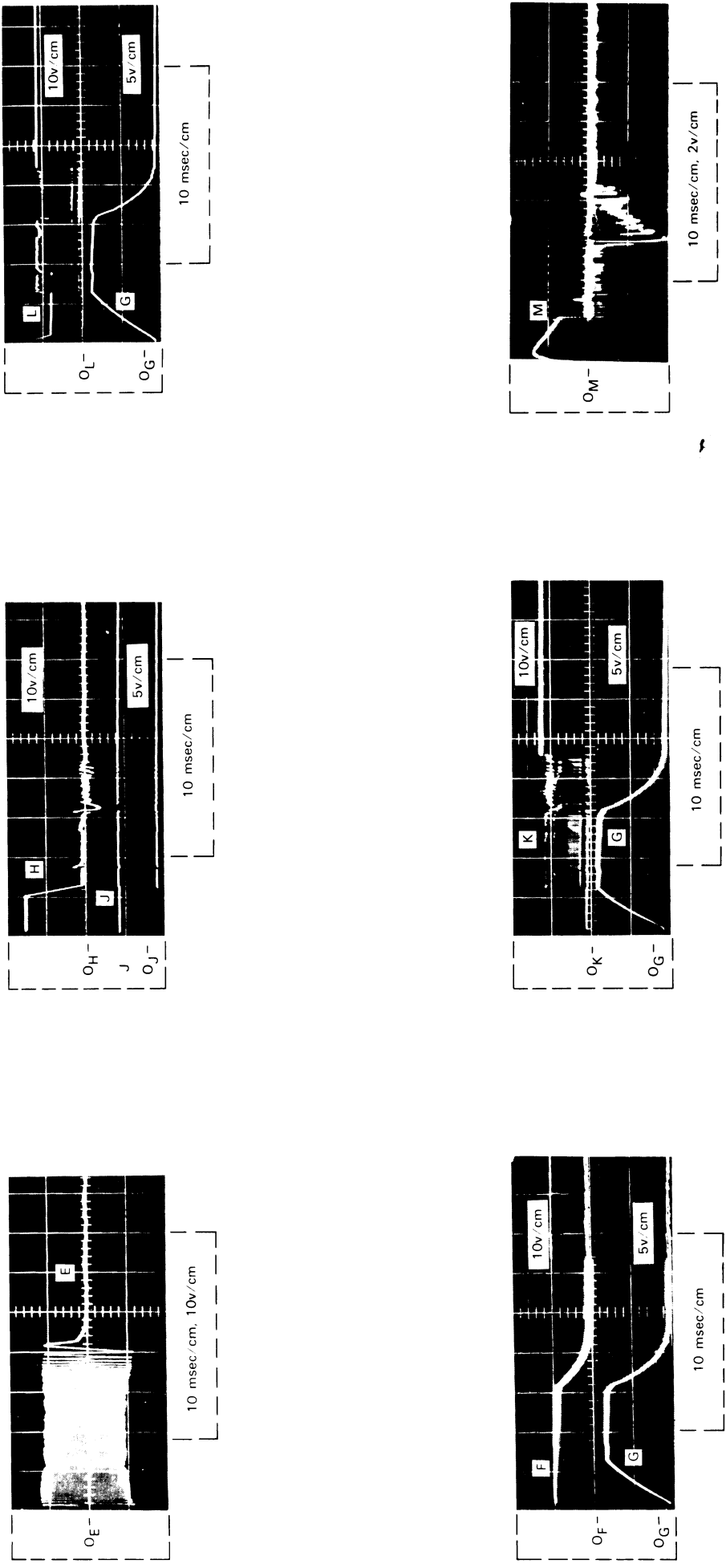
The following six photos show signal waveforms taken during a 200-Track Seek. Their sequence of presentation, and the particular signals shown on each photo, are the same as those previously presented for either a One-, Two- or Ten-Track Seek.



**FIGURE 3-58. SERVO SYSTEM WAVEFORMS (Part 5 of 6) — TWO HUNDRED TRACK SEEK FORWARD**

**FOUR HUNDRED-TRACK SEEK FORWARD**

The following six photos show signal waveforms taken during a 400-Track Seek. Their sequence of presentation, and the particular signals shown on each photo, are the same as those previously presented for either a One-, Two-, or 200-Track Seek.



**FIGURE 3-58. SERVO SYSTEM WAVEFORMS (Part 6 of 6) — FOUR HUNDRED TRACK SEEK FORWARD**

## 3.5 READ/WRITE SYSTEM

### 3.5.1 System Description

The Read/Write System is used to select the head to be used in transferring data, to poll the drive circuits for the presence of no unsafe condition as a prerequisite to data transfer, and for actual reading and writing. To provide these functions, the system contains read/write circuits and 19 read/write heads. These elements of the system, and the functions they provide, are described below in introductory format.

#### 3.5.1.1 Head Numbering and Containment

The nineteen read/write heads are addressable as Heads 00 to 18. The servo head is not addressable. All twenty heads are mounted to the left and right sides of the T-block in banks of ten each. As shown in Figure 3-59, odd-numbered heads are mounted to the left side and even-numbered heads are mounted to the right side. Each head/arm assembly fits into precision slots in the T-block and is held in place by an alignment clip and mounting screws.

#### 3.5.1.2 Head/Arm Assembly Components

For each head/arm assembly, a read/write coil is imbedded into a slider which is mounted to the head arm by means of a flexure (Figure 3-59). The construction of the slider, and the forces produced by the arm and flexure, give the magnetic head the capability of flying at 45 or 50 microinches (depending on head and drive type) above the disc surface—and never contacting the disc surface. The air between the slider surface and the disc surface is referred to as the air bearing.

#### 3.5.1.3 Head Communication with Read/Write Circuits

The coil in the slider communicates with the read/write circuits through pigtail wires (Figure 3-59). To sustain rigorous, motions during repetitive seek operations, the pigtail is routed through a spring, then plugs into the Matrix PCB. Three wires connect the channel with coil. Two wires attach to the coil ends, and the third wire attaches to the center tap of the coil.

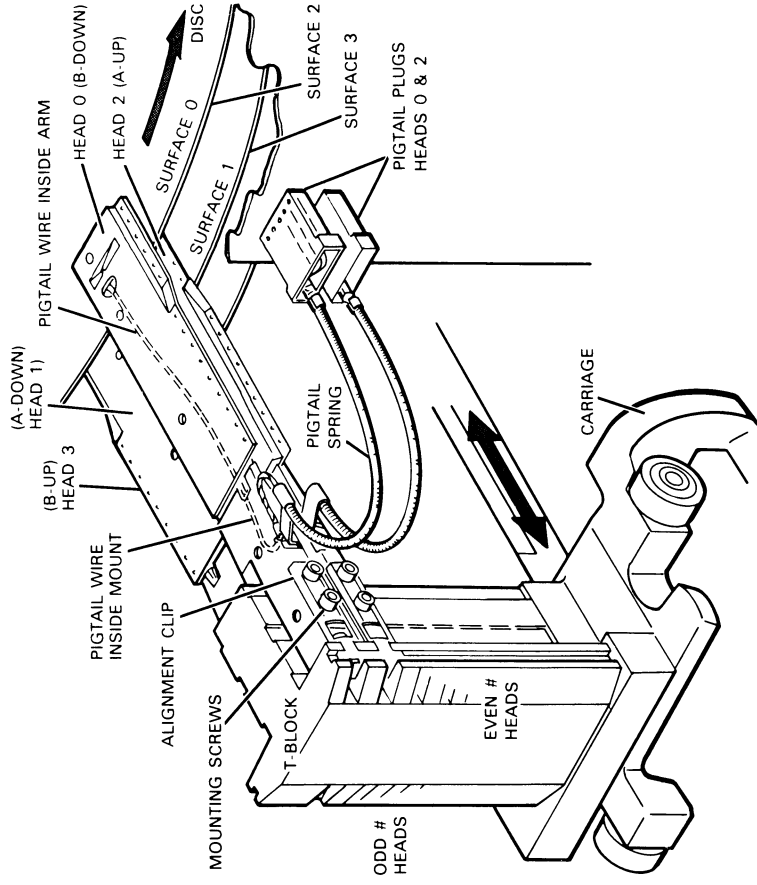


FIGURE 3-59. HEAD DETAILS

#### 3.5.1.4 Selection of Read or Write Operation

A head is selected to read or write by controlling current passage in the coil through the center tap. The channel grounds the center tap of a head in order to perform a read or write operation.

Contrasting with the read/write heads, the center tap of the servo head is always selected, thereby allowing continuous reading of the servo data prerecorded in the pack.

### 3.5.1.5 Identification of Servo Head

The servo head/arm assembly is readily identifiable by its longer cable and double plug.

### 3.5.1.6 Identification of 100 MB vs 200 MB Heads

A serial number is engraved on every head/arm assembly. For 200 MB heads only, serial numbers have the prefix "M".

### 3.5.1.7 Head Adjustments

The head load force, circumferential alignment, head pitch and roll attitudes, and load/unload points are fixed parameters. They are factory set and require no adjustments. The radial position of each read/write head relative to the servo head is adjustable, by reading special tracks prewritten on the FE Alignment Disc Pack (special tool).

### 3.5.1.8 Data Transfer Synchronization

To synchronize data transfer operations, servo data is sent from the drive to the DCL. Each servo track is divided into 13,440 equal intervals. A servo data pulse is transmitted for each interval. Since the number of intervals is constant, the transmitted pulses are directly proportional to pack rotational speed, and for this reason the write and read circuits between the two end points of the data transfer can be phase locked to insure proper spacing in the data.

### 3.5.1.9 Write Operation

Referring to Figure 3-60, write data level (NRZ) and write data strobes in conjunction with write command from the DCL are received by Receivers. PRCO PCB (precompensation) encodes write data in modified frequency modulation (MFM) form, and precompensates it to allow for the bit shift that is inherent when writing high density data. MFM write data is then applied to the Write Trigger which provides the switching signals to either left or right Write Current driver. The driver accepts the current from its current source and switches it from one head coil to the other, alternately, as instructed by the Write Trigger and write data.

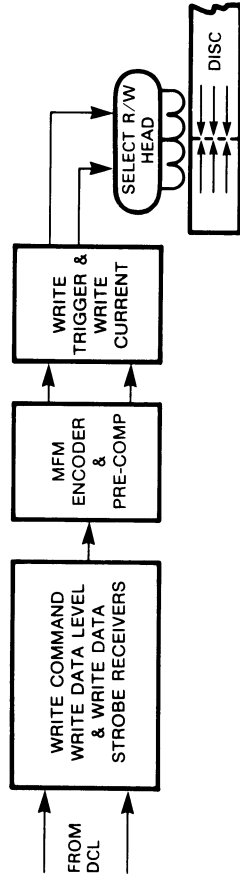


FIGURE 3-60. SIMPLIFIED WRITE OPERATION

### 3.5.1.10 Read Operation

Referring to Figure 3-61, when a head is selected for read command operation its read signal is passed to the Read Preamp where the signal is amplified by a factor of 100. At this point the signal is applied to LINA PCB (D18). The read signal passes through a voltage controlled Attenuator where the gain is adjusted to maintain a constant signal amplitude at the output. The Main Amp and Filter raise the signal to a 4 V peak-to-peak differential level (for 2F only), and drive a detector section (Detector and Gate Generator) and an AGC Feedback Control circuit. The latter supplies the voltage necessary to drive the Attenuator. The Differentiator and Limiter provide timing information for the detector section. Detector and Gate Generator provide gating information; their outputs are combined to drive the Data Latch Single Shot. Its raw data output drives VFO PCB (D05). To accommodate variations in disc speed, VFO is synchronized to the raw data in MFM form read from the disc. The raw data is also sent through a data separator, which removes the clock pulses interspersed with the data pulses. The result is standardized read data. In addition, the VFO generates VFO Clock signal used to develop a read strobe. Both read data level and read strobe are sent to the DCL, when read command is true.

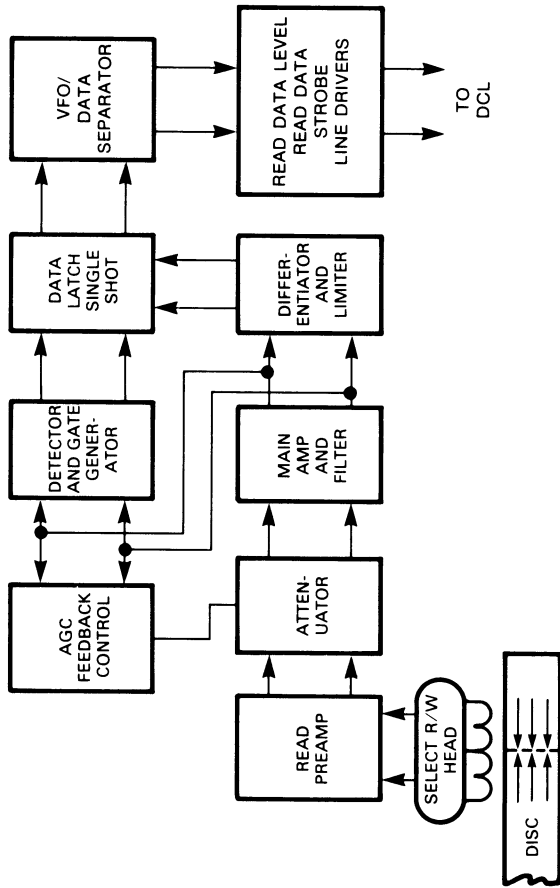


FIGURE 3-61. SIMPLIFIED READ OPERATION

### 3.5.2 Read/Write Circuits

To select the head to be used in reading or writing data, and to transfer data while insuring that no condition which may degrade data integrity is present in the drive, the Read/Write System uses circuits packaged in six PCBs. They are: DSHS (Data Safety and Head Select), WLOG (Write Logic), DTEC (Detector), LINA (Linear Amplifier), and two MTRX (Left Read/Write Matrix and Right Read/Write Matrix). The two MTRX PCBs are functionally the same. Left MTRX is dedicated to odd numbered heads (mounted on left side of T-block) and Right MTRX is dedicated to even numbered heads (mounted on right side).

Figure 3-62 is a block diagram of the system. DSHS and WLOG provide the general functions indicated in their names. DTEC accepts the linear signal from LINA and determines if a bit was written. LINA uses an AGC closed loop circuit to maintain outputs at a constant level and original resolution in

the input head signal regardless of AGC action. Left or Right MTRX grounds one of the even or odd numbered heads in response to DSHS select lines, to allow selection of a read or write operation. If a read is selected, a preamp is used. Only two outputs generated by these PCBs leave the system, these being raw data sent to VFO (for decoding and transmission to the DCL via OPUT) and unsafe conditions sent to OPUT (for transmission to the DCL and the operator control panel, the latter as a single summary indicator). The raw data is read from the pack by the read/write heads, and the unsafe conditions result from monitoring every system in the drive which contains electronic circuitry.

In the following paragraphs, PCBs containing read/write circuits are described individually, then read and write operations are described at the system level using flowcharts.

### 3.5.3 Data Safety and Head Select PCB

DSHS insures that the drive's read/write circuits are operating properly before allowing a read or write operation. If an unsafe condition is detected, DSHS inhibits reading and writing.

To write data, the following conditions are satisfied (refer to Figure 3-63):

- READY, WRITE (or OP PAD), and LIN AMP ON are true.
- OFFSET ACTIVE, READ ONLY, INDEX ERROR, and R/W INOP are false.

With all conditions above satisfied, a write operation is initiated. Within 500 nsec, the sensing of write current flowing (ANY  $I_w$  is true) and data being written (AC WRITE is true) occurs. If either of these lines is enabled before the write operation is initiated, or not enabled after the operation is initiated, a read/write inoperable condition occurs to stop the write process.

If an address mark area (blank area of approximately 3.7  $\mu$ sec) is to be written on the disc, WRITE AM is made true to fire a 6.5  $\mu$ sec single shot (AM O/S in Figure 3-63) which simulates AC WRITE remaining enabled to prevent activation of the AC Write latch.

At the end of the write operation, WRITE becomes false. Within 500 nsec, AC WRITE and ANY  $I_w$  also become false. A Write AC Clamp single shot is activated for 3.5  $\mu$ sec to stop write current being transmitted to WLOG by shorting the current to ground.



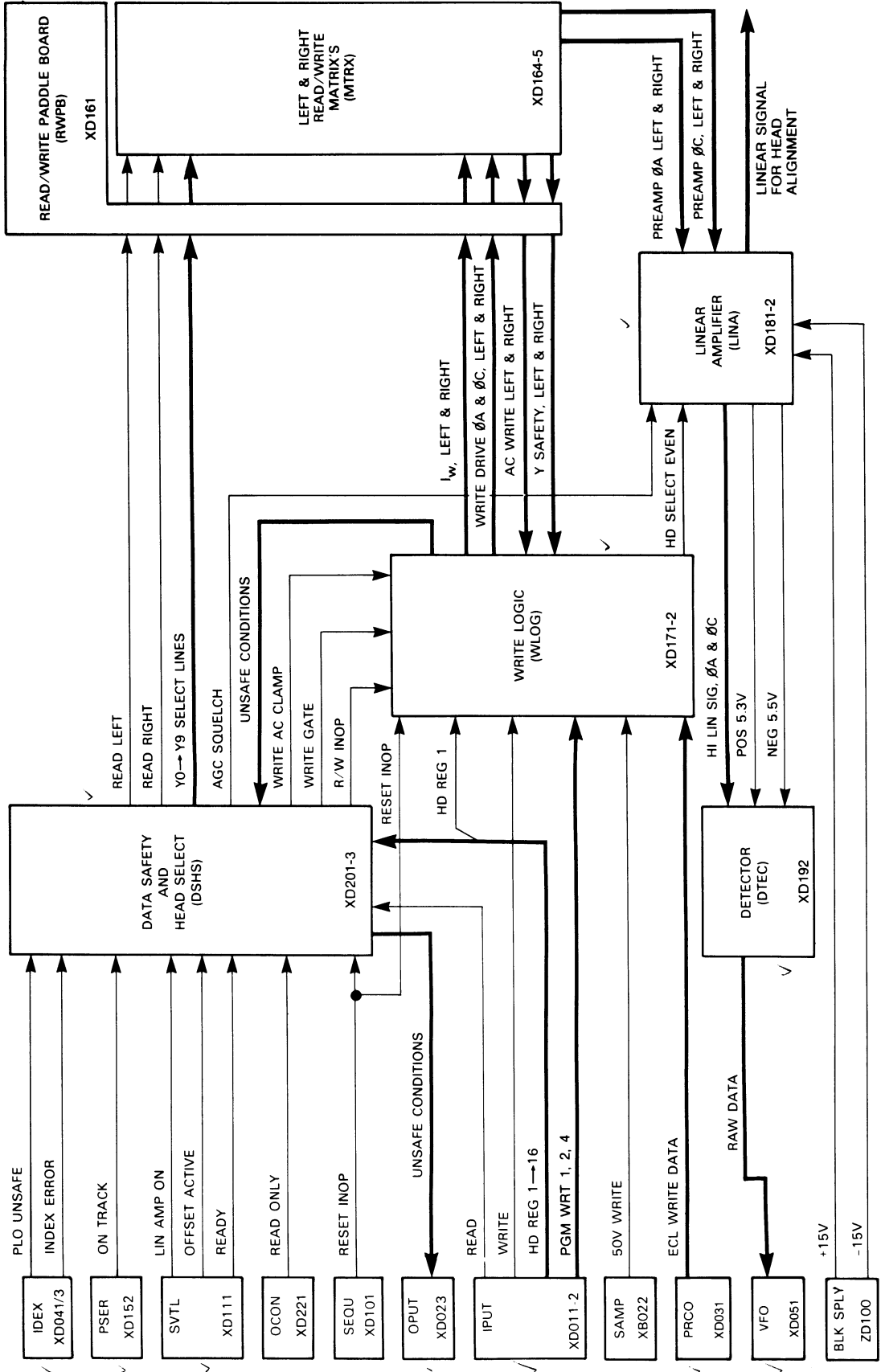


FIGURE 3-62. READ/WRITE SYSTEM

If READ ONLY is true, a write operation is disabled providing this signal is made true before the operation starts. If made true during the operation, it has no effect. During a pad to index operation, WRITE GATE is made true by OP PAD being true. Then the drive pads "all zeros" to index.

**To read data,** READY, READ, and LIN AMP ON are true and WRITE is false, and none of the read/write inop latches is set by any one of the other input signals. A read process is then activated. AM SEARCH is used to reduce the sensitivity of DETC PCB so that noise pick up during the blank address mark area is not detected as data.

### 3.5.3.1 Read/Write Inoperate Circuits (Figure 3-63, Part 1 of 2)

These circuits protect data from being destroyed in event of a component failure. There are 15 inoperate conditions which can occur. Once an inoperate condition occurs, it is latched in and can only be removed by the failure disappearing and grounding RESET INOP. During troubleshooting, an inoperate condition can be disabled by grounding the output +R/W INOP (DEFEAT) on pin D20-L30. This will inhibit the inoperate condition from being sensed. UNSAFE indicator on the control panel will be illuminated when R/W INOP occurs.

- WRITE READY UNSAFE true indicates writing after a loss of on track.
- NO HEAD SELECTION true indicates read or write gate active when LIN AMP ON is false.
- MULTI HEAD SELECT true indicates more than one head selected with read or write gate active.
- WRITE AND OFFSET true indicates OFFSET ACTIVE is true during write operations. If WRITE PROTECT switch has been depressed to WRITE PROTECT position, and the DCL begins to send WRITE COMMAND to the drive, it will cause WRITE AND OFFSET/NOT READY unsafe (R/W INOP) in the drive.
- WRITE SELECT UNSAFE true indicates both left and right write-current sources are active simultaneously.
- CURRENT SWITCH UNSAFE true indicates writing with the wrong write current for the selected track.

- 35V REG FAIL is true if indicates the regulator voltage is either too low or high for writing.
- WRITE CURRENT UNSAFE true indicates write current (any current, from left or right current sources) is available without write gate active.
- PLO UNSAFE true indicates a loss of synchronization of PLO with read or write gate active.
- PAD UNSAFE true indicator PAD circuits (optional) are improperly selected.
- READ AND WRITE true indicates the drive is ready but both read (internal) and write gates are active.
- AC WRITE UNSAFE indicates writing with no write data, meaning no data was written within 383 nsec. If the DCL tries to write and read simultaneously, it will cause AC WRITE UNSAFE which generates TRANSITIONS UNSAFE sent to the DCL. (Refer to paragraph 3.5.7.2.)
- AM SS FAIL true indicates failure of the AM Single Shot, representing an active state of the single shot before write gate is active.
- TRANSITIONS DETECTOR FAIL indicates write transitions without the presence of a write command.
- TRANSITIONS UNSAFE indicates the absence of write transitions during a write command.
- AC SS FAIL true indicates failure of the AC Single Shot, representing an active state of the single shot before write gate is active.
- SINK FAIL true indicates transistor used to short write current to ground is not turned on in less than 700 nsec.

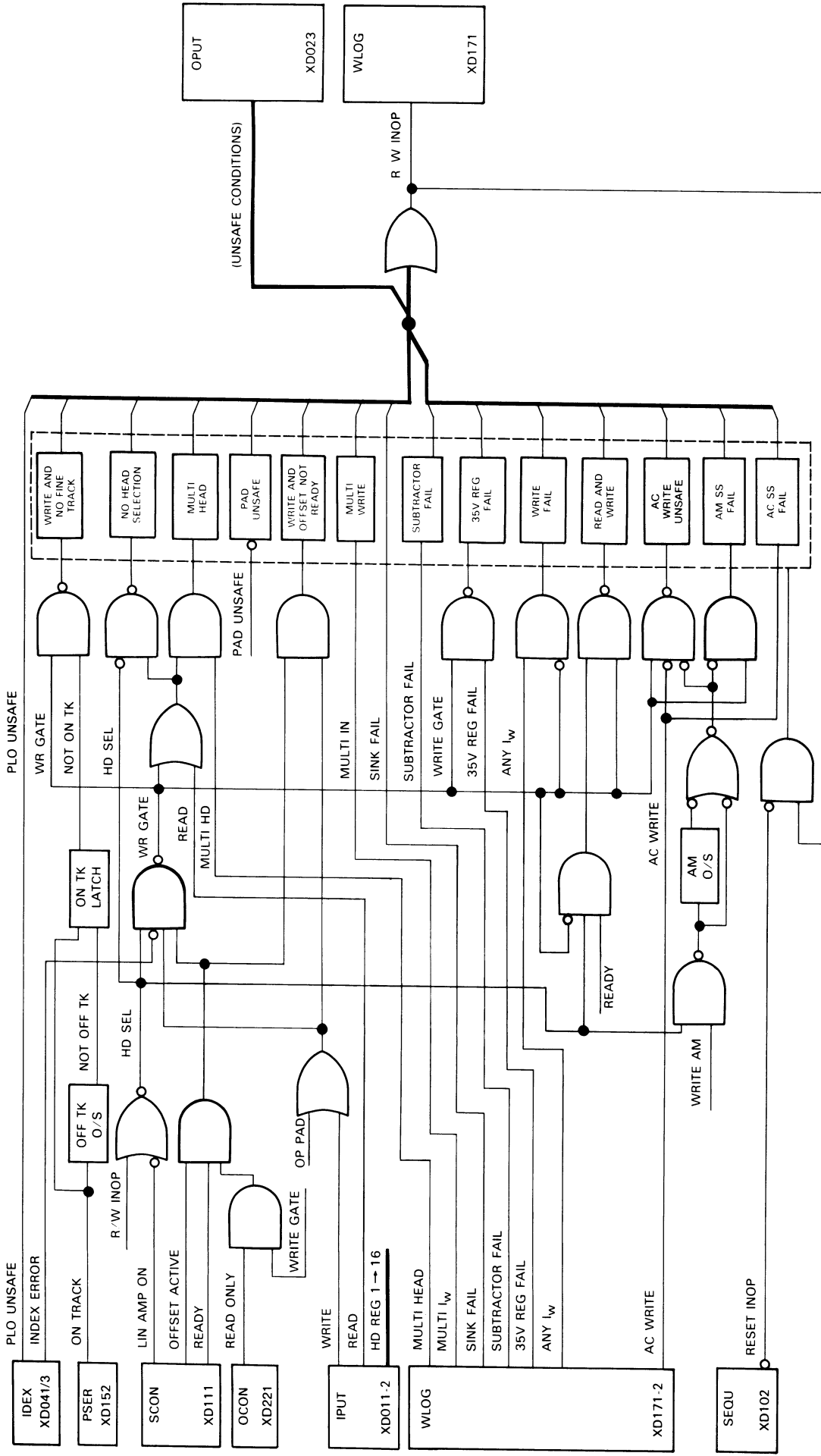


FIGURE 3-63. DATA SAFETY AND HEAD SELECT PCB (Part 1 of 2)

### 3.5.3.2 Activating Head Select Line (Figure 3-63, Part 2 of 2)

There are five Head Select lines (Head Select 16, 8, 4, 2, 1) from the DCL. HD REG 1 (Head Select 1) generates Read Right and Read Left to select the right or left (even or odd) Read/Write Matrix and preamplifier. HD REG 2, 4, 8, 16 (Head Select 2, 4, 8, 16) are decoded by an IC 4-line to 16-line decoder to control 10 head center tap select lines Y0-Y9. The decoder is inhibited by either R/W INOP (DEFEAT) true or HD SELECT false.

### 3.5.3.3 Activating Read Matrix

DSHS determines which one of two read select circuits (in Left MTRX and Right MTRX) is to be activated. Its decision is controlled by the Head Select 1 (HD REG 1). Referring to part 2 of Figure 3-63, this bit being false causes selection of the right matrix (READ RIGHT is true), provided write gate is not active, drive is ready, no unsafe condition exists, and the LIN AMP ON is true. The bit being true causes selection of the left matrix (READ LEFT is true), provided the same conditions are satisfied.

### 3.5.3.4 Suppressing AGC Control

DSHS suppresses automatic gain control of the linear amp to allow recovering a read capability for 7  $\mu$ sec after the read channel is enabled. As indicated in part 2 of Figure 3-63, this action is caused by Squeelch Single Shot generating AGC SQUELCH true which is sent to the linear amp.

### 3.5.3.5 Performance Requirements

With the LIN AMP ON true and R/W INOP false, the head must be selected according to Table 3-3. Selected center-tap voltage as measured at pin B on each matrix card head plug is equivalent to a "Y" voltage of  $+0.15 \pm 0.15$  V and disabled center-tap voltage is equivalent to a "Y" voltage of  $+15.0 \pm 1.0$  V.

#### NOTE

Do not unplug a head when a customer's disc pack is installed in the drive. It may destroy customer data on the disc pack.

TABLE 3-3. HEAD AND Y SELECT EQUIVALENCE

Decimal	HEAD (Head Select Line)		Center-tap Selected	Y ENABLE	Head Pin Location
	1	6 8 4 2 1			
0	00000		Y0		0B Right Matrix
1	00001		Y0		9B Left Matrix
2	00010		Y1		1B Right Matrix
3	00011		Y1		8B Left Matrix
4	00100		Y2		2B Right Matrix
5	00101		Y2		7B Left Matrix
6	00110		Y3		3B Right Matrix
7	00111		Y3		6B Left Matrix
8	01000		Y4		4B Right Matrix
9	01001		Y4		4B Left Matrix
10	01010		Y5		5B Right Matrix
11	01011		Y5		3B Left Matrix
12	01100		Y6		6B Right Matrix
13	01101		Y6		2B Left Matrix
14	01110		Y7		7B Right Matrix
15	01111		Y7		1B Left Matrix
16	10000		Y8		8B Right Matrix
17	10001		Y8		0B Left Matrix
18	10010		Y9		9B Right Matrix

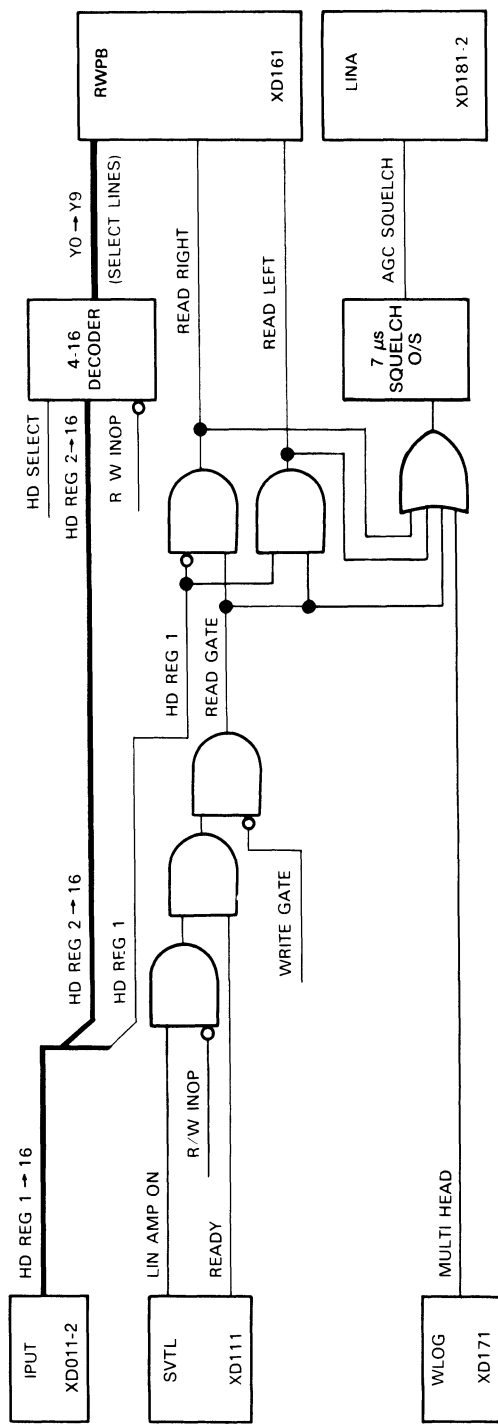


FIGURE 3-63. DATA SAFETY AND HEAD SELECT PCB (Part 2 of 2)

### 3.5.4 Left and Right Matrix PCBs

Left MTRX and Right MTRX perform the same functions, the former for 9 data heads and one servo head, and the latter for 10 data heads. The functions provided are described below, addressing the block diagram of Right MTRX in Figure 3-64.

#### 3.5.4.1 Grounding Head Center Tap

Right MTRX grounds one of ten even-numbered head center taps in response to one of ten Y-select lines. For the case of Y0 true, center tap of Head 00 is grounded as shown in Figure 3-64. Grounding allows selection of a read or write operation, as discussed below in paragraphs 3.5.4.2 (read operation) and 3.5.4.3 (write operation).

#### 3.5.4.2 Connecting Head to Preamp

If a read operation using an even numbered head is selected (READ RIGHT is true), the head is connected to Read Select which selects the Right Preamp as the one to be used. The magnetic fields stored on the recording disc induce a voltage into the selected head every time a flux reversal on the disc is passed. This voltage read from the head (Head 00 for the example in Figure 3-64) passes through its diode matrix and is amplified by a factor of 100, and transmitted to LINA via Line Driver as RIGHT PREAMP 0A and RIGHT PREAMP 0C.

#### 3.5.4.3 Switching Current to Head

If a write operation using an even numbered head is selected (lw RIGHT is true), write current (WRITE DRIVE RIGHT 0A and WRITE DRIVE RIGHT 0C) is switched sequentially from one-half of the head to the other half. This switching is controlled by the signal from the write trigger in WLOG (see paragraph 3.5.6). Applying current to the head writes flux changes onto the disc that are representative of each clock and data bit.

#### 3.5.4.4 Failure Monitoring

There are two failure monitoring circuits on the board, AC Write and Right Y Safety. If more than one head select line is selected (i.e., Y0 and Y1), RIGHT Y SAFETY being a ground voltage is sensed and routed (via RWPB) to pin D17-R19 on WLOG PCB. This signal generates MULTIPLE HEAD SELECT, indicating an unsafe condition in the drive during a read or write operation.

When write current is switched, the head inductance causes voltage spikes. A sample of these pulses is sensed at AC WRITE RIGHT, and is routed (via RWPB) to pin D17-R3 on WLOG PCB. If an "all ones" pattern is written, the negative going pulses at D17-R3 have a pulse width of 40 nsec and occur at 155 nsec intervals. AC WRITE RIGHT generates an AC Write Unsafe condition in the drive during a write operation. Both MULTIPLE HEAD SELECT and TRANSITIONS UNSAFE (AC Write Unsafe) are transmitted to the DCL.

### 3.5.5 Linear Amplifier PCB

LINA (Figure 3-65) is an automatic-gain-controlled amplifier. It selects linear readback data from either the Left or Right Read/Write Matrix PCB, and amplifies the signal to a level adequate for proper data bit detection. The Head Select 1 determines which preamp in MTRX is to be connected to the main amp in LINA. As indicated in the figure, Matrix Select makes this decision based on the condition of HD SEL EVEN (which is true for HD REG 1 false).

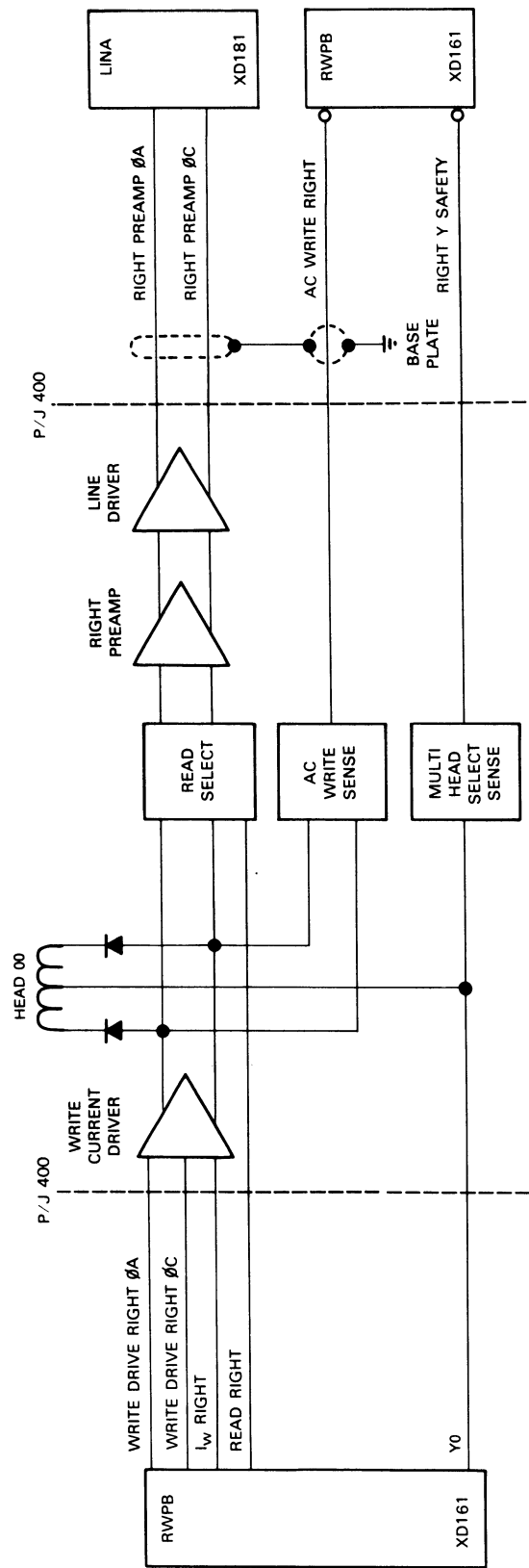
At this point, the signal is supplied to two paths. One path is to the Low Level Line Driver, the output from which may be viewed as any selected head's signal amplitude characteristics (LIN SIG 0A and LIN SIG 0C). Regarding the path to the main amplifier, the read signal passes through a voltage controlled Attenuator which adjusts gain to maintain a constant signal amplitude at the output. Using four stages of amplification, one of attenuation, and a filter, the adjusted head signal is raised to a 4 volt peak to peak differential level (HI LIN SIG 0A and LIN SIG 0C for 2F only) to drive the Detector PCB (DTEC) and an AGC feedback control circuit. The latter supplies the voltages necessary to drive the attenuators.

#### 3.5.5.1 LINA Circuitry

The functional blocks of LINA in Figure 3-65 are described below.

**Matrix Select.** This circuitry consists of two unity gain differential amplifiers with outputs connected in parallel. A current source is switched between the differential amplifiers to select either the left or right MTRX signal.

**Low Level Line Driver.** This is an ac coupled differential amplifier, with an unterminated voltage gain of approximately 2. It supplies a signal which is directly proportional to the linear input signal, for head alignment purposes only.



- NOTES:**
1. ODD-NUMBERED HEADS CONNECT TO LEFT R/W MATRIX PCB. EVEN-NUMBERED HEADS CONNECT TO RIGHT R/W MATRIX PCB.
  2. ILLUSTRATION ABOVE SHOWS HEAD 00 CONNECTED TO RIGHT R/W MATRIX PCB. OTHER EVEN-NUMBERED HEADS (02, 04, 06, 08, 10, 12, 14, 16, 18) ARE SIMILARLY CONNECTED, AND SELECTED USING Y-SELECT LINES AS INDICATED ABOVE.
  3. NOTING THE ABOVE, LOGIC FOR LEFT R/W MATRIX PCB IS THE SAME AS RIGHT R/W MATRIX PCB (INPUTS AND OUTPUTS SAY "LEFT" INSTEAD OF "RIGHT").
  4. SERVO HEAD IS HEAD 19. ITS CENTER TAP IS ALWAYS GROUNDED.

**FIGURE 3-64. RIGHT READ/WRITE MATRIX PCB**

**10:1 Attenuators.** An FET transistor is used as a variable resistance to provide a gain-controlled stage. A pair of chopper transistors having very low junction impedance is also used to effectively ground the signal lines during intervals when AGC SQUELCH is true.

**A=10 Amplifiers.** These amplifiers consist of a linear IC differential amplifier with a fixed voltage gain of 10 and bandwidth of 70 MHz. Test points are provided at the outputs of each amplifier. Two stages of attenuation and amplification are used to provide 40 dB of possible gain control.

**Filter and A=2 Amplifier.** A 5 pole Butterworth filter is used to limit the amplifier bandwidth to approximately 6 MHz, the lowest bandwidth for error-free recovery of MFM encoded data at the highest expected data rate. In addition, the phase characteristic of the filter is used to compensate other system phase characteristics, thereby providing a linear phase response. The filter is terminated by an emitter follower stage which drives a dc coupled differential amplifier.

**High Level Line Driver.** An emitter follower stage provides a low impedance to drive the lines to the DTEC board (HI LIN SIG  $\emptyset$ A and HI LIN SIG  $\emptyset$ C). This output is sampled by automatic gain control circuitry, and maintained at 4 V p-p differential for 2F signals (all ones or all zeroes bit pattern). A zener diode is used to adjust the dc signal level.

**Resolution Filter.** This filter consists of an RC coupled differential amplifier. The level of the linear signal from MTRX varies with frequency; with changing data frequency, the AGC circuit would accentuate this problem. The Resolution Filter's RC coupling is selected to attenuate signals opposite to the data signal frequency response, to provide an AGC error voltage which is constant with frequency.

**Full Wave Rectifier.** The high level linear output signal is full wave rectified by a pair of emitter followers which are diode coupled. The result is a dc level which may be compared with a reference level, to provide a control voltage to adjust the amplifier gain.

**AGC Filter.** The full wave rectified signal is smoothed by a single section RC filter, providing a dc voltage to compare with the AGC reference level. The time required by the automatic gain control circuitry to respond to changes in level of the input signal is dependent on the bandwidth of the RC filter. The filter is coupled to the Full Wave Rectifier with a diode providing a peak detector. The capacitor charges up to the peak value of the rectified signal

plus the AGC reference voltages. An emitter follower is used to isolate the filter from the following amplifier circuitry. A transistor is used to discharge the capacitor during intervals when AGC SQUELCH is true. A separate input pin is provided for controlling this transistor to allow LINA testing in an open loop condition.

**Discharge Amplifier.** A differential current switch coupled to the Full Wave Rectifier through a lead network discharges the AGC Filter during the leading edge of the rectified signal. The discharge current is selected to give the filter approximately equal charge and discharge characteristics. A second feature of this circuit is that the filter is not discharged during the absence of a signal, thereby maintaining the AGC level through a disc defect region.

**AGC Amplifier.** The filtered signal is compared with a fixed reference by a linear IC amplifier with a gain of 50. The resultant voltage is used to control the gate voltage of the FET attenuators, adjusting the linear amplifier gain until the reference level is achieved.

**Diagnostic Gain Control Circuits (Optional).** Input pins D18-L29 (READ LOW R/W DIAG2) and D18-L26 (READ HIGH R/W DIAG 4) are provided to select reference voltages above and below the normal value. This yields three possible levels for the High Linear Signal amplitude which is valuable for diagnostic system analysis. If diagnostic gain control circuits are not required, pin D18-L29 is tied to +5 V through a resistor, and pin D18-L26 is grounded.

### 3.5.5.2 Performance Requirements

LINA PCB (Logic XD181-2) is located on logic gate location D18. The input/output performance requirements are presented below.

- a. For a repetitive "all ones" bit pattern (1111 1111), the read signal amplitude at inputs and outputs shall be verified as follows:
  - **PREAMP  $\emptyset$ A/ $\emptyset$ C.** The peak-to-peak read back signal measured differentially shall be approximately 125 mv on cylinder 404 (RPO5) or approximately 200 mv on cylinder 807 (RPO6) at the piggy back connector on D18, between pins 1 and 9 for the even heads, and between pins 3 and 7 for odd heads. The peak-to-peak read signal measured on each pin should be within 10% of each other. The signal base line voltage (dc) on each pin is +1.0 V typical.



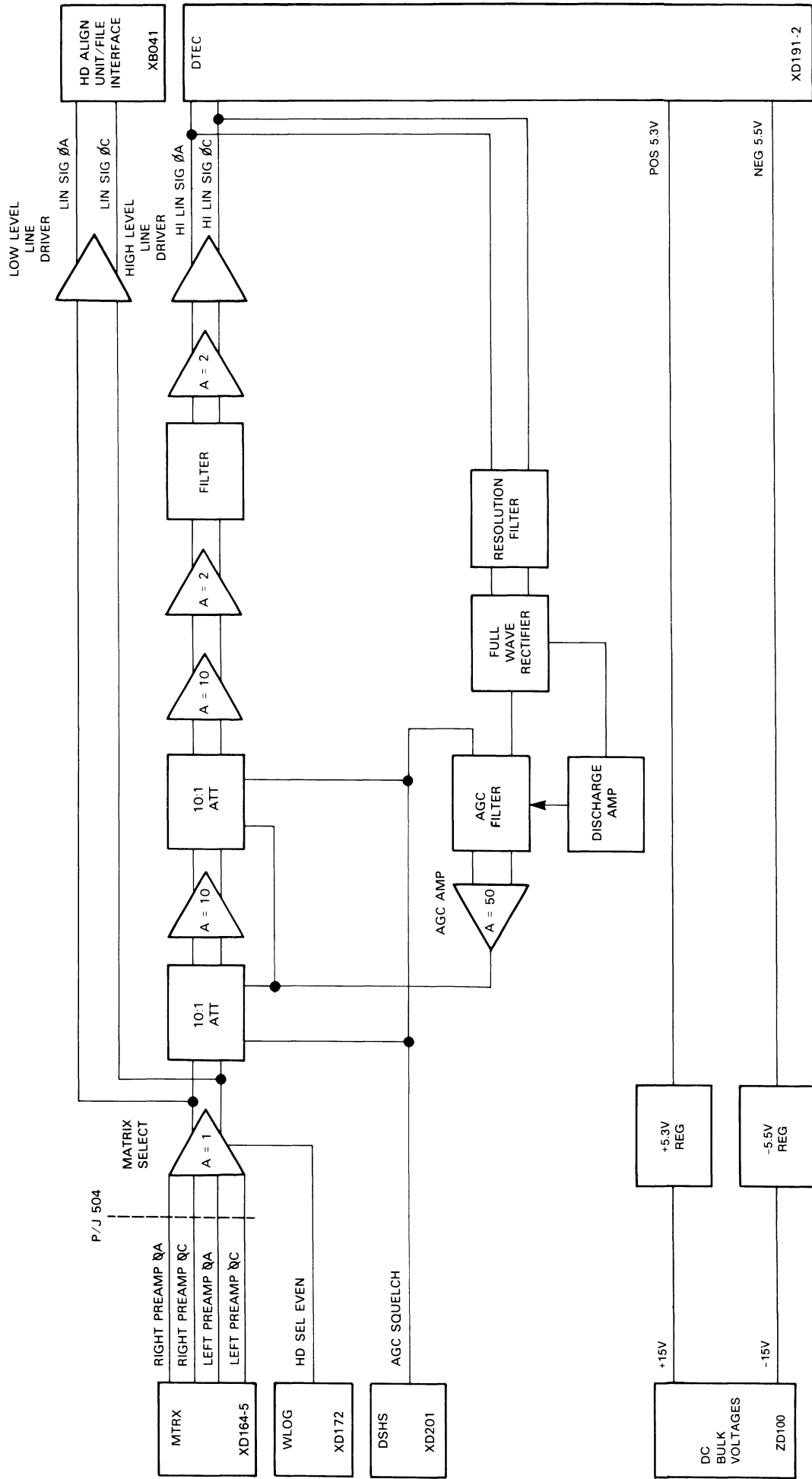


FIGURE 3-65. LINEAR AMP PCB

- **LIN SIG  $\emptyset A/\emptyset C$ .** The peak-to-peak differential amplitude measured between pins D18-L38 and D18-R38 shall be approximately 250 mv on cylinder 404 (RP05) or approximately 400 mv on cylinder 807 (RP06). The signal base line voltage on each pin should be  $+1.40 \pm 0.20$  VDC.
- **Preamplifier Recover Time.** Recovery of the preamplifier (R/W Matrix) signal base line must be complete to 90% within 10  $\mu$ sec following the Read Left true (D20-L4) or Read Right true (D20-R3), as measured differentially between pins D18-L38 and D18-R38 (LIN SIG  $\emptyset A/\emptyset C$ ).
- **HI LIN SIG  $\emptyset A/\emptyset C$ .** The read signal must measure  $4.0 \pm 0.3$  V (p-p) between HI LIN SIG  $\emptyset A$  and HI LIN SIG  $\emptyset C$  WITHIN 20  $\mu$ s following the true of false transition of AGC SQUELCH (D18-L35). The signal is to be measured differentially at pin R20 and R21 of the D19 Card. The amplitude remains constant regardless of cylinder. The signal base line voltage on each pin shall be  $-3.4 \pm 0.8$  VDC. Note that for a repetitive 10101010 bit pattern (1F), the read back signal shall be approximately 6.2 V p-p differential between these pins.
- b. **AGC Voltage Test Point.** For a train of "all ones" bit pattern on cylinder 404 (RP05) or cylinder 807 (RP06), the AGC voltage at pin D18-L34 shall be  $-3.2 \pm 1.5$  VDC.
- c. **VOLTAGE REGULATORS.** POS 5.3 V measured at pin D19-L29 is  $+5.30 \pm 0.40$  V/-0.20 VDC. NEG 5.5 V measured at pin D19-R19 is  $-5.50 \pm 0.30$  VDC.
- d. **BIAS Test Point.** BIAS voltage at pin D18-L24 shall be  $-9.20 \pm 0.25$  VDC.

### 3.5.6 Detector PCB

Detector PCB (Logic Page XD192) is located on Logic Gate position D19. It provides detection and gating of peaks in the linear read data signal (which contain the recorded digital information) and generation of corresponding ECL level read data pulses. Head Select circuits on the Logic Page XD191 are not used, and are replaced by Head Select Circuits on Data Safety and Head Select PCB (referring to Logic Page XD203).

#### 3.5.6.1 Detector Circuitry

Referring to Figure 3-66, Read signal HI LIN SIG  $\emptyset A/\emptyset C$  from LINA PCB is received by a Differentiator and Limiter which provide timing information for the Detector circuitry. Detector and Gate Generator provide gating information; their output signals are ANDed to drive a Data Latch-controlled Bidirectional One Shot which places RAW DATA on differential lines to the VFO.

Functional blocks of Figure 3-66 are described below.

**Differentiator and Limiter.** Read signal received from LINA (HI LIN SIG  $\emptyset A$  and HI LIN SIG  $\emptyset C$ ) is differentiated using a RC coupled differential amplifier, changing the signal peaks to zero crossings. For each side of the differentiating amplifier, adjustable current sources are used to maintain signal symmetry, since any asymmetry will be reflected as asymmetry in the timing of the resultant waveforms. The signal from the Differentiator circuit is limited to 0.8 volt peak-to-peak differential by a pair of hot carrier diodes.

**Squaring Amplifiers.** The limited signal is further shaped by a high gain four-stage amplifier to produce a square wave signal. The test point (TP1) is provided to monitor the symmetry of the squaring amplifier output waveform. Due to dc offset and circuit component tolerances, a potentiometer R105 is provided to be adjusted so that the waveform at TP1 is symmetrical. The adjusting screw on the potentiometer is sealed in factory after PCB testing.

**100 nsec Delay and A=10 Amplifier.** A delay line is used to align the pulses at the Data Window for proper gating. The signal delay in Gate Generator is a function of pulse amplitude. The delay line is adjusted to maintain the pulse from Gate Generator for both minimum and maximum input signal levels. Test points are provided for alignment purposes. The delayed data is reshaped using an IC amplifier with gain of approximately 10.

**Split One Shot.** A capacitively coupled differential switch generates pulses from each edge of the input signal. The pulse width determined by the RC combination of the emitter circuit is approximately 38 nsec. Separate outputs are provided for pulses representing positive or negative going edges for use by the Data Window.

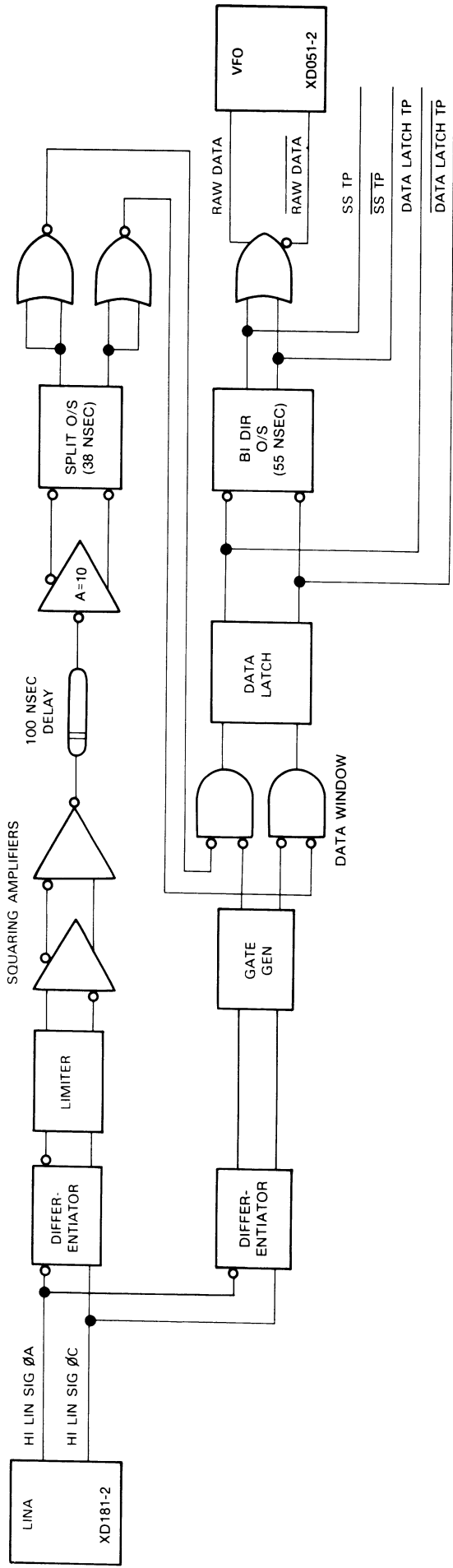


FIGURE 3-66. DETECTOR PCB

**Differentiator and Gate Generator.** This is a variable threshold differential Schmitt trigger. Crossover points of the differentiated linear signal are detected by a high gain differential saturating amplifier with positive feedback. Due to the high gain, the output remains saturated until the differential input signal reaches the crossover point. At the crossover point, the output changes state. The positive feedback adds a dc component to the incoming signal, which adds an offset to the crossover point. This offset determines the minimum amplitude input signal which can transfer through the circuit. The amount of offset can be increased during "Address Mark Search" by increasing the amount of positive feedback. This is necessary to make the gate generator less sensitive to noise during this time. If +Address Mark Search (optional) is not required, the signal input pin D19-L21 must be grounded.

**AND Gates (Data Window).** Data signal pulses are separated from noise signal pulses by AND gates which determine whether the pulse was recognized by both the Split One Shot and the Gate Generator. This one shot may be triggered by both signal peaks and noise pulses; however, Gate Generator responds only to signals of alternating polarity and of a given amplitude. The output of the "Data Window" is a pulse representing only data pulses.

**Data Latch.** Output from the Data Windows drive both the set and reset lines of the Data Latch; secondary pulses due to noise are ignored. The resulting square wave edges contain the timing information needed by the Bidirectional One Shot.

**Bidirectional One Shot and ECL OR Gate.** A capacitively coupled differential switch regenerates pulses from each edge of the input square wave. The RC combination of the emitter circuit provides pulses 55 nsec wide. One output contains pulses representing positive going edges, while the other output contains pulses representing negative going edges. The two outputs are combined with an ECL ORing circuit with differential output to generate plus and minus Raw Data signals.

### 3.5.6.2 Performance Requirements

DTEC (Logic Gate location D19) performance requirements are presented below.

- a. **Input Requirements:** Input requirements for HI LIN SIG  $\emptyset$ A, HI LIN SIG  $\emptyset$ C NEG 5.5 V and POS 5.3 V have been described on paragraph 3.5.5.2.

### b. Output Performance

- The maximum bit shift for clock or data pulses in a train of 0000 or 1111 bit pattern must be within  $\pm 10$  ns, measured at D19-L26 (+Raw Data) and D19-L27 (-Raw Data). This requirement must be met at any cylinder and particularly at cylinder 814 (RP06) or cylinder 410 (RP05), (Figure 3-71).
- The Raw Data pulses measured at pins D19-L26 and D19-L27 must have a pulse width measured between the 50% points of  $55 \pm 10$  ns.

- c. **Test Point Waveforms.** The waveforms of Test Points are shown in Figures 3-67 to 3-71 for reference only. Note that HI LIN SIG  $\emptyset$ A (D19-R20) in these figures is not an actual read-back head signal, and is the waveform of a sine-wave oscillator output with a frequency of 3.22 MHz.

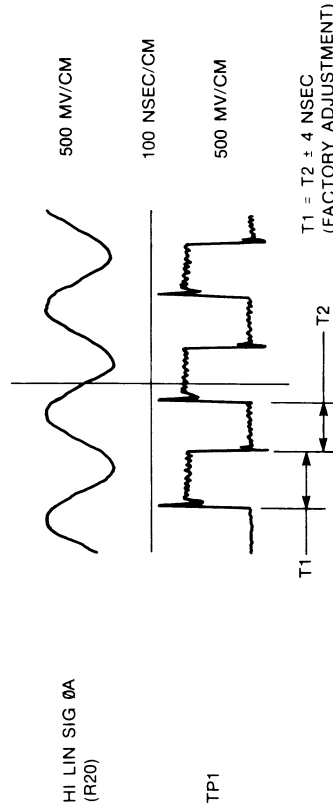


FIGURE 3-67. DIFFERENTIATOR SYMMETRY

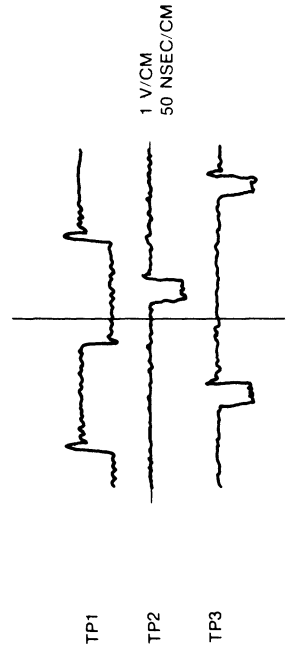


FIGURE 3-68. SPLIT ONE SHOT

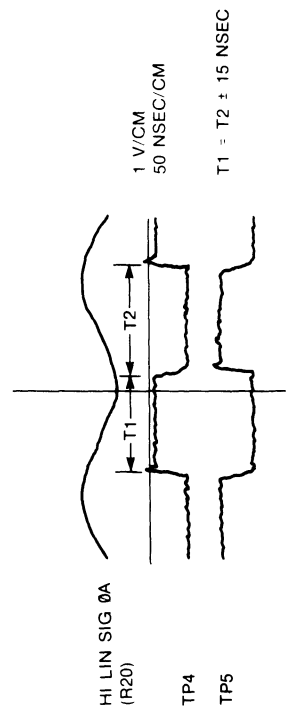


FIGURE 3-69. GATE GENERATOR

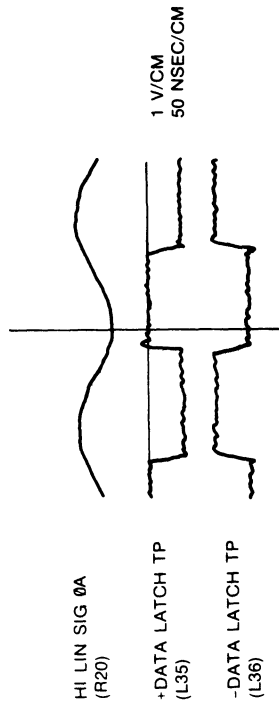


FIGURE 3-70. BIDIRECTIONAL ONE SHOT, DATA LATCH

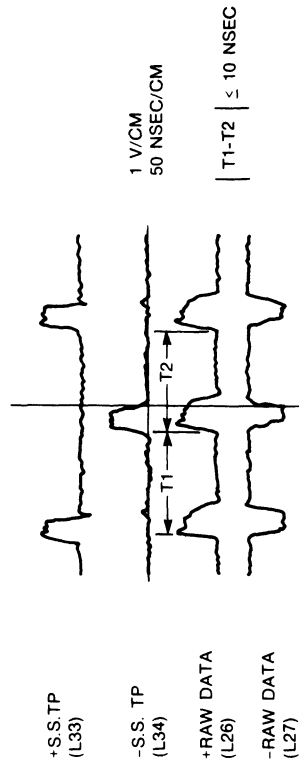


FIGURE 3-71. BIDIRECTIONAL ONE SHOT

### 3.5.7 Write Logic PCB (Referring to Logic Page XD171-2)

Functions provided by WLOG are described below, addressing the block diagram in Figure 3-72.

#### 3.5.7.1 Supplying Head Switching Current

Write current is generated using the 35 Volt Regulator (Figure 3-72). The write circuitry associated with this supply is separated into two identical sections. These sections supply write current to the head coil to write data on the disc using an odd numbered head ( $I_w$  LEFT) or an even numbered head ( $I_w$  RIGHT), as follows:

- Current subtractor received three cylinder address inputs (PGM WRT 1, 2, 4) which subtract amounts of write current through the selected head. The amount of write current is determined by the disc cylinder position at which the heads are located. Less current is used when writing in the inner cylinders. Refer to Table 3-4.
- The particular current source activated depends on the state of HD REG 1. If true, Left Current Source is activated and generates write current for odd numbered heads. If HD REG 1 is false, Right Current Source is activated and generates write current for even numbered heads.
- Generating write current is stopped if WRITE AC CLAMP or R/W INOP (DEFEAT) is true, which is the case if a fault condition occurs while writing. WRITE AC CLAMP shorts write current to ground at the end of a write operation.

#### 3.5.7.2 Supplying Write Data

MFM write data received by VFO is sent to WLOG. The data pulses received by WLOG (ECL WRT DATA) are translated from ECL to TTL levels, then connected to a differential amplifier which establishes the proper voltage and current levels for sending write data pulses to the Left or Right Matrix PCB as WRITE DRIVE LEFT (or RIGHT)  $\emptyset$ A and  $\emptyset$ C. Write Trigger is inhibited by Read Command from the DCL. If the DCL tries to write and read at the same time, Transition Unsafe shall be sent to the DCL. If WLOG receives PAD DATA D17-R8 (optional) at TTL levels, then the input OP PAD (D17-L9) should be grounded.

TABLE 3-4. WRITE CURRENT AMPLITUDE

CYLINDER RANGE		SUBTRACTOR CIRCUIT			WRITE CURRENT Peak-to-Peak Differential		
RP06	RP05	PW1	PW2	PW4	RP06	RP05	
0	63	0	127	OFF	OFF	112 mA	180 mA
64	127	128	255	ON	OFF	109 mA	173 mA
128	191	256	383	OFF	ON	106 mA	166 mA
192	255	384	511	ON	ON	103 mA	160 mA
256	319	512	639	OFF	OFF	99 mA	153 mA
320	383	640	767	ON	OFF	95 mA	147 mA
384	410	768	814	OFF	ON	92 mA	140 mA

#### NOTE

1. In RP06 drive:  
Input PGM WRT 1 is cylinder address 138.  
Input PGM WRT 2 is cylinder address 256.  
Input PGM WRT 4 is cylinder address 512.
2. In RP05 drive:  
Input PGM WRT 1 is cylinder address 64.  
Input PGM WRT 2 is cylinder address 128.  
Input PGM WRT 4 is cylinder address 256.
3. Write current amplitude is measured at the head plug on Left or Right Matrix with a special tool and current probe. Writing a train of 10101010 bit pattern is used for this current measurement. **Warning:** Do not make current measurement when a customer's disc pack is installed in the drive; it will destroy customer's data previously written on the pack.

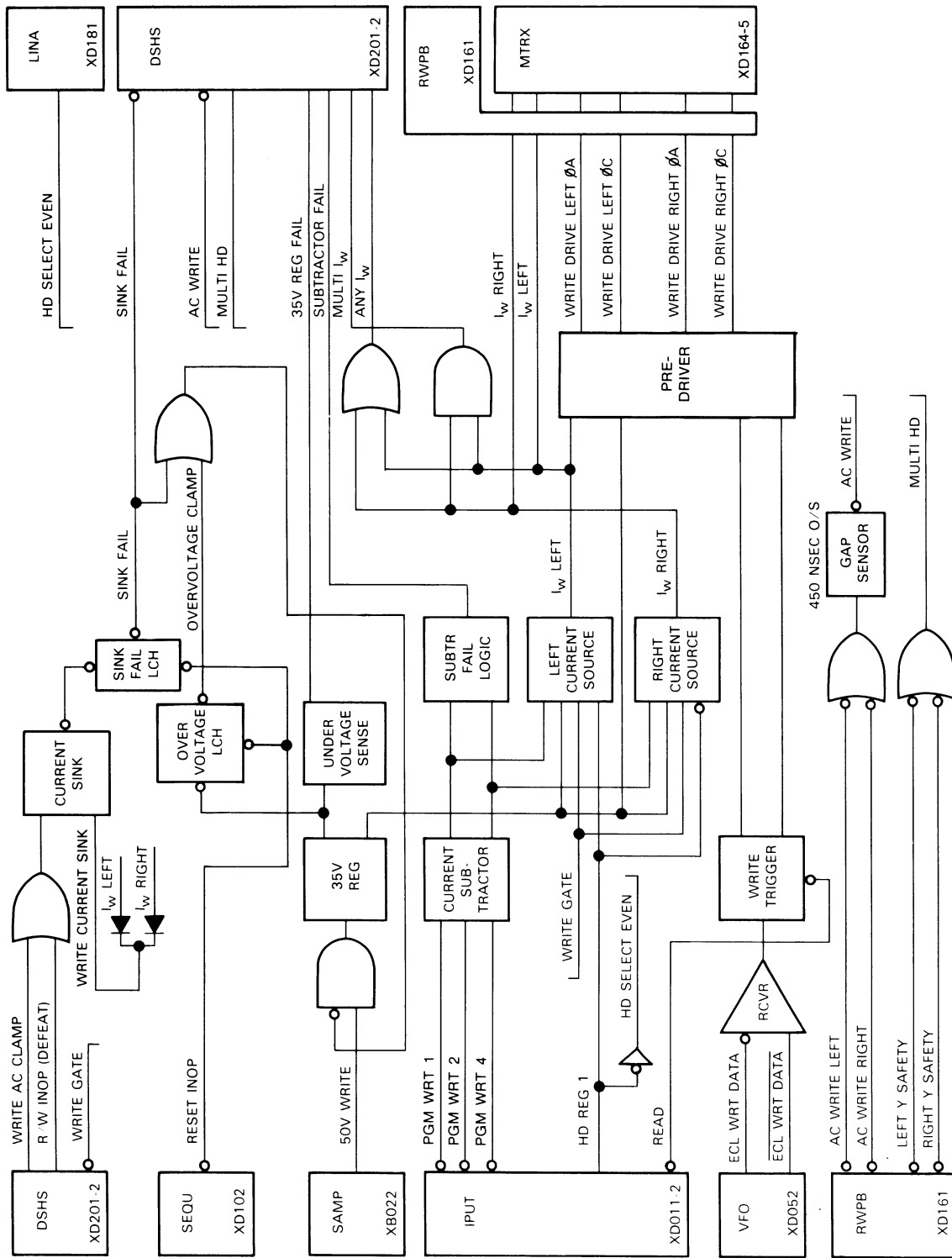


FIGURE 3-72. WRITE LOGIC PCB

**BLANK**



### 3.5.7.3 Failure Monitoring

WLOG generates most of the safety signals received by DSHS during a write operation for failure monitoring. These signals are (refer to Figure 3-72):

- SINK FAIL is true if, at the end of a write operation, write current is not shorted to ground within 700 nsec.
- AC WRITE is false if no data was written within 383 nsec. The -AC Write (D17-L3) remains at ground during a normal write operation.
- MULTI HD is true if more than one recording head on either the Left or Right Read/Write Matrix PCB is active.
- 35 V REG FAIL is true if the regulator voltage is either too low or high for writing.
- SUBTRACTOR FAIL is true if the wrong write current is selected for a particular cylinder.
- MULTI I<sub>w</sub> is true if both LEFT and Right Current sources are turned on.
- ANY I<sub>w</sub> is true if any write current source is on.

### 3.5.7.4 Connecting Preamp to Linear Amplifier

WLOG inverts the received state of HD REG 1 to generate HD SEL EVEN, and sends it to LINA which connects itself to either the Left Matrix PCB (HD SEL EVEN is false) or Right Matrix PCB (HD SEL EVEN is true).

### 3.5.7.5 Performance Requirements (Refer to XD171-2)

Input requirements for AC Write Left, AC Write Right, Left Y Safety, Right Y Safety are described in paragraph 3.5.4.4.

Output signals will be verified as follows:

- A scratch disc pack should be used for troubleshooting write problems; otherwise it will destroy customer's data previously written on their disc pack.
- **+35 V TP:** With Write Gate true (ground voltage at pin D17-L11), the voltage at pin D17-R37 is measured to be  $+34.6\text{ V} \pm 0.5\text{ VDC}$ . The voltage is adjusted by the potentiometer R6. The adjusting screw on the potentiometer is sealed in factory after PCB testing.
- **I<sub>w</sub> Left (D17-R36) or I<sub>w</sub> Right (D17-R35):** The voltage on each pin shall be approximately  $-0.5\text{ V}$  when the current source is off, and approximately  $+20\text{ V}$  when the current source is selected for writing.
- **Write Drive Left 0A (D17-R13)/0C (D17-R14), Write Drive Right 0A (D17-R12)/0C (D17-R14):** If ECL Write Data signal is present at pins D17-L10 and D17-R10, and Read (D17-R7) is false, the Write Drive switching signal on each pin shall be approximately  $+18\text{ V}$  to  $+19\text{ V}$ . Note that each switching transition (positive or negative) represents data or clock bit to be written on the disc pack.

### 3.5.8 Operation Flowcharts and Timing Diagrams

Figures 3-73 and 3-74 present flowcharts and timing diagrams of normal write and read operations, for use in classroom instruction on the basic functions provided by the drive.

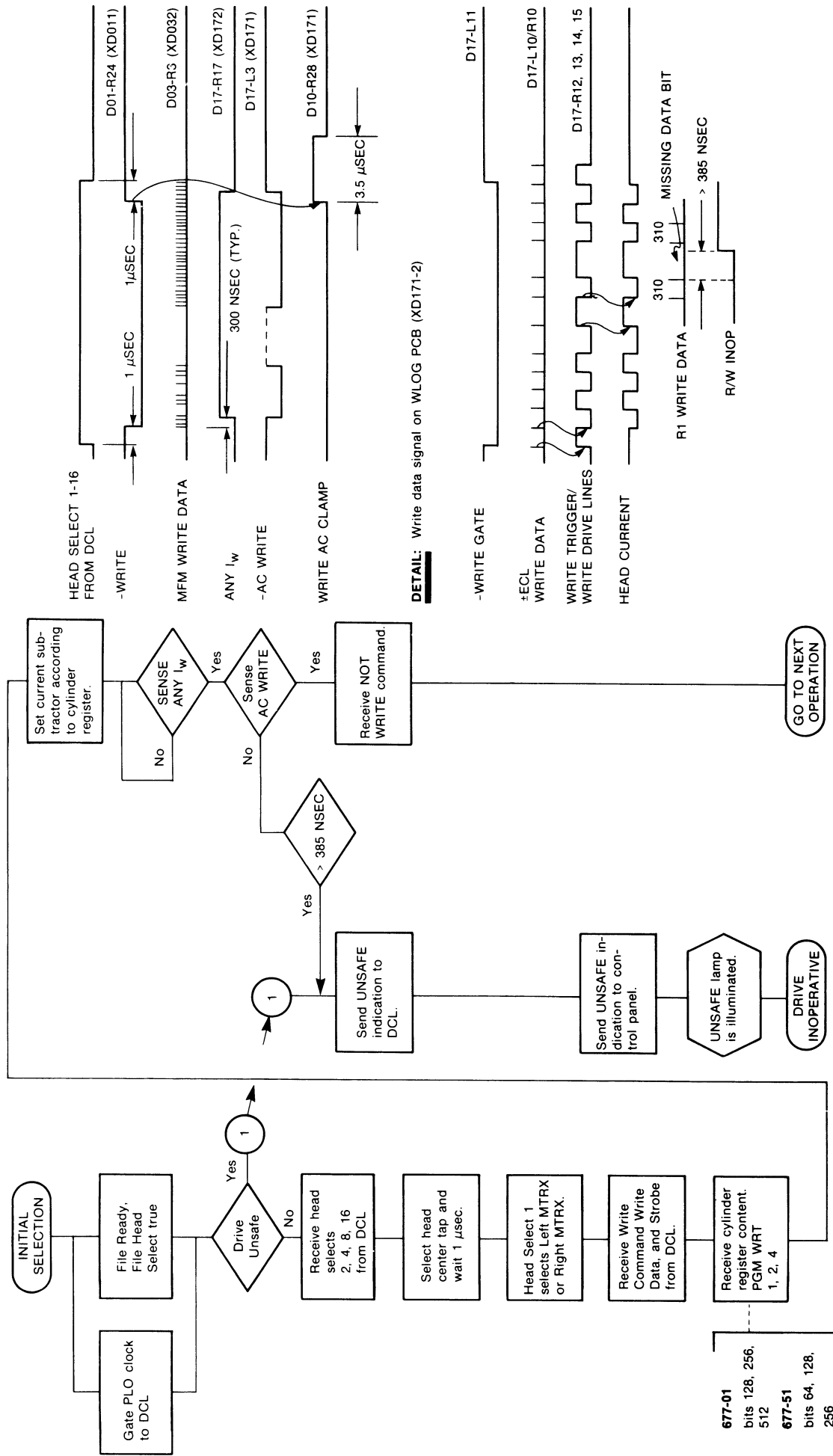


FIGURE 3-73 WRITE OPERATION FLOWCHART AND TIMING

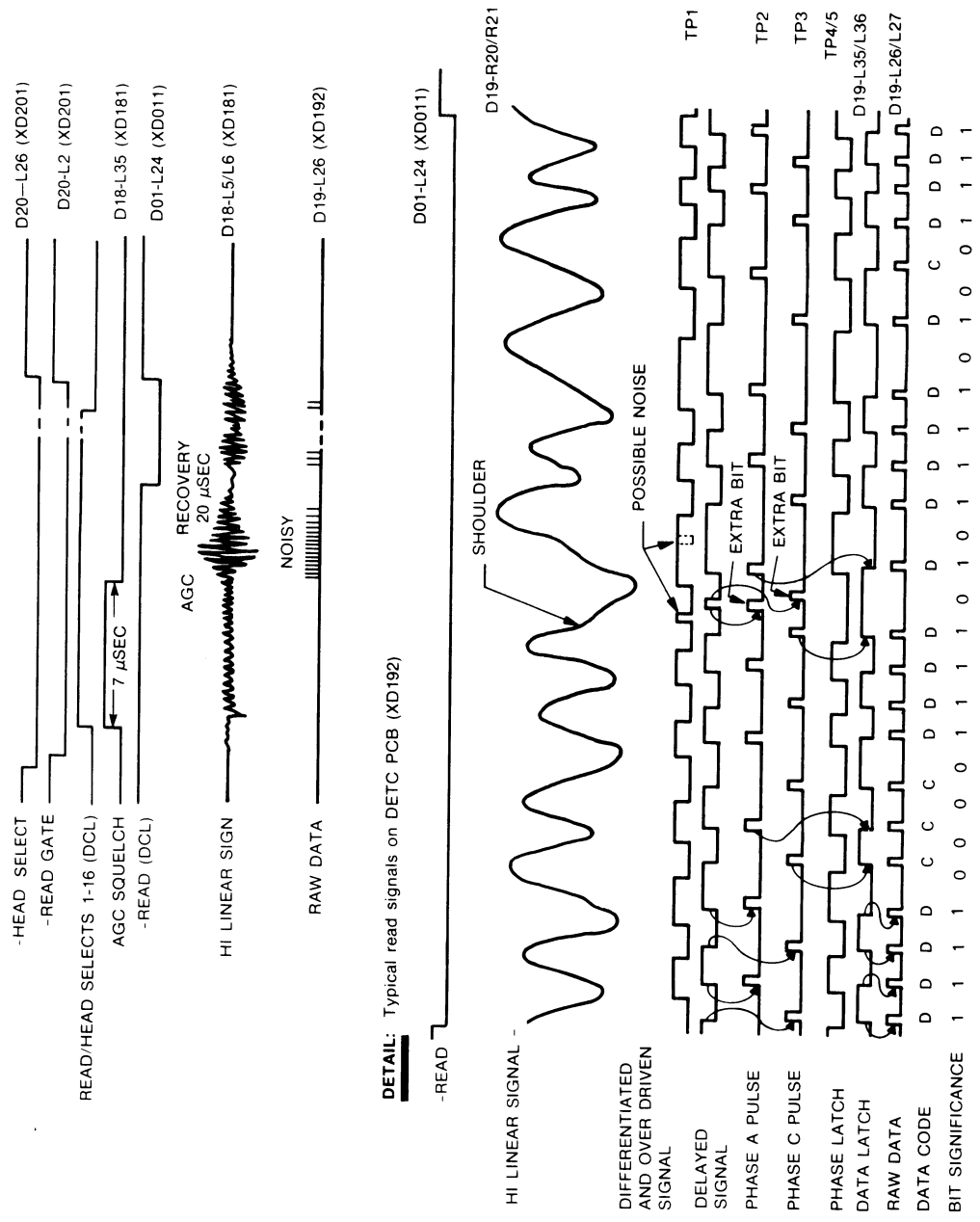
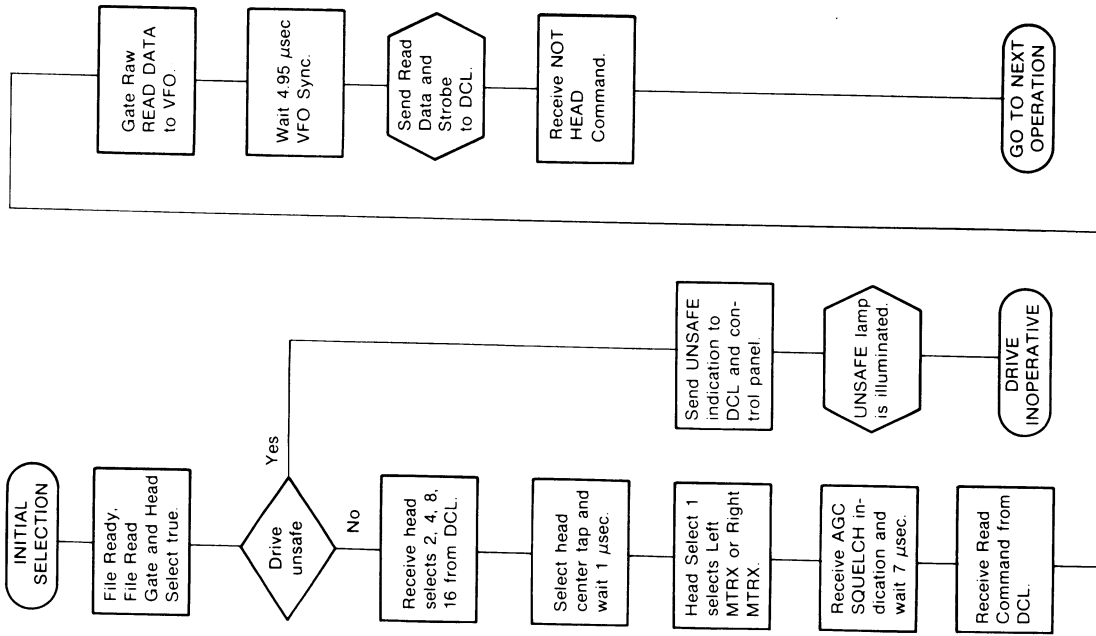


FIGURE 3-74. READ OPERATION FLOWCHART AND TIMING

## 3.6 SPINDLE CONTROL SYSTEM

### 3.6.1 System Description

The Spindle Control System is used to execute and control sequencing of the drive. Sequencing means accelerating the disc pack "up" to rated rotational speed, holding speed constant, and decelerating "down" to zero. To execute sequencing, the system uses a pack drive assembly which consists of the drive motor and spindle — and ancillary hardware. To control sequencing, the system uses sequence control circuitry which receives instructions from the Operator Control, DCL Support, and Servo Systems, and the door closed switch — and processes these instructions to either control normal system operation or issue an abnormal stop indication. These elements of the system are described below.

#### 3.6.1.1 Pack Drive Assembly

Referring to Figure 3-75, the disc pack attaches to the spindle, and the drive belt attaches the spindle to the pulley which is mounted on the motor shaft. The spindle is part of a precision ball-bearing subassembly which is aligned to the positioning motor and carriage way at the factory.

The spring (Figure 3-75) provides belt tension. When power is applied to the drive motor, pack rotation reaches 3600 rpm within 20 seconds. Electrodynamic braking power is applied to stop pack rotation within 20 seconds, to terminate normal sequencing (down) or to respond to detection of a serious malfunction in the drive. Fast braking is achieved by applying dc current to the motor, thereby creating an electrodynamic field opposing motor rotation.

A pack cover on sensor switch (Figure 3-75), which protrudes through the shroud, is activated by its contact with the disc pack cover. Activation of the switch, which is in parallel with the door locked switch, prevents the sequence logic from sensing door locked, and mechanically locks the spindle to the pack via the spindle locking arm.

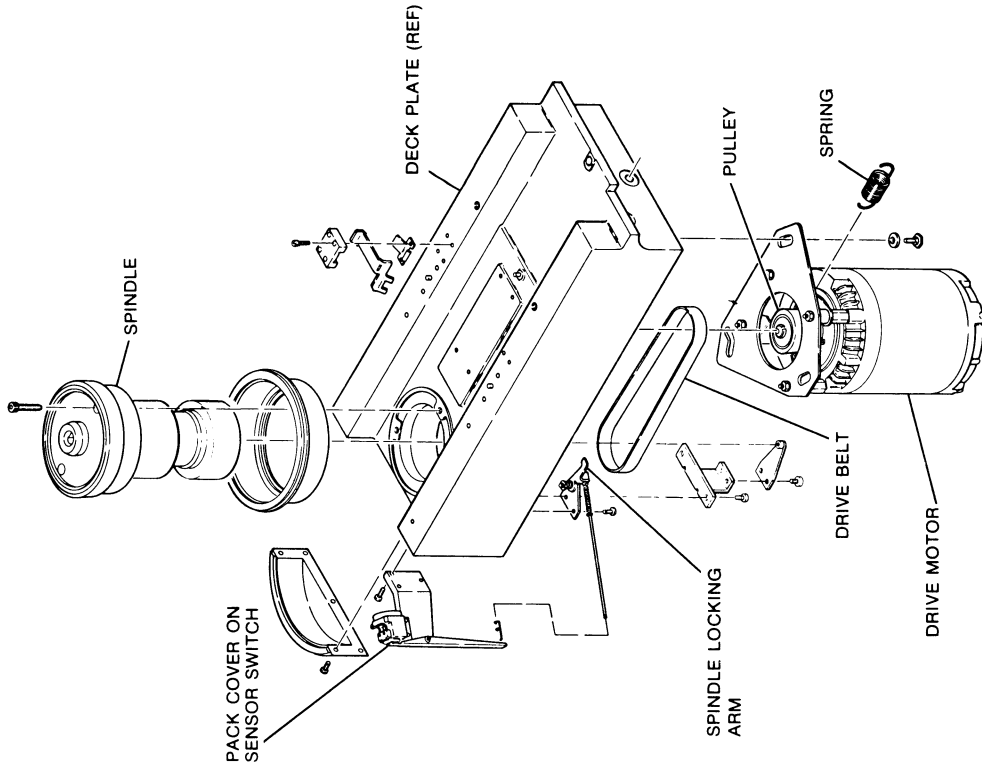


FIGURE 3-75. PACK DRIVE ASSEMBLY

### 3.6.1.2 Control Circuitry

While accelerating from zero to 3600 rpm, the drive motor requires considerably more current than is required thereafter to maintain full rated speed. For this reason, only one of the drives attached to the host system is allowed to perform an up sequence at one time. The drive that is sequencing up sends an inhibit signal to all other drives (via the DCLs attached to these drives) which prevents their drive motors from starting. This inhibit signal is removed when the starting drive reaches a particular rpm, designated such that the motor current required to continue acceleration is considerably less than at start up.

Signals controlling motor operation are generated in SEQU (Sequence PCB), located in the drive's logic file. These signals allow ac connection to the motor, and dc current to flow in the motor windings. SEQU is described in paragraph 3.6.2.

The power distribution unit (PDU) in the Power System uses outputs from SEQU to provide additional motor control functions. BRAK (Brake PCB) in the PDU contains a switching transistor and interlocks for dc current control. SUPR (Arc Suppressor PCB) in the PDU provides a discharge path for energy stored in the motor windings when ac power to the drive motor is disconnected. The Power System is described in paragraph 3.9.

### 3.6.2 Sequence PCB

Functions provided by SEQU are described in the following paragraphs, addressing the block diagrams in Figure 3-76 (Parts 1 and 2).

#### 3.6.2.1 Starting Sequencing

Referring to Part 1 of 2 of Figure 3-76, start conditions are satisfied (START COND is true) if no dc power failure in the drive is detected (CLEAR is false), no other serious malfunction is detected (ABN STOP is false), the pack access door is locked closed (DR LKD is true), and the drive is not manually stopped (START is true).

The signal START COND is used internally only.

#### 3.6.2.2 Up Sequencing

Refer to the flow of logic across the top of Figure 3-76, Page 2 of 2. To initiate an up sequence, a drive must have its start conditions satisfied (START COND is true) and be the only drive in the host system that is up

sequencing, and heads retracted (HDS RET is true), and pack rotation less than upspeed (UPSPEED is false). Sequence Up FF, Spindle FF, and Retract Heads FF are set, the latter momentarily.

Sequence Counters (Page 1 of 2) are activated and at 21.7 seconds upspeed is tested. As shown in Page 2 of 2, an upspeed failure is an abnormal stop condition. As shown in Page 1 of 2, ABN STOP being true disables sequencing and removes the indication that start conditions are satisfied.

#### 3.6.2.3 Down Sequencing

Set Sequence Down SS (Page 2 of 2) is fired if start conditions are not satisfied. In this event, Sequence Down FF and Retract Heads FF are used to generate RETRACT HEADS true, and then the Spindle FF resets to cut ac power to the drive motor. At 0.340 seconds, the Dynamic Brake (DB) FF is activated. At 0.425 seconds, the Dynamic Brake Current (DCDB) FF is activated.

Down sequencing brakes the spindle to a full stop in approximately 20 seconds. At 19.0 seconds, holding the pack access door in a locked condition is terminated to allow operator access to the almost-stopped or stopped disc pack.

The abnormal stop conditions (inputs to Abnormal Stop Register shown in Page 1 of 2) are:

- Servo operation in the emergency retract mode is required (ER ACTIVE is true).
- Emergency Retract Power is lost (ER LOSS is true).
- Servo is unable to perform a recalibrate operation for two times in a row (SERVO RETRACT is true).
- Servo is unable to complete a seek operation and heads are retracted (ANDed result of SK INCOMPLETE true and HDS RET true).
- Heads are retracted but the servo heads loaded signal is true (ANDed result of HDS RET true and HEADS LOADED true).
- Upspeed test indicates that 70% of full rated speed was not achieved at 21.7 seconds (ANDed result of UPSPEED false and UPSPEED TEST FF true).

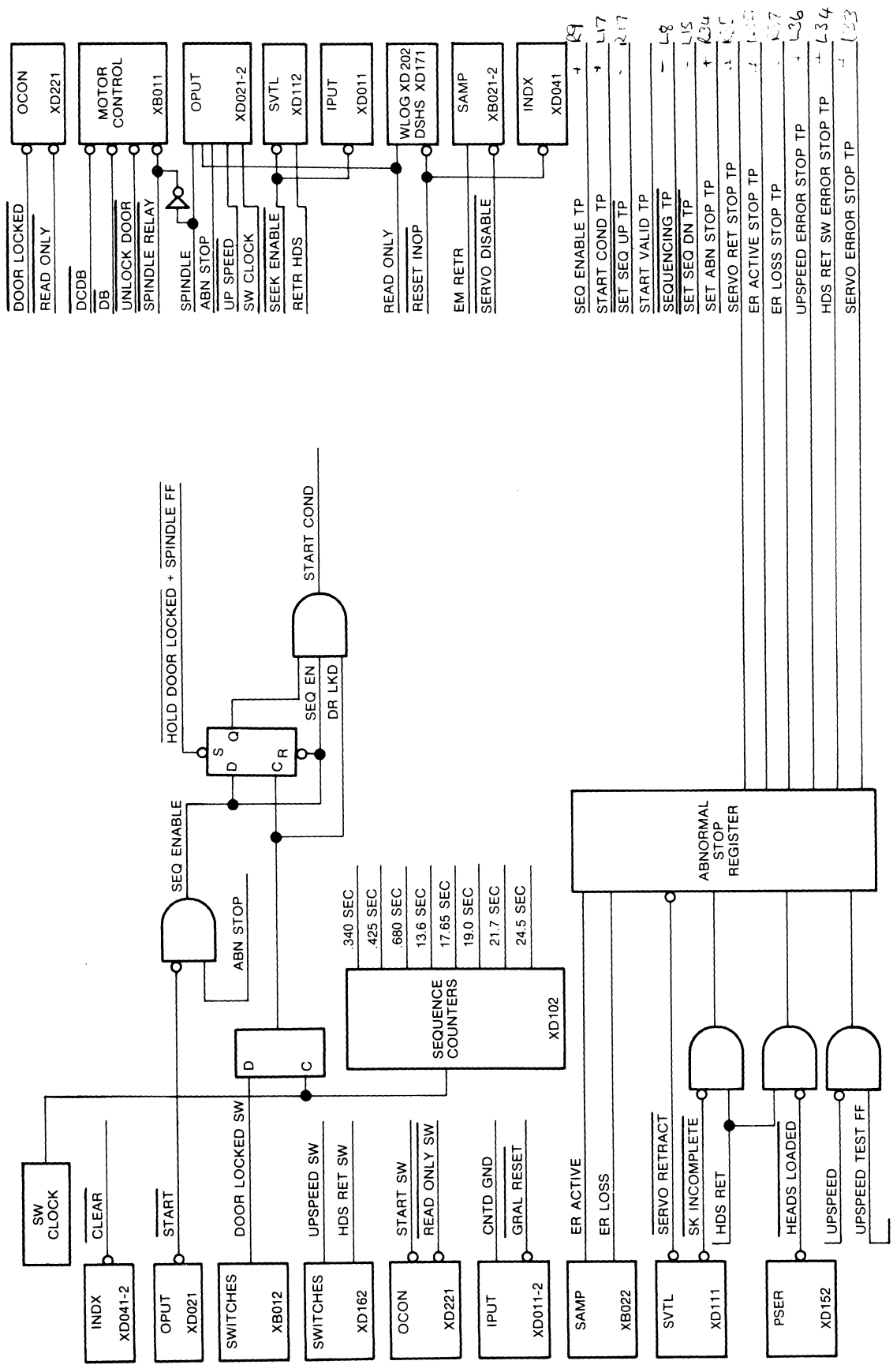


FIGURE 3-76. SEQUENCE PCB (Part 1 of 2)

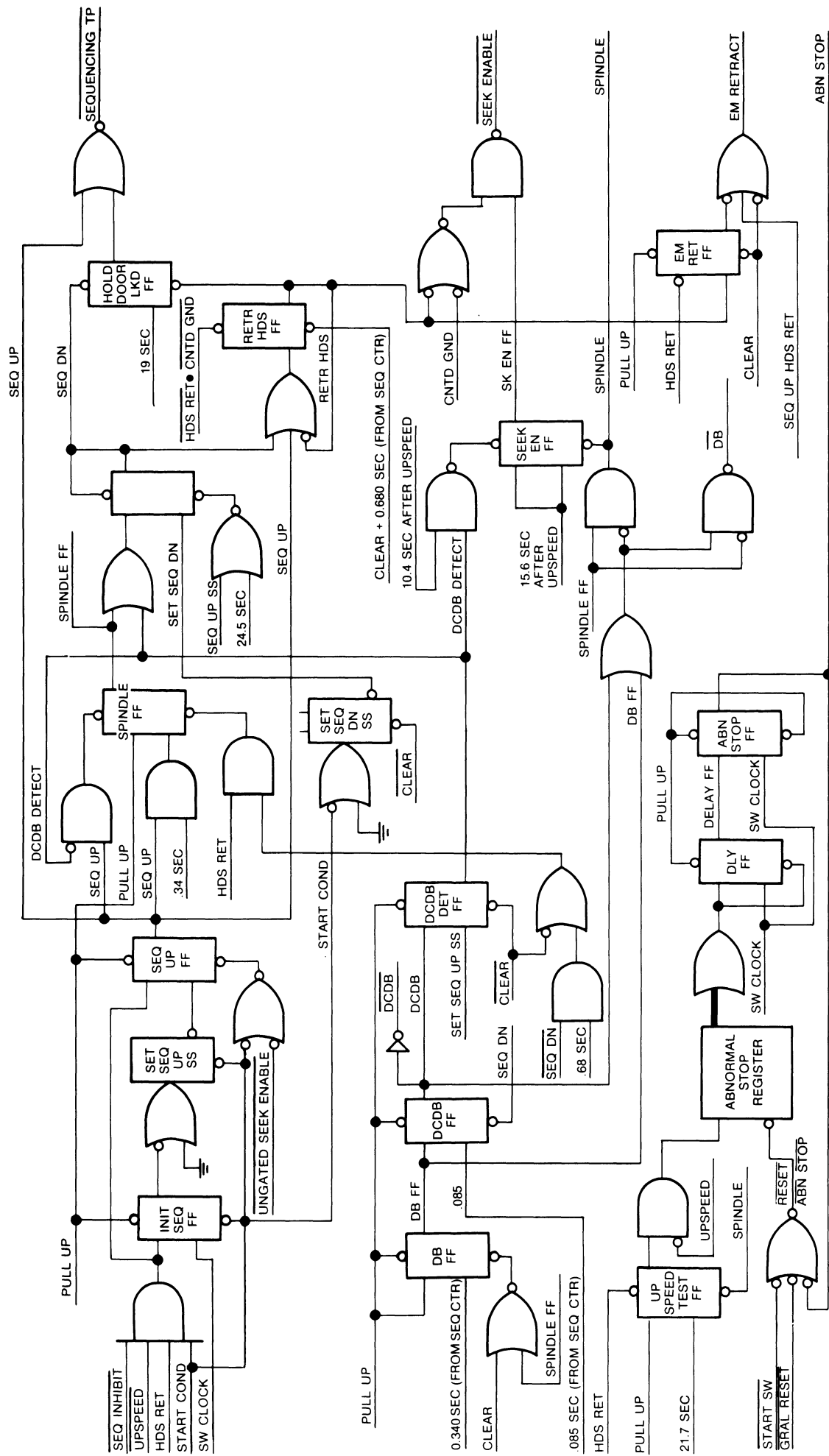


FIGURE 3-76. SEQUENCE PCB (Part 2 of 2)

## 3.7 PACK ACCESS SYSTEM

### 3.7.1 System Description

The Pack Access System is used to provide operator access to the pack area for loading and unloading disc packs. It consists of a sliding glass door assembly, locking mechanism, and ancillary hardware. These elements of the system are described in paragraph 3.7.2. The significance of an effective air seal (as provided), and its operation, are discussed in paragraph 3.7.3.

### 3.7.2 Door Assembly and Locking Mechanism

The drive uses a waist high, sliding glass door assembly for easy access to the disc pack area. Referring to Figure 3-77, four rollers attached to the door ride on two rails along the shroud cover. Pushing against the cover bar causes the door to slide rearward, (door can not be opened until "DOOR LOCKED" light is off) under the logic file. With the door in its rearward position, the space within the shroud for installing or removing a disc pack is unrestricted by the presence of hardware.

The door switch (Figure 3-77) detects the open or closed condition of the door. If open, starting the drive motor is not possible, and the door locked indicator will not be lit on the drive's operator panel. A solenoid-actuated door lock mechanism locks the door closed while the pack is rotating. Locking the door closed is a safety measure which guards against accidental/inappropriate opening of the door when the drive is being operated. If the door is opened while the drive is operating, the heads are automatically retracted and pack rotation is automatically braked to a complete stop.

### 3.7.3 Air Seal

The smoke glass door, in addition to offering visual inspection of the pack and heads while closed, provides for an air seal which protects the entire shroud area from contaminants. This protection is extremely important because the heads rely on a thin air bearing to maintain a 45 or 50 microinch (depending on head and drive type) clearance between each head and its disc surface. Introduction of foreign material into the air bearing can affect the head flying capability, resulting in the worst case in head-to-disc interference (HDI). Recognition of and recovery from HDI are discussed in Section 4, MAINTENANCE.

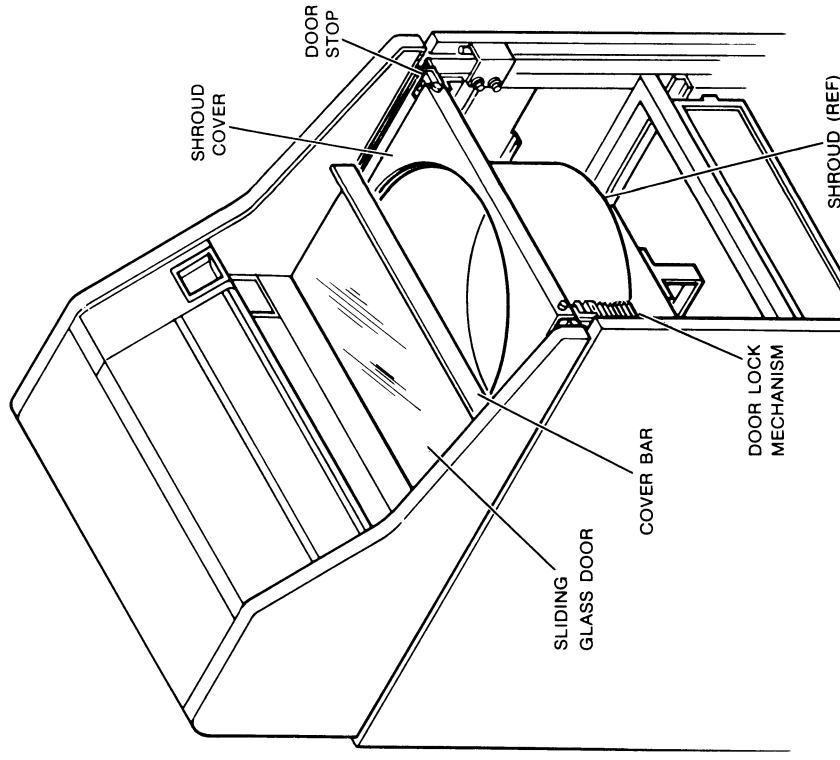


FIGURE 3-77. PACK ACCESS DOOR ASSEMBLY



### 3.8 AIRFLOW AND FILTRATION SYSTEM

#### 3.8.1 System Description

The Airflow and Filtration System is used to create and maintain a controlled environment inside the drive cabinet. Having this environmental control, supplying cooled/filtered air to the drive from external sources is not required — and drive reliability and performance are independent of the computer room environment provided normal room temperature and humidity (Table 1-1) exists.

Air is filtered to remove contaminants, and moved within the cabinet in fixed paths which traverse parts that operate with known sensitivities to local temperature and humidity. Such parts include the disc pack and, referring to Figure 3-79, the power supply, servo power amplifier assembly, logic file, and linear (positioning) motor.

Referring to Figure 3-79, air from the computer room enters the cabinet above the power distribution unit, and convection cools components in the ac box. Air entering through the bottom of the power supply is unfiltered, and circulated to cool components in the power supply and servo power amplifier (mainly rectifiers and heat sinks). One additional fan at rear cools the heat sink asm in PS. As shown by the arrows, air that is allowed to enter the shroud must pass through the 0.3-micron absolute filter. This filtered air passes through the air duct and enters the shroud to cool the disc pack, and leaves the shroud through the baffle opening to cool the linear motor, and is moved by a unitized assembly of three muffin fans into the logic file. The circulated, filtered air leaves the cabinet through the rear.

A plexiglass air deflector (not shown in Figure 3-79) sits atop the deck plate over the linear motor. It guides air exhausted out of the baffle opening over the carriage way to remove any foreign particles, before reaching the linear motor. The deflector slides to the rear to allow access to the heads.

As indicated above, air is circulated around the shroud and deck plate areas without the use of fans. This air circulation is accomplished as described in the following paragraph.

To make the air seal, compressive foam is used and the glass door rails are detented. Referring to Figure 3-78, as the door is pulled forward a cam action positions the door up and onto the railings for sliding on rollers to the closed position. As the door is fully closed, a cam action positions the door down onto compressive foam for sealing the shroud from contaminated air. As the door is pushed toward the rear, a cam action raises the door up slightly to break the air seal by allowing the foam to expand. When the door is pushed all the way to the rear, a cam action positions the door down as a positive indication for the operator that the door is fully opened.

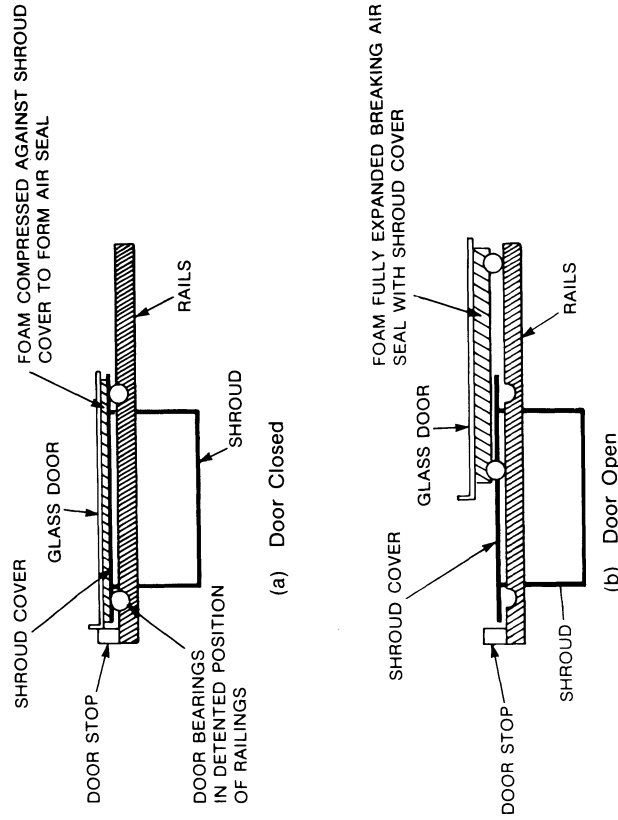


FIGURE 3-78. OPERATION OF DOOR AIR SEAL

### 3.8.2 Mechanism for Upper Air Circulation

To remove foreign particles from the disc pack and carriage way, and to cool the linear motor, the system uses the pumping characteristic of a rotating disc pack instead of fans. A rotating pack acts as a fan, and when rotating in a closed environment an exhaust opening creates a low pressure zone immediately following it. This aerodynamic lift characteristic is used to open the comb-like device called the baffle (Figure 3-79). The baffle's spring tension is designed to allow opening just before the pack reaches 3600 rpm, at the pre-designated speed called Upspeed. When opened, a switch is activated to indicate Upspeed and cooling air is allowed to pass out of the shroud. The same low pressure zone draws the filtered air into the shroud from the air duct.

## 3.9 POWER SYSTEM

### 3.9.1 System Description

The Power System is used for distributing filtered ac power, providing regulated dc voltages, and controlling the drive motor. It consists of the ac Power Distribution Unit (PDU) and the dc Power Supply. The motor control circuitry is contained in the PDU.

The three functions of the Power System (indicated above) are discussed in the following paragraphs.

#### NOTE

Since power up/down sequencing is the joint function of the drive and DCL — and is enabled or disabled by control units attached to the DCL, sequencing is performed pursuant to specifications negotiated with the customer. These specifications, and the conditions for powering up and down, are described in paragraph 1.3.1.4.

### 3.9.2 Power Distribution Unit

The PDU, located at the front of the drive on the cabinet floor, receives wall power and accomplishes three-phase filtering at its input and certain points of distribution. The ac to the dc Power Supply, power supply fan, and drive motor is filtered twice. The ac to the logic fans and the DCL (its dc power supply) is filtered once. The drive's main circuit breaker and power conversion plug are provided before load distribution to either DCL or drive components.

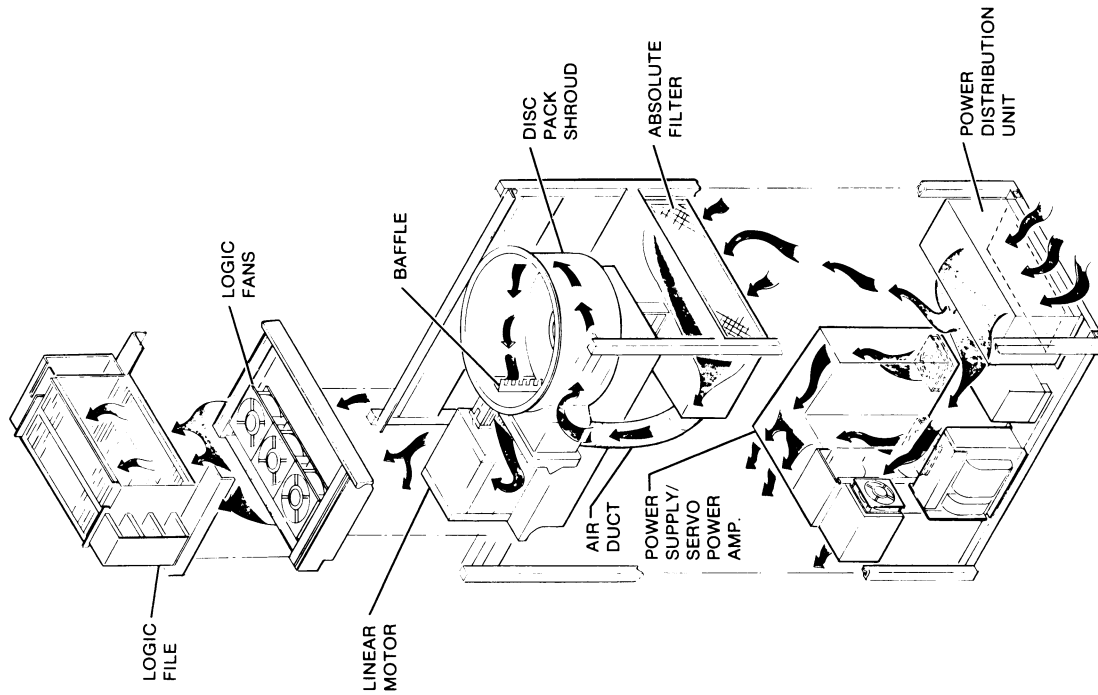


FIGURE 3-79. AIRFLOW AND FILTRATION SYSTEM

Since the PDU is the interface for power between DCL and the drive, its physical and electrical configuration depends on DCL (customer) interface specifications, and these are addressed in Section 1. The PDU is described in paragraph 1.3.1.7. Grounding is described in paragraph 1.3.1.8.

### 3.9.3 Power Supply

The Power Supply, located on the cabinet floor near the PDU, contains dc bulk voltage circuitry and voltage regulators, and produces the voltages used by PCBs, cover on and door closed switch, motor control circuits, and the servo power amplifier.

- Referring to Figure 3-80, twice filtered ac power is sent to the power supply Transformer.
- Power from the Transformer is sent to the 50 V Rectifier and Filter, then through circuit protectors (fuses and circuit breakers) to Terminal Board TB304, and supplied to the Servo Power Amplifier (SAMP) and Motor Control circuits. The 50 V loads supplied are +50 V BRAKE, +50 V SERVO, +50 V EMERGENCY RETRACT, and +50 V WRITE. When the pack access door is detected as not fully closed, Cover Interlock removes the servo voltage before all other dc voltages are removed.

- Power from the Transformer is sent to the Rectifiers and Filters, then to voltage regulators. Their outputs are received by Terminal Board TB500, and supplied to PCBs in the Logic File. All PCBs in the Logic File receive -15 V, +5 V, and -15 V; only the Operator Control and Index PCBs receive +24 V. The three regulated voltages are also supplied to the Head Alignment Unit/File Interface, and the +24 V is also supplied to Motor Control circuits and the Cover On and Door Closed Switch.

Each PCB in the Logic File receives the three regulated voltages as follows:

- 15 V at pin R25
- + 5 V at pins R1 and R40
- +15 V at pin R16.

#### 3.9.3.1 Performance Requirements

DC power requirements are presented below.

- **Power Outputs.** Outputs from the Power Supply, when fully loaded by the drive electronics, are as follows:

Nominal Voltage	TB Location	± Tolerance	P-P Ripple
- 5.2 V	TB500-3	208 mv	25 mv
+ 5 V	TB500-2	100 mv	25 mv
-15 V	TB500-9	150 mv	30 mv
+15 V	TB500-5	150 mv	30 mv
+24 V	TB500-12	4.8 V	2 V
+50 V	TB304-5	5 V	N/A

- **Noise.** When measured at the 5 V supply line on the logic file, total noise generated with the servo operating is 125 mv p-p or less.
- **DC Failure Indication.** CLEAR being false (at D04-R29) indicates no unsafe voltage exists. CLEAR is true if one or more of the following conditions is satisfied:
  - DC power is on for  $1 \pm 0.5$  seconds.
  - Any one of the following conditions exists for 500  $\mu$ sec or longer:
    - +24 V is less than 10 V.
    - +15 V is not within  $+15 \pm 1.65$  V.
    - + 5 V is not within  $+5 \pm 0.55$  V.
    - 5.2 V is not within  $-5.2 \pm 0.57$  V.
    - 15 V is not within  $-15 \pm 1.65$  V.

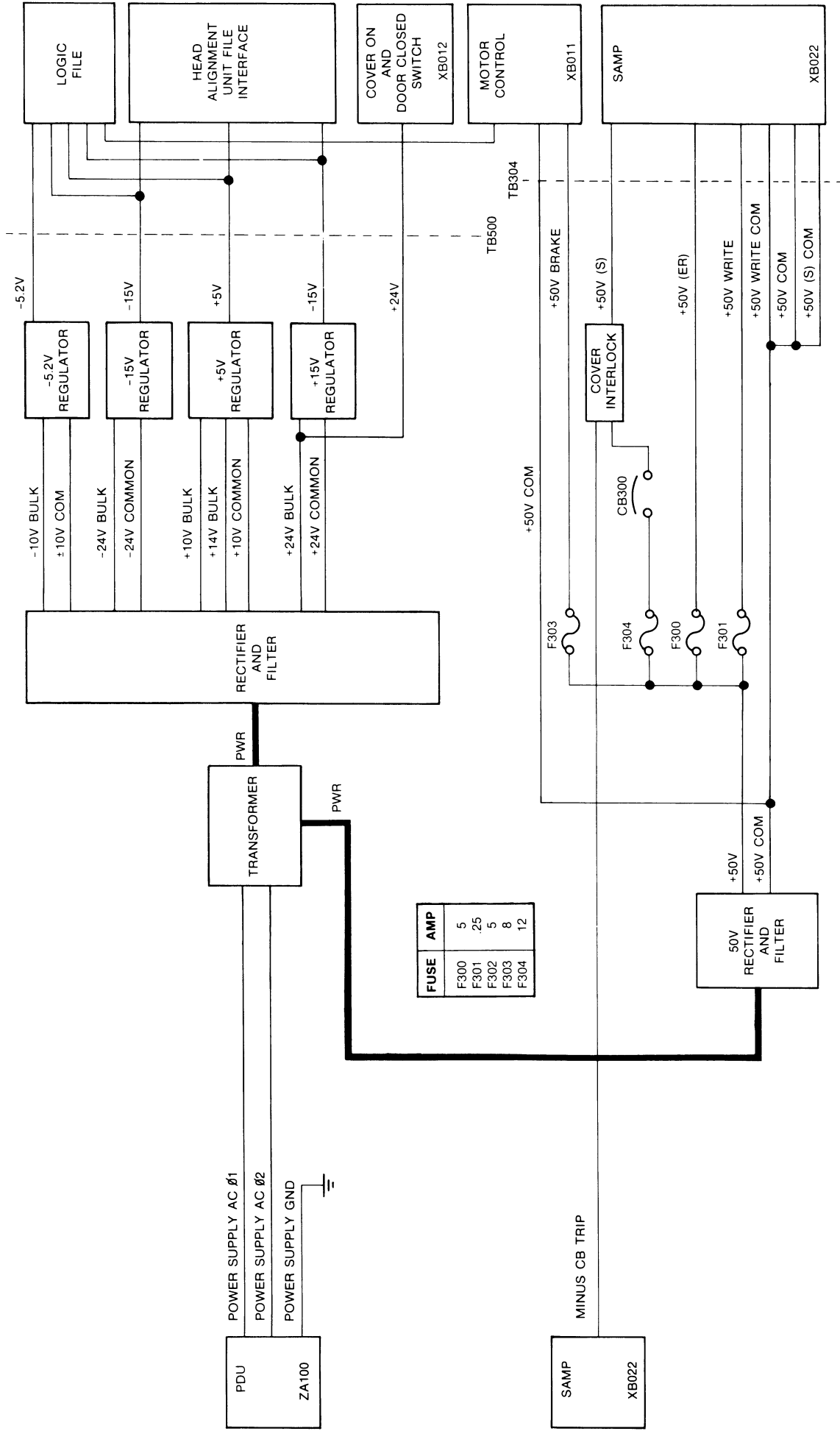


FIGURE 3-80. DC BULK VOLTAGES, VOLTAGE REGULATORS, AND SERVO VOLTAGES

## SECTION 4 MAINTENANCE

### 4.1 INTRODUCTION

This section contains procedures for scheduled and unscheduled maintenance of RP05 DEC and RP06 DEC Disc Storage Drives. The maintenance procedures also include troubleshooting recommendations. Recommended safety practices are included in this section.

Service personnel should become familiar with the special tools that are used (paragraph 4.3), and the basics of offline tester operation (paragraph 4.4).

Scheduled maintenance procedures are condensed for presentation (in paragraph 4.5) as a single standalone flowchart which recognizes the involvement of drives with the rest of the system.

Unscheduled maintenance procedures are presented (in paragraph 4.6) in step-by-step format. The procedures contain detailed instructions for inspection, adjustment, alignment, or replacement of drive parts. Fault isolation to a particular part determines the point of entry into the unscheduled maintenance procedures.

#### NOTE

Applicable field service notes or suggestions are included in the maintenance procedures. Field feedback is considered an important source for improvements to the procedures. FEs are urged to submit comments/suggestions to the Memorex Publications Department.

### 4.2 SAFETY PRACTICES AND GENERAL PRECAUTIONS

#### 4.2.1 Personnel Safety

The following safety precautions are recommended for all personnel involved in maintenance of RP05/6 drives.

1. Working alone is not recommended. Advise your manager if you **MUST** work alone.

2. Remove all ac and dc power before removing or assembling major components, working near the power supply, or installing changes in machine circuitry.
3. When the wall box power switch is turned off to perform maintenance, it should be locked or tagged. If possible, pull the power cable from the ac outlet.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, the following precautions must be taken:
  - a. Another person familiar with power-off controls must be in the immediate vicinity.
  - b. Avoid/wearing loose clothing that may be caught in machinery.
  - c. Rings, wrist watches, chains, bracelets, metal cuff links, etc., should not be worn.
  - d. Only insulated pliers and screwdrivers are approved for use.
  - e. When using test instruments, be sure controls are set correctly, and proper-capacity insulated probes are used.
5. Wear safety glasses when using a hammer, power tools, spring hooks or springs, chemicals, sprays, solvents, etc.—and when soldering.
6. Special safety instructions in the maintenance procedures **must** be followed.
7. Avoid touching moving mechanical parts.
8. Before starting equipment, ensure all personnel are clear of the drive.
9. The linear motor has a powerful magnetic field. Exercise care when using tools near the motor.
10. Be aware of the fire protection system and procedures.

## 4.2.2 Equipment Safety

The following general precautions should be observed.

1. The pack access door is glass; it must be handled with care.
2. Do not place a heavy object such as a disc pack on the pack access door.
3. Power (dc) must be off for PCB replacement.
4. The tachometer rod is ceramic, and therefore breakable; handle carefully.
5. Care must be used when handling read/write and servo head assemblies. No attempt should be made to install a spare head assembly that has been improperly packaged, or which may have been damaged in shipment. Do not attempt to straighten bent head flexures.
6. The heads must remain on the unload cams (retracted) unless the head separator tool is installed. Failure to observe this caution will result in damage to the heads.
7. Completely remove all shipping brackets and material before applying power to the drive.
8. Screws and other hardware, which might be dropped into the drive during maintenance, should be located and removed immediately.
9. Do not use solvents, chemicals, greases, or oils that have not been approved by Memorex.

10. Any cracked or broken disc pack cover should be replaced.
11. Exercise care when installing a pack in a drive. Improper installation could scar the spindle hub or pack drum, which may result in misregistration of the disc pack with respect to the read/write heads.
12. Never leave the pack access door open unnecessarily. The longer it is open, the greater the susceptibility of contamination. Tobacco smoke and ashes create serious contamination problems.
13. "Kimwipes" (trademark of Kimberly-Clark Corporation) are the only approved disposable wipers to be used.
14. Don't use excessive force on self-tapping screws.

## 4.2.3 Housekeeping

After performing maintenance, the equipment should be restored to like-new appearance. All covers removed must be in place and the outside of the equipment cleaned as follows:

1. Using a Kimwipe sprayed with Windex, remove fingerprints and smudges from the pack access door and operator panel. Do not spray directly on equipment.
2. Clean covers and panels with a damp rag.
3. Clean pack access door tracks with a small brush.
4. If dust or foreign material is visible in the shroud area, clean shroud with a Kimwipe dampened with alcohol.

### 4.3 SPECIAL TOOLS

Special tools used in drive maintenance procedures are listed below.

	<b>MRX P/N</b>
• Head Alignment Kit	215970
• Head Cleaning Kit	202159
• Mechanical Alignment Kit	215971
• CE Pack (200 MB)	335001
• PCB Extender	011086
• Absolute Filter Gauge	211663

Regarding the tools listed above, and available tools which are not listed above, note the following:

1. Head Alignment Kit contains the following tools:

	<b>MRX P/N</b>
• Head Alignment Unit	211292
• Head Alignment Tool	211526
• Head Installation Tool	210105
• Head Torque Tool	210109
• Replacement Shaft, Head Torque Tool	211516

If the 800 Disc Storage Subsystem Tester is available, the Head Alignment Unit listed above is not required, providing the P/N of tester is 215935. This P/N of tester includes all functions of the Head Alignment Unit. Therefore, this P/N of tester plus the four tools listed above can be substituted for the Head Alignment Kit.

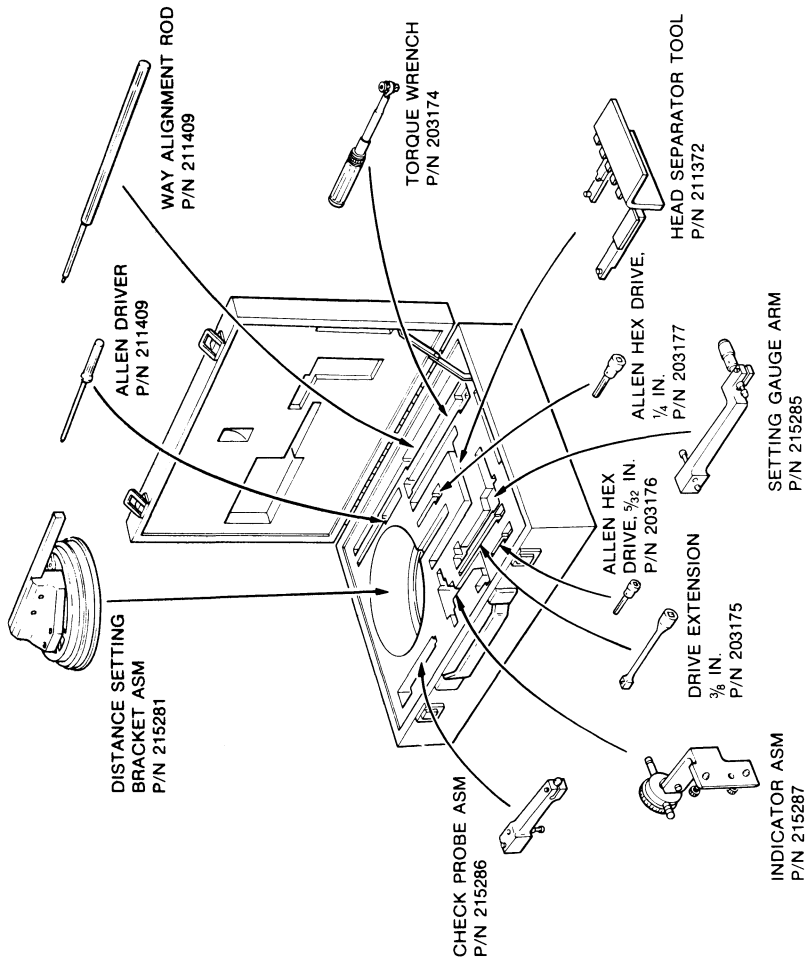
2. Tester P/N 215900 does not provide a head alignment capability.
3. When replacing the drive motor, some strength on the part of the FE is required to avoid dropping the heavy motor as it is released at arm's length and withdrawn from the cabinet. To aid the FE in this maintenance activity, a tool to simplify drive motor replacement is shown in Figure 4-14, and its use is described in paragraph 4.6.6.1.
4. All items in the Head Cleaning Kit are not "special tools"—sources of these items, other than Memorex, may be available. This kit contains Memorex-approved disposable wipers ("Kimwipes"), 90% solution of isopropyl alcohol, a small brush, and a head paddle—the latter of which is like a plastic tongue depressor.

#### **NOTE**

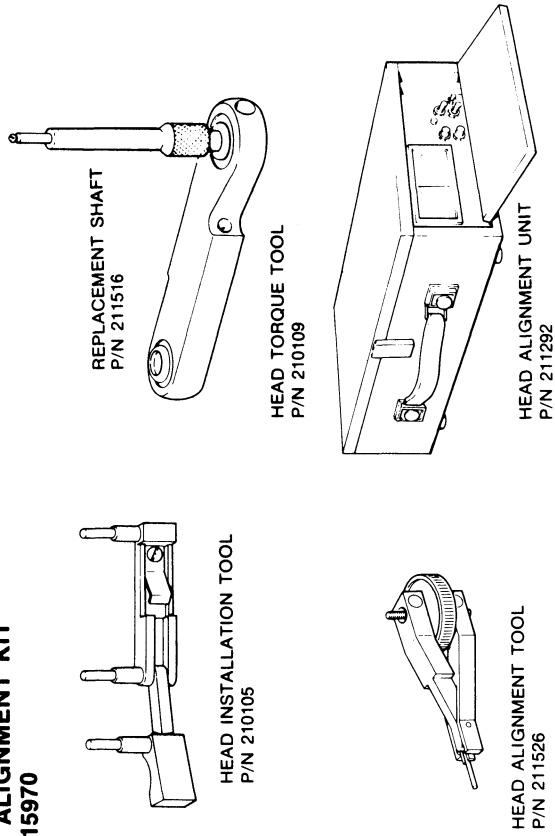
The head paddle must not be wood. Isopropyl alcohol can cause wood to leave deposits.

Figure 4-1 illustrates many of the special tools available.

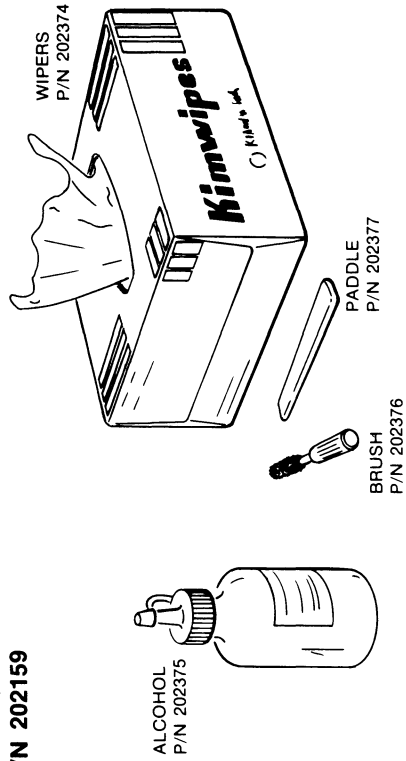
**MECHANICAL ALIGNMENT KIT  
P/N 215971**



**HEAD ALIGNMENT KIT  
P/N 215970**



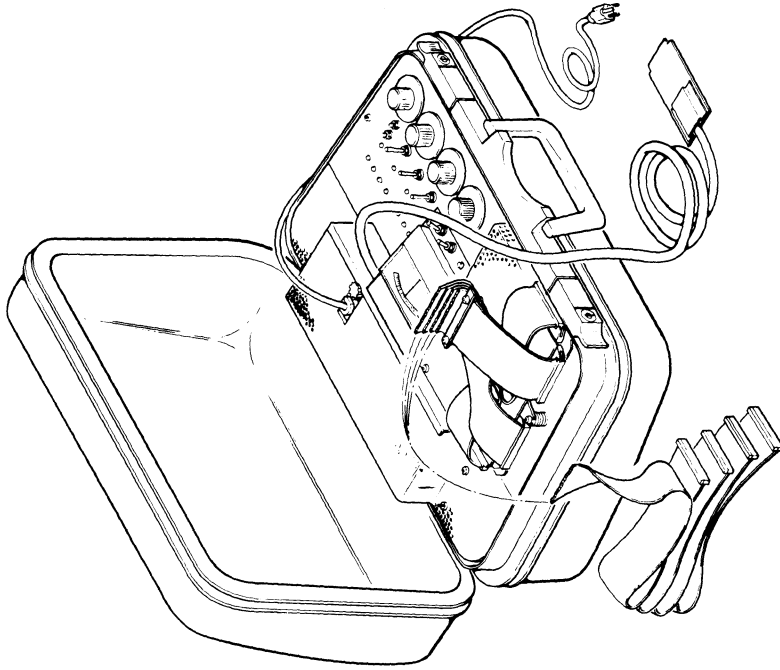
**HEAD CLEANING KIT  
P/N 202159**



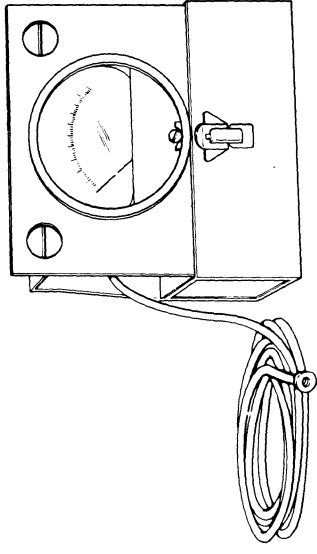
**FIGURE 4-1. SPECIAL TOOLS (Part 1 of 2)**



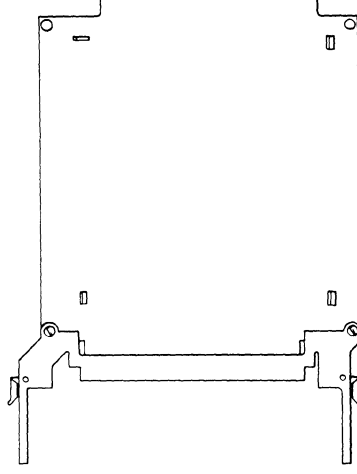
**800 DISC STORAGE SUBSYSTEM TESTER**  
P/N 215900 STANDARD MODEL, OR  
P/N 215935 STANDARD MODEL WITH HEAD ALIGNMENT (SHOWN)



**ABSOLUTE FILTER GAUGE**  
P/N 211663



**PCB EXTENDER**  
P/N 011086



**FIGURE 4-1. SPECIAL TOOLS (Part 2 of 2)**

#### 4.4 TESTER HOOKUP, ROUTINES, AND RUN OPTIONS

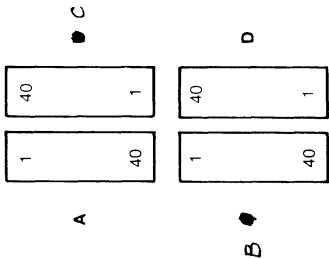
Once the FE becomes familiar with the 800 Disc Storage Subsystem Tester, a list of routine numbers and run options and a condensed installation procedure will probably be the only documentation needed to use the tester. This information is contained in Tables 4-1 and 4-2.

TABLE 4-1. TESTER HOOKUP

1. Connect tester to 115 Vac 50/60 Hz wall power and run Wrap Test for tester checkout. Proceed to steps below if no error occurs.
2. Turn off ac power to the drive.
3. Disconnect the drive from DCL I/O cables A,B,C,D.
4. Connect tester I/O cables A,B,C,D to the drive.
5. Connect tester's head alignment cable to the drive in slot B04 if head alignment is to be done.
6. Connect the drive to ac wall power and set all ac/dc circuit breakers to ON. STANDBY display in drive should be illuminated.
7. Toggle RESET in tester; all LED displays should illuminate. Release RESET; all displays should go off.
8. Press the drive's START switch once.

**NOTE:** See the Appendix B for tester operating procedures.

#### CONNECTOR PIN INFORMATION



PADDLE BOARDS				PCB POSITION														
A01	A02	A03	A04	D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	D13	D14	D
				IPUT	OPUT	PRCO	INDX	VFO	NOT USED	NOT USED	NOT USED	NOT USED	SEQU	SVTL	NOT USED	NOT USED	VSER	
B01	B02	B3	B04															
COVER ON AND DOOR CLOSED SW	SERVO POWER AMP	HEAD ALIGN																
C01	C02	C03	C04															
				PCB COMPLEMENT LOGIC GATE														

TABLE 4-2. TESTER ROUTINE NUMBERS AND RUN OPTIONS

Test	Run Time (sec)*	Routine	Error Control/Run Options	Test	Run Time (sec)*	Routine	Error Control/Run Options
Wrap	<1	00	01 = Loop on pass. 02 = Loop on error.	Read Continuously (Errors Monitored)	~20 min.	0A	01 = Read 65,535 times and stop (default). 02 = Loop on error.
Incremental Seek	<1	01	01 = Run continuously and stop on error (default). 02 = Loop on error.	Read/Write Safety	<1	0B	00 = Check latches once (no link). 02 = Loop on error. 80 = Check latches once and link (default).
Alternate Seek	<1	02	01 = Alternate seek; stop on error. 02 = Loop on error.	Offset	<1	0D	00 = Run once and stop (no link). 01 = Run continuously and stop on error. 02 = Loop on error. 80 = Run once and link (default).
Random Seek	<1	03	01 = Run continuously and stop on error (default). 02 = Loop on error.	Index	<1	10	00 = Run once (no link). 01 = Run continuously and stop on error. 02 = Loop on error. 80 = Run once and link (default).
Tachometer Gain Adjustment	<1	04	00 = Verify tach gain (no link). 01 = Adjustment mode. 02 = Loop on error. 80 = Verify tach gain and link (default).				
Head Alignment	<1	05	01 = Run continuously and stop on error (default). 02 = Loop on error.				
Head Alignment Verification	~10	06	00 = Verify mode (default). 02 = Loop on error.	Display Drive Output Byte	<1	11	00 = Display one drive output byte, byte number 00 (default).
Head Alignment Track Seek	<1	07	00 = Run once and stop (default)	Recalibrate	<1	12	00 = Run once (default). 02 = Loop on error.
Write/Read Verification	<2	08	00 = Write all heads of cylinder and stop (default). 02 = Loop on error.	Write	<1	13	00 = Write all heads of cylinder and stop. 01 = Write continuously and stop on error. 02 = Loop on error.
Incremental Offset Read	<2	09	00 = Read once and stop (default). 01 = Read continuously and stop on error. 02 = Loop on error.				

**NOTE**

ERROR CODE DICTIONARIES AND FLOWCHARTS FOR TESTER ROUTINES ARE CONTAINED IN APPENDIX B.

\*Time required for one loop through the routine.

## 4.5 SCHEDULED MAINTENANCE

A flowchart containing drive scheduled maintenance requirements is presented in Figure 4-2. Special tools needed to perform the scheduled maintenance activities are discussed in paragraph 4.3.

To align the heads, you need an offline tester having the head alignment option (P/N 215935) **PLUS** four head alignment tools (P/Ns 210105, 210109, 211516, 211526), **OR** a Head Alignment Kit (P/N 215970). In other words, the tools come with the kit, but not with the tester.

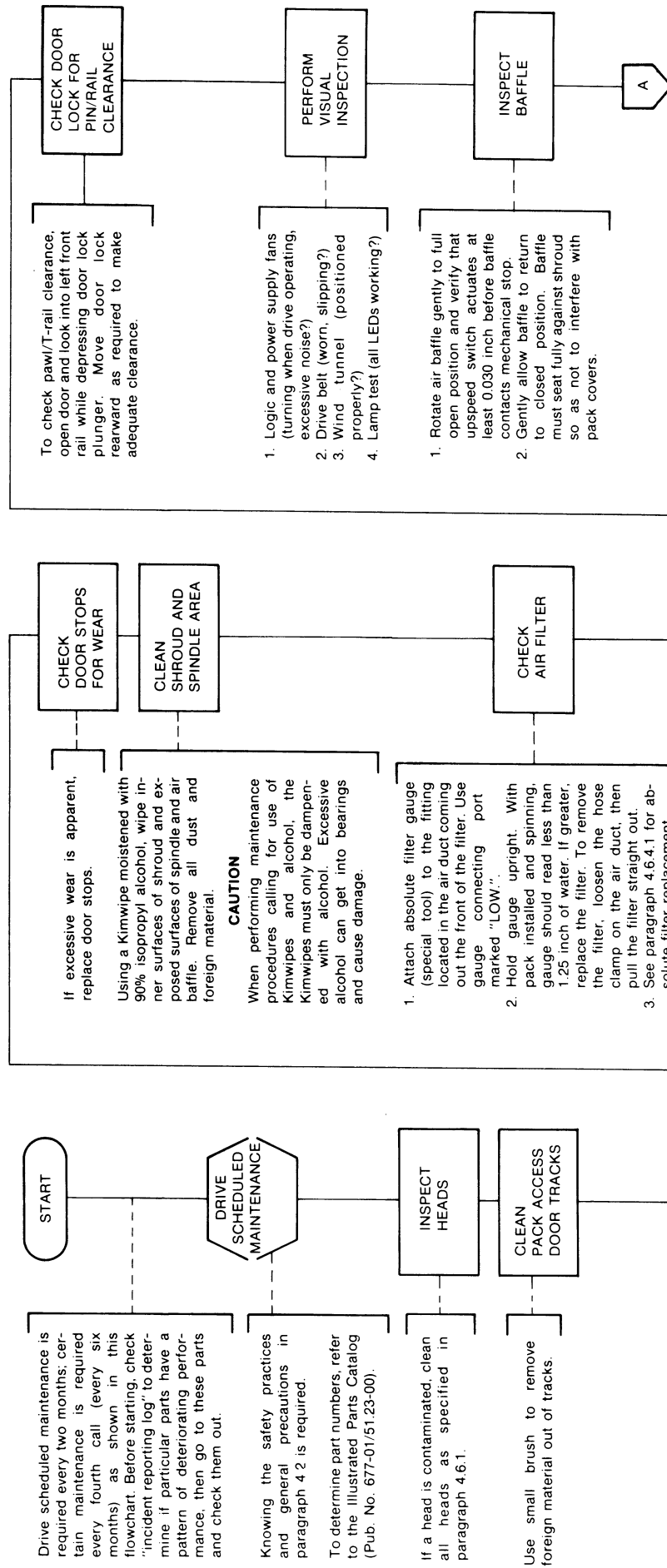


FIGURE 4-2. SCHEDULED MAINTENANCE FLOWCHART (PART 1 of 2)

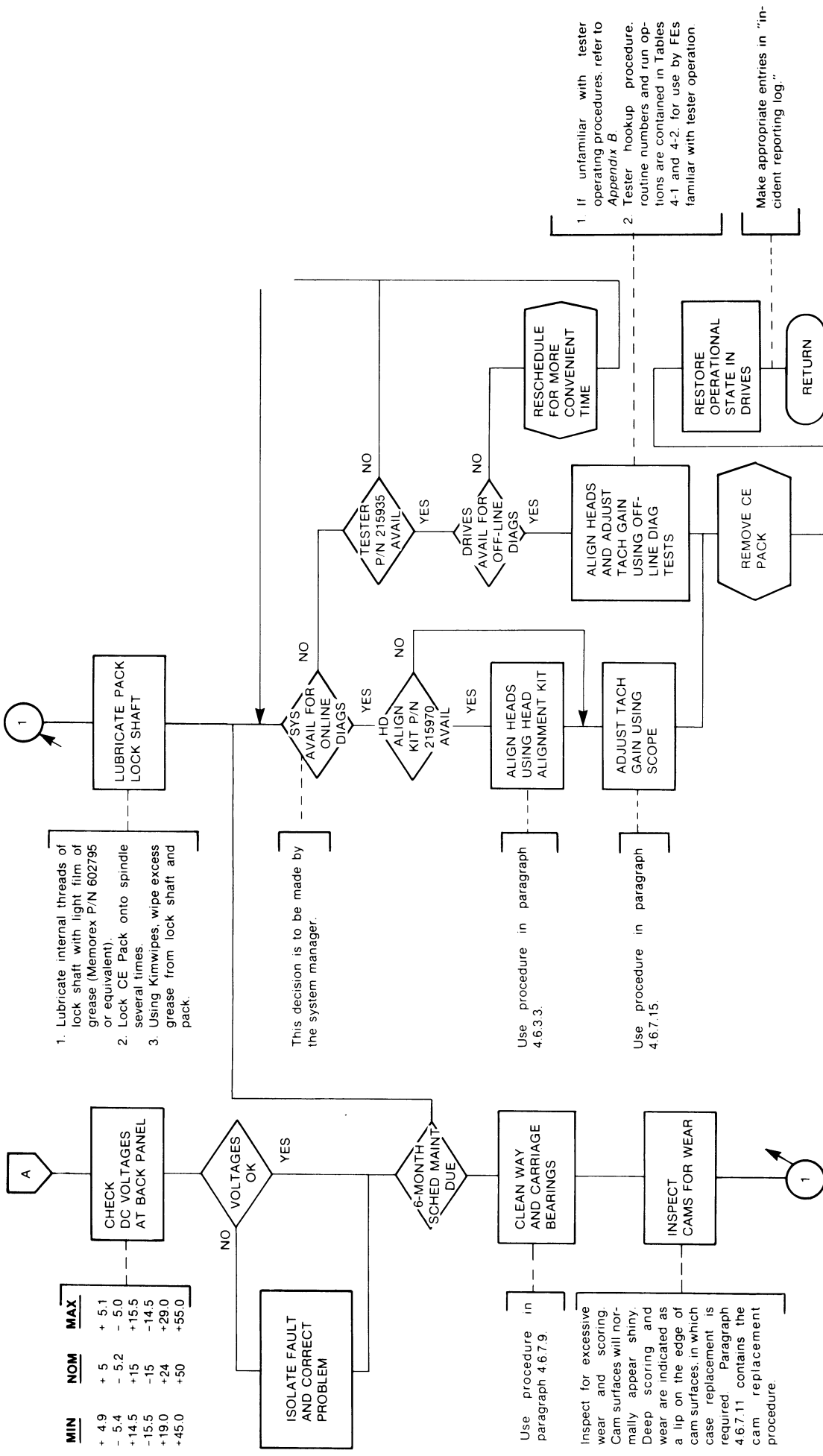


FIGURE 4-2. SCHEDULED MAINTENANCE FLOWCHART (PART 2 of 2)

## 4.6 UNSCHEDULED MAINTENANCE

Parts inspection, alignment, adjustment, and replacement procedures are presented in the paragraphs which follow. Table 4-3 can be used to locate a procedure in a minimum of time.

### NOTE

**NO** potentiometer, other than tach gain, may be adjusted.

Applicability and scope of the unscheduled maintenance procedures are discussed below:

- All procedures make the necessary distinctions between the RP06 and RP05 DEC drives. If same-name parts in the two drives are maintained identically, a common maintenance procedure is presented even though the parts may be different (examples: drive motor and heads). If the part differences are visible, they are illustrated.
- Although the disc pack is not a part of the drive, maintenance of the pack is covered with respect to recognition and prevention of head-to-disc interference (HDI), and recovery from HDI.

### NOTE

A disc pack mounted on a drive when HDI is experienced must be returned to the pack manufacturer for inspection, cleaning, and repair.

- Parts having obvious maintenance procedures are not covered (examples: replacing PCBs, door stops, entire power supply, or entire power distribution unit).

Fault Isolation Procedures for drive sequencing and servo failures are contained in Appendix A.

**TABLE 4-3. HARDWARE VERSUS APPLICABLE PARAGRAPH**

Amplifier, Servo Power	4.6.8.5
Baffle, Air	4.6.4.3
Belt, Pack Drive	4.6.6.3 - 4.6.6.4
Bobbin, Linear Motor	4.6.7.4
Cable, R/W Preamp	4.6.8.7
Carriage T-Block Assembly	4.6.7.6 - 4.6.7.10
Cams, Head Unload	4.6.7.11
Cam Tower	4.6.7.12
Control Panel, Operator	4.6.8.1
Door, Pack Access	4.6.5.1
Fan, Logic	4.6.4.2
Filter, Absolute	4.6.4.1
Heads	4.6.1 - 4.6.3
Motor Assembly, Drive	4.6.6.2
Motor, Linear	4.6.7.2 - 4.6.7.3
PCB, Lamp Matrix	4.6.8.2
PCB, Logic Asm Motherboard	4.6.8.3
Preamp, R/W	4.6.8.4
Preamp, Servo	4.6.8.6
Sensor, Pack Cover	4.6.6.7
Shroud	4.6.5.2
Spindle Assembly	4.6.6.6
Spindle Lock Shaft	4.6.6.5, 4.6.6.8
Switch, Heads Retracted	4.6.7.5
Switch, Upspeed	4.6.4.4 - 4.6.4.5
Tachometer	4.6.7.13 - 4.6.7.15
Way, Carriage	4.6.7.8 - 4.6.7.10

**4.6.1.2 Cleaning and Handling Precautions**

1. Never extend the heads unless the Head Separator Tool is installed.
2. Use only the Memorex-approved disposable wipers (Kimwipes) to clean and dry sliders. Wipers are contained in the Head Cleaning Kit.
3. Do not touch face of slider with fingers. Skin oil causes contamination.
4. Do not blow breath on sliders or discs. Moisture causes contamination.
5. Install a slider only after cleaning and inspection.
6. Do not allow alcohol to dry by evaporation on slider surface. Alcohol residue causes contamination.
7. Use only the paddle supplied in the Head Cleaning Kit. Wood or plastic substitutes can react with the alcohol to leave contaminants.

**4.6.1.3 Inspecting Heads**

1. Check the air bearing surfaces of all sliders for contamination and scratches. Contamination can be the presence of slight oxide streaks on the bearing surfaces, oxide buildup around the periphery, or excessive accumulation of oxide or other foreign material in the relief slot or R/W core area. Ignore any discoloration of the ceramic slider or small pits in the ceramic surface.
2. Clean only those sliders that show signs of contamination. The cleaning procedure to use is given below.

3. Replace any slider having scratches or dark brown/black streaks (burned oxide or aluminum) on the bearing surface. Such scratches or streaks indicate damage by HDI. The procedure to use is given on the next page.

**4.6.1.4 Cleaning Heads in Machine**

1. Power down and remove the pack.
2. Wrap a Kimwipe tissue around the head paddle (all of it) and dampen one end with alcohol (do not soak). The particular kind of tissues to use, the paddle, and alcohol solution are in the Head Cleaning Kit.

**4.6.1 Head Inspection and Cleaning**

**4.6.1.1 Tools Required**

Special tools required are the Head Separator Tool (P/N 211372) and Head Cleaning Kit (P/N 202159). To clean the heads while installed in the machine, a head inspection mirror (like a dental mirror) is also required to make a final check for contamination after cleaning. This mirror is OEM-supplied (not a Memorex special tool).

3. Referring to Figure 4-3, wipe bearing surface of each slider thoroughly with dampened end of Kimwipe (on paddle). Use **only** sufficient pressure against the slider to clean it and then dry it. Excessive pressure **will** damage the slider pitch and roll attitude adjustments.

4. Push paddle further into assembly to dry the head surface. Remove paddle by pushing it toward center of carriage until it is clear of the slider, and then pull it out. Don't let the dampened portion of the Kimwipe touch the cleaned portion of the slider.

5. Using a head inspection mirror, inspect each slider for contamination. Any head with contamination or cleaning residue which cannot be removed **must** be replaced. Remember that discoloration of the ceramic slider is **not** contamination.

6. Inspect gimbal flexures and arm assemblies for damage and loose pieces of tissue.

7. Remove any loose tissue and replace any defective assemblies.



FIGURE 4-3. CLEANING HEADS IN DRIVE

#### 4.6.1.5 Cleaning Heads Out of Machine

##### NOTE

Refer to paragraph 4.6.2.2 for head removal.

1. Wrap a Kimwipe tissue around the head paddle (all of it) and dampen one end with alcohol (do not soak). The particular kind of tissues to use, the paddle, and alcohol solution are in the Head Cleaning Kit.

2. Gently scrub slider bearing surface with wetted end, paying special attention to leading and trailing edges and the relief slot. Figure 4-4 shows how to hold and clean the slider. Use **only** sufficient pressure against the slider to clean it and then dry it. Excessive pressure **will** damage the slider pitch and roll attitude adjustments.



FIGURE 4-4. CLEANING HEADS OUT OF DRIVE



## 4.6.2 Head Replacement

### 4.6.2.1 Tools Required

Tools required are the Head Installation Tool (P/N 210105), Head Torque Tool (P/N 210109), and Torque Tool Shaft (P/N 211526).

Torque Tool Shaft has a press-fitted Allen tip. The shaft slides into the opening at either end of the torque tool itself, one end of which is calibrated to provide an INITIAL torque and the other end a FINAL torque. The words INITIAL and FINAL are etched onto the tool itself.

### 4.6.2.2 Removing a Head

1. Remove pack.
2. Slide logic gate forward by releasing both latches at the rear of the gate and pushing with equal force on each side (don't twist the gate as it slides).
3. Release the leaf-spring latch on the bottom right side of the wind tunnel, and slide the wind tunnel to the rear.

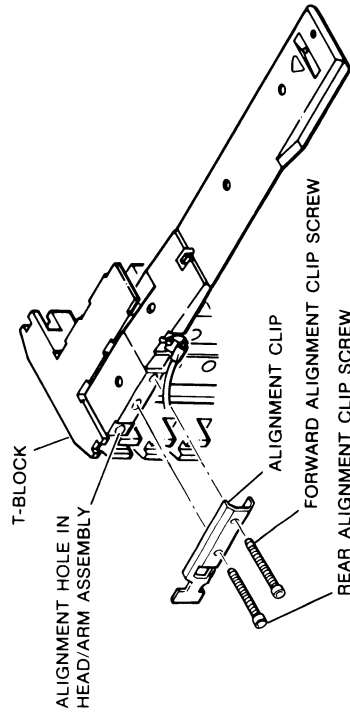


FIGURE 4-5. HEAD ALIGNMENT CLIP AND SCREWS

4. Remove the clamps on each side of cam tower that hold the head plugs in place by pressing down on the leaf spring at the top and pulling back.
5. Disconnect head plug.
6. Referring to Figure 4-5, remove the two alignment clip screws and the alignment clip which hold the head assembly in the T-block slot.
7. Determine whether the head is an 'A' or 'B' type head by referring to Figure 4-6.
8. Grip head assembly with Head Installation Tool, as indicated in Figure 4-7 ('A' type head) or Figure 4-8 ('B' type head).
9. Close jaws of installation tool completely and remove head assembly from drive. Do not touch the slider face or press against the flexure (see Figure 4-8). Even slight pressure against the flexure could bend it; excessive pressure will damage the head's pitch and roll attitude adjustments.

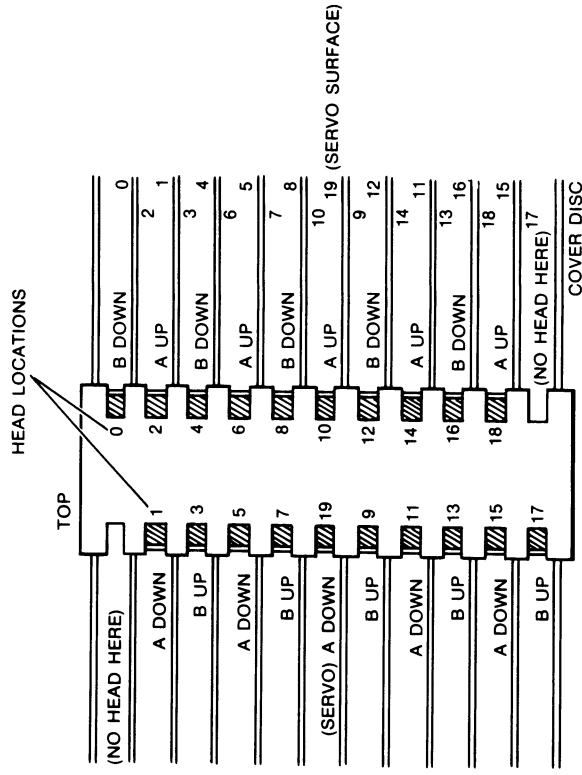


FIGURE 4-6. T-BLOCK, VIEWED FROM LINEAR MOTOR

#### 4.6.2.3 Installing a Head

1. Remove the alignment clip screws and the alignment clip from the head assembly being installed.

#### NOTES

- **UPPER LEFT AND LOWER RIGHT SLOTS DO NOT RECEIVE HEADS.** (Refer to Figure 4-6.)
  - Replacement head assemblies supplied to DEC contain alignment hardware (alignment clip and screws).
2. After reading the notes below, install the head into the drive.
    - a. The head's serial number is engraved on the head assembly. A prefix "M" denotes a 200 MB head.
    - b. An 'A' or 'B' type head assembly must be installed into an appropriate position, noting whether it is "up" or "down" (see Figure 4-6). This information is engraved on the head assembly.
    - c. A head assembly must be installed into its rearmost position in the T-block slot.
    - d. To hold a head assembly, grip it with the Head Installation Tool as indicated in Figure 4-7 ('A' type head) or Figure 4-8 ('B' type head).

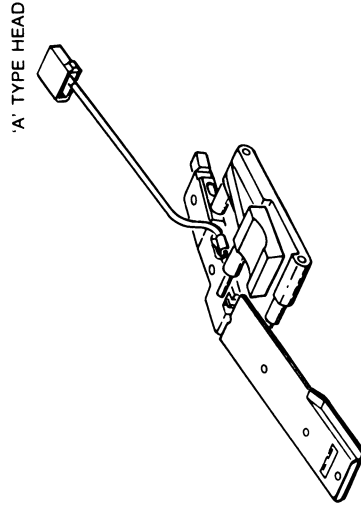


FIGURE 4-7. HEAD INSTALLATION TOOL IN 'A' TYPE HEAD

- e. To place a head assembly into the drive, close jaws of installation tool completely and insert into rearmost position in T-block slot. Don't pinch the pigtail wire with the tool. Do not touch the slider face or press against the flexure. Even slight pressure against the flexure could bend it; excessive pressure will change its setting.

- f. Before torquing the screws (see Figure 4-9), check to see that the arm is resting properly on the cam surface and that the flexure has not been bent during head installation. This can most easily be observed from the front of the machine.
  - g. When installing several head assemblies, both screws should be torqued to INITIAL torque using the Head Torque Tool. (Servo head is always torqued to FINAL torque.) Begin at the bottom of the T-block and proceed to the top, one side at a time, leaving all head plugs disconnected. Be sure to install servo head screws guard after FINAL torque; failure to do so may prevent proper alignment of the read/write head assemblies.
3. With all alignment screws torqued to INITIAL torque, except servo which is torqued at FINAL torque, connect read/write head plugs to matrix PCBs. Connect servo head plug to matrix PCB and servo preamp.
  4. Replace the head plug clamps, being sure that the tabs on the leaf springs are fully seated into the cam tower holes.

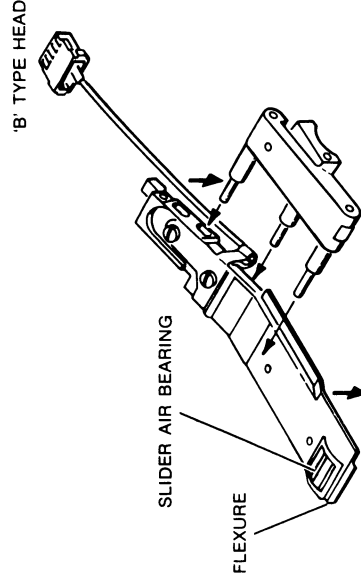


FIGURE 4-8. HEAD INSTALLATION TOOL IN 'B' TYPE HEAD

5. Check for HDI after purging system 5 minutes by performing a manual head load.
6. Perform the head alignment procedure in paragraph 4.6.3.



**FIGURE 4-9. USING HEAD TORQUE TOOL**

### 4.6.3 Head Adjustment

The procedure for head adjustment in the system environment is presented below. The procedure for offline head adjustment using the 800 Disc Storage Subsystem Tester is provided in the *Model 800 Operator's Manual*.

#### 4.6.3.1 Tools Required

Tools required are the Head Alignment Kit (P/N 215970) and a CE Disc Pack. To adjust heads in the RP06 drive, the CE Pack to use is P/N 335001. Use P/N 320100 for the RP05 drive.

The Head Alignment Unit (part of Head Alignment Kit) indicates the presence or absence of valid data and the magnitude and direction of misalignment when valid data is present. The DATA INVALID indicator lamp indicates the former, and the MICROINCHES indicator the latter. When DATA INVALID is out, valid data is present. Note the following when using the Head Alignment Unit:

- The MICROINCHES indicator indicates the selected data head alignment with respect to the servo head.
- An indication of 0 means the head is in perfect alignment. Deflection of the indicator in either direction indicates the number of microinches of misalignment in RP05, and **twice** the number of microinches of misalignment in RP06.
- The direction of deflection indicates the direction in which the data head is misaligned.
- For RP05, the alignment cylinder is Cylinder 245. At this odd alignment cylinder, a positive (right-hand) indicator deflection means the data head is ahead of the servo head (offset towards spindle centerline), and a negative (left-hand) deflection means it is behind the servo head (offset away from spindle centerline).
- For RP06, the alignment cylinder is Cylinder 496. At this even alignment cylinder, a positive (right-hand) deflection means the data head is behind the servo head (offset away from spindle centerline), and a negative (left-hand) deflection means it is ahead of the servo head (offset towards spindle centerline).
- For RP05/6, RESET HAR and ADVANCE HAR switches in the Head Alignment Unit have no effect and are not used.

When the DATA INVALID lamp is lit, valid data is not present for one of the following reasons:

- On Track signal is false.
- Alignment Carrier signal is not present because:
  - a. CE Pack is not loaded.
  - b. Head is grossly misaligned beyond carrier area.
  - c. Head Alignment Unit is faulty and must be replaced.

#### 4.6.3.2 Checking Alignment

1. Select WRITE PROTECT drive mode. Install CE Pack.
2. Slide logic gate fully forward. Turn off drive dc power.

3. Connect alignment unit's interface cable to B04 slot of logic assembly (see Figure 3-1 for drawing of location).
4. Turn on dc power. Press START switch.
5. Wait until the servo makes a first seek to Cylinder 000. Verify that the alignment unit's DATA INVALID lamp is lit, and extinguishes when the unit is switched to CALIBRATE.
6. Seek to alignment cylinder.
7. Assure that thermal equilibrium is established, as is required before checking alignment or adjusting alignment. Minimum requirements are:
  - a. With the wind tunnel in the closed position, the drive must operate in a track-following or seek mode for at least 20 minutes. Any disc pack may be used for the first 15 minutes; however, the CE Pack must be used and the **heads positioned at the head alignment cylinder** during the last 5 minutes.
  - b. The CE Pack must reach thermal equilibrium by running on a drive for 20 minutes, or by being used as described in a. above.
8. Set alignment unit's CALIBRATE/DRIVE READOUT switch to CALIBRATE. DATA INVALID lamp must be out, and MICROINCHES indicator must be at  $0 \pm 10$  microinches. If out of tolerance, problem could be in either drive servo system or head alignment unit.
9. Release switch.
10. Select head 00-18. If the MICROINCHES reading is not  $\pm 75$ , head alignment is required.

#### 4.6.3.3 Adjusting Alignment

1. Perform steps 1 through 6 in paragraph 4.6.3.2.
2. Open wind tunnel.
3. Engage carriage safety lock (Figure 4-10).

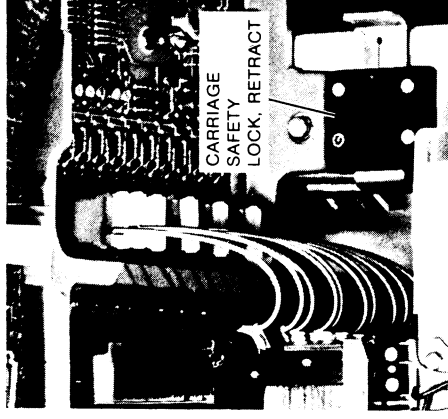


FIGURE 4-10. CARRIAGE SAFETY LOCK

4. Select head to be aligned. If more than one head or a full complement of heads is to be aligned, the alignment order should be as follows: Align heads 9 through 18, incrementing one head at a time, then heads 8 through 0, decrementing one head at a time. See Figure 4-6 for head numbering scheme.
5. Referring to Figure 4-11, loosen forward alignment clip screw and apply INITIAL torque using the Head Torque Tool. Then repeat for rear alignment clip screw.

#### CAUTION

Do not attempt to change the position of the servo head. If it is changed, all data heads may have to be aligned.

#### NOTES

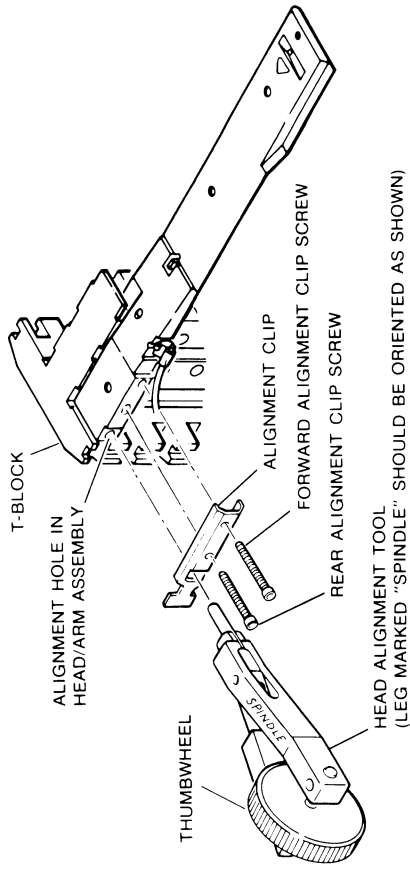
- a. When using the Head Torque Tool, continue applying torque until one or two detent clicks are felt.
- b. Do not attempt to adjust a head unless **both** screws are set at INITIAL torque. If attempted, a cracked head or broken tool may result.

6. Refer to Figure 4-11 to see the correct orientation of the word "SPINDLE" on the Head Alignment Tool relative to the head. Then insert the alignment tool such that the tapered pressure shoes on the tool (Figure 4-12) enter the square hole in the alignment clip, contacting the hole's vertical sides.
7. Rotate alignment tool's thumbwheel so that head moves to rearmost position in T-block slot. To avoid tool breakage, **do not continue rotation after the head bottoms out in the T-block**.
8. Carefully move head toward spindle by rotating thumbwheel clockwise until Head Alignment Unit's MICROMETER reads as indicated in **Table 4-4**, line "A".
9. Carefully remove alignment tool. Using the Head Torque Tool, tighten **forward** alignment clip screw to FINAL torque, then the **rear** alignment clip screw to FINAL torque.
10. At this point in the procedure the alignment error should be as indicated in **Table 4-4**, line "B". If this is not true, repeat steps 5 through 9.

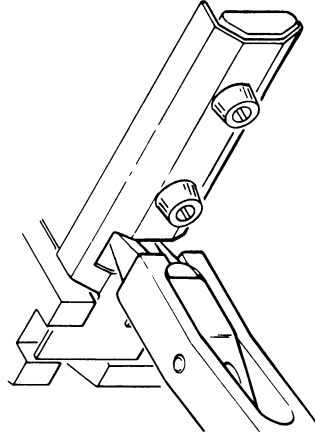
#### CAUTION

If you are experiencing problems aligning a head, look for a cracked head mount at the alignment hole or a pinched pigtail wire. If the head mount is cracked at the alignment hole, it probably resulted from failure to tighten both alignment screws to INITIAL torque before aligning. If the pigtail wire is pinched, it was done with the tool.

11. Repeat steps 5 through 10 for all heads to be aligned.
12. Retract carriage safety lock (Figure 4-10). Move wind tunnel to forward position.
13. Perform an alternate seek for two minutes, then stop the drive; repeat for a total of 8 times.
14. Assure that thermal equilibrium is established. Recheck the alignment of all heads adjusted. The alignment error should be as indicated in **Table 4-4**, line "C". If this is not true, repeat steps 2 through 13.



**FIGURE 4-11. ORIENTATION OF ALIGNMENT TOOL TO HEAD**



**FIGURE 4-12. ALIGNMENT TOOL IN HEAD**

TABLE 4-4. ALIGNMENT SPECIFICATIONS

		HEAD ALIGNMENT UNIT'S MICROINCHES READING			
		RP05	RP06*		
WIND TUNNEL OPEN CLOSED	ALL HEADS	-60 ±30 -20 ±40 ±75	HEADS 00-02 +RED ZONE +120 ±80 ±75	HEADS 03-13 +60 ±60 0 ±80 ±75	HEADS 14-18 -20 ±60 -80 ±80 ±75
	A. "INITIAL" TORQUE BIAS				
	B. "FINAL" TORQUE BIAS				
C. ALIGNMENT AFTER SEEKING					

\* On RP06 DEC DRIVES, Head Alignment Unit's microinches reading is twice the actual head alignment error.

#### 4.6.3.4 Circumferential Alignment

If a head has been replaced and the necessary equipment is available, the following check may be made after the head has been aligned.

1. The time from the leading edge of INDEX to the "Sync Byte" must range from +105  $\mu$ sec to +118  $\mu$ sec for each data head located at Cylinders 018 and 790 for the RP06 drive, or Cylinders 009 and 395 for the RP05 drive. This time measurement must be made using a **Memorex CE Pack**.

#### NOTE

Cylinders mentioned above are prerecorded, read-only cylinders. To protect these cylinders, the READ/WRITE-WRITE PROTECT switch in the operator panel must be positioned to WRITE PROTECT.

2. The Sync Byte may be recognized by the first of several larger amplitude signals following INDEX when the scope is connected to HI LIN SIG 0A. See Figure 4-13. If the scope is set so INDEX is displayed on the A trace and HI LIN SIG 0A on the B trace, and sweep mode set for Alternate with sync set for Internal Channel A, this timing may be measured at 20  $\mu$ sec/cm using the time delay control for readout.

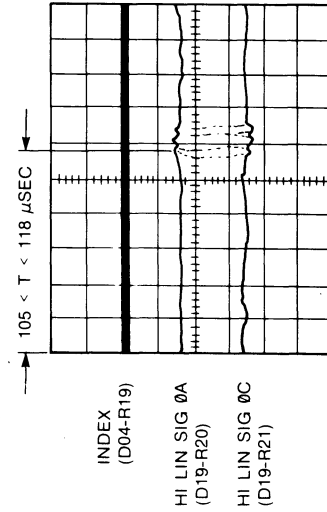


FIGURE 4-13. CIRCUMFERENTIAL ALIGNMENT TIMING

#### 4.6.4 Filtration and Cooling Components

Procedures to use in replacing the absolute filter, a logic fan, air baffle, or upspeed switch are presented in the following paragraphs (refer to Figure 4-14). No special tools are required.

#### 4.6.4.1 Replacing Absolute Filter

1. Remove the absolute filter and the flexible air duct as a unit, by removing the hose clamp under the shroud. During removal of filter from drive, lift the filter retaining clips up for the first inch.
2. After absolute filter/hose air duct has been removed from the drive, filter replacement can be made by removing air duct from filter and installing it on the replacement filter.
3. Install absolute filter/hose air duct by reversing step 1 above.

#### 4.6.4.2 Replacing Logic Fan

**CAUTION**  
230 Vac exists.

1. Disconnect power connector to fan.
2. Remove cover bar from front of the fan assembly by removing five screws. To remove one of these screws, the clamp for the read/write preamp cable (right side of cover bar) must be removed by removing four screws.
3. Remove four screws, **1** in Figure 4-14. The two screws at the rear are removed from the rear of the drive. When all screws are removed, the logic fan assembly is free (can be dropped and withdrawn from the drive).
4. Replace individual fans as necessary, and reinstall fan assembly by reversing the steps above.

#### 4.6.4.3 Replacing Baffle

Two screws hold the air baffle to the shroud. To access the two screws, remove the shroud using the procedure in paragraph 4.6.5.2. When installing the replacement baffle, be sure it is properly seated on the shroud locator pins as the baffle screws are tightened. Do not lubricate the baffle pivot points. After installing the new baffle, adjust the upspeed switch using the procedure in paragraph 4.6.4.5.

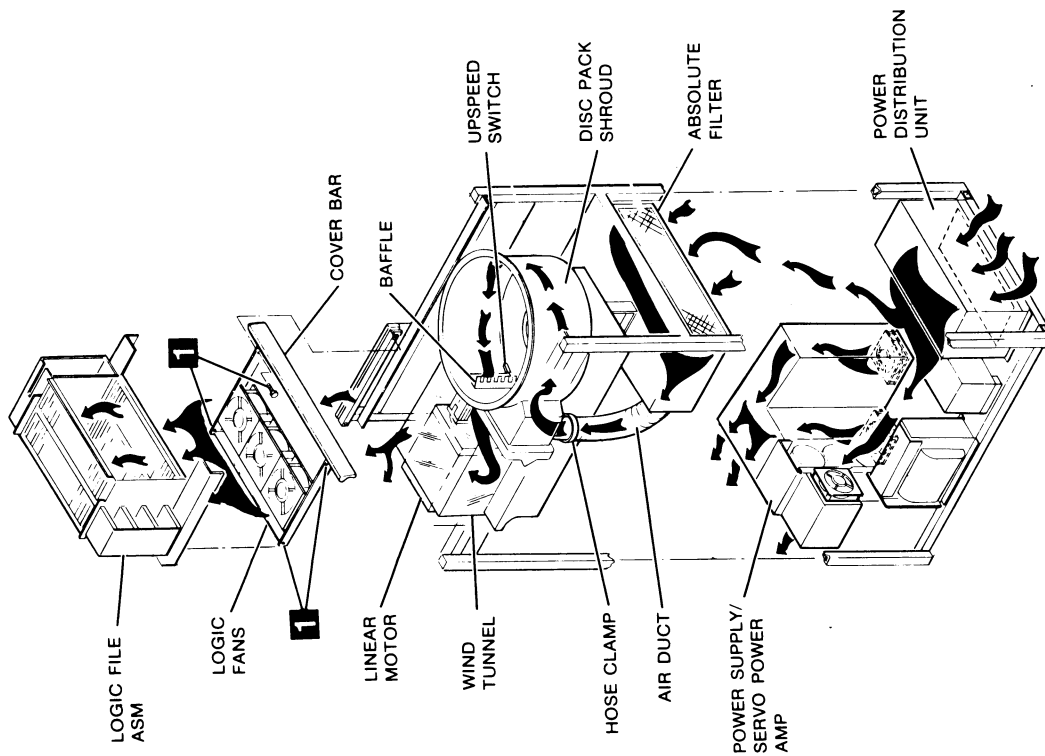


FIGURE 4-14. AIRFLOW AND FILTRATION SYSTEM

#### 4.6.4.4 Replacing Upspeed Switch

Remove the shroud (using the procedure in paragraph 4.6.5.2), switch cover, then the switch and cable assembly. When installing the replacement switch, be sure the switch wires do not interfere with head or carriage motion either in or out of the shroud area.

#### 4.6.4.5 Adjusting Upspeed Switch

With switch cover removed, adjust switch so that it closes when the baffle is 0.010 to 0.100 inch from the fully open position, then replace switch cover and verify that the adjustment is still valid.

#### 4.6.5 Shroud and Pack Access Door

Procedures to use in replacing the pack access door and shroud are presented below. No special tools are required.

##### 4.6.5.1 Replacing Pack Access Door

Remove door stops/anti lift from frame by removing two screws and nuts. While depressing the door lock plunger, slide door forward and remove from rails. Depress the plunger when installing the replacement door. After replacing glass door and door stops/anti lift, restore power to the spindle and test the door lock switch against the panel indicator (with door locked, the DOOR LOCKED lamp is illuminated).

##### 4.6.5.2 Replacing Shroud

1. Remove absolute filter as described in paragraph 4.6.4.1, step 1.
2. Disconnect upspeed switch.
3. Remove two of the three screws that attach the pack sensor to the deck plate, and rotate the pack sensor free of the shroud. Rotating the pack sensor away from the shroud will prevent damage to the pack sensor seal during removal of shroud.

4. Remove two screws located at rear of shroud cover (logic file full forward), then remove two screws at front of shroud cover. Lift front of shroud cover and remove from drive.

#### NOTE

Whenever shroud cover is removed, inspect the foam gasket underneath. Replace the gasket if damage is visible.

5. Remove two screws from behind the air baffle, which attach the shroud to the cam tower. (The shroud is positioned to the cam tower by a pin.)
6. Remove the four screws holding the shroud to the deck plate.
7. Remove shroud by lifting it from cam tower locating pin, using care not to damage the heads or switch cable and plug. Slight rotation of shroud may be necessary when lifting shroud from drive.
8. Remove air baffle by removing two screws. Install baffle onto replacement shroud, being sure baffle is properly seated on shroud locator pins as the baffle screws are tightened.
9. Install shroud by reversing the removal procedure, taking care that the shroud is firmly seated on the cam tower locating pin while the two screws under the air baffle are installed. Then install the four screws which attach the shroud to the deck plate.

#### 4.6.6 Drive Mechanism

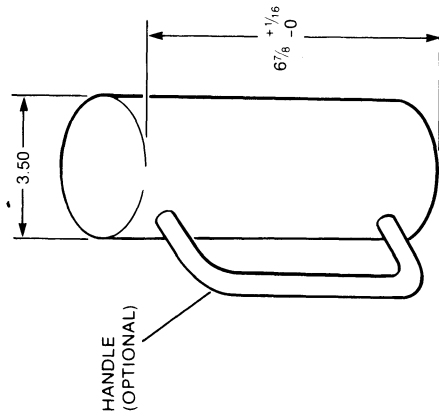
Procedures to use in replacing the drive motor, drive belt, spindle lock shaft, and spindle—and adjusting the belt tension, spindle lock, and pack cover sensor—are presented below.

##### 4.6.6.1 Tools Required

Special tools required are contained in the Mechanical Alignment Kit (P/N 215971).

Supplying the FE with one additional tool is recommended to simplify drive motor replacement; it is shown in Figure 4-15. It is a simple device used as a "spacer" between cabinet floor and bottom of the motor to support the weight of motor as retaining bolts are removed and to move the motor near the side of the drive where it can be withdrawn without special effort.





**NOTE**

THIS CYLINDRICAL TOOL CAN BE PLASTIC, ALUMINUM, OR HARDWOOD WHICH IS SPLINTER-FREE. CONFIGURATION MAY BE A 3.00 SQUARE.

**FIGURE 4-15. RECOMMENDED DRIVE MOTOR REPLACEMENT TOOL**

**4.6.6.2 Replacing Drive Motor**

Unlike other maintenance activities, replacing the drive motor requires two FEs (to manipulate the heavy motor safely in/out the drive) and a variety of standard shop tools (nut drivers, clipper, socket wrench and accessories). Completing the procedure which follows will require about 45-60 minutes time.

1. Verify that all power to drive is off.
2. Provide space for accessing into the drive's right side, by moving the drive and attached DCL away from the line. Detaching the DCL from the drive is **not** required.

**NOTE**

Pay close attention to cable location and tension.

3. If the drive has a side cover, remove it by raising until brackets disengage, then remove the ground wire from the ground lug.
4. Remove the front and rear covers. Each cover is removed by opening the cover, pulling the quick-disconnect ground lug (near top hinge), and lifting the cover off its hinges.
5. Disconnect the air duct from the shroud, by loosening the screw in the hose clamp and pulling down.
6. Remove the absolute filter and flexible air duct as a unit. Lift the filter retaining clips up for the first inch of travel, then slide the filter all the way out.
7. Remove Power Distribution Unit (PDU) cover and disconnect drive motor wiring. Cut the plastic cable ties with a clipper as required to free up motor wiring from other wiring.
8. Replace PDU cover; hand tighten the screws. (Cover is replaced at this time for protection when motor is removed.)
9. Remove power supply cover to allow for accessing into the rectifier assembly. Using a long 1/4" nut driver, remove four screws holding fan to rectifier assembly and place the fan over the transformer.
10. Remove capacitor from cabinet floor under the drive motor, by loosening one screw and pulling up on the capacitor. The clamp which is screwed to the floor remains in place.
11. Remove the drive belt adjustment nut, [1] in Figure 4-16, using a 3/8" nut driver (or 3/8" socket and ratchet wrench). About 50 turns will be required.
12. Working at the front of the drive, remove drive belt from motor pulley by "walking the belt upwards" from the left of the pulley, and manipulating the belt out of the motor plate. Remove the belt.

13. Unhook tension spring **2** from motor bracket. To locate the spring, reach through the front of the drive, under and around the motor from the left, to the area behind the motor.

**NOTE**

The bracket end of spring fits into an insulating sleeve which prevents static buildup. Be sure the sleeve is in place.

14. Place a "spacer" (like that shown in Figure 4-15) on cabinet floor under the motor. With this spacer capable of supporting the weight of motor, remove three bolts, 3 in Figure 4-16, holding drive motor to deck plate. To remove these bolts, a  $\frac{3}{8}$ " ratchet wrench and the following accessories are needed:  $\frac{5}{8}$ " socket, a 2" extension, and a 12" extension, the latter for the rear bolt. Socket set is stocked under DEC part number 29-22445.

**CAUTION**

A "spacer" must be used to avoid injury by losing control of the motor when the bolts are removed.

15. With the motor resting "free" on the spacer, remove the motor from the drive. For safety (mainly against jamming fingers), the motor is removed by two FEs, working together from the front and side of the drive, to manipulate the motor over the PDU sideways and out through the front.

**CAUTION**

When removing the motor, avoid a hard impact against the PDU or other components.

16. Install replacement motor as follows:

**NOTE**

A spacer must be used for safety's sake. Do not attempt procedure without providing for a spacer sized per Figure 4-15.

- a. If the insert comes loose or a bolt breaks, use the enclosed insert or bolt as replacement. Locktite should be used only on the insert as it is placed into the casting. Torque insert to 100 in. lbs.

- b. Manipulate the motor over the PDU and into the drive, sideways and bottom first, then turn vertically (plate up) and hold while the other FE positions the spacer underneath.

- c. Line up the motor bolt holes (motor plate to deck plate holes) by moving and turning the spacer/motor combination over the cabinet floor. The motor bracket for the tension spring points toward the rear of the drive.

- d. Hand tighten the three motor bolts, then remove the spacer.

- e. Using the new belt supplied with the replacement motor, replace the drive belt by reversing step 12 above. Be sure the smooth side of the belt faces the pulleys. If difficulty is encountered, loosen the three motor bolts.

- f. Hook the tension spring onto the motor bracket, being sure hook points down and that the insulating sleeve is properly installed in bracket, and hold until step g below is completed.

- g. Attach other end of tension spring (one FE) and tighten belt adjustment nut (other FE) just enough to hold the spring in place.

- h. Tighten the three motor bolts using the tools in step 14 (50 in. lbs.).

- i. Adjust drive belt tension using the procedure in paragraph 4.6.6.3.

- j. Replace the fan. One FE should hold the fan and line up the holes from the front of the drive, while the other FE tightens the four retaining screws from the rear.

- k. Replace the power supply cover. Don't use excessive force on the self-tapping screws.

- l. Remove PDU cover and replace the motor wires (which are number coded against terminal numbers), then replace the cover.

- m. Replace the capacitor.

- n. Replace the absolute filter and air duct. Tighten the clamp holding the air duct to the shroud.

- o. Replace side cover by reversing step 3 above.
- p. Replace front and rear covers by reversing step 4 above.
- q. Return the drive and DCL to its original position in the customer subsystem.

#### 4.6.6.3 Adjusting Drive Belt Tension

Adjust belt tension by tightening tension adjustment nut (1<sup>1</sup>/<sub>32</sub>" ) 1 such that a total of 7 threads protrude from the nut. With exactly 7 threads showing, the required belt tension (55 pounds) is applied.

#### 4.6.6.4 Replacing Drive Belt

##### CAUTION

Drive motor can start without a pack mounted.

1. Remove absolute filter as described in paragraph 4.6.4.1, step 1.
2. Remove spindle grounding assembly 4.
3. Loosen drive belt adjustment nut 1. While turning the motor pulley counterclockwise (looking from bottom), remove belt from motor pulley by "walking the belt upwards" from the left. Work belt out of motor plate, and remove from drive.
4. Install replacement belt by reversing steps 1 through 3 above, being sure the smooth side of the belt faces the pulleys, then adjust belt tension as stated in paragraph 4.6.6.3.

#### 4.6.6.5 Replacing Spindle Lock Shaft

##### CAUTION

Drive motor can start without a pack mounted.

1. Remove absolute filter as described in paragraph 4.6.4.1, step 1.
2. Remove spindle grounding assembly, 4 in Figure 4-16.
3. Remove three screws holding retaining spring/cover to spindle pulley, and remove cover.

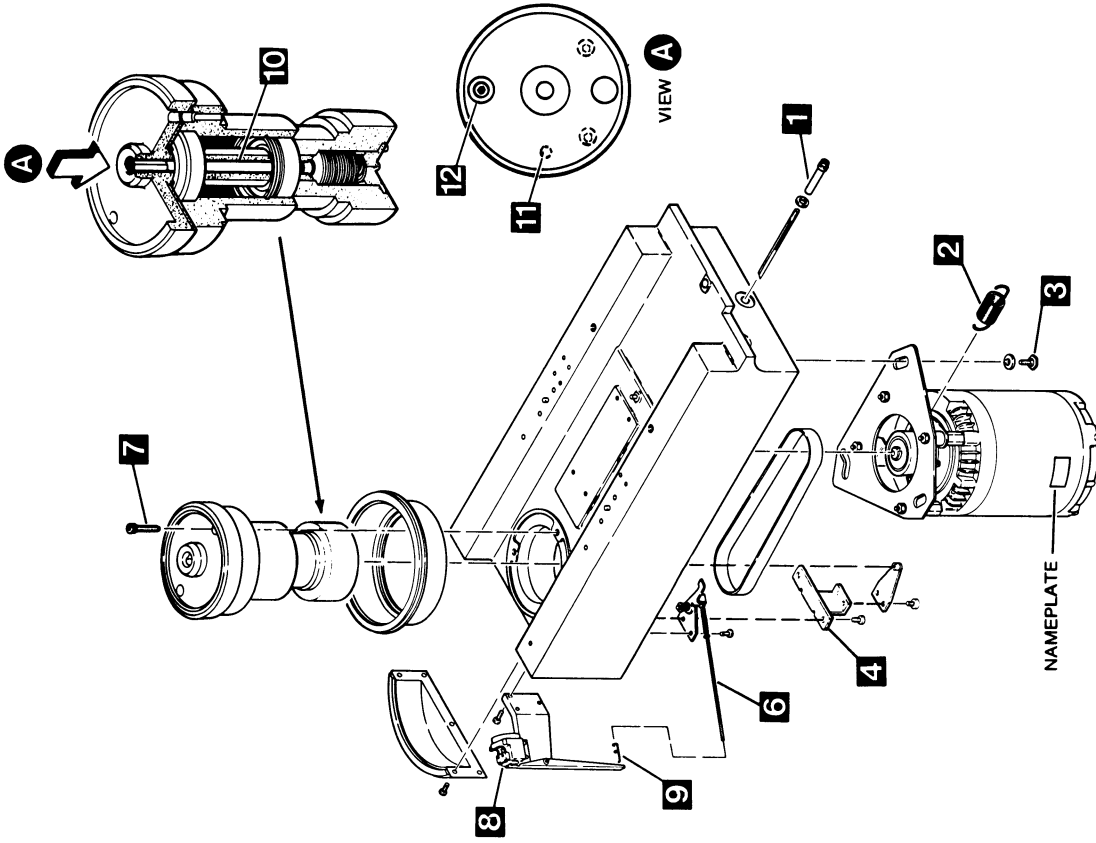


FIGURE 4-16. DRIVE MECHANISM

4. After reading the WARNING below, tap top of spindle; lock shaft **10** will drop straight down. Remove from spindle. Remove and save any brass shims.

#### WARNING

The large springs on the end of the spindle lock shaft are held in place under great pressure by a hex nut and snap ring. The shaft must be handled carefully to avoid dropping or in any way disturbing the spring assembly. Inadvertent release of the springs could cause serious injury.

5. Install replacement shaft by replacing the brass shims and reversing steps 1 through 4 above.

#### 4.6.6.6 Replacing Spindle

##### CAUTION

Drive motor can start without a pack mounted.

1. Remove absolute filter as described in paragraph 4.6.4.1, step 1.
2. Remove shroud as follows:
  - a. Disconnect upspeed plug. Disconnect air duct from absolute filter.
  - b. Remove shroud cover shroud and hardware as described in paragraph 4.6.5.2, steps 2 through 7.
3. Remove spindle grounding assembly, **4** in Figure 4-16.
4. Loosen drive belt adjustment nut **1**. While turning the drive motor pulley counterclockwise (looking from bottom), remove belt from motor pulley by “walking the belt upwards” from the left. Work belt out of motor plate and remove from drive.
5. Three allen screws **7** hold spindle housing to deck plate; rotate spindle so that screws are visible through access hole **12** in hub, and remove.
6. Pull spindle up, slowly to avoid binding, and remove from drive.

7. Install replacement spindle as follows:

- a. Mount spindle housing by reversing steps 5 and 6. **Be sure to orient spindle housing so that the small hole **11** is on the left (9 o'clock position as viewed from the front VIEW A, Figure 4-16).**
- b. Check for binding of housing with deck plate by: inserting an allen wrench into the spindle housing hole and turning the housing on the deck plate. A bound assembly will not turn. Free the binding by applying force to the bottom of the pulley. **IF THE SPINDLE IS NOT SEATED PROPERLY WHEN THE DRIVE IS STARTED, ALL TWENTY HEADS WILL CRASH! TORQUE SCREWS TO 200 IN. LBS. (+00/-50) WITH TORQUE WRENCH.**

- c. Remove all heads using the procedure in paragraph 4.6.2.2.
- d. Adjust carriage way alignment using the procedure in paragraph 4.6.7.10.
- e. Adjust linear motor alignment using the procedure in paragraph 4.6.7.3.
- f. Replace drive belt, spindle grounding assembly, absolute filter, and shroud by reversing steps 1 through 4. Adjust belt tension by tightening adjustment nut **1** such that a total of 7 threads protrude from nut.

#### NOTE

Whenever a spindle is replaced or the old spindle is reinstalled, it is necessary to perform carriage way alignment.

#### 4.6.6.7 Adjusting Pack Cover Sensor

Clearance between edge of spindle hub and tip of actuator in the pack cover sensor must be  $4\frac{9}{64} \pm \frac{1}{64}$  inches, as shown below. If not, adjust as follows:

## 4.6.7 Actuator Mechanism

Procedures to use in aligning and/or replacing the following parts are presented in the paragraphs below: linear motor, bobbin, carriage T-block assembly, carriage way, head unload cams, cam tower, tachometer, and tach rod. Procedures for adjusting tack gain and cleaning the carriage way and bearings are included.

### 4.6.7.1 Tools Required

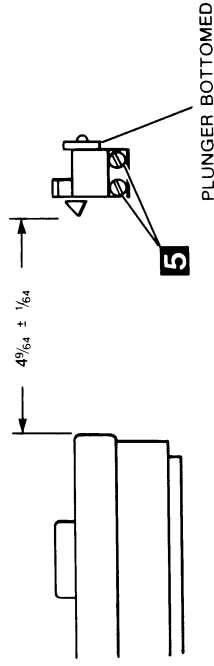
Special tools required are the Mechanical Alignment Kit (P/N 215971) and the four head tools (see paragraph 4.3).

### 4.6.7.2 Replacing Linear Motor

1. Remove large screw and standoff which hold each spring clip to wind tunnel. Remove wind tunnel by sliding off the rails.
2. Carefully insert head separator tool into head and carriage area from the front, and attach tool to carriage using captive screws on tool. Move carriage forward.
3. From rear of drive, remove two of the three allen screws holding carriage to bobbin. Loosen the third screw by inserting the allen driver through the access hole in the head separator tool; leave driver and screw in the tool to simplify reinstallation.
4. Push carriage forward about three inches, then unscrew tach rod (1) in Figure 4-17) from carriage using a 1/4-inch open-end wrench.
5. Push rod into tachometer coil but do not withdraw it. The tach rod is brittle and must be handled with care to avoid breakage.
6. Disconnect tach plug and open cable clamp on cable. Remove screw and clip (2) in rear center of motor, and withdraw tachometer coil together with the rod from rear of motor. Do not place them on the linear motor after removal.

### NOTE

Cable clamps are friction type and open from larger end. When reassembling tach into motor, the wires must point downward.



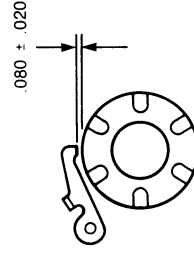
1. Loosen both screws (5) holding sensor (8) to mounting bracket.
2. Adjust sensor to obtain clearance of  $4\frac{9}{64} \pm \frac{1}{64}$  inches between tip of switch actuator and outer edge of spindle hub. Tighten screws (5) and recheck adjustment.
3. Perform spindle lock adjustment (see paragraph below).

### 4.6.6.8 Adjusting Spindle Lock

#### CAUTION

Drive motor can start without a pack mounted.

1. Raise actuator rod (6) out of slot, and rotate rod to obtain clearance of  $0.080 \pm 0.020$  inch between spindle lock and lock pawl (see sketch below).
2. Replace actuator rod retaining clip (9).
3. Verify that actuator rod (6) is bottomed in slot, and spring clip is installed.



7. Remove plastic wind deflector from side of motor by removing three screws.
8. Remove plug connected to switches on top of motor, and loosen cable clamps.
9. Unplug five wires at motor terminal strip.
10. Remove three large allen screws **3** holding linear motor to deck plate (two screws on top front, one screw on bottom rear).
11. After reading the WARNING and NOTE below, slide linear motor from rear of drive without lifting.

**WARNING**

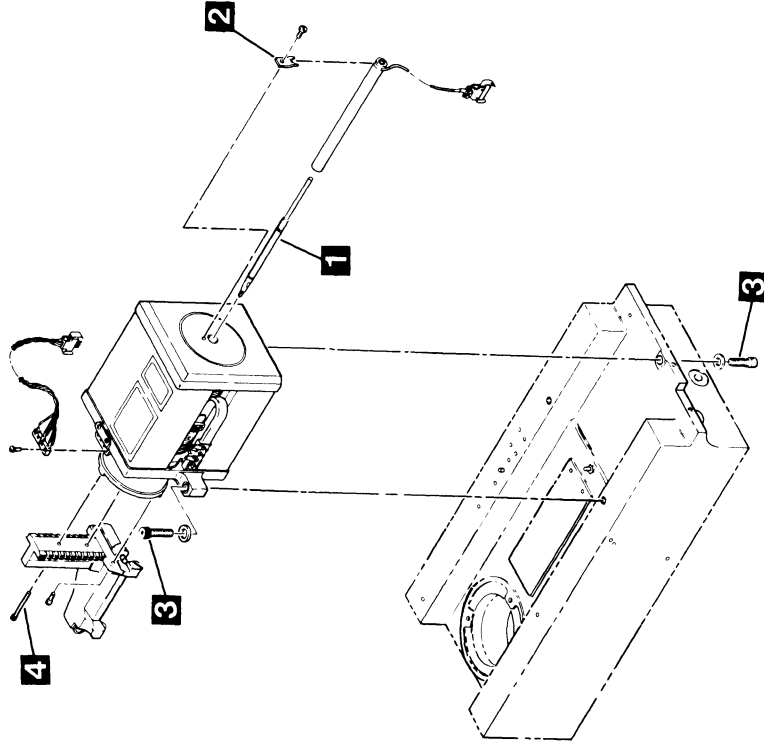
When removing linear motor, take it "straight away" from the drive to avoid serious injury which will result if fingers are caught between motor and frame members. In addition, take precautions to prevent the carriage assembly from slipping off the end of the way, and the head assembly from slipping off the back of the cams.

**NOTE**

Before removing the linear motor, prepare a clean working area to receive the motor. This working area, preferably a wooden desk or bench that is free of metal particles and tools, should be covered with clean paper such as printer paper.

**To install a linear motor, proceed as follows:**

12. Place linear motor on deck plate back pad, and slowly slide forward.
13. Install the three motor screws **3**, finger tight. Be sure the front end of the motor is registered against the end of the way.
14. Align the linear motor using the procedure in paragraph 4.6.7.3. Alignment must be performed before further reassembly.
15. Install tachometer and rod (see steps 4 through 6 above).



**FIGURE 4-17. ACTUATOR MECHANISM**

2. With carriage about one inch from motor, move front of motor sideways, as necessary for the tip of the alignment rod to fit into alignment hole in carriage.
3. While taking care not to shift the front of motor, move carriage against crash stop and adjust rear of motor so that alignment rod again fits alignment hole in carriage.
4. Secure motor to deck plate; first tighten the front screws and then the rear screw.
5. Recheck alignment with carriage at both forward and rear positions. Realign if necessary.

#### 4.6.7.4 Replacing Bobbin

##### CAUTION

Use head separator tool for machine with heads installed.

With both linear motor and tachometer removed (refer to paragraph 4.6.7.2), replace bobbin as follows (refer to Figure 4-18):

1. Remove screw [4] holding terminal strip to side of motor.
2. Remove two screws [1] holding flex conductor to bobbin.
3. Locate depression in side of motor pole piece, and, using a screwdriver handle, tap the two brass nuts [2] used to attach flex conductor into depression.
4. Withdraw bobbin from front of motor.

**To replace or reinstall bobbin in motor, proceed as follows:**

5. Place bobbin in motor.
6. Place one flex conductor nut [2] in pole-piece depression. Slide bobbin over nut and, using screw [1], reach through bobbin and thread screw into nut two or three turns. Draw nut through hole in bobbin. Repeat this step for other nut. Remove screws from nuts.

16. Connect bobbin to T-block as follows:

- a. Cut 0.005-inch thick paper (thickness of a punch card), making a paper strip 12.0 x 0.75 inches.
- b. Apply Loctite #C to the three bobbin mounting screws [4] and assemble bobbin to T-block; do not tighten screws.
- c. Place paper strip around front of bobbin, and slide into magnet assembly.
- d. Starting with the two bottom mounting screws first, tighten the three bobbin mounting screws [3] using a torque wrench to 17 +0/-4 inch-pounds.
- e. Remove paper strip. Check way alignment using the procedure in paragraph 4.6.7.10. If way alignment is within specification, remove way alignment tool and install tach coil assembly. If way alignment is not within specification, distortion caused by interference of bobbin with linear motor can result. **The occurrence of such distortion would be a worst-case condition, requiring bobbin replacement using the procedure in paragraph 4.6.7.4.**

17. Check for bobbin interference with motor. Repeat step 16 if necessary to correct interference.

18. Looking through rear of tachometer, slide the carriage the full length of its travel several times, checking to be certain that the tach rod never touches the tachometer. This clearance must exist; if not, replace the tach rod using the procedure in paragraph 4.6.7.13.

##### CAUTION

Head separator tool must be used when heads are on drive T-block.

#### 4.6.7.3 Aligning Linear Motor

With alignment rod inserted through center of motor, the three motor screws [3] finger tight only, and the front end of the motor registered against the end of the way, align the linear motor as follows:

1. Orient alignment rod so that wide end of diamond shaped tip is in a horizontal plane.

10. Check electrical continuity of flex conductor and bobbin as follows:

- a. While moving bobbin back and forth in motor, use a screwdriver to short between center conductor on terminal strip and one end of terminal. When shorted, a definite magnetic drag must be felt as the bobbin is moved.
- b. Repeat (a) above, shorting this time between center terminal and other end terminal. If magnetic drag is not felt, find and correct the open circuit.

11. Perform the linear motor replacement procedure in paragraph 4.6.7.2.

#### 4.6.7.5 Replacing Heads Retracted Switch

The switch bracket [3] is installed and adjusted at the factory. If the switch must be replaced, do not loosen the bracket on the linear motor. Remove only the screws passing through the body of the switch.

#### 4.6.7.6 Replacing Carriage T-Block Assembly

1. Remove data heads using the procedure in paragraph 4.6.2.2.
2. Remove shroud using the procedure in paragraph 4.6.5.2, steps 1 through 8.
3. Remove linear motor using the procedure in paragraph 4.6.7.2, steps 1 through 11.
4. Referring to Figure 4-19, disconnect carriage ground strap [1] from deck plate.
5. Roll carriage to rear of carriage way, and carefully remove carriage from drive.

#### To reassemble with a replacement carriage, proceed as follows:

6. Clean way and carriage bearings using the procedure in paragraph 4.6.7.9.

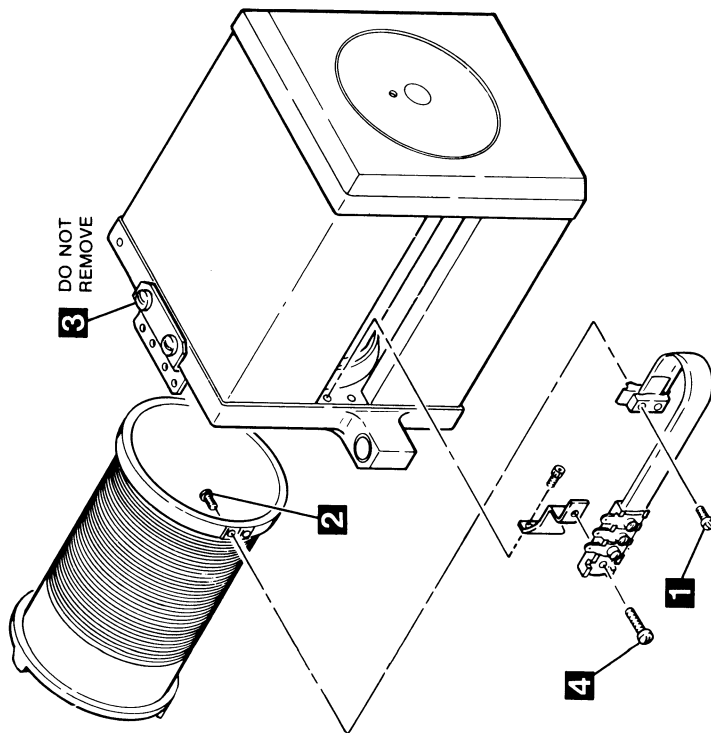


FIGURE 4-18. BOBBIN AND LINEAR MOTOR

7. Inspect flex conductor for cracks. Replace if necessary.
8. Taking care not to push nuts out of holes, install flex conductor. Make certain that conductors and insulator are square before tightening screws. If screws cannot be tightened, loosen and retighten.
9. Attach terminal strip to motor using screw [4].



7. Carefully install carriage onto carriage way.
8. Perform carriage tilt-limit adjustment as described in paragraph 4.6.7.7.
9. Connect carriage ground strap **1**.
10. If a new carriage T-block assembly is being installed, perform way alignment procedure in paragraph 4.6.7.10.
11. Reinstall and align linear motor and bobbin (paragraphs 4.6.7.2 through 4.6.7.4).
12. Reinstall data heads and adjust (paragraphs 4.6.2 and 4.6.3).

**4.6.7.7 Adjusting Carriage Tilt Limit**

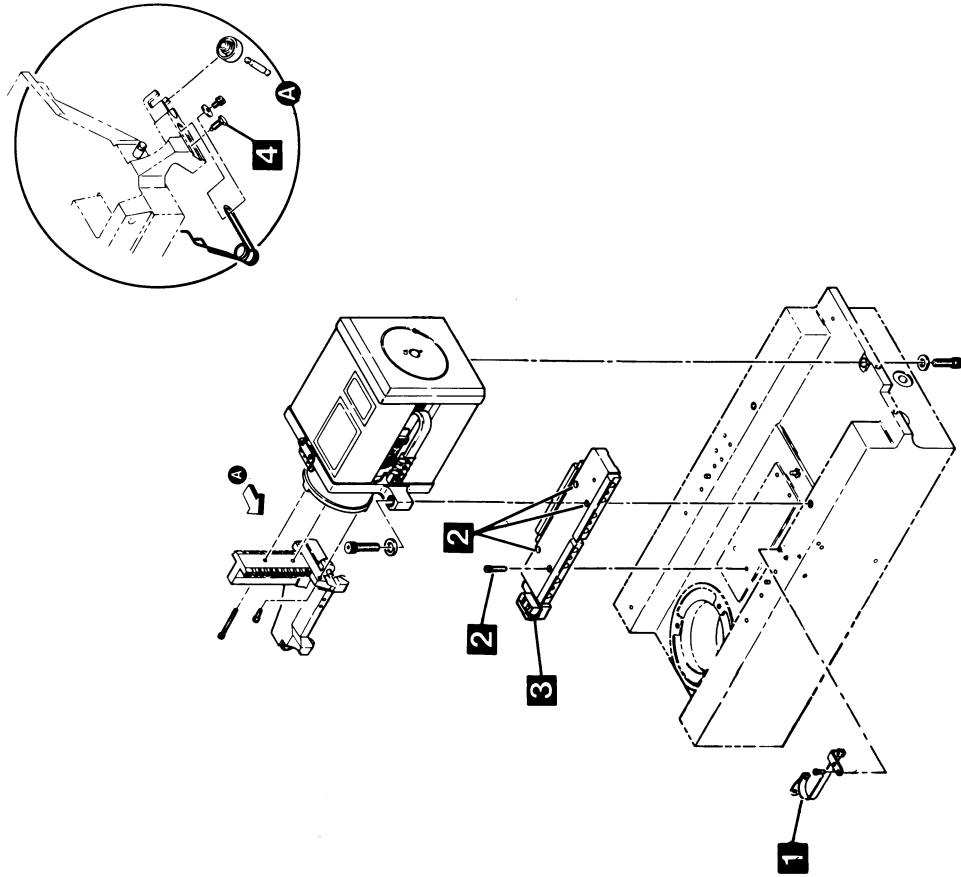
Using a feeler gauge, adjust carriage tilt-limit screw **4** to obtain clearance of  $0.002 \pm 0.001$  inches between limit-screw tip and way.

**4.6.7.8 Replacing Carriage Way**

1. Remove all heads as described in paragraph 4.6.2.2, steps 1 through 9.
2. Remove absolute filter as described in paragraph 4.6.4.1, step 1.
3. Remove shroud cover and shroud as described in paragraph 4.6.5.2, steps 2 through 7.
4. Remove linear motor as described in paragraph 4.6.7.2, steps 1 through 11.
5. Remove four screws (**2** in Figure 4-18) holding way to deck plate, and remove way from drive.

**To install way, proceed as follows:**

6. Clean way (paragraph 4.6.7.9) and deck plate.
7. Install crash stop **3** on new way.
8. Align way (paragraph 4.6.7.10).



**FIGURE 4-19. CARRIAGE T-BLOCK ASSEMBLY AND WAY**

9. Torque four screws [2] to 50 +00/-10 inch pounds.
10. Reinstall and align linear motor and bobbin (paragraphs 4.6.7.2 through 4.6.7.4).
11. Install linear motor, shroud, shroud cover, and absolute filter by reversing the removal procedure.
12. Reinstall data heads and adjust (paragraphs 4.6.2 and 4.6.3).

#### 4.6.7.9 Cleaning Carriage Way

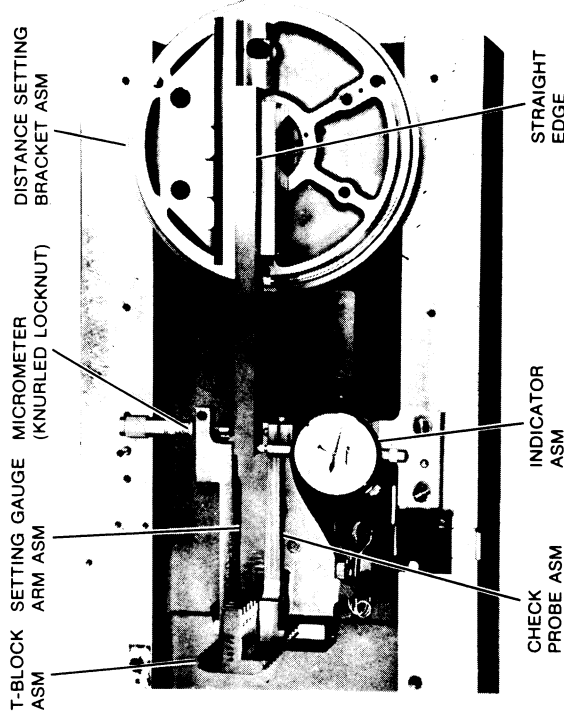
With shroud removed, clean way and carriage bearings as follows:

1. Install head separator tool.
2. Clean way with Kimwipes moistened with isopropyl alcohol. Move carriage as necessary.
3. Remove alcohol residue with dry Kimwipe. Remove all foreign material from way area.
4. Clean carriage bearing surfaces with Kimwipes slightly moistened with isopropyl alcohol. **Do not allow alcohol to enter bearing seals.**
5. Wipe bearing surfaces with dry Kimwipe.
6. Remove head separator tool and reinstall shroud (paragraph 4.6.5.2)

#### 4.6.7.10 Adjusting Carriage Way

1. Remove cam tower assembly (see paragraph 4.6.7.12).
2. Referring to Figure 4-20, mount the distance setting bracket assembly on the drive spindle; the micrometer should be set at 0.200 or higher. Make certain the mating surfaces of adapter and spindle are free of foreign particles.
3. Mount the setting gauge arm on T-block over mark "S." When correctly mounted, five rows of holes show on the T-block above the arm. Do not torque the screws.

4. Adjust the arm to locate the micrometer ball attachment up from the bottom of the straight edge.
5. Mount the way check probe in the same manner, on the opposite side of the T-block (refer to Figure 4-20). The ball attachment on the micrometer and the spherical point on the way check probe should be at an equal height 0.1 inch from the bottom of the straight edge. Torque the four screws retaining the check probe using the torque wrench at 6 in-lbs.



**FIGURE 4-20. WAY ADJUSTMENT TOOLS ON FULLY RETRACTED WAY**

6. Loosen the knurled lock nut (Figure 4-20), and **very gently** crank the micrometer head on the setting gauge arm until both spherical points touch the straight edge. This must be done gently to prevent gauge deflection. The carriage must be in the fully retracted position. Be advised that **the micrometer ball attachment comes off easily**.

7. Align the way using Table 4-5. Enter this table (first column) with the micrometer reading at the end of step 6, and read across for the optimum alignment setting. Set the micrometer to the optimum setting for your actual case, and lock the knurled nut on the micrometer handle.

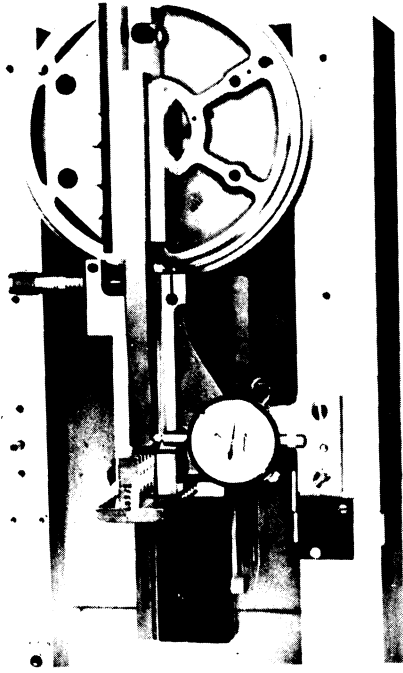
**TABLE 4-5. WAY ALIGNMENT EXAMPLE CASES**

Initial Micrometer Reading	Final Micrometer Reading
.1710	.1980
.1715	.1982
.1720	.1985
.1725	.1987
.1730	.1990
.1735	.1992
.1740	.1995
.1745	.1997
.1750	.2000
.1755	.2002
.1760	.2005
.1765	.2007
.1770	.2010
.1775	.2012
.1780	.2015
.1785	.2017
.1790	.2020

8. Mount the way indicator assembly.

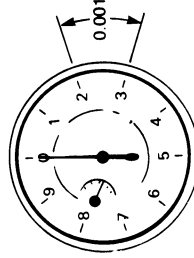
9. With a finger placed behind the T-block to avoid jarring, move the carriage from its fully retracted position (Figure 4-20) to its fully extended position (Figure 4-21) to verify that:

- a. Readings in the indicator stay within the indicator's range, and



**FIGURE 4-21. WAY ADJUSTMENT TOOLS ON FULLY EXTENDED WAY**

- b. Full swing in the readings is 0.001 or less (see sketch below). If greater than 0.001, shift the front end of the way sideways until the full swing is within 0.001. A pin secures the rear of the way to the deck plate, and serves as a pivot during this adjustment.



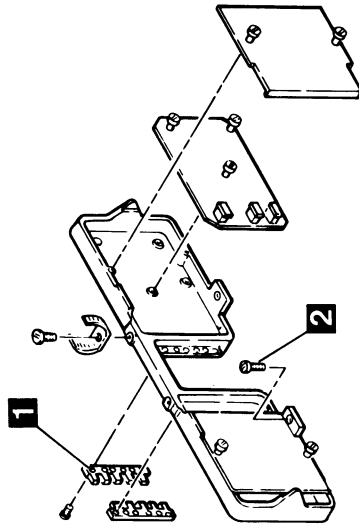
If the 0.001 tolerance cannot be achieved, check way and carriage bearings for foreign particles, and clean if required (paragraph 4.6.7.9). Again shift the front end of the way sideways to obtain the required adjustment. If tolerance is still unattainable, the way or carriage may need replacement.

10. Snug each carriage way screw, then apply equal torque increments to each screw until all reach full torque (55 in-lbs).

11. Repeat step 9. This is necessary to ensure the distance setting bracket assembly was correctly installed and that the mating surfaces were clean.
12. If the voice coil was disconnected during this alignment, repeat step 9 with the coil connected (see paragraph 4.7.6.2, step 16).

#### 4.6.7.11 Replacing Cams

1. Remove absolute filter as described in paragraph 4.7.4.1, step 1.
2. Remove shroud cover and shroud assembly (see paragraph 4.6.5.2, steps 2 through 7).
3. Carefully insert head separator tool into head/carriage assembly, and fasten tool to carriage.
4. Push carriage forward so that heads are supported by the tool.
5. Remove four screws, **1** in figure 4-22, holding each cam to cam tower, and carefully remove cams.



**FIGURE 4-22. RETAINING SCREWS, CAMS AND CAM TOWER**

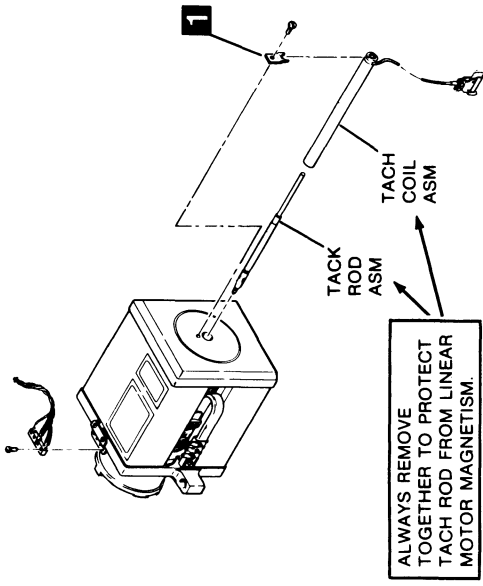
6. To install replacement cams, reverse the steps above. Be sure cams are positioned against outer vertical edge of cam tower as screws are tightened. After cams are installed, retract carriage and inspect heads to verify that arms are properly seated and flexures are not bent.
7. Install filter, shroud, and shroud cover by reversing the removal procedure.

#### 4.6.7.12 Replacing Cam Tower

1. Remove cams (see paragraph 4.6.7.11, steps 1 through 6).
2. Disconnect paddle cards from R/W preamps.
3. Remove head plug clamps and unplug heads.
4. Loosen cable clamps on top of cam tower. Remove screws, **2** in Figure 4-22, holding cam tower to deck plate.
5. With logic gate in rear position, remove tower from top front of drive; lift up about a quarter inch to clear alignment dowel pins.
6. To install a cam tower, reverse the steps above taking care that cams are positioned against outer vertical surfaces of tower. Tighten screws holding paddle cards to tower with a screwdriver to ensure a good ground.

#### 4.6.7.13 Replacing Tachometer Rod

1. Carefully insert head separator tool into head/carriage assembly and fasten tool to carriage.
2. Push carriage forward about two inches. Using a 1/4-inch open-end wrench, reach between carriage and bobbin and unscrew tach rod from carriage.
3. Move carriage to its fully retracted position. Do not remove tach rod (Figure 4-23), now protruding beyond rear of tachometer. The tach rod is brittle and must be handled with care to avoid breakage.



**FIGURE 4-23. TACH RETAINING SCREW AND CLIP**

4. Disconnect tachometer plug and loosen cable clamp.
5. Remove screw and clip, **1** in Figure 4-23, on rear center of linear motor.
6. Withdraw tachometer coil and rod together from linear motor; do not pull on wires.
7. Withdraw and replace tach rod.
8. To install a tach rod, reverse the steps above, check clearance of rod within tachometer, and adjust tachometer gain using the procedure in paragraph 4.6.7.15. To check clearance, slide the carriage the full length of its travel several times; rod must not touch tachometer. It may be necessary to shine a flashlight through front of tachometer to see clearly.

**4.6.7.14 Replacing Tachometer Coil**

1. Perform steps 1 through 3 in paragraph 4.6.7.13.

2. To install a tachometer, reverse the steps above, making certain that tachometer wires point downward, then perform the tachometer gain adjustment in paragraph 4.6.7.15. While installing, take care not to push the tach rod forward; this motion could cause the heads to move off the unload cams.

**4.6.7.15 Adjusting Tachometer Gain**

To adjust tach gain in an **RP06** drive in the system environment, proceed as follows:

1. Sequence up the drive.
2. Exercise the drive for at least five minutes by making alternate seeks between Cylinders 000 and 600. Continue seeking while performing step 3 below.
3. Adjust potentiometer on Velocity Servo PCB (location D14 in logic gate) such that the **average time difference between the signals +DIFF LESS THAN 32 (positive edge) and -DIFF=0 (negative edge) is 8.0 msec.** These signals are at location D02 in the logic gate, pins L24 and R23, respectively. **The forward and reverse seek times will be different.**

To adjust tach gain in a **RP05** drive in the system environment, use the procedure above, noting the two exceptions below:

- a. Make alternate seeks between Cylinders 000 and 300.
- b. The required time difference between signals is 9.5 msec.

**4.6.8 Miscellaneous Electrical Assemblies**

Procedures to use in removing and installing the following parts are presented in the paragraphs below: control panel, lamp matrix and motherboard PCBs, R/W preamp, servo power amp, servo amp, internal R/W cable, and R/W preamp cable. No special tools are required.

#### 4.6.8.1 Replacing Operator Control Panel

1. Loosen thumb screw, **1** in Figure 4-24, holding panel to logic assembly.



**FIGURE 4-24. OPERATOR CONTROL PANEL, HALF WAY OUT**

2. Slide panel out halfway, and disconnect connector **2** on top of operator control PCB; look and correct for possible binding where shown in Figure 4-24. Remove panel from drive.
3. To reinstall the panel, reverse the procedure above, taking care to check keying of PCB connector.

#### 4.6.8.2 Replacing Lamp Matrix PCB

1. Remove connector on top of operator control PCB.
2. Loosen three thumb screws holding lamp matrix PCB to panel, and remove PCB.
3. Install a lamp matrix PCB by reversing the procedure above.

#### 4.6.8.3 Replacing Logic Assembly Motherboard PCB

1. Remove all PCBs and paddle boards from logic assembly.
2. Remove operator control panel.
3. Remove both screws holding R/W internal cable connector to motherboard, and unplug connector.
4. Remove dc cable from motherboard TB.
5. From front of drive, remove all four screws holding motherboard to logic assembly.
6. Remove motherboard from rear of assembly.
7. Remove magnetic door catch from old motherboard.

#### To install a motherboard PCB:

8. Install magnetic door catch on new motherboard.
9. Reverse removal procedure to install new motherboard, making sure locating pins are aligned in holes in logic frame. **Before tightening the four screws holding motherboard, install a PCB at each end of the logic gate.**

#### 4.6.8.4 Replacing Read/Write Preampifier

1. Position air exhaust housing to allow access to preampifier.
2. Remove preampifier covers.

3. Remove head plug clamps.
4. Remove head plugs.
5. Loosen captive screw holding paddle card to cam tower, and unplug paddle card.
6. Loosen all three captive screws holding R/W preamplifier to cam tower.
7. Slide PCB out of slot near center of cam tower.

**To install:**

8. Reverse removal procedure.
9. To provide a good ground, tighten paddle card screws with a screwdriver.

**4.6.8.5 Replacing Servo Power Amplifier**

1. Tag and remove wires from power amplifier lower terminal block. Remove cable clamp.
2. Tag and remove wires from power amplifier upper terminal block. Remove cable clamp.
3. Disconnect PCB cable connector.
4. Remove power amplifier from drive.
5. To install a servo power amplifier, reverse the removal procedure above.

**4.6.8.6 Replacing Servo Preamplifier**

1. Position air exhaust housing to gain access to servo preamplifier.
2. Loosen cover screw, and remove cover.

3. Remove servo head plug.
4. Loosen captive screw holding PCB to deck plate.
5. Pull up on PCB to remove.

**To install:**

6. Reverse the removal procedure.
7. Tighten captive screw on PCB with a screwdriver to provide a good ground.

**4.6.8.7 Replacing Read/Write Preamplifier Cable**

Replace this cable as follows (refer to Figure 4-25):

1. Remove operator control panel.
2. Remove all four screws holding curved cable clamp underneath operator control panel.
3. Pull PCB in location D18 halfway out, remove both screws from piggyback connector, and remove connector from PCB. Reinsert PCB.
4. Unplug R/W paddle card from logic assembly.
5. Remove screws holding metal cable guide located on the deck plate right side (when viewed from front of drive).
6. Loosen cable clamps on top of cam tower and clamp below deck plate near absolute filter.
7. Loosen captive screws holding both R/W paddle cards to cam tower.
8. Remove servo preamplifier cover, servo head plug, and loosen captive screw on servo preamplifier. Remove preamplifier PCB.
9. Unplug connectors for tachometer and up-speed switch.

- Remove screws from servo preamplifier guide frame, which holds bracket containing servo preamplifier connector, and jacks disconnected in preceding step 9.

**NOTE**

The screws removed in this step pass through standoffs. Catch the standoffs as the screws are withdrawn.

- Loosen captive screws holding both R/W paddle cards to cam towers, and remove paddle cards from cam towers.
- Remove both screws from cable clamp attached to module center baffle plate.

**NOTE**

The exact routing of this cable should be noted before removal so that it can be reinstalled with the same routing.

- Remove R/W cable from drive by feeding cable up through the hole underneath operator control panel. Take care that paddle cards, brackets, etc. do not snag on drive mechanism and cause damage to cable assembly or drive mechanism.

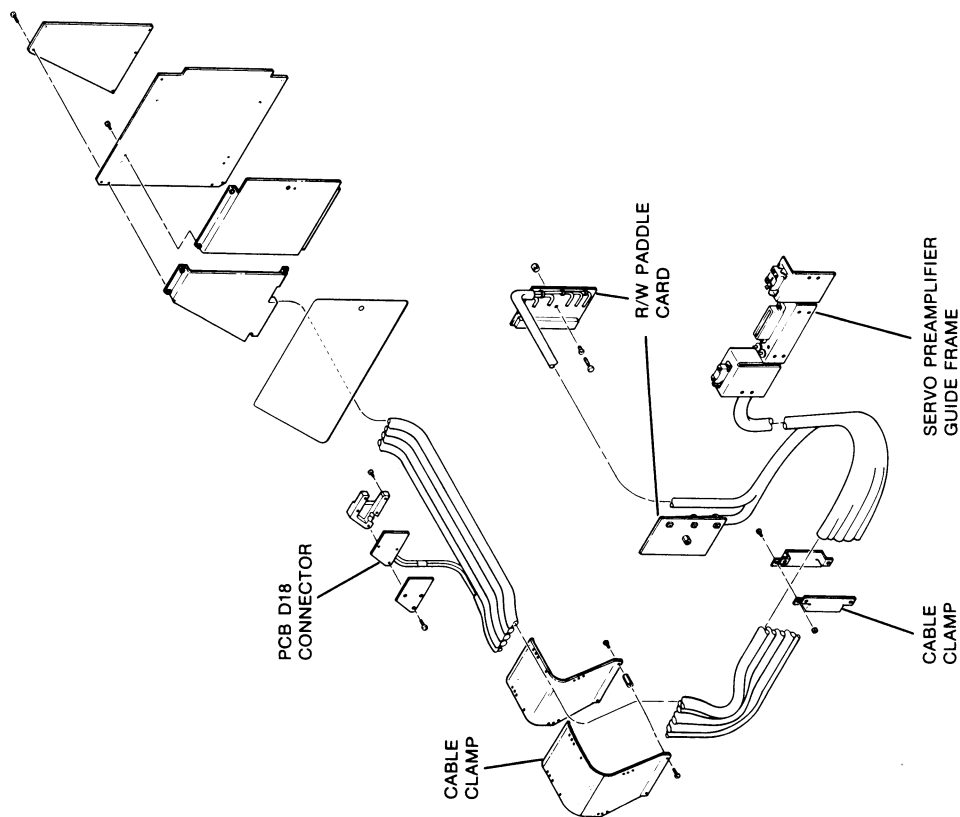
**To install an R/W preamplifier cable:**

- Reverse removal procedure.

**NOTE**

To provide good grounds for R/W and servo functions, tighten both preamplifier paddle-card clamp screws with a screwdriver (see item 7 above).

- Feed cable down through hole underneath operator control panel.



**FIGURE 4-25. R/W PREAMP CABLE ROUTING**



#### 4.6.8.8 Replacing Power Supply

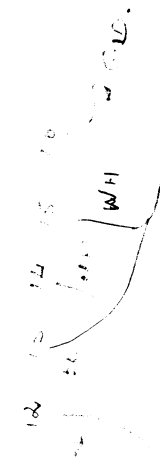
Replacing the entire power supply is accomplished with the drive in line with the customer subsystem, by a single FE in about 30-45 minutes using the procedure below. The only tools required are a small (4") crescent wrench and screwdriver.

#### NOTE

Many wires are disconnected to remove the power supply. All wires are tagged, each with a number indicating its correct terminal-number connection. Replace each wire only after checking that wire and terminal numbers are the same.

1. Verify that all power to the drive is off.
2. Remove the front cover by opening it, pulling the quick-disconnect ground lug (near top hinge), and lifting the cover off its hinges.
3. Disconnect the air duct from the shroud, by loosening the screw in the hose clamp and pulling down.
4. Remove the absolute filter and flexible air duct as a unit. Lift the filter retaining clips up for the first inch of travel, then slide the filter out.
5. Remove the transparent plastic cover over the RF filter (FL300), by removing two nuts with a small crescent wrench. The RF filter is located at the rear of the power supply, on the right side when viewing through the front of the drive.
6. Remove the two wires (one white, other black) from terminals on the RF filter's **right** side.
7. Remove two screws below RF filter, holding power supply to cabinet floor.
8. Remove PDU cover.
9. Remove five wires (from power supply fan) from terminals 12-16 on TB100 in PDU.

10. Remove the drive's rear cover by opening it, pulling the quick-disconnect ground lug (near top hinge), and lifting the cover off its hinges.
11. Remove two screws at the bottom left which hold the control panel (fuse panel) to cabinet floor.
12. Remove power supply cover.
13. Remove cable guard from control panel.
14. Remove two strain-relief cable clamps from front of servo power amp (SAMP).
15. Remove three wires from terminals 2,3,4 on TB200 (front of SAMP), and the ground wire directly above the terminal board.
16. Slide the SAMP module about half way out. Locate J200 (long connector) in the SAMP printed circuit board, and pull it out. Slide the module back in.
17. Remove the plastic guard over terminal strip on the transformer, and remove all transformer wires.
18. Remove the output cable from each Regulator printed circuit board (total of four PCBs), by sliding the PCB about half way out of the power supply and using the crescent wrench.
19. Remove three wires from terminals 11,12,13 on TB304.
20. Remove ground connections to deck plate, by removing one screw in the deck plate's rear lower left corner.
21. Notice that output cables from Regulator PCBs (cables are tied together) pass under a horizontal frame member, and the cables interfere with sliding out the power supply. Clear the way for sliding out by feeding the cables up and under the frame member.
22. Verify all cables from the power supply (front and rear) are disconnected, then slide it all the way out.
23. Install the replacement power supply as follows:
  - a. Slide the power supply into the drive.

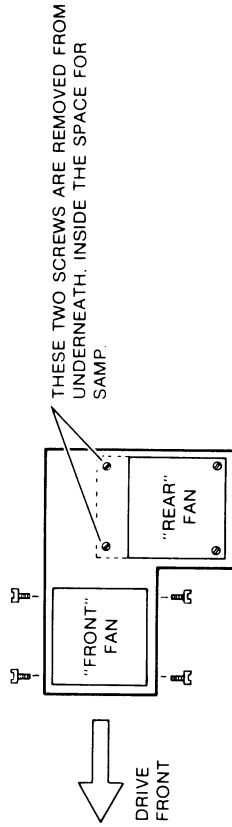


- b. Feed output cables for the Regulator PCBs down and under the horizontal frame member. To increase clearance for feeding cables, push the power supply a few inches further into the drive.
- c. Move power supply to line up screw holes in cabinet floor with slots for control panel screws. Replace and hand tighten the two screws.
- d. Connect all transformer wires to terminal strip on transformer. Each wire is number coded against terminal number. After verifying correct hookup, replace plastic guard over terminal strip.
- e. Connect each output cable to its appropriate Regulator PCB (total of four), by sliding the PCB half way out and using the crescent wrench. Each wire in an output cable is number coded. The length and bend of cable wires identify corresponding PCBs.
- f. Connect three wires to terminals 11,12,13 on TB304. Wires are number coded against terminal numbers.
- g. Connect three wires to terminals 2,3,4 on TB200, and the ground wire directly above the terminal board.
- h. Slide the SAMP module about half way out, and plug the wire with connector J200 into the SAMP printed circuit board. Slide the module back in.
- i. Replace two strain-relief cable clamps into front of SAMP.
- j. Replace ground connection to lower left corner of deck plate. Two wires are grounded into the deck plate using one screw and star washer. Be sure to make a good ground by locating the washer against the deck plate.
- k. Working through the front of the drive, replace two screws holding power supply to cabinet floor. Holes in the power supply are slotted, and located below the RF filter. Line up by moving the power supply, and tighten the screws.
- l. Connect power supply fan to PDU by connecting five wires to terminals 12-16 on TB100.
- m. Connect PDU with power supply by connecting two wires to two terminals on the RF filter's right side. The white wire connects to the top terminal, and the black wire connects to the lower terminal.
- n. Replace transparent plastic cover over RF filter.
- o. Replace PDU cover.

- p. Replace the absolute filter and air duct. Connect the air duct to the shroud by tightening the clamp.
  - q. Replace front cover by reversing step 2 above.
  - r. Working at the rear of the drive, replace cable guard over control panel.
  - s. Tighten two screws holding control panel to cabinet floor.
24. Return drive to operating condition by following procedures in SECTION 2 (Installation and Operation), paragraphs 2.3.5 through 2.3.10.

#### 4.6.8.9 Replacing Power Supply Fan

1. Prepare to slide out the power supply by performing the procedure in paragraph 4.6.8.8, steps 1 through 21.
2. There are two fans under the power supply, as shown in the sketch below of the underside of the power supply. If the "front" fan is to be replaced, slide out the SAMP module. If only the "rear" fan is to be replaced, skip this step.



3. Verify all cables from the power supply (front and rear) are disconnected, then slide it all the way out and place on the floor, topside down.
4. Referring to the sketch above, remove four screws retaining fan to be replaced, and pull out its power plug. Plug in the replacement fan, and install using the four screws.
5. Slide the power supply into the drive. If SAMP was removed, replace it being sure to slide along the two plastic runners.
6. Complete the installation of the power supply using the procedure in paragraph 4.6.8.8, step 23, items b through u.

## 4.6.9 Power Conversion

### NOTE

Following any frequency conversion, be sure to check power supply voltages both at the transformer primary and secondary windings and at regulator outputs.

### 4.6.9.1 50 Hz to 60 Hz Conversion

Materials needed are P/N 210626 (Drive Motor Assembly, 60 Hz) and P/N 200230 (Belt, Endless, Flat, 60 Hz). The conversion procedure follows:

1. Replace drive motor as described in paragraph 4.6.6.2.
2. Replace drive belt as described in paragraph 4.6.6.4.
3. Verify that the Power Conversion Plug Assembly P/N 215766 (shown in Figure 2-8 and the *Illustrated Parts Catalog*, Figure 2-83) has the PHASE TO PHASE connector installed (shown as P110 in *Logic Manual*, page ZA100).

4. Determine the phase-to-phase voltage of the power source, and move power supply leads to appropriate terminals of TB319 on transformer (refer to *Logic Manual*, page ZD100).

### 4.6.9.2 60 Hz to 50 Hz Conversion

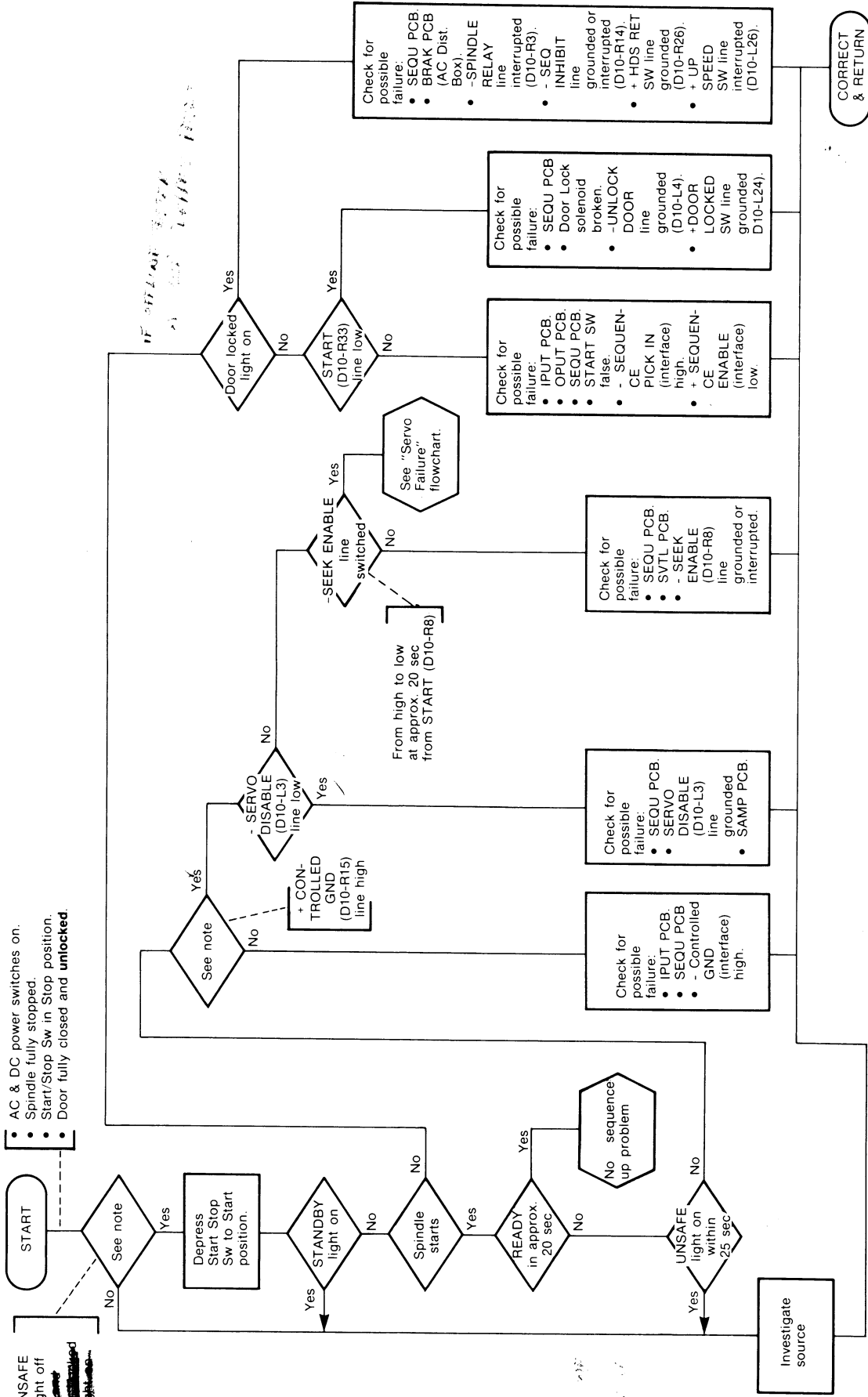
Materials needed are P/N 211680 (Drive Motor Assembly, 50 Hz) and P/N 211672 (Belt, Endless, Flat, 50 Hz). The conversion procedure follows:

1. Replace drive motor as described in paragraph 4.6.6.2.
2. Replace drive belt as described in paragraph 4.6.6.4.
3. Determine if power source is WYE or DELTA configured. Locate the Power Conversion Plug P/N 215766 (shown in Figure 2-8 and the *Illustrated Parts Catalog*, Figure 2-83). If source is DELTA, install the PHASE TO PHASE plug. If source is WYE, install the PHASE TO NEUTRAL plug. (Refer to P110 in *Logic Manual*, page ZA100.)
4. Determine the phase-to-phase voltage of power source if DELTA configured, or the phase-to-neutral voltage if WYE configured, and move power supply leads to appropriate terminals of TB319 on transformer (refer to *Logic Manual*, page ZD100).

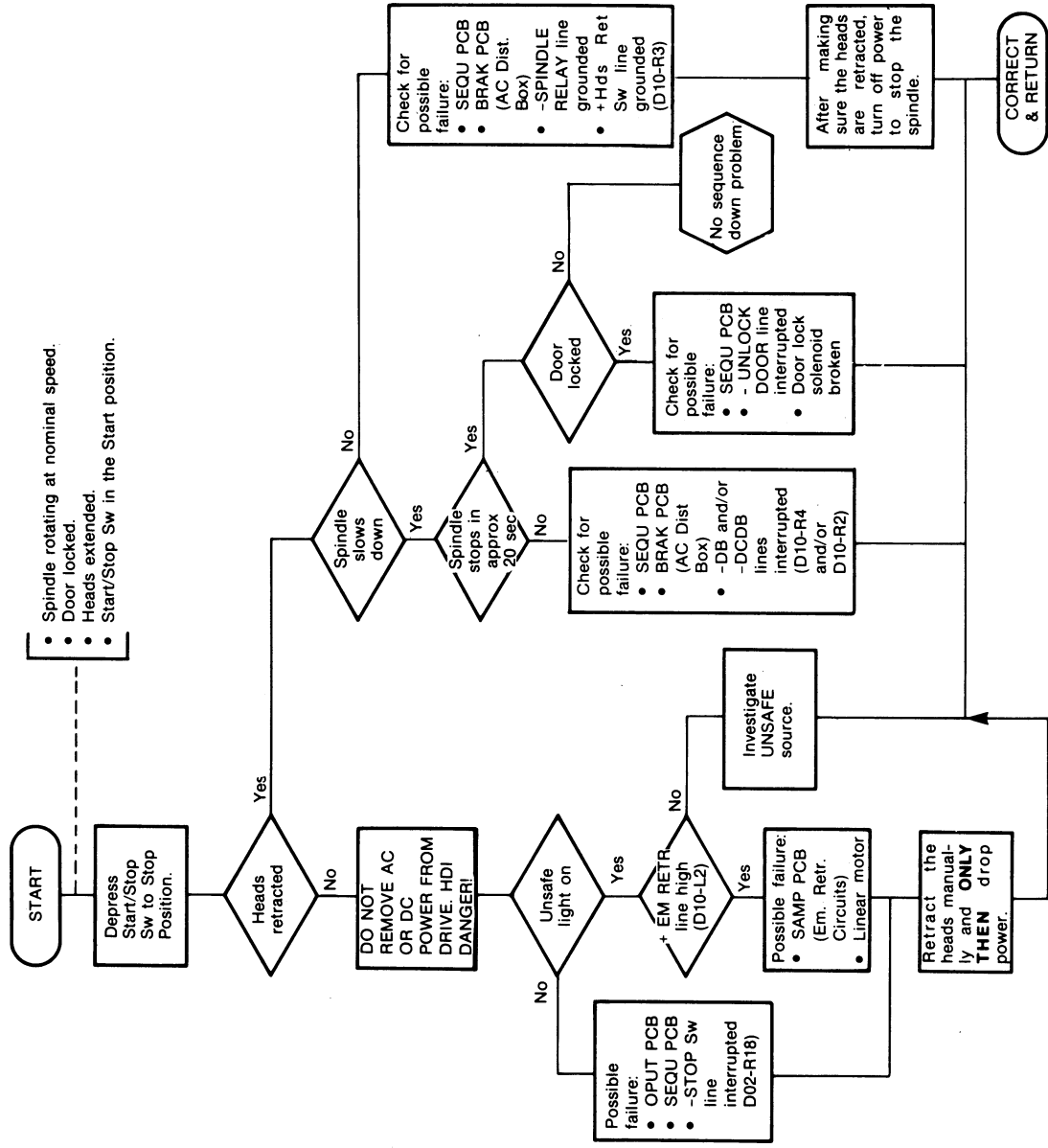


**APPENDIX A**  
**FAULT ISOLATION PROCEDURES (FLOWCHARTS)**

# Sequence Up and Head Launch Failure

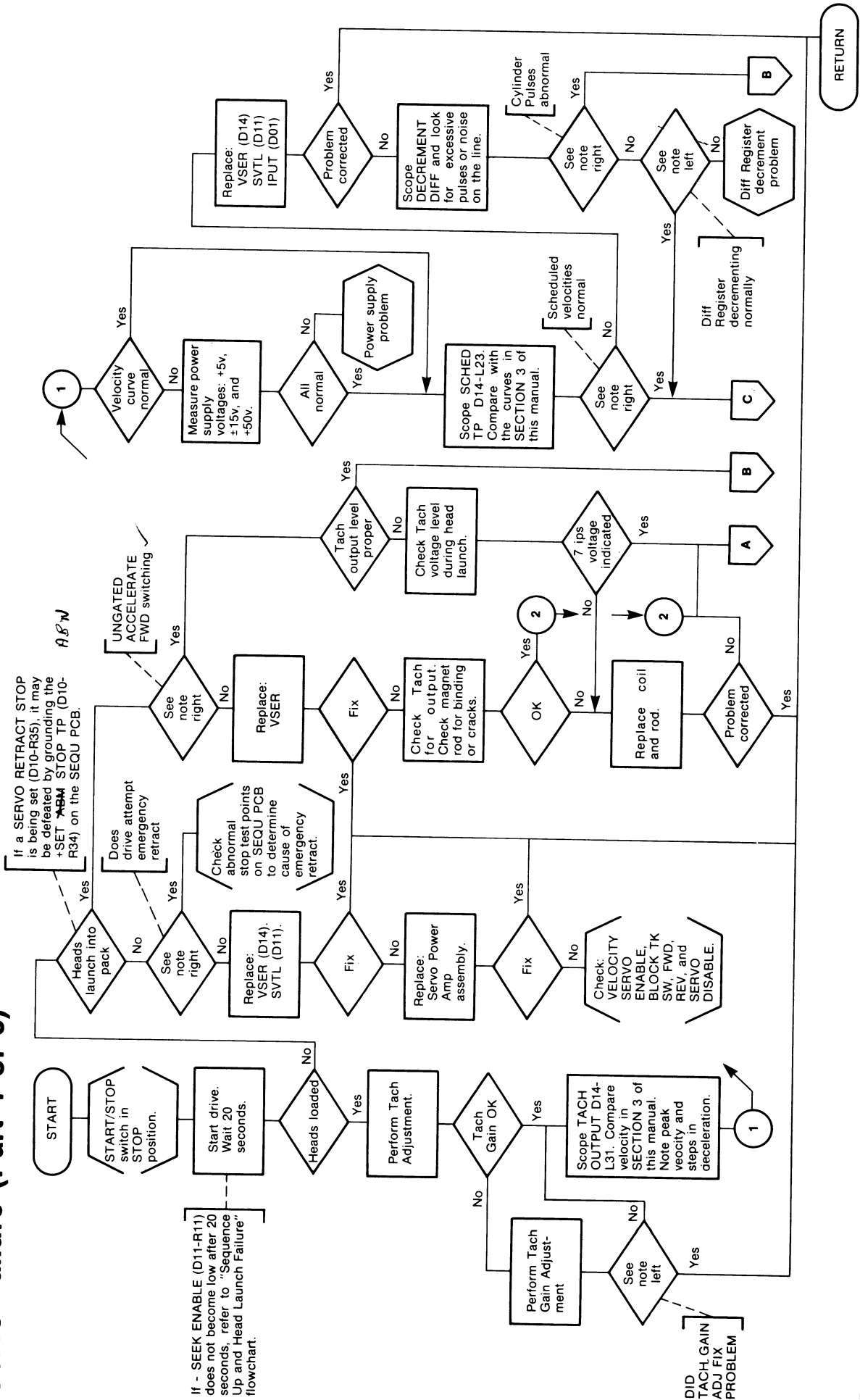


# Sequence Down Failure



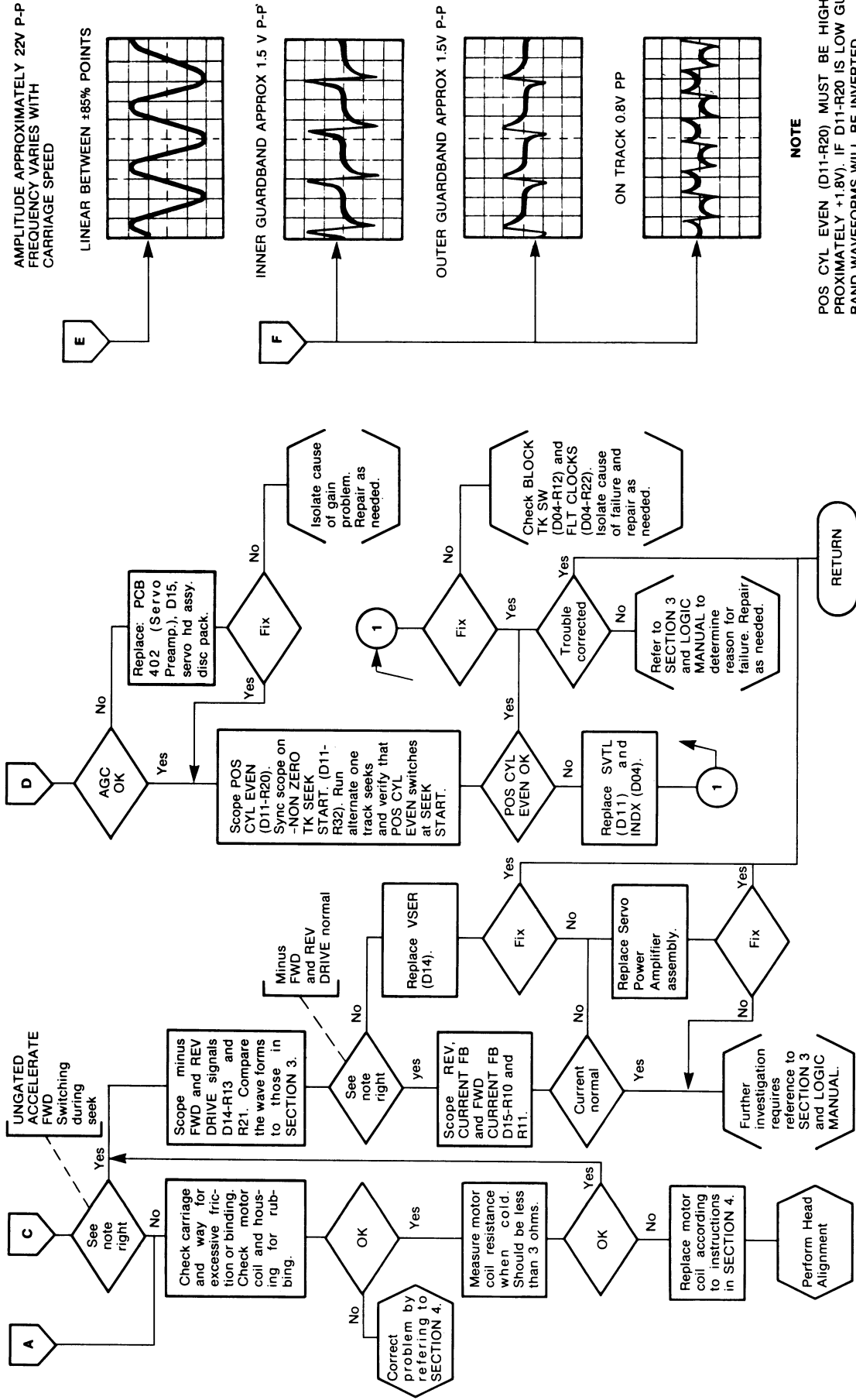
- Spindle rotating at nominal speed.
- Door locked.
- Heads extended.
- Start/Stop Sw in the Start position.

# Servo Failure (Part 1 of 3)





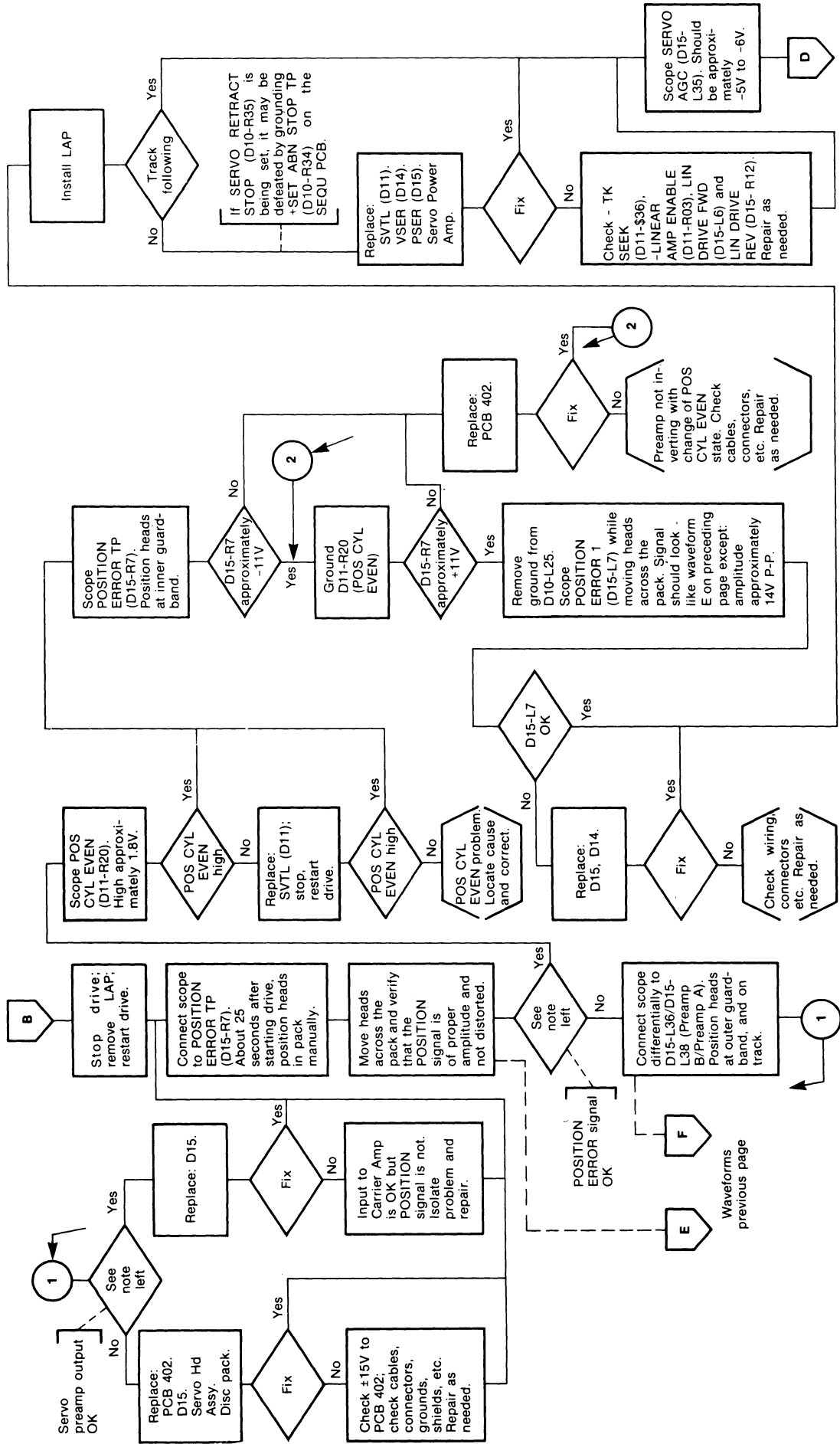
# Servo Failure (Part 2 of 3)



**NOTE**

POS CYL EVEN (D11-R20) MUST BE HIGH (APPROXIMATELY +1.8V). IF D11-R20 IS LOW GUARDBAND WAVEFORMS WILL BE INVERTED.

# Servo Failure (Part 3 of 3)



## APPENDIX B

### MEMOREX 800 DISC STORAGE SUBSYSTEM TESTER

The Memorex 800 Tester is designed to verify the following functions of the 677 OEM Disc Drive.

	FUNCTION #	OPERATION
• Wrap	0	EXECUTE ROUTINE
• Incremental Seek	1	SET ROUTINE #
• Alternate Seek	*	WRITE DATA INTO SELECTED
• Random Seek	2	BYTE
• Tachometer Gain	3	SET BYTE ADDRESS (FROM DATA
• Head Alignment	3	SW)
• Head Alignment Verification	*	READ DATA FROM SELECTED
• Head Alignment Track Seek	4	BYTE
• Write/Read Verification	5	SET DESIRED RUN (FROM
• Incremental Offset Read	6	ADVANCE HEAD ADDR ON
• Read Track 65,535 Times	6	EXECUTE TOUCH
• Read/Write Safety	6	
• Offset	*	BYTE ADDRESS INCREMENTED ON EXECUTE SW
• Index		
• Display Drive Output Bytes		
• Recalibrate		
• Write		

#### B.1 INSTALLATION

Before connecting the tester to a 677 drive, insert the tester's power cord into a 115-VAC 50/60 Hz power source and run the tester's internal diagnostics (Routine 00) to ensure that the tester is operating correctly. The following procedure outlines the steps required to connect the 800 Tester to the 677 OEM Disc Drive.

1. Disconnect the 677 drive from the DCL by removing the four (4) flat input/output cables marked A, B, C, and D from the IPUT and OPUT PCBs in the 677 drive. Cables A and B from the tester are then connected to edge-card connectors A and B of the IPUT PCB; cables C and D are connected to edge-card connectors C and D of the OPUT PCB.
2. Mount a Scratch disc pack on the drive. Do not use a CE pack or a data pack. Routine 8 (Write/Read Verification) and routine 13 (Write) overlay a one-byte bit pattern from index to index on the specified cylinder. The default bit pattern is DB and cylinder zero is the default cylinder.
3. If the Head Alignment feature is installed in the tester, insert the Head Alignment cable into the drive in connector location B04 (see Section B.3.2) before running Head Alignment diagnostic routines.
4. Press the RESET switch on the tester. All LED displays should come on.

5. Release the RESET switch and note that all LED displays are off.
6. Set the DC and AC power circuit breakers in the drive to the ON position. Apply power to the 677 drive by placing the ON/OFF switch to the ON position.
7. Press the START switch on the drive.

DRIVE STARTS & COMES UP TO SPEED BUT DOES NOT LOAD HEAVY.

## B.2 OPERATION

The 800 Tester provides the user with a variety of diagnostic routines to test the 677 drive. The following paragraphs describe the run options, operating procedure, and purpose of each routine.

### B.2.1 Wrap Test—Routine 00

The purpose of the Wrap routine is to check the I/OP board on the tester and the connector cables from it to the drive. Before running the Wrap test, a special four-way plugboard, provided with the tester, must be connected to the four I/O cables in the tester. (See Figure B-1).

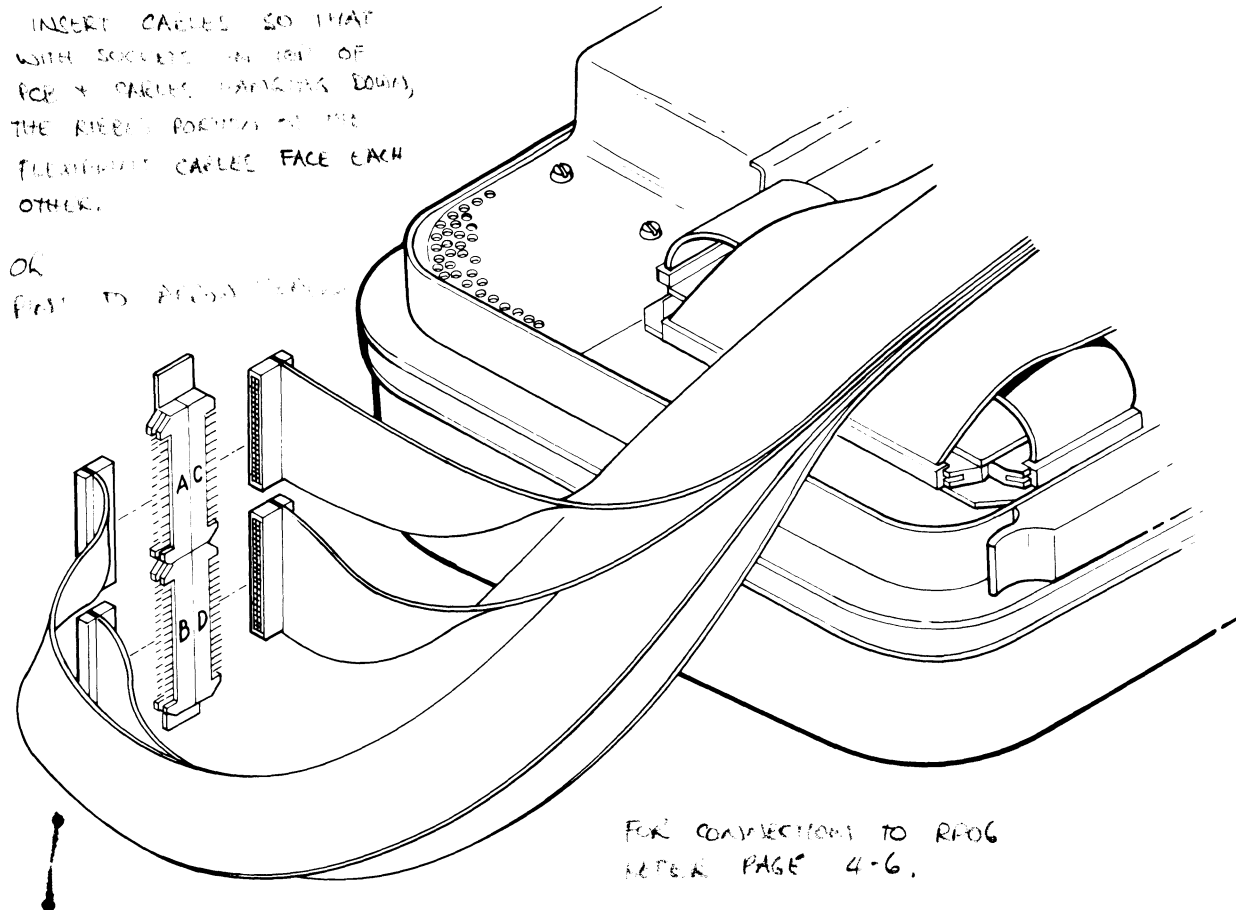


FIGURE B-1. TESTER WITH WRAP PLUGBOARD

The routine can be run with the following run options.

= 00 RUN 1 PASS ONLY

Error Control = 01 Loop on pass.

= 02 Loop on error.

1. Set 00 in the DATA switches.
2. Select 1 on the FUNCTION switch.
3. Press the EXECUTE switch. (No LEDs should be on in the INFORMATION Display area of the control panel.)
4. Set the desired run option (01 or 02) in the DATA switches.
5. Select 5 on the FUNCTION switch.
6. Press the EXECUTE switch.
7. Select 0 on the FUNCTION switch.
8. Press the EXECUTE switch.
9. The microdiagnostic routine will now run as specified by the selected run option (step 4).

If no error occurs, the INFORMATION Display area will indicate "FF" (SDSD/NORMAL switch must be in the NORMAL position) and the ERROR CODE indicator will come on since "FF" is the error code indicating "test completion". If an error occurs, an error code in the range "10" to "1F" is displayed in the INFORMATION Display area and the ERROR CODE indicator will light.

To find the error bit(s), set the Error Control to loop on error (02). Set the SYNC Address switches to 0089 and the SDSD/NORMAL switch to the SDSD position. The INFORMATION Display area will indicate the error bit(s). Compare the error bit(s) with those in Table B-1 and replace the most probable failing cable(s). If the error persists after replacing the suspected cable(s), assume the I/O PCB is bad and replace it.

### **B.2.2 Incremental Seek—Routine 01**

The purpose of the Incremental Seek routine is to verify that the drive can seek incrementally from cylinder zero to cylinder 814 (677-01) or to cylinder 410 (677-51) and then back to cylinder zero. This cycle is repeated until it is stopped by pressing the EXECUTE switch while the routine is running or an error is encountered during the seeks.

The routine can be run with the following run options.

Error Control = 01 Run continuously and stop on error (default).

= 02 Loop on error.

**TABLE B-1. ERROR CODES FOR WRAP TEST (ROUTINE 00)**

<b>Error Code</b>	<b>Error Bits</b>	<b>Possible Failing Cable(s)</b>
10 or 18	Bit 2 Bit 3, 5 Bit 4, 6, 7	B A or D A or C
11 or 19	Bit 1-3 Bit 5, 6 Bit 7	B or D A or D A or C
12 or 1A	Bit 1 Bit 3-7	A or D B or D
13 or 1B	Bit 2-5 Bit 7	B or C B or D
15 or 1D	Bit 1-7	A or C
16 or 1E	Bit 2-7	B or C
17 or 1F	Bit 1, 3-5, 7 Bit 2, 6	A or C B or C

1. Set 01 in the DATA switches.
2. Select 1 on the FUNCTION switch.
3. Press the EXECUTE switch. The 0 bit on the INFORMATION Display should light indicating Routine 01.
4. Set the desired run option (02 = loop on error) in the DATA switches (see Note).
5. Select 5 on the FUNCTION switch (see Note).
6. Press the EXECUTE switch (see Note).
7. Select 0 on the FUNCTION switch.
8. Press the EXECUTE switch.
9. The microdiagnostic routine will cause the drive to seek incrementally.

If no seek error occurs, the INFORMATION Display area continues to indicate the routine number (SDSD/NORMAL switch in NORMAL position) and the RUNNING LED is on. If an error occurs, the error code is displayed in the INFORMATION Display area and the ERROR CODE LED comes on.

#### NOTE

Steps 4, 5 and 6 are optional steps which are performed to select an Error Control run option other than the default option.

This is an example of a routine which uses run options that are entered with the FUNCTION and DATA switches. The procedure given above should be used to execute any other routines which require run options to be entered.

### B.2.3 Alternate Seek—Routine 02

This microdiagnostic routine performs alternate seeks between any two cylinders. The specified cylinders are between cylinder zero and cylinder 814 for 677-01, and between cylinder zero and cylinder 410 for 677-51.

The routine has the following run options.

Error Control = 01 Alternate seek; Stop on error (default).

= 02 Loop on error.

The cylinder addresses are selected by entering the parameter data byte in the DATA switches with the FUNCTION switch set to 2. Bytes are defined as follows.

Byte No.

- |    |   |
|----|---|
| 00 | High order inner cylinder 00-03 (Hex Range for 677-01) or<br>00-01 (Hex Range for 677-51) |
| 01 | Low order inner cylinder 00-FF (Hex Range)  |
| 02 | High order outer cylinder 00-03 (Hex Range for 677-01) or<br>00-01 (Hex Range for 677-51) |
| 03 | Low order outer cylinder 00-FF (Hex Range)  |

**NOTE:** Maximum cylinder address is 032E (677-01) or 019A (677-51).

1. Set 02 in the DATA switches.
2. Set the FUNCTION switch to 1.
3. Press the EXECUTE switch. The INFORMATION Display should light indicating 02.

4. Set the DATA switches to YY (YY is the high order byte of the first cylinder to be selected as defined above for Byte No. 00).

**CAUTION**

The byte number points to byte 00 after each routine number is entered. The byte number automatically increments and points to the next byte **after** an operation (display or change contents) is performed. Therefore, if the byte number to be operated on is not byte number 00, the byte number that is to be operated on must be entered. Set the desired byte number as follows:

1. Set the DATA switches to the desired byte number.
2. Set the FUNCTION switch to 3.
3. Press the EXECUTE switch.
5. Set the FUNCTION switch to 2.
6. Press the EXECUTE switch.
7. Set the DATA switches to ZZ (ZZ is the low order byte of the first cylinder to be selected as defined above for Byte No. 01).
8. Set the FUNCTION switch to 2.
9. Press the EXECUTE switch.
10. Repeat steps 4 through 9 to select the second cylinder address which is defined above as Byte No. 02 and Byte No. 03. (Byte numbers 02 and 03 default to 00.)

**EXAMPLE:** If YY = 01 and ZZ = 02, the selected cylinder address is 258.

$$YY = \frac{0}{0000} \frac{1}{0001} \quad ZZ = \frac{0}{0000} \frac{2}{0010}$$

Binary Bit  
Significance  
Values

32K	16K	8K	4K	2K	1K	512	256	128	64	32	16	8	4	2	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0
0				1				0				2			

$$\text{Cylinder address} = 256 + 2 = 258$$

11. Set the DATA switches to 02 or the desired Error Control run option as defined above (see Note on page B-5).
12. Set the FUNCTION switch to 5 (see Note on page B-5).
13. Press the EXECUTE switch (see Note on page B-5).
14. Set the FUNCTION switch to 0.



15. Press the EXECUTE switch.
16. The routine will start to execute and cause the drive to seek between the cylinder addresses defined in the above procedure. To stop the test, press the EXECUTE switch. To change cylinder addresses for the seek operation, select the byte(s) containing the cylinder address to be changed, repeat steps 4 through 9 as applicable, and then steps 11 through 16.

### **B.2.4 Random Seek—Routine 03**

This microdiagnostic routine performs random seeks.

The following run options apply:

- Error Control = 01 Run continuously and stop on error (default).
- = 02 Loop on error.

The procedure to initiate the Random Seek test is identical to the procedure given in *Section B.2.2, Incremental Seek—Routine 01*, except that 03 is set in the DATA switches (step 1).

### **B.2.5 Tachometer Gain Adjustment—Routine 04**

This microdiagnostic routine performs seeks between cylinder zero and cylinder 600 on the 677-01 or between cylinder zero and cylinder 300 on the 677-51 (decimal range).

The following run options apply:

- Error Control = 00 Verify Tach Gain (no link)
- = 01 Adjustment mode.
- = 02 Loop on error.
- = 80 Verify Tach Gain and link (default)

With the exception of the routine number and the error control options, the procedure to initiate this routine is the same as the procedure given in *Section B.2.2*.

### **B.2.6 Head Alignment—Routine 05**

#### **NOTE**

A Head Alignment Unit or the Head Alignment feature on the tester is required to run this routine (see *Section B.3*).

F - 0  
1-5  
0-0  
6-0

The Head Alignment microdiagnostic routine seeks to the head alignment cylinder defined by the operator (by default, seeks to cylinder 496 on the 677-01 or seeks to cylinder 245 on the 677-51) and then gates the alignment signal to the Head Alignment Unit.

The run options for this routine are:

Error Control = 01 Run continuously and stop on error (default)  
= 02 Loop on error.

Byte No.

00 High order cylinder address 00-03 (Hex Range for 677-01)  
00-01 (Hex Range for 677-51)  
01 Low order cylinder address 00-FF (Hex Range)

**NOTE:** Maximum cylinder address is 032E (677-01) or 019A (677-51).

This routine is initiated in the same manner as the procedure given in *Section B.2.3, Alternate Seek—Routine 02*, **except** that only one cylinder address is required.

**NOTE**

Head zero (Display 00) is selected initially while the routine is running. Heads can be advanced by positioning the FUNCTION switch to position 6 and pressing the EXECUTE switch.

### **B.2.7 Head Alignment Verification—Routine 06**

**NOTE**

A Head Alignment Unit or the Head Alignment feature on the tester is required to run this routine (see *Section B.3*).

The Head Alignment Verification routine verifies the alignment of all heads.

The following run options apply:

Error Control = 00 Verify mode (default).  
= 02 Loop on error.

To initiate this routine, use the procedure in *Section B.2.2*.

**NOTE**

Before running Routine 06, execute Routine 07, Head Alignment Track Seek, to seek to the head alignment cylinder (496 decimal (for 677-01) or 245 decimal (for 677-51) on CE disc pack). Warm up the drive for 20 minutes to stabilize the heads and then run Routine 06.

## B.2.8 Head Alignment Track Seek—Routine 07

Routine 07 seeks to the head alignment cylinder specified by the operator (defaults to cylinder 496 on 677-01 and to cylinder 245 on 677-51).

### NOTE

Before running Routine 06, Head Alignment Verification, run this routine to seek to the head alignment cylinder and then warm up the drive for 20 minutes. Connect a Head Alignment Unit, or the Head Alignment feature on the tester, to location B04 on the drive before running this routine (see *Section B.3, Head Alignment Checks*).

The following run options apply:

Error Control = 00 Run once and stop (default)

= 02 Loop on error

To initiate this routine, use the procedure given in *Section B.2.3*.

## B.2.9 Write/Read Verification—Routine 08 DESTROYED PAGE REFORMATTING

The Write/Read Verification routine writes a one-byte data pattern using all heads of a cylinder and then it reads back the data pattern to verify the write process. The data pattern is read back on track first, and then + offset (+300 microinches on 677-01 or +600 microinches on 677-51) is read and finally reverse offset (-300 microinches on 677-01 or -600 microinches on 677-51).

The following run options apply:

Error Control = 00 Write all heads of cylinder and then stop (default).

= 02 Loop on error.

Byte No.

00 High order cylinder 00-03 (Hex Range for the 677-01) or  
00-01 (Hex Range for the 677-51)

01 Low order cylinder 00-FF (Hex Range)

03 Data pattern to be written 01-FF (Hex Range). (Defaults to DB pattern.)

**NOTE:** Maximum cylinder address is 032E (677-01) or 019A (677-51).

To initiate this routine, use the procedure given in *Section B.2.3*.

MOST HAVE WRITTEN ELEMENT CYL , TRACK 4 DATA  
PREVIOUSLY - ROUTINE 08

### B.2.10 Incremental Offset Read—Routine 09

The Incremental Offset Read routine reads data with a head specified by the operator and compares this data with the expected data pattern. The routine then increases the offset by 25 microinches and reads and compares again. The read operation stops whenever an error (unsafe or data miscompare) is encountered or when the offset reaches -300 microinches on the 677-01 (-600 microinches on the 677-51).

The following run options apply:

Error Control = 00 Run routine once and then stop (default).

= 01 Read continuously and stop on error.

= 02 Loop on error.

Byte No.

00 High order cylinder 00-03 (Hex Range for 677-01) or  
00-01 (Hex Range for 677-51)

01 Low order cylinder 00-FF (Hex Range)

02 Head to be selected 00-12 (Hex Range)

03 Data pattern to be compared 01-FF (Hex Range). (Defaults to DB pattern.)

**NOTE:** Maximum cylinder address is 032E (677-01) or 019A (677-51).

Use the procedure in *Section B.2.3* to initiate this routine.

### B.2.11 Read Track 65K Times (Errors Monitored)—Routine 0A

This routine performs 65,535 reads of one track with a specified head. It also monitors read errors if any occur.

The following run options apply:

Error Control = 01 Read track 65,535 times and then stop (default).

= 02 Loop on error.

Byte No.

00 High order cylinder 00-03 (Hex Range for 677-01) or  
00-01 (Hex Range for 677-51)

01 Low order cylinder 00-FF (Hex Range)

02 Head to be selected 00-12 (Hex Range)

03 Data pattern to be compared 01-FF (Hex Range)

04 Amount of offset desired ± 775 micrometers (Decimal Range)

# OF 25µ" STEPS  
PAGE 233  
21 STEPS = 775µ"  
37µ" = 15 HEX

**NOTE:** Maximum cylinder address is 032E (677-01) or 019A (677-51).

Use the procedure in Section B.2.3 to initiate this routine.

### B.2.12 Read/Write Safety—Routine 0B

This routine sets and resets the safety latches (AC Write Unsafe, Transition Unsafe, Write and Offset, and No Head Select) to ensure that they are functioning correctly.

The following run options apply:

- Error Control = 00 Check latches once (no link).
- = 02 Loop on error.
- = 80 Check latches once and link (default)

Use the procedure in Section B.2.2 to initiate this routine.

### B.2.13 Offset—Routine 0D

This routine commands the drive to offset and then checks the signal ON TRACK to ensure that it goes away after the offset operation.

The following run options apply:

- Error Control = 00 Run once and stop (no link).
- = 01 Run continuously and stop on error.
- = 02 Loop on error.
- = 80 Run once and link (default)

Use the procedure in Section B.2.2 to initiate this routine.

### B.2.14 Index—Routine 10

This routine checks for the period of index on track and also in offset.

The following run options apply:

- Error Control = 00 Run once (no link).
- = 01 Run continuously and stop on error
- = 02 Loop on error.

*NOTE: There may be a few µs with the pulse.  
If the pulse is RPS1 NOT R1 will run and free the RPS1 00  
and more at command  
at RPS1 01*

1.2.

= 80 Run once and link (default)

Use the procedure in *Section B.2.2* to initiate this routine.

### B.2.15 Display Drive Output Bytes—Routine 11

This routine reads the drive's output lines (8 bits at a time) and sends the status of the drive's output lines to the INFORMATION Display area on the control panel. The desired output byte that is to be displayed may be specified by the operator by loading the byte number into parameter byte #00; otherwise, output byte #00 is displayed (default). After displaying an output byte, the output byte pointer points to the next output byte to be displayed. When the output byte pointer overflows, the pointer points to output byte #00.

The displayed output bytes are defined as follows:

8	4	2	1	8	4	2	1
80	40	20	10	8	4	2	X

X = not used

#### Output Byte #00

- 2 — -RP06
- 4 — Sequence enable
- 8 — Online
- 10 — File ready
- 20 — Seek incomplete
- 40 — Offset ready
- 80 — Sequence pick out

#### Output Byte #01

- 2 — Servo data
- 4 — Index Pulse
- 8 — On track
- 10 — Not used
- 20 — Sign
- 40 — Difference less than 32
- 80 — Index error

#### Output Byte #02

- 2 — Off cylinder
- 4 — Not used
- 8 — Reset register
- 10 — Difference equal to zero
- 20 — Velocity servo enable
- 40 — Stop velocity
- 80 — Coarse track

Output Byte #03

- 2 — Not used
- 4 — Head unsafe
- 8 — DC Write unsafe
- 10 — AC Write unsafe
- 20 — Abnormal stop
- 40 — Not used
- 80 — Unsafe

Output Byte #04

- 2 — Write ready unsafe
- 4 — Current sink fail
- 8 — Write select unsafe
- 10 — Current switch unsafe
- 20 — Write current unsafe
- 40 — Transitions unsafe
- 80 — Transitions detector failure

Output Byte #05

- 2 — DC unsafe
- 4 — PLO unsafe
- 8 — 35 V Regulator fail
- 10 — No head select
- 20 — Multi-head select
- 40 — Read and Write
- 80 — Write and Offset

Output Byte #06

- 2 — Write protect
- 4 — Plug enable
- 8 — Port B locked
- 10 — Port A locked
- 20 — Logical address 1 <
- 40 — Logical address 2 < DEPENDS ON V116
- 80 — Logical address 4 <

Use the procedure in *Section B.2.3* to initiate this routine.

### **B.2.16 Recalibrate—Routine 12**

This routine positions the servo mechanism on cylinder zero.

Error Control = 00 Run once (default)

= 02 Loop on error

Use the procedure in *Section B.2.2* to initiate this routine.

## B.2.17 Write—Routine 13

The Write routine writes a one-byte data pattern with all heads of a cylinder or with a single head defined by the operator.

The following run options apply:

- Error Control = 00 Write all heads or a specified head of cylinder and then stop (default).  
= 01 Write continuously and stop on error  
= 02 Loop on error.

Byte No.

- 00 High order cylinder 00-03 (Hex Range for 677-01) or 00-01 (Hex Range for 677-51)  
01 Low order cylinder 00-FF (Hex Range)  
02 Head to be selected 00-12 (Hex Range)  
03 Data pattern to be written 01-FF (Hex Range). (Defaults to DB pattern.)  
04 Head select option  
00 = All heads starting from the head specified in Byte No. 02 (default).  
8X = Single head. The selected head is specified in Byte No. 02.

**NOTE:** Maximum cylinder address is 032E (677-01) or 019A (677-51).

To initiate this routine, use the procedure given in *Section B.2.3*.

## B.3 HEAD ALIGNMENT CHECKS

### B.3.1 Tools Required

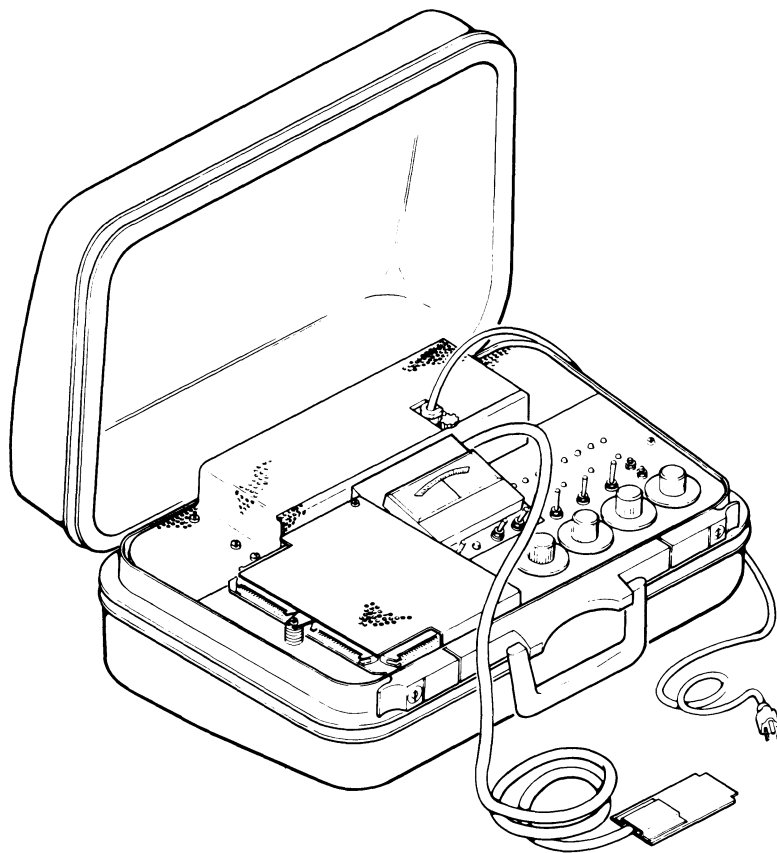
U Q

1. Memorex CE pack Mark X (100 megabyte) or Mark XI (200 megabyte) or equivalent.
2. Head Alignment Unit (PN 211292) or Head Alignment feature installed on tester. (See Figure B-2.)
3. Head Alignment Tool (PN 210106).
4. Head Torque Wrench (PN 210109).

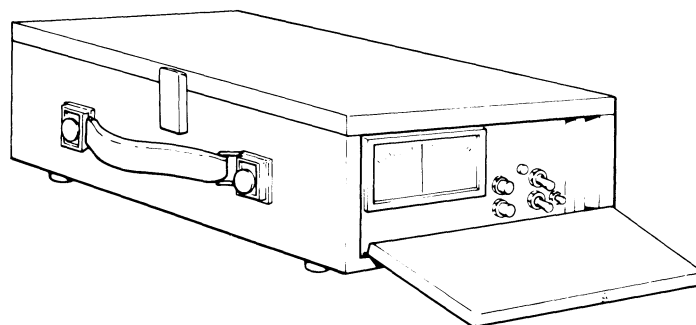
### B.3.2 Preliminary Steps

1. On the disc drive select READ ONLY drive mode, and install CE Disc Pack.
2. Slide logic assembly fully forward.
3. Turn off drive dc power.





**TESTER WITH HEAD ALIGNMENT FEATURE**



**HEAD ALIGNMENT UNIT (PN 211292)**

**FIGURE B-2. HEAD ALIGNMENT UNITS**

4. Connect Head Alignment Unit (PN 211292) interface cable or tester's Head Alignment cable to B04 slot of logic assembly.
5. Turn on dc power.
6. Press the CALIBRATE switch on the Head Alignment Unit or the tester's control panel to verify that the offsets in the head alignment circuits are within tolerance.
7. Verify that the head alignment unit's DATA INVALID lamp is lit.

### **B.3.3 Thermal Equilibrium Requirements**

Thermal equilibrium requirements must be established before head alignment or head alignment verification is attempted. Minimum requirements are as follows:

1. With the wind tunnel in the closed position, the drive must operate in a track-following or seek mode for at least 20 minutes. Any disc pack may be used for the first 15 minutes; however, the CE pack must be used during the last 5 minutes.
2. The CE pack must reach thermal equilibrium by either being in the computer room for one hour, or by being used during the entire 20 minute stabilization described in step 1 above.

### **B.3.4 Alignment Verification and Data Interpretation**

At the tester's operator panel, load Routine 07, Head Alignment Track Seek, (see *Section B.2.8*) with default parameters to seek to cylinder 496 (677-01) or 245 (677-51). Execute Routine 07.

The Head Alignment Unit or the Head Alignment feature on the tester indicates the presence or absence of valid data and the magnitude and direction of misalignment when valid data is present. The DATA INVALID indicator lamp indicates the former, and the MICROINCHES indicator, the latter.

When the DATA INVALID lamp is out, valid data is present. The MICROINCHES indicator indicates the selected data head alignment with respect to the servo head. An indication of 0 means the two heads are in perfect alignment. Deflection of the indicator in either direction indicates the number of microinches of misalignment. The direction of deflection indicates the direction in which the data head is misaligned with the servo head. A positive (right hand) indicator deflection means the data head is ahead of the servo head (offset toward spindle centerline), and a negative (left hand) deflection means it is behind the servo head (offset away from spindle centerline).

When the DATA INVALID lamp is lit, valid data is not present for one of the following reasons:

1. Fine Track signal is false.

2. Alignment Carrier signal is not present because:
  - a. CE disc pack is not loaded.
  - b. Head is grossly misaligned beyond carrier area.
  - c. A Device Check has prevented head selection.
  - d. Heads are not at Alignment Carrier signal cylinder due to FE procedural error or Seek Error.
  - e. The Head Alignment Unit or the Head Alignment feature on the tester is faulty and must be replaced.

#### **B.4 MICRODIAGNOSTIC ERROR CODE DICTIONARIES AND FLOWCHART ROUTINE DESCRIPTIONS**

The following pages contain the Error Code Dictionary for each routine and a flowchart Routine Description as indicated below.

	<b>Routine</b>	<b>Page</b>
	Routine Index*	B-19
	Wrap Test, Routine 00	B-20
	Incremental Seek, Routine 01	B-21
	Alternate Seek, Routine 02	B-22
	Random Seek, Routine 03	B-23
	Tachometer Gain Adjustment, Routine 04 (Part 1 of 2)	B-24
	Tachometer Gain Adjustment, Routine 04 (Part 2 of 2)	B-25
	Head Alignment, Routine 05	B-26
	Head Alignment Verification, Routine 06	B-27
	Head Alignment Track Seek, Routine 07	B-28
	Write/Read Verification, Routine 08 (Part 1 of 3)	B-29
	Write/Read Verification, Routine 08 (Part 2 of 3)	B-30
	Write/Read Verification, Routine 08 (Part 3 of 3)	B-31
	Incremental Offset Read, Routine 09 (Part 1 of 2)	B-32
	Incremental Offset Read, Routine 09 (Part 2 of 2)	B-33
	Read 65K Times (With Read Error Monitoring), Routine 0A (Part 1 of 2)	B-34
	Read 65K Times (With Read Error Monitoring), Routine 0A (Part 2 of 2)	B-35
	Read/Write Safety, Routine 0B (Part 1 of 3)	B-36
	Read/Write Safety, Routine 0B (Part 2 of 3)	B-37
	Read/Write Safety, Routine 0B (Part 3 of 3)	B-38
	Offset, Routine 0D	B-39
	Index, Routine 10 (Part 1 of 2)	B-40
	Index, Routine 10 (Part 2 of 2)	B-41
	Display Drive Output Byte, Routine 11 (Part 1 of 2)	B-42
	Display Drive Output Byte, Routine 11 (Part 2 of 2)	B-43
	Recalibrate, Routine 12	B-44
	Write, Routine 13	B-45

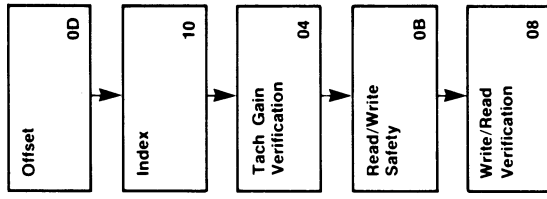
**Microdiagnostic  
Error Code  
Dictionaries  
(Tables)**

Identifies linked routines vs. independent routines

<b>Microdiagnostic Routine Descriptions (Flowcharts)</b>	<b>Routine</b>	<b>Page</b>
	Wrap Test, Routine 00	B-46
	Incremental Seek, Routine 01	B-47
	Alternate Seek, Routine 02	B-48
	Random Seek, Routine 03	B-49
	Tachometer Gain, Routine 04 (Part 1 of 2)	B-50
	Tachometer Gain, Routine 04 (Part 2 of 2)	B-51
	Head Alignment, Routine 05	B-52
	Head Alignment Verification, Routine 06 (Part 1 of 2)	B-53
	Head Alignment Verification, Routine 06 (Part 2 of 2)	B-54
	Head Alignment Track Seek, Routine 07	B-55
	Write/Read Verification, Routine 08 (Part 1 of 2)	B-56
	Write/Read Verification, Routine 08 (Part 2 of 2)	B-57
	Incremental Offset Read, Routine 09	B-58
	Read 65K Times, Routine 0A	B-59
	Read/Write Safety, Routine 0B (Part 1 of 2)	B-60
	Read/Write Safety, Routine 0B (Part 2 of 2)	B-61
	Offset, Routine 0D	B-62
	Index, Routine 10	B-63
	Display Drive Output Byte, Routine 11	B-64
	Recalibrate, Routine 12	B-65
	Write, Routine 13	B-66
	Subroutines (Part 1 of 3)	B-67
	Subroutines (Part 2 of 3)	B-68
	Subroutines (Part 3 of 3)	B-69
	Monitor (Part 1 of 2)	B-70
	Monitor (Part 2 of 2)	B-71

# Routine Index

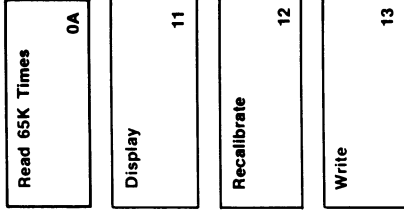
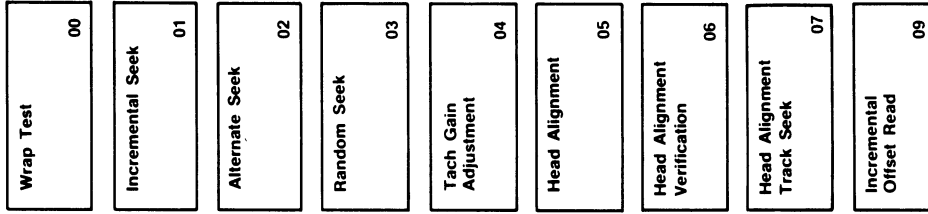
## LINKED ROUTINES



*DESTROY  
PACK FOR ALIENS*

END

## INDEPENDENT ROUTINES



# Microdiagnostic Error Code Dictionary — Wrap Test, Routine 00

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
10 OR 18	Bit 2 Bit 3, 5 Bit 4, 6, 7		<u>CABLE</u> B A OR D A OR C	If error occurs, note error code indication with SDSA switch set to NORMAL. Then, set Error Control to loop on error and SYNC ADDRESS to 0089. Write down displayed information error bits by setting SDSA switch to SD. By comparing the error bit(s), either replace the cable or suspect bad I/O PCB.
11 OR 19	Bit 1, 2, 3 Bit 5, 6 Bit 7		B OR D A OR D A OR C	
12 OR 1A	Bit 1 BIT 3, 4, 5, 6, 7		A OR D B OR D	
13 OR 1B	Bit 2, 3, 4, 5 Bit 7		B OR C B OR D	
15 OR 1D	Bit 1, 2, 3, 4, 5, 6, 7		A OR C	
16 OR 1E	Bit 2, 3, 4, 5, 6, 7		B OR C	
17 OR 1F	Bit 1, 3, 4, 5, 7 Bit 2, 6		A OR C B OR C	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary—Incremental Seek, Routine 01

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug.
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
FF	Successful Completion			

## Microdiagnostic Error Code Dictionary —Alternate Seek, Routine 02

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
01	Input parameter not valid	Byte # 00 High order inner CAR Range 00-03 (677-01) 00-01 (677-51) 01 Low order inner CAR Range 00-FF 02 High order outer CAR Range 00-03 (677-01) 00-01 (677-51) 03 Low order outer CAR Range 00-FF		All input parameter ranges are in Hexadecimal notation except when otherwise specified. Check to ensure that the parameters specified in byte #00, 01, 02 and 03 are valid.
A1	Drive not online before recalibrate		OPUT (D02)	
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
FF	Successful Completion			



# Microdiagnostic Error Code Dictionary—Random Seek, Routine 03

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEOU (D10) SVTL (D11) PSER (D15) SAMP	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary — Tachometer Gain Adjustment, Routine 04 (Part 1 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
01	Drive tach gain low but within tolerance			Tach gain need not be adjusted
02	Drive tach gain high but within tolerance			
10	After initiating a seek and waiting for 278 msec. line DIFF<32 is not true		OPUT (D02)	
20	DIFF=0 line is not true after DIFF<32 has been true and 69 msec have passed		OPUT (D02) SVTL (D11)	
81	Tach gain low and out of tolerance			Adjust tach gain
82	Tach gain high and out of tolerance			
00	UNSAFE TO USE UNLESS MOUNTED SECTION 80 (DEFAULT)			

# Microdiagnostic Error Code Dictionary —Tachometer Gain Adjustment, Routine 04 (Part 2 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
FF	Successful completion			

# Microdiagnostic Error Code Dictionary—Head Alignment, Routine 05

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
01	Invalid input parameters	Byte 00 High order CAR Range 00-03 (677-01) 00-01 (677-51) 01 Low order CAR Range 00-FF		All input parameter ranges are in Hexadecimal notation except when otherwise specified. Check to ensure that the parameters specified in byte #00 and 01 are valid
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary—Head Alignment Verification, Routine 06

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
				<p><b>Caution:</b> Before Routine 06 is run, Routine 07 must be run to position heads to head alignment cylinder (1F0 or 0F5 Hex). Warm up the drive for 20 minutes.</p>
01	Drive not online and/or not ready			Run Routine 07 to position heads to head alignment cylinder 1F0 Hex/677-01 or cylinder 0F5 Hex/677-51
02	One or more heads are misaligned more than 100 $\mu$ inches	<p>Byte #            Failing Head</p> <p>Bit Position 8   4   2   1   8   4   2   1</p> <p>08            7   6   5   4   3   2   1   0</p> <p>09            15 14 13 12 11 10 9   8</p> <p>0A                                    18 17 16</p>		Run Routine 05, Head Alignment, to align the heads which are offset
A7	Offset not ready after offset command or reset offset command has been initiated and 200 msec have passed		IPUT (D01) OPUT (D02) SVTL (D11)	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary—Head Alignment Track Seek, Routine 07

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug.
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary — Write/Read Verification, Routine 08 (Part 1 of 3)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES																																																																
01	"WRITE PROTECTED" switch is on			Turn off "WRITE PROTECTED" switch, then run routine #08 again.																																																																
02	Invalid input parameters	<p>Byte #</p> <p>00 High Order CAR Range 00-03 (677-01) 00-01 (677-51)</p> <p>01 Low Order CAR Range 00-FF</p> <p>03 Data Pattern—01-FF</p>		<p><b>CAUTION:</b></p> <p>Routine 08 will destroy customer data by overlaying a pattern specified by the FE. Data pattern is from index to index. (DB pattern is used by default).</p> <p>Do not use CE pack or customer data pack.</p> <p>Check to ensure that the parameters entered and specified by Byte #00-01 are valid.</p> <p>All input parameters are in Hexadecimal notation except when otherwise specified.</p>																																																																
03	No index found within 18 msec		OPUT (D01) INDX (D04) PSER (D15)																																																																	
04	"Unsafe" during Write	See Additional Action and Reference Notes column	OPUT (D02) DSHS (D20) WLOG (D17) X PRCO (D03)	<p>Byte #08 Error Summary</p> <table border="1"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Unsafe</td> <td>Not Used</td> <td>Abnor- mal Stop</td> <td>AC Write Unsafe</td> <td>DC Write</td> <td>Head Unsafe</td> <td>Not Used</td> <td>Not Used</td> </tr> </table> <p>Byte #09 Unsafe Write Condition</p> <table border="1"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Transi- tion Detect Failure</td> <td>Transi- tion Unsafe</td> <td>Write Current Unsafe</td> <td>Current Switch Unsafe</td> <td>Write Select Unsafe</td> <td>Current Sink Fail</td> <td>Write Ready Unsafe</td> <td>Not Used</td> </tr> </table> <p>Byte #0A Other Errors</p> <table border="1"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Write &amp; Offset</td> <td>Read &amp; Write</td> <td>Multi Head Select</td> <td>No Head Select</td> <td>35V Reg Fail</td> <td>PLO Unsafe</td> <td>DC Unsafe</td> <td>Not Used</td> </tr> </table> <p>Byte #02 Head Address</p> <table border="1"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Not Used</td> <td>Not Used</td> <td>Not Used</td> <td>HAR 16</td> <td>HAR 8</td> <td>HAR 4</td> <td>HAR 2</td> <td>HAR 1</td> </tr> </table>	8	4	2	1	8	4	2	1	Unsafe	Not Used	Abnor- mal Stop	AC Write Unsafe	DC Write	Head Unsafe	Not Used	Not Used	8	4	2	1	8	4	2	1	Transi- tion Detect Failure	Transi- tion Unsafe	Write Current Unsafe	Current Switch Unsafe	Write Select Unsafe	Current Sink Fail	Write Ready Unsafe	Not Used	8	4	2	1	8	4	2	1	Write & Offset	Read & Write	Multi Head Select	No Head Select	35V Reg Fail	PLO Unsafe	DC Unsafe	Not Used	8	4	2	1	8	4	2	1	Not Used	Not Used	Not Used	HAR 16	HAR 8	HAR 4	HAR 2	HAR 1
8	4	2	1	8	4	2	1																																																													
Unsafe	Not Used	Abnor- mal Stop	AC Write Unsafe	DC Write	Head Unsafe	Not Used	Not Used																																																													
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Transi- tion Detect Failure	Transi- tion Unsafe	Write Current Unsafe	Current Switch Unsafe	Write Select Unsafe	Current Sink Fail	Write Ready Unsafe	Not Used																																																													
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Write & Offset	Read & Write	Multi Head Select	No Head Select	35V Reg Fail	PLO Unsafe	DC Unsafe	Not Used																																																													
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Not Used	Not Used	Not Used	HAR 16	HAR 8	HAR 4	HAR 2	HAR 1																																																													
05	"Unsafe" during Read																																																																			

# Microdiagnostic Error Code Dictionary — Write/Read Verification, Routine 08 (Part 2 of 3)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES																																																						
06	On track read error	<p>Byte #</p> <table border="0"> <tr> <td></td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Bit Position</td> <td>08</td> <td>07</td> <td>06</td> <td>05</td> <td>04</td> <td>03</td> <td>02</td> <td>01</td> </tr> <tr> <td></td> <td>09</td> <td>15</td> <td>14</td> <td>13</td> <td>12</td> <td>11</td> <td>10</td> <td>9</td> </tr> <tr> <td></td> <td>0A</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>8</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>17</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>16</td> </tr> </table> <p>Failing Head</p>		8	4	2	1	8	4	2	1	Bit Position	08	07	06	05	04	03	02	01		09	15	14	13	12	11	10	9		0A							8									17									16	IPUT (D01) OPUT (D02) VFOS (D05) LINA (D18) DTEC (D19)	*Applies only if all 19 heads fail.
	8	4	2	1	8	4	2	1																																																		
Bit Position	08	07	06	05	04	03	02	01																																																		
	09	15	14	13	12	11	10	9																																																		
	0A							8																																																		
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								16																																																		
16	Positive offset read error (-300 $\mu$ inches offset for 677-01) (+600 $\mu$ inches offset for 677-51)	Same as 06		The heads which failed may be weak.																																																						
26	Reverse offset read error (-300 $\mu$ inches for 677-01) (-600 $\mu$ inches for 677-51)	Same as 06		The heads which failed may be weak.																																																						



# Microdiagnostic Error Code Dictionary—Write/Read Verification, Routine 08 (Part 3 of 3)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEOU (D10) SVTL (D11) PSER (D15) SAMP	
A7	Offset not ready after offset command or reset offset command has been initiated and 200 msec have passed.		IPUT (D01) OPUT (D02) SVTL (D11)	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary —Incremental Offset Read, Routine 09 (Part 1 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES																																																																																																																																																
01	Invalid input parameters	Byte # 00 High Order CAR Range 00-03 (677-01) 00-01 (677-51) Byte # 02 HAR Range 00-12 Byte # 03 Data Pattern		Call out Byte #3 and enter data pattern used in Routine 08 or Routine 13. Data pattern DB is used by default.  Check to ensure that the parameters entered in by Byte #00-02 are valid.  All input parameter ranges are in Hexadecimal notation except when otherwise specified.																																																																																																																																																
02	No index found after 18 msec		OPUT (D02) INDX (D04) PSER (D15)																																																																																																																																																	
03	"Unsafe" condition occurs during reading	See Additional Action and Reference Notes column		<table border="1"> <tr> <td colspan="12">Byte #08 Error Summary</td> </tr> <tr> <td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td> </tr> <tr> <td>Unsafe</td><td>Not Used</td><td>Abnor- mal Stop</td><td>AC Write Unsafe</td><td>DC Write</td><td>Head Unsafe</td><td>Not Used</td><td>Not Used</td><td>DC Write</td><td>Head Unsafe</td><td>Not Used</td><td>Not Used</td> </tr> <tr> <td colspan="12">Byte #09 Unsafe Write Condition</td> </tr> <tr> <td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td> </tr> <tr> <td>Transi- tion Detect Failure</td><td>Transi- tion Unsafe</td><td>Write Current Unsafe</td><td>Current Switch Unsafe</td><td>Write Select Unsafe</td><td>Current Sink Fail</td><td>Write Ready Unsafe</td><td>Not Used</td><td>Write Select Unsafe</td><td>Current Sink Fail</td><td>Write Ready Unsafe</td><td>Not Used</td> </tr> <tr> <td colspan="12">Byte #0A Other Errors</td> </tr> <tr> <td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td> </tr> <tr> <td>Write &amp; Offset</td><td>Read &amp; Write</td><td>Multi Head Select</td><td>No Head Select</td><td>35V Reg Fail</td><td>PLO Unsafe</td><td>DC Unsafe</td><td>Not Used</td><td>35V Reg Fail</td><td>PLO Unsafe</td><td>DC Unsafe</td><td>Not Used</td> </tr> <tr> <td colspan="12">Byte #02 Head Address</td> </tr> <tr> <td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td> </tr> <tr> <td>Not Used</td><td>Not Used</td><td>Not Used</td><td>HAR 16</td><td>HAR 8</td><td>HAR 4</td><td>HAR 2</td><td>HAR 1</td><td>HAR 8</td><td>HAR 4</td><td>HAR 2</td><td>HAR 1</td> </tr> </table>	Byte #08 Error Summary												8	4	2	1	8	4	2	1	8	4	2	1	Unsafe	Not Used	Abnor- mal Stop	AC Write Unsafe	DC Write	Head Unsafe	Not Used	Not Used	DC Write	Head Unsafe	Not Used	Not Used	Byte #09 Unsafe Write Condition												8	4	2	1	8	4	2	1	8	4	2	1	Transi- tion Detect Failure	Transi- tion Unsafe	Write Current Unsafe	Current Switch Unsafe	Write Select Unsafe	Current Sink Fail	Write Ready Unsafe	Not Used	Write Select Unsafe	Current Sink Fail	Write Ready Unsafe	Not Used	Byte #0A Other Errors												8	4	2	1	8	4	2	1	8	4	2	1	Write & Offset	Read & Write	Multi Head Select	No Head Select	35V Reg Fail	PLO Unsafe	DC Unsafe	Not Used	35V Reg Fail	PLO Unsafe	DC Unsafe	Not Used	Byte #02 Head Address												8	4	2	1	8	4	2	1	8	4	2	1	Not Used	Not Used	Not Used	HAR 16	HAR 8	HAR 4	HAR 2	HAR 1	HAR 8	HAR 4	HAR 2	HAR 1
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Not Used	Not Used	Not Used	HAR 16	HAR 8	HAR 4	HAR 2	HAR 1	HAR 8	HAR 4	HAR 2	HAR 1																																																																																																																																									

# Microdiagnostic Error Code Dictionary—Incremental Offset Read, Routine 09 (Part 2 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES																							
04	Read error	Byte # 04 Amount of offset during read error		Byte #04 <table border="1" style="display: inline-table; border-collapse: collapse; text-align: center;"> <tr> <td style="padding: 2px;">8</td> <td style="padding: 2px;">4</td> <td style="padding: 2px;">2</td> <td style="padding: 2px;">1</td> <td style="padding: 2px;">1</td> <td style="padding: 2px;">1</td> <td style="padding: 2px;">2</td> <td style="padding: 2px;">4</td> <td style="padding: 2px;">8</td> <td style="padding: 2px;">1</td> <td style="padding: 2px;">1</td> </tr> <tr> <td style="padding: 2px;">Offset Rev</td> <td style="padding: 2px;">Not Used</td> <td style="padding: 2px;">Offset 800 <math>\mu</math>in</td> <td style="padding: 2px;">Offset 400 <math>\mu</math>in</td> <td style="padding: 2px;">Offset 200 <math>\mu</math>in</td> <td style="padding: 2px;">Offset 100 <math>\mu</math>in</td> <td style="padding: 2px;">Offset 50 <math>\mu</math>in</td> <td style="padding: 2px;">Offset 25 <math>\mu</math>in</td> <td colspan="4"></td> </tr> </table>	8	4	2	1	1	1	2	4	8	1	1	Offset Rev	Not Used	Offset 800 $\mu$ in	Offset 400 $\mu$ in	Offset 200 $\mu$ in	Offset 100 $\mu$ in	Offset 50 $\mu$ in	Offset 25 $\mu$ in				
8	4	2	1	1	1	2	4	8	1	1																	
Offset Rev	Not Used	Offset 800 $\mu$ in	Offset 400 $\mu$ in	Offset 200 $\mu$ in	Offset 100 $\mu$ in	Offset 50 $\mu$ in	Offset 25 $\mu$ in																				
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug																							
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)																								
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)																								
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)																								
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)																								
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP																								
A7	Offset not ready after offset command has been initiated and 200 msec have passed.		IPUT (D01) OPUT (D02) SVTL (D11)																								
FF	Successful Completion																										

# Microdiagnostic Error Code Dictionary—Read 65K Times (With Read Error Monitoring), Routine 0A (Part 1 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
01	Invalid input parameters	Byte # 00 } 01 } Same as Routine 09 (Incremental Offset 02 } Read) 03 } 04 } Offset Range 00-1F		Check to ensure that the parameters entered in Byte #00-02 are valid.  Default to Head 00, Cylinder 000.  Each additional head must be selected by changing Byte 02.
02	No index found after 18 msec		OPUT (D02) INDX (D04) POSITION SERVO (D15)	
03	"Unsafe" condition occurred during read	Byte # 0C } 0D } Same as 08, 09, 0A respectively in 0E } Routine 08 (Write/Read Verification)		
04	Read error	Byte # 08 } High order byte # of times tried 09 } Low order byte # of times tried 0A } High order byte # of error occurred 0B } Low order byte # of error occurred		When the program stops by itself (EXECUTE switch not pressed or no "Unsafe" conditions), the registers which contain the number of times tried will be equal to zero. This means that the track has been read 65,535 times and the routine has run to completion.
A1	Drive not online before recalibrate		OPUT (D02)	
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	

# Microdiagnostic Error Code Dictionary—Read 65K Times (With Read Error Monitoring), Routine 0A (Part 2 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
A7	Offset not ready after offset command or reset offset command has been initiated and 200 msec have passed		IPUT (D01) OPUT (D02) SVTL (D11)	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary —Read/Write Safety, Routine 0B (Part 1 of 3)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES																																																
01	"Unsafe" condition exists after device initialization pulse is sent	See Additional Action and Reference Notes column	IPUT (D01) OPUT (D02) DSHS (D20)	<p>Byte #08 Error Summary</p> <table border="1" data-bbox="381 601 511 929"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Unsafe</td> <td>Not Used</td> <td>Abnor- mal- Stop</td> <td>AC Write Unsafe</td> <td>DC Write</td> <td>Head Unsafe</td> <td>Not Used</td> <td>Not Used</td> </tr> </table> <p>Byte #09 Unsafe Write Condition</p> <table border="1" data-bbox="381 714 511 929"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Transi- tion Detect Failure</td> <td>Transi- tion Unsafe</td> <td>Write Current Unsafe</td> <td>Current Switch Unsafe</td> <td>Write Select Unsafe</td> <td>Current Sink Fail</td> <td>Write Ready Unsafe</td> <td>Not Used</td> </tr> </table> <p>Byte #0A Other Errors</p> <table border="1" data-bbox="381 929 511 1213"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Write &amp; Offset</td> <td>Read &amp; Write</td> <td>Multi Head Select</td> <td>No Head Select</td> <td>35V Reg Fail</td> <td>PLO Unsafe</td> <td>DC Unsafe</td> <td>Not Used</td> </tr> </table>	8	4	2	1	8	4	2	1	Unsafe	Not Used	Abnor- mal- Stop	AC Write Unsafe	DC Write	Head Unsafe	Not Used	Not Used	8	4	2	1	8	4	2	1	Transi- tion Detect Failure	Transi- tion Unsafe	Write Current Unsafe	Current Switch Unsafe	Write Select Unsafe	Current Sink Fail	Write Ready Unsafe	Not Used	8	4	2	1	8	4	2	1	Write & Offset	Read & Write	Multi Head Select	No Head Select	35V Reg Fail	PLO Unsafe	DC Unsafe	Not Used
8	4	2	1	8	4	2	1																																													
Unsafe	Not Used	Abnor- mal- Stop	AC Write Unsafe	DC Write	Head Unsafe	Not Used	Not Used																																													
8	4	2	1	8	4	2	1																																													
Transi- tion Detect Failure	Transi- tion Unsafe	Write Current Unsafe	Current Switch Unsafe	Write Select Unsafe	Current Sink Fail	Write Ready Unsafe	Not Used																																													
8	4	2	1	8	4	2	1																																													
Write & Offset	Read & Write	Multi Head Select	No Head Select	35V Reg Fail	PLO Unsafe	DC Unsafe	Not Used																																													
02	Unsafe condition exists but does not make "Unsafe" active	Same as 01	OPUT (D02)																																																	
03	No index found within 18 msec		OPUT (D02) INDX (D04) PSER (D15)																																																	
04	"Unsafe" is not active after trying to set "AC Write" latch		IPUT (D01) OPUT (D02) DSHS (D20)																																																	

# I Microdiagnostic Error Code Dictionary —Read/Write Safety, Routine 0B (Part 2 of 3)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
05	"AC Unsafe" and/or "Transition Unsafe" does not set as expected	Same as 01	IPUT (D01) OPUT (D02) DSHS (D20)	
06	"Unsafe" does not reset after setting "AC Unsafe" and then trying to reset "AC Unsafe"		IPUT (D01) OPUT (D02) DSHS (D20)	
09	"Unsafe" is not active after trying to set "Write and Offset" latch		IPUT (D01) OPUT (D02) DSHS (D20)	
10	"Write and Offset" latch not set as expected	Same as 01	OPUT (D02) DSHS (D20)	
11	"Unsafe" does not reset after setting "Write and Offset" and then trying to reset "Write and Offset" latch afterwards	Same as 01	OPUT (D02) DSHS (D20)	
12	"Unsafe" not active after trying to set "No Head Select" latch		IPUT (D01) OPUT (D02) DSHS (D20)	
13	"No Head Select" latch not set as expected	Same as 01	OPUT (D02) DSHS (D20)	
14	"Unsafe" does not reset after setting "No Head Select" latch and then trying to reset the same latch afterwards	Same as 01	OPUT (D02) DSHS (D20)	

# Microdiagnostic Error Code Dictionary—Read/Write Safety, Routine 0B (Part 3 of 3)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug.
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEOU (D10) SVTL (D11) PSEB (D15) SAMP	
FF	Successful Completion			



# Microdiagnostic Error Code Dictionary —Offset, Routine 0D

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
01	No "On Track" signal		OPUT (D02) PSER (D15)	
02	"On Track" signal still active after offsetting +600 $\mu$ inches (or -600 $\mu$ inches)		OPUT (D02) PSER (D15)	
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug.
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
A7	Offset not ready after offset command or reset offset command has been initiated and 200 msec have passed		IPUT (D01) OPUT (D02) SVTL (D11)	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary—Index, Routine 10 (Part 1 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
01	Invalid input parameters	Byte # 00 High Order CAR Range 00-03 (677-01) 00-01 (677-51) 01 Low Order CAR Range 00-FF		Check to ensure that the parameters entered in Byte #00-01 are valid. All input parameter ranges are in Hexadecimal notation except when otherwise specified.
02	No index found within 18 msec		OPUT (D02) INDX (D04) PSER (D15)	
03	On track index tolerance greater than +330 $\mu$ sec			
13	Offset index tolerance greater than +330 $\mu$ sec			
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug.
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	

# Microdiagnostic Error Code Dictionary—Index, Routine 10 (Part 2 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
A7	Offset not ready after offset command or reset offset command has been initiated and 200 msec have passed		IPUT (D01) OPUT (D02)	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary —Display Drive Output Byte, Routine 11 (Part 1 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES																
XX	Shifting one bit from right to left	<p>Byte #</p> <table border="1" data-bbox="427 1165 483 1551"> <tr> <td>8</td><td>4</td><td>2</td><td>1</td><td>8</td><td>4</td><td>2</td><td>1</td> </tr> <tr> <td>bit 7</td><td>bit 6</td><td>bit 5</td><td>bit 4</td><td>bit 3</td><td>bit 2</td><td>bit 1</td><td>X</td> </tr> </table> <p>X - not used</p> <p>Byte #00</p> <ul style="list-style-type: none"> <li>Bit 1 - - RP06</li> <li>2 - sequence enable</li> <li>3 - on line</li> <li>4 - file ready</li> <li>5 - seek incomplete</li> <li>6 - offset ready</li> <li>7 - sequence pick out</li> </ul> <p>Byte #01</p> <ul style="list-style-type: none"> <li>Bit 1 - servo data</li> <li>2 - index</li> <li>3 - on track</li> <li>4 - not used</li> <li>5 - sign</li> <li>6 - diff less than 32</li> <li>7 - index error</li> </ul> <p>Byte #02</p> <ul style="list-style-type: none"> <li>Bit 1 - off cylinder</li> <li>2 - not used</li> <li>3 - reset register</li> <li>4 - diff = 0</li> <li>5 - velocity servo enable</li> <li>6 - stop velocity</li> <li>7 - coarse track</li> </ul>	8	4	2	1	8	4	2	1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	X		<p>Invalid byte # for display</p> <p>Reload byte # to be displayed</p>
8	4	2	1	8	4	2	1													
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	X													

# Microdiagnostic Error Code Dictionary — Display Drive Output Byte, Routine 11 (Part 2 of 2)

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
		<p>Byte #03</p> <ul style="list-style-type: none"> <li>Bit</li> <li>1 - not used</li> <li>2 - heads unsafe</li> <li>3 - DC write unsafe</li> <li>4 - AC write unsafe</li> <li>5 - abnormal stop</li> <li>6 - not used</li> <li>7 - unsafe</li> </ul> <p>Byte #04</p> <ul style="list-style-type: none"> <li>Bit</li> <li>1 - write ready unsafe</li> <li>2 - current sink fail</li> <li>3 - write select unsafe</li> <li>4 - current switch unsafe</li> <li>5 - write current unsafe</li> <li>6 - transition unsafe</li> <li>7 - transition detector failing</li> </ul> <p>Byte #05</p> <ul style="list-style-type: none"> <li>Bit</li> <li>1 - DC unsafe</li> <li>2 - PLO unsafe</li> <li>3 - 35 V Reg. Fail</li> <li>4 - no head select</li> <li>5 - multi-head select</li> <li>6 - read and write</li> <li>7 - write and offset</li> </ul> <p>Byte #06</p> <ul style="list-style-type: none"> <li>Bit</li> <li>1 - write protected</li> <li>2 - plug enable</li> <li>3 - port B locked</li> <li>4 - port A locked</li> <li>5 - logical address 1</li> <li>6 - logical address 2</li> <li>7 - logical address 4</li> </ul>		

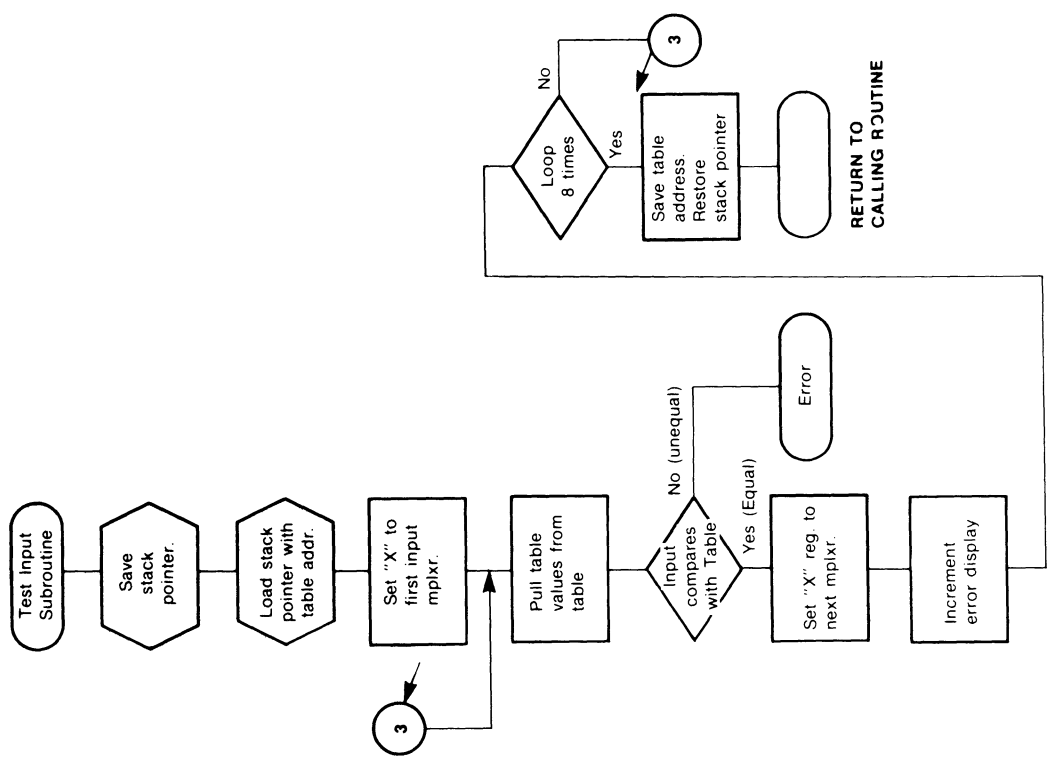
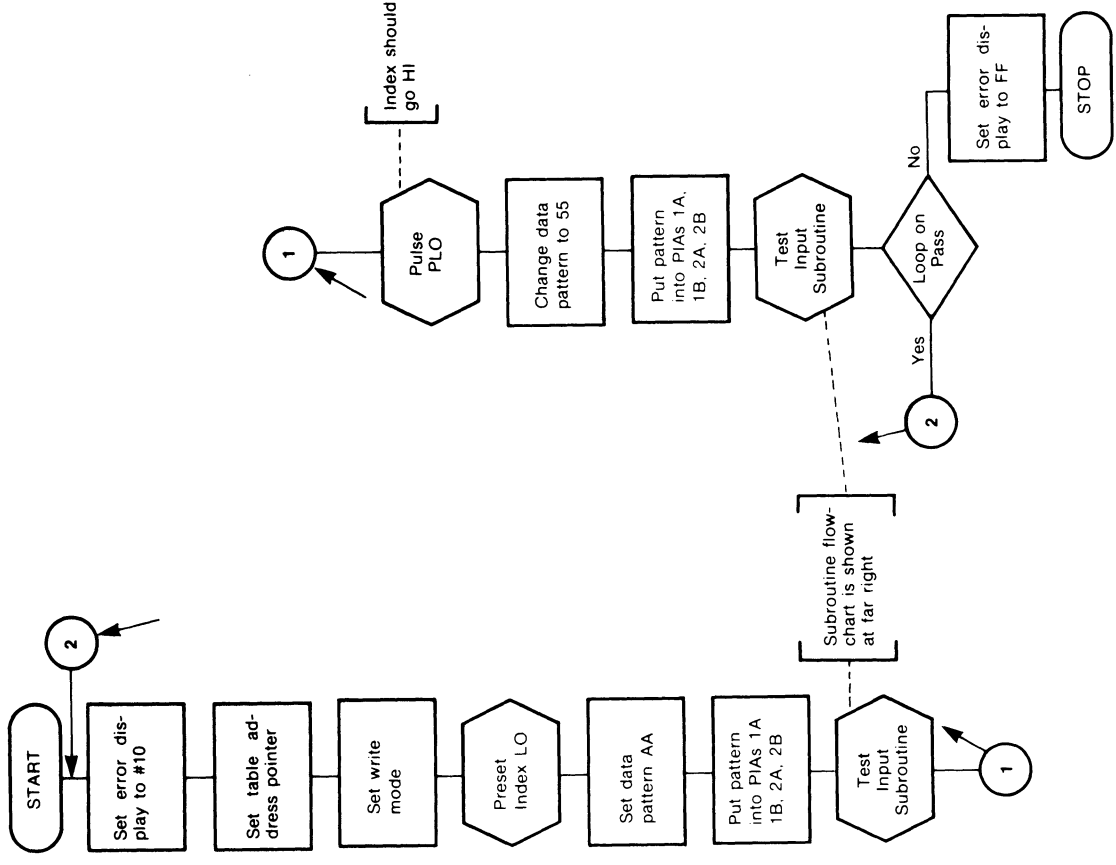
# Microdiagnostic Error Code Dictionary — Recalibrate, Routine 12

ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES
A1	Drive not online before recalibrate		OPUT (D02)	Check logical address plug
A2	Drive not ready before recalibrate		OPUT (D02) SVTL (D11)	
A3	Drive is ready after a recalibrate command has been initiated		IPUT (D01) OPUT (D02) SVTL (D11)	
A4	Seek incomplete		IPUT (D01) OPUT (D02) SVTL (D11)	
A5	Drive not ready within one second after a recalibrate command or a seek command has been initiated		SVTL (D11)	
A6	Drive not online and/or not ready after sequence up for 30 seconds		IPUT (D01) OPUT (D02) SEQU (D10) SVTL (D11) PSER (D15) SAMP	
FF	Successful Completion			

# Microdiagnostic Error Code Dictionary —Write, Routine 13

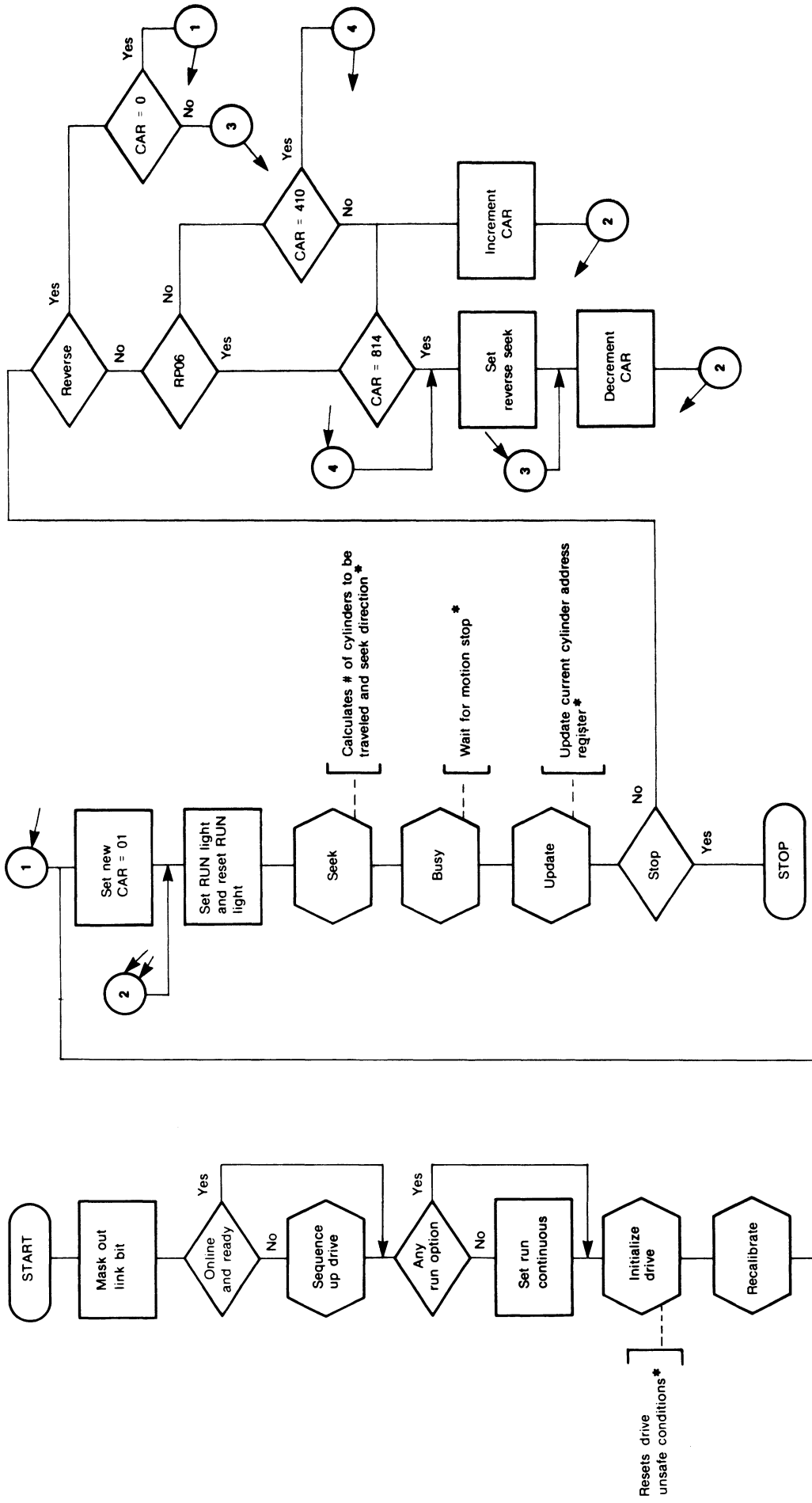
ERROR CODE	ERROR DESCRIPTION	MICRODIAGNOSTIC OUTPUT BYTES	MOST PROBABLE FAILING UNITS	ADDITIONAL ACTION AND REFERENCE NOTES																																																																
01	"WRITE PROTECTED" switch is on			<p><b>CAUTION:</b></p> <p>Routine 13 will destroy customer data by overlaying a pattern specified by the FE. Data pattern is written from index to index. Do not use CE pack or customer data pack. DB data pattern is used by default (Defaults to Cylinder 0).</p> <p>Turn off "WRITE PROTECTED" switch, then run routine #13 again.</p>																																																																
02	Invalid input parameters	<p>Byte #</p> <p>00 High Order CAR Range 00-03 (677-01) 02 HAR Range 00-12</p> <p>01 Low Order CAR Range 00-FF 03 Data Pattern</p>		<p>Check to ensure that the parameters entered in Byte #00-02 are valid.</p> <p>All input parameters are in Hexadecimal notation except when otherwise specified.</p>																																																																
03	No index found within 18 msec		<p>OPUT (D01)</p> <p>INDX (D04)</p> <p>PSER (D15)</p>																																																																	
04	"Unsafe" during Write	See Additional Action and Reference Notes column	<p>OPUT (D02)</p> <p>DSHS (D20)</p> <p>WLOG (D17)</p> <p>PRCO (D03)</p>	<p>Byte #08 Error Summary</p> <table border="1"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Unsafe</td> <td>Not Used</td> <td>Abnor- mal Stop</td> <td>AC Write Unsafe</td> <td>DC Write</td> <td>Head Unsafe</td> <td>Not Used</td> <td>Not Used</td> </tr> </table> <p>Byte #09 Unsafe Write Condition</p> <table border="1"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Transi- tion Detect Failure</td> <td>Transi- tion Unsafe</td> <td>Write Current Unsafe</td> <td>Current Switch Unsafe</td> <td>Write Select Unsafe</td> <td>Current Sink Fail</td> <td>Write Ready Unsafe</td> <td>Not Used</td> </tr> </table> <p>Byte #0A Other Errors</p> <table border="1"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Write &amp; Offset</td> <td>Read &amp; Write</td> <td>Multi Head Select</td> <td>No Head Select</td> <td>35V Reg Fail</td> <td>PLO Unsafe</td> <td>DC Unsafe</td> <td>Not Used</td> </tr> </table> <p>Byte #02 Head Address</p> <table border="1"> <tr> <td>8</td> <td>4</td> <td>2</td> <td>1</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>Not Used</td> <td>Not Used</td> <td>Not Used</td> <td>HAR 16</td> <td>HAR 8</td> <td>HAR 4</td> <td>HAR 2</td> <td>HAR 1</td> </tr> </table>	8	4	2	1	8	4	2	1	Unsafe	Not Used	Abnor- mal Stop	AC Write Unsafe	DC Write	Head Unsafe	Not Used	Not Used	8	4	2	1	8	4	2	1	Transi- tion Detect Failure	Transi- tion Unsafe	Write Current Unsafe	Current Switch Unsafe	Write Select Unsafe	Current Sink Fail	Write Ready Unsafe	Not Used	8	4	2	1	8	4	2	1	Write & Offset	Read & Write	Multi Head Select	No Head Select	35V Reg Fail	PLO Unsafe	DC Unsafe	Not Used	8	4	2	1	8	4	2	1	Not Used	Not Used	Not Used	HAR 16	HAR 8	HAR 4	HAR 2	HAR 1
8	4	2	1	8	4	2	1																																																													
Unsafe	Not Used	Abnor- mal Stop	AC Write Unsafe	DC Write	Head Unsafe	Not Used	Not Used																																																													
8	4	2	1	8	4	2	1																																																													
Transi- tion Detect Failure	Transi- tion Unsafe	Write Current Unsafe	Current Switch Unsafe	Write Select Unsafe	Current Sink Fail	Write Ready Unsafe	Not Used																																																													
8	4	2	1	8	4	2	1																																																													
Write & Offset	Read & Write	Multi Head Select	No Head Select	35V Reg Fail	PLO Unsafe	DC Unsafe	Not Used																																																													
8	4	2	1	8	4	2	1																																																													
Not Used	Not Used	Not Used	HAR 16	HAR 8	HAR 4	HAR 2	HAR 1																																																													
FF	Successful Completion																																																																			

# Wrap Test — Routine 00



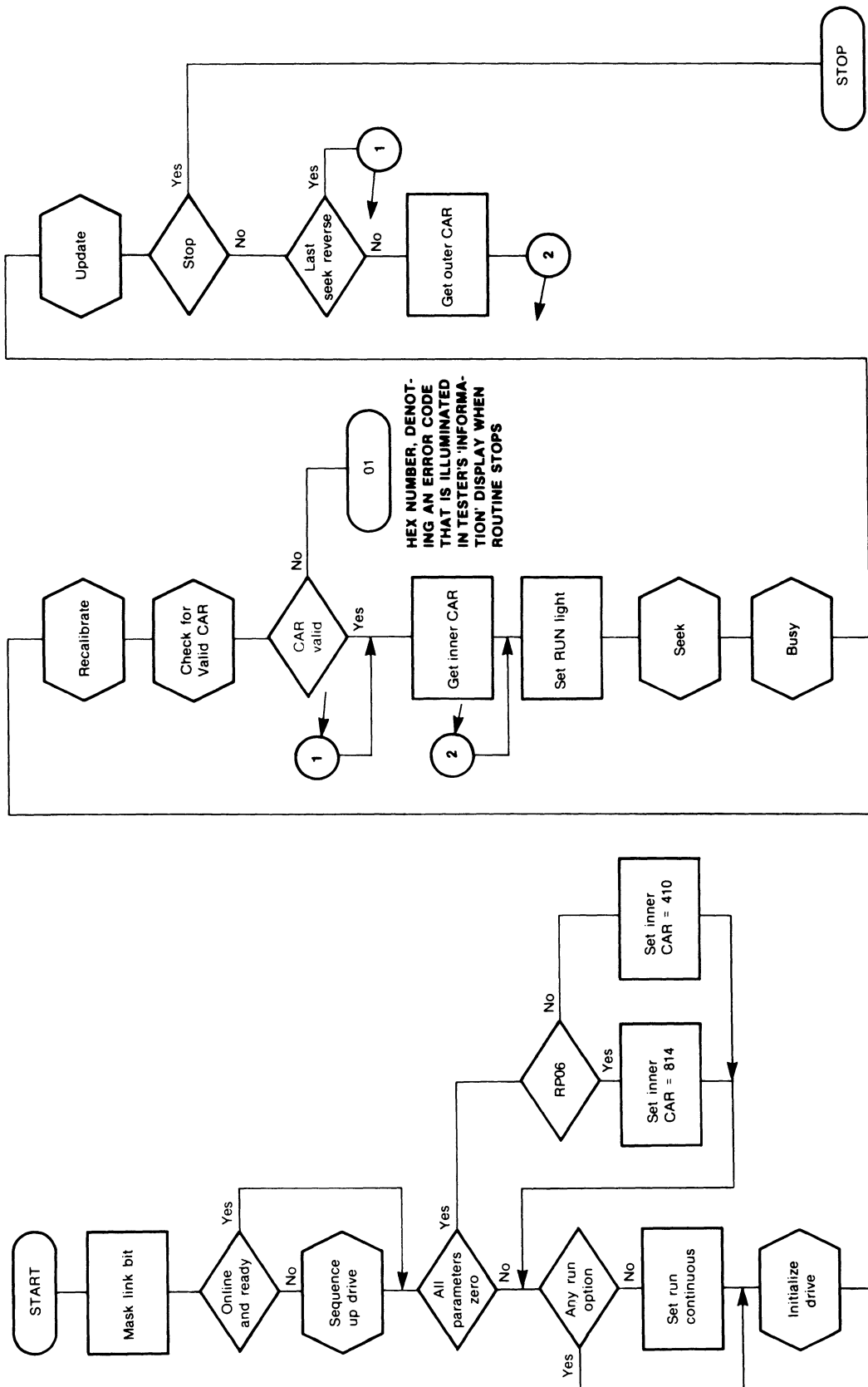


# Incremental Seek — Routine 01



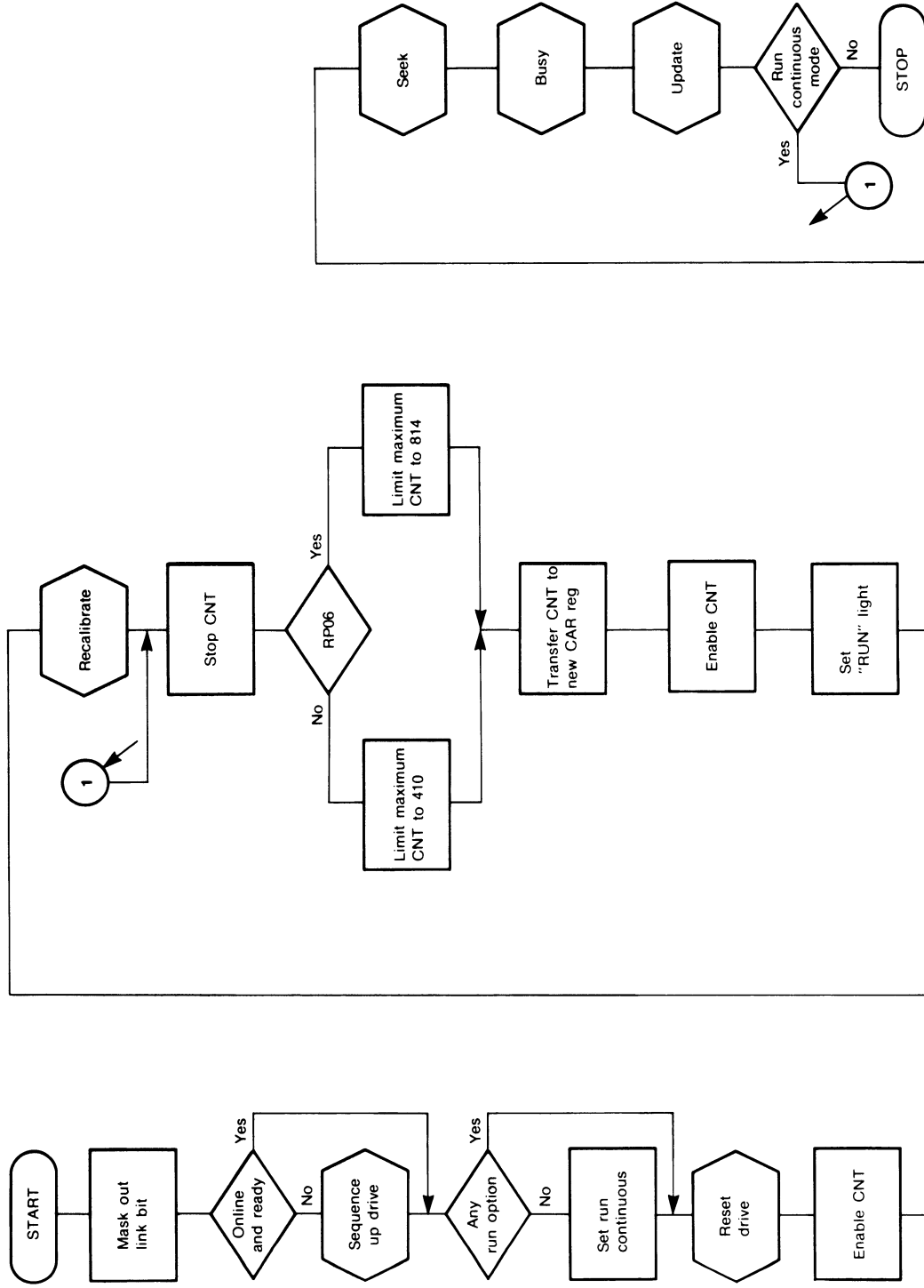
\* Applies to any routine having this block

# Alternate Seek — Routine 02

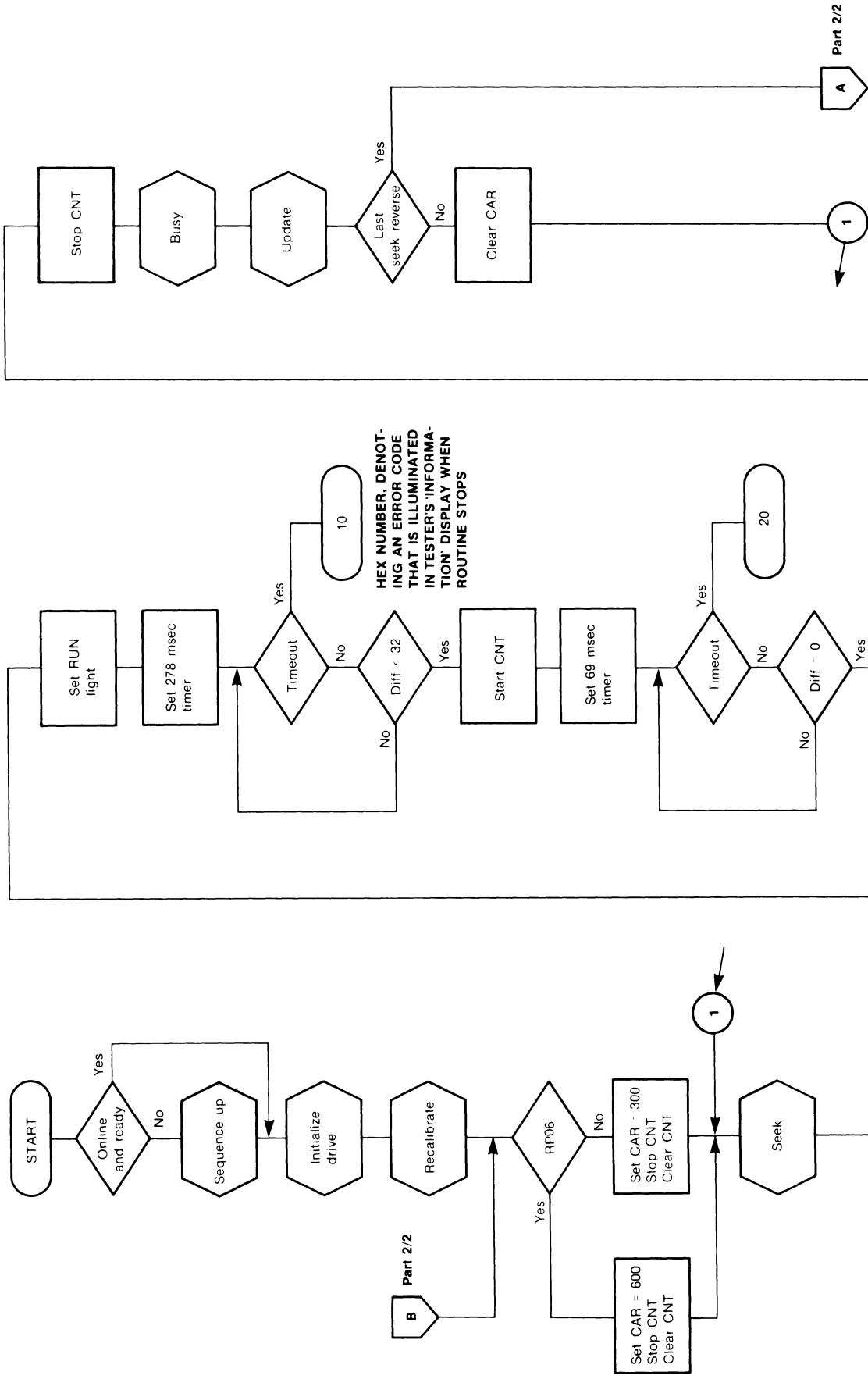


HEX NUMBER, DENOTING AN ERROR CODE THAT IS ILLUMINATED IN TESTER'S 'INFORMATION' DISPLAY WHEN ROUTINE STOPS

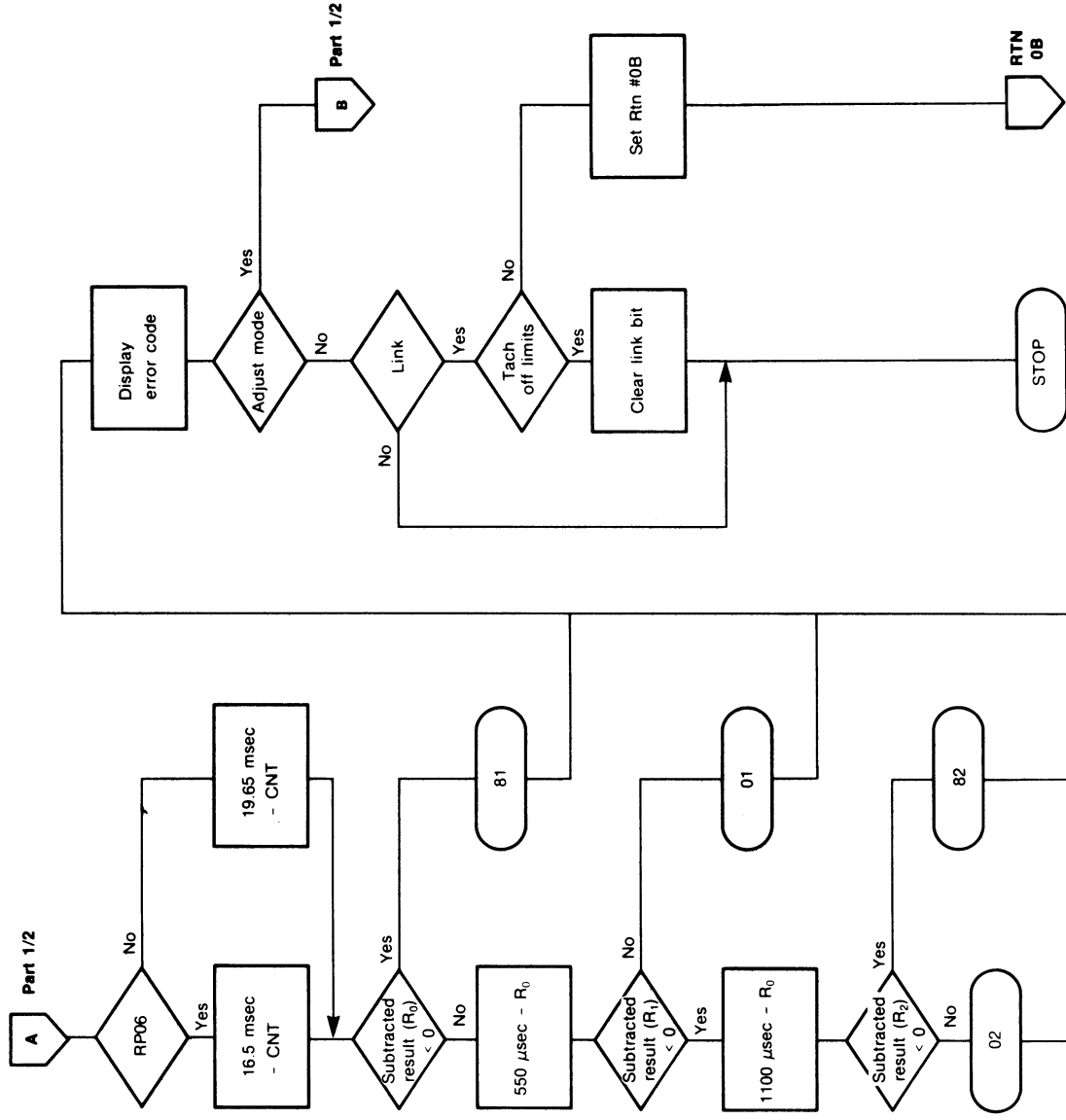
# Random Seek — Routine 03



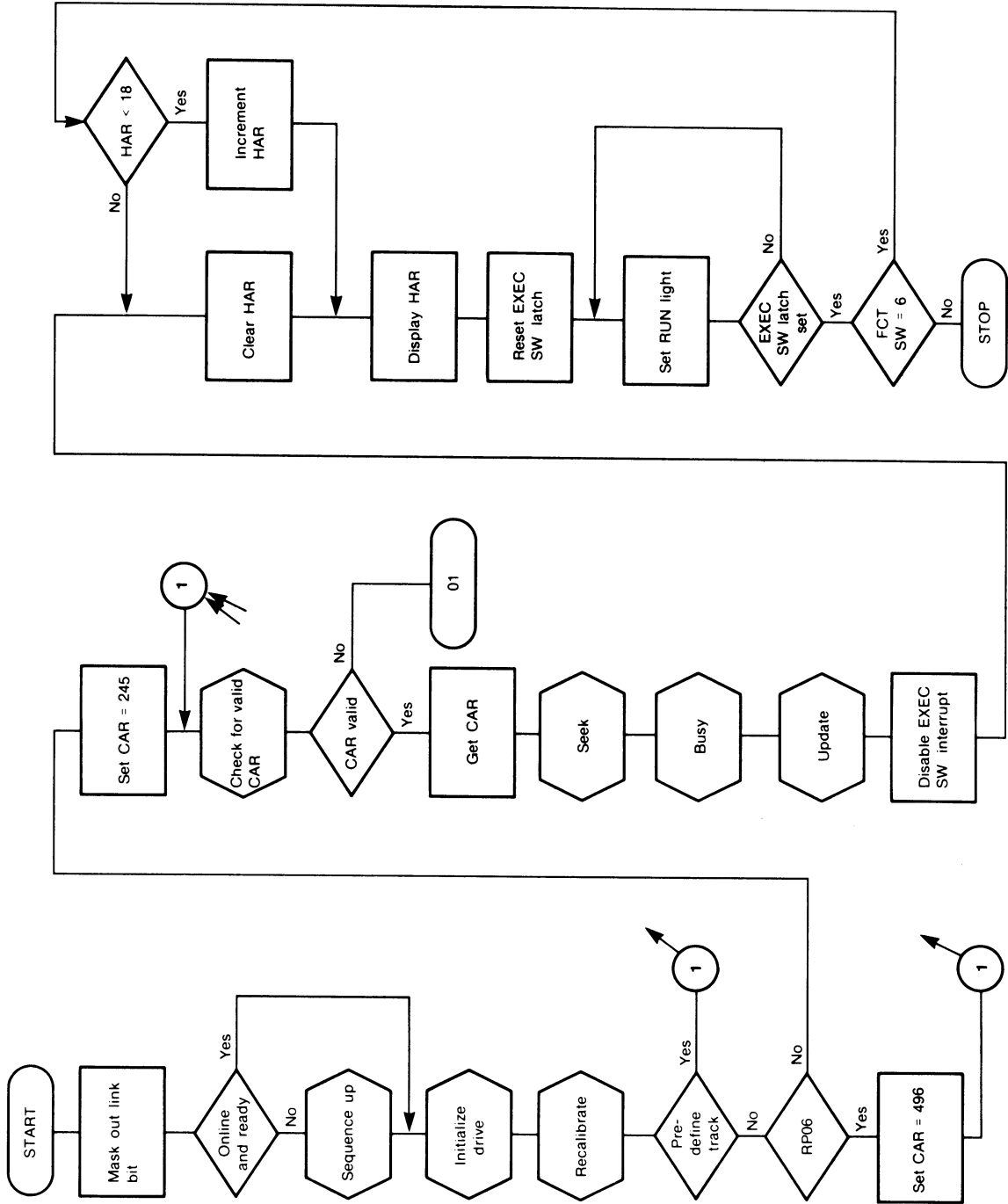
# Tachometer Gain — Routine 04 (Part 1 of 2)



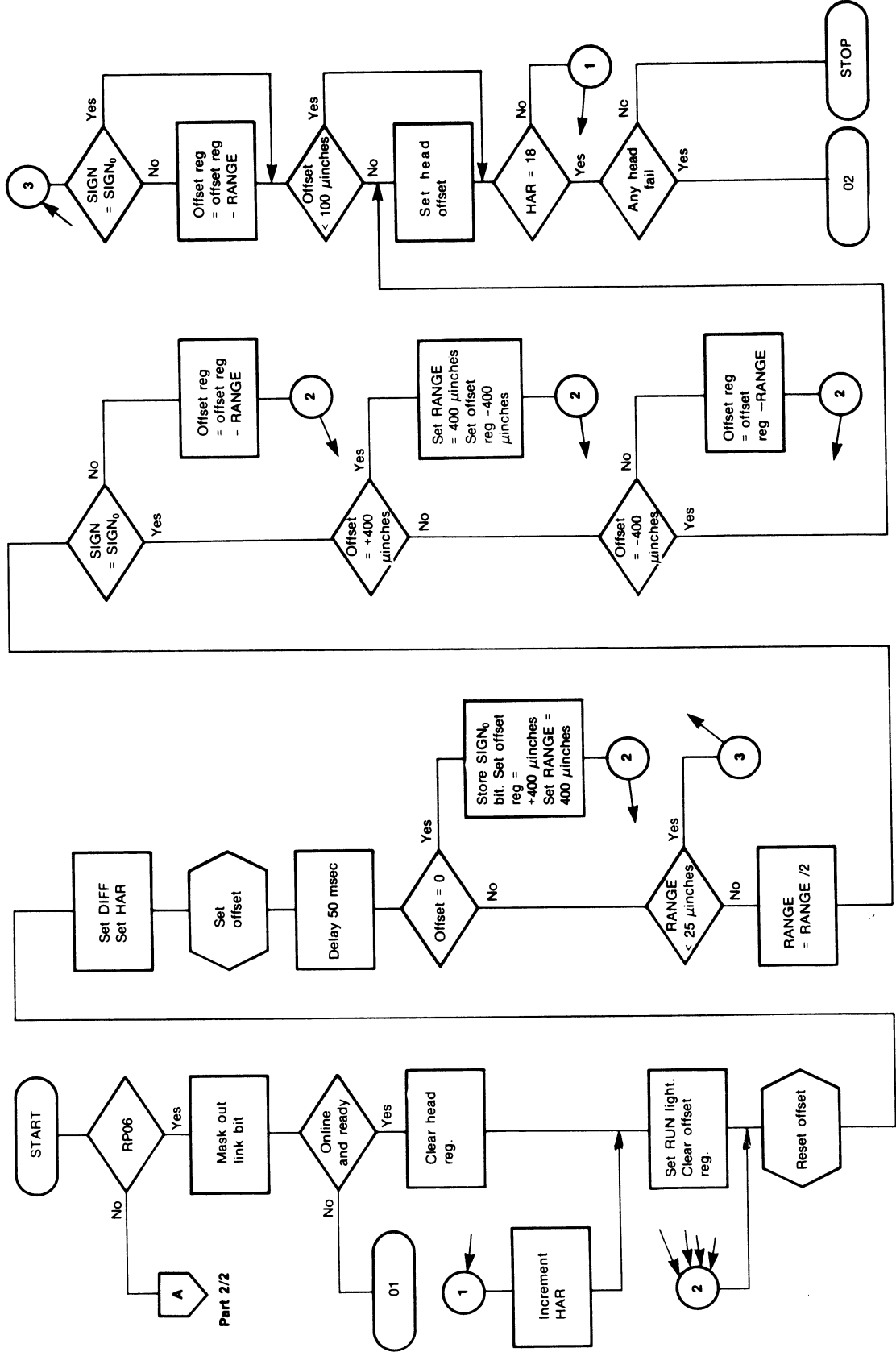
# Tachometer Gain — Routine 04 (Part 2 of 2)



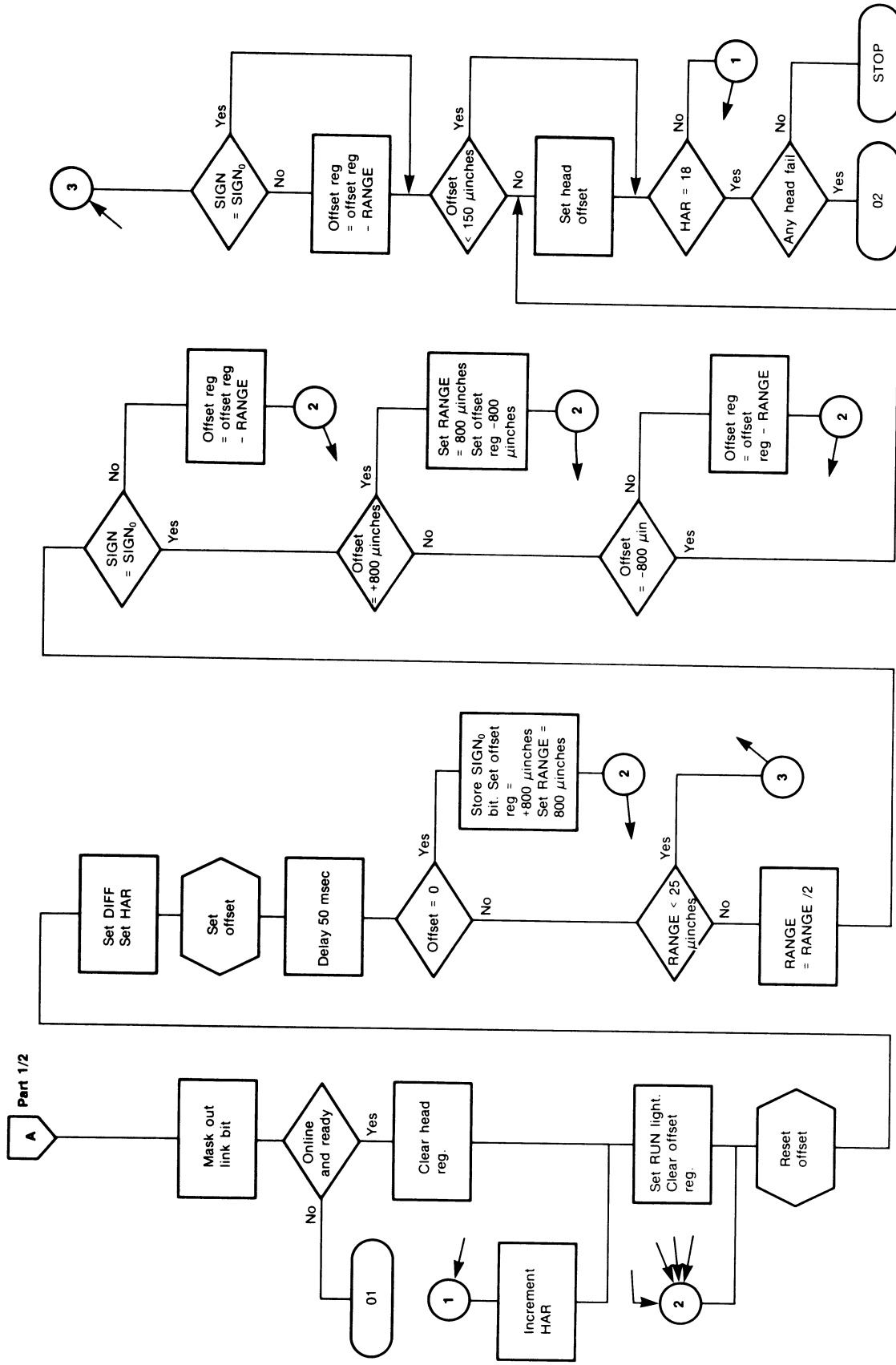
# Head Alignment — Routine 05



# Head Alignment Verification — Routine 06 (Part 1 of 2)

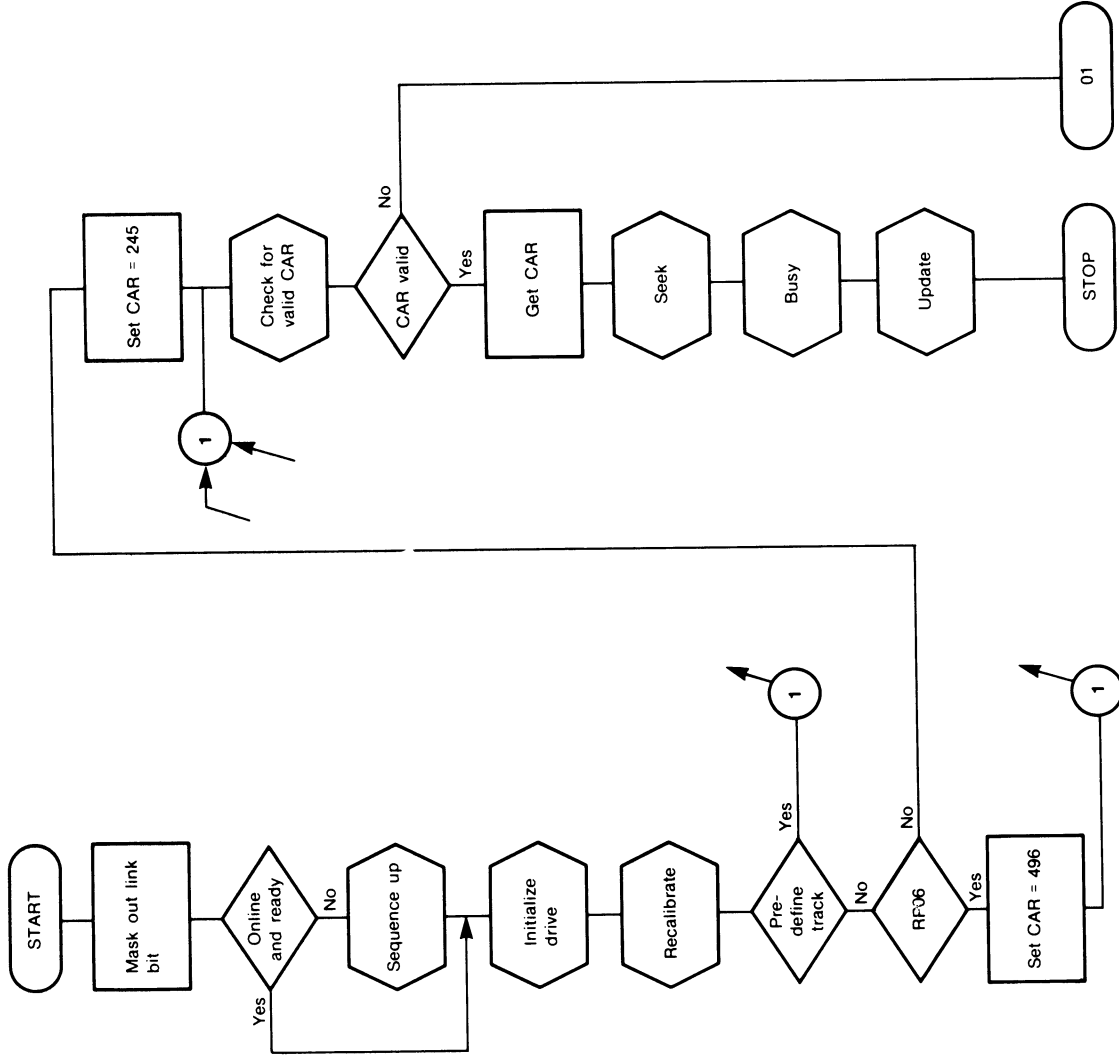


# Head Alignment Verification — Routine 06 (Part 2 of 2)

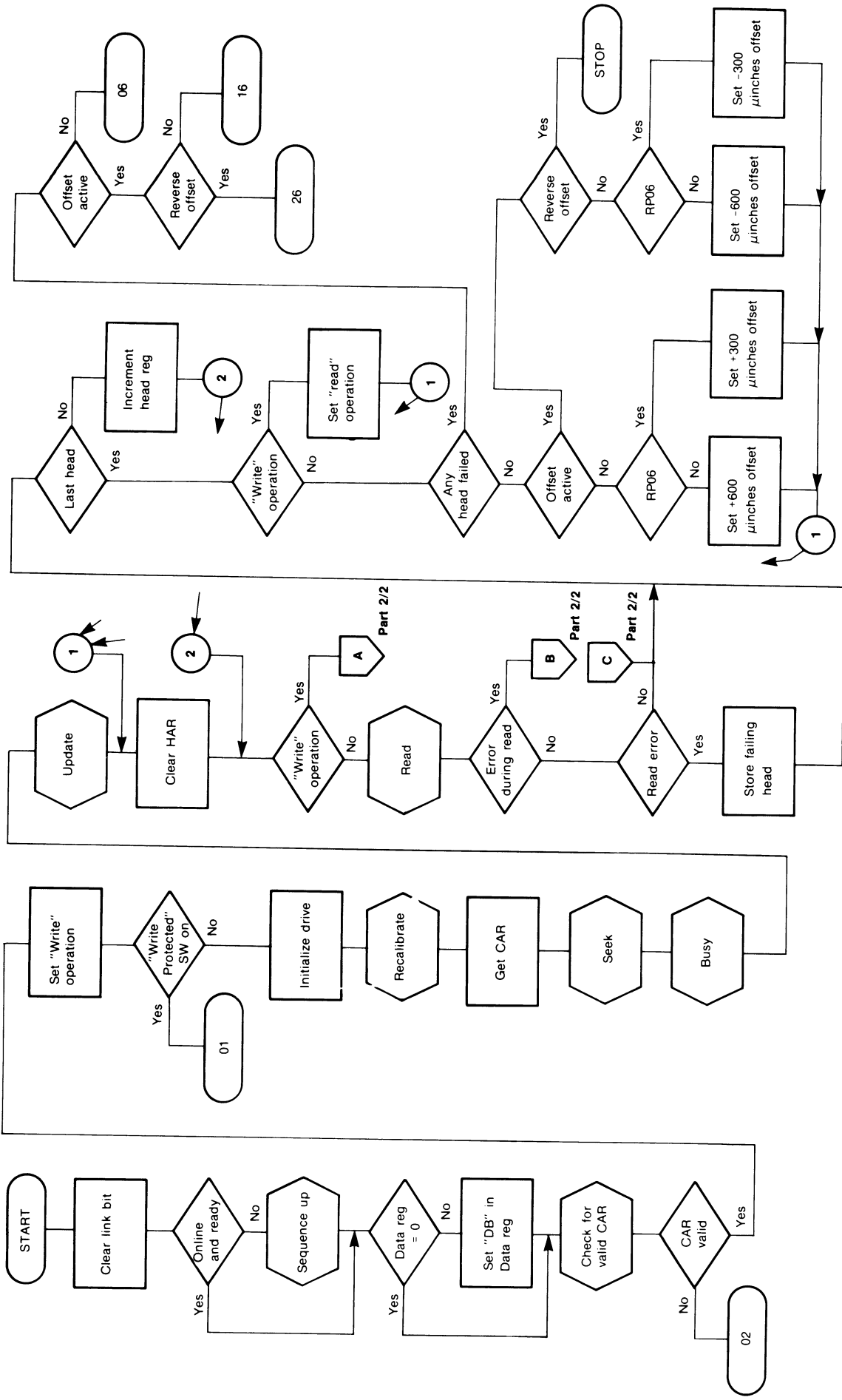




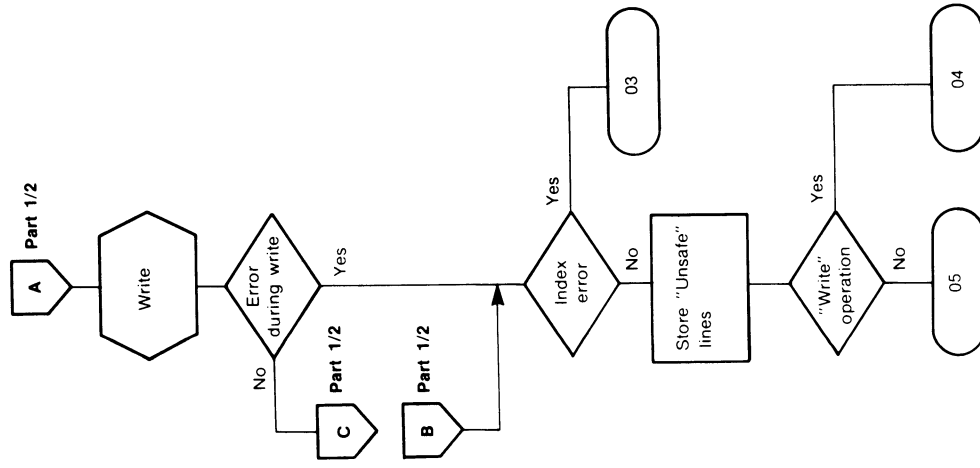
# Head Alignment Track Seek — Routine 07



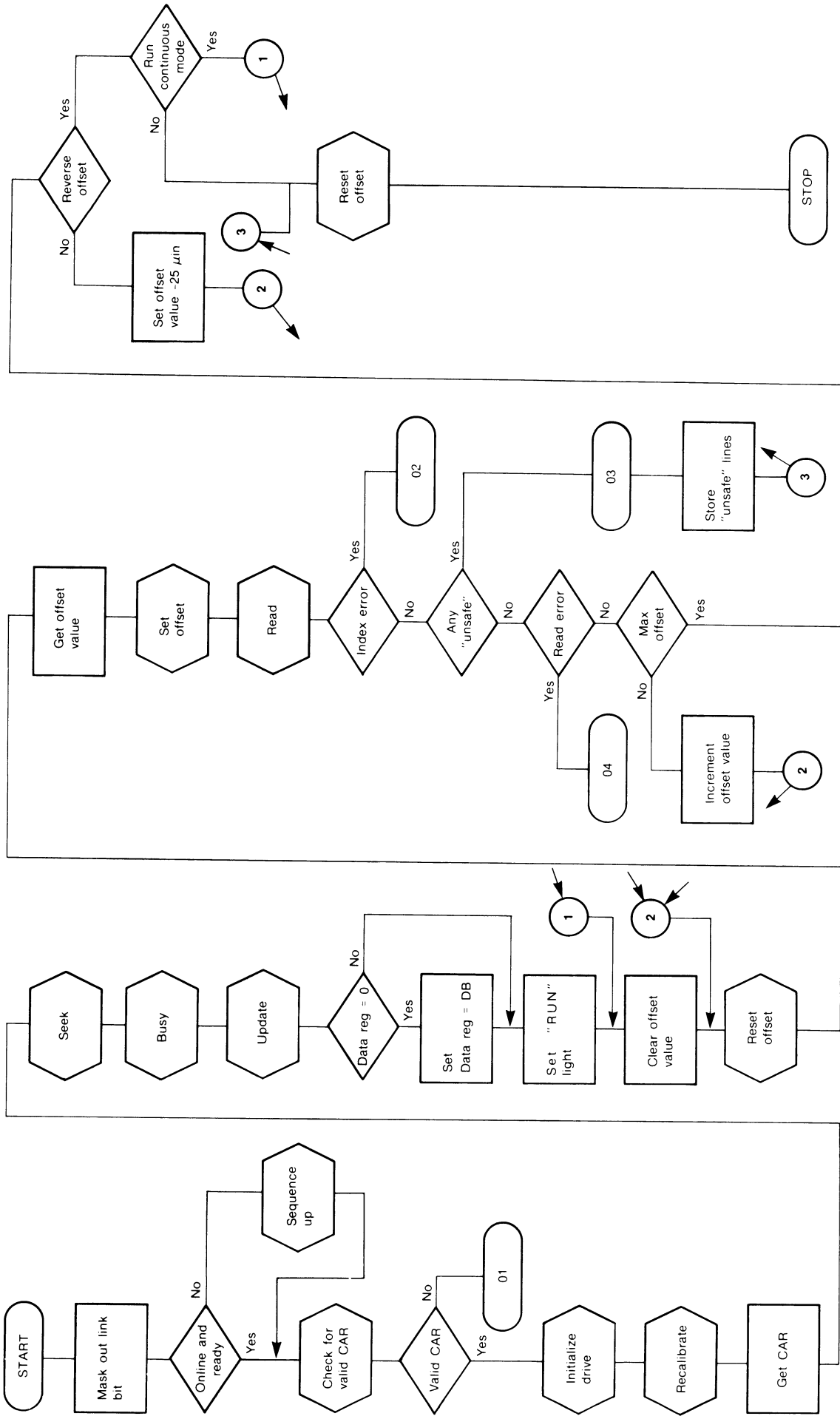
# Write/Read Verification — Routine 08 (Part 1 of 2)



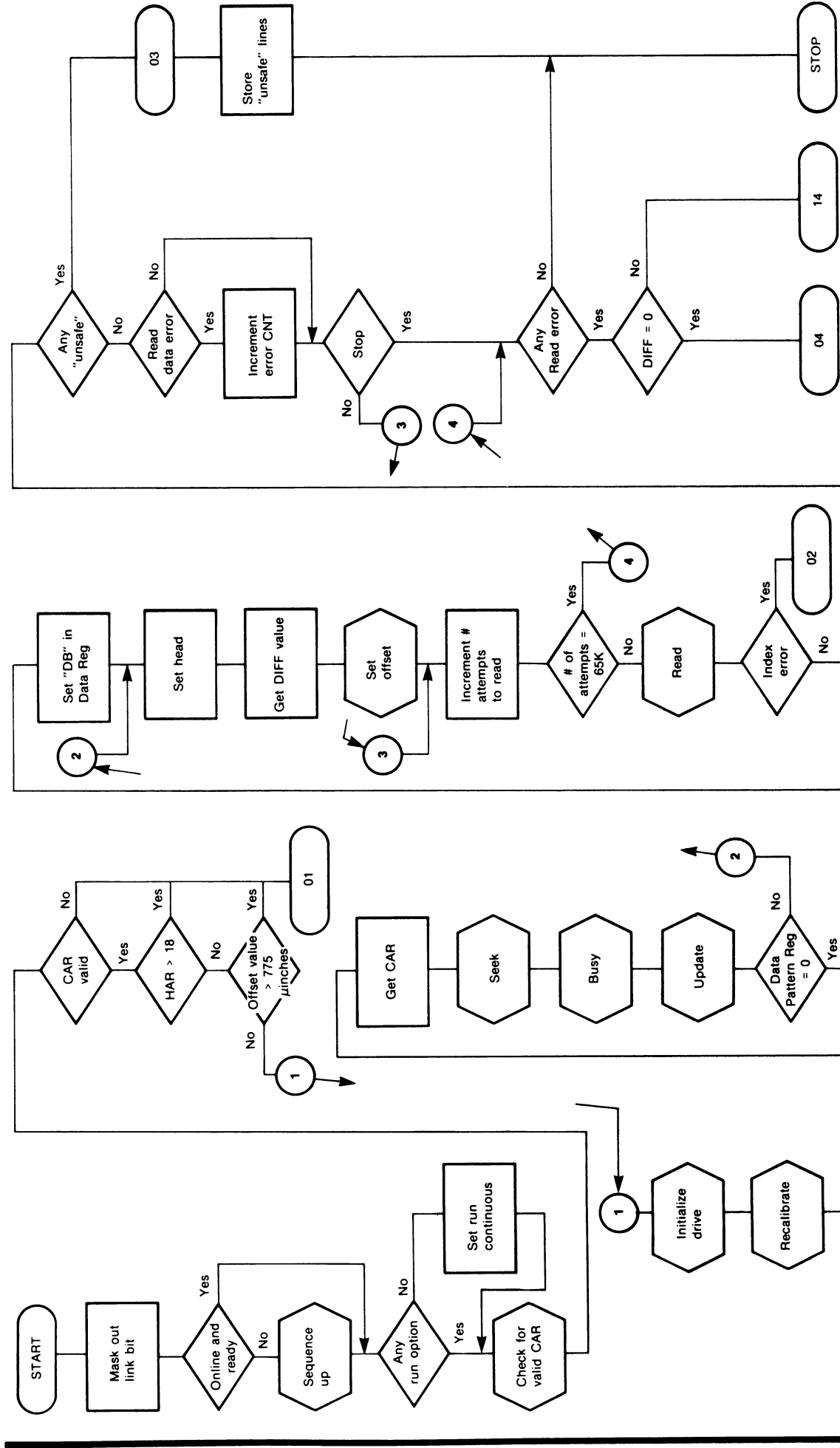
# Write/Read Verification — Routine 08 (Part 2 of 2)



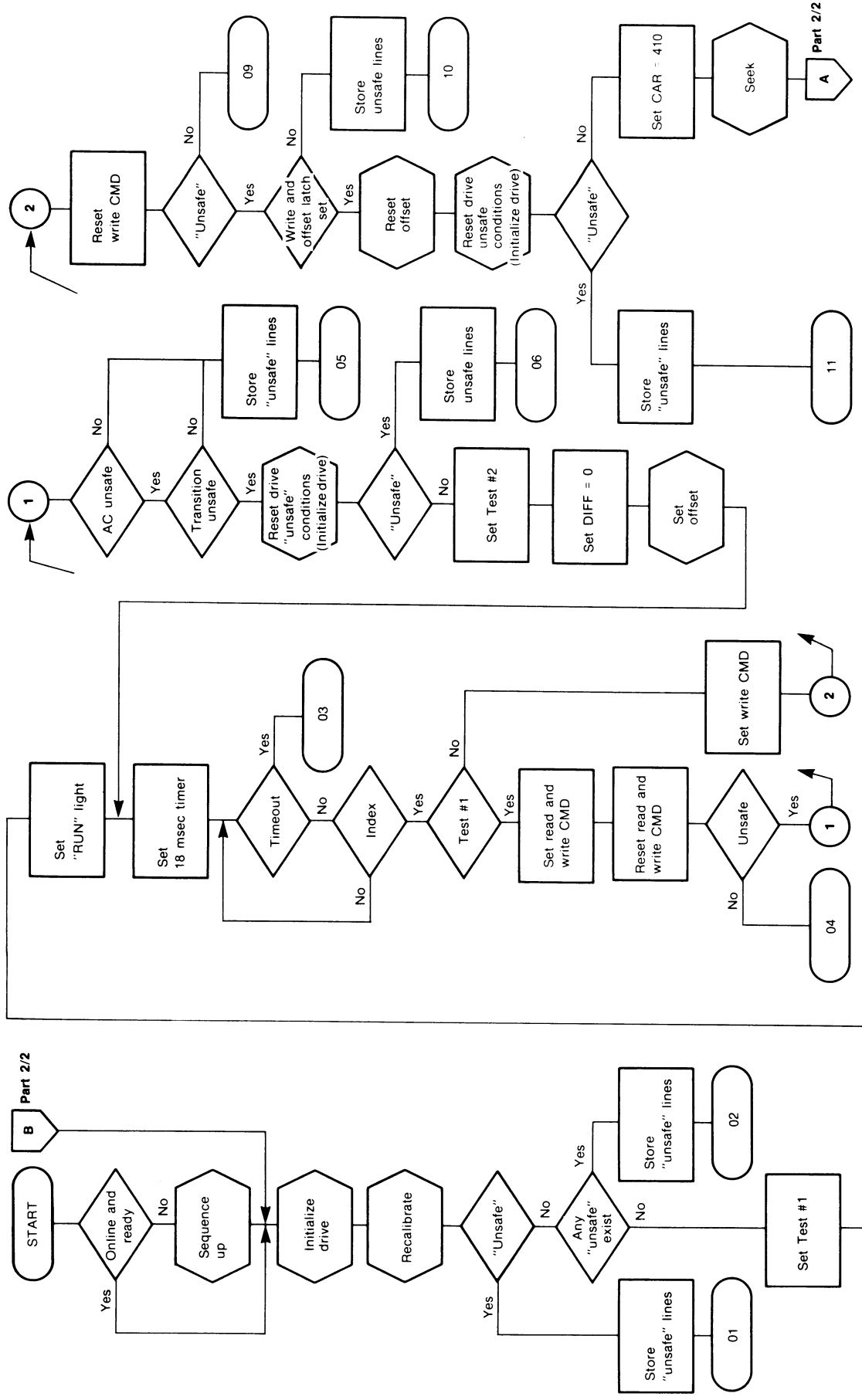
# Incremental Offset Read — Routine 09



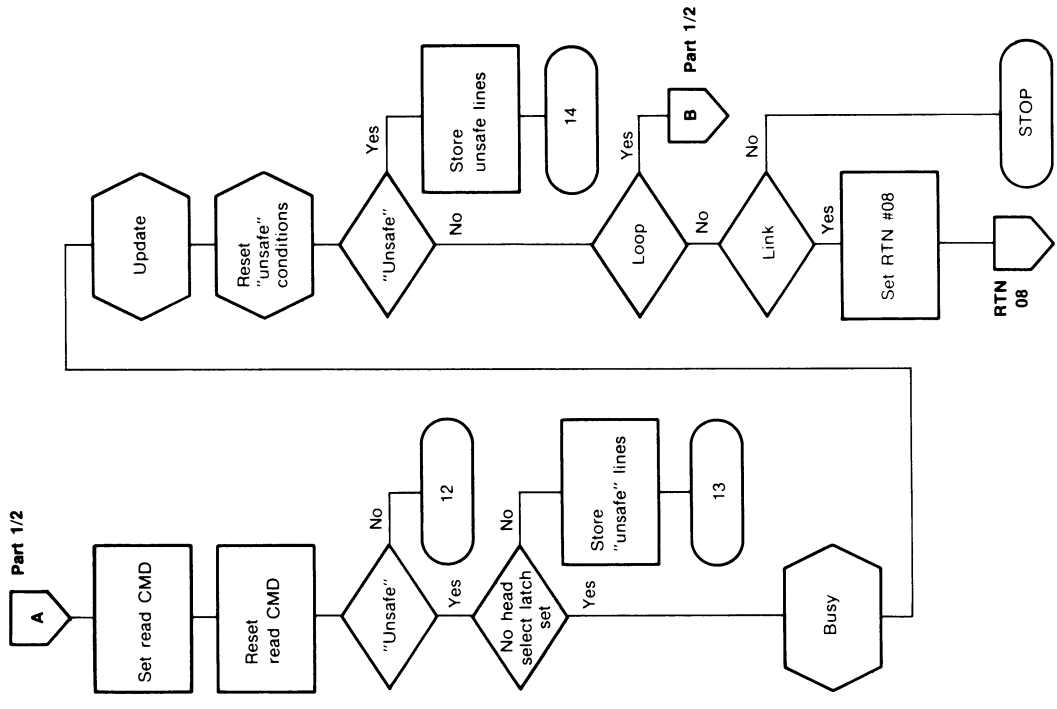
# Read 65K Times — Routine 0A



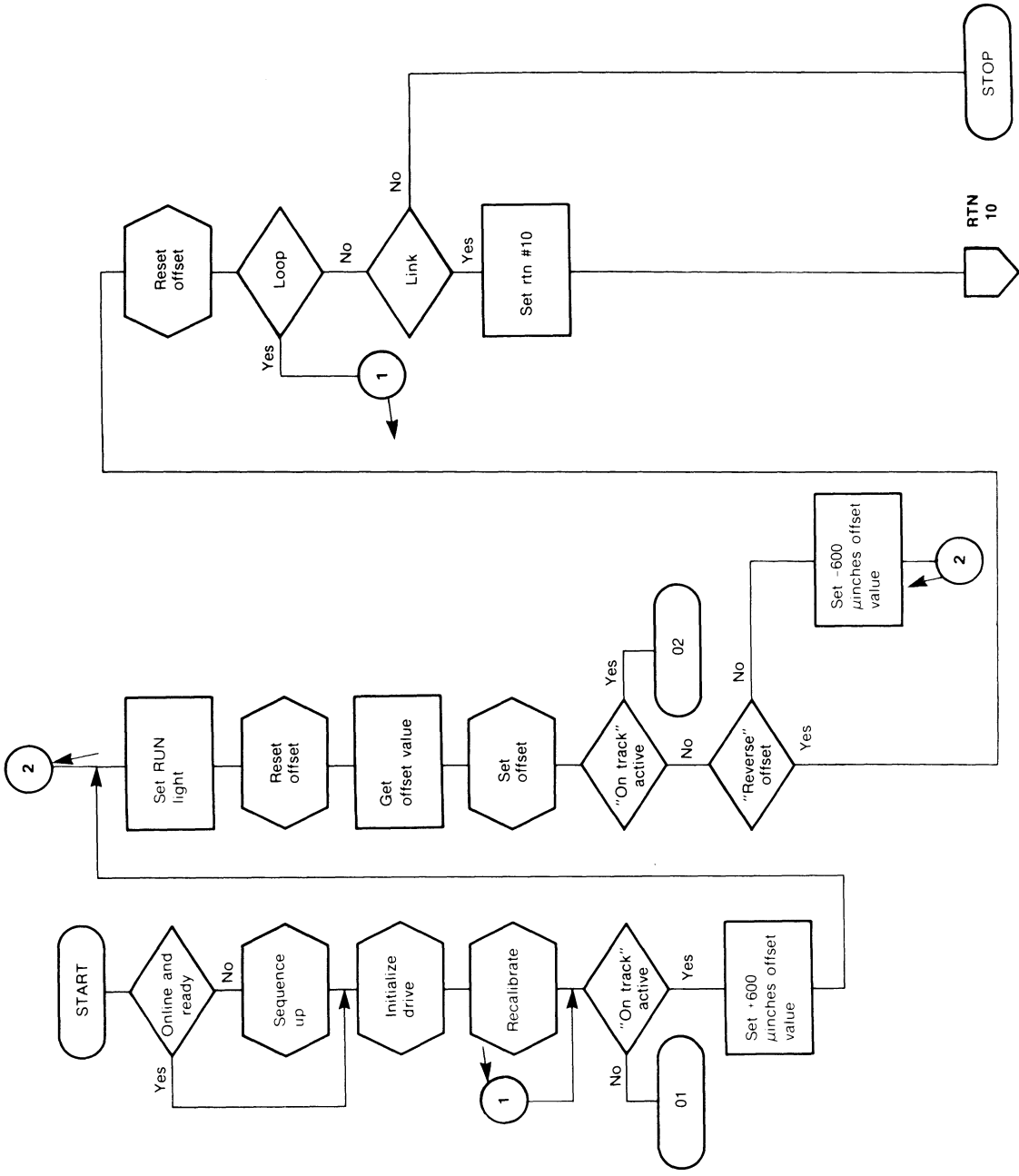
# Read/Write Safety — Routine 0B (Part 1 of 2)



# Read/Write Safety — Routine 0B (Part 2 of 2)

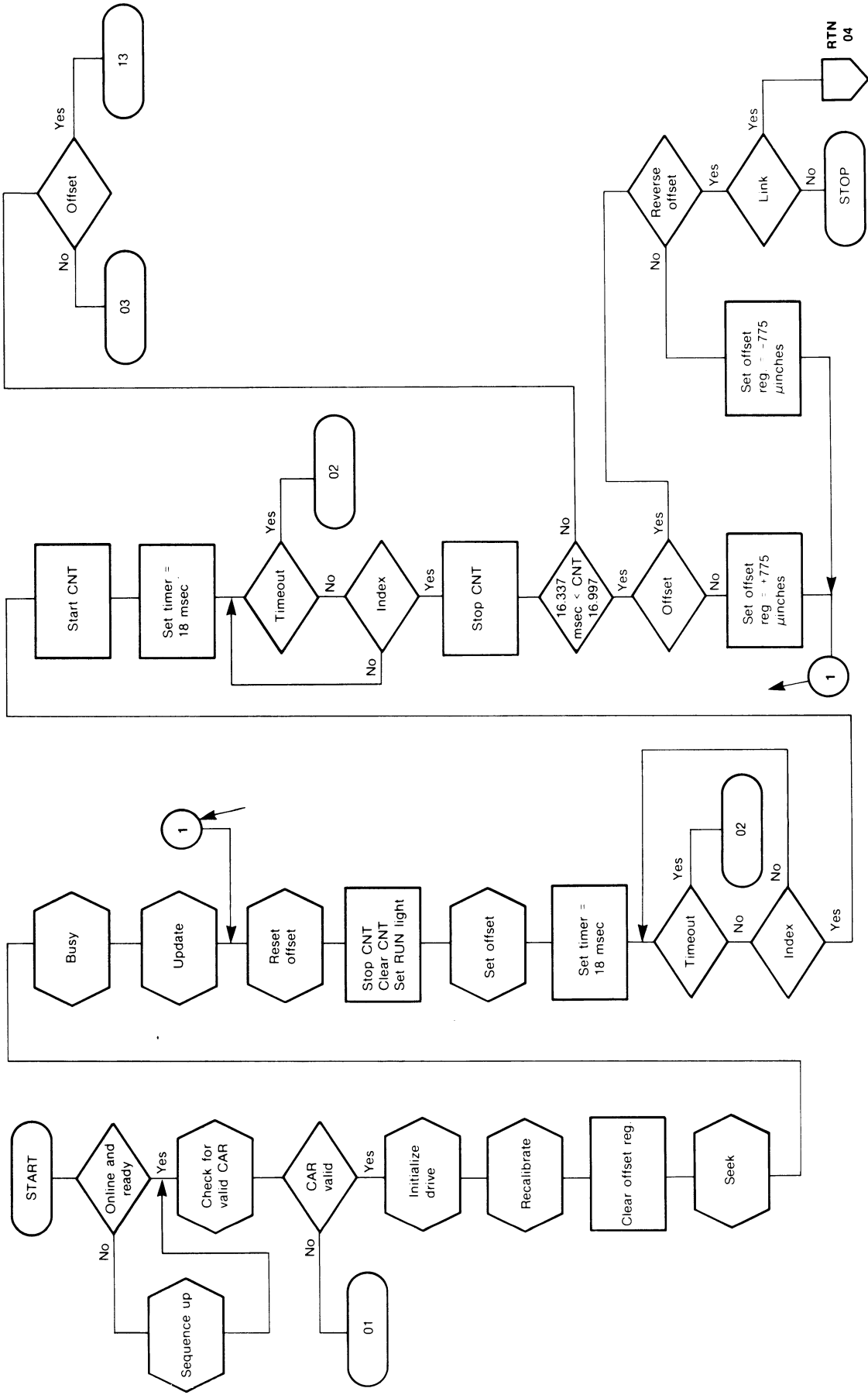


# Offset — Routine 0D

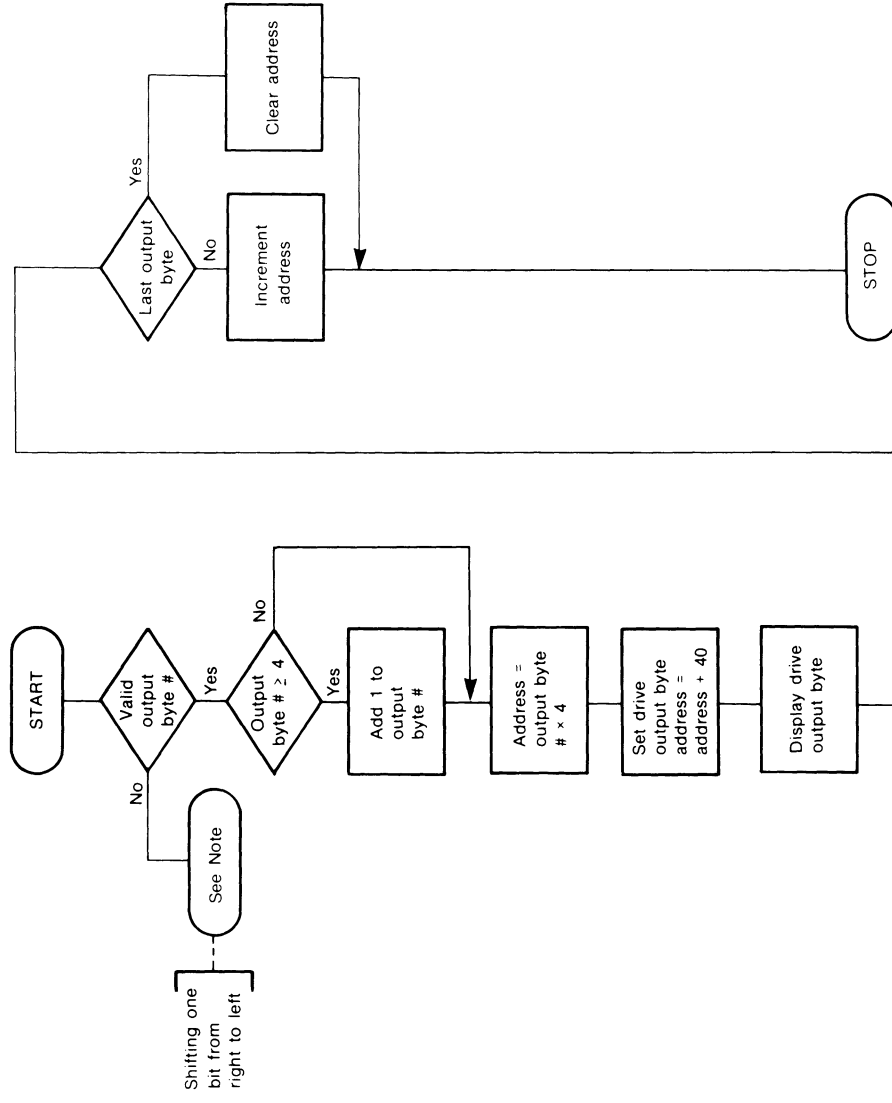




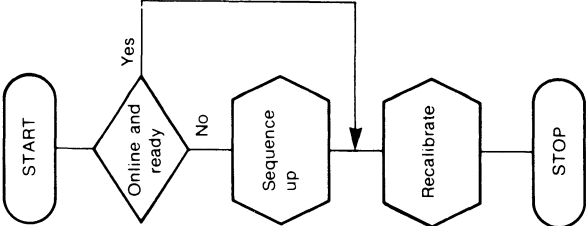
# Index — Routine 10



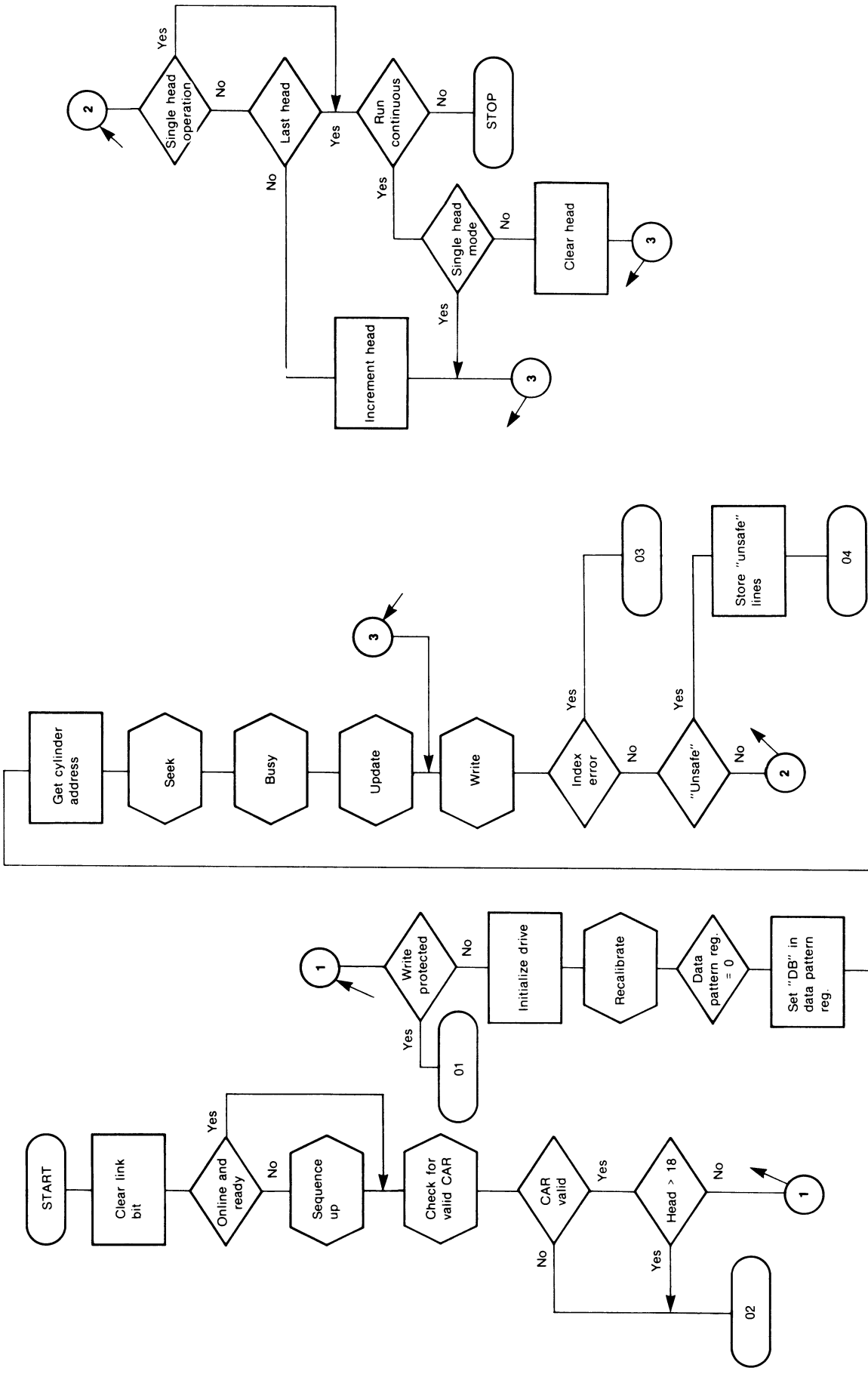
# Display Drive Output Byte — Routine 11



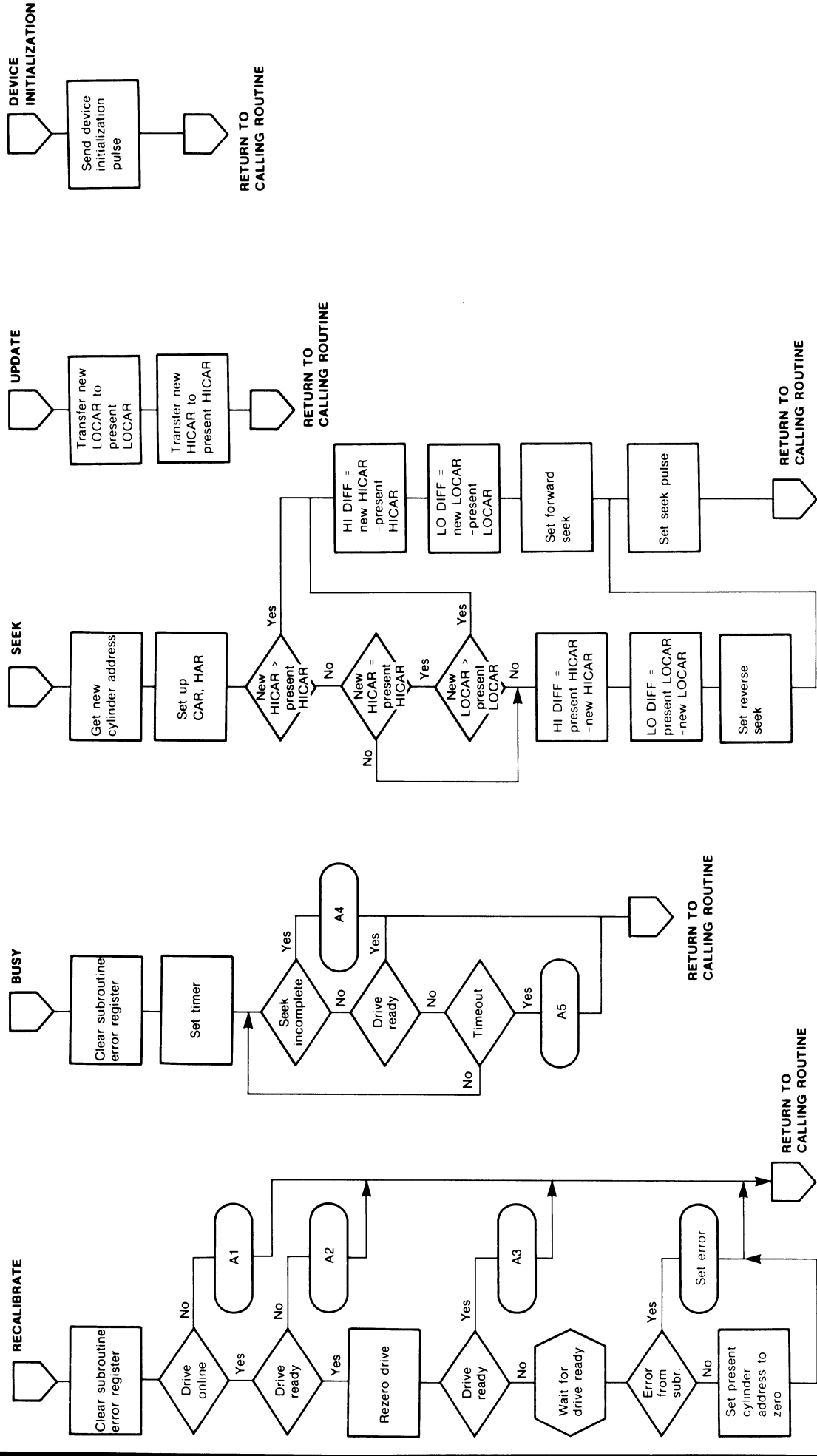
# Recalibrate — Routine 12



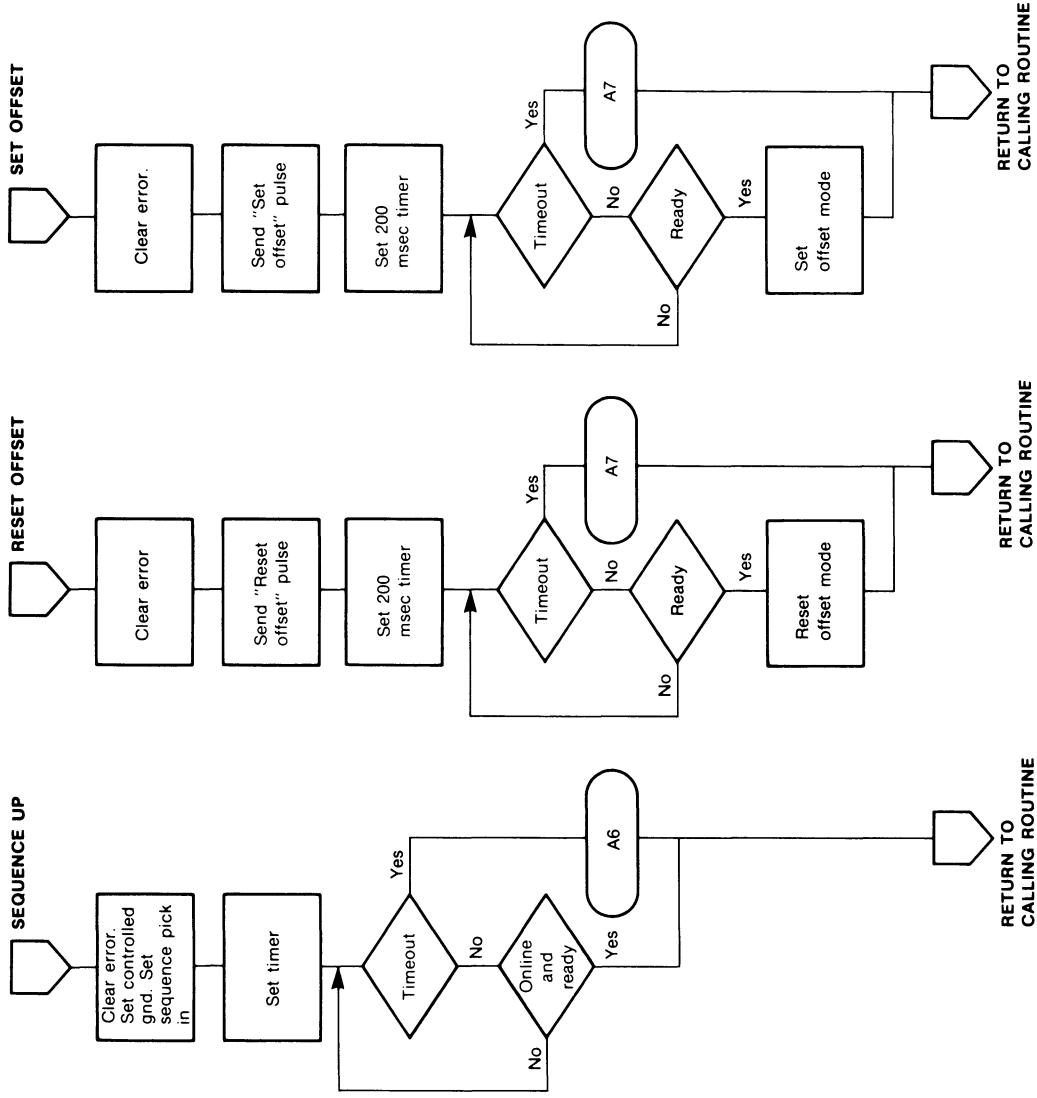
# Write — Routine 13



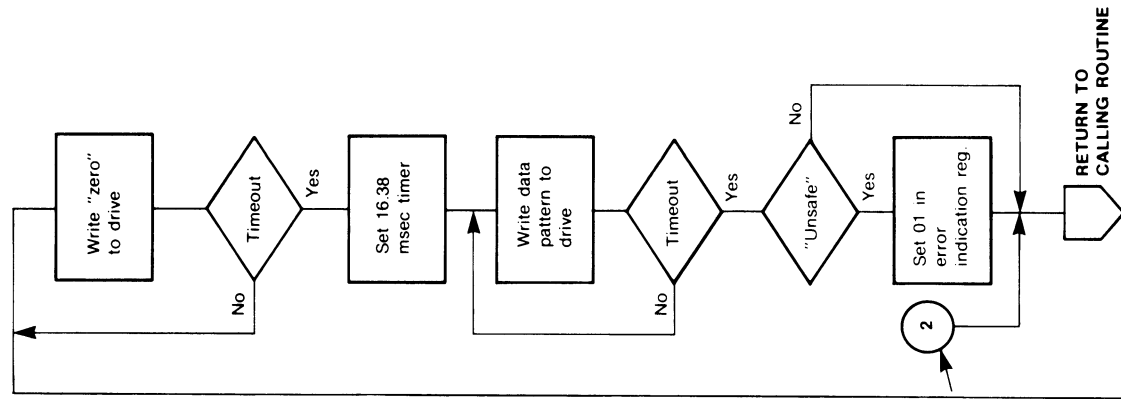
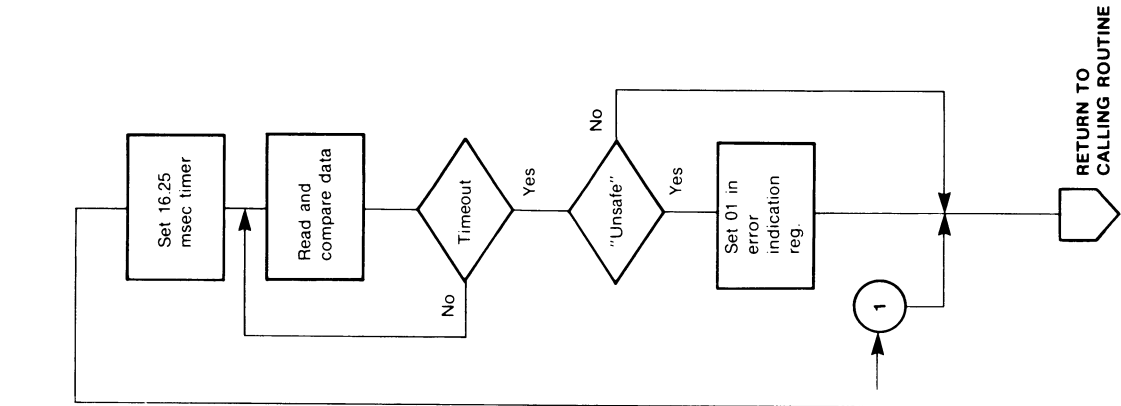
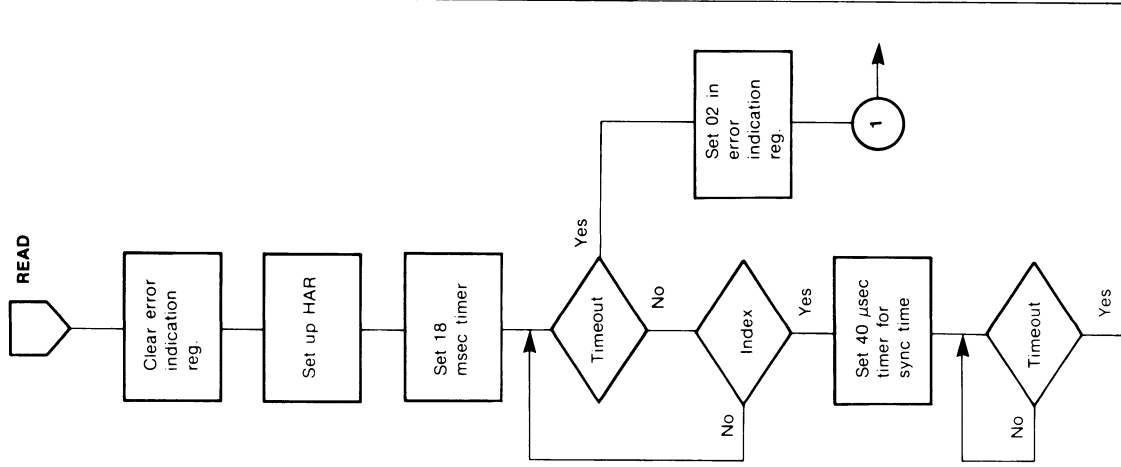
# Subroutines — (Part 1 of 3)



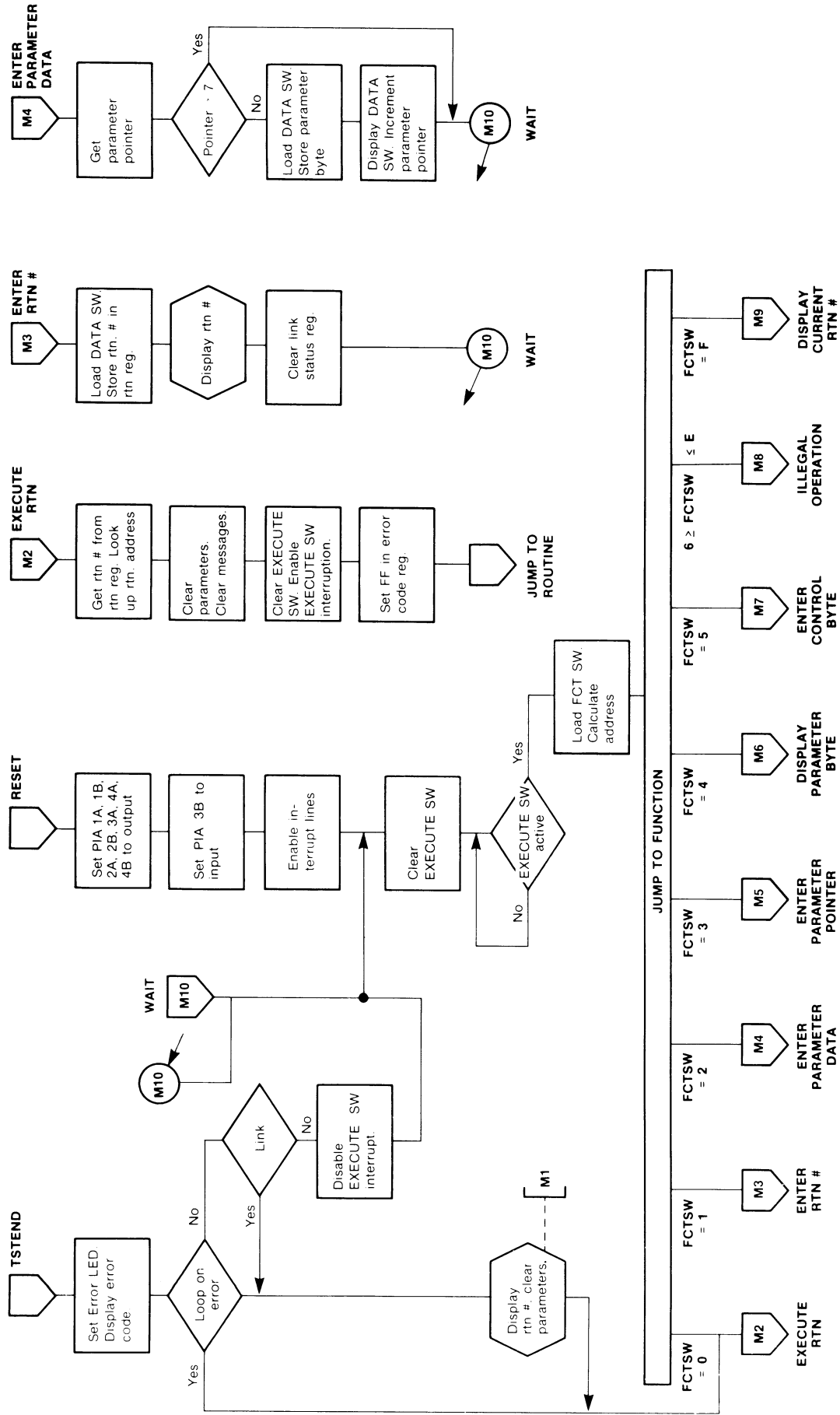
# Subroutines — (Part 2 of 3)



# Subroutines — (Part 3 of 3)

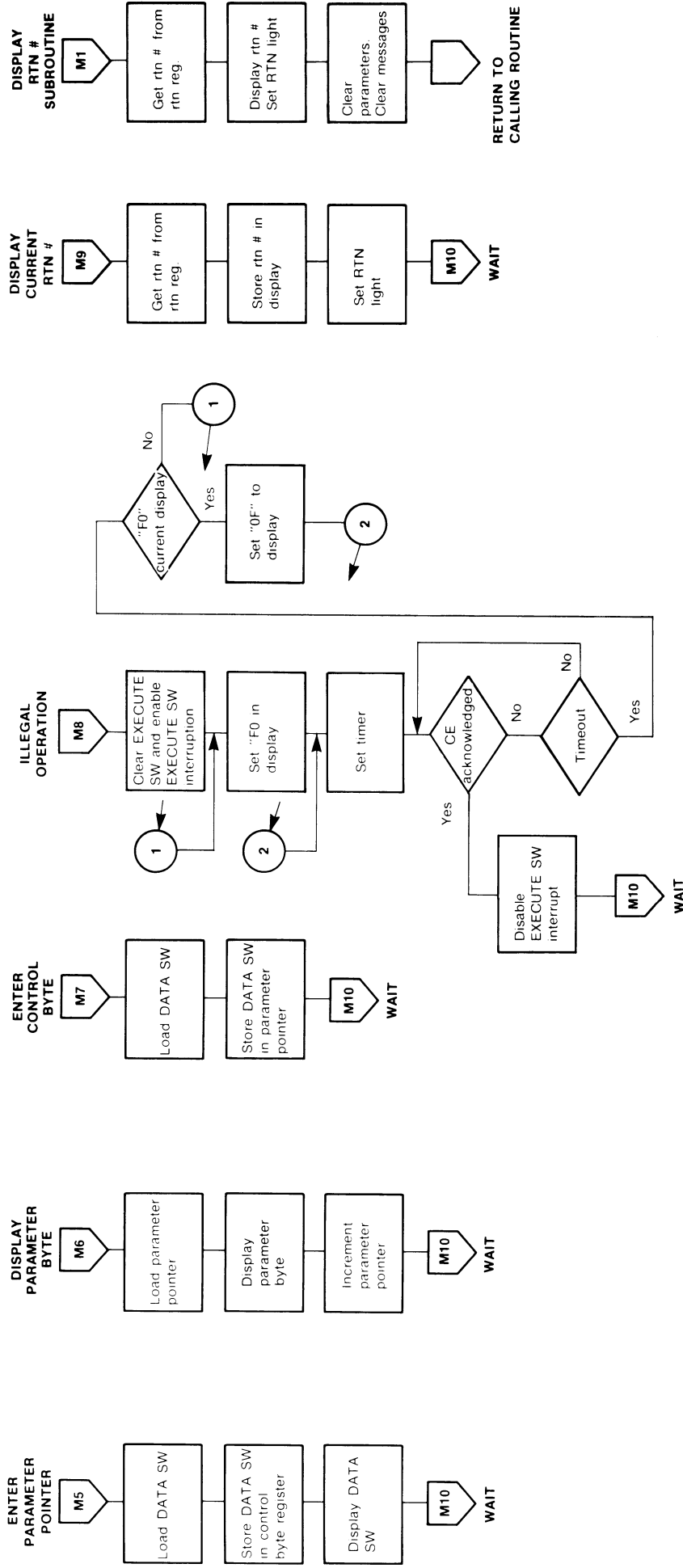


# Monitor — (Part 1 of 2)





# Monitor — (Part 2 of 2)





## APPENDIX C HEXADECIMAL-OCTAL CONVERSION

Since the Technical Manual contains many references to numbers in Hexadecimal form (base 16) rather than in Decimal (base 10), and DEC frequently uses an Octal form (base 8), the following conversion procedure may be useful to DEC personnel using this manual:

Decimal	Binary	Octal	Hexadecimal
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

To convert between Hexadecimal (Hex) and Octal, first convert to binary and then repartition. Example:

```

HEX   = | | | | 4 | | | | E | | | | B | | | | 5 | | | |
        | | | | | | | | | | | | | | | | | | | | | |
BINARY= | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
        | | | | | | | | | | | | | | | | | | | | | |
OCTAL = | | | | 4 | | | | 7 | | | | 2 | | | | 6 | | | | 5 | | | |
    
```



# Field Engineering Feedback Form

# TECHNICAL MANUAL

This form is an open pipeline to **Memorex** Engineering and Publications. Help us to help you in making problem analysis more effective by sharing any error information you have, such as:

- Indicated probable-failing unit did not correct the problem. (What did?)
- Fault isolation procedure hard to follow or not clear. (Please explain.)
- Don't understand the meaning. (Tell us where.)
- Personal techniques are better. (Send your suggested improvements.)
- Relevant information is missing. (Provide/identify it.)
- Unnecessary information is included. (Tell us where and why.)

677-01/51.20-01	PAGE <input type="checkbox"/> — <input type="checkbox"/>
DRIVE RP05 <input type="checkbox"/> RP06 <input type="checkbox"/>	FREQUENCY 50 HZ <input type="checkbox"/> 60 HZ <input type="checkbox"/>
SERIAL NUMBER <input type="text"/>	VOLTAGE <input type="text"/> VAC

Describe the machine problem.

Describe the maintenance or documentation problem.

Fill in your name and office address if you want an acknowledgement:


FOR PLANT USE ONLY:

Rec'd \_\_\_\_\_

Ack \_\_\_\_\_

Act \_\_\_\_\_

Chg \_\_\_\_\_

*All comments and suggestions become the property of Memorex.*

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