

3. (Continued)

ROM memory configuration continued - refer to Figure 2

J29, J15 - pin 23 - ROM address bit 9

J39, J33 - pin 21 - ground
J39, J34 - pin 21 - +3V
J39, J35 - pin 21 - ROM address bit 12
J39, J40 - pin 21 - +5V

J38, J33 - pin 19 - ground
J38, J34 - pin 19 - +3V
J38, J36 - pin 19 - ROM address bit 11

J37, J33 - pin 18 - ground
J37, J34 - pin 18 - +3V
J37, J35 - pin 18 - ROM address bit 12

4. Crystal Clock Option

- To connect 60Hz clock to BEVENT, wire-wrap J3 to J4.

5. Factory Configuration

J1 serial line

J23, J18 } address 176500 J45, J50 38.4K baud
J24, J19 }

J53, J57 } vector 300
J54, J52 }

J2 serial line

J28, J19 } J46, J48 9600 baud
J26, J15 } address 177560

J25, J14 } J6, J7 HALT on BREAK
J27, J13 } (framing error)

J56, J51 } vector 60
J54, J55 }

- Both serial lines have the following characteristics:

8 data bits, no parity, one stop bit J59, J61 J61, J62
J62, J64 J59, J66
J60, J63 J63, J65

- RAM is addressed at Bank 0

J30, J31 J32, J33 J31, J32

- ROM is addressed for TU58 bootstrap

J37, J38
J21, J22
J34, J37
J33, J39
J29, J15

- Clock to BEVENT is disabled.

3. ROM Memory Enable

- Address Response

	Wire-Wrap Pairs		
Bank 0	J20, J21	J10, J11	J29, J15
Bank 1	J20, J21	J 9, J11	J29, J15
Bootstrap Window (173000 or 773000)	J22, J21		

If using the MXV11-A2 bootstrap ROMs:

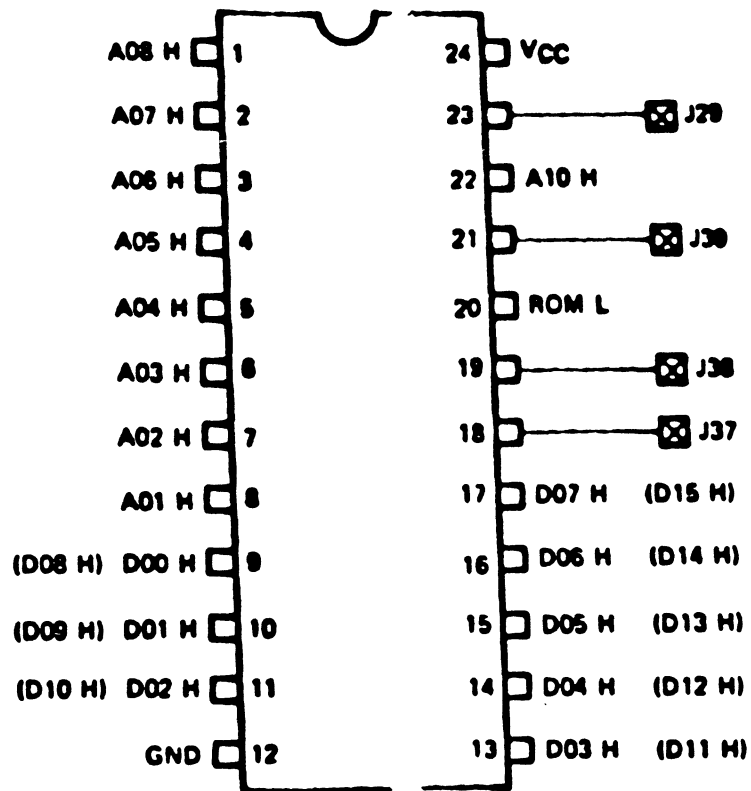
	Wire-Wrap Pairs	
Disk Boot	J22, J21 ✓	J16, J29 ✓
TU58 Boot	J22, J21	J15, J29

- To disable ROM memory:

wire-wrap pair J21, J8

- Configuring module for user ROMs

note: user must consult ROM vendor's spec. to determine the correct level for pins



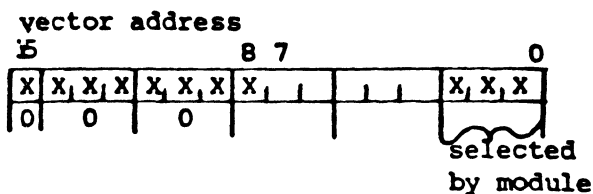
NOTE:

DATA OUT PINS SHOWN IN PARENTHESES REFER TO THE HIGH BYTE SOCKET XE67.
 DATA OUT PINS D00 H THRU D07 H REFER TO THE LOW BYTE SOCKET XE57.

MA 2267

Figure 2

1. (Continued)



Note on Wire-Wrapping:

Do not wrap more than two wires per post. Daisy-chain the wire-wraps to connect multiple pins.

- Baud Rate Selection

wire-wrap the appropriate pair:

	Printer J1	CONSOLE J2
150 baud	J45, J41	J46, J41
300	J45, J43	J46, J43
1200	J45, J42	J46, J42
2400	J45, J44	J46, J44
4800	J45, J47	J46, J47
9600	J45, J48	J46, J48
19.2 K	J45, J49	J46, J49
38.4 K	J45, J50	J46, J50

- Transmit/Receive Characteristics

wire-wrap the appropriate pair:

	J1	J2
8 data bits/no parity**	J62, J66	J59, J66
7 data bits/parity	J62, J65	J59, J65
two stop bits	J63, J66	J60, J66
one stop bit	J63, J65	J60, J65
even parity*	J64, J66	J61, J66
odd parity*	J64, J65	J61, J65

* if 7 data/parity option is selected

** odd or even parity must be selected, though ignored - i.e., the parity wire-wrap pins can't be left floating

- Console Operation - J2

wire-wrap pair:

boot on framing error (break) J6, J5
halt on framing error (break) J6, J7

2. RAM Memory

- Starting address selection; wire wrap the three pairs which correspond to the desired baud rate.

Starting Address	Bank	Wire Wrap Pairs		
000000	0	J32, J33	J31, J33	J30, J33
020000	1	J32, J33	J31, J33	J30, J34
040000	2	J32, J33	J31, J34	J30, J33
060000	3	J32, J33	J31, J34	J30, J34
100000	4	J32, J34	J31, J33	J30, J33
120000	5	J32, J34	J31, J33	J30, J34
140000	6	J32, J34	J31, J34	J30, J33
160000	7	J32, J34	J31, J34	J30, J34

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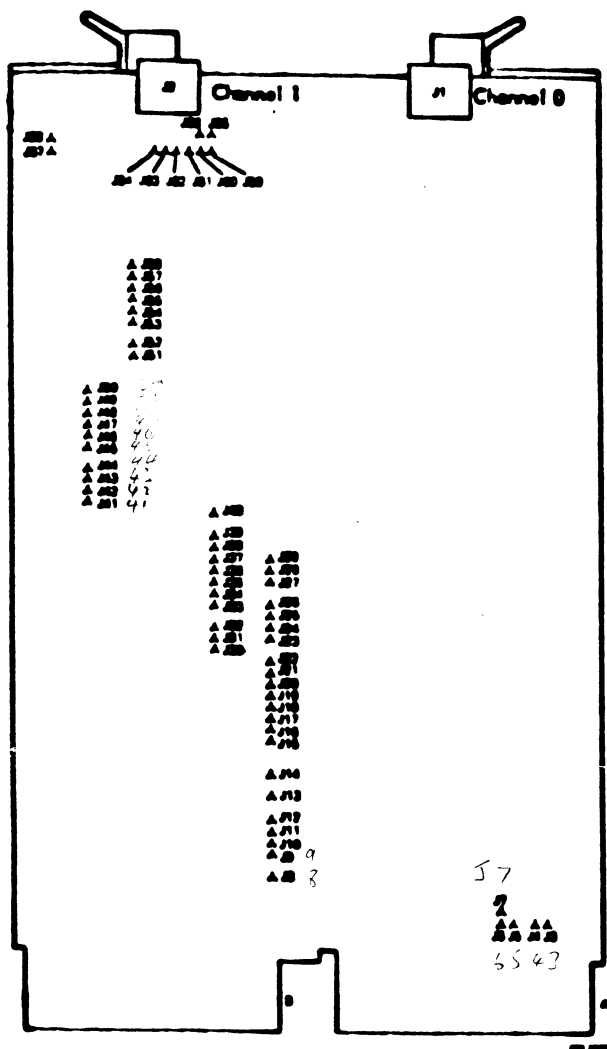


Figure 1

1. Serial I/O ports J1, J2

- only J2 may be used as the console

- Address Selection - J1

address bit

decoded as:

bit 3 → 1 J24, J12

→ 0 J24, J19

bit 4 → 1 J23, J13

→ 0 J23, J18

- Address Selection - J2

bit 3 → 1 J28, J12

→ 0 J28, J19

bit 4 → 1 J27, J13

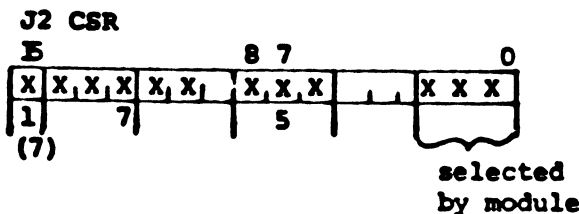
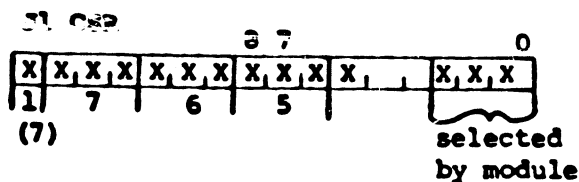
→ 0 J27, J18

bit 5 → 1 J25, J14

→ 0 J25, J17

bit 9 → 1 J26, J15

→ 0 J26, J16



- To disable the serial ports

channel	wire wrap
J1	J8 to J23 or J24
J2	J8 to J25, J26, J27, or J28

- Vector Address Selection

Note - Vectors for both I/O ports must be determined before the vector jumpers can be wire wrapped.

wire-wrap the appropriate pair:

	J1 = 0 J2 = 0	J1 = 1 J2 = 0	J1 = 0 J2 = 1	J1 = 1 J2 = 1
bit 3	J53, J57	J53, J51	J53, J52	J53, J58
bit 4	J54, J57	J54, J51	J54, J52	J54, J58
bit 5	J55, J57	J55, J51	J55, J52	J55, J58
bits 6 & 7	J56, J57	J56, J51	J56, J52	J56, J58