data products LSi®

ADM-3A

Maintenance Manual

TABLE OF CONTENTS

Section			Page
1	GENERAL DESCRIPTION		
	1.1	INTRODUCTION	1-1
	1.2	ADM-3A CAPABILITIES	1-1
	1.3	PHYSICAL DESCRIPTION	1-1
	1.4	SPECIFICATIONS	1-2
2	INSTALLATION		
	2.1	GENERAL	2-1
	2.2	VISUAL INSPECTION	2-1
	2.3	INSTALLATION	2-1
	2.4	SETTING INTERNAL SWITCHES	2-1
	2.5	SETTING FRONT PANEL SWITCHES	2-3
	2.6	SETTING DISPLAY CONTROL	2-4
	2.7	CONNECTING CABLES & TURNING ON POWER	2-4
3	OPERATION		
	3.1	GENERAL	3-1
	3.2	DISPLAYING CHARACTERS	3-1
	3.3	SPECIAL FUNCTION KEYS	3-1
	3.4	PROGRAMMING & WORD STRUCTURE	3-2
4	THEORY OF OPERATION		
	4.1	GENERAL	4-1
	4.2	GENERAL FUNCTIONAL DESCRIPTION	4-1
	4.3	LOGIC DESCRIPTION	4-1
5	MAINTENANCE		
	5.1	GENERAL	5-1
	5.2	INSTALLATION	5-1
	5.3	ROUTINE MAINTENANCE	5-1
	5.4	OPENING ADM-3A COVER	5-1
	5.5	ADJUSTMENTS	5-1
	5.6	CORRECTIVE MAINTENANCE	5-3
6	DRAWINGS		
	6.1	SCHEMATIC SHEET #2	
		SYSTEMS COUNTERS	6-1
	6.2	SCHEMATIC SHEET #12	
		INTERFACE CONTROL	6-1
	6.3	SCHEMATIC SHEET #3	
		CLEAR/ERASE LOGIC	6-3
		OFFSET COUNTER	6-4
		ROW COUNTER	6-4
		BEEPER CIRCUIT	6-5

TABLE OF CONTENTS (Continued)

Section			Page
	6.4	SCHEMATIC SHEET #4	
		COLUMN COUNTER	6-5
		WRITE-PULSE LOGIC	6-6
	6.5	SCHEMATIC SHEET #5	
		MEMORY ADDRESS GENERATION	6-6
	6.6	SCHEMATIC SHEET #6	
		DATA RECEIVER	6-7
		CHARACTER DECODERS	6-8
		LOAD CURSOR SEQUENCE DETECTOR	6-8
	6.7	SCHEMATIC SHEET #7	
		CLEAR CIRCUIT	6-8
		READ BACK	6-10
		MONITOR DRIVE SIGNALS	6-10
		CURSOR GENERATION	6-10
	6.8	SCHEMATIC SHEET #8	
		REFRESH MEMORY	6-10
		CHARACTER GENERATORS	6-11
		VIDEO SERIALIZER	6-11
		TRANSMIT DATA MULTIPLEXERS	6-11
	6.9	SCHEMATIC SHEET #9	
		KEYBOARD CIRCUIT	6-11
	6.10	SCHEMATIC SHEET #10	
		DATA TRANSMITTER	6-13
		CONTROL SECTION OF UART	6-13
		CURRENT LOOP XMTR/RCVR	6-14
		KEYBOARD LOCK CIRCUIT	6-14
	6.11	SCHEMATIC SHEET #11	
		BAUD RATE GENERATION	6-14
7		PARTS LIST	7-1
8		RETURNING EQUIPMENT FOR REPAIR	8-1
9		PAINT	9-1
APPENDICES			
A		TIMING	A-1
		MONITOR	A-2
		POWER SUPPLY	A-3
		P.C. BOARD ASSEMBLY	A-4
B		SCHEMATICS	B-1
C		OPTIONS	C-1
		WIRING DIAGRAMS	C-9

SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains a general description, installation and operating instructions, theory of operation, and maintenance information for the Lear Siegler ADM-3A Interactive Display Terminal.

Additional information is contained in the ADM-3A Operator's Handbook. The maintenance technician should be thoroughly familiar with material in the Operator's Handbook before attempting to troubleshoot or repair the ADM-3A.

1.2 ADM-3A CAPABILITIES

The ADM-3A has the following general capabilities:

a. Receives USASCII-coded data from a remote computer and displays it on a CRT screen displaying up to 1920 characters.

b. Permits the operator, using a keyboard, to compose a message, visible on the screen as it is transmitted to the remote computer or other device.

c. Through an extension port, permits interfacing with a hard-copy printer, magnetic tape recorder, or other terminals.

d. Provides for full-duplex or half-duplex communications, through either an RS-232C or current-loop interface.

e. Permits 202 communications line turnaround by means of either EOT or ETX code-turnaround (in which the controlling device transmits a turnaround code to give control to the device at the other end of the line), or secondary-channel turnaround (in which a secondary channel selection establishes control of a device for data transmission through the primary channel).

f. Allows the operator to select between a double underline cursor which enters data on the bottom line, or a reverse block cursor homed at the top left of the screen.

g. The terminal has the ability to recognize and position the cursor at any location on the screen.

h. The ADM-3A contains an overflow detector which causes wrap-around or scrolling on forward or downline operations and allows the cursor to be 'homed.'

1.3 PHYSICAL DESCRIPTION

Principal components of the ADM-3A are as follows:

a. A molded case comprising a base and a cover. The base contains the power switch, power transformer, beeper speaker, and intercomponent cabling. The main circuit board rests on supports molded in the base and is held in place by two guide pins.

The cover contains the monitor CRT and other monitor subassemblies. It is hinged at the rear so that all components of the ADM-3A are accessible when it is opened. The cover is easily removed by swinging it back as far as it will go, and then sliding it to the left, off the hinge pins. (The monitor-connecting cable must be disconnected.)

b. The main circuit board which contains all elements of the ADM-3A except monitor, power switch, line fuse and transformer, and beeper speaker. The keyboard consists of integrated key rows and is built directly on the main circuit board.

The main circuit board rests on supports within the base and is held in place by guide pins. Two connectors on the rear edge of the board provide the RS-232C and current loop (optional printer port) interface at both the main and extension ports.

c. The CRT monitor which comprises three subassemblies, as follows:

1. The CRT itself, which is mounted in a metal frame with its face held against the cover bezel by two brackets, each retained by a single screw.

2. A printed circuit board (video board), containing most circuits of the monitor. The video board is held in place by the cover molding on one side, and by pressure of the flyback assembly on the other.

3. The flyback assembly, which is held in place by a single screw. Bosses in the cover molding assembly surface retain the edge of the video board.

1.4 SPECIFICATIONS

DISPLAY

Screen

12-inch (diagonally measured) rectangular CRT with P4 white phosphor and etched non-glare surface.

Display Format

Standard:	960 characters, 12 lines of 80 characters
Optional:	1920 characters, 24 lines of 80 characters

Character Set

Generated:	128 ASCII characters (upper and lower case, numeric, punctuation and control)
Displayed:	Standard — 64 ASCII characters (upper case, numeric, punctuation)
	Optional — 95 ASCII characters (upper and lower case, numeric, punctuation)

Character Generation

5 x 7 dot matrix, 0.18 in. high x 0.075 in. wide

Cursor (2 modes)

(1) Underline, homes to lower left of screen
(2) Reverse block image, homes to upper left of screen

Data Entry

New data enters on progressive lines, top to bottom or on bottom line of screen. Line feed causes upward scrolling of entire display page with top-of-page overflow, if cursor is on bottom line.

Refresh Rate

60Hz or 50Hz, dependent on an internal switch set to match power line frequency.

KEYBOARD

59-key solid-state keyboard designed similar to a teletypewriter layout and containing the following keys:

47 alphanumeric keys	CTRL (Control)
RETURN	BREAK
LINE FEED	CLEAR
RUB	REPT (Repeat)
HERE IS	ESC (Escape)
SHIFT	Space Bar

COMMUNICATIONS

Modem Interface

EIA standard RS-232C and 20mA current loop (switch selectable)

Extension Interface

Extension RS-232C port for interfacing serial asynchronous auxiliary device (e.g., hard copy printer, magnetic tape recorder or additional data terminals).

Optionally, the extension port is available with both RS-232C and 20mA current loop interfaces.

Communication Rates

75, 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200 baud (switch selectable)

Send/Receive Modes

Full duplex and half duplex (switch selectable)

Word Structure

Total word length is switch selectable to 9, 10 or 11 bits consisting of the following:

7-bit data word	1 start bit
8th bit - parity, odd or even	1 or 2 stop bits
OR	
forced to 1 or 0	
OR	
8th bit suppressed	

PHYSICAL AND ELECTRICAL

Dimensions

13.5 in. high x 15.5 in. wide x 19 in. deep

Weight

25 pounds

Power Consumption

60 watts @115 Vac 10%

50Hz or 60Hz, switch selectable
Optional 230 Vac

Operating Environment

5 - 55°C (41 - 122°F), 5 - 95% relative humidity without condensation.

MONITOR ELECTRICAL SPECIFICATIONS

TABLE 1-1. MONITOR INPUT DATA SPECIFICATIONS

	Video	Vertical Drive Signal	Horizontal Drive Signal
Input Connector	(Necessary Accessory — Available) Printed circuit board card edge connector — Viking No. 2VK10S/1-2 or Amphenol No. 225-21031-101		
Pulse Rate or Width	Pulse Width: 100 nsec min.	Pulse Rate: 47 to 63 pulses/sec	Pulse Rate: 15,000 to 16,500 pulses/sec
Amplitude	Low = Zero $^{+0.4}_{-0.0}$ volts High = 4 ± 1.5 volts		
Signal Rise and Fall Times (10% to 90% amplitude	Less than 20 nsec	Less than 100 nsec	Less than 50 nsec

DATA DISPLAY SPECIFICATIONS

Input Impedance

	Minimum Shunt Resistance	Maximum Shunt Capacitance
(a) Video Input:	3.3 K ohms	40 pF
(b) Vertical Drive Input:	3.3 K ohms	40 pF
(c) Horizontal Drive Input:	470 ohms	40 pF

Video Amplifier

(a) Bandwidth:	12 MHz (—3 dB)
(b) Rise and Fall Times (10% to 90% amplitude):	Less than 35 nsec (linear mode)
(c) Storage Time:	315 nsec, maximum (linear mode)

Retrace and Delay Times

(a) Vertical:	900 sec retrace, maximum
(b) Horizontal:	7 sec retrace plus 4 sec delay, maximum

TABLE 1-2. CRT DISPLAY SPECIFICATIONS

Nominal Diagonal Measurement (inches)	Phosphor	*Resolution (TV Lines)	
		Center	Corner
12	P4	900 at 40 fL	800 at 40 fL

*Resolution is measured in accordance with EIA RS-375 except Burst Modulation (or Depth of Modulation) is adjusted for 100 percent.

Geometric Distortion

The perimeter of a full field of characters shall approach an ideal rectangle to within 1.5% of the rectangle height.

Power Requirements

Input Connector	Receptable, Molex No. 03-06-1041 Supplied with Unit Mating Plug, Molex No. 03-06-2041 — Necessary Accessory (Available)
Input Voltage	105 V to 130 V rms (120 V nominal); 50/60 Hz
Input Power	24W (Nominal)
Output Voltages	+15 V DC (short circuit protected) +12 kV DC; 12.6 V rms

ENVIRONMENTAL SPECIFICATIONS

Temperature (Chassis or Custom Unit)

Operating Range:	5°C to 55°C Ambient
Storage Range:	—40°C to 65°C

Humidity

5 to 95 per cent (Noncondensing)

Altitude

Operating Range:	Up to 10,000 feet

HUMAN FACTORS SPECIFICATIONS

X-Ray Radiation

These units comply with DHEW Rules-42-CFR-Part 78

SECTION 2
INSTALLATION

2.1 GENERAL

This section contains information to aid in installing the ADM-3A and preparing it for use. Included are instructions and information for inspecting the ADM-3A, installing it in a suitable environment, setting internal switches, connecting cables, and turning-on power.

2.2 VISUAL INSPECTION

It is recommeded that you save the original shipping carton and all packing materials to prevent damage should you wish to transport or ship the terminal.

Carefully inspect your ADM-3A for signs of damage during shipping. The terminal has undergone stringent quality inspections and operational tests prior to shipping; it left the factory in perfect operating condition.

If the unit is damaged, notify the carrier immediately. Save the damaged shipping container as evidence for inspection by the carrier.

Only the consignee may register a claim with the carrier for damage during shipment. However, Lear Siegler Data Products will cooperate fully with the customer should such action be necessary.

2.3 INSTALLATION

The ADM-3A is designed to operate in a wide range of environmental conditions:

5-55°C (41-122°F), 5-95% relative humidity without condensation.

The unit is designed to sit on a table or desk top, or any other suitable hard, flat surface.

CAUTION

In cold climates, care should be exercised to allow the temperature of the terminal to equalize with room temperature before removing the unit from the shipping carton; this will prevent moisture from condensing on a cold terminal exposed to warm air. Avoid operating the unit on a soft surface, such as carpeting, which would obstruct the flow of cooling air up through the bottom of the chassis. This could result in overheating and damage to the unit.

2.4 SETTING INTERNAL SWITCHES

Twelve slide switches located inside the ADM-3A case on the printed circuit logic board are used to select various terminal operating characteristics. These switches are set at the factory during pre-shipping checkout according to operating parameters specified by the customer when ordering the terminal. Only the parameters listed on the Ordering Form packed inside the shipping carton have been selected at the factory. Any required switch setting changes should be made before attempting to operate the terminal. Locations of the internal switches are shown in Figure 2-1.

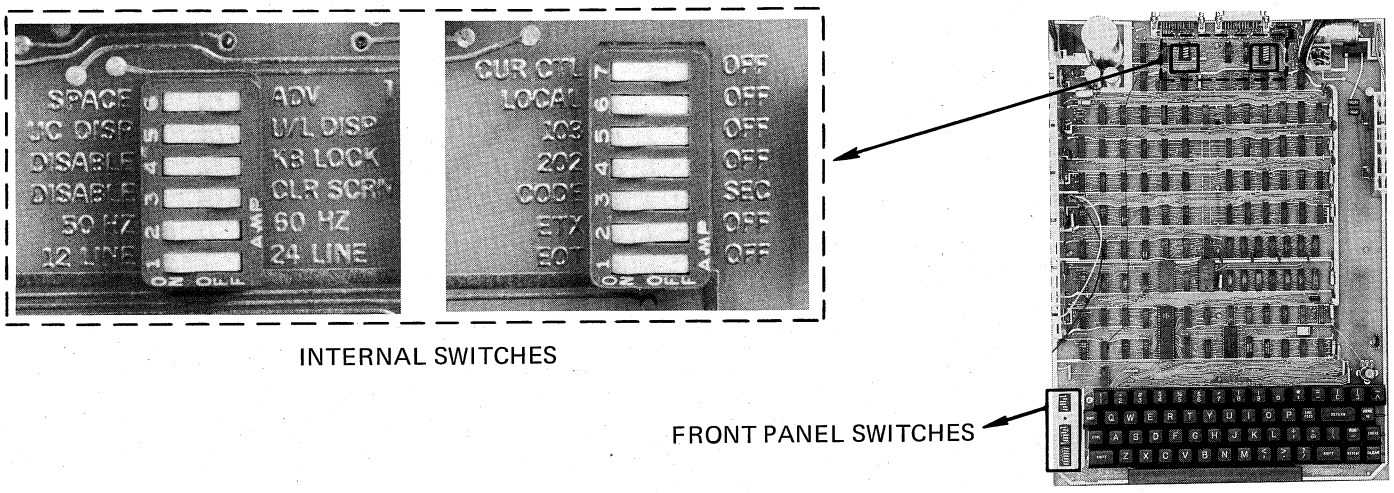


Figure 2-1. ADM-3A Internal Switches and Controls

WARNING

Always disconnect the ac power cord from the power source before opening the ADM-3A case to access any internal component.

Switch functions are described below:

SPACE — ADV

In SPACE position, selects destructive cursor. Pressing the space bar or receiving a space code ALWAYS overwrites the display memory location with a space code and advances the cursor.

In ADV position, selects non-destructive cursor between a Return and subsequent Line Feed only; the cursor may be advanced but a space code does not overwrite display memory locations. The space code is destructive between a Line Feed and the next Return.

UC DISP — U/L DISP

In UC DISP position, allows display of upper case characters only. Lower case codes are transmitted as such but are converted to upper case for display. If lower case is not installed or if it is not to be utilized, the switch must stay in the UC DISP position.

In U/L DISP position, allows display of upper and lower case characters if the terminal is equipped with the Upper/Lower Case option.

DISABLE — KB LOCK

In DISABLE position, prevents locking of keyboard.

In KB LOCK position, allows keyboard to be electrically disabled (locked) by remote control codes.

DISABLE — CLEAR SCREEN

In DISABLE position, prevents clearing of displayed information except by executing repetitive line feeds.

In CLEAR SCREEN position, allows computer to clear ADM-3A screen by transmitting a control code (CTRL Z).

50Hz — 60 Hz

Selects 50Hz or 60Hz display refresh rate; must be set to correspond with input power frequency.

12 LINE — 24 LINE

If terminal is equipped with 24-line display option, this switch may be used to select 12 or 24 line display.

On terminals with standard 12 line display this switch must be set to the 12 LINE position.

CURSOR CONTROL

In the ON position, this switch selects a moveable reverse block cursor which accesses any area on the screen.

In the OFF position, this switch selects the standard double-underline cursor. In this mode, data is entered from the bottom of the screen.

Upward scrolling and top-of-the-page overflow occur when a full line of data has been entered from the bottom line in either mode.

LOCAL — OFF
103 — OFF
202 — OFF

These three switches are used to select ADM-3A operation for one of the following methods of interfacing to the computer: (1) without modems (direct, local connection), (2) with 103-type modems, or (3) with 202-type modems. The appropriate switch is set (left position) according to the connection method used; the other two switches must be set to the OFF positions.

Setting the LOCAL switch causes line CA (Request to Send) to rise and fall with each character transmitted.

Setting the 103 switch holds CA high, if required.

Setting the 202 switch enables 202-type operation using the secondary channel or turnaround code to change the direction of data over the primary data channel (half-duplex operation).

With all three switches off, CA is held low all the time.

CODE — SEC CHAN

This switch is active only with the 202 switch (described above) in the on position. It is used to select the method of line turnaround for half-duplex operation with 202-type modems.

In SEC CHAN position, enables line turn-around using the secondary channel. 202 modem operation is summarized in the back of this handbook.

The CODE position allows line turnaround control by a turnaround code transmitted over the primary data channel. The turnaround code may be either EXT or EOT, as selected by the switches described below.

EXT—OFF
EOT—OFF

One of these two switches is set to the on (left) position to select the line turnaround code for primary channel operation with 202-type modems. (See CODE - SEC CHAN switch description.) With 202 and CODE selected, one of these switches must be on and the other off; with 202 and SEC CHAN selected, or 202 off, both the ETX and EOT switches must be set to the OFF positions.

2.5 SETTING FRONT PANEL SWITCHES

Twenty slide switches for selecting the primary terminal operating characteristics are accessible from the ADM-3A front panel without opening the case or removing power to the unit. To gain access to these switches, remove the screw securing the identification plate on the left side of the keyboard and remove the ID plate. The switches are shown in Figure 2-2.

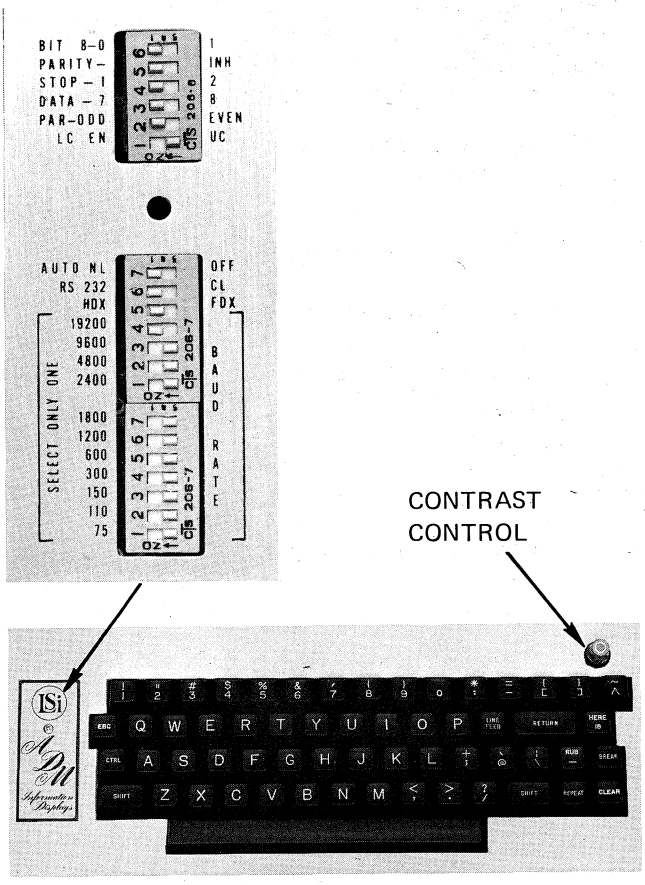


Figure 2-2. ADM-3A Front Panel Switches

It is recommended that you check the positions of these switches before operating the terminal for the first time. Switch functions are described below:

BIT 8-0—1

This switch has effect only with the DATA-7-8 switch in the 8 position.

In BIT 8-0 position, bit 8 is forced to a zero value on all transmitted characters.

In the 1 position, bit 8 is forced to a one value.

PARITY — INH

In PARITY position, the bit following the 7 - or 8 - bit data word is a parity bit (parity enabled).

In INH position, no parity bit will be generated (parity inhibited). The bit following the data word will be the (first) stop bit.

STOP - 1 — 2

In STOP-1 position, one stop bit is generated.

In the 2 position, two stop bits are generated.

DATA - 7 — 8

In DATA-7 position, 7-bit data word length is selected.

In the 8 position, 8-bit data word length is selected. (The 8-bit word consists of the standard 7-bit data word plus an 8th bit forced to one or zero according to the setting of the BIT 8-0 — 1 switch.)

PARITY-ODD — EVEN

This switch has effect only with the PARITY — INH switch in the PARITY position.

In PARITY-ODD position, selects odd parity.

In EVEN position, selects even parity.

LC EN — UC

In LC EN position, the SHIFT key is fully operational allowing generation of both upper and lower case alphabetic character codes.

In UC position, only upper case alphabetic characters will be generated regardless whether or not the SHIFT key is held down. The SHIFT key remains operational for all non-alphabetic keys.

AUTO NL — OFF

In AUTO NL position, typing in the 80th character position will automatically cause the cursor to move to the first position of the next line. If the cursor was previously on the bottom line, the display will scroll upward one line. The operator continues typing on the next new line.

In OFF position, the automatic New Line function is disabled. Continued typing at the 80th character position transmits each new character and changes the 80th character on the display.

RS232 — CL

In RS-232 position, selects RS-232C communications at the MODEM (computer) interface connector on the rear panel.

In CL position, selects 20mA current loop communications at the MODEM interface connector.

HDX — FDX

In HDX position, selects half duplex operation. Characters typed are transmitted and automatically echoed back from the ADM-3A I/O Channel for display.

In FDX position, selects full duplex operation. Characters typed are displayed only if echoed back by the computer or modem.

Communication Rate Switches

19200		
9600	B	These switches are used to select the send/receive rate for data communications with the computer and auxiliary device. Setting one switch to the left-hand (BAUD RATE) position selects the associated rate.
4800	A	
2400	U	
1800	D	
1200		
600	R	
300	A	
150	T	
110	E	
75		

NOTE

Only one BAUD RATE switch may be selected (left position) at a time.

2.6 SETTING DISPLAY CONTROLS

Contrast

The Contrast control is located to the right of the keyboard on the ADM-3A front panel. It is used by the operator to adjust brightness of the characters for optimum readability. The Contrast knob is turned clockwise to increase character brightness, counterclockwise to decrease brightness.

Background intensity

A Background Intensity potentiometer is located inside the ADM-3A case on the circuit board in the top of the case. (See Figure 2-1.) Background intensity is adjusted at the factory before the terminal is shipped and should not require readjustment prior to using the terminal.

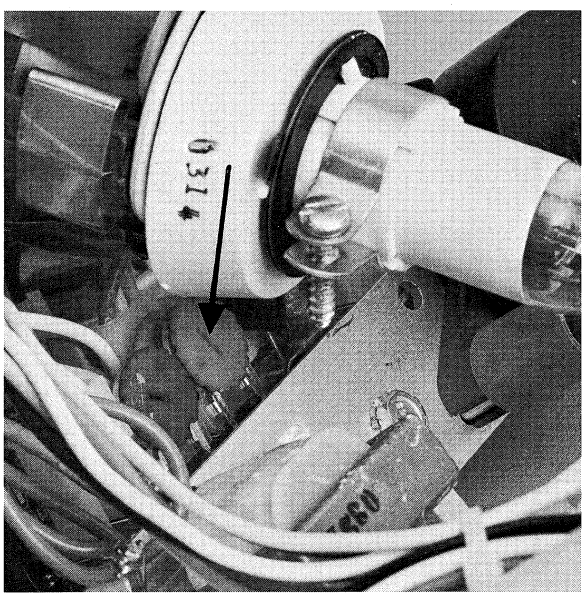


Figure 2-3. Background Intensity Control (located in top of case)

WARNING

Because the Background Intensity control must be adjusted with the ADM-3A case open with power on, it should be adjusted only by qualified service personnel.

ON/OFF Switch

The power ON/OFF switch is located on the ADM-3A rear panel.

2.7 CONNECTING CABLES AND TURNING ON POWER

a. With the ON/OFF switch in the OFF position, plug the ADM-3A power cord into the proper AC power outlet.

b. Connect the interface cable from the computer or modem to the MODEM interface connector on the ADM-3A rear panel.

c. Connect the interface cable from the auxiliary device (if present in your system) to the EXTENSION interface connector on the ADM-3A rear panel.

d. Check the settings of all front panel switches to verify that the terminal is set up for proper operation in your system. Make switch setting changes if necessary.

e. Set the ON/OFF power switch to the ON position.

f. Allow approximately 20 seconds for the unit to warm up.
   - If the cursor control mode has been selected, a reverse block cursor should appear in the upper left corner of the screen.
   - If the cursoe control mode is OFF an underline cursor should appear near the bottom left of the screen.
   - If the cursor does not appear, adjust the contrast control on the front panel for proper intensity.

NOTE

If the Full-Duplex mode is selected, typing at the keyboard will not display characters unless echo-back is provided by the computer or modem. If half-duplex is selected, data will be displayed only if clear-to-send is present or cable is disconnected.

SECTION 3
OPERATION

3.1 GENERAL

This section contains information and instructions for using the ADM-3A keyboard facilities, and for programming control functions at the computer. The keyboard allows the operator to generate and transmit to the computer (and/or auxiliary device) all 128 USASCII character codes.

3.2 DISPLAYING CHARACTERS

In the standard ADM-3A, 64 characters are displayed on the screen (upper case alphabet, numbers and most symbols and punctuation). When a non-displayable lower case character is typed, the proper lower case code is transmitted but the character is displayed as upper case.

If your terminal contains the Upper/Lower Case Display feature, 95 characters will be displayed (upper and lower case alphabet, numbers and all punctuation and symbols).

NOTE

Typing at the keyboard always generates codes which are transmitted; however, in order for characters to be displayed and control codes to affect the ADM-3A display the codes must be echoed back to the ADM-3A display memory and control logic, either by the computer (FDX) or the ADM-3A I/O Channel (HDX).

All display actions described in the key descriptions that follow assume the generated codes are echoed.

3.3 SPECIAL FUNCTION KEYS

In addition to the displayable character keys, the ADM-3A keyboard contains a number of other keys for various terminal and system control functions. Use of these keys is described below;

RETURN Key

A code is generated by this key which moves the cursor to the first character position of the line.

If the front panel SPACE-ADV switch is in the ADV position, the space code is non-destructive after typing the RETURN key; that is, the operator or computer can space over data on the line without overwriting each character with a space. The space bar remains non-destructive following a RETURN function until a LINE FEED code is generated.

LINE FEED Key

A code is generated by this key which causes the cursor to move downward one line. If the cursor was on the bottom line, the entire display will scroll upward one line. LINE FEED does not return the cursor to the first character position of the new line.

SHIFT Keys

Either of the two SHIFT keys is held down while typing another key to generate upper case alphabetic characters or to generate the character shown in the upper portion of a typed key.

NOTE

Setting the "LC EN — UC" switch under the front panel ID plate to the UC position causes upper case alphabetic characters to be generated with or without the SHIFT key depressed. The SHIFT key remains operational for all non-alphabetic keys.

RUB (Rubout) Key

When typed while holding down the SHIFT key transmits a non-displayable Rubout code (ASCII DEL) to the computer. The cursor is not advanced and the character code stored in the ADM-3A display memory is not overwritten.

The Rubout function is normally used to tell the computer that a previous character should be deleted.

The lower case RUB key transmits/displays an underline.

REPT (Repeat) Key

When held down while pressing a character key, repeats the character at a rate of 12.5 per second. (If the terminal is operating at a baud rate that will not permit 12.5 cps transmission, the repeat rate is reduced to the transmission rate.)

Space Bar

The Space Bar is considered a displayable character key.

Causes the ASCII code for a space to be transmitted and stored in the ADM-3A display memory and a blank space to appear on the screen. (For the only exceptions see RETURN Key).

CTRL (Control) Key

When held down while typing another key, modifies the code pattern of the typed key. The code is forced to one of the two control code columns in the ASCII Code chart.

The ADM-3A is capable of generating all 32 possible ASCII codes, although only 14 of them have a function within the machine. These are listed in Table 3-1.

Backspace (CTRL/H). Each time the H key is typed while holding down the CTRL key, the cursor moves non-destructively one character position to the left. The CTRL/H backspace code is transmitted to the computer. CTRL/H may be used in conjunction with the Repeat key.

Bell (CTRL/G) Sounds the audible beep in the ADM-3A and transmits the CTRL/G bell code.

UPLINE (CTRL/K)

When in the Cursor Control Mode, causes the reverse-block cursor to move upward one line.

Return (CTRL/M). Duplicates the function of the RETURN key.

Line Feed (CTRL/J). Duplicates the function of the LINE FEED key.

Lock Keyboard (CTRL/O). Electrically locks (disables) the ADM-3A keyboard, preventing any further keyboard activities. The keyboard can be unlocked by a control code from the computer, clearing the screen with the CLR key or by turning power off, then on again.

FORWARD SPACE (CTRL/M)

When in the Cursor Control Mode, causes the reverse block cursor to advance.

HOME CURSOR (RS)

When in the Cursor Control Mode, causes the reverse block cursor to return to the upper left corner of the screen.

ESCAPE KEY (ESC)

When in Cursor Control Mode, initiates a load-cursor sequence. ESC must be followed by an = character, a row code (SPACE through 7) and a column-code (SPACE through 0) to complete the sequence. In any mde, causes the ASCII ESCape code to be transmitted to the computer.

CLEAR Key

Typing the CLEAR key while holding down the SHIFT key clears the entire screen to spaces. (This function may be disabled by the internal CLEAR SCREEN — DISABLE Switch.)

HERE IS Key

If your terminal is equipped with the Automatic Answer Back feature, typing this key transmits an identification message (stored in the ADM-3A in a special memory) to identify your terminal and alert the computer that a message is to follow.

In terminals without Automatic Answer Back capability, this key has no function.

BREAK Key

This key activates the standard teletypewriter Break function, normally used to interrupt an incoming message.

NOTE

The Break function is sustained as long as the BREAK key is held down. Holding the key down for an extended period may cause the computer to disconnect from your terminal.

3.4 PROGRAMMING & WORD STRUCTURE

The computer to which the ADM-3A is interfaced has full control over the terminal. All control functions which are possible from the ADM-3A keyboard, plus a few additional functions, can also be executed from the computer.

The computer controls the ADM-3A by transmitting the appropriate ASCII codes. Displayable character codes will be displayed, and valid control codes will be recognized and acted upon.

3.4.1 Remote Control Functions

The remote computer can perform the following control functions:

Backspace BS (CTRL/H). Moves the cursor non-destructively one character position to the left.

Bell BEL (CTRL/G). Sounds the audible beep in the ADM-3A.

Return CR (CTRL/M) Moves the cursor non-destructively to the first character position of the present line.

Line Feed LF (CTRL/J). Causes the entire display to move upward one line, leaving the cursor positioned in the same character position on the next new line.

Upline (VT) — Moves cursor up vertically when in Cursor Control Mode.

Forward Space (FF) — Moves cursor forward when in Cursor Control Mode.

Lock Keyboard SI (CTRL/O). Electrically locks the ADM-3A keyboard, disabling all keyboard functions.

Unlock Keyboard SO (CTRL/N). Unlocks the ADM-3A keyboard, restoring all keyboard functions.

Clear Screen SUB (CTRL/Z). Clears all character positions in the ADM-3A display memory and clears the screen to blank spaces. (This function may be disabled by the internal (DISABLE — CLEAR SCREEN switch.)

Home Cursor (HOME) — Causes the cursor to return to the upper left corner of the screen, when in the Cursor Control Mode.

Load Cursor (ESC = YX) — This four-character sequence causes the cursor to be positioned to the row and column defined by the ASCII values of Y and X respectively.

The Reference Tables 3-1 and 3-2 of this manual show the actual binary codes generated by the ADM-3A and used for computer control of the terminal.

Table 3-1. ADM-3A Control Codes

Code	ASCII Mnemonic	Function ADM-3A
CTRL/@	NUL	
CTRL/A	SOH	
CTRL/B	STX	
CTRL/C	ETX	Available as secondary channel line turnaround code for 202 modem operation
CTRL/D	EOT	Available as secondary channel line turnaround code for 202 modem operation
CTRL/E	ENQ	Initiates ID message in terminals with automatic "Answer Back" option*
CTRL/F	ACK	
CTRL/G	BEL	Sounds audible beep in ADM-3A
CTRL/H	BS	Backspace
CTRL/I	HT	
CTRL/J	LF	Line Feed
CTRL/K	VT	Upline
CTRL/L	FF	Forward Space
CTRL/M	CR	Return
CTRL/N	SO	Unlock Keyboard*
CTRL/O	SI	Lock Keyboard*
CTRL/P	DLE	
CTRL/Q	DC1	
CTRL/R	DC2	
CTRL/S	DC3	
CTRL/T	DC4	
CTRL/V	NAK	
CTRL/V	SYN	
CTRL/W	ETB	
CTRL/X	CAN	
CTRL/Y	EM	
CTRL/Z	SUB	Clear Screen
CTRL/[	ESC	Initiate Load Cursor
CTRL/×	FS	
CTRL/]	GS	
CTRL/^	RS	Home Cursor

*Executable only from computer.

Table 3-2 USASCII Character Codes

		CONTROL		GRAPHIC CHARACTER SET					
BITS	BITS	0	1	2	3	4	5	6	7
4321	765	000	001	010	011	100	101	110	111
0000		NUL	DLE	SP		@	P	`	p
0001		SOH	DC1	!	1	A	Q	a	q
0010		STX	DC2	"	2	B	R	b	r
0011		ETX	DC3	#	3	C	S	c	s
0100		EOT	DC4	$	4	D	T	d	t
0101		ENQ	NAK	%	5	E	U	e	u
0110		ACK	SYN	&	6	F	V	f	v
0111		BEEP	ETB	'	7	G	W	g	w
1000		BS	CAN	(	8	H	X	h	x
1001		HT	EM	)	9	I	Y	i	y
1010		LF	SUB	*	:	J	Z	j	z
1011		VT	ESC	+	;	K	[	k	{
1100		FF	FS	,	<	L	\	l	|
1101		CR	GS	-	=	M	]	m	}
1110		SO	RS	.	>	N	^	n	~
1111		SI	US	/	?	O	+	o	DEL

Control Codes (Generated by holding CTRL key while typing the corresponding key shown in columns 4 and 5.)

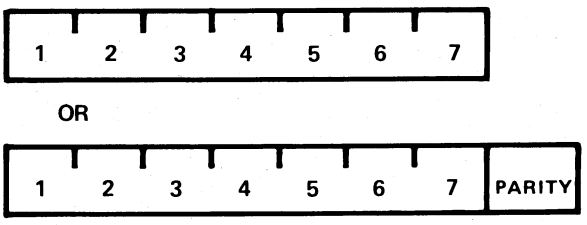
Displayable in standard ADM-3A

Displayable with ADM-3A Upper/Lower Case Display feature.

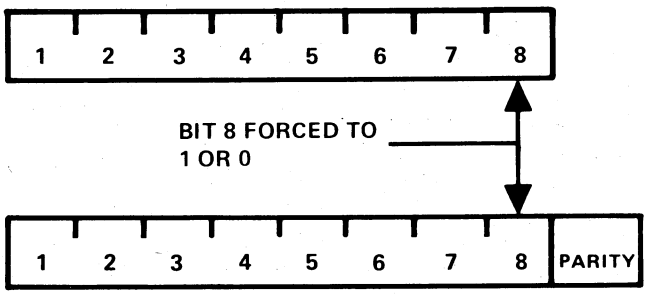
3.4.2 Data Character Format

The ADM-3A uses USASCII (United States of America Standard Code for Information Interchange). USASCII is a 7-bit code. But because many of the computers and other devices to which the ADM-3A may be interfaced use 8-bit words (plus parity or without parity), the ADM-3A offers a wide choice of word formats selectable by the user.

The data character may be 7 bits in length, with or without an optional parity bit generated on transmission:

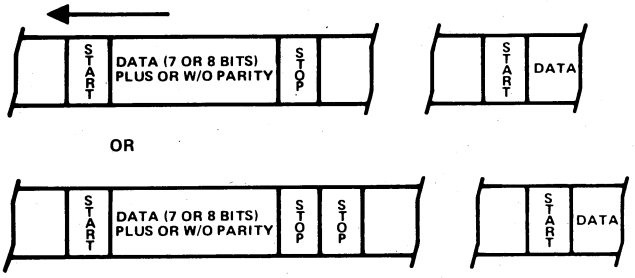


The data character may be 8 bits in length, plus or without the optional parity bit. In the case of 8-bit characters, bit 8 is always forced to 1 or 0 as selected by the user.



3.4.3 Data Transmission Format

The ADM-3A uses asynchronous transmission. This means each character is transmitted as a complete, self-contained message consisting of the data character with or without parity, preceded by a start bit and followed by one or two stop bits.



When the start bit is received, a clock signal is initiated to clock in the remainder of the word. The one or two stop bits are used to signify the end of the word and terminate the receive clock.

Generally, transmission rates of 110 baud and lower use two stop bits, and rates of 150 and higher use one stop bit.

The ADM-3A control codes and the USASCII code set are shown in tables 3-1 and 3-2, respectively.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

This section describes the manner in which the ADM-3A performs its different functions. Logic is first described with reference to an overall block diagram, and then each element shown in the block diagram is described with reference to specific illustrations and to logic diagrams contained in Section 6 of this manual (Drawings).

4.2 GENERAL FUNCTIONAL DESCRIPTION

The general organization of logic in ADM-3A is shown in figure 4-1. This figure divides ADM-3A logic into functional blocks and shows the relationships between blocks. It also indicates the sheet of the logic diagram on which logic in any block is detailed.

4.2.1 Display Generation

Signals that cause a display to be generated and maintained on the screen are furnished by a string of counters (display counter logic).

The first counter (the dot counter) is clocked by pulses from an oscillator. This clock is the primary timing signal in the ADM-3A. The purpose of the dot counter is to time the presentation of the sequential address to the character generator and the presetting of the video serializer. Each increment of the counter defines the position of a single dot in any line (dot row) of any character in the display. Any character is made up of a 5 x 7 array of dots (figure 4-2). A character position is seven dots wide and nine dots high to provide 2-dot spacing between characters both horizontally and vertically.

A single horizontal sweep of the CRT beam produces all dots in a given dot row for all characters in the character row. The character dot counter is incremented for every seventh dot column to define the position of each character in the row. At the end of each dot row, the line counter is incremented and the next dot row is scanned out. The character row counter is incremented by every ninth dot line to define the position of the next character row.

The four display counter outputs control memory addressing, character generation, and many other functions of ADM-3A logic.

4.2.2 Display Refresh Operation

Except when received data is being loaded, the contents of the refresh memory (an entire "page" of data) are continuously presented on the screen. Memory address logic requires only sequential character and row counts (CCn and RCn) to read out the memory contents to the storage latches.

Each character read from the refresh memory is stored for presentation to the ROM character memory (and to data transmitter logic for read-back test operation).

The ROM character generation decodes the stored USASCII-coded character and produces a five-bit output specifying dots to be displayed for each dot row. That is, the character is presented to the ROMs for each dot row as the character row is generated. The count CCn selects the dot pattern for each dot row.

4.2.3 Monitor Video and Drive Circuits

The 5-bit dot row data read from the ROM character generator is presented to the monitor video circuits as a serial data stream, continuous except during CRT retrace periods. Character position and row counts are used to generate CRT sweep drive signals, with horizontal drive triggered by the start of each dot row, and vertical drive triggered when the character row count reaches 12 (standard) or 24 (optional).

4.2.4 Receiving and Storing Data

Data transmission rates are selected in the ADM-3A to match those devices on the other end of the line. Baud rates are derived from the LSB of the dot count, DC1. The receive clock and the transmit clock may be the same or different rates (split baud rate option).

Received data is clocked into the refresh memory, which is addressed by memory address logic. The memory address, during loading, is formed by summing the Cursor Row Position Count (CRn) which represents the true position of the cursor on the screen, and the Offset Count (OCn), which represents the number of lines (since Reset) that the display has scrolled. The virtual address which is thus derived corresponds to the refresh address for that data row. The Refresh Address is determined

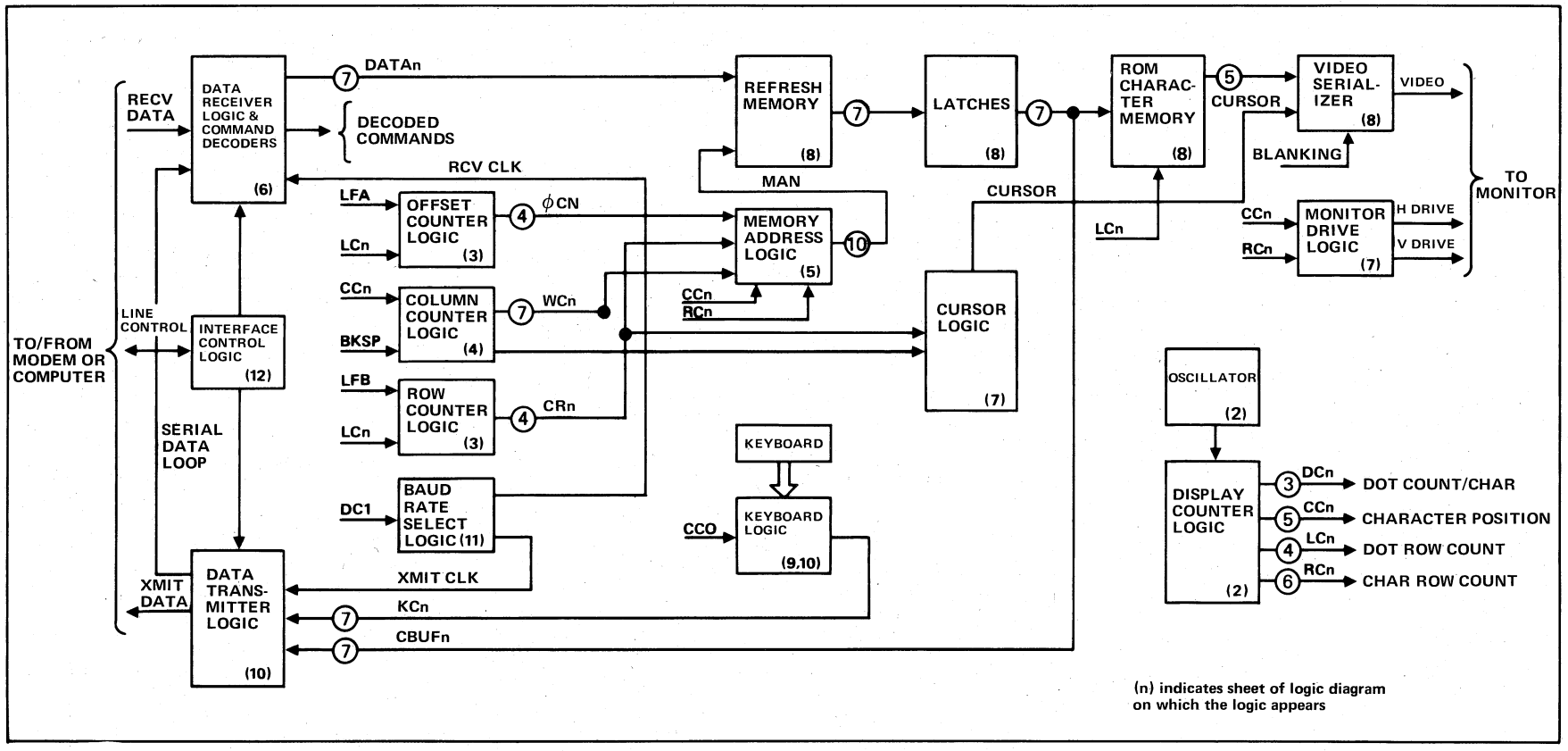


Figure 4-1. ADM-3A Interactive Display Terminal, Functional Block Diagram

by another circuit which sums the current Display Row Count (RCn) and the Offset Count (OCn).

Received commands are decoded and used to control ADM-3A logic. Commands include Line Feed, Backspace, Carriage Return, and other functions.

4.2.5 Cursor Generation

The cursor marks the position on the display in which the next character will appear. When the Cursor Control switch is in the OFF position, data will be entered in the bottom row: Line Feed will cause the display to roll upward. The cursor is formed by displaying five dots in the eighth and ninth dot rows of the character position in which it rests. Cursor information is ORed into video output logic along with character bits read from the ROMs.

When the Cursor Control is in the ON position, the reverse block cursor is a 7 x 9 dot figure containing the reverse image of the character upon which the cursor currently resides.

The cursor position code WCn is used to address the refresh memory in read-back test operation.

4.2.6 Keyboard Logic

The keyboard and associated logic are used to compose data for display and simultaneous transmission. As a character is typed by the operator, it appears (as KCn) at data transmitter logic, and (in half-duplex transmission) is loaded into the refresh memory for display. In full-duplex, communications characters originating at the keyboard appear on the display only if they are echoed back from the computer or modem.

4.2.7 Data Transmitter Logic

Data transmitter logic receives characters generated at the keyboard (or generated at optional answerback logic and put on KCn lines) and converts the seven-bit character into serial-bit form along with start, parity, and stop bits, and sends the formatted data word to the modem or computer.

In read-back test operation, the contents of the memory buffer (CBUFn) may be accepted for transmission in the same manner as data on the KCn lines.

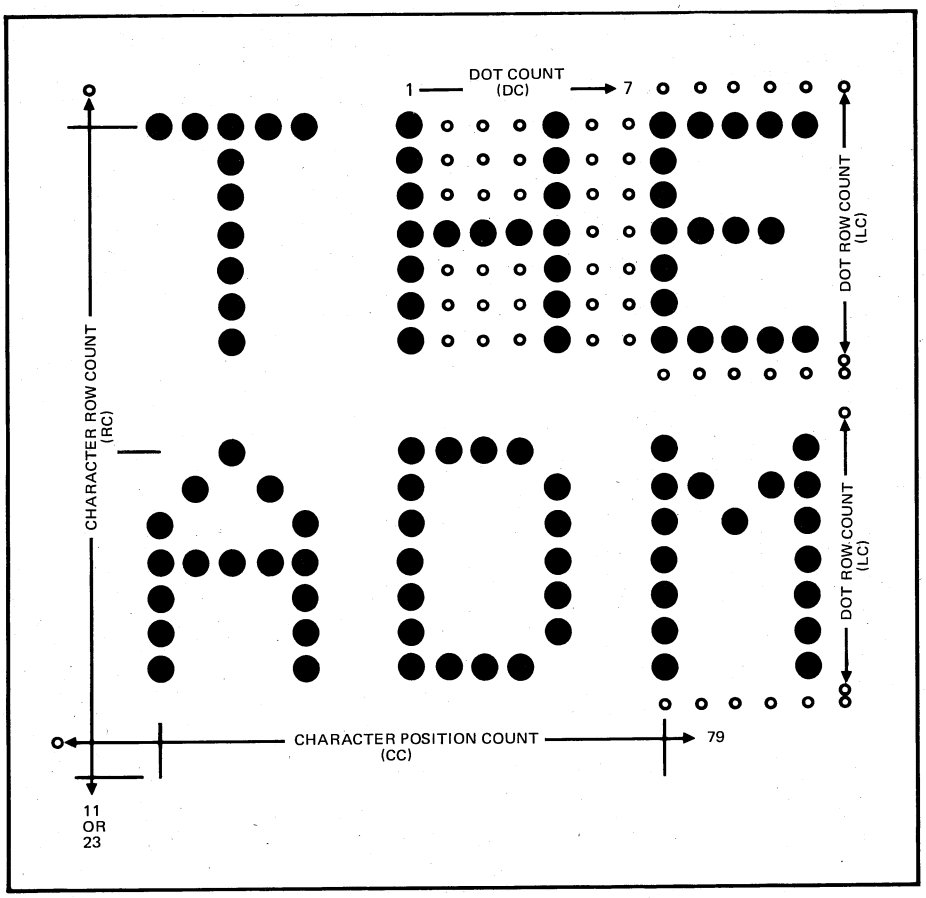


Figure 4-2. CRT Display Monitor

4.2.8 Interface Control Logic

This logic controls Clear-to-Send and Request-to-Send exchanges between modem or computer and the ADM-3A. Either a code-turnaround or a reverse-channel system may be used to transfer control from one end of the communication line to the other.

Switches adapt the logic to interface with the common type 103 or 202 modems, or to operate under internal control.

4.2.9 CRT Display Monitor

The CRT display monitor employed in the ADM-3A is a solid-state unit for use in industrial and commercial installations where reliability and high-quality video reproduction are desired.

The monitor features printed circuit board construction for reliability and uniformity. All circuits of the TV monitor are transistorized.

4.3 LOGIC DESCRIPTION

The following paragraphs describe the operation of logic represented by each block in the overall block diagram, figure 4-1, as well as logic and circuits performing functions not indicated in Figure 4-1. Refer to block and timing diagrams that accompany the text, as well as to the logic diagram included in Section 6 in this manual.

4.3.1 General Clear Circuit

Circuits shown on sheet 7 of the logic diagram cause all control logic in the ADM-3A to be initialized when applied power causes the +5V dc supply to rise.

As the supply voltage reaches trigger level of a retriggerable one-shot, the one-shot creates the reset signal CLEAR, which is distributed to ADM-3A logic through six inverters. In circuit board testing, the signal TESTER INITIALIZE simulates the action of the one-shot.

4.3.2 Display Counters

The display counters provide a count of dot positions and dot rows, character position in a character line, and character rows. These counts define the position of each dot in a character matrix, and the position of each character in the total display. Figure 4-3 is a block diagram of this logic, and timing is shown in figure 4-4.

The basic clock is a 10.8864-MHz signal generated by a simple oscillator circuit. The clock frequency is twice the video frequency. The clock (CLK) drives the dot counter.

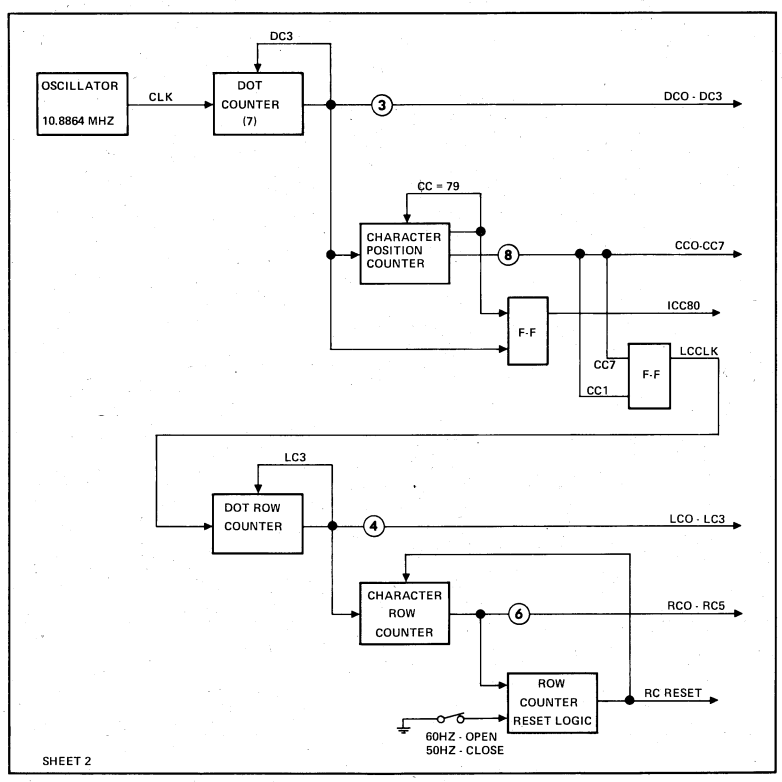


Figure 4-3. Display Counters, Block Diagram

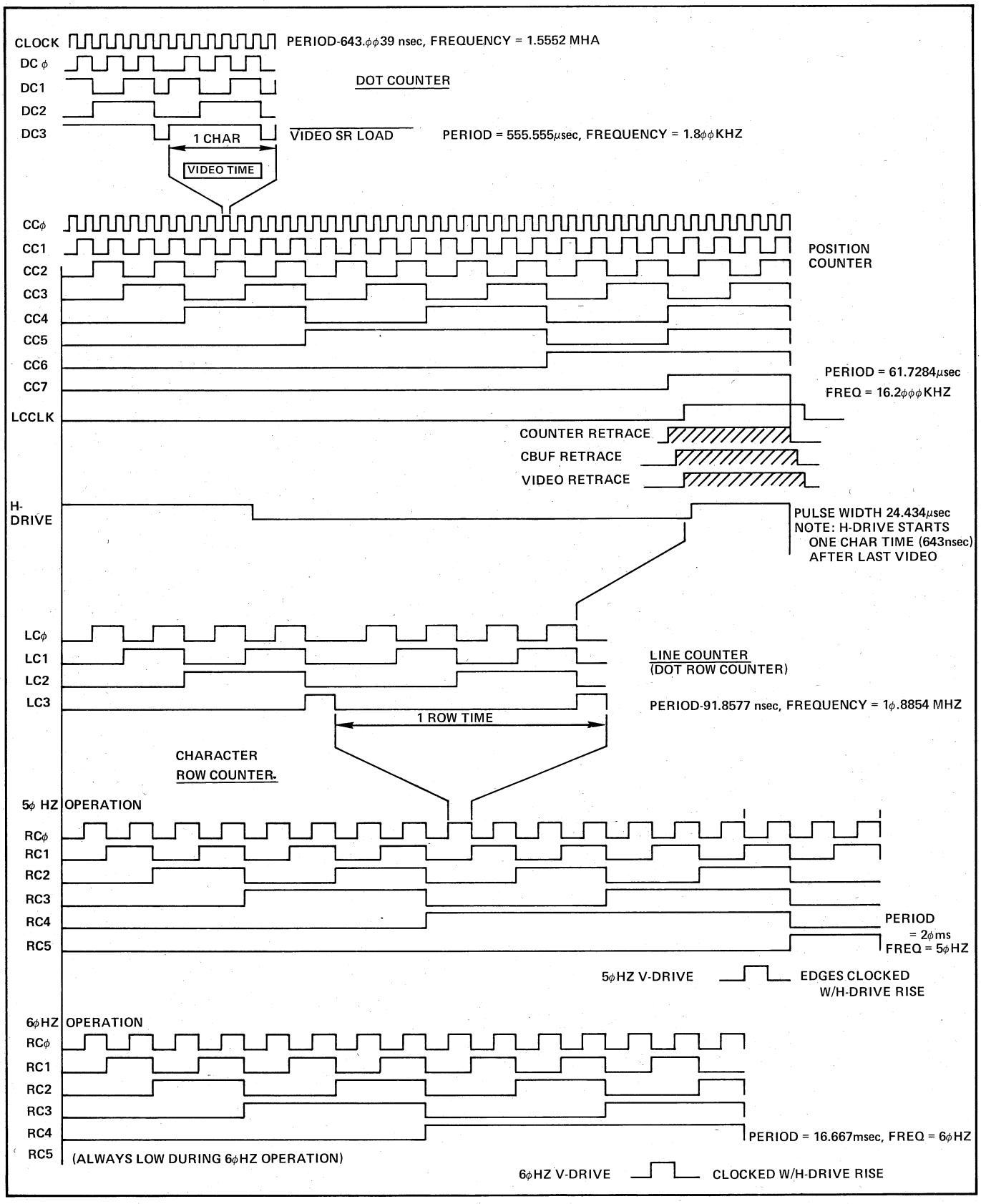


Figure 4-4. Display Counter Timing

The dot counter counts the seven dot columns comprising each character. The character is preset to 10 at the count of zero, counts through the overflow at 15, and is again preset at zero. Its final count, DC3, clocks successive addresses to the character ROMs, and triggers the character position counter.

The eight-stage character position counter controls the position of each character on the 80-character raster line, and controls horizontal retrace time. The counter provides a total count of 96 (80 counts for character position, and 16 count for the retrace). The character position counter counts from zero to 79, presets to 240, counts through the overflow at 255, and then wraps to zero. Outputs CC0 through CC6 are binary counts, but CC7 has a value of 80. That is, CC7 is low while 80 character positions are counted, and high during retrace time.

A flip-flop produces the signal ECC80 for the first count of retrace time. ICC80 indicates the time at which a command at the I/O interface may be acted upon. The output of the LCCLK flip-flop clocks the character line counter.

The character line counter counts the lines that form each row of characters. The counter counts module nine. Counts 0 and 8 form spaces between characters, and dot rows are formed by counts 1 through 7. The last count, LC3, clocks the character row counter at a frequency of 1.8 KHz.

The character row counter counts the 24 character rows appearing vertically on the display, and counts through vertical retrace time (six counts for a 60-Hz power line, and 12 counts for a 50-Hz line). A switch (60 EN) sets up logic to produce RCRESET at the proper time, resetting the counter to zero to begin the next character row count.

4.3.3 Row Counter & Offset Counter Logic

The Row Counter (Figure 4-5 and Logic sheet 3) defines the actual row in which the cursor resides, and consequently, the row in which new data entered into memory will appear on the screen. This counter will be cleared to zero on 24-line, and on 12-line mode by a power-up clear, key-clear operation, or a clear screen command, irrespective of the position of the Cursor Control switch.

The Offset Counter relates absolute memory addresses, during data entry and refresh, to the virtual (apparent visual) row addresses which are generated by scrolling operations. The OC, like the

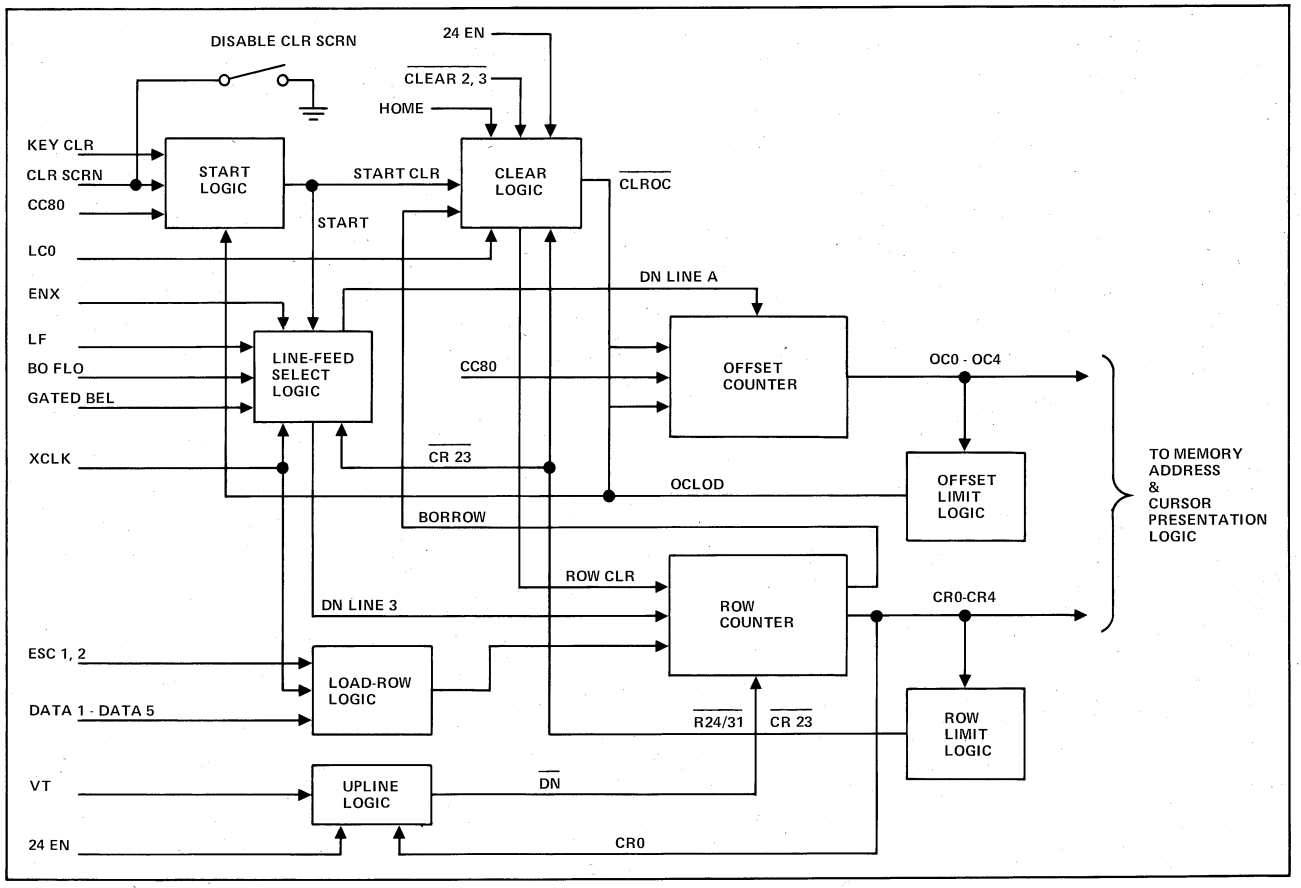


Figure 4-5. Row Counter & Offset Counter Logic, Block Diagram

RC, is initially cleared by any one of the clear-screen operations noted above, however, a sequence is then initiated by the START logic, which causes space-codes to be written into each character cell of the current row during first 80 character-periods of one line-scan period. At the end of the line-scan, CC80 will generate a line-feed signal, DNLINEA, which will increment the OC. The process is then repeated, with the OC pointing to the next row of memory addresses, which are also filled with space-codes.

After 24 such operations (12, if the 12/24 select switch is closed), the OCLOD signal is generated, which terminates the START operation, and freezes the OC at a count of zero (1, if in 12-line mode). At this point, both the Row and Offset counters will contain "minimum count" (zero in 24-line, and 1 in 12-line mode), and the true and virtual row-addresses will be the same. (MS-A).

After completion of a clear operation, the Offset Counter will be disabled until the Row Counter has been advanced or set to 23 (bottom row). If the Cursor Control switch is open ($\overline{ENX}$ true), line-feed signals (DNLINEB) will be sent to the Row Counter each CC80 time, until a count of 23 has been reached. At this point, the Row Counter will be disabled until either the Cursor Control switch is closed or another Clear is performed, and the Offset Counter will be enabled.

If the Cursor Control switch is closed, the Row Counter will remain at minimum count after a clear operation, and will respond to any downline, upline, Home and absolute (load cursor) row directives. In the same manner as when Cursor Control is off, downline directives which occur when the Row Counter is at 23 will be routed to the Offset Counter, causing it to increment, and scroll the entire display by adding a difference of one unit between the true and virtual row addresses.

Whereas the Offset Counter can only be incremented (DNLINEA), the Row Counter can be incremented, decremented, cleared or loaded with an absolute value ($\overline{DNLINEB}$, VT, ROWCLR, $\overline{LDROW}$). In the event a value in excess of 23 is loaded, the counter will be cleared to minimum count. If the Row Counter is decremented when it currently holds the minimum count, BORROW will occur, and the counter will be forced back to minimum count (ROWCLR). ROWCLR is also generated if a HOME (RS), directive is received.

Both counters, when in 12-line mode, have the least significant bit forced true, and all increment or decrement directives will affect only the higher order bits. In this mode, therefore, only odd virtual addresses will be accessible. Note, that scrolling the display will still produce only odd addresses, since the Offset Counter will count in units of two, which when "added" to the odd Row Count will still result in an odd virtual address.

Figure 4-6 Shows the timing for the Clear Screen Operation. The timing for Key Clear or power-on clear operations is identical to that shown, except that in the latter two situations, START is forced high without benefit of DOIT.

4.3.4 Column Counter Logic

The Column Counter (figure 4-8 and logic sheet 4) and its associated logic define the character-position of the cursor, irrespective of the current cursor mode. The counter is bidirectional, to accommodate both backspace and forespace operations, and is capable of being loaded, via an associated multiplexor, with either of two fixed values, or a variable position-code which is obtained as the last character of the four-part Load Cursor sequence.

Back-spacing (count-down) is affected only by a local or remote backspace command (BKSP), while forward-spacing may be accomplished by either a character-entry, a forespace command or a 'Read' operation. All received characters will cause a forespace after the character is written into memory, except control characters and the three non-control characters which follow ESC during a Load Cursor sequence. For both character-entry and forespace commands (FF), the counter is advanced during CC80 time. During Read operations (test only), a forespace is generated each time $\overline{XLOAD}$ occurs, indicating, the initiation of character transmission.

The Column Counter is cleared in any one of four situations:

a. A Carriage Return (CR) command is received, either from the keyboard or a remote source.

b. A Home (RS) command is received.

c. An underflow occurs, due to attempts to back-space from column 0.

d. A start-sequence is initiated by one of the power-up/clear operations.

When the Column Counter is incremented past the 80th column-count (code=79), an overflow signal is generated, causing an absolute count value to be loaded into the counter at the next LCCLK transition (CC81-time). If the auto-new-line switch is open, a 79_{10} code will be loaded, forcing the cursor back to the last column position. If auto-newline is closed, a zero-code will be loaded (carriage return) and a line-feed enable signal (BOFLO) will be

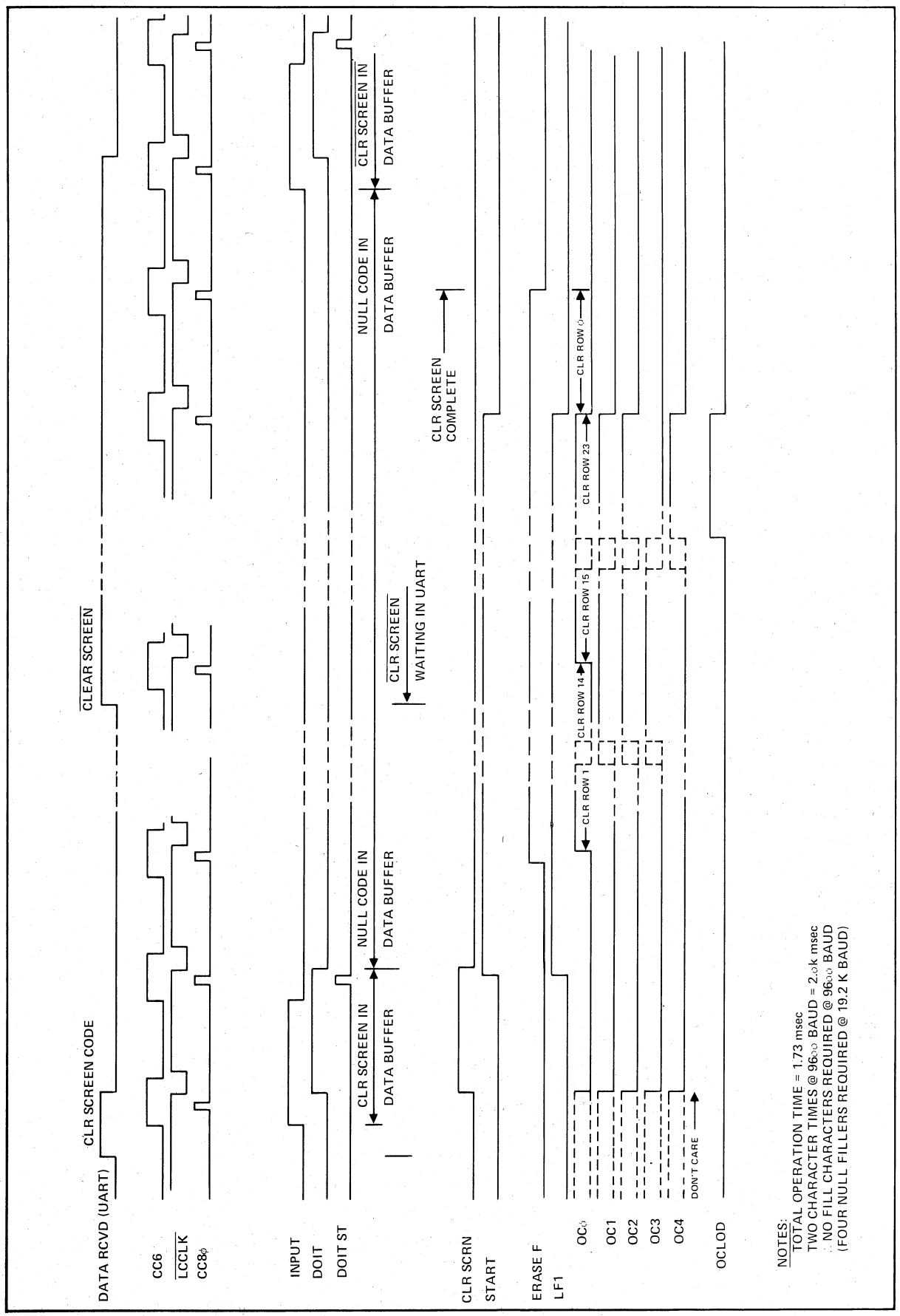


Figure 4-6. Clear Screen Timing

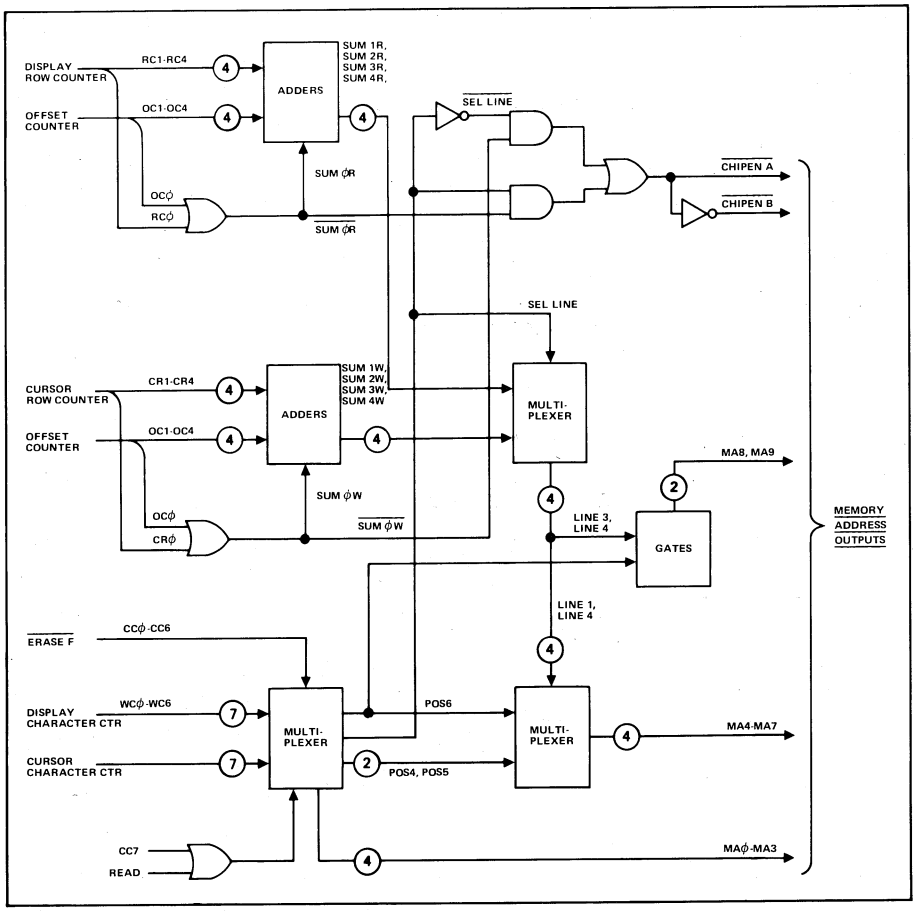


Figure 4-7. Memory Address Logic, Block Diagram

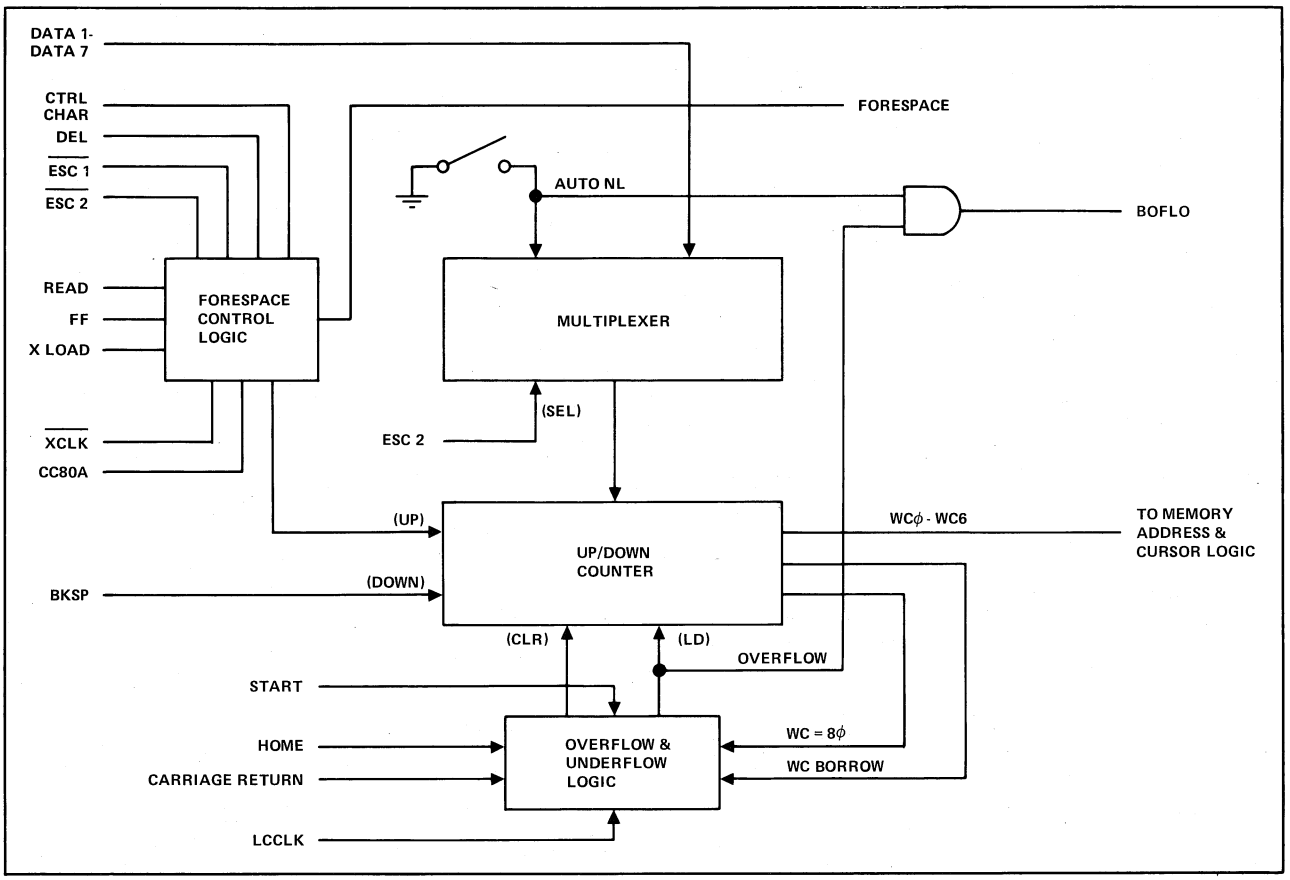
generated, to enable either the Row or Offset counter to be incremented.

When the code in the Column Counter reaches 71_{10}, the signal LINE END is generated. This signal, like a received BEL-code, will cause the Beeper to sound a tone, announcing the approach of the end-of-line. If the Cursor Control switch is on ($\overline{ENX}$-true) and a Load Cursor sequence is performed, the Column Counter multiplexor will select the DATA lines from the Received Data Buffer, and the Column-code on these lines will be loaded into the counter at CC80 time. The two most significant bits of the code (DATA6 and DATA7) are modified in order that ASCII codes space (040_8) through L/C "O" (137_8) are interpreted as column codes 000_8 through 117_8. In the event a translated code greater than 117_8 (79_{10}) is loaded, the OVERFLOW logic will force the counter either back to 117_8 (Auto-Newline off) or 000_8 (Auto-Newline on).

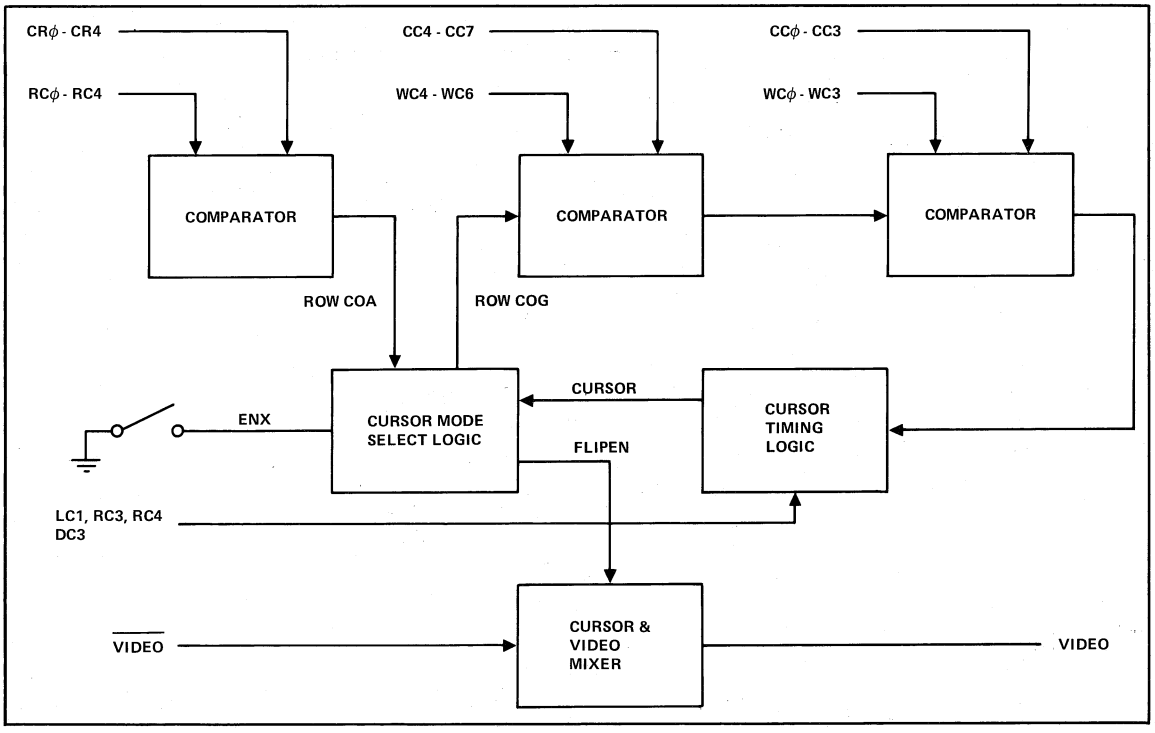
4.3.5 Cursor Presentation Logic

The cursor logic (see figure 4-8 and logic sheets 7 & 8) performs the function of detecting the current character-cell in which the cursor resides, and mixing the coincidence signal with the character video to obtain a representation determined by the Cursor-mode switch. The logic consists of a set of three comparators, a pair of unit-delay flip-flops and video mixing circuits. One comparator relates the current cursor row, as defined by the cursor Row Counter, to the Display Row Count. When coincidence occurs, an equality signal (ROWCOA) is generated.

If the Cursor Control switch is off, row-equality is forced true, since the cursor will always reside on the bottom line. If the switch is on, ROWCOA is gated to the two column comparators. The two column comparators relate the 7-bit WC counter code to the Display Column Count. When coincidence occurs, and ROWCOG is true indicating row-coincidence, an equality signal will be sent to the delay flip-flops. If the Cursor Control switch is off, the delay flip-flops will be enabled only during the period when the counters are scanning the two likes immediately below the 24th row of data, whereas in the on position the flip-flops will always be enabled. In the enabled condition, the flip-flops will delay the detected coincidence signal two character periods, to synchronize the cursor with the displayed characters on the screen.



Column Counter



Cursor Presentation

Figure 4-8. Logic Block Diagrams

With Cursor Control off, no additional mixing is required, since the double-underscore representation occurs during the period when no characters are being displayed. With Cursor Control on, the cursor coincidence signal (CURSOR) is gated with character-video data in an exclusive-OR element, causing the cursor to appear as a reverse image of the character in which position it resides.

4.3.6 Memory Address Logic

The logic group shown in figure 4-7 and Logic Sheet 5 performs all the functions related to reconciling the current entry-row (Cursor Row Counter) and virtual row (Offset Counter) positions to a physical row-address in memory, and additionally, converting the visual 80-character by 24-row visual format to a 64 by 30 byte memory array. The first task is accomplished by two five-bit and two two-bit full adders, while the second is performed by a set of multiplexors.

The first five-bit adder produces a sum equal to:
Display Row Count + Offset Count + 1

This function provides the required relationship between current display rows and the virtual row-address during refresh scanning, in order that the data might be displayed on the proper row of the screen, consistent with the scroll-history since the last clear-screen operation. If no scrolling has occurred, the offset count will be zero, and data for the top row of the display will be obtained at memory-row 1 (0 + 0 + 1= 1). Likewise, data for display-row 22 will come from memory-row 23, and data for the bottom row will come from memory-row zero. One of the two-bit adders, plus associated gates, performs the function of reconciling sums greater than 23 to a 24-row universe, by adding an appropriate adjustment factor to all such sums (23 + 0 + 1 = 24→0).

If the display has been scrolled one time, data for the top row will be obtained from memory-row 2 (0 + 1 + 1 = 2) and data for the bottom row from memory-row 1, thus, it can be demonstrated that all the data in memory will appear to have moved upward on the display by one row, after the scrolling operation, even though its actual physical location in memory is unchanged. The only physical alteration, in this example, occurs in memory-row 1, which is erased (see section 4.3.8) during the scroll operation, leaving the new bottom row address locations clear for new data-entry.

Each subsequent scroll operation will, therefore, cause a successively higher memory-row address to assume the top display-row position, with the row previously associated with that position erased and "rolled" to the bottom position of the display.

The second five-bit adder produces a sum equal to:
Cursor Row Count + Offset Count + 1

This function reconciles the current cursor row-position, which is the row on which new data-entries must appear on the display, to the scroll-history, which determines the last memory-row that was erased and rolled to the bottom of the display. If no scrolling has occurred and the cursor is on the top row, the resultant sum will be memory-row 1, which is the desired row for data-entry, since that is the row from which data will be obtained for the top row of refresh. If the cursor were moved to the bottom row, the sum would be zero (23 + 0 + 1 = 24 → 0), due to the action of a second adder and gate set which reconciles all CR + OC + 1 sums greater than 23 to values between 0 and 23. This also is consistent with the refresh adder-set, since any data entered under these circumstances will be routed to memory-row zero.

As scrolling occurs, the second adder group maintains the proper relationship between the cursor position and the virtual display-rows, such that data-entry will always occur in the memory-row which is displayed during the same row-scan time as the cursor. Consider as another example, a display which has been scrolled six rows, after which the cursor is positioned to row 20. The memory-row actually displayed on row 20 will be:

$$20 + 6 + 1 = 27 \longrightarrow 3$$

If an entry is made at the current cursor position, the same summation will occur using the Cursor Row and Offset Counter values, and the entry will be made in row 3.

The multiplexor section of the Memory Address Logic manipulates the CR + OC and RC + OC sums derived above, plus the information from the Display Column Counter (CC0 - CC7) and Cursor Column Counter (WC0 - WC6) in order to resolve the 80 x 24 display matrix to a 64 x 30 memory matrix. The first-stage multiplexors distinguish between Refresh accesses to memory and write accesses, since the former are governed by the RC + OC sum and the CC Counter information, while the latter are governed by the CR + OC sum and the WC counter.

The time-period when CC7 is false is the active display-time for each scan-line, and therefore,

defines Refresh-access time. During horizontal retrace, when CC7 is true, the memory is available for data-entry. During test read-back, the first-stage multiplexor is locked into the "Write" mode in order to expedite the transfer of information, since display functions are not necessary during this operation.

The most significant position of the CC/WC multiplexor is used as a selection signal for the SUMR/SUMW multiplexor, and in the write-phase will always cause selection of SUMW (CR + OC) for the LINE1 - LINE4 and Chip-Enable functions. In Refresh mode the SUMR (RC + OC) outputs will normally be selected, however, during Clear Screen or Line Erase (when scrolling) operations the term $\overline{\text{ERASEF}}$ will force selection of the SUMW terms, in order that all erasures can take place during $\overline{\text{CC7}}$ time and thereby minimize the total time required for such operations (See Section 4.3.8).

The selected low-order column terms (MA0 - MA3) require no additional modification, since the smallest increment of memory allocated to a given line is 16 characters. The three high-order column terms (POS4 - POS6) and the four high-order row terms (LINE1 - LINE4), however must be modified to account for the maximum column-width of the memory matrix of 64 characters. Accordingly, the final multiplexor stage uses the column-term POS6 to distinguish between column-positions greater (or equal to) and less than 64. For positions less than 64, the high-order address functions MA4 - MA9 are derived from POS4, POS5 & LINE1 - LINE4 respectively. This translation provides a direct relationship between a 24 x 64 section of memory, and that portion of the display defined by 18WS 0-23 and columns 0-63. For column positions 64-79, POS6 switches the multiplexor to derive MA4 - MA7 from LINE1 - LINE4, respectively, and forces MA8 and MA9 true. This translation relates a 6 x 64 section of memory to the last 16 column positions of the 24 display rows, by allocating one-quarter of each memory-row, progressively, to the remainder of each display row. The chip-enable functions define even and odd display rows and memory-groups, and therefore, require no translation. The organization of display data in memory, is shown on figure 4-9.

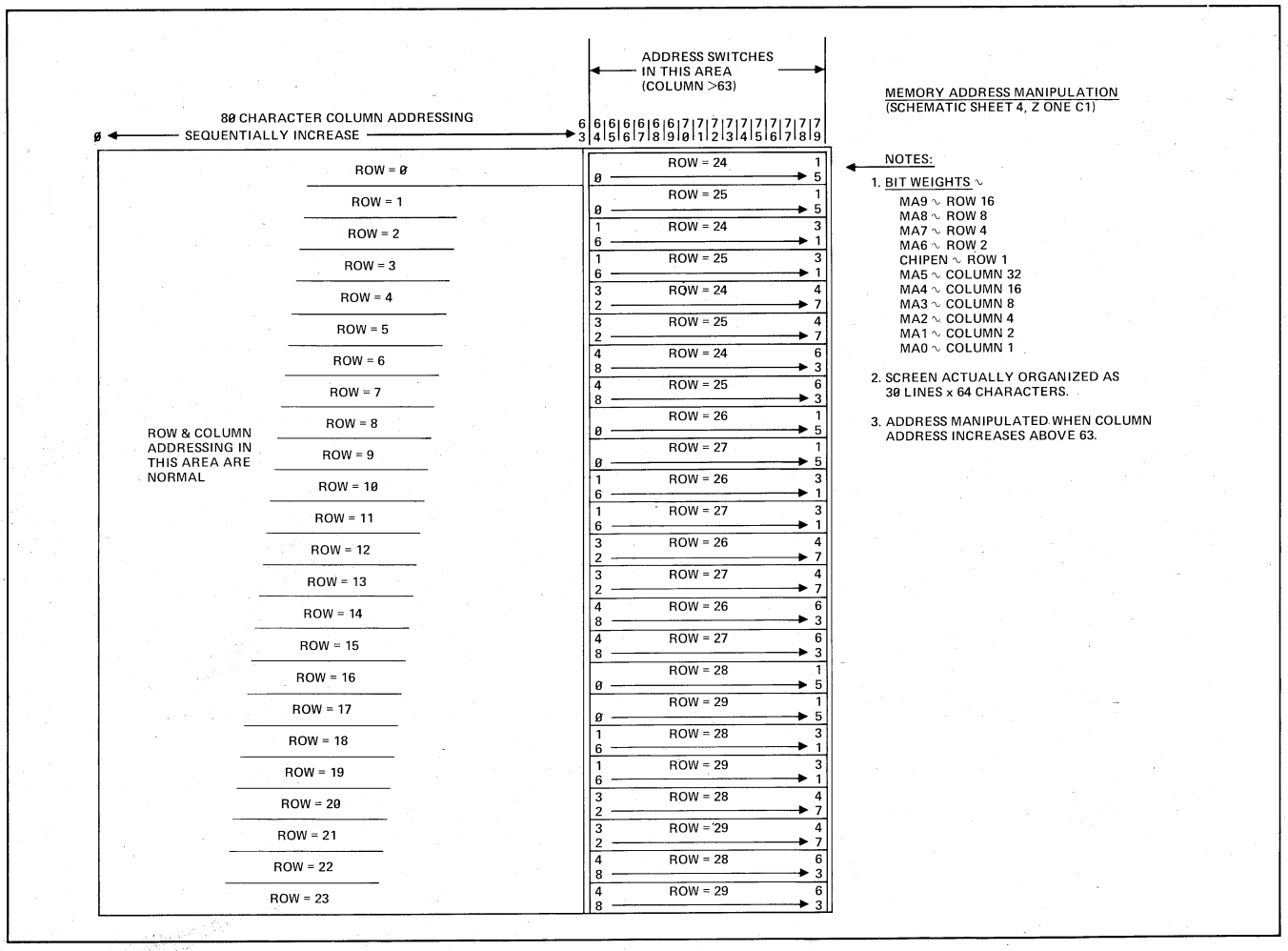


Figure 4-9. Organization of Display Data in Refresh Memory

4.3.7 Refresh Memory and Character ROM Logic

Figure 4-10 shows logic comprising the refresh memory, buffer latches, and character memory ROMs.

The refresh memory is made up of 2K, 7-bit semiconductor RAM devices in one of four configurations as follows:

a. Six RAMs for upper-case only, 12-line display.

b. Seven RAMs for upper/lower-case, 12-line display.

c. Twelve RAMs for upper-case only, 24-line display.

d. Fourteen RAMs for upper/lower-case, 24-line display.

A switch (UCEN) sets up the logic to operate with, or without, the lower-case RAMs. UCEN alters data to adapt the logic for either 6-bit codes (upper-case only) or 7-bit codes (upper/lower case). Term ERASEF causes the logic to force bit 6 high, creating a SPACE code in place of the received NULL code.

Data from the input buffer (DATA1-DATA7) is loaded into, or read from, the refresh memory by address lines MA0-MA9. The memory is clocked, for each character time, by WRITE PULSE.

CHIPENA is low as data is loaded into, or read from, RAMs storing the 12 odd lines of display data. CHIPENB enables the RAMs storing the 12 even lines in a 24-line display.

At the end of each character period, DC3 clocks an addressed character into buffer latches which store the character to be encoded by the ROMs. The buffer latches are cleared by VIDEO BLANK. Because CBUF6 is normally inverted, however, a SPACE code, rather than NULL, is presented to the ROMs.

Two ROMs decode CBUFn characters and produce a 5-bit output code that provides the dot pattern for each line in the character matrix. Each of the seven lines in the character matrix is identified by the line count LC0-LC2. The parallel-bit information output by the ROMs is serialized for presentation to the video monitor.

One ROM contains upper-case characters, and the other contains lower-case characters. Select logic senses states of CBUF6 and CBUF7 to enable either ROM device.

CBUFn is available at data transmitter logic for transmission in read-back test operation.

4.3.8 Erase Logic

A display line is erased by the Logic shown on Schematic pages 3 and 4.

The ERASEF signal is turned on by SETERA. SETERA describes the condition in which both PGMOD & LFI are true, causing the offset counter to begin counting and the lines to scroll each time a line-feed is caused by the column counter overflowing (BOFLO).

ERASEF is turned off by CC80A after a single character row has been cleared, during scrolling.

However, when START is raised by a CLR SCRN Code, ERASEF remains high until START is turned off by an overflow of the offset counter. Consequently the entire screen is erased.

4.3.9 WRITE PULSE Logic

The WRITE PULSE signal clocks the refresh (RAM) memory. Logic that generates WRITE PULSE is shown in sheet 4 of the logic diagram.

WRITE PULSE consists of gated pulses clocked by dot count DC2, and is normally gated on by FORESPACE (the input of the cursor counter) or ERASE LINE.

The non-destructive space code feature allows writing a SPACE code (040_8) into the RAM memory any time between a Line Feed (LF) code and a Carriage Return (CR) code, with writing of SPACE inhibited between the CR code and the next LF code. This permits the computer or operator to write a display on the screen, issue a CR code, and space over the previously written data, with the cursor, without writing over the data.

The NO write signal inhibits FORESPACE so that WRITE PULSE is not generated during that period. A switch permits inhibiting the non-destructive space code feature.

4.3.10 Keyboard Logic

Keyboard logic is shown on sheet 9 of the logic diagram (except for lock/unlock logic shown on sheet 10). Timing of keyboard logic functions is shown in figure 4-11.

The keyboard is encoded by generating the complete sequence of 7-bit USASCII codes at high speed, and trapping the code that matches a depressed key. The codes are generated continually and repetitively unless a key is pressed. The code sequence is clocked at a counter by KBCLK, which is the gated character rate signal CC0.

The four least-significant bits of the count (KC1-KC4) encode the 16 rows of the USASCII code

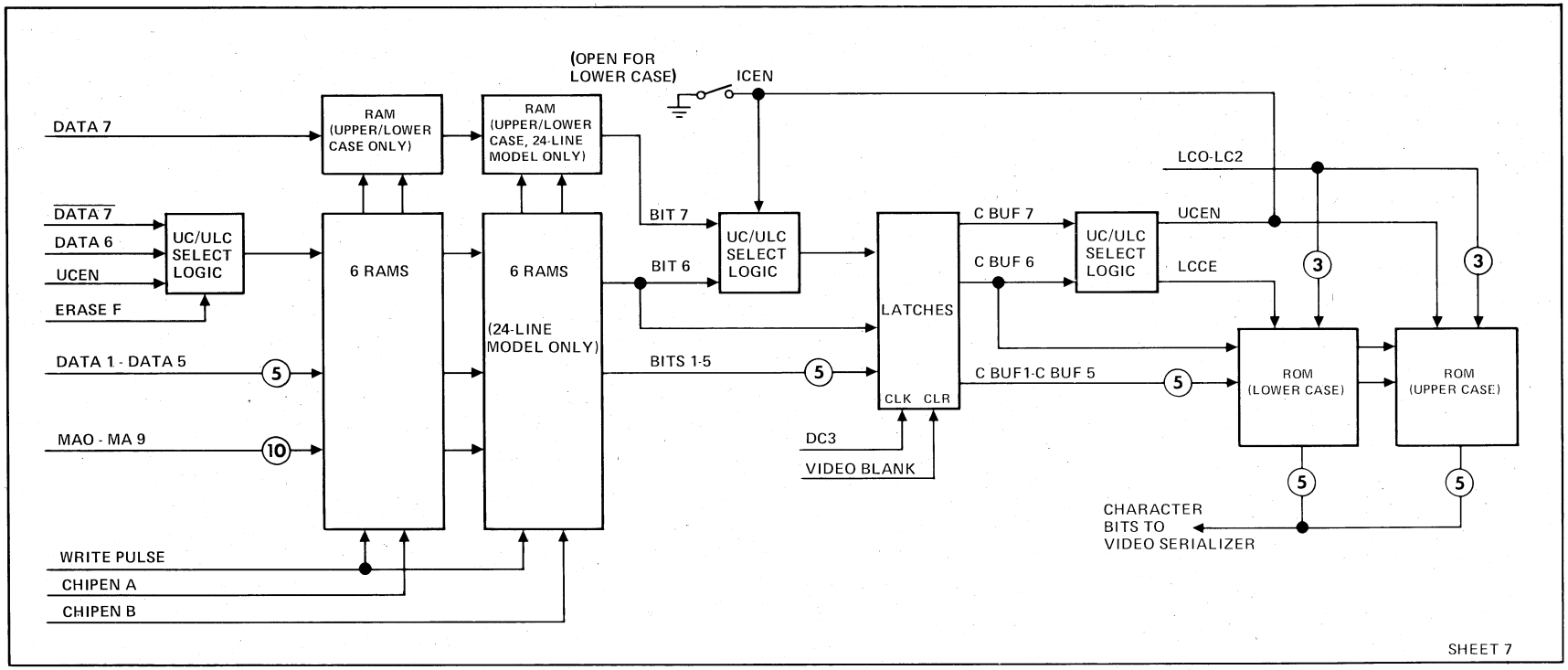


Figure 4-10. Refresh Memory and Character ROM Logic, Block Diagram

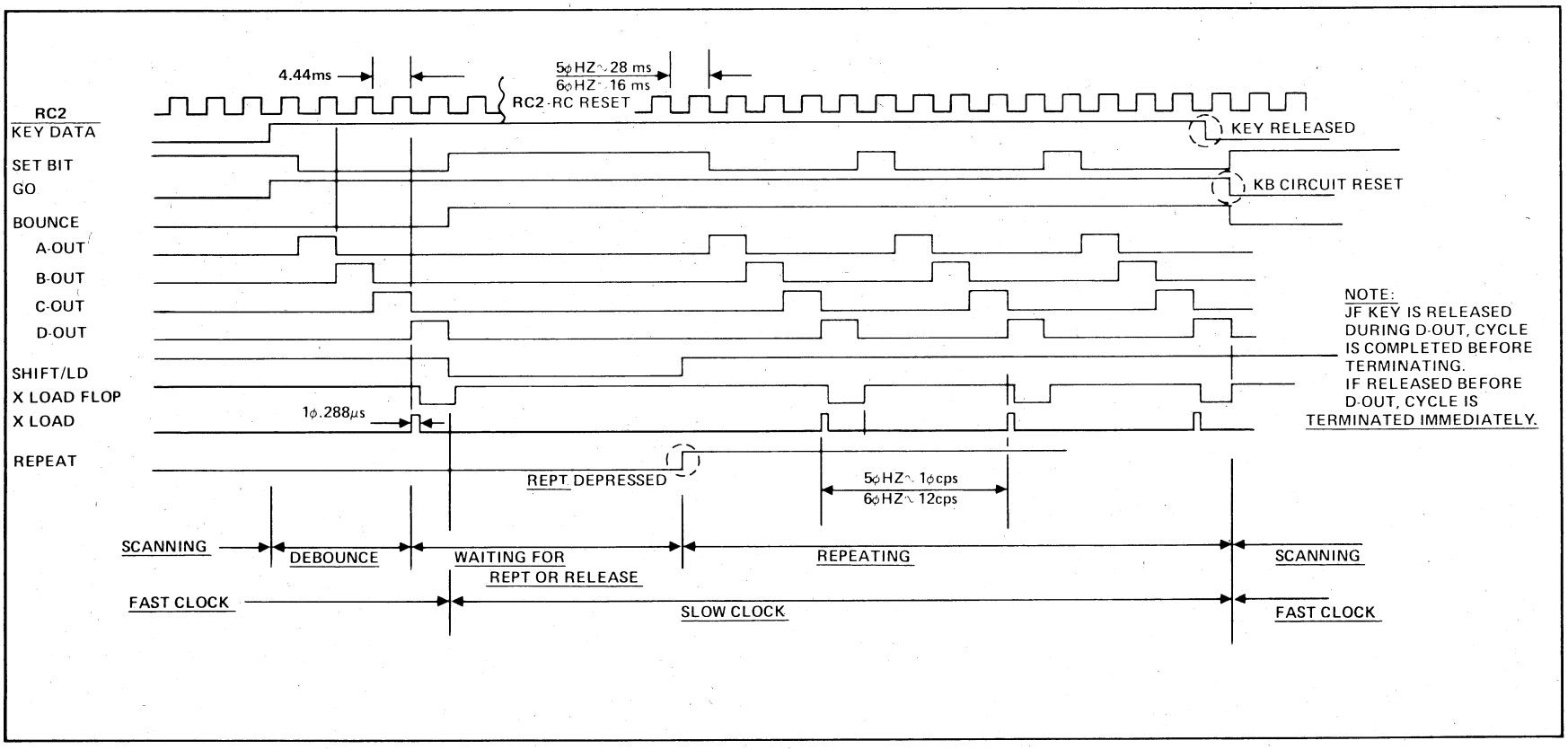


Figure 4-11. Keyboard Logic Timing

chart. The three remaining bits (KC5-KC7) encode the eight columns of the chart.

When no key is depressed, KEY DATA is high and KBCLK cycles the counter, and bounce logic holds BOUNCE high. When a key is depressed and then the corresponding code appears on lines KC1-KC7, KEY DATA falls, preventing generation of further KBCLK pulses so that the code is held on KCn lines. KEY DATA also causes GO to rise, causing bounce logic to count 900H, RC0 pulses until a fifth pulse has completed a 5.56-msec delay period.

At the end of the key-bounce delay period, BOUNCE becomes true, inhibiting further counts of RC0. If the key is released, KEY DATA immediately rises and counter cycling resumes. If the key is held down, along with the REPT (Repeat) key, however, the high BOUNCE signal permits RCRESET pulses (at the ac power line frequency) to clock the bounce delay period, generating the GO signal at a rate of 12.5 characters per second at 60-Hz, or 10 characters per second at a 50-Hz line rate. Consequently, the character is repeated at that rate until either key is released.

The term THRE limits the repeat rate if the period of the selected baud rate creates a character time longer than the repeat cycle.

When the CTRL (control) key is pressed, bits KC6A and KC7A are forced to zero, forcing any generated code into column 0 or 1 of the USASCII code chart. Bit KC5A selects either column 0 (when false) or column 1 (when true). For example, when the "2" key is pressed (0110010) along with CTRL, the effective code becomes control code DC2 (0010010).

With either SHIFT key depressed, bit 6 (KC6A) is inverted to select upper-case alpha characters (USASCII column 4 or 5, instead of column 6 or 7). Also, INVERT 5 selects codes in USASCII column 2 instead of column 3, to encode the "upper-case" symbols on numeral and symbol keys. Terms COL2 and COL3 identify those codes in the shift logic. Row 0 codes in columns 2 and 3 (SP and 0) are excluded from this action because they have no "upper case" functions.

The UPPER CASE key is used in units that do not include the lower-case alpha characters. When the key is depressed, use of the SHIFT key has no effect on alpha keys. Lower-case alpha codes are encoded in USASCII columns 6 and 7. Therefore, the gated term KC6 KC7 causes INVERT6 to maintain upper-case codes without use of the SHIFT key. Other codes in columns 4 through 7 are identified by KC7 SHIFT EN which permits normal shifting up and down.

The BREAK key is depressed to signal the computer that the operator wishes to terminate data transfer. The Break function is maintained for as long as the key is held down. The signal BREAK appears at interface control logic where it forces the primary data transmit line to the "space" state if the unit is transmitting, or forces the secondary transmit line to the "mark" state if data is being received and the interface is in the secondary-channel mode of operation.

When the CLEAR key is pressed, and the SHIFT key is also depressed (SHIFT EN), KEY CLR clears keyboard lock logic, the refresh memory, and interface control logic.

The HERE IS key activates an optional Answer Back function which causes a unique, fixed message to be sent to the computer. The message, up to 32 characters long, is contained in a PROM device. Either the level from the HERE IS key, or an ENQ command received from the computer, causes the IDENT signal to activate logic on the Answer Back board.

Keyboard lock logic (sheet 5) permits the computer to enable or disable the keyboard logic. The KBLOCK signal is set-enabled locally by KEY CLR, or by the decoded UNLOCK command, and reset-enabled by the decoded LOCK command. Keyboard lock logic by CC80. KBLOCK prevents DOIT from generating GO, inhibiting any keyboard action. A switch permits holding KBLOCK true regardless of received LOCK commands.

4.3.11 Beeper Logic

Beeper logic (sheets 3 & 4 of the logic diagram) produces an audible signal as a near-end warning. The signal that drives the speaker is the character row rate LC2, which has a rate of 3.6 KHz.

The rate LC2 is enabled to the speaker during the "on" period of a one-shot circuit. The one-shot is triggered on by WRITE CHAR as the 71st character is written in any line (WC0 WC1 WC2 WC3 WC6). The one-shot is triggered when a BEL code is received at the I/O interface.

Because a read-back operation is initiated by BEL code, the term READ is used to disable the one-shot so that the BEL code cannot cause the audible signal.

The OVERFLOW signal is used to turn-off the one-shot when a baud rate higher than 2400 baud is used. Because the period of the one-shot is greater than the period between successive 71st characters in this case, the beeper would otherwise remain energized continuously while data is being received.

4.3.12 Data Receiver and Command Decoder Logic

This logic (figure 4-12, schematic 6 & 10) receives data from the computer through either a standard RS232 interface, or a current loop interface. Serial data is received through the RS 232 interface by an RS232 receiver which sends the data to an OR circuit which also receives data from the current loop receiver.

The current loop receiver is a bipolar circuit and responds to current in either direction. The receiver comprises a rectifier/limiter which drives an optical coupler, and a single-transistor amplifier driven by the optical coupler. If the RS232/CL switch is open, the amplifier output appears at the OR logic that furnishes the UART input.

A third input to the OR logic is data being transmitted from the ADM-3A (XDATA) and appears if the HDX (half duplex) switch is closed.

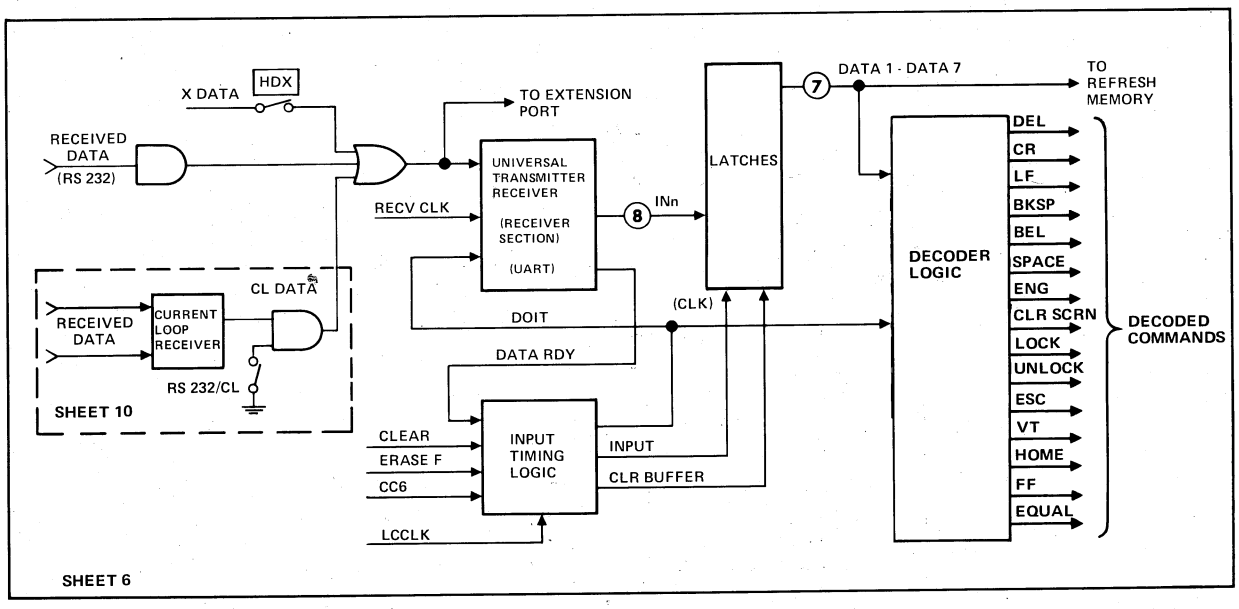


Figure 4-12. Data Receiver Logic and Command Decoders

The received serial data, from whatever source, is clocked into the UART by RECV CLK (at the selected baud rate). In the UART, each received character is stored and presented in parallel-bit form to latches, with the most-significant bit appearing on the IN7 line. (IN8 is not used in the ADM-3A.)

The character stored in the UART is clocked into latches by INPUT as DATA RDY is output by the UART (unless ERASEF inhibits INPUT). INPUT rises when CC6 occurs at the end of every horizontal scan. Then LCCLK turns on DOIT, which remains on for the next full horizontal scan period during which the last received command is executed.

The data character stored in the latches is decoded to obtain the different control command signals. The three least-significant bits are used as chip-enable codes and are made effective by DOIT. Consequently, control commands are not effective until execution time.

4.3.13 Data Transmitter Logic

Data transmitter logic is shown in figure 4-13 (schematic sheets 8, 10 & 12). Data that may be applied to the transmitter section of the UART are:

a. Keyboard characters KCn, and the XLOAD signal from keyboard logic, when READ is false (normal operation).

b. Characters of the answer-back message, applied through KCn lines, when the answer-back option is included in the ADM-3A, and READ is false.

c. The contents of the refresh memory buffer (CBUFn) when READ is true (in read-back test operation).

The UART XMIT CLK that clocks the UART is the gated XMIT CLK selected at baud rate select logic and is 16 times the baud rate. The UART is loaded from XDATAn lines by LOA ART, which is normally high.

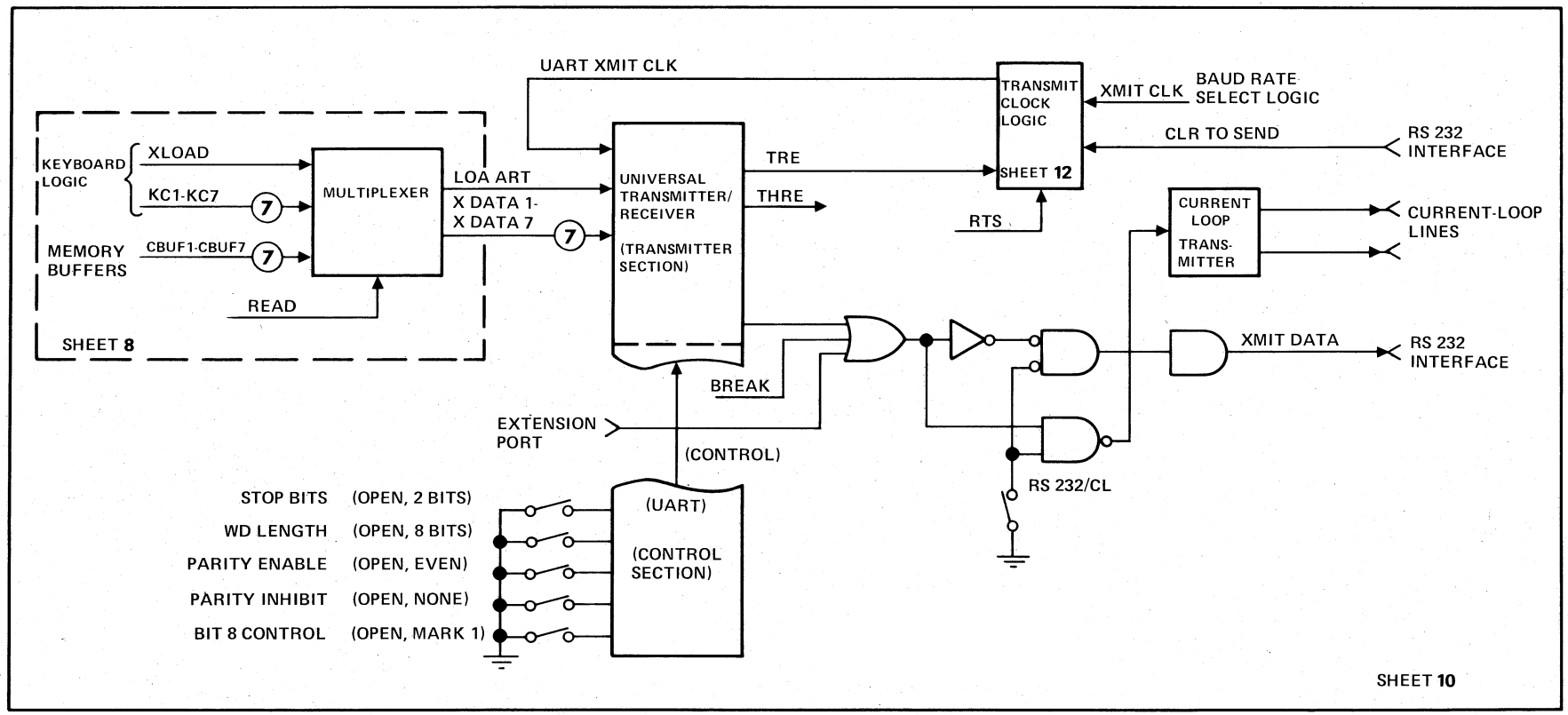


Figure 4-13. Data Transmitter Logic, Block Diagram

The UART XMIT CLK is enabled when CLR TO SEND appears at the interface, and further controlled by TRE. TRE and THRE are output by the UART. THRE falls when XDATA loads the holding register in the UART. If the serializer (which is loaded from the holding register) is empty, TRE is high. With the holding register full and the serializer empty, the UART automatically transfers the character into the serializer. At this time THRE rises, ready to accept the next character, and TRE falls to indicate that the serializer is busy. Both THRE and TRE are high when the UART holds no data.

Transmit clock logic is reset by the next Request to Send (RTS) signal from the interface.

Five switches permit formatting the transmitted character. First transmitted is always the Start bit, followed by the seven data bits (LBS first). The parity bit, odd or even, then follows (if enabled); followed by one or two Stop bits.

The serial bit stream is ORed to transmitter circuits through a gate which also receives data which may appear (from another device) at an extension port.

If the BREAK key is depressed, the XMIT DATA line is forced to the high (SPACE) level.

Data is sent through either the RS232 or current loop interface, depending on the position of the RS232/CL switch. The unselected interface maintains a marking level. The RS232 interface comprises a simple driver. The current loop interface uses an optical coupler to couple the TTL data to an amplifier, and then through a diode output network to the current loop.

The optical coupler completely isolates the current loop transmitter from the ADM-3A. One leg of the current loop may be tied through a register to +12V dc to create a current source. As an alternative, a ground strap may be used instead of the resistor, to act as a sink for an external positive source, or a current source for an external negative voltage.

4.3.14 Video Blanking and Serializer Logic

Logic that controls blanking during horizontal and vertical retrace time, and converts the parallel-bit ROM outputs to a serial bit stream, is shown in figure 4-14.

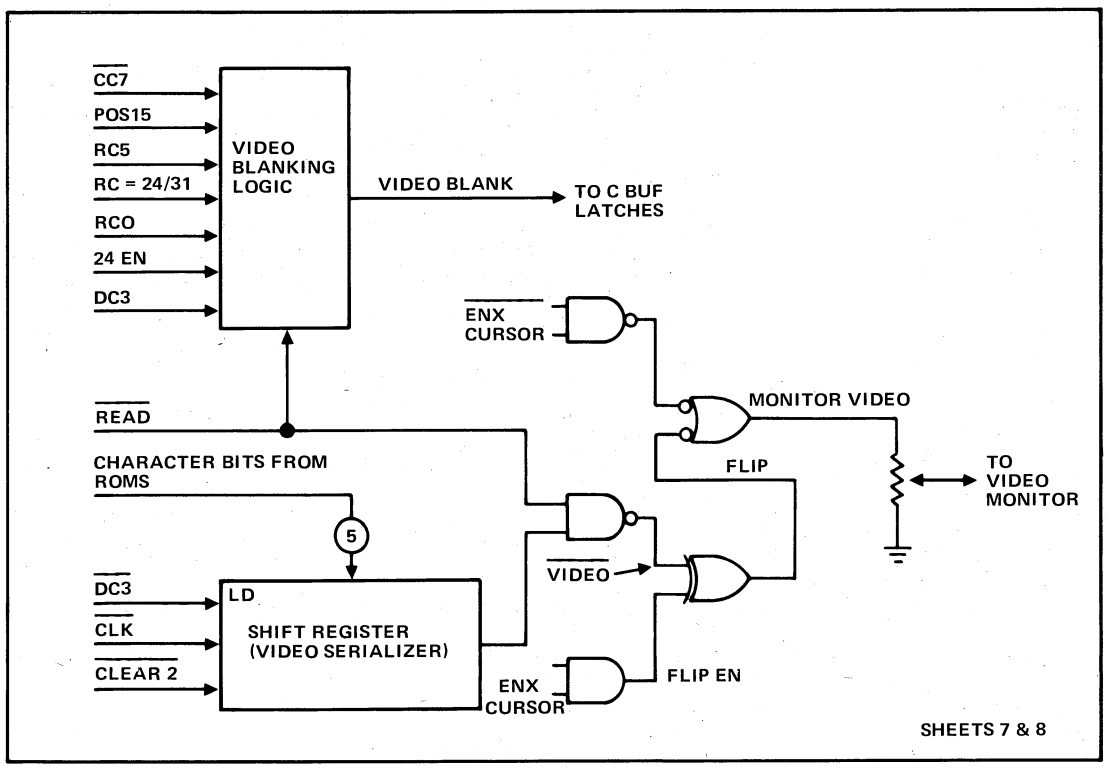


Figure 4-14. Video Blanking and Serializer Logic, Block Diagram

Terms CC7, POS15, and RC5 control blanking for row counts of 32 and higher, and are effective only when the ADM-3A is operating at a vertical rate of 50-Hz (the count reaches only 29 in 60-Hz operation). For counts below 32, term RC=24/31 controls blanking.

Terms RC0 and 24EN cause all even-numbered character rows to be blanked if the ADM-3A is operating with a 12-line display.

In every case, VIDEO BLANK is clocked to the memory buffer latches by BDC3 as the current character is completed. VIDEO BLANK clears the buffer latches but, because bit 6 is normally inverted, the USASCII SPACE code is presented to the ROMs, instead of NULL.

During a read-back test operation, READ blanks the video but permits sending CBUFn data to transmitter logic.

The video serializer is an 8-bit shift register. Term DC3 loads it with the ROM output character bits every 643 nsec, and the bits are shifted (by CLK) at a rate of 10.8864 MHz. The shift register output is ORed with cursor information to produce the MONITOR VIDEO signal. The video level adjustment potentiometer is located at these circuits.

4.3.15 Monitor Drive Logic

This logic (shown on sheet 7 of the logic diagram) generates signals that trigger horizontal and vertical drive cycles in the monitor. To obtain the horizontal drive signal HDRIVE, character position counts are decoded to set HDRIVE false at the start of a row. HDRIVE is set true one count after the rise of CC7 to start the video retrace period.

The vertical drive cycle is begun by VDRIVE. This signal is generated by decoding character row counts RCn, and setting theVDRIVE flip-flop one count after the last character of the last line has been written. The flip-flop is clocked by the HDRIVE signal for the line just completed.

The level 60EN controls timing for 50-Hz or 60-Hz power lines. Refer to figure 4-4 for timing diagrams.

4.3.16 Baud Rate Select Logic

Figure 4-15 illustrates the logic used to generate and select baud rates for data transmission and reception.

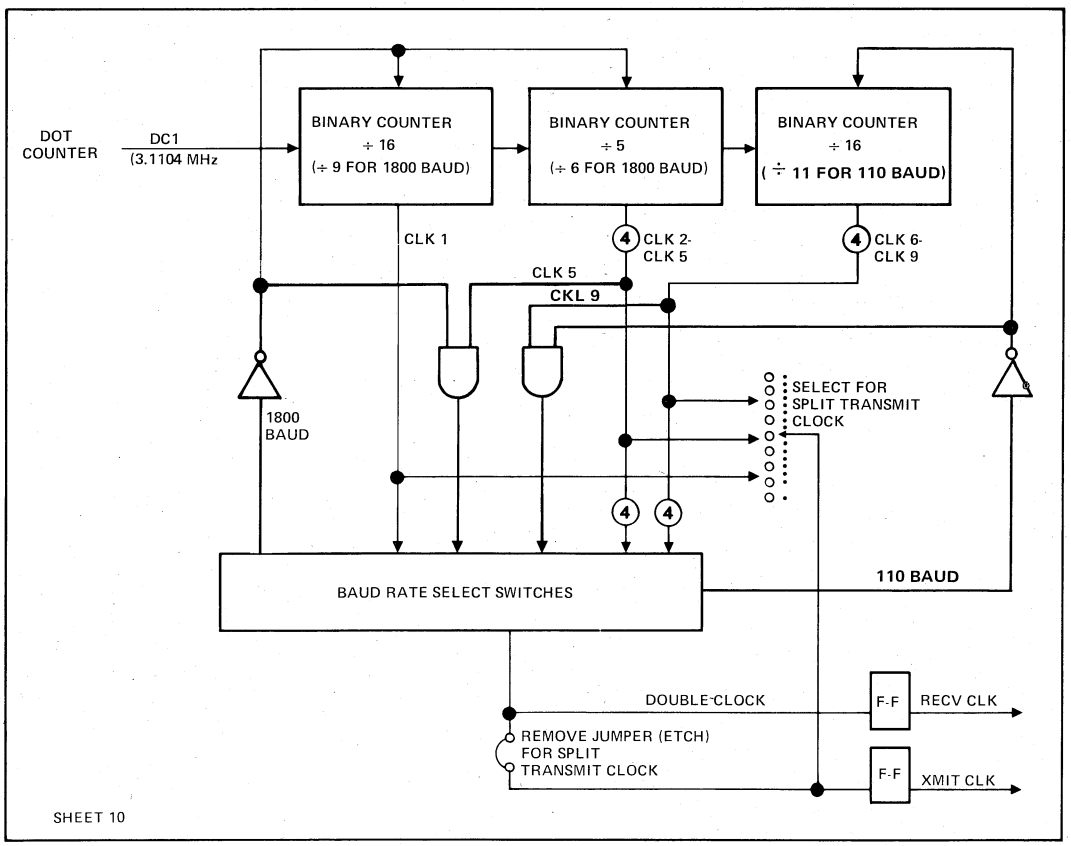


Figure 4-15. Baud Rate Select Logic, Block Diagram

The basic clock used in this logic is the 3.1104-MHz pulse stream DC1, which originates at the display dot counter. The 3 binary counters divide pulse rates by 5, 16 and 16 respectively except when an 1800 or 110 baud rate is selected. These rates (from 75-19,200 baud) are obtained from the counters and are selected by means of a BAUD RATE Switch.

When BAUD RATE switch 1800 is on, the 3 binary counters divide pulse rates by 6, 9 and 16 respectively and CLK5 is selected as the double clock.

When BAUD RATE switch 110 is on, the counters divide the pulse rate by 5, 16 and 11 respectively and CLK9 is selected as the double clock.

The double clock rate is divided by flip-flips to provide the RECV CLK and XMIT CLOCK signals. Normally, both flip-flops are clocked at the same rate. However, when a split clock is required, the XMIT CLOCK may be derived from another rate selected by means of a rotary switch located inside the ADM-3A case.

When the common clock is used, the rotary switch must be in position 12. When the split clock is used, the printed circuit joining clock inputs of both flip-flops must be cut.

NOTE: XMIT CLOCK can be split off only if the RECV CLOCK is **NOT** set to 110 or 1800 baud.

4.3.17 Interface Control Logic

Interface control logic appears on sheet 12 of the logic diagrams. This controls request-to-send and clear-to-send communications for the ADM-3A.

CLR TO SEND (high) permits data transmission logic to produce UART XMIT CLK, sending data from the ADM-3. If CLR TO SEND falls while a byte is being transmitted, TRE maintains the transmit clock until the byte has been completed, and then falls to shut off the clock and return the line to the marking state.

REQ TO SEND (RTS) may be controlled in any of four ways, as follows:

a. RTS may originate at an extension port.

b. If switches 202, 103, and LOCAL are all open RTS remains low all the time.

c. If only switch 103 is closed, RTS remains high all the time.

d. If only the LOCAL switch is closed, signals THRE and TRE control RTS. RTS rises to transmit each character, and falls when the character has been shifted out of the ADM-3A.

e. If only the 202 switch is closed, RTS may be controlled through the ADM-3A interface in either code-turnaround, or reverse-channel operation.

4.3.17.1 Code-Turnaround Control. Either an ETX code or an EOT code may be selected to initiate turnaround, depending on the position of the ETX-EOT switch. When the selected code appears in the input data, LATCHED CODE is set. When CARRIER DETECT falls (figure 4-16), indicating that the remote end of the line has dropped, RTS is set.

RTS is reset when ETX or EOT is again decoded, and the logic switches to the receive mode. Following a turnaround command, no further command will be recognized for approximately 250 msec. This interval gives the modem time to propagate its signals. The interval is timed-out by two flip-flops and a counter, and the signal SBEN controls resetting of RTS.

4.3.17.2 Reverse-Channel Control. In reverse-channel operation RTS is controlled by SEC RECV DATA (SB) and CARRIER DETECT (CF) from the modem. When SB goes low, RTS is unconditionally reset (figure 4-17), switching the interface to receive data. In normal reverse-channel receive operation, CF is high at this time, causing SEC XMIT DATA to rise.

When the remote end of the line raises SB, and then drops its RTS (and CF), the ADM-3A turns on its RTS. The ADM-3A will then ignore further commands for a 250-msec period while the modem propagates its signals.

4.3.18 Power Supplies

AC power is applied to the transformer through the ON/OFF switch on the rear of the ADM-3A. The different stepped-down ac voltages connect to the main circuit board through connectors J3 and J4.

Rectifiers, filter capacitors, and voltage regulators are all located on the main circuit board. Three type 7805 devices provide the +5V dc logic supply, and two type 7815 devices furnish 12V dc to operate memory devices and interface drivers.

A +15V dc supply required by the monitor is made up of a type 7815 device and a simple transistor shunt regulator. Located at the bottom of the terminal pan is a primary fuse. It is an 8/10 amp Slo-Blo 115V fuse or a 4 amp Slo-Blo 230V fuse.

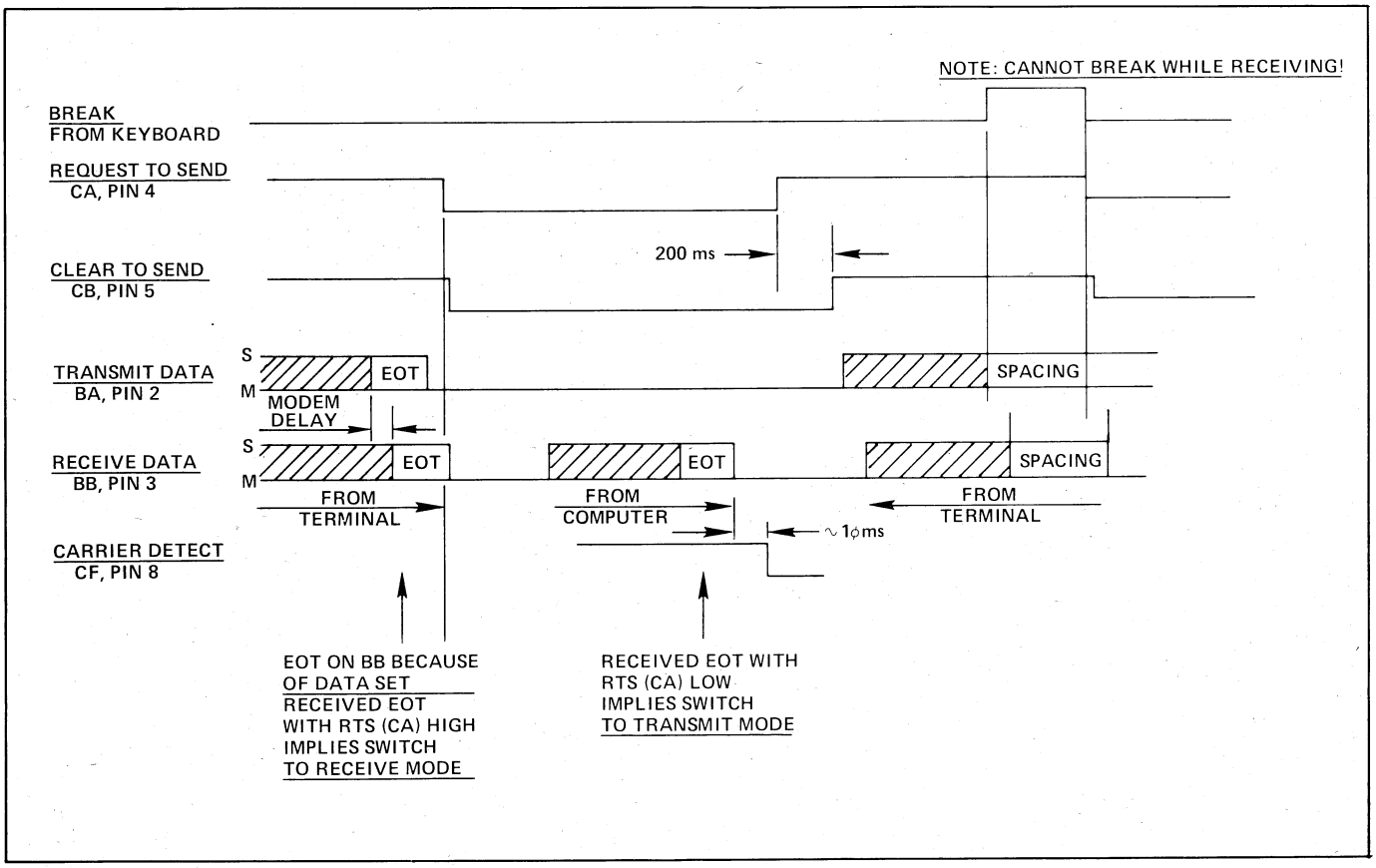


Figure 4-16. Interface Timing for Code Turnaround

4.3.19 CRT Display Monitor Logic

VIDEO AMPLIFIER

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101 and its components comprise the video output driver with a gain of about 17. Q101, operating as a class B amplifier, remains cut off until a DC-coupled, positive-going signal arrives at its base and turns on the transistor. R111 adds series feedback which makes the terminal-to-terminal voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient temperature variations.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential at the grid and is varied by the brightness control.

VERTICAL DEFLECTION

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116 and Capacitors C105 and C106 form an RC network providing proper timing.

When power is applied, C105 and C106 charge exponentially through R115 and R116 until the voltage at the junction of R116 and C105 equals the anode "A" firing voltage. At this time, one of the unijunction's diodes that is connected between the anode and anode gate "G" becomes forward biased allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R120.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter. Therefore, the changing of firing points from one device to another, together with the temperature dependency of this parameter, is no longer a problem as it can be with conventional transistors.

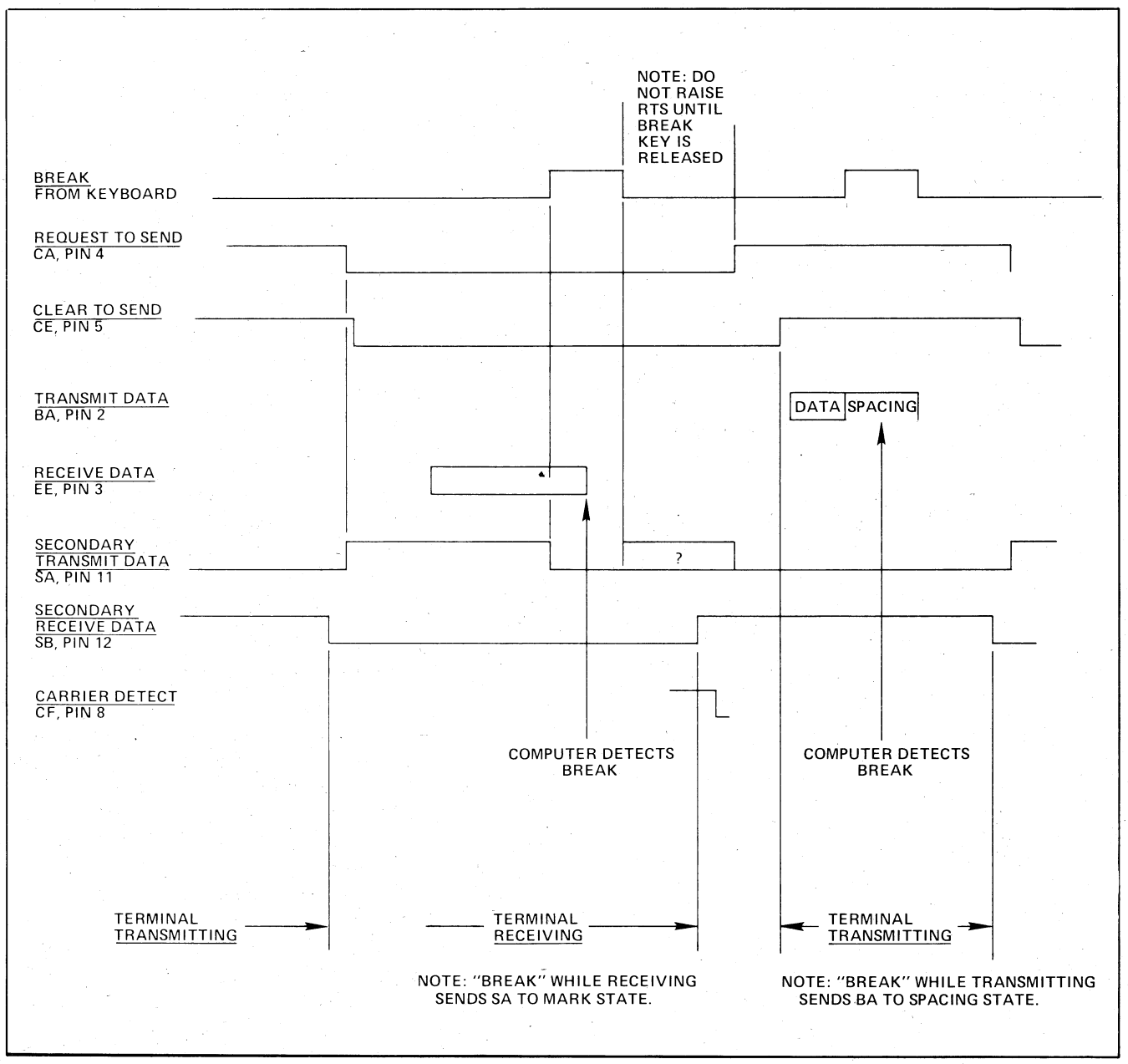


Figure 4-17. Interface Timing for Reverse-Channel Operation

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113. At the time of the vertical interval, an external negative pulse is applied through R113, C104, and CR101 to the gate of Q102, causing the firing level of the unijunction to decrease.

The sawtooth voltage at the anode of Q102, is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104.

The output waveform from the unijunction oscillator is not suitable, as yet, to produce a satisfactory vertical sweep. Such a waveform would produce severe stretching at the top of the picture and compression at the bottom. C105 and C106 modify the output waveform to produce satisfactory linearity. The sawtooth waveform output at Q103 is coupled through R122, the

vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope. Slope change rate is determined by the position of the variable resistor R121.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power type transistor which operates as a class A amplifier. No output transformer is required since the output impedance of the transistor permits a proper impedance match with the yoke connected directly to the collector. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

HORIZONTAL DEFLECTION

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. The circuitry associated with Q105 and Q106 has been designed to optimize the efficiency and reliability of the horizontal deflection circuits.

A positive going pulse is coupled through R127 to the base of Q105. The amplitude and duty cycle of this waveform must be as indicated in the electrical specifications (Section 1.2) for proper circuit operation.

The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling tranformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

The horizontal output stage has five main functions: to supply the yoke with the correct horizontal scanning currents; develop a "C" VDC supply voltage for use with the CRT; develop a "B" VDC supply voltage for the video output stage; and develop a "D" VDC for the CRT bias.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, also serves to block DC currents through the yoke and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not describe the same arc.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by CR110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12 kV (9 and 12 inches) or 9 kV (5 inches), "C" VDC, and "B" VDC respectively. 12 kV or 9 kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier Q101.

LOW VOLTAGE REGULATED SUPPLY

All models use a series-pass, low voltage regulator designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240 V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VDC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

Operation of this regulator may be better understood by assuming a certain operation condition has caused the output voltage to increase above normal. This positive increase of voltage is transferred to the base of Q202 where it is compared to the zener of VR201. The increase of forward bias of Q202 causes the collector voltage to drop as a result of the increased collector current through R202. This voltage is directly coupled to the base of Q1 through Q201 where it causes Q1 to conduct less and brings the regulated voltage back to its proper state.

The short circuit protection or current limiting action can be explained as follows. Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of Q202 turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on. Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector voltage of Q203 which is detected by the base of Q201 and direct-coupled to the base of Q1 causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition. Circuit breakers and fuses are not fast enough to protect transistors.

4.3.20 ADM-3A Answer Back

The ADM-3A answer back option provides the transmission of a predetermined message of up to 32 characters in length. This message can be sent by depressing the "here is" key on the keyboard or by the computer command "ENQ." The message is stored in a read only memory (ROM) and is supplied at time of purchase. This message can be exchanged by LSI customer service.

4.3.21 ADM-3A Extension Port Current Loop

The extension port of the ADM-3A provides an auxiliary port for interfacing other peripheral devices in a loop through or daisy chain environment.

The addition of current loop to this port adds to the flexibility and allows more devices to hook up in this manner.

The transmitted data output for current loop is on pin 25 of connector J-2 and does not supply current (external source). Received data is inputed on pin 2 and is internally grounded (Terminal ground).

4.3.22 ADM-3A Numeric Pad

The numeric pad option (Figure 4-18) provides 14 keys for operator convenience. These keys consist of 10 numeric (0-9), 3 punctuation (- . ,) and an "Enter" key. The codes associated with these are transmitted as such with the exception of "Enter" which transmits the ASCII character "RETURN."

NOTE

The numeric keys on the Key pad parallel the numeric on the standard Keyboard, therefore, if the shift key is depressed when using the keypad, the shifted characters will be generated as on the standard keyboard.

Figure 4-18. ADM-3A Numeric Key Pad

SECTION 5
MAINTENANCE

5.1 GENERAL

This section contains instructions and information for performing routine and corrective maintenance of the ADM-3A. It is assumed that the maintenance technician is thoroughly familiar with information in Sections 1 through 4 of this manual.

5.2 INSTALLATION

It is assumed that the ADM-3A has been installed and set-up for operation in accordance with procedures outlined in Section 2. Any operating problem following installation should be approached initially by checking settings of internal switches and front panel switches located under the identification plate, and checking interface cables. Figure 5-1 shows assignments of terminals in interface connectors J1 and J2.

5.3 ROUTINE MAINTENANCE

The operator is expected to keep the exterior of the ADM-3A clean. The case should be cleaned using a household cleaner and a soft, damp, lint-free cloth or paper towel. **NEVER** use a petroleum-base solvent such as lighter fluid which could damage the plastic or painted surface.

Be careful not to wipe dust into the keyboard, and don't let excessive spray cleaner run between the keys.

Other than cleaning, the ADM-3A needs no routine maintenance.

5.4 OPENING ADM-3A COVER

To remove the cover of the terminal (along with the monitor CRT) for access to adjustments or for other maintenance, proceed as follows:

a. Remove the two slot-head screws located under the front corners of the terminal base.

b. Lift the cover from the front, lifting it upward and rearward until it is lowered to rest on the table.

c. To remove the cover from the base, disconnect the cable connecting the monitor to the printed circuit board, slide the cover toward the left on its hinge pins, and then remove the cover from the base.

Note that all components on the ADM-3A circuit board are accessible for inspection and voltage measurement when the cover is fully open.

5.5 ADJUSTMENTS

All adjustments in the ADM-3A are associated with the CRT monitor.

5.5.1 Contrast Adjustment

Contrast may be adjusted for best viewing by the operator. The control is located at the upper right-hand corner of the keyboard.

5.5.2 Brightness Adjustment

The brightness (background intensity) control is located on the video board assembly within the ADM-3A cover.

WARNING

Brightness must be adjusted with power applied to the ADM-3A. To avoid hazardous electrical shock, adjust using a non-conductive screwdriver and considerable care.

Adjust brightness just to the level at which the white raster is extinguished. The optimum contrast can then be obtained when a video signal is applied.

5.5.3 Vertical Adjustment

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

a. Apply video and synchronization signals to the monitor.

b. Set the vertical frequency control (R116) near the mechanical center of its rotation.

c. Adjust the vertical height control (R124) for desired height.

d. Adjust the vertical linearity control (R121) for best vertical linearity.

e. Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.

f. Readjust the vertical frequency control (R116) until the picture rolls up slowly.

g. Restore vertical drive to the monitor.

h. Recheck height and linearity.

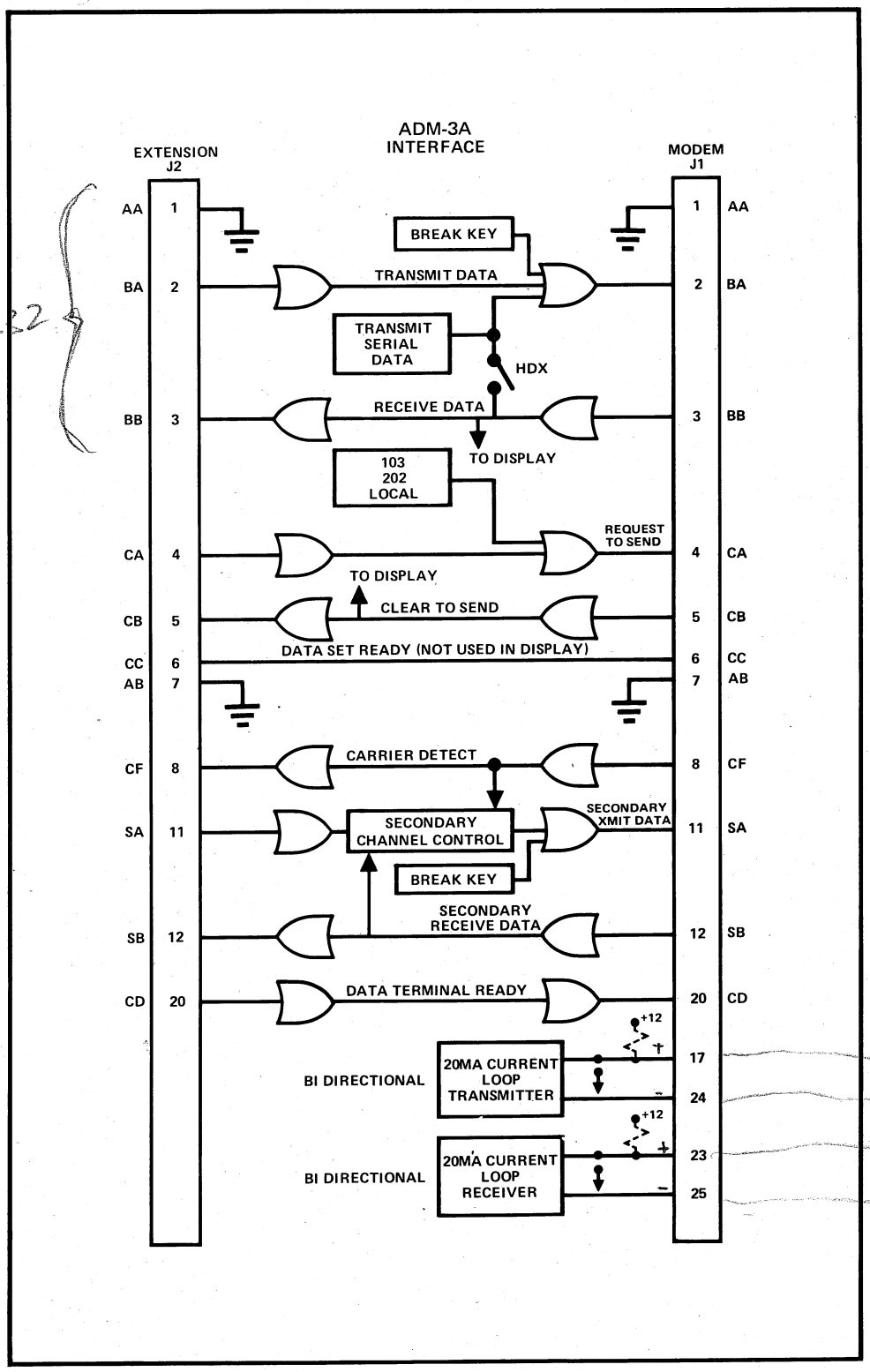


Figure 5-1. Interface Connector Terminal Assignments

5.5.4 Horizontal Adjustments

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

a. Apply video and synchronization signals to the monitor. Insert the horizontal linearity sleeve about 2/3 of its length under the yoke. (If you received a monitor from the factory in which the placement of the linearity sleeve has been determined, make a mark on the sleeve and reinsert the sleeve to this mark when removal of the yoke and linearity sleeve are required.)

   If the linearity sleeve is inserted farther than necessary, excessive power will be consumed and the horizontal output circuitry could be overstressed.

b. Adjust the horizontal width coil (L101) for the desired width.

c. Insert the linearity sleeve farther under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.

d. Readjust L101 for proper width.

e. Observe final horizontal linearity and width, and touch up either adjustment if needed.

No horizontal hold control is used in this monitor.

5.5.5 Focus Adjustment

The focus control (R107) adjusts best overall display focus. However, because of the construction of the gun assembly in the CRT, this control does not have a large effect on focus.

5.5.6 Centering

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

Do not use ring magnets to offset the raster from its nominal center position; this will degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

5.6 CORRECTIVE MAINTENANCE

Corrective maintenance consists of locating the cause of a malfunction and repairing it. The cause may be isolated only to the module level, with the failed module sent to a repair facility or returned to Lear Siegler for repair or replacement; or the user may choose to isolate the cause to the component level and replace the failed component.

Repair at the component level should not be attempted except by trained personnel using suitable tools and test equipment.

5.6.1 Failure Analysis

Troubleshooting of the ADM-3A is straightforward and conventional. Suggested steps in troubleshooting are:

a. **Get the facts.** Learn the state of the machine when the malfunction occurred. Look for operator error, blown fuses, or modem or computer failure.

b. **Operate the ADM-3A to determine which functions have failed.** For example: Does it receive but not transmit? Has a single function (like Clear Screen or Backspace) failed? Intelligent use of this information will speed fault isolation.

c. **Isolate the cause of the failure to a specific module** (for example, to the CRT, a keyboard row, the flyback assembly, or the main circuit board).

d. If the failed module is to be repaired at the machine site, **further isolate the cause to a failed component** (or components). Refer to information in Section 4 and to the logic and assembly drawings in Section 6 of this manual.

e. **Replace the failed module or component and test** by running the ADM-3A in the same mode of operation in which the failure occurred.

f. **Record the symptoms, cause, trouble-shooting procedure, and mode of repair** for future reference.

Following are useful ideas to speed troubleshooting and repair:

a. After warmup, the cursor should appear at its "home" position. If it does not, enter data from the keyboard (with the HDX/FDX switch in the HDX position) and see if it appears on the screen. If it does not, proceed to check power supply voltages, intensity and contrast control settings, clock and display counter operation, monitor sweep drive signals and monitor video and drive circuits, in that order.

b. To verify operation of transmitter logic, simply see that data generated at the keyboard appears on the screen (HDX/FDX switch in the HDX position only!). This checks all transmitter logic except the inverter B7-10 and

driver A9-3. To check FDX, create a short in pins 2 and 3 of the modem connector. This will also check the inverter B7-10 and the driver A9-3.

c. It is possible to use internal turnaround switches (LOCAL, 103 and 202) to force Request to Send to either state, or put it under ADM-3A control. Intelligent use of these switches, and reference to paragraph 4.3.16, may simplify interface troubleshooting.

5.6.2 Troubleshooting the Monitor

Following is a guide to troubleshooting the CRT monitor. It is assumed that sweep drive and video signals from the main circuit board are normal (see figure 5-2).

a. **Screen is dark.** Check settings of brightness and contrast controls. Check +15V dc supply at junction of R114 and R130. Check security of all monitor connectors.

b. **No video.** Check setting of contrast control, check Q101 (refer to monitor schematic diagram in Section 6 of this manual).

c. **Overheating** and excessive power consumption. Check horizontal linearity sleeve (para. 5.5.5) Check Q105 and Q106.

Refer to the monitor voltage waveforms (figure 5-3), and component layout (figure 5-4), and to cabling and schematic diagrams in Section 6 of this manual.

5.6.3 Removing and Replacing Monitor CRT and Subassemblies

WARNING

Be sure to discharge anode voltage to ground before attempting to remove any monitor subassembly or CRT.

The monitor comprises the CRT with its steel mounting frame, the flyback assembly, and the circuit board.

To remove the CRT, proceed as follows:

a. Unhook (at both ends) the spring that lies across the CRT.

b. Remove connector from the base of the CRT.

c. Remove the anode connector from the lower surface of the CRT.

d. Using a socket wrench or screwdriver, loosen the clamps at both sides of the CRT frame until the clamps can be turned to clear the CRT frame.

e. Grasping the CRT securely, lift it upward and out of the ADM-3A cover and set it aside.

To install a new CRT, follow the preceding steps in reverse order.

To remove the flyback assembly, proceed as follows:

a. Disconnect anode connector from CRT.

b. Disconnect Molex connector that connects flyback assembly to the monitor circuit board.

c. Using a screwdriver, loosen the hex-head screw that clamps the flyback assembly to the molded cover.

d. Lift flyback assembly upward until the screw clears the slot in the mounting plate, then remove assembly from the cover.

To remove the monitor circuit board, proceed as follows:

a. Remove the flyback assembly (refer to preceding steps).

b. Disconnect all Molex connectors from the monitor circuit board.

c. Slide circuit board from the slots in the molded cover and remove.

To replace monitor circuit board and flyback assembly, perform the preceding steps in reverse order.

5.6.4 Troubleshooting the Main Circuit Board

Troubleshooting of the main circuit board is based essentially on the principles outlined in paragraph 5.6 — that is, the technician must be familiar with the theory of operation (Section 4) and must be equipped with suitable test equipment.

With the ADM-3A cover opened, all components on the main circuit board are accessible to probes and other test devices. Components are generally identified on the board; but reference may be made to the component layout drawing, and the logic diagrams in Section 6 of this manual.
Table 5-1 lists connectors on the board and defines all terminal assignments.

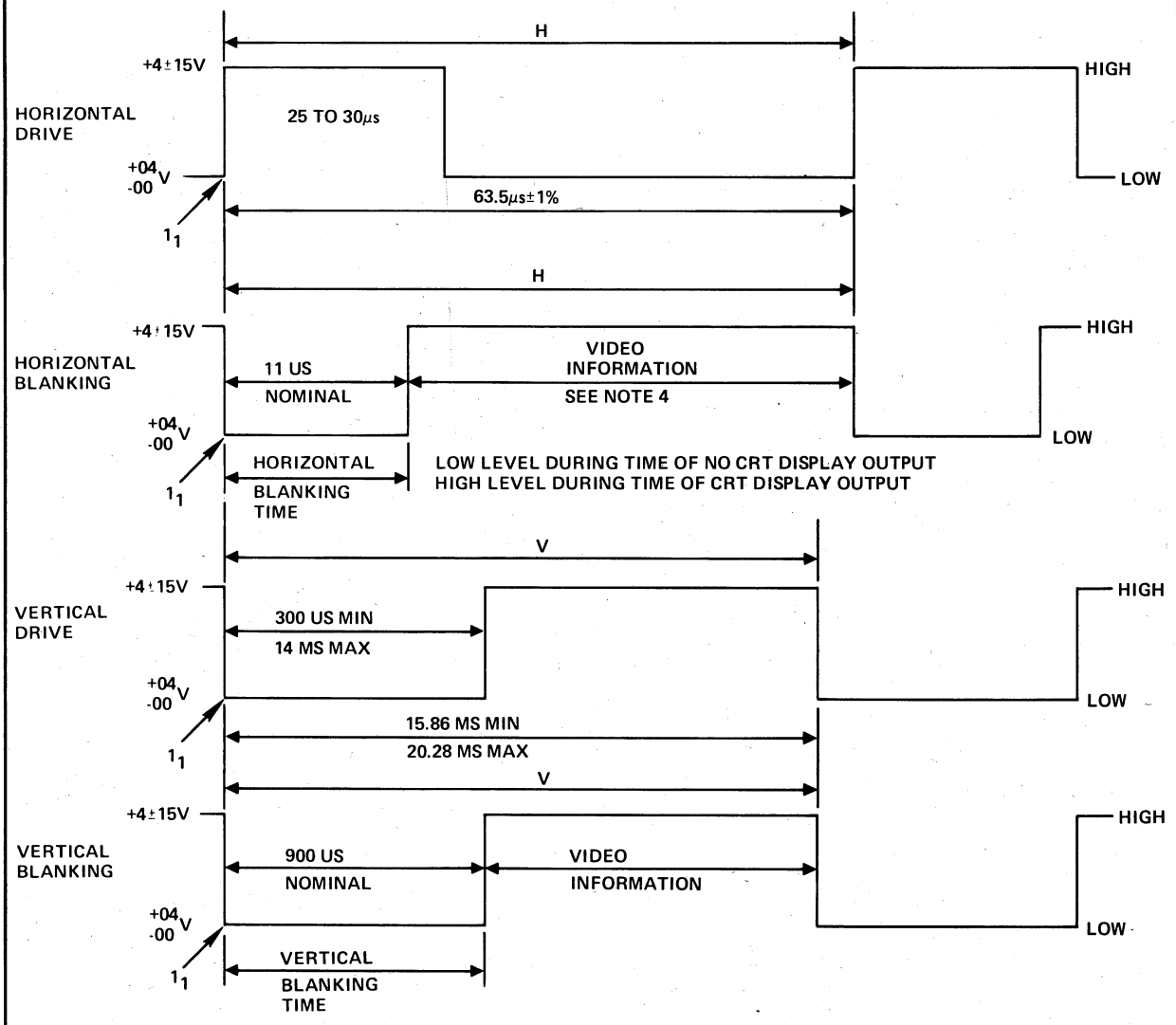
5.6.5 Removing and Replacing the Main Circuit Board

To remove the main circuit board, proceed as follows:

a. Remove external cables from connectors J1 and J2 at the rear of the ADM-3A.

b. Remove all cable connectors from the upper surface of the circuit board.

c. Lift circuit board straight upward to clear the guide pins, then remove from the base.



NOTES

1. The leading edges of Drive and Blanking waveforms must start at time tp. Nominal Blanking times should be observed.
2. H = time from start of one line to start of next line.
3. V = time from start of one field to start of next field.
4. Video pulse width should be equal to or greater than 100 nsec.

Figure 5-2. Inputs to Monitor, Timing Diagram

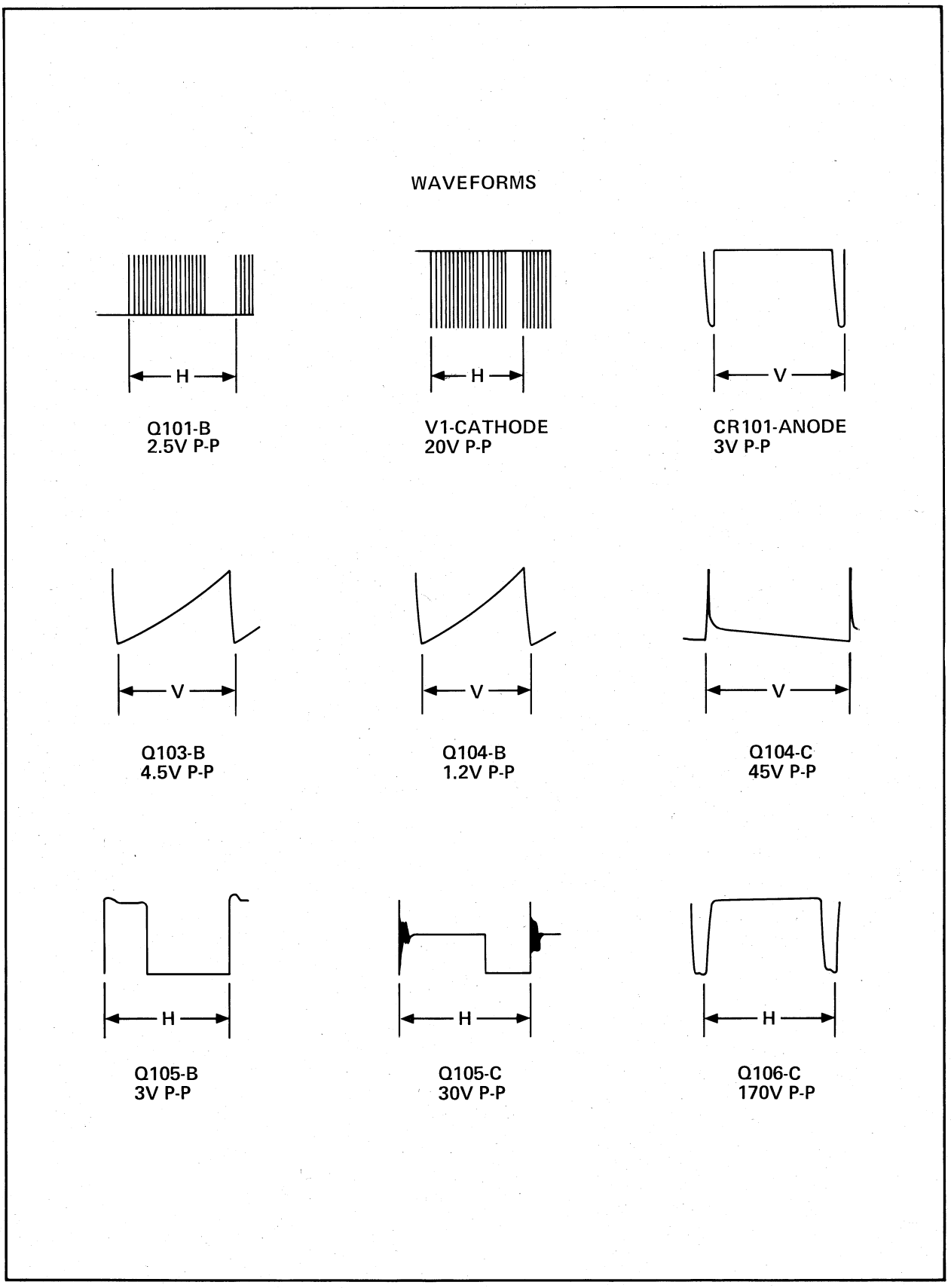


Figure 5-3. Monitor Voltage Waveforms

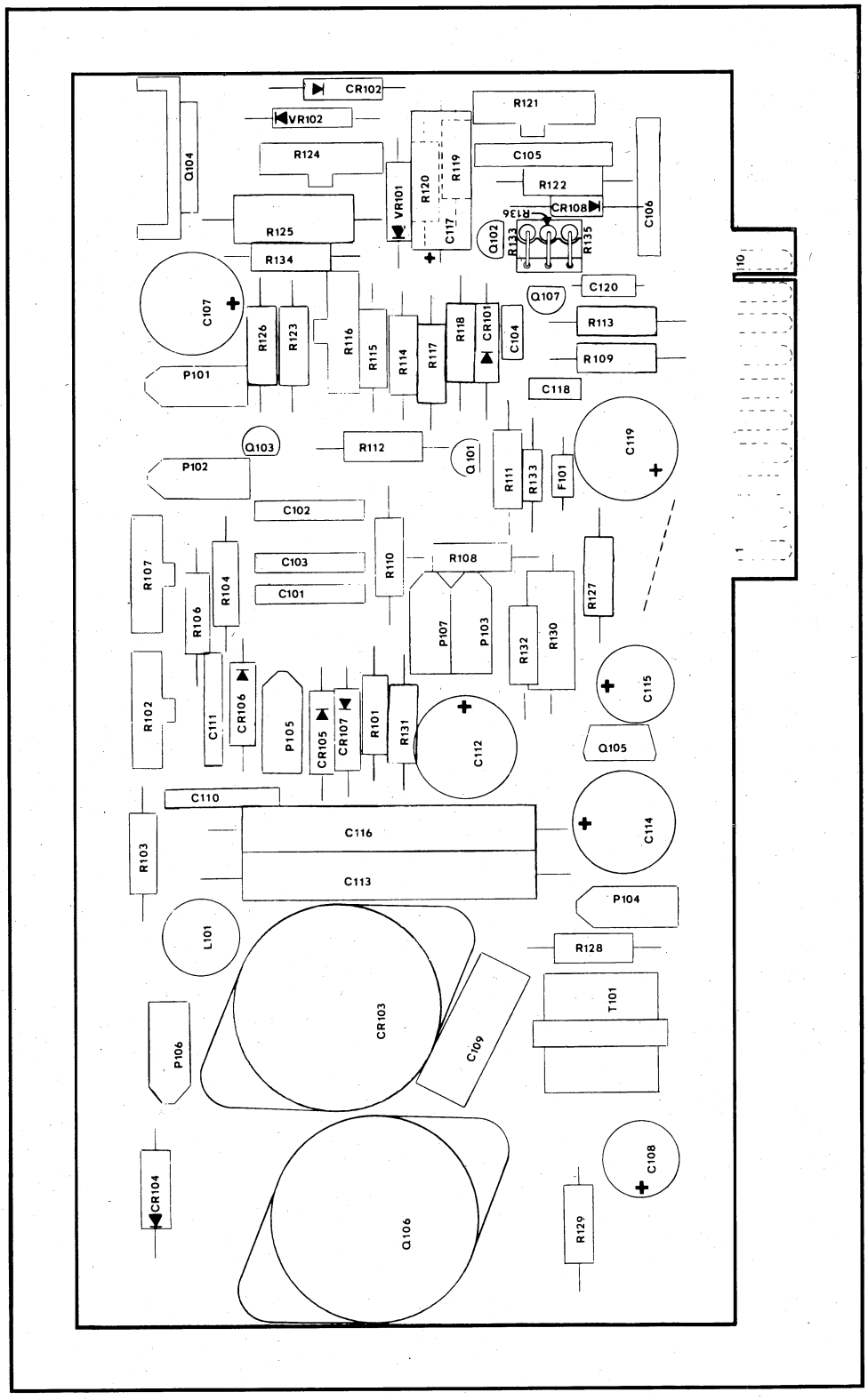


Figure 5-4. Monitor Video Board, Component Layout

Table 5-1. Main Circuit Board Connector Terminals

Connector/Symbol	Pin	Signal
RS232 Interface (J1)	1	Frame Ground
	2	BA (Transmit Data)
	3	BB (Receive Data)
	4	CA (Request to Send)
	5	CB (Clear to Send)
	6	CC (Data Set Ready)
	7	Signal Ground
	8	CF (Carrier Detect)
	9,10	(not used)
	11	SA (Secondary Transmit Data)
	12	SB (Secondary Receive Data)
	13-16	(not used)
	17,24	Current Loop Transmitter
	20	CD (Data Terminal Ready)
	18-22	(not used)
	23,25	Current Loop Receiver
RS232 Extension (J2)	1	Frame Ground
	2	BA (Transmit Data)
	3	BB (Receive Data)
	4	CA (Request to Send)
	5	CB (Clear to Send)
	6	CC (Data Set Ready)
	7	Signal Ground
	8	CF (Carrier Detect)
	9,10	(not used)
	11	SA (Secondary Transmit Data)
	12	SB (Secondary Receive Data)
	13-19	(not used)
	20	CD (Data Terminal Ready)
	21-25	(not used)
Low-Voltage AC Power (J3)	1,2	Input to +V dc rectifier
	3,5	Input to +12V dc rectifier
	4	Ground
Monitor Low-Voltage AC Power (J4)	1,2	Input to +V dc rectifier
	3	
Beep Speaker (J5)	2,3	Drive to beeper speaker
Keyboard Interface to 10-Key Pad (J6)	2,3,16	Col 3, 2, 0
	5,9,10	Row 0, 1, 2
	11,12,13	Row 3, 4, 5
	14,8,7	Row 6, 7, 8
	5,1,15,4	Row 9, C, D, E
Monitor Interface (J7)	1	
	2	
	3	
	4	Video to monitor
	5,6,7	Ground
	8	Horizontal drive to monitor
	10	Ground
	11	+15V dc to monitor

Note that there are no fasteners to hold the circuit board, which is kept in place by the two steel guide pins and the closed cover.

Replace the circuit board by performing removal procedures in reverse order.

5.6.6 Removing and Replacing Key Switch Contacts

The tools required to remove the key switch contacts from the keyboard are:

insertion tool and guide
soldering iron (low temperature)
wicking device
short-nosed needle nose pliers
with serrated jaws

The procedure is as follows:

a. Remove the solder from the contact (dewick) with a low-heat soldering iron so as not to damage circuit pads. The contacts will protrude about 1/32 inches beyond the back of the logic board. Make sure that the contacts are completely free of any solder by brushing them with your finger, the contacts should move freely.

b. Turn the board over so that the keyboard is up.

c. Remove the key top whose contacts need to be replaced.

d. With the pliers, firmly grasp the plunger in the corner (see figure 5-5). Pull straight up with a firm pull.

CAUTION

The plunger is fragile; pulling to the side can break plunger or housing.

e. Remove the spring.

f. With the pliers, grasp the contact and pull vertically; remove both contacts.

g. Place the insertion tool guide in the switch housing making sure that the keyway is toward the front of the keyboard. (See figure 5-6).

h. Insert the solid contact (P/N 373-30052-2) in the insertion tool with the bend to the outside and the solder end up (see figure 5-7). Insert the split contact (P/N 373-30053-2) with the split end in first (see figure 5-8).

i. Place the insertion tool into the guide matching keyway slot and key. Press the tool firmly straight down until the contacts are seated firmly (the tool clicks). (See figure 5-9)

j. Remove the tool and the guide.

k. Replace the spring.

l. Replace the plunger making sure that the bar is parallel with the contact opening. Work the plunger down slowly, separating the contacts with the crossbar of the plunger (see figure 5-10).

m. Press the plunger firmly down until it is seated (it clicks).

n. Replace the key top.

o. Turn the board over and verify that the contacts extend about 1/32 inch past the board.

p. Resolder the contacts in place.

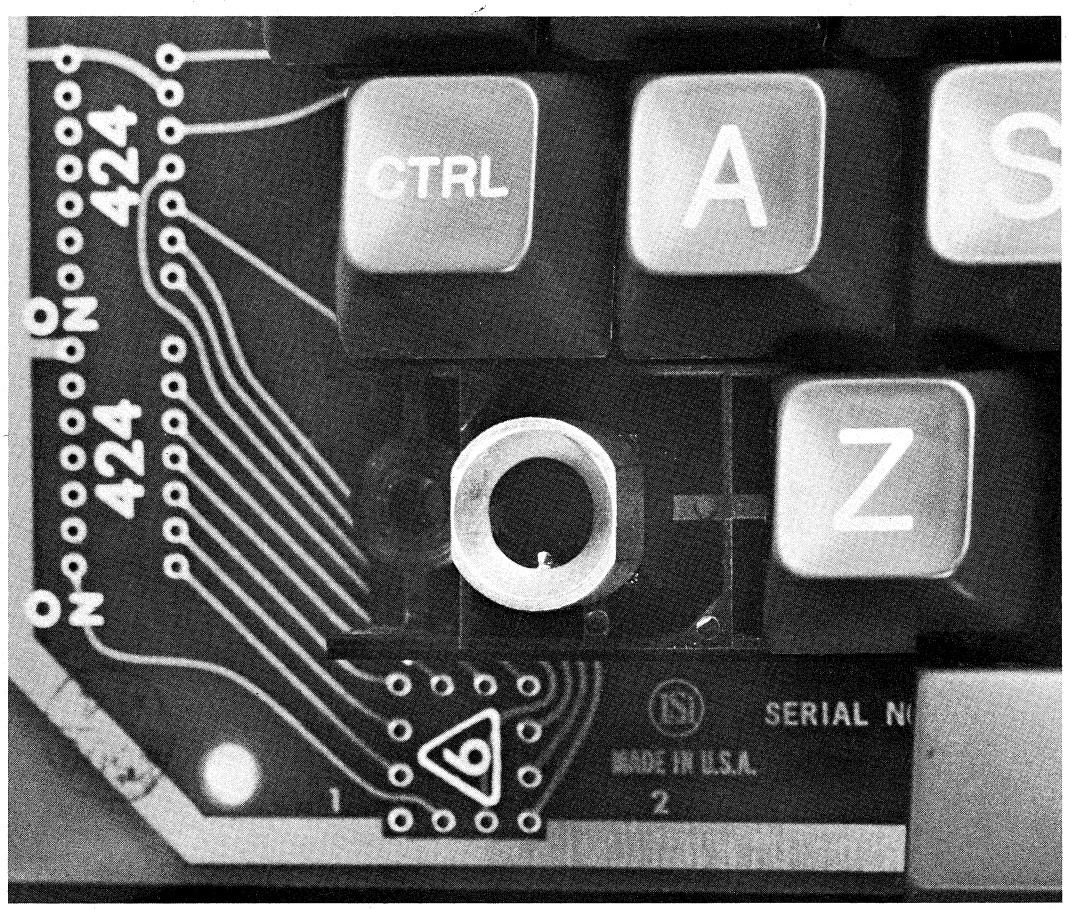


Figure 5-6

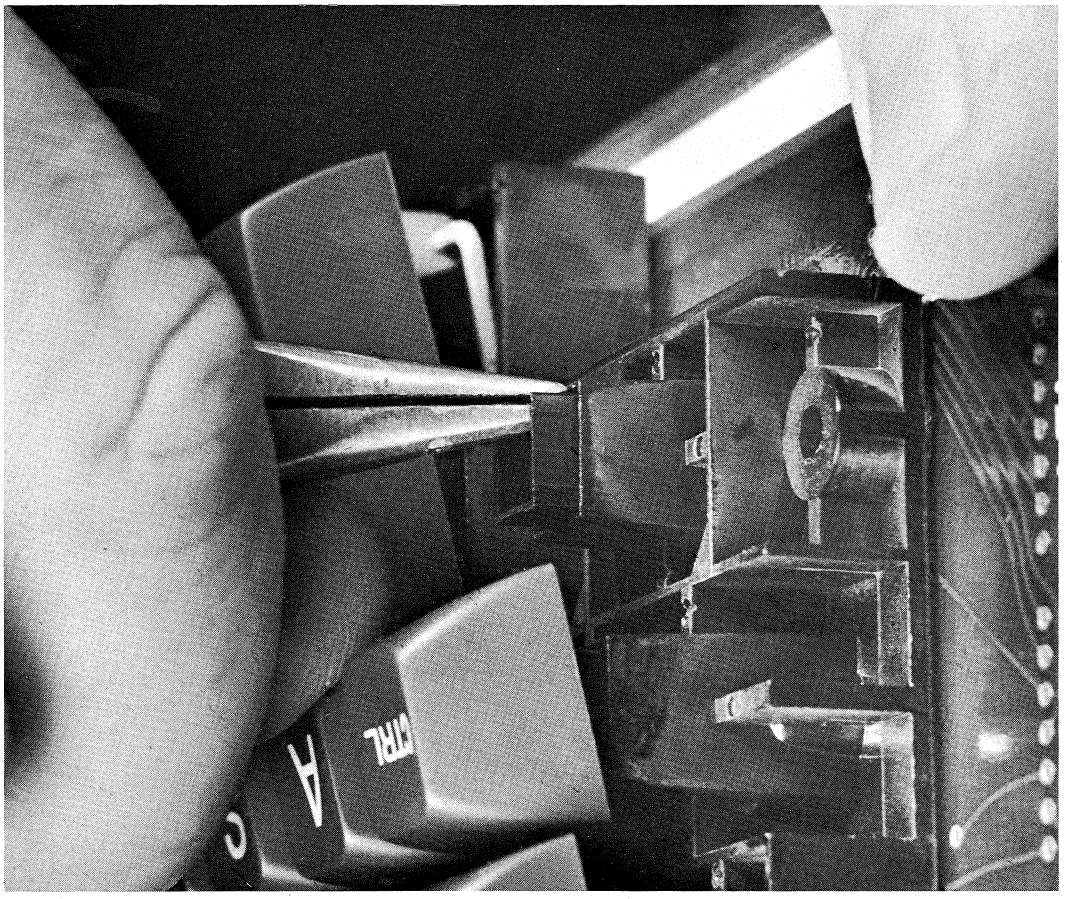


Figure 5-5

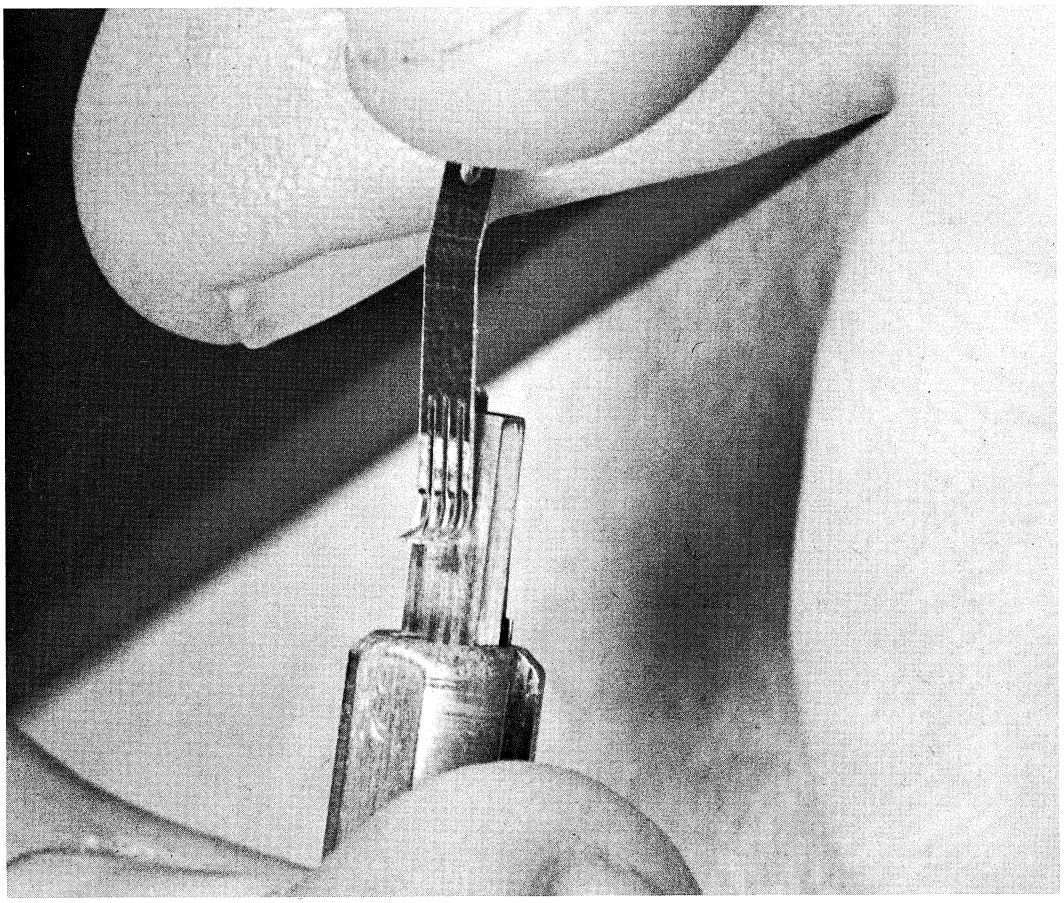


Figure 5-8

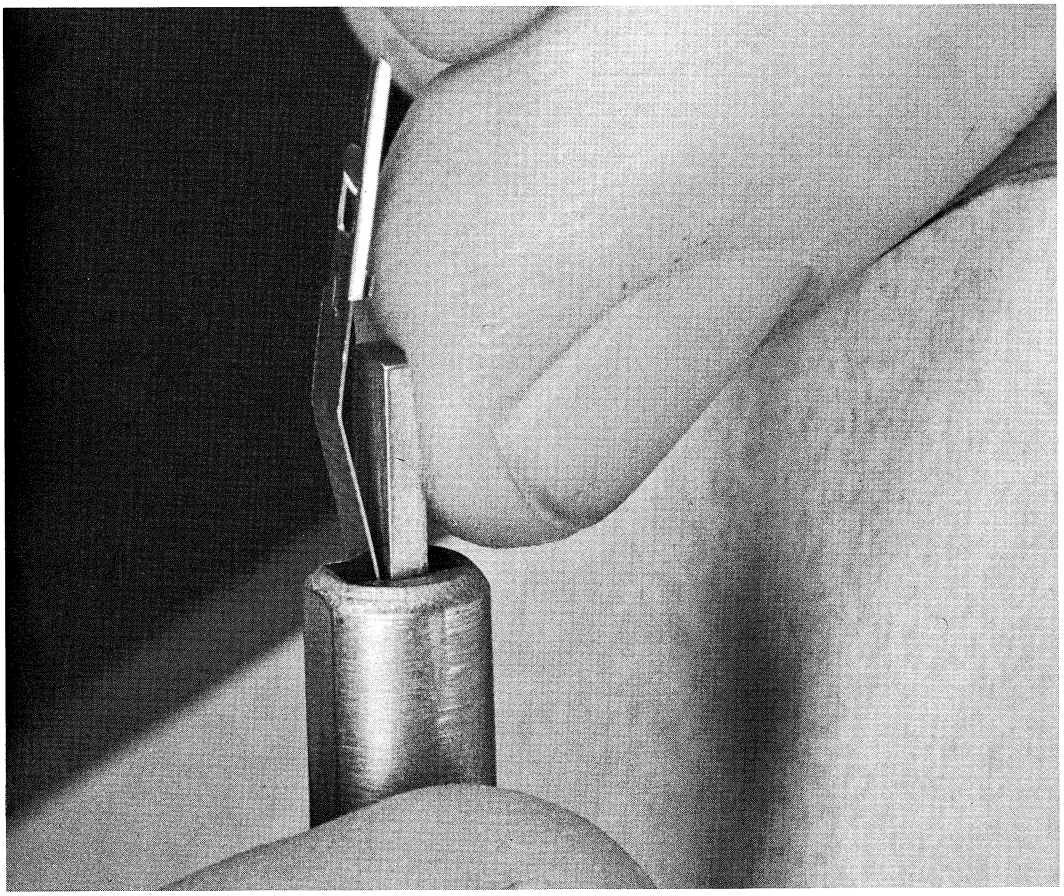


Figure 5-7

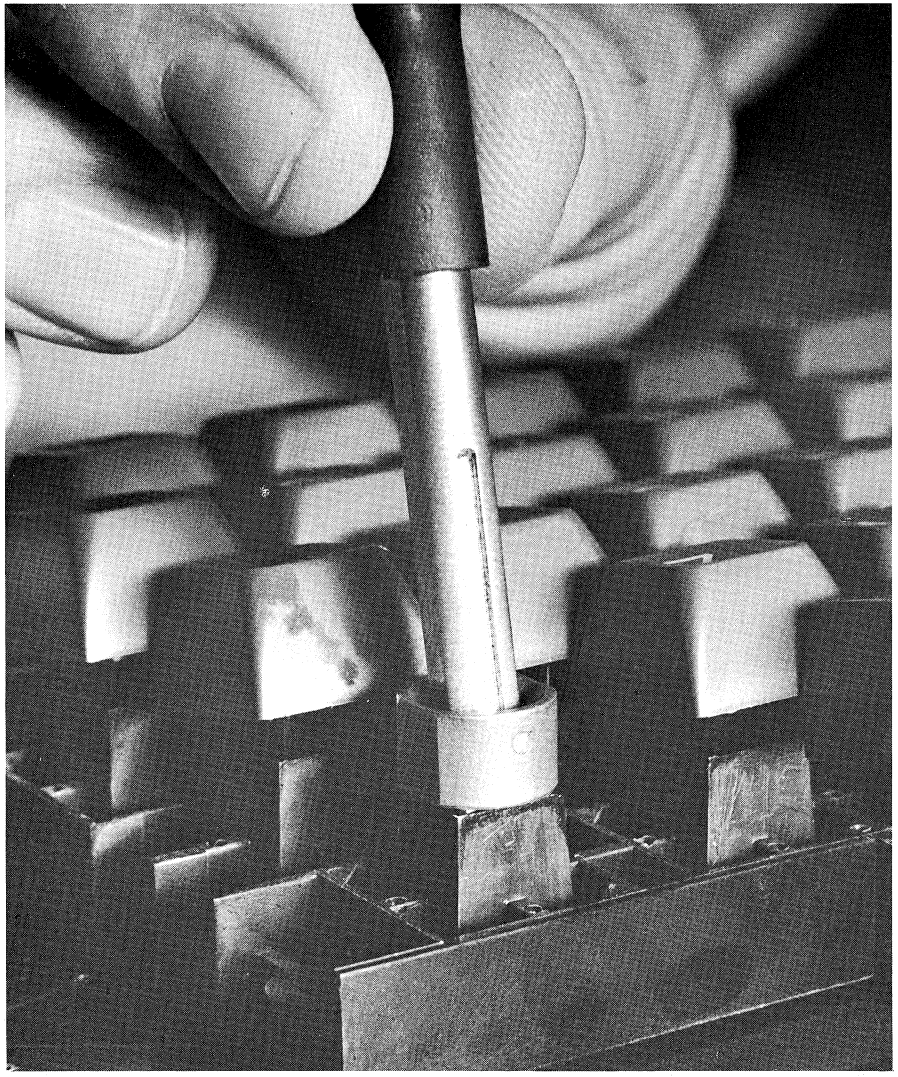


Figure 5-9

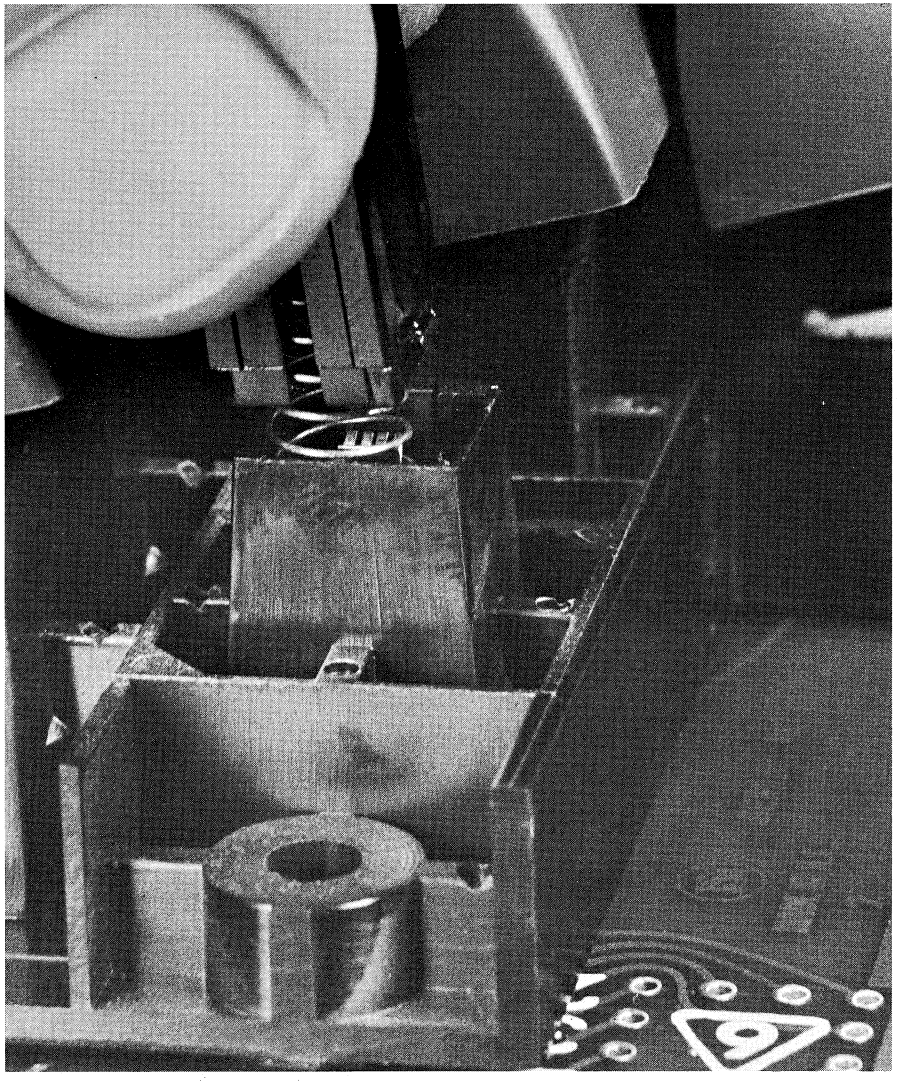


Figure 5-10

SECTION 6
DRAWINGS

This section contains drawings of the functional areas of the ADM-3A as well as a technical description of the logic in each area. The basic logic was presented in Section 4 (Theory of Operation).

6.1 SCHEMATIC SHEET #2— SYSTEM COUNTERS

The oscillator located in zone D4 provides the basic clocking for the entire display unit. It oscillates at a frequency of 10.8864 MHz (period = 91.8577 nsec.) which is twice the frequency of the video going to the monitor. This clock also goes to the DOT counter which counts the seven dot positions horizontally in a character position. This DOT counter (74LS161 — zone D2) has seven different states. It begins its cycle by presetting to a count of 10, counts through the overflow at 15, and presets again at a count of 0. The purpose of this counter is to time the presentation of the sequential addresses to the character generator and the presetting of the video serializer. Its final output, $\overline{DC3}$, has a duty cycle of 85.7% and a frequency of 1.5552 MHz. It also is the clock to the next counter in line.

The CHARACTER counter (zone C3) has eight stages and is used to time the positioning of the eighty characters and the horizontal retrace time along one video raster line. The total division provided by this counter is 96, 80 for the video portion of the raster line and 16 for the horizontal retrace. The actual count goes from 0 to 79, presets to 240, and counts out to the overflow point at 255 and restarts another cycle for the next raster line. Stages labeled CC0 through CC6 are straight binary counts while CC7 actually has a weight of 80. This means that all CHARACTER counter decodes less than 80 have CC7 low and all decodes 80 and higher have CC7 high. In practical usage, CC7 low indicates that the unit is operating in the video portion of the raster and CC7 high indicates horizontal retrace time.

The flip-flop labeled $\overline{ICC80}$ (zone C2) actually represents the decode CHAR COUNTER = 80 or one count into the horizontal retrace. This term is utilized internally to indicate the time when a command received from the normal I/O interface can be acted upon. The $\overline{LCCLK}$ circuit (zone B1) provides the clock for the following counter.

The next counter is the LINE counter which counts the raster lines in one row of characters. This counter divides by nine and is a straight binary count. Counts 0 and 8 indicate the two raster lines vertically between two rows of characters while counts 1 through 7 are the raster lines during which the video is being generated. The final stage out of this counter provides the clock for the ROW counter and has a frequency of 1.800 KHz.

The ROW counter (zone A2) is a variable counter. Its purpose is to count the rows of characters appearing vertically down the screen. It also counts through the vertical retrace time. Its count changes from a division by 30 for 60 HZ refresh to a division by 36 for 50 HZ refresh. The 50/60 HZ switch is positioned according to the frequency of the primary input power line. The ROW counter progresses in a straight binary fashion up to its selected maximum count and presets to zero.

The tri-state buffers (74LS125) located in zones D3, C4 and A4 are for the use of the automatic test equipment and essentially have no effect on the normal operation of the display unit.

6.2 SCHEMATIC SHEET #12— INTERFACE CONTROL

This schematic essentially shows the request-to-send and clear-to-send operation for the ADM-3A. The flip-flop B2 (74LS74, zone D3) is the CLEAR TO SEND control flop. If clear to send is high at the RS232 level, then the UART transmit clocks are turned on and the unit can transmit at any time. If CTS falls during the time a byte is being transmitted, the ADM-3A will continue to transmit the remainder of that byte then shut down in the "marking" state.

There are four ways that REQUEST-TO-SEND can be controlled in the ADM-3A. First, RTS can be low all of the time which is accompanied by opening all three of the switches located in zone A2. Then RTS can rise before the transmission of a character, stay up during the transmission of that one character, and fall as soon as it clears the UART. This is done by closing the switch marked LOCAL. If the switch labeled 103 is closed, then RTS will be held high all of the time. A device setting on the extension port can also exercise RTS control through Pin 4 of connector J2. The last switch on this section is labeled "202". If this RTS CONTROL switch is closed, then one other selection must be made. The two choices are RTS control utilizing code turn-around and RTS under reverse channel control. This selection is made using switch in zone C4. If code turn is selected, then the actual code to be used must be specified. This is done by closing one of the two switches located on

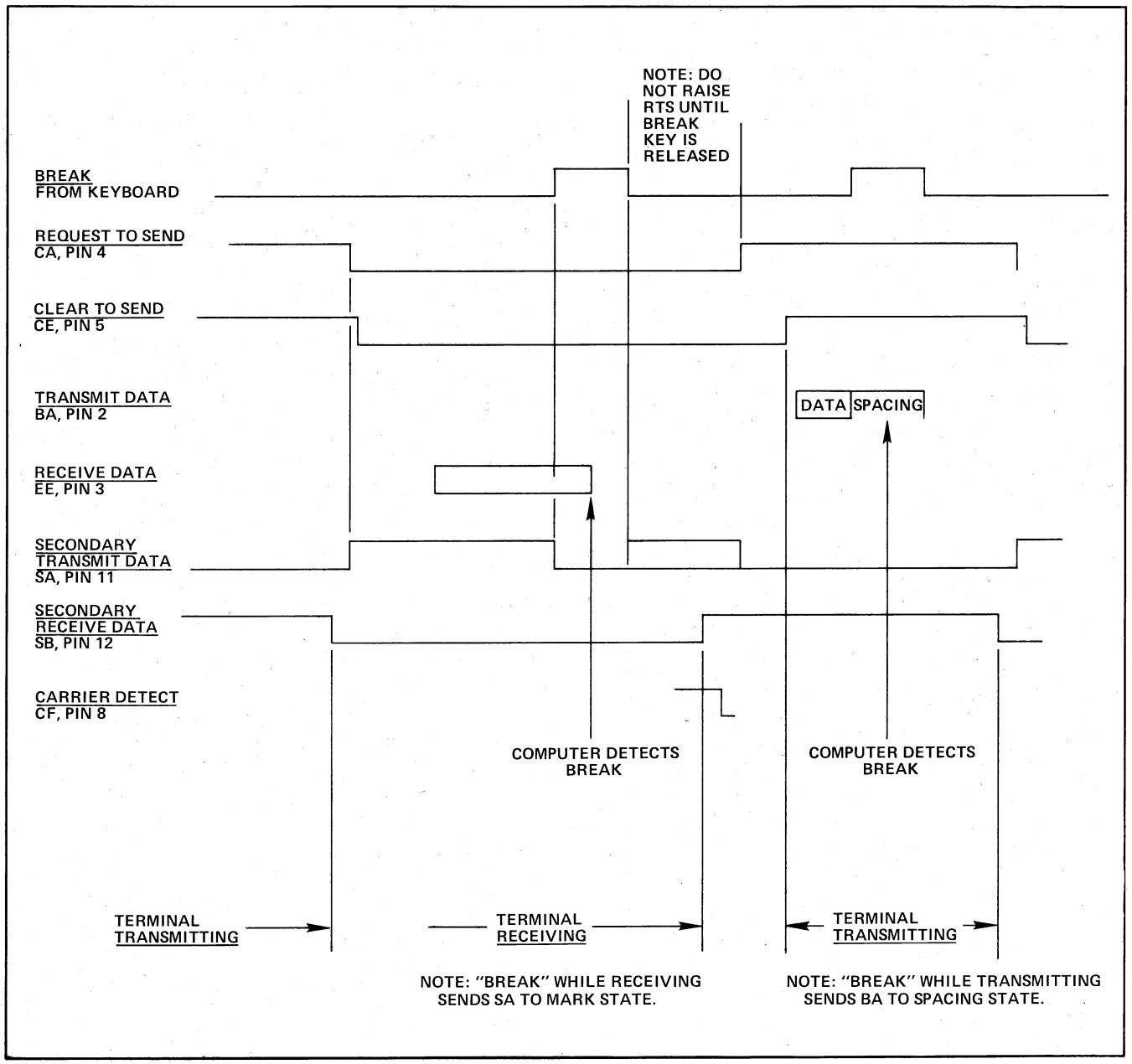


Figure 6-1. Interface Timing for Reverse-Channel Operation

gate input J8-13 (74LS27, zone C4) which are labeled ETX or EOT. These are the only two selections provided for in the ADM-3A. When the selected code is received into the INPUT DATA BUFFER, this information is latched into flop B10-6 (74LS113, zone C3) labeled LATCHED CODE. This information is allowed to toggle flop C8-2 (zone B2) if CARRIER DETECT (zone B4) has gone low, indicating that the distant end has stopped transmission.

If another of the selected codes is then received, the unit will immediately switch to receive without waiting for carrier detect since our RTS was maintaining CARRIER DETECT high.

If reverse channel operation is selected, then the two inputs that control RTS are SECONDARY RECEIVE DATA and CARRIER DETECT (SB and CF respectively). If SP goes low, the ADM-3A will unconditionally switch to the receive mode (RTS low). If CF is also low, SECONDARY TRANSMIT DATA will go low. If CF is high, indicating that the distant end has turned on, SECONDARY TRANSMIT DATA (SA) will go high. This last condition is the normal receive condition in reverse channel operation. In order to switch to the transmit mode, the distant end controlling the terminal raises SECONDARY RECEIVE DATA (SB). Then, the only other condition that has to be met is that CARRIER DETECT (CF) must fall, indicating that the distant end has dropped its RTS. At that time, the ADM-3A will turn RTS on within 62msec. In this reverse channel operation, if a command is given to turn RTS, then no further commands will be recognized for a period of approximately 250msec. This gives the modem time to propagate its signals. This timing is accomplished with the counter and two flops. All controlling inputs and controlled outputs can be driven from the extension port.

6.3 SCHEMATIC SHEET #3 — CLEAR/ERASE LOGIC OFFSET COUNTER ROW COUNTER BEEPER CIRCUIT

6.3.1 CLEAR/ERASE LOGIC

The Clear and Erase Logic (zones D1-D4, A1 & C4) performs the function of initializing the counters on power-up or other clear-screen operations and forcing a write-space action for a sufficient period to clear either a single line, or the entire screen. During power-up the functions CLEAR2 and CLEAR3 force flops F6-5 (START) and F6-10 (ERASEF) true, and flop K8-6 false. The latter function, via gate F2-3, generates the signal CLROC, which clears the Offset and Row Counters.

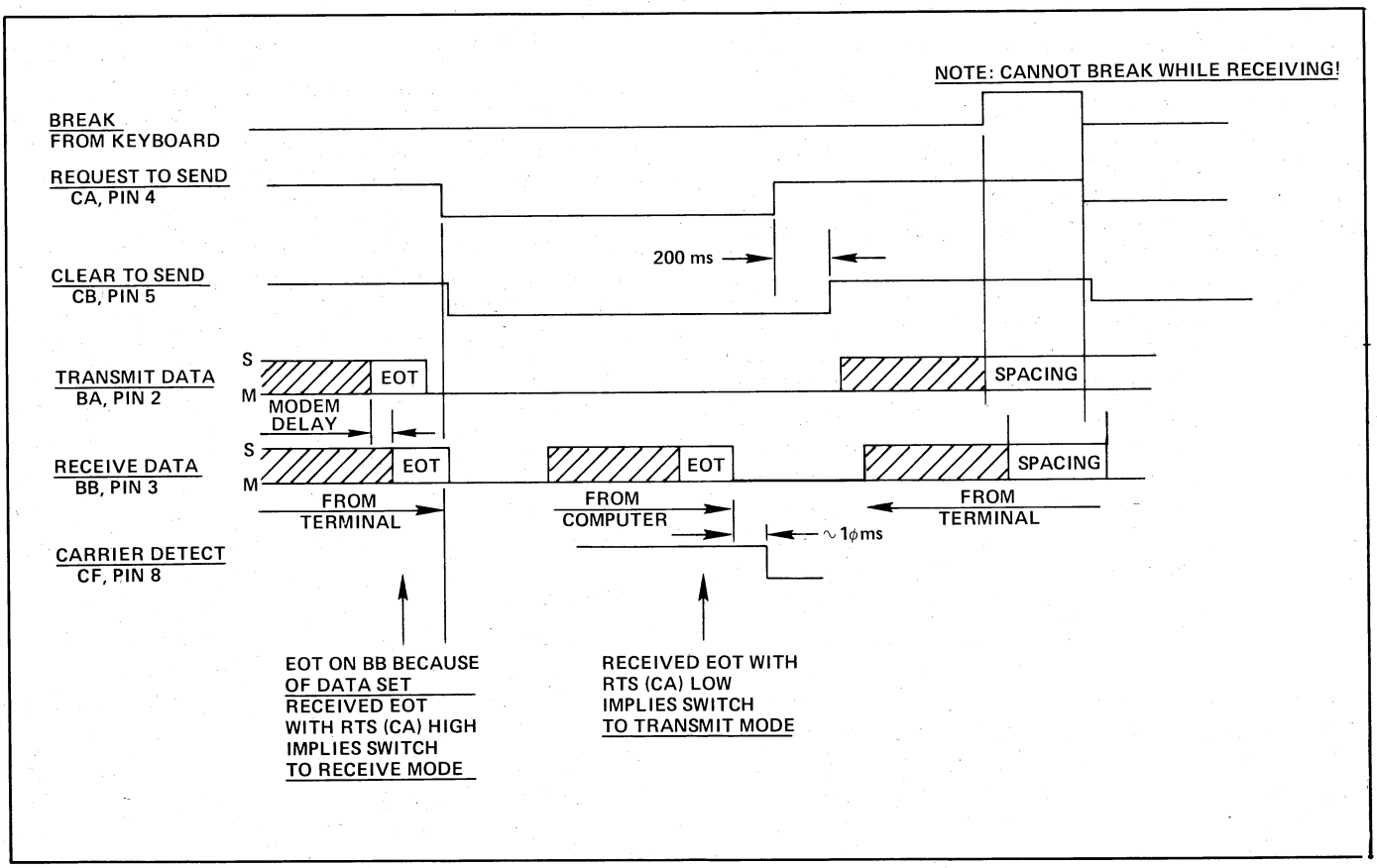


Figure 6-2. Interface Timing for Code Turnaround

If a key-clear (KEY CLR) operation is initiated from the keyboard, or a clear-screen command (CLR SCRN) is received, CLROC is generated directly, but the START and ERASEF flops are set in sequence by successive CC80A signals, the latter flop via the SETERA gate. The remaining erase function, which occurs when a line-feed is generated with the cursor on Row 23, does not affect the START flop. The SETERA signal, derived from CR23 and LF1, causes ERASEF to be set for one line-period. By the time the next CC80A signal occurs, LF1 will be false and START, also being false, will cause ERASEF to be reset. Gated with $\overline{CC7}$ to form $\overline{ERASE\ LINE}$, this function is used to clear the memory-row which was "rolled to the bottom" during a scrolling operation.

Clear-screen operations, however initiated, are terminated when the Offset Counter overflows, generating, OCLOD. The first CC80A signal after OCLOD resets START, and the next CC80A resets ERASEF. This action is necessary in order that memory-row 0 may be cleared.

6.3.2 OFFSET COUNTER

The Offset Conter and its associated logic (zones B1 and C1-C3) perform the dual function of defining the memory-row addresses during clear-screen operations and maintaining the scrolling history of the unit to facilitate the reconciliation of display row-positions to the physical memory-rows. Consisting of five counter stages (OC0- OC4), Row-23 detection logic (OCLOD) and Line-feed definition and vectoring logic (LF1, PGMOD, DNLINEA), the OC will be enabled to react to line-feed directives whenever the unit is currently executing a clear-screen operation. (START TRUE) or the Cursor Row Counter (zones B2, B3) is in count-condition 23_{10}. In either situation, line-feeds derived either from START, LF (line feed command) or BOFLO (overflow from last column of the column-counter) will be translated in the term DNLINEA, which will cause the OC to increment at the next CC80 signal. The OC will increment either one or two units, depending upon the position of the 12/24 Line-Select switch (zone A-3). In 24-line mode, OC0 will toggle at each DNLINEA directive, with a normal binary count propagated to the four upper stages of the counter. In 12-line mode, OC0 is forced true (odd-lines only) and each DNLINEA directive will then increment the upper stages one unit, causing an effective count-by-two operation. Whenever the value held in the OC reaches 23, OCLOD will become true, and the next line-feed will cause the counter to be loaded with a zero-count.

6.3.3 ROW COUNTER

The Cursor Row Counter and its associated logic (zones A1-A4, B1-B4, D3 & D4) perform the task of maintaining the current display-row position of the cursor. Due to the mobility of the cursor, this counter is capable of being incremented, decremented, cleared or loaded with a code from the data-buffer which represents an absolute cursor row-position on the display. Like the Offset Counter, the Row Counter consists of five stages (CR0-CR4) capable of counting in the range 0 to 23; with the same provision for locking the LSB (CR0) into the true condition in 12-line mode, and counting module-2.

The Row Counter is allowed to increment in situations complementary to those for the Offset Counter, that is, when START is false and the row-count is other than 23. In these cases, LF1, derived from the same three possible sources noted for the OC, will be translated into the Row Counter increment signal DNLINEB. One additional source of line-feed enabling is directed to the Row Counter, however, when the Cursor Control switch is open. In this situation, the Row Counter will increment continuously after START falls, until a count of 23 is reached. The counter will then be disabled so long as the switch is open (ENX false) and no further clear-screen operations are initiated. This characteristic of the counter effectively locks the cursor to the bottom row of the display, and directs all subsequent line-feeds to the Offset Counter.

If the Cursor Control switch is closed (ENX true), the upline and Load-Cursor functions will be enabled. The upline command signal, VT, will be invariably routed to the LSB of the Row Counter, as one of three possible clock-enabling terms (VT, $\overline{LDROW}$, DNLINEB). Unless CR0 is locked true by the 12/24 line select switch, it will toggle any time ESC2 is false; a situation which will occur at all times except during cursor-load operations. Decrementing the high-order (CR1-CR4) part of the counter will occur when either CR0 is false or the unit is in 12-line mode (DNSEL), and a VT command is issued.

The Row Counter may be cleared in one of four different situations. The first situation is that caused by one of the three clear-screen operations ($\overline{CLROC}$). The second case is that effected by a HOME command, permitted only when the Cursor Control switch is on. The third circumstance occurs whenever the counter is decremented past zero, in which case BORROW is used as a clock to set ROWCLR (zone D3). The last situation occurs whenever an attempt has been made to load an absolute row-count value greater than 23, causing the term $\overline{R24/31}$ to pull ROWCLR true. The jam-

clear function is removed, either as the result of a DNLINEB (increment) signal, or during the load-row phase of a Load Cursor operation ($\overline{\text{LDROWEN}}$).

The Row Counter may be loaded to any value between zero and 23, provided the Cursor Control switch is on. The actual loading of row-data takes place during the third phase of the four-character sequence, defined by the condition when ESC1 and ESC2 are both true. In this situation, ROWCLR is reset, as described above, and a clocked load signal is directed to the LSB and four MSB's of the row counter ($\overline{\text{LDROW}}$ - $\overline{\text{LDROWEN}}$ - $\overline{\text{XCLK}}$). The information from the data-buffer, DATA1 - DATA5, is then loaded into the counter.

6.3.4 BEEPER CIRCUIT

The circuits which produce an audible tone for operator signaling, are shown in zones C1-C2 & D1-D2, plus related gates at zones A2 & D1 of logic-sheet 4. The duration of the tone is governed by the one-shot (zone C1) which is triggered either by receipt of a BEL code (BEL and CC80) or the occurrence of the LINE END function. The latter function occurs (see logic sheet 4) whenever the Cursor Column counter is advanced from column 71 to column 72. The frequency of the tone (3.6 Khz) is governed by the modulating signal, LC2. The tone is cut off by clearing the one-shot ($\overline{\text{CLRBEL}}$) whenever a READ operation is initiated, or an overflow (OVERFLOW) from the column counter occurs. The first case is necessitated by the fact that BEL is used in conjunction with the Read Back Enable function to initiate the readback operation; therefore, if the tone were not disabled in this situation, excessive noise would result during testing. The second situation is required, to prevent a continuous tone from occurring during high baud-rate transmissions, since at rates higher than 2400 baud, re-triggering by the LINE END function would occur before the one-shot could normally time out.

6-4 SCHEMATIC SHEET #4 COLUMN COUNTER WRITE-PULSE LOGIC

6.4.1 COLUMN COUNTER

The majority of the logic shown on sheet 4 (exclusive of zones D1-D4) is concerned with the task of managing the columnar position of the cursor. As described in the theory of operation, the counter is capable of being incremented, decremented, cleared and loaded with either one of two fixed position-codes or a code derived from data received via the UART and stored in the Data Buffer. Incrementing is effected in one of three ways:

1. As the result of a character-entry into memory.
2. As the result of receiving a Forespace (FF) command.
3. As the result of a start-transmit signal, when in the test-readback mode.

A forespace signal (FORESPACE, zone C1) will be generated for any character received, except Control character (CTRL CHAR), Delete codes (DEL) or characters which follow an Escape code, and constitute either part of the four-character sequence, or an illegal second-character. All possibilities excluded under the last classification are covered by the term $\overline{\text{NOLOAD}}$, derived from $\overline{\text{ESC1}}$ and $\overline{\text{ESC2}}$. Evidence of receipt of a character is provided by the function $\overline{\text{XCLK}}$, which is derived from DOIT and CC80A. The Forespace command (FF) contains an implicit DOIT function, therefore, must only be combined with CC80A to form a properly gated signal (RTCURG) for direct OR-ing. The Readback increment (READ INC) function results from the transmission, rather than reception of a character, and therefore, is a combination of the Read-mode enabling signal ($\overline{\text{READ}}$) and the initiate-transmit term ($\overline{\text{XLOAD}}$). The Column Counter may only be decremented when a Backspace code (BKSP) is received by the unit. This function, containing an implicit DOIT gate, is fed directly to the count-down input of the counter.

The counter is cleared in one of four different situations. The first is occasioned by any of the Clear Screen operations ($\overline{\text{START}}$), insuring that all post-clear action starts from the Home position. Receipt of either a Home command ($\overline{\text{HOME}}$) or Carriage Return (CR) command will also clear the counter, however, the Home function is only recognized when the Cursor Control switch is on. The last situation which will elicit a counter-clear, is a decrement from Column-0. In this situation, the back-count will evoke a borrow ($\overline{\text{WC BORROW}}$) from the counter, which is captured as $\overline{\text{UNDER-FLOW}}$, and used to force the counter back to column zero.

A multiplexor (zones C1-C4) is utilized in the Column Counter logic to control the source of data for loading into the counter. If the counter is incremented past column 79, the event is stored as OVERFLOW, and used to pulse the load-ports of the counter. The OVERFLOW term is also sent to the Offset and Row Counter increment logic, if the Auto-Newline switch is on. The information loaded into the counter by OVERFLOW, is also dependent upon the Auto-Newline switch, zero being loaded if the switch is on, and 79_{10} if it is off. The multiplexor

will always be switched to the A-ports during overflow processing, since the selection term (ESC2) cannot be true simultaneously with an increment (RTCUR) signal.

When a four-character cursor-load operation is initiated, the term ESC2 will be true during both the third and fourth phases, and will switch the Column Counter Mux to the B-ports, enabling translated character-codes (DATA1 - DATA5, $\overline{\text{DATA6}}$ & DATA67) to be loaded during the last phase ($\overline{\text{ESC1}}$, ESC2, XCLK). The translation is required to allow the more common alphanumeric codes to be used, rather than control codes. Row codes in the range 040_8 through 067_8, and column code in the range 040_8 through 157_8 are translated, respectively, to codes in the range 000_8 through 027_8 and 000_8 through 117_8.

6.4.2 WRITE-PULSE LOGIC

Write pulses, which effect the storage into data-memory of the current contents of the Data Buffer, are generated by the logic in zones D1-D4, during two situations. One case is that precipitated by a line-erase operation (see SETERA, sheet-3) due to a clear-screen or scroll situation. In these circumstances, the term $\overline{\text{ERASE LINE}}$ will be generated during one or more complete line-scan periods, allowing 80 write-pulses to be enabled for each such period. In the second situation, a single write-pulse is enabled for each character clocked into the Data Buffer, as evidenced by the FORESPACE signal. The generation of a write-pulse, in this case, is conditioned by the presence of a SPACE code, and the position of the Disable Non-Destructive Space switch. If the switch is closed (disabled) a write-pulse will be enabled for every received character. If the switch is open, all SPACE codes encountered after a Carriage Return will cause inhibition of write-pulses, thereby preventing the entry of such codes into memory. The inhibit function will be cleared by the next Line Feed code.

The duration of the write-pulses is controlled by the write-clock (WRTCLK) flip-flop, which provides a pulse which occupies the last four dot-positions of each character period. The width, therefore, is 367 nanoseconds.

6.5 SCHEMATIC SHEET #5 — MEMORY ADDRESS GENERATION

The logic on this sheet provides four major functions related to the manipulation of the 1920 byte data memory address structure, to facilitate data entry and data retrieval for display refresh. These functions are:

1. Reconciliation of the current cursor row-position with the scroll-history to generate a virtual entry-row address.
2. Reconciliation of the dynamic display row positions with the scroll-history, to virtual refresh-row addresses.
3. Selection of either entry or refresh row-address information in a manner consistent with the periodic demand requirements of the display.
4. Reconciliation of the 64 by 30 byte physical memory array with the 80 by 24 character array used by the display.

The generation of entry-row addresses is performed by a five-bit full adder set comprised of the elements in zones C4 & D2-D4. The adder combines the functions from the Cursor Row Counter (CR0-CR4) and those from the Offset Counter (OC0 - OC4) in the manner:

$$SUMW = CR + OC + 1$$

The unit is added to the counter functions, in order that a unit in bottom-entry mode (cursor control switch off) will initially make access to row-address zero, consistent with the original ADM-3. If the Cursor Control switch is on, the memory-row initially available for data entry ("top row") will be row one. As the display is scrolled, and the Offset Counter incremented, the virtual row-address of each row, relative to the top-of-display will advance proportionately; for example, on a display which has been scrolled five times, with the cursor on the top row, the virtual entry row address will be six (0 + 5 + 1). As the cursor advances down the display, the contribution of the CR register to the sum will also increase. If the unit which was scrolled, as described in the example above, subsequently has its cursor moved to the sixth row of the display, the virtual row address will be 12 (6 + 5 + 1).

The logic shown in zones D2 & D3 (SUM34W, SUM345W, SUM3WSC, SUM3WS, & SUM4WS) is charged with the task of reconciling the row sums from the CR & OC adder, to an allowable address range of 0 to 23. This logic causes sums in the range 24-47 to effectively undergo a "subtract 24" operation.

The generation of refresh-row addresses is also performed by a five-bit adder and two-bit "range adjuster", comprised of the elements in zones A4, B4 and C2 - C3. The second adder-set is functionally identified with the first, combining the contents of the Offset Counter (OC0-OC4) and the Refresh Row Counter (RC0-RC4) to form the sum:

$$SUMR = OC + RC + 1$$

As a consequence of this sum, a unit without scrolling history currently scanning along the top row of the display, will access row-address one, and as the scan progresses down the display, the indicated addresses will progress from 1-23, finally accessing row-address zero when the bottom row of the display is being scanned. As the unit acquires a scroll-history, the virtual addresses will advance, relative to the display rows, with row-addresses previously associated with the top display-row rolled to the bottom and the contents erased, as described earlier. This procedure allows the data in memory to be visually advanced upward, row by row, without necessitating the actual relocation of that data in the physical memory.

In the same manner as that performed on entry-address sums, the row refresh-address sum (SUM0R - SUM5R) is reconciled to a 0-23 range by effectively subtracting 24 from sums in the range 24-47. (SUM34R, SUM345R, SUM3RS and SUM4RS).

The multiplexor-set, located at zones A2, A3, B2, B3, and C1-C3 perform the function of selecting refresh address, during active scan periods, and data-entry addresses during periods of horizontal retrace (C7 true). The complete refresh-address is comprised of SUM0R-SUM2R, SUM3RS, SUM4RS and the refresh column - count functions, CC0-CC6. The complete entry-address is comprised of SUM0W - SUM2W, SUM3WS, SUM4WS and the cursor column-count functions, WC0 - WC6.

The result of the column-count selection is the function-group MA0-MA3, which form the low-order memory address terms directly, and POS4-POS6, which must undergo matrix conversion to derive the mid-range address terms. In addition, the term SEL LINE, which is always false during the data-entry phase, will be true during refresh except during line-erase operations ($\overline{\text{ERASEF}}$). This exception is required, in order that data-entry row-addresses rather than refresh row-address be accessed, thereby allowing 80 space-codes to be written into the virtual memory-row associated with the current cursor position. The SEL LINE function switches the multiplexor in zone C6 to select the high-order row-definers SUM1W, SUM2W, SUM3WS & SUM4WS, or SUM1R, SUM2R, SUM3RS & SUM4RS. The resultant terms LINE1 - LINE4, must be resolved into the physical memory matrix.

The low-order row-definers, SUM0W or SUM0R are selected for the chip-enable functions by the logic in zone D1. Since $\overline{\text{CHIPENA}}$ and $\overline{\text{CHIPENB}}$ point, respectively, to the odd and even rows of both display data and memory data, they are used directly in addressing data-memory, without modification.

Since the display matrix is 80 characters by 24 rows, the largest binary factor which can be used as a "common denominator" for matrix conversion, is 16. Removing this factor, the remaining column factor, 5, is considered as the sum of a four-unit and a one-unit factor. By recombining these factors as products of sums, each column is considered as the sum of a 64-unit increment and a 16-unit increment. If 64 is chosen as one of two coordinates which define a rectangular array, the other coordinate, based on 1920 characters, becomes 30. The visual display, then, is apportioned into the 64x30 memory array as one 64x24 character block and one 64x6 character block, the latter further subdivided into 24 16-character increments. Each row, then, is comprised of the sum of one 64-character slice of the major block, plus one of the minor increments.

Resolution of the display matrix into the memory matrix, is accomplished in the multiplexor (zones A1, B1, & D1) whose outputs are designated MA4 - MA9, by utilizing that fact that whenever columns 64 through 79 are indicated, the term POS6 will be true, and for columns 0 through 63 it will be false. Accordingly, this term will select the "normal" binary column and row definers (POS4, POS5, LINE1 - LINE4) when false, and the 16-character line-increment definers (LINE1 - LINE4, MA8 and MA9 forced true) when true. If the unmodified address - definers, MA0 - MA3 and $\overline{\text{CHIPENA}}$ are included in each array, it can be verified that POS6 false calls up an array of 64 columns by 24 rows, while POS6 true calls up an array of 16 columns by 4 increments by 6 rows, restricted by MA8 & MA9, to rows 24 through 29.

6.6 SCHEMATIC SHEET #6 — DATA RECEIVER CHARACTER DECODERS LOAD-CURSOR SEQUENCE DETECTOR

6.6.1 DATA RECEIVER

All data admitted for interpretation or storage in the ADM-3A is routed initially, as a serial data-stream, into the UART, shown in zones A4, B4 & C4. The source of this data may be from either the Current Loop Receiver circuit ($\overline{\text{CL DATA}}$ From Sheet 10), the RS232 Receive Circuit ($\overline{\text{RECEIVED DATA}}$, Zone D4) or transmitted data ($\overline{\text{XDATA}}$ From Sheet 10). As shown in Zone D4, RS232 data must be level-shifted in the 1489 receiver circuit (A10-3), and transmitted data can only be admitted if the Half-Duplex (FDX/HDX) switch is closed. Routed through the OR-gate (B5-6), the serial data is routed to both the UART and the Extension Port.

If the UART is clear (no overrun from the last character), the serial data will be clocked in at the proper baud-rate (RECV CLK, zone A4), and accumulated in accordance with the format-switch settings shown on sheet 10, zone C4. When a complete character has been accumulated, and is available in parallel (IN1 - IN8), the term DATA RDY (zone A3) will go true. Framing, parity and overrun errors are ignored on the ADM-3A, therefore, the integrity of data rates, duty-cycles and formats must be guaranteed by the source device.

Unless the ADM-3A is currently executing a clear or erase operation ($\overline{\text{ERASEF}}$ low), the Data Ready signal from the UART will be synchronized with the system decoding and writing circuits by timing-signal CC6. The resultant signal (INPUT, zone A3) will strobe the parallel contents of the UART into the Data Buffer (zones B3, C3). The information in the buffer (DATA1 - DATA7, $\overline{\text{DATA1}}$ - $\overline{\text{DATA7}}$) is used directly for entry into memory, or routed to the decoder logic for interpretation of control functions.

6.6.2 CHARACTER DECODERS

The character decoders (zones A1, B1-2, C1-2, D1-2) interpret the received data by analyzing the current 7-bit code in three stages. The first stage examines the three or four high-order bits (DATA4-DATA7), and resolves the character into an ASCII Column or Half-Column position. Columns 0 & 1 are used in most cases, since they define the ASCII Control characters. Additionally, column 3 and the half-columns, 4L and 7H are decoded, to aid in the analysis of "Equal", "Space" and "Delete" codes, respectively.

The second stage (zone B2) fully decodes the low-order three-bits of the character-code, to generate eight row identifiers ($\overline{\text{XX0}}$ - $\overline{\text{XX7}}$), applicable to each of the 16 half-columns in the ASCII matrix. The first stage combines the column or half-column identifier, the row identifier, and where required, DATA4 (or $\overline{\text{DATA4}}$), to provide half-column identification, resulting in a unique character identifier. Eight control characters plus the "displayable" SPACE and DELETE codes are decoded irrespective of the condition of the Cursor Control switch. Four control characters (RS, VT, FF & ESC) and the EQUAL code, however, can only be decoded ($\overline{\text{DATA4A}}$ low), if the Cursor Control switch is on ($\overline{\text{ENX}}$ true).

6.6.3 LOAD-CURSOR SEQUENCE DETECTOR

In order to execute the storage, in the Cursor Row and Column counters, of two bytes of information which represent the absolute position of the cursor, a sequence detector is provided (zones D2-D4) which can:

1. Reset to the occurrence of an ESC code, and hold control until another character is received.
2. Verify the intent to load cursor data, if the second code is "Equals" (=), or abort the sequence if it is not.
3. Maintain control of the terminal until the two additional bytes of Row and Column data are received.
4. Vector the row and column data to the proper destinations.

These tasks are accomplished with a modulo-four counter (ESC1, ESC2), which is normally clear ($\overline{\text{ESC1}}$, $\overline{\text{ESC2}}$). If an ESC character is detected, ESC1 will be set true on the next received-character strobe (XCLK). The ESC code will cause FORESPACE (cursor advance) and data entry into memory to be inhibited. If the next character received is anything but EQUALS, ESC1 will be reset (RSESC1), thereby terminating the sequence. If it is EQUALS, ESC2 will be set true and ESC1 allowed to remain true. In both situations ESC1 true will cause inhibition of FORESPACE. The condition of ESC1 and ESC2 both true will cause the next character received to be interpreted as the Row code, and loaded into the Row Counter. It will also cause ESC1 to be reset on the next strobe. With ESC1 false and ESC2 true, FORESPACE will remain inhibited, and the next received character will be translated and loaded into the Column Counter. At the next strobe, ESC2 will be set false, and the sequence will be complete.

6.7 SCHEMATIC SHEET #7 — CLEAR CIRCUIT READ BACK MONITOR DRIVE SIGNALS CURSOR GENERATION

6.7.1 CLEAR Circuit

The DM74123 (retriggerable one-shot, D1,) located in zone D4 provides the power on clear signal. The RC circuit is connected to the positive trigger input. Therefore, when the power is up and the capacitor finally charges to the input threshold, the one-shot triggers off and creates the reset signal. This unit is unusual in that every single storage element in the system is reset with the CLEAR pulse except for the refresh memories. This was done to accommodate the automatic board testers. The signal labeled $\overline{\text{TESTER INITIALIZE}}$, entering the circuit D2-1 (74LS00, zone C3) accomplishes the same function

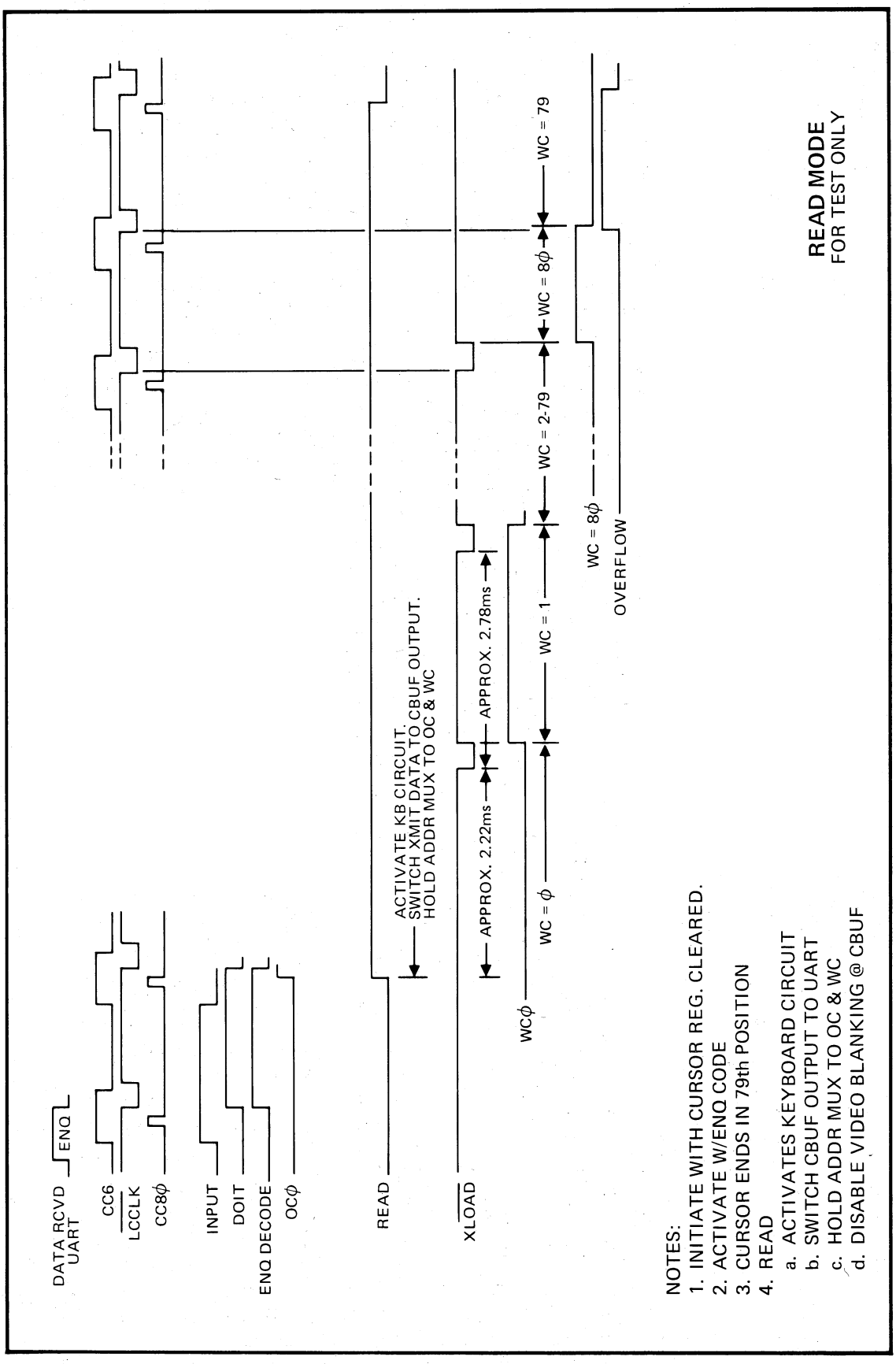


Figure 6-3. Read Mode

as the power on clear except that the signal is generated by the automatic tester. These two clearing sources are combined at D2-3 (74LS00, zone C3) and is called CLEAR. A positive level at this point is the clearing level. This signal is buffered through six inverters to create the negative-going CLEAR signal. Each inverter has only 10 loads and they were used instead of a power buffer because of automatic board tester restrictions.

6.7.2 READ BACK

The flip-flop located in zone C4 (EZ-8, 74LS113) is part of the READ BACK feature. This flop can set only if pin 22 on the main I/O connector J1 is held to ground. READ BACK is a test only feature therefore only internal test cables should have this pin grounded. This function is initiated by issuing a USASCII BEL code (octal 007) through the normal data input which sets this flip-flop. The ADM-3A then responds by sending all data on the top line of the display from the cursor position to the end of the line inclusive. The screen is rolled one line but the data remains on the screen and the bottom line is not erased. The cursor remains on the last character position transmitted which is the last position on the line. The READ flip-flop is cleared at the end of the operation when the CURSOR register overflows.

6.7.3 MONITOR DRIVE Signals

The monitor drive signals, HDRIVE and VDRIVE are generated in zones C1 and D1. The horizontal drive signal, HDRIVE never moves regardless of the position of the 50/60 Hz selection switch. However, the VDRIVE signal changes between 50 Hz and 60 Hz refresh in order to maintain the same relative position of the video display on the display screen. (See the MAIN TIMING DIAGRAM for the positioning of these drive signals.

6.7.4 CURSOR GENERATION

The circuits shown on zones A1-A4, B1-B4 and C1-C2 comprise the cursor generation and control logic. Three comparators are provided to continuously compare the cursor row and column counters with the corresponding display counters and generate a signal when all elements are in coincidence. The stage which compares CR0 - CR4 with RC0 - RC4 will be allowed to propagate its coincidence signal into the next stage, only if the Cursor Control switch is on ($\overline{ENX}$ false). Otherwise, a continuous coincidence signal (ROWCO) is forced to the next stage, since the cursor will always reside below the bottom row. In the event one of the clear-screen operations is under way, $\overline{START}$ will hold ROWCOG low preventing any cursor comparison, thereby blanking the cursor.

When both row and column coincidence occur, a true output will be presented from the last comparator stage (E15-6). This signal is delayed by a pair of flip-flops for two character-periods, to synchronize the cursor with the video data, which is delayed two character periods in the course of accessing and processing. Whenever the Cursor Control switch is off ($\overline{ENX}$ false) CURENA will be true only when the display row-count is greater than 23. This function is clocked by LC1 into the flip-flop E4-6 ($\overline{CURSTOP}$), and combined with its output to form a signal (CUREN) which will be true only during the two line-scan periods immediately below the last row of data on the display.

If the Cursor Control switch is on, CUREN will be forced true continuously, allowing all coincidence signals to be propagated through the delay flip-flops. Coincidence will never occur outside the bounds of the data-display, since the cursor row and column counters are restricted to that area. The output of the delay flip-flops (CURSOR) will be mixed with video data in an exclusive -OR gate, if Cursor Control is on, resulting in a reverse image of the character over which the cursor resides. If Cursor Control is off (see sheet 8, zone A1), the double-underscore cursor signal will be admitted to the video driver in parallel with the non-inverted video signals (FLIP).

6.8 SCHEMATIC SHEET #8 — REFRESH MEMORY CHARACTER GENERATORS VIDEO SERIALIZER TRANSMIT DATA MULTIPLEXERS

6.8.1 Refresh Memory

The refresh memory is composed of 14 - 2101 RAMs which have 500 nsec access times. These RAMs are organized as a 2K by 7-bit memory which hold the 1920 USASCII codes for screen refresh. There are four configurations of memory in the ADM-3A. The first configuration is six RAMs which is used for the upper case only, 12 line display. Then seven RAMs are used for the upper/lower case, 12 line version. Twelve RAMs are required if upper case only, 24 lines. Then all 14 rams are installed if the fully configured upper/lower case, 24-line combination is desired.

The selection between 12 and 24 lines is made with a switch. (See sheet 3 zone A3.) Zone A4 of this schematic has a switch labeled $\overline{UC\ EN}$ which switches the unit from upper case only to upper/lower case display. The 74LS157 sections located in zones C4 and C3 (2:1 Mux, H7) alter the data properly for 7 bit USASCII to 6 bit USASCII for upper case only display. The output K12-12

(zone C4) selects between two sources for bit 6 storage. Upper case only display utilizes DATA7 while upper/lower cases uses DATA6. Gate H7-8 simply forces bit 6 to a high level when the ADM-3A is erasing a line. This converts the NULL code coming in to a proper SPACE code. The 74LS86 in zone C4(k9-3) has the function of being able to clear the memory to zeros with the activation of a switch located internally.

6.8.2 Character Generators

The circuitry located above the refresh memory is used to blank the video display at selected times. This function is normally accomplished at the video serializer but was placed here to allow the automatic board tester to shut the video off without affecting the character generators or the video serializer.

The horizontal blanking is accomplished with gate C5-4 (zone D4, 74LS02). The term RC5, entering the circuit at C5-2 does the blanking for row counts 32 and higher. This signal is active only if the unit is operating at 50 Hz since the 60 Hz units reach a maximum count of 29. The term RC=24/31 accounts for the blanking immediately below the video and up to row count 31. Gate D4-3 (74LS02, zone D4) generates the term that blanks every other line if the ADM-3A is operating in the 12 line mode. The combined blanking term, called $\overline{\text{VIDEO BLANK}}$ and going to the clear inputs of the two 74LS175's (K13 and L13, zones B3 and C3) used as the character generator input buffers, is generated in the flop K8 (74LS74,zone D3). Notice that clearing the CBUF registers does not present a NULL code to the character generator inputs. The outputs associated with bit 6 are inverted. Therefore, when $\overline{\text{VIDEO BLANK}}$ is active, the CBUF outputs present a USASCII SPACE code to the character generators.

The two character generator ROMs are rather straightforward. The upper case ROM is a standard masked part (2513) but the lower case ROM is a custom masked part. The one unusual thing about this is that all of the address lines into the lower case character generator are inverted.

6.8.3 Video Serializer

The video serializer used is a 74166, eight bit shift register which is preset once every 643 nsec and shifted at an input clock rate of 10.8864 MHz. Gate K16-5 (74LS00, zone A1) is used to blank the video during a READ BACK operation. This is required because the CBUF registers are used to send memory data to the transmit UART without regard to its effect on the video display. Since the result is quite unusual, this gate was installed. Gate J9 (74LS00, zone A1) is used as the video driver.

6.8.4 Transmit Data Multiplexers

The two multiplexers (74LS157, K6 and L6, zones D1 and D2) are used to select between keyboard or refresh memory as the source of the data going to the transmit UART. The refresh memory is selected during the READ BACK operation and the keyboard output is selected at all other times.

6.9 SCHEMATIC SHEET 9 — KEYBOARD CIRCUIT

The keyboard is encoded utilizing a normal scanning-type circuit. The two counters (74LS293) located in zones D3 and D4 clock through all possible 128 USASCII codes. The four least significant bits are decoded through the 1 of 16 decoders (74LS154-L8) whose outputs appear as one side of the encoding matrix. The three most significant bits, K5 through K7, operate the selection inputs of the 8 to 1 multiplexer (74LS151-L9). The inputs of this multiplexer represent the second side of the encoding matrix. This encoding matrix has a direct relationship with the USASCII code chart. The outputs of the decoder represent the rows of the chart while the inputs of the multiplexer represent the columns. The key switches are then placed selectively within this matrix on the intersection that generates the lower case code associated with that particular switch.

The detection of a switch closure occurs in the following manner. When none of the keys are depressed (all switches open), the output of the multiplexer L9 is high and the clock (KBCLK) to the code generating counters is running. While KEY DATA is high, the signal labeled GO (zone C1) will be held low, which clears the shift register F1 (zone C2) and holds flop E2 (zone D1) in the key debouncing state. This is the normal idling state with the counters cycling, $\overline{\text{KEYDATA}}$ high, shift register F1 cleared, and BOUNCE low. When an encoded key is depressed, the counters continue cycling until the selected ROW and COL are simultaneously enabled. At this time the low level signal from the row decoder is propagated through the key switch, through the multiplexer, to gate E7 (zone B2) which effectively shuts off the clock to the code generating counters. When $\overline{\text{KEY DATA}}$ goes low, the signal labeled GO is enabled, thereby releasing the shift register and the Bounce flop. At this time the signal BOUNCE is low which enables every cycle of the clock RC0 to propagate through gate E3, located in zone D2, to the clock input of the shift register. This clock (900 Hz) determines the length of time allowed for the mechanical key switch to stop bouncing. It allows five cycles of this clock to pass before the decision is made that the code is

stable. At the end of these five cycles, the signal BOUNCE goes high which does two things. First, the clock input to the shift register is disabled through gate D2 at zone D2. Secondly, the SHIFT/LD line to the shift register is taken to the loading state by gate F5 in zone D2. The circuit is now waiting for one of two things to happen; the character key being released or the REPT key being depressed. In the event that the key is released, $\overline{\text{KEY DATA}}$ will immediately go high and the entire circuit will revert to the idling state. If the REPT key is depressed without releasing the first key, the SHIFT/LD line goes to the shift state because of F5-2 (zone D2). Notice now that when $\overline{\text{BOUNCE}}$ went high at the end of the first shift register cycle, the term $\overline{\text{RCRESET}}$ was allowed to gate the clock RC0 effectively cutting its rate to 60 Hz to 50 Hz depending on the position of the 50/60 Hz selection switch. This new clock rate will now determine the repeat rate from the keyboard. The shift register will now shift at the lower rate, generating a load pulse every time DOUT goes high and continuing until the REPT key is released or the primary key is released. The repeat rate is 12.5 char/sec at 60 Hz and 10 char/sec at 50 Hz. The term THRE into gate H5-5 (zone D2) is there to slow the repeat rate if the baud rate selected has a character time longer than the period of the repeat cycle. The terms READ and $\overline{\text{READ}}$ in this circuit are activated by the read-back circuit which is used for internal LSI testing only. In normal operation, the ADM-3A memory cannot be read by the computer. When the read-back is activated, the keyboard control circuit is fooled into thinking that it is repeating a code. The one difference is that the circuit now repeats utilizing the debouncing clock and not the slower clock. The data lines are naturally switched to the memory output which occurs on schematic sheet 8.

There are three methods by which the code normally generated by the scanning circuit can be altered. First, the depression of the CTRL key (zone A2) unconditionally drives bits 6 and 7 to the low state. This means that the code generated will be driven to columns 0 or 1 depending on the state of bit 5. This is the means by which control codes, not on individual keys, are generated. The next way that the code can be altered is by inverting bit 5. This is used to create the shifted (upper case) codes in USASCII columns 2 and 3. Gate K10 (74LS00) in zone A4 identifies the code generated as a column 2 or 3 code. Row 0 is eliminated from this shifting because the SPACE code and the ZERO code are not affected by the shift key. This is done at L10-9 (zone A3). The last way to alter the code is by inverting bit 6. This is used to shift from the lower case alpha codes in column 6 and 7 to the upper case codes in columns 4 and 5. There are two ways to effect this bit 6 inversion. The normal shift keys and the UPPER CASE ALPHA switch.

The UPPER CASE ALPHA switch is used on systems where no lower case alpha codes are tolerated. Therefore, while in this mode, the normal SHIFT keys have no effect on the alpha keys. Upper case alpha is always generated. This is accomplished at gate L10 (zone A3). L10-2 and L10-1 decode the fact that the code originates in columns 6 or 7. Notice that in the matrix above, the only codes in columns 6 or 7 are the twenty-six lower case alpha codes. The six remaining non-alpha codes are placed in columns 4 and 5. Therefore, the KC6 KC7 decode in gate L10 definitely picks out only the lower case alpha codes. The normal SHIFT function for columns 4 through 7 is accomplished in gate K10 (zone B4). If KC7 is set, identifying it as columns 4 through 7, and the SHIFT key is depressed, bit 6 is unconditionally inverted.

The CLEAR key, located in zone A2, is utilized in conjunction with the SHIFT key to clear the refresh memory, clear the KEYBOARD LOCK circuit, and clear the I/O interface circuitry. This combination is done in gate L12 located in zone A1.

The BREAK key (zone B3) is used to signal the computer that I/O termination is desired. When depressed, this key has one of two effects, depending on whether the unit is in the transmit or receive mode. If the unit is transmitting when the BREAK is activated, the primary transmit data line (BA, pin 2) is driven to the "spacing" state for as long as the key is depressed. If the unit is receiving data and is in the 202, reverse channel mode, the SECONDARY TRANSMIT DATA line (SA, pin 11) is driven to the "marking" state.

The last function on this sheet is the HERE IS circuit. If the ADM-3A has this option installed, the depression of this key initiates the transmission of a unique message to the computer. This message is contained in PROM in the option and can be up to 32 characters long. This transmission can also be activated with the receipt of an ENQ code from the computer. An ENQ code generated at the local keyboard will not be recognized because of the lockout circuit in zones A1 and A3. Locally generated characters will cause the flip-flop (KSDLY) to be set at the time the character is transmitted ($\overline{\text{XLOAD}}$). The output $\overline{\text{KSDLY}}$ will be false until either a remote character is received, or the local character is acknowledged in half-duplex. At this time $\overline{\text{DOIT}}$ will reset the flop. The term $\overline{\text{KSDLY}}$, in conjunction with the Enquiry-code (ENQ) will prevent a locally-generated ENQ from being recognized.

6.10 SCHEMATIC SHEET #10 — DATA TRANSMITTER CONTROL SECTION OF UART CURRENT LOOP XMTR/RCVR KEYBOARD LOCK CIRCUIT

6.10.1 Data Transmitter

The transmitter and control sections of the UART are shown on this schematic. Indicated on UART pins 26 through 32 are the seven bits which comprise the USASCII code. XDATA7 is the most significant bit and XDATA1 the least significant. This code to be transmitted to the line comes from one of three sources. In normal operation, the keyboard circuit and the ANSWER BACK option can generate the code. However, during testing the contents of the memory are sent through the UART during READ-BACK. Pin 40 of the UART is the transmitter clock input. The source of this clock comes from sheet 11 where it is controlled by CLEAR TO SEND (sheet 12, zone D3). If there is no CTS, this input will remain high. In normal operation, the clock on this line will be the same as receive clock input. The frequency will be 16 times the desired transmit baud rate. However, with the split clock option, the transmit and receive rates can be different. The receive rate is always controlled by the main baud rate switches under the cover, while with the split speed option, the little rotary switch in front of the keyboard controls the transmit rate. This rotary switch is accessible only when the unit is open. All baud rates are available on this switch except for 1800 baud. With the split speed option, the selection of 1800 baud as the receive rate limits the selection of the transmit rate to 110 baud. No other baud rates are legal.

Pin 23 on the UART is the loading signal for the transmitter section. The normal state of this line is high and it only goes low when serial tranmission of the data present on the XDATA input pins 26 through 32 is desired. The two sources of this loading signal are the keyboard circuit and the ANSWER BACK option board.

Two control signals are utilized from the transmitter section. These are TRANSMITTER HOLDING REGISTER EMPTY (THRE) and TRANSMIT REGISTER EMPTY (TRE). The UART utilized in this unit is buffered on the transmitter data input lines and therefore, when the loading signal is given on pin 23, the XDATA lines are transferred to a buffer register instead of directly to the serializer. When this buffer, called the TRANSMITTER HOLDING REGISTER is loaded, the signal THRE (zone A3) goes low. The transfer of the data from this buffer to the serializer is contingent on the transmitter clocks being present (CTS high) and the serializer being empty. If the serializer is empty, the signal TRE (zone B3) is high. If both conditions are present, the buffer data will be automatically transferred to the serializer on the next clock. At this time, TRE will go low to indicate that the serializer is being used. When both signals are high, the transmitter section is completely empty. These two UART signals are combined to create the "bouncing" REQUEST TO SEND signal selectable on the interface. When either of these signals, THRE or TRE, is low it will cause RTS to be high. Therefore, the RTS signal will "surround" the transmitted character.

The last signal out of the UART transmitter section, is naturally, the serial data. This line marks in the high state and the indication of character starting is this line going low for the start bit of the character. The data bits in the following byte are then sent in a serial manner with the least significant bit first, through data bit 7, followed by the parity bit (if enabled) and the one or two stop bits. The data at this point is "true" data, that is a "one" is indicated by a high level and a "zero" by a low level. This data is then sent through gate C6 (zone A3). C6-4 accepts the signal from the BREAK key shown on drawing 9, zone B3. The depression of this key takes the transmit data line to the spacing (high) state. Input C6-3 accepts data generated by the device connected to the extension port and received by the 1489 EIA receiver A6 (zone A4). This combined data signal (C6-6, 74SL10, zone A3) is then sent to both the EIA and CURRENT LOOP transmitters. The selection of the transmitter to be used is governed by the switch schematically represented in zone C3 and labeled RS232/CL. This switch is physically located under the little plate next to the keyboard. When the switch is positioned to the left (closed), the EIA transmitter is selected. When one transmitter is selected, the unused transmitter will maintain a marking output to the outside world. Therefore, the RS232/CL switch can be used for "local" operation where data is desired out the extension port but not out of the main I/O port. The transmitted EIA data is level shifted through the 1488 A9 located in zone A1 and out to the EIA connector, pin 2.

6.10.2 Control Section of UART

The control section of the UART is also shown on schematic #10. The MASTER CLEAR is driven high when the UART is to be cleared (pin 21). There are five characteristics of the transmitted data that can be selected by the toggle switches under the panel. First is the STOP BIT SELECT input on pin 36. When this line is held low, one stop bit will be attached to the transmitted byte while a high signal will select two stop bits. The next input controls the WORD LENGTH SELECT. A high input selects an 8 bit data word while a low level selects a 7 bit

data word. UART pin 39 is EVEN PARITY ENABLE which it would do if this pin is allowed to go high. Odd parity is selected by moving the switch to the left and driving this input low. PARITY INHIBIT is located on UART pin 35. Parity generation is inhibited if the switch is to the right and the input is high. If this input is low then the UART control will read the parity selection input (pin 39). If this input is high, then pin 39 is ignored. The last control input is pin 33, BIT 8 CONTROL. This input is active only if the ORD LENGTH SELECT input (pin 38) is high and an 8 bit word is selected. This control input is then used to choose a "mark" or a "space" in the eighth data bit position.

6.10.3 Current Loop XMTR/RCVR

The last item on this sheet is the CURRENT LOOP transmitter/receiver combination. The current loop differs from the circuits in the ADM-1A and 2 primarily because it is bipolar. That is, current direction is immaterial. The transmitter and receiver can run completely isolated from the ADM-3A which is its normal operating mode. However, provision has been made inside the unit to tie one leg of the transmitter or receiver to +12 volts through a resistor to create a current source. As an alternative, a ground strap can be installed, in place of the resistor, to act as a current sink in the case of a positive external voltage source or as a current source in the event an external negative sink is provided. The CURRENT LOOP circuits operate over a range of 16 to 24ma, at a peak supply voltage of 20 VDC.

6.10.4 Keyboard Logic

The signals labeled LOCK and UNLOCK are used to control the KEYBOARD LOCK flip-flop located in zone D1 of this sheet. The code used to unlock the keyboard is a USASCII SO (octal 016) and the code used to lock is a USASCII SI (octal 017). The CLEAR SCREEN function is activated by USASCII SUB (octal 032). The SPACE decode is created in H2-4 (7402, zone A1) to recognize this code for the nondestructive cursor feature. The USASCII ENQ is used to activate the ANSWER BACK option (if installed). This decode is combined with the depression of the HERE IS key on the keyboard schematic (sheet #8).

The flip-flop located in zone D1 is used to control the locking and unlocking of the keyboard circuit. Notice that there is a switch in the LOCK input to disable this feature if the particular application dictates that the USASCII SI code be used for other purposes. There are two ways to unlock a previously locked keyboard. The first is the receipt of the USASCII SO code. The keyboard can also be unlocked by the simultaneous depression of the SHIFT and CLEAR keys which generate the signal named KEY CLR.

6.11 SCHEMATIC SHEET #11 — BAUD RATE GENERATION

This schematic comprises the counters and associated logic, required for the generation of transmit and receive clocking functions for the UART. For a given BAUD-rate at the interface and to the terminal, the UART must be supplied with a clock-train 16 times the frequency of the I/O serial pulse-train. For the highest available BAUD-rate (19,200), this requires a UART clock-rate of 307.2 Khz. For the lowest (75 baud) rate, the UART must be supplied with a 1.2 Khz clock. To accomplish the required frequency division, three counters are provided (zones D1 - D4) which use as their primary input, the DC1 function from the dot-counter, which has a cyclic rate of 3.1104 Mhz. The three counters normally divide this signal, progressively by 5, 16 and 16. Accordingly, the output from the third stage of the first counter (CLK1, zone D3) will represent a division by 5, and have a cyclic rate of 622.08 Khz; approximately double the required UART clock rate for 19,200 baud. If the 19200 baud switch (zone B2) is closed, this signal (DOUBLE CLK) is routed to the Receive Clock (RECV CLK) Flip-flop, where is it divided by two, to provide a clock-rate of 311 Khz. This signal is approximately 1.2% higher than the ideal rate, but well within the accuracy requirements of contemporary communications links. Unless the etch-link is cut, to enable split baud rates, the same signal selected for the Receive Clock, is also sent to the Transmit Clock (XMIT CLK) flip-flop, for division by two.

Since most of the common baud-rates used with the ADM-3A are sub-multiples of 19200 baud, they are derived by progressively dividing the 622 Khz signal by 256 in the two remaining counters. The only rates which cannot be derived in this manner are 1800 baud and 110 baud. The former is generated by causing the first counter to divide by 6 instead of 5, and the second to divide by 9 rather than 16. The resultant division by 54 will provide a signal at the fourth stage (CLK5) of the second counter, with a cyclic-rate of 57.6 Khz, which is exactly the required double-clock frequency.

If a baud-rate of 110 is desired, the counters are forced to divide by 5, 16 and 11 for a combined division of 880. The resultant signal at the fourth stage (CLK9) of the final counter will have a cyclic rate of 3.534 Khz, which is 0.4% higher than the ideal double-clock frequency of 3.52 Khz.

In the event split baud rates are desired, the etch-link shown at zone B1 must be cut, and a rotary baud-rate switch (zone A2) must be installed. Due to the nature of non-standard division-string, the split-baud rate features cannot be used when either 110 or 1800 baud are selected.

SECTION 7
PARTS LIST

Included in this section are lists of both the major components as provided by Lear Siegler and the general parts which are a part of the major components.

ADM-3A REPLACEABLE PARTS INFORMATION

Spare parts and renewal parts for the ADM-3A are available from Lear Siegler Electronic Instrumentation Division. When ordering parts, include the following information.

1. ADM-3A Serial Number
2. Part Description
3. LSI or Manufacturer's Part Number

Routine parts orders may be mailed to:

Lear Siegler, Inc.,
Electronic Instrumentation Division
Data Products Customer Service
714 North Brookhurst Street
Anaheim, California 92803

Emergency parts orders may be placed by telephoning:

Data Products Customer Service
Telephone (714) 774-1010

or by teletype to:

TELEX 655444
TWX 910-591-1157

ADM-3A ASSEMBLY PARTS LIST 129450

LSI Part Number	Description
129450	ADM-3A Final Assembly
128214	Label, High Voltage
128565-23	Wire Assy, 15" Yellow
129452-3	Housing, Top
129452-5	Housing, Bottom
129453-3	Logo, ADM-3A
129454-3	Bracket, CRT Mount
129455-3	Cord, Power 115VAC
129455-5	Cord, Power 230VAC
129456-3	Nameplate (115V)
129456-5	Nameplate (230V)
129457-3	Legend, Switch
129458-3	Transformer, 115V
129458-5	Transformer, 230V
129459-10	Wire, 10.5"
129459-23	Wire, 23" Green
129470-11	Board Assy, ADM-3A
129479-1	Monitor, P4 Etch
128481-11	Cable, 18"
129482-3	Bracket, CRT Board Mount
129483-3	Clip, Retainer Bracket
129484-3	Screen
129485-3	Plate, Baffle
129486-3	Spacer
129487-1	Speaker
129494-3	Support, CRT
804011	Switch, TGC0411-TW-B
807001	O Ring, 214-060307-00-2303
809015	Connector, 03-09-1033
809023	Contact Amp 350418-1
821001	Screw, 10-32x7/16 Sems
821002	Screw, 10-32x3/4 Ph
821402	Screw, 4-40x3/16 Ph
821403	Screw, 4-20x5/16 Plastite
822001	Nut, 10-32 8041-NP Brass
823001	Washer 10
824001	Rivet, Pop AD66ABSLF
830001	Strain Relief, Heyco SR6N3-4
830002	Fastener, ABMM-AC
830003	Fastener, Cadle Panduit PLTIM-M
835002	Lug, RA873
839014	Sleeving, Shrink Fit 221x3/4
840001	Fuse, 313.80, 8 Amp Sloblo
840002	Holder, Fuse 342038L
129459-9	Wire, Ground

ORDERING PARTS

Most parts contained in the monitor are available commercially from electronic parts outlets. When it is necessary to order spare or replacement parts from BBRC, Miratel Division, include the part description, part number, model and serial number data of the monitor as listed on the serial number plate and, if applicable, the schematic reference number listed in the parts list. Orders for these parts should be sent to:

Ball Brothers Research Corporation
Miratel Division
1633 Terrace Drive
Roseville, Minnesota 55113

For rapid service:

Telephone area (612) 633-1742
or
Teletype area (910) 563-3552

RETURNING PARTS

When the monitor requires service or repair in accordance with the enclosed warranty, return the unit or part to:

Ball Brothers Research Corporation
Miratel Division
1633 Terrace Drive
Roseville, Minnesota 55113
Attn: Customer Service
Telephone area (612) 633-1742
Teletype area (910) 563-3552

Unnecessary delays may be avoided when parts are returned to Miratel Division using the following procedures:

1. Package the unit or part in accordance with the method of shipment. Enclose a list of the material being returned and the reason for returning it.

2. Send the unit or part, transportation prepaid, to the address stipulated for returning parts.

All equipment and parts described in the warranty will be replaced, provided Miratel's examination discloses that the defects are within the limits of the warranty. If damages or defects are not within the limits of the warranty, the customer will be notified of the extent of repairs required and the cost. The unit will be repaired and returned upon agreement.

MONITOR PARTS LIST

Symbol	Description	Mfg.	Mfg. Part Number	BBRC Part Number
	Capacitor, Fixed; uF Unless Otherwise Stated			
C1	3300; 60V, Electrolytic	BBRC		1-012-2156
C101	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C102	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C103	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C104	0.001 + 10%; 1000V, Ceramic Disc	ERIE	Type 801	1-012-0540
C105	0.47 + 10%, 100V. Mylar	PAK	MF830	1-012-1005
C106	0.47 + 10%; 100V Mylar	PAK	MF830	1-012-1005
C107	500; 6V, Electrolytic	BBRC		1-012-2158
C108	100; 6V, Electrolytic	BBRC		1-012-2160
C109	0.022 + 10%, 400V, Mylar	SPRA	Type 225P	1-012-0800
C110	.1 + 10%; 200V, Mylar	PAK	MF580	1-012-0870
C111	0.02 + 20%; 1000V, Ceramic Disc	ERIE	Type 841	1-012-0780
C112	50; 50V, Electrolytic	BBRC		1-012-2157
C113	10 + 10%, 63V, Mylar	BBRC		1-012-1130
C114	200; 25V, Electrolytic	BBRC		1-012-2159
C115	50; 25V, Electrolytic	BBRC		1-012-2165
C116	20; 150V, Electrolytic	BBRC		1-012-1260
C117	6uf; 25V, Electrolytic	SPRA	TE1203	1-012-2066
C118	820pf + 5%; 500V, Dipped Mica	ARCO	Type DM	1-012-0482
C119	25; 50V, Electrolytic	BBRC		1-012-2193
C120	.01 + 20%; 1000V; Ceramic Disc	ERIE	Type 811	1-012-0740
C201	50; 50V, Electrolytic	BBRC		1-012-2157
C202	0.01 + 20%; 1000V; Ceramic Disc	ERIE	Type 841	1-012-0780
C203	50; 50V, Electrolytic	BBRC		1-012-2157
CR1	VS148, Bridge Rectifier	VARO	VS148	1-021-0413
CR2	H510, High Voltage Rectifier	VARO	H510	1-021-0424
CR101	1N3605	SYL	1N3605	1-021-0410
CR102	1N3605	SYL	1N3605	1-021-0410
CR103	1N4785	RCA	1N4785	1-021-0360
CR104	1N3279	DI	1N3279	1-021-0380
CR105	1N3279	DI	1N3279	1-021-0380
CR106	1N3279	DI	1N3279	1-021-0380
CR107	1N3279	DI	1N3279	1-021-0380
CR108	1N3605	SYL	1N3605	1-021-0410
F1	Fuse, 0.6A-250V, ¼x1¼, Slo-Blo	LF	Type AGC	1-028-0244
or	Fuse, 0.6A-250V, 9/32x1¼, Slo-Blo (TV-B12)	BUSS	Type MDM	1-028-0245
F101	Fuse, 2A-125V, Picofuse	LF	276002	1-028-0247
L1	Vertical Choke	BBRC		6-003-0321
L101	Coil, Width	BBRC		1-016-0303
	TRANSISTOR			
Q1	2N3055	RCA	2n3055	1-015-1134
Q101	2N5830	MOT	2N5830	1-015-1172
Q102	D13T1	GE	D13T1	1-015-1157
	Resistor, Film: ½W + 5% Unless Otherwise Stated			
R133	4.7K; ¼W			70-16-0472
R134	Not Used			
R135	22K			70-16-0223

MONITOR PARTS LIST (Continued)

Symbol	Description	Mfg.	Mfg. Part Number	BBRC Part Number
R136	22K			70-16-0223
R137	33K; 1W Composition			1-001-2448
R201	1K			1-011-2270
R202	1K			1-011-2270
R203	10K			1-011-2294
R204	0.68 + 10%; 2W, Wirewound	IRC	Type BHW	1-011-2217
R205	1.5K			1-011-2274
R206	470			1-011-2262
R207	470			1-011-2262
R208	Var; 500 + 20%; 1/5W, Composition	CTS	Type 201	1-011-5604
R209	470			1-011-2262
	TRANSFORMER			
T1	Power	BBRC		1-017-5390
T2	High Voltage (TV-12C, TV-12, & TV-E12)	BBRC		6-003-0320
or	High Voltage (TV-B12, TV-TC12, & TV-C12)	BBRC		6-003-0325
or	High Voltage (TV-T12)	BBRC		6-003-0326
or	High Voltage (TV-D12)	BBRC		6-003-0333
T101	Horizontal Driver	BBRC		1-017-5338
VR101	1N758	T1	1N758	1-021-0180
VR102	VR56	ST	VR56	1-021-0420
	MISCELLANEOUS			
	Socket, CRT (TV12)	BBRC		1-022-0427
	Fuseholder, Extractor Post, Fuse Size: ¼x1¼	LF	342012	1-028-0210
	Fuseholder, Extractor Post, Fuse Size: 9/32x1¼ (TV-B12 Only)	BUSS	Type HCM	1-028-0246
	Low Voltage Circuit Board Assembly	BBRC		6-003-0459
	Main Chassis Circuit Board Assembly	BBRC		6-003-0500
	Main Chassis Circuit Board Assembly (TV-T12)	BBRC		6-002-0476
	Main Chassis Circuit Board Assembly (TV-TC12)	BBRC		6-002-0502
	Main Chassis Circuit Board Assembly (TV-C12)	BBRC		6-002-0504
	Main Chassis Circuit Board Assembly (TV12, Tektronics)	BBRC		6-002-0506
	Cable Assembly; 8 Inch	BBRC		
	Cable Assembly; 5 Inch	BBRC		6-004-0631
	Power Supply Module (TV-12, 120VAC)	BBRC		6-003-0371
	Power Supply Module (TV-12, 220VAC)	BBRC		6-003-0372
	Power Supply Module (TV-B12, 120VAC)	BBRC		6-003-0368
	Power Supply Module (TV-B12, 220VAC)	BBRC		6-002-0370
	Deflection Coil Assembly	BBRC		6-004-0314
	Deflection Coil Assembly (TV-B12)	BBRC		6-004-0321
V1	CRT, 12 Inch, P4 Phosphor	BBRC		1-014-0737
	Power Cable Assembly, 120VAC	BBRC		6-003-0645
	Power Cable Assembly, 200VAC	BBRC		6-003-0652

MONITOR VENDOR CODES AND LOCATIONS

Code	Manufacturer	Location
BBRC	Ball Brothers Research Corporation, Miratel Division	Roseville, Minnesota
BUSS	Bussman Manufacturing	St. Louis, Missouri
CRL	Centralab	Milwaukee, Wisconsin
CTS	CTS Corporation	Elkhart, Indiana
DI	Diode, Inc.	Chatsworth, California
ERIE	Erie Technological Products, Inc.	Erie, Pennsylvania
GE	General Electric	Syracuse, New York
IRC	IRC Corporation	Philadelphia, Pennsylvania
LF	Littelfuse Company, Inc.	Des Plaines, Illinois
MALL	P. R. Mallory Company, Inc.	Indianapolis, Indiana
MOT	Motorola Semiconductor Products	Phoenix, Arizona
NPC	Neucleonics	Los Angeles, California
PAK	Paktron	Alexandria, Virginia
RCA	RCA Semiconductor Division	Harrison, New Jersey
SPRA	Sarkes Tarzian, Inc.	Bloomington, Indiana
SYL	Sylvania Electric Products	Seneca Falls, New York
TI	Texas Instrument	Dallas, Texas
VARO	Varo Corporation	Garland, Texas

P.C. BOARD ASSEMBLY, ANSWER BACK

Ref. Des.	Description	Lsi Part No.	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty. 01 011	Note
1	P.C. Board Assy., Answer Back	129489-01				
2	I/C	128348-02			1	
3	I/C	128348-74			1	
4	I/C	128348-93			1	
5	I/C	128348-113			2	
6	I/C	128348-157			2	
7	Capacitor .1 uF	129329-104			2	
8	Capacitor 10 uF	129469-106			2	
9	P.W. Board	129489-05			1	
10	Prom, 82S23 Type	129493			1	
11	Socket, 16 Pin	802002	CA-16S-10SD	Circuit Assy.	3	
12	Socket, 18 Pin	802003	CA18S-10SD	Circuit Assy.	2	

ADM-3A P.C. BOARD ASSEMBLY

LSI Part Number	Description
128348-1	IC
128348-123A	IC
128348-1488	IC
128348-1489	IC
128348-154	IC
128348-1602	IC
128348-166	IC
128348-25	IC
128348-2513	IC
128348-4102	IC
128348-78M12	IC
128348-7805	IC
128348-7815	IC
128348-79M12	IC
128518-101	Cap, DM 15-101
128518-225	Cap 2.2 uF
128518-334	Cap .33 uF
128533-101	Resistor
128533-102	Resistor
128533-103	Resistor
128533-183	Resistor
128533-201	Resistor
128533-241	Resistor
128533-271	Resistor
128533-393	Resistor
128533-471	Resistor
128533-473	Resistor
128533-7R5	Resistor
129329-104	Cap
129451-3	Keyboard ADM-3A
129467-0	IC
129467-10	IC
129467-11	IC
129467-112	IC
129467-113	IC
129467-125	IC
129467-13	IC
129467-151	IC
129467-157	IC
129467-161	IC
129467-175	IC
129467-193	IC
129467-195	IC
129467-2	IC
129467-20	IC
129467-27	IC

ADM-3A P.C. BOARD ASSEMBLY (Continued)

LSI Part Number	Description
129467-283	IC
129467-293	IC
129467-32	IC
129467-4	IC
129467-42	IC
129467-51	IC
129467-74	IC
129467-8	IC
129467-85	IC
129467-86	IC
129468-108	Capacitor
129468-189	Cap
129468-506	Cap
129469-106	Cap
129469-306	Cap
129469-358	Cap
129470-5	Board, PC
129472-510	Resistor
129473-5	Jackscrew, Rev. "A"
129474-3	Heatsink
129474-9	Heatsink
129476-241	Network, Resistor
129476-472	Network, Resistor
129476-512	Resistor, Network
129478	Connector
129496-3	Plate, Clocure, Rev. "A"
801006	Pot, BM5874
802002	Socket CA16S10SD
802003	Socket, CA-18S-10SD
802006	Socket, CA24S10D
802008	Socket, CA40S10SD
803001	Resistor, PC5800
803002	Resistor, PC5802
804006	Switch, 435640-4
804007	Switch, 435640-1
804012	Switch, MSS1040D-1
806001	Knob, IRQ-5000-1-Blk
808001	Rectifier, Bridge MDA970-1
808002	Rectifier, Bridge W005M
808003	Diode, 1N914
808004	Diode, 1N4001
808006	Diode, 1N5231B
808007	Diode, 1N5338B
808008	Rectifier, Bridge WO2M
809001	Connector, 22-02-2041
809002	Connector, 22-02-2051

ADM-3A P.C. BOARD ASSEMBLY (Continued)

LSI Part Number	Description
809007	Connector, 09-18-5031
809008	Connector, 09-18-5051
809009	Connector, 09-18-5059
809012	Connector, 09-18-5121
810001	Transistor, 2N3904
810003	Transistor, 2N3906
810005	Transistor, 2N5986
811003	Crystal, 800A-10.8864MHz
819001	Isolator, Optical MCT-2
820002	Heatsink, 207-SB
821404	Screw, 4-40x3/8 Self-Tap PH
821601	Screw, 6x3/8 F504M
822401	Nut, 4 F557-7
823401	Washer, 4 MW 401M
823403	Washer, 4 Ext. Tooth
823601	Washer, 6 MW-423M
824010	Rivet, R3479x1/4
839001	Insulator, Mylar, 43-77-2
839003	Insulator, 97405 or 4x1/32
839012	Insulator, 7717-5
839013	Tape, Mylar, 1/2x5/8x.003
840003	Fuse, 273001 1 amp
840004	Holder, Fuse 281005

QTY REQD			FIND NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
			1				
			2				
		2	3	2-350803-2	.250X.032 TAB RCPT	AMP	1
			4				
			5				
		1	6	03-09-1033	RCPT 3CKT	MOLEX	
		3	7	350417-1	TERM, .093 SCK	AMP	1
			8				
		1	9	31889-1	TERM, PIOG RING #10	AMP	1
		AIR	10	18AWG(16x30) BLK	WIRE, UL STYLE 1015	PVC	1
		AIR	11	22AWG(7x30) YEL	WIRE, UL STYLE 1015	PVC	1
			12				
		AIR	13	20AWG(10x30)GRN	WIRE, UL STYLE 1015	PVC	1

SIZE A | CODE IDENT 98438 | 1294S9 | REV C

SCALE

SHEET 2

WIRE LIST

WIRE LIST (Continued)

LINE NO.	TERMINATION INFORMATION						WIRE INFORMATION						
	CABLE NO.	WIRE NO. OR COLOR	FROM		TO		FIND NO./NOTES					ROUTING	LGTH (IN.)
							FROM END		TO END		WIRE OR CABLE		
			REF DES	PIN	REF DES	PIN	CONN	TERMINATION	CONN	TERMINATION			
1													
2		YEL	SPKR		P5	2		SOLDER	6	7	11		15"
3		YEL	SPKR		P5	3		SOLDER		7	11		
4													
5									CONN PART OF TRANS				
6		GRN	GR. POINT		P4	3		9		7	13		23"
7													
8		BLK	S1	3	F1	END		3		3	10		10½"
9													
10													
11													
12													
13													
14													
15													
16													
17													
18													
19													
20													
21													
22													
23													
24													
25													

CODE NOTES:

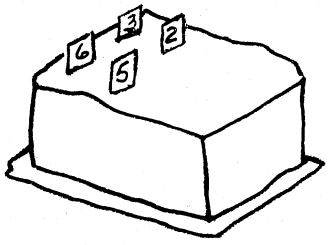
7-0601d (7-64)

SIZE	CODE IDENT		REV
A	98438	129459	C
SCALE		SHEET 3	

WIRE LIST (Continued)

LINE NO.	TERMINATION INFORMATION: CABLE NO.	WIRE NO. OR COLOR	FROM: REF DES	FROM: PIN	TO: REF DES	TO: PIN	WIRE INFORMATION: FIND NO./NOTES: FROM END: CONN	FROM END: TERMINATION	TO END: CONN	TO END: TERMINATION	WIRE OR CABLE	ROUTING	LGTH
1	TRANSFORMER HOOK-UP (REF 1294458)	YEL	T1	3	P3	1							
2		YEL		4		2							
3		RED		5		3							
4		RD/WH		6		4							
5		RED		7		5							
6													
7													
8													
9		ORN		8	P4	1							
10		ORN		9		2							
11													
12		BLK		1	S1	3							
13		BLK		2	F1	SIDE							
14													
15	PWR CORD 115 V (REF 1294455)	BLK	PWR CORD		S1	2							
16		WHT			S1	5							
17		GRN			GRD POINT								
18													
19	PWR CORD 230 V (REF 1294455)	BRN	PWR CORD		S1	2							
20		BLU			S1	5							
21		GN/YL			GRD POINT								
22													
23													
24													
25													

CODE NOTES:



REAR VIEW OF S1 (PWR SW)

SIZE	CODE IDENT		REV
A	98438	129459	C
SCALE		SHEET 4	

7-0601d (7-64)

WIRE LIST (Continued)

LINE NO.	TERMINATION INFORMATION						WIRE INFORMATION						
	CABLE NO.	WIRE NO. OR COLOR	FROM		TO		FIND NO./NOTES					ROUTING	LGTH
							FROM END		TO END		WIRE OR CABLE		
			REF DES	PIN	REF DES	PIN	CONN	TERMINATION	CONN	TERMINATION			
1	MONITOR HOOK-UP (REF 129481)	BRN	P7	1	MON P1	2							
2		RED		2		3							
3		ORG		3		4							
4		YEL		4		8							
5													
6		WHT		6		10							
7		GRN		7		5							
8		BLU		8		6							
9		VIO		9		9							
10		WHT		10		1							
11		BLK		11		7							
12													
13													
14													
15													
16													
17													
18													
19													
20													
21													
22													
23													
24													
25													

CODE NOTES:

SIZE	CODE IDENT		REV
A	98438	129459	B
SCALE		SHEET 5	

7-0601d (7-64)

SECTION 8
RETURNING EQUIPMENT FOR REPAIR

Equipment returned to LSI must be shipped prepaid and must have a Return Goods Authorization (RGA) number on the outside top of the carton or the shipment may be lost, misrouted or returned to you.

STEP 1

Prepare the following information:

Model type of equipment to be returned
Serial number
Reported symptom (if failure)
Type of modification or option to be installed (if applicable)

STEP 2

Please call (714) 774-1010 ext. 371 or write to

Lear Siegler Inc./EID
714 N. Brookhurst St.
Anaheim, Ca. 92803
Attn: Customer Service

Please state that you would like a Return Goods Authorization number. At this time, we will record the information you prepared as well as a purchase order number, if applicable.

STEP 3

You will then be provided with an RGA number and the address of the depot where we request that you return the equipment.

NOTE

All modifications and repairs are FOB Anaheim, California; Chicago, Illinois, or Philadelphia, Pennsylvania, whichever depot is used. Warranty repairs are to be sent to the repair depot with freight prepaid. They will be returned to you with the freight prepaid.

SECTION 9
PAINT

DRYING:

POLANE T®, catalyzed with POLANE® Catalyst V66 V 27, air-dries to touch and handle in 30-60 minutes, and can be force dried for 30 minutes at 180°-200° F. POLANE T® catalyzed with POLANE® Catalyst V66 V 29 air dries to touch and handle in 2-4 hours and can be force dried in 30 minutes at 200°-250° F.

POT LIFE:

POLANE T® is a two-component system — but this does not affect its production versatility. Finish coats have an 8 hr. working pot life after catalyzation. If it's necessary to "carry" catalyzed material over a week-end, simply add 80% uncatalyzed material to the mixture to extend pot life. On Monday, the required amount of catalyst is added.

PRECAUTIONS:

Do not spray hot. Heat will shorten pot life.

Do not pump from drums into circulating systems. Friction heat developed by pumps and circulation will shorten pot life.

Do not dip.

Do not flo-coat.

The catalyzing ratios as outlined have been established to provide optimum hardness, flexibility and chemical and solvent resistance. Slight over or under catalyzation will not seriously affect performance.

Excessive over catalyzation will result in increased hardness with marked brittleness and less flexibility. The gloss will also be increased. In the case of the spray fillers and glazing fillers, sanding will become more difficult.

Excessive under catalyzation will produce insufficient hardness, poor adhesion and poor chemical and solvent resistance.

POLANE T® should be applied only in well-ventilated areas. Wearing of a chemical cartridge respirator is recommended.

CHARACTERISTICS:

The tests below were conducted on standard POLANE T® quality. Test surface — Panels of Parker Bonderite 1000 with 1 to 1.2 mil dry film thickness of POLANE T®.

All tests conducted after fourteen days air curing period.

1. 5% salt spray — 500 hours, plus. Excellent
2. 100% relative humidity — 500 hours. No effect.
3. Water immersion — fresh, salt, distilled — 100 hours, plus. No effect.
4. Lacquer thinner, acetone, gasoline, Xylol resistance. 20 rubs with saturated cloth.
5. Excellent resistance to lubricating oils, coolants and phosphate ester hydraulic fluids.
6. 24 hours boiling water. Excellent.
7. Cold check: 16 cycles; 24 hours, 100% humidity; 24 hours, —10° F; 24 hours —72° F. — excellent.
8. Pencil hardness — H to 2H.
9. Flexibility — ⅛ inch conical mandrel. No effect.
10. Excellent abrasion resistance. Taber abrasion — CS17 wheel, 1000 gm. load: 2,500 revolutions/1 mil removal; 0.090 gm. loss/1,000 cycles.

Gloss — textured finish gloss range 10°-30°, measured on 60° photovoltmeter. Higher ranges are available.

APPLICATION CATALYZATION:

POLANE T® is a two-component finish, and must be catalyzed 6 parts base materials to 1 part POLANE® Catalyst V66 V 27 or V66 V 29. This mixture is then split into two batches — one for the smooth and one for the spatter coat that is necessary to obtain the textured effect.

Prior to application, the smooth base coat should then be reduced three parts catalyzed material to one part POLANE® Reducer R7 K 69.

The spatter coat is not reduced.

POLANE® Catalyst V66 V 27 is recommended for interior use. POLANE® Catalyst V66 V 29 is recommended for exterior use. The use of POLANE® Catalyst V66 V 27 on an exterior exposure would lead to premature chalking or loss of gloss. The POLANE® Catalyst V66 V 29 produces a more chalk resistant coating with excellent gloss retention. POLANE® Catalyst V66 V 29 does however increase the cure time requirement.

REDUCTION:

POLANE T® Reducer R7 K 69 is a medium to fast evaporating solvent recommended for reducing catalyzed POLANE T® first smooth coat to spraying viscosity.

For more specific information on the catalyzation and reduction of POLANE T® materials, follow instructions on the direction label or request a detailed data sheet on the particular POLANE T® material in question.

SPRAYING:

POLANE T® Base coat can be applied with standard pressure or suction feed spray equipment. The texture coat must use pressure equipment.

Polane T® First (Base) Coat

Pressure feed — Use De Vilbiss MBC gun with E tip and needle and No. 765 air cap.
5-8 p.s.i. fluid pressure.
40-45 p.s.i. atomizing pressure.

Suction feed — Use De Vilbiss MBC gun with E tip and needle and No. 30 air can.
40-50 p.s.i. atomizing pressure.

The smooth first coat should be sprayed to approximately 1 mil dry. Allow 5 minutes to flash-off before application of the spatter coat.

Polane T® — Second Texture Coat

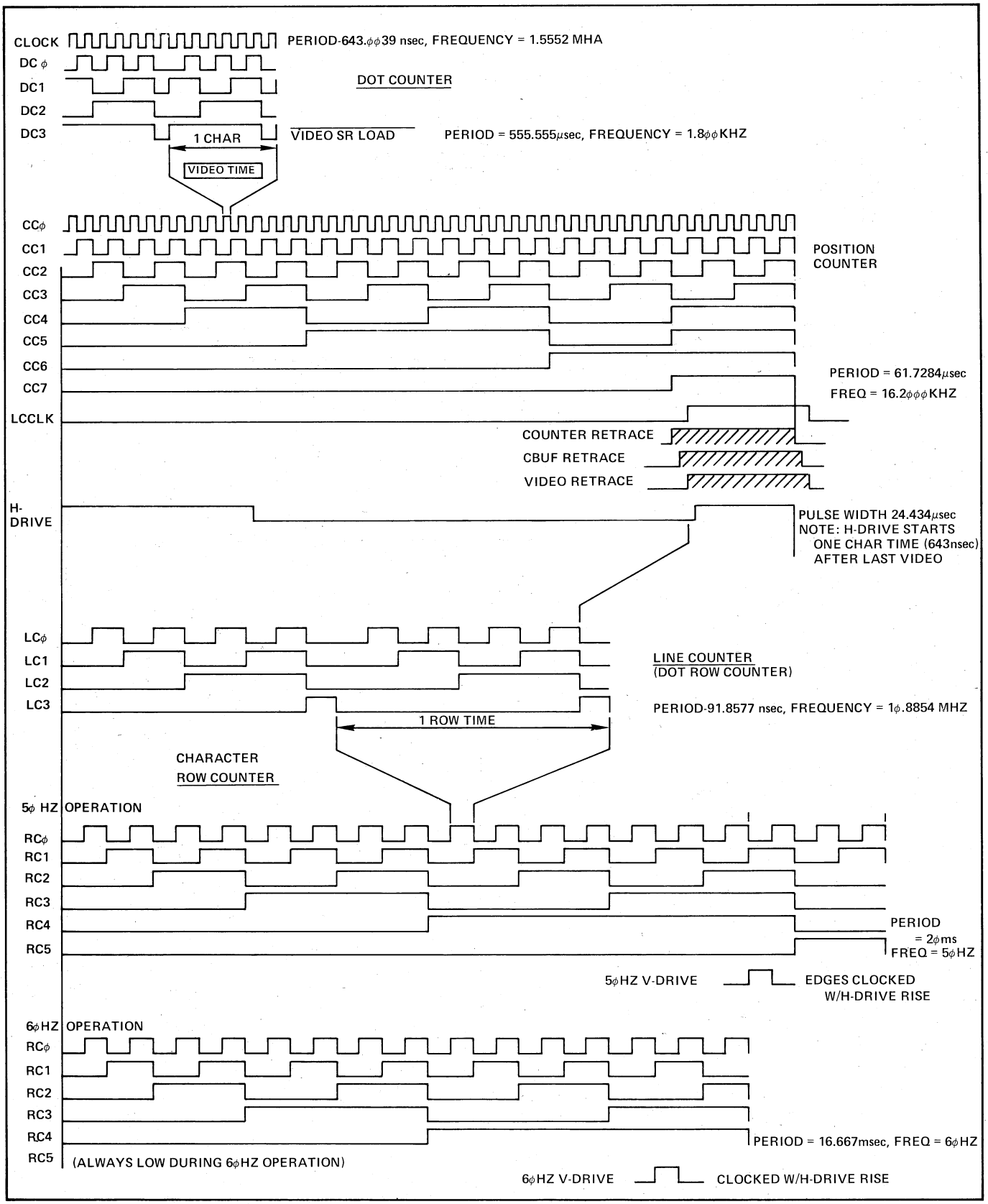
Use De Vilbiss MBC gun with E tip and needle and No. 70 air cap of Binks No. 19 gun with 66-66PD nozzle combination.
15 p.s.i. fluid pressure.
15-20 p.s.i. atomizing pressure.

For application by Ransburg, DeVilbiss or Nordson electronstatic hand guns, the solvent balance can generally be adjusted to the proper polarity using R7 K 69 reducer to produce satisfactory wrap of base coat.

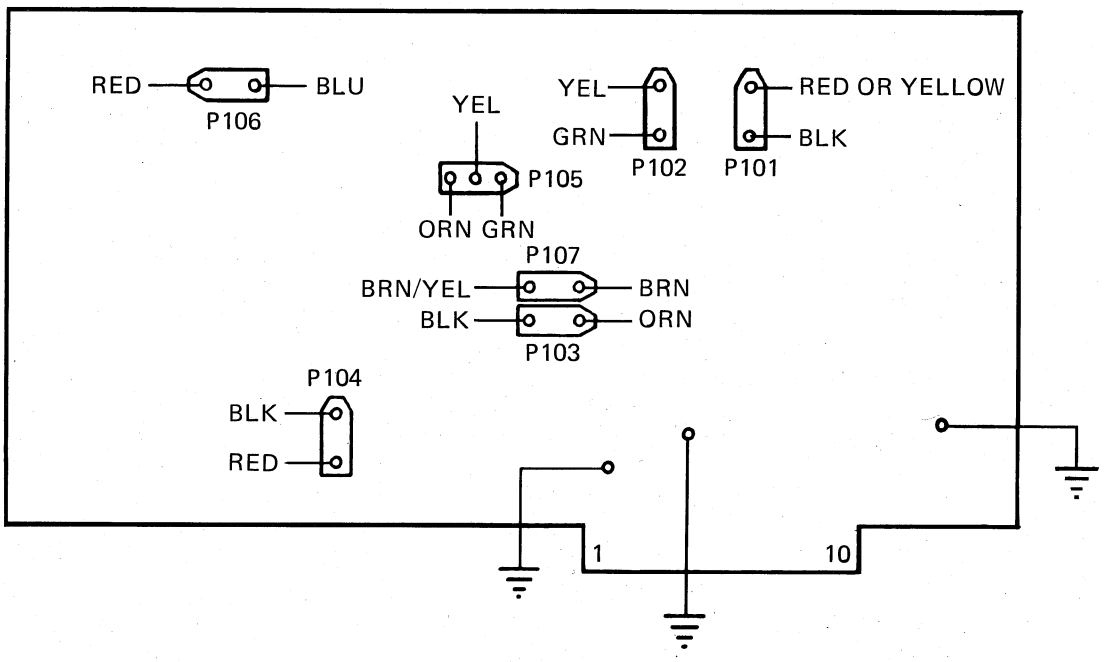
These adjustments will vary with the particular POLANE T® material involved, and specific recommendations should be requested from the laboratory before conducting trial runs or tests.

In regard to the texture coat, the texture may be varied by balancing the atomizing against the fluid pressure until the desired size is obtained. The lower the atomizing pressure, the larger the pattern. The flatness of the pattern can be set by adjusting the viscosity of the spatter coat. The lower the viscosity, the flatter the texture. Recommendations above indicate no reduction for the spatter coat to obtain an acceptable pattern; however, reduction may be necessary to obtain special effects. Once the variables — viscosity, atomizing and fluid pressure — have been set, it is a simple matter to obtain a consistent texture on each part.

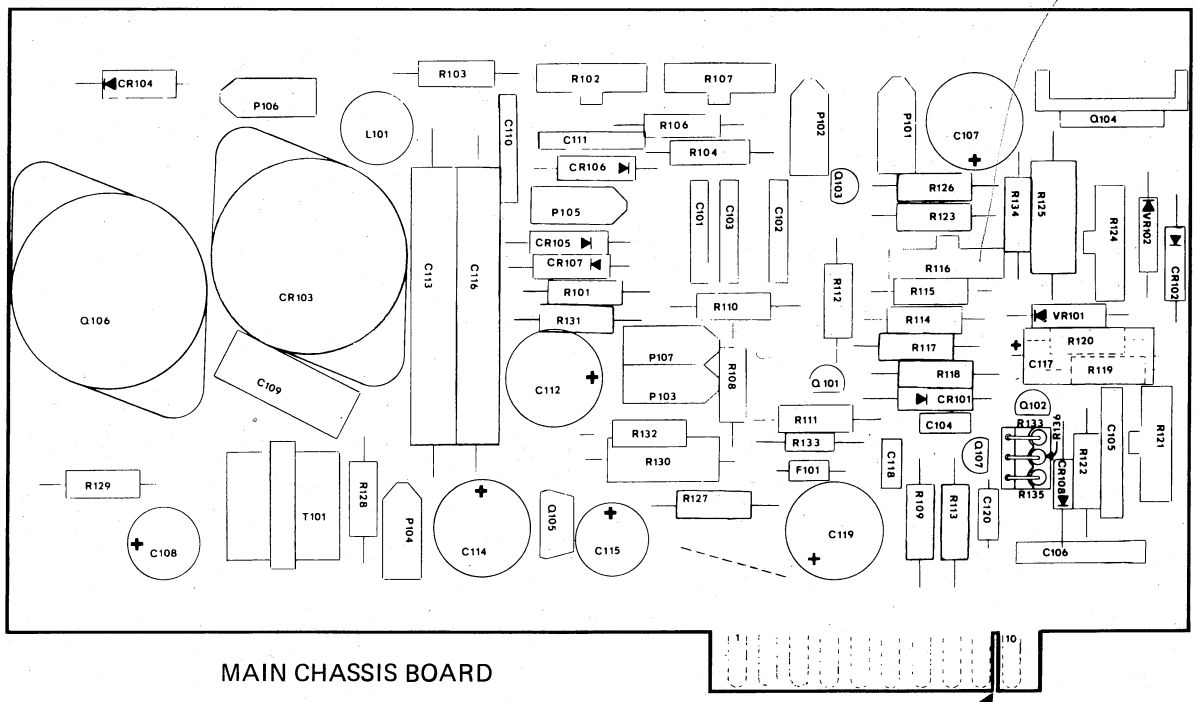
APPENDIX A



DISPLAY COUNTER TIMING



Vent Freq

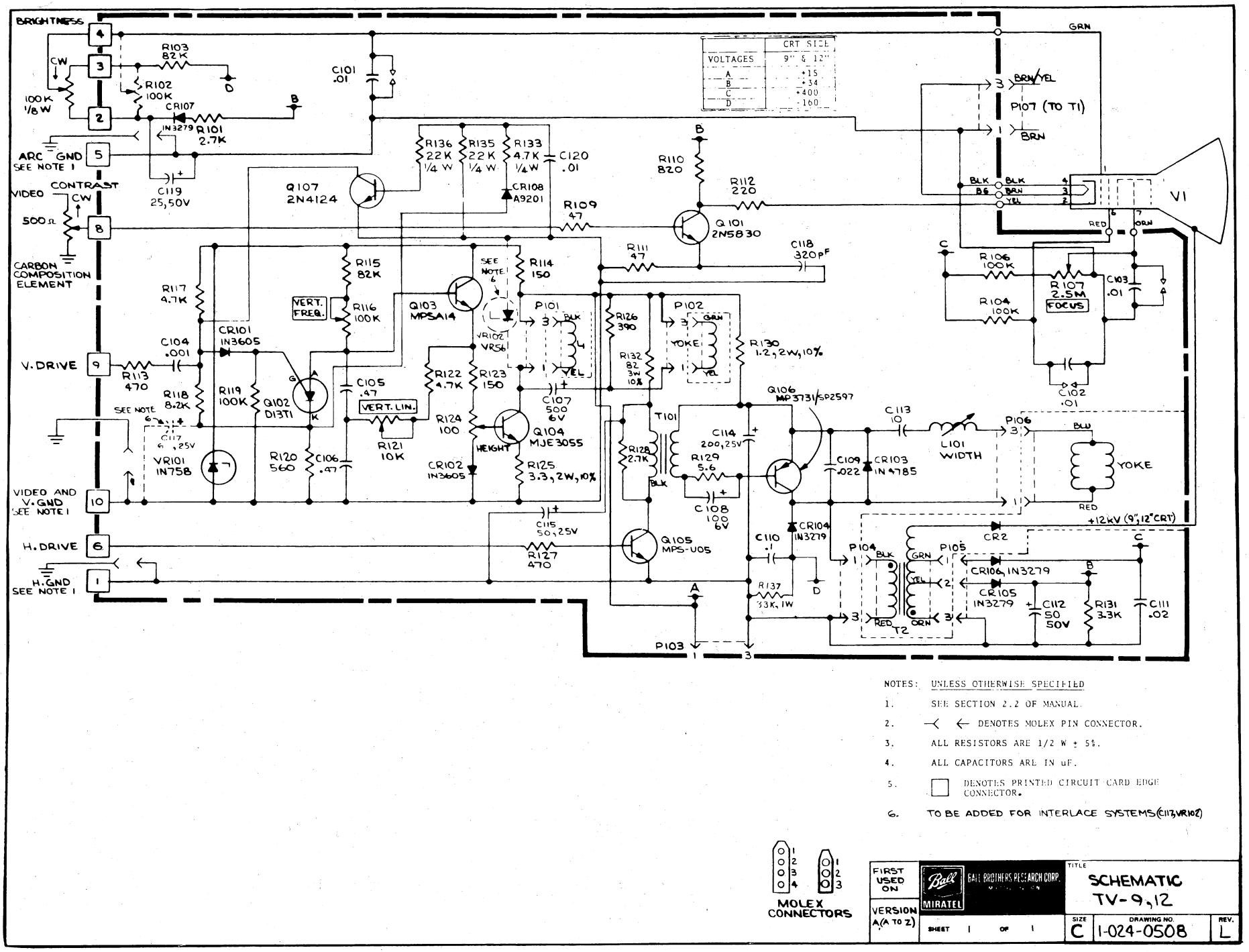


MAIN CHASSIS BOARD

KEYWAY FOR CONNECTOR POLARIZATION

NOTE:
F101 AND R108 ARE USED ONLY WHEN LOW VOLTAGE POWER SUPPLY IS NOT SUPPLIED.

MONITOR CIRCUIT BOARD COMPONENTS LOCATION

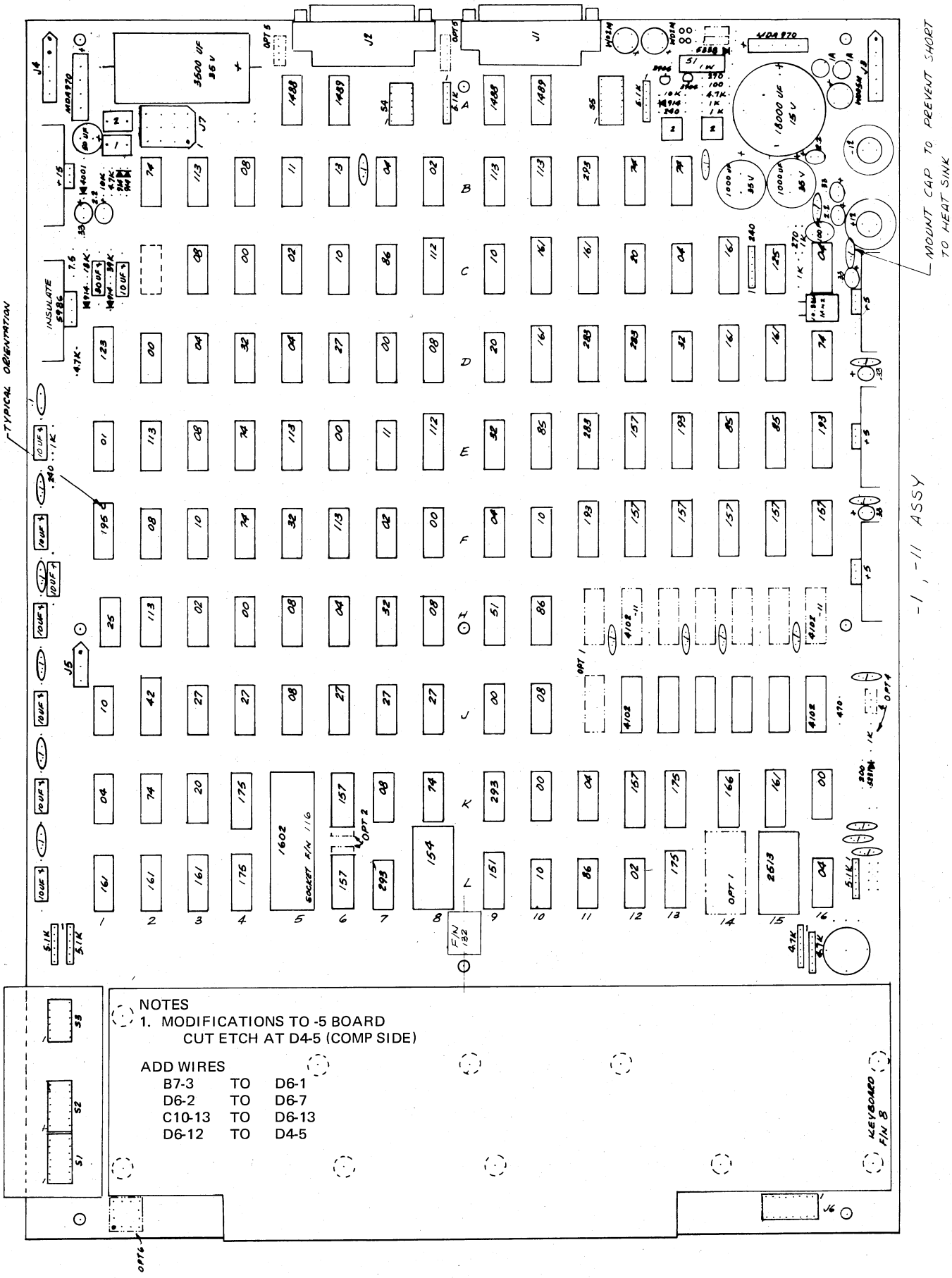


NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE SECTION 2.2 OF MANUAL.
2. ← DENOTES MOLEX PIN CONNECTOR.
3. ALL RESISTORS ARE 1/2 W ± 5%.
4. ALL CAPACITORS ARE IN uF.
5. □ DENOTES PRINTED CIRCUIT CARD EDGE CONNECTOR.
6. TO BE ADDED FOR INTERLACE SYSTEMS (C113, VR102)

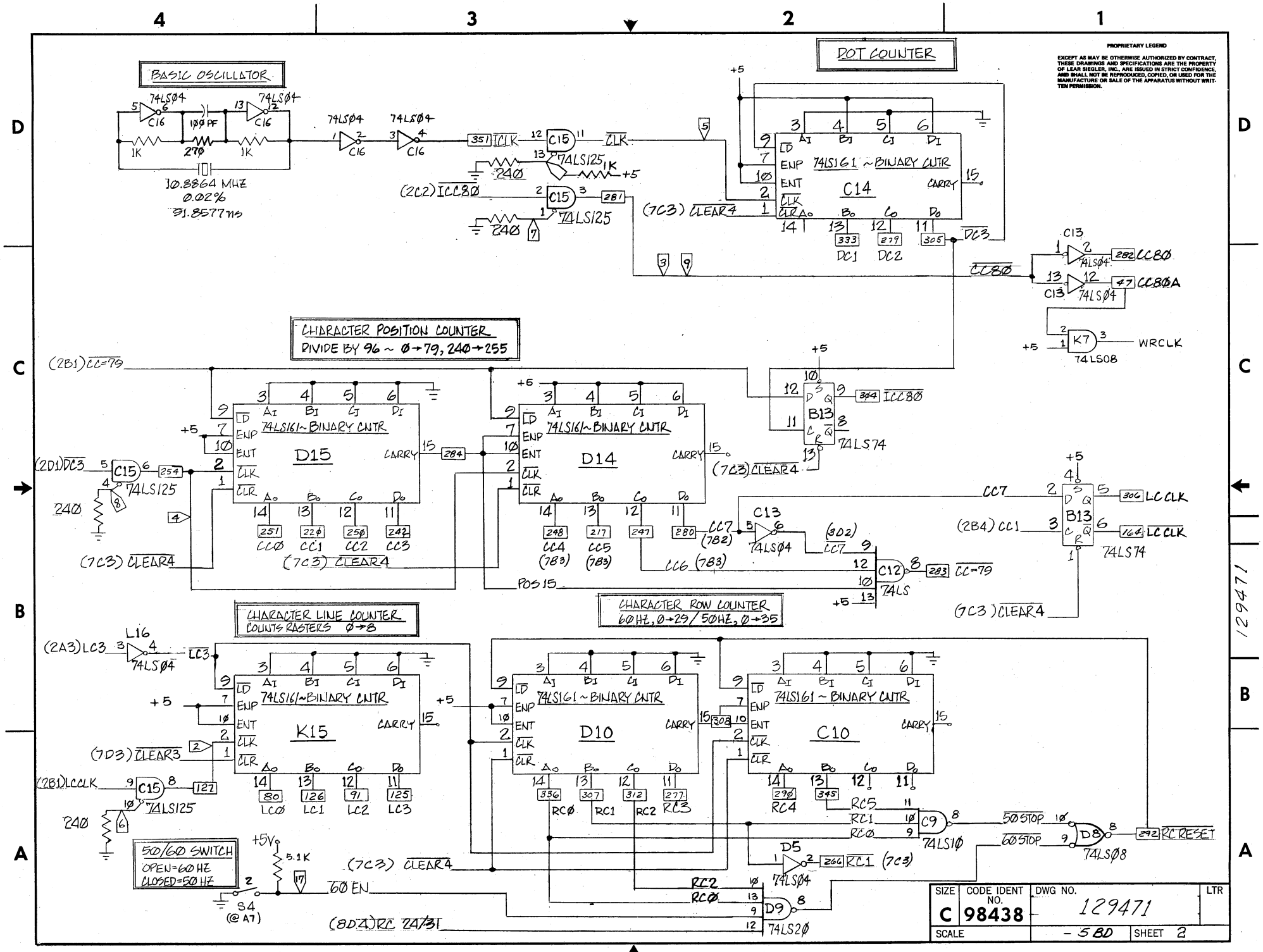
MOLEX CONNECTORS

FIRST USED ON	Ball BALL BROTHERS RESEARCH CORP. MIRATEL	TITLE: SCHEMATIC TV-9,12	
VERSION A(A TO Z)	SHEET 1 OF 1	SIZE C	DRAWING NO. 1-024-0508 REV. L

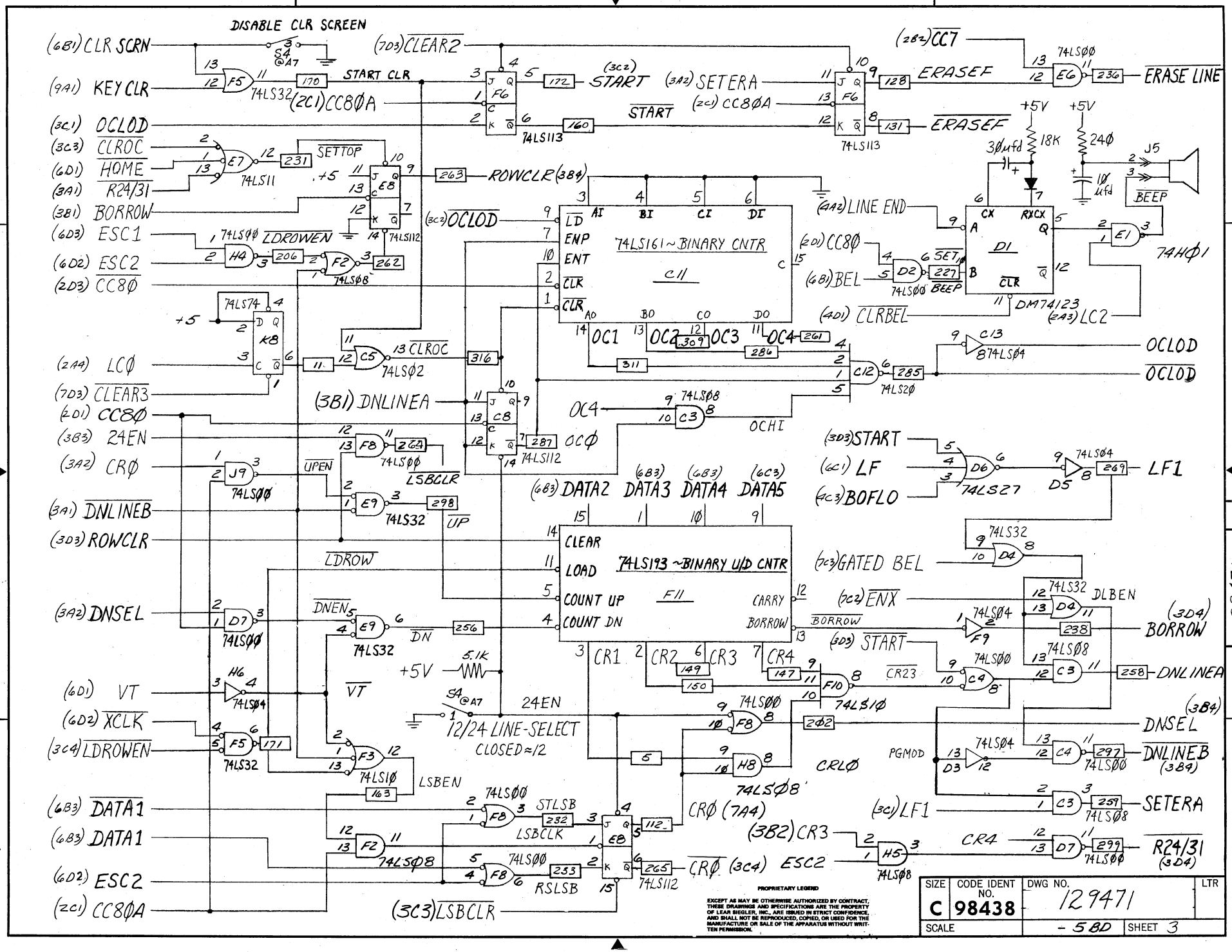


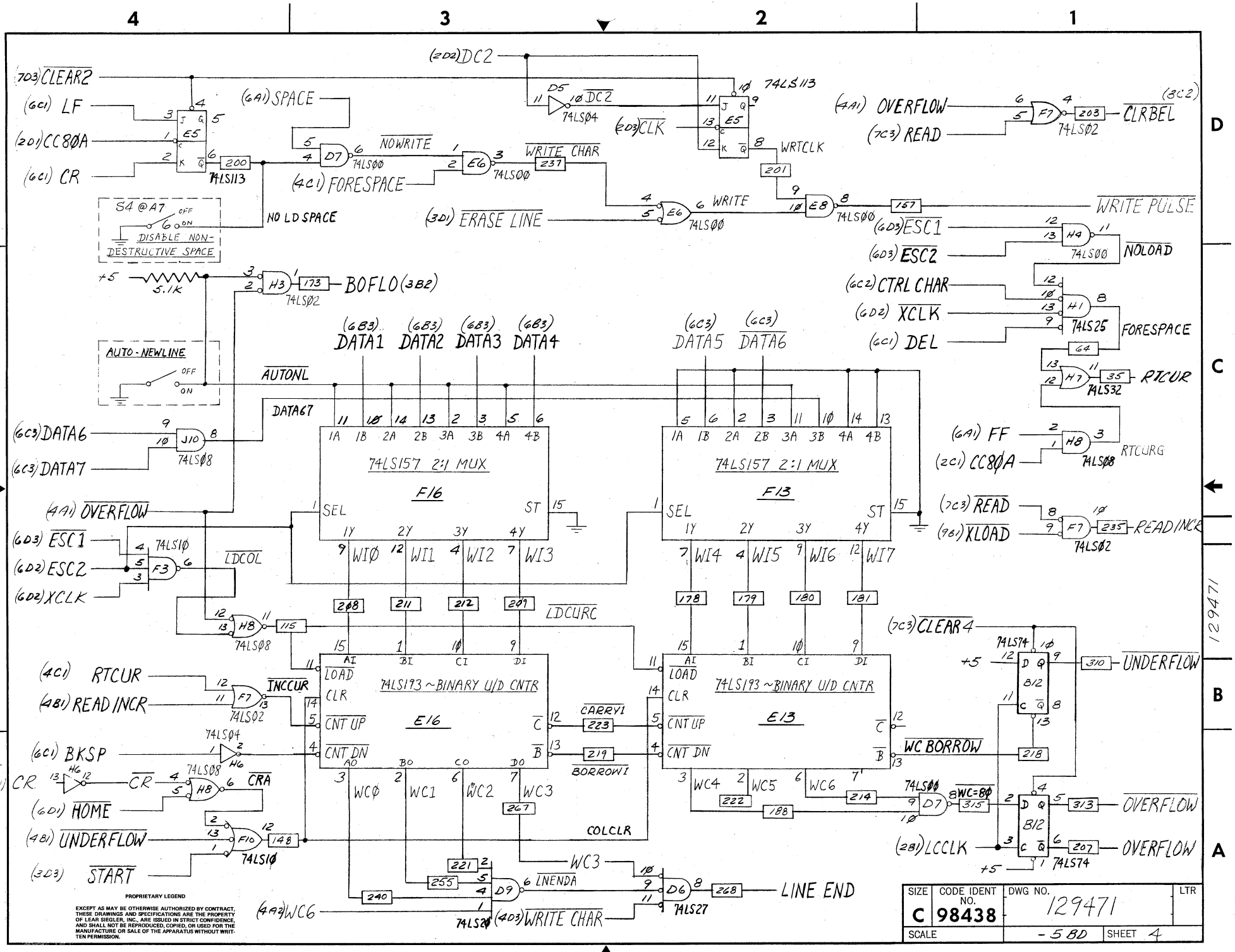
P.C. BOARD ASSEMBLY

APPENDIX B



BASIC OSCILLATOR
DOT COUNTER
CHARACTER POSITION COUNTER
DIVIDE BY 96 ~ 0→79, 240→255
CHARACTER LINE COUNTER
COUNTS RASTERS 0→8
CHARACTER ROW COUNTER
60HZ, 0→29 / 50HZ, 0→35
50/60 SWITCH
OPEN=60 HZ
CLOSED=50 HZ
10.8864 MHZ
0.02%
91.8577 ns
74LS161 ~ BINARY CNTR
74LS04
74LS125
74LS08
74LS74
74LS10
74LS20
74LS
C14
D15
D14
K15
D10
C10
B13
C15
C13
C12
C9
D5
D8
D9
L16
S4
(@ A7)
WRCLK
LC CLK
RC RESET
50 STOP
60 STOP
60 EN
(7C3) CLEAR4
(7D3) CLEAR3
(2B1) CC=79
(2D1) DC3
(2A3) LC3
(2B1) LCCLK
(2B4) CC1
(8D4) RC 24/31
PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
SIZE C
CODE IDENT NO. 98438
DWG NO. 129471
LTR
SCALE
- 5 BD
SHEET 2
129471


DISABLE CLR SCREEN
(6B1) CLR SCRN
(9A1) KEY CLR
(3C1) OCLOD
(3C3) CLROC
(6D1) HOME
(3A1) R24/31
(3B1) BORROW
(6D3) ESC1
(6D2) ESC2
(2D3) CC8Ø
(2A4) LCØ
(7D3) CLEAR3
(2D1) CC8Ø
(3B3) 24EN
(3A2) CRØ
(3A1) DNLINEB
(3D3) ROWCLR
(3A2) DNSEL
(6D1) VT
(6D2) XCLK
(3C4) LDROWEN
(6B3) DATA1
(6B3) DATA1
(6D2) ESC2
(2C1) CC8ØA
(7D3) CLEAR2
START CLR
(2C1) CC8ØA
(3C2) START
START
(3A2) SETERA
(2C1) CC8ØA
(2B2) CC7
ERASEF
ERASEF
ERASE LINE
SETTOP
ROWCLR (3B4)
(3C2) OCLOD
LDROWEN
74LS161 ~ BINARY CNTR
C11
LD
ENP
ENT
CLK
CLR
AI
BI
CI
DI
AO
BO
CO
DO
OC1
OC2
OC3
OC4
(4A2) LINE END
(2D1) CC8Ø
(6B1) BEL
(4D1) CLRBEL
DM74123
(2A3) LC2
74HØ1
BEEP
J5
+5V
18K
24Ø
3Ø µfd
1Ø µfd
OCLOD
OCLOD
CLROC
(3B1) DNLINEA
OCØ
OCHI
(3D3) START
(6C1) LF
(4C3) BOFLO
LF1
(6B3) DATA2
(6B3) DATA3
(6B3) DATA4
(6C3) DATA5
74LS193 ~ BINARY U/D CNTR
F11
CLEAR
LOAD
COUNT UP
COUNT DN
CARRY
BORROW
CR1
CR2
CR3
CR4
(7C3) GATED BEL
(7C2) ENX
DLBEN
BORROW
(3D4) BORROW
(3D3) START
CR23
DNLINEA
DNSEL
(3B4) DNLINEB
PGMOD
SETERA
(3C1) LF1
R24/31
(3D4)
CRØ (7A4)
(3B2) CR3
CRØ (3C4)
ESC2
CRØ
(3C3) LSBCLR
LSBCLR
UPEN
UP
LDROW
DNEN
DN
VT
LSBEN
STLSB
LSBCLK
RSLSB
5.1K
24EN
12/24 LINE-SELECT
CLOSED ≈ 12
PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
SIZE C
CODE IDENT NO. 98438
DWG NO. 129471
LTR
SCALE
- 5BD
SHEET 3
129471

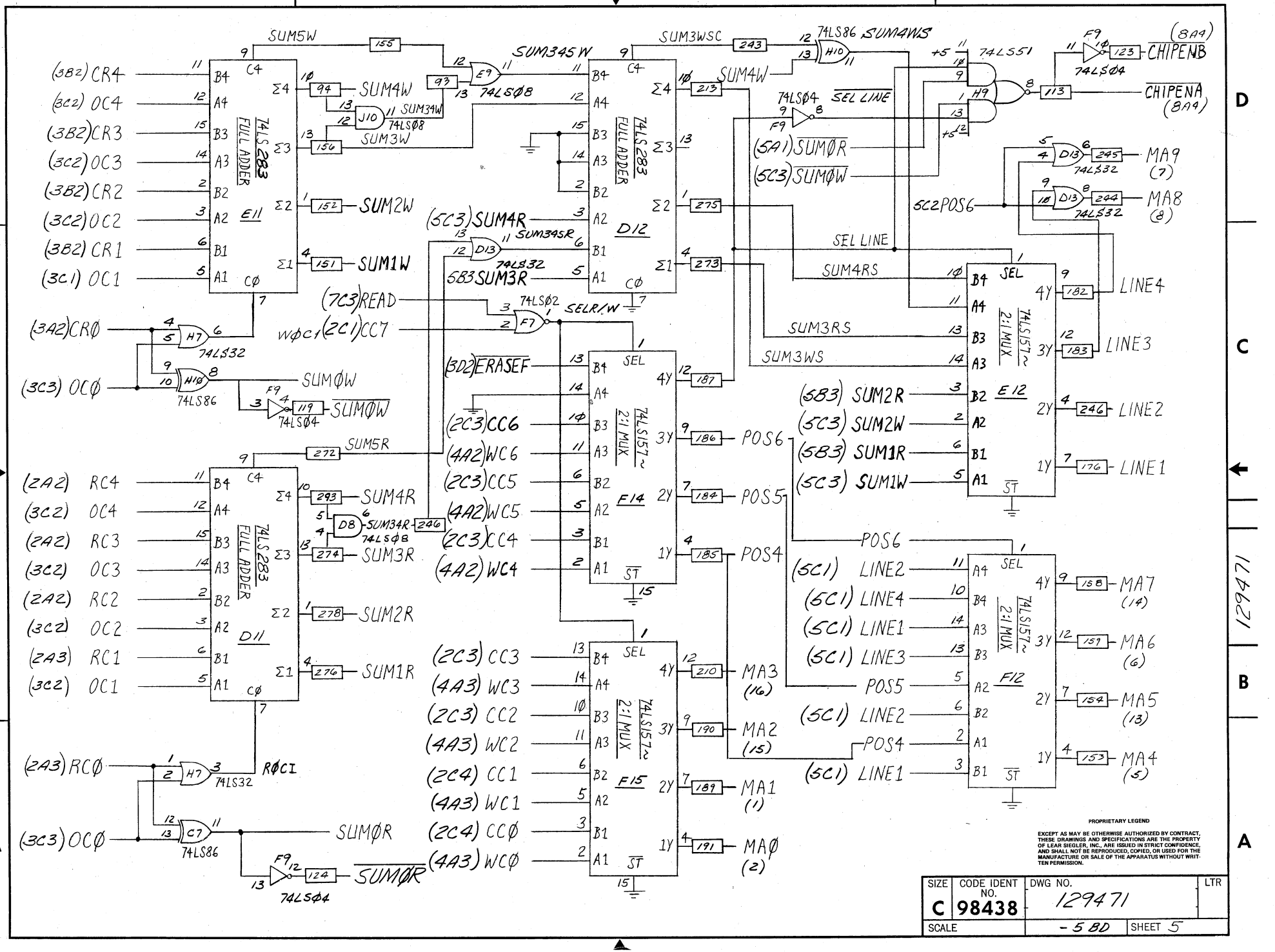


PROPRIETARY LEGEND

EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE		- 580	SHEET 4

129471

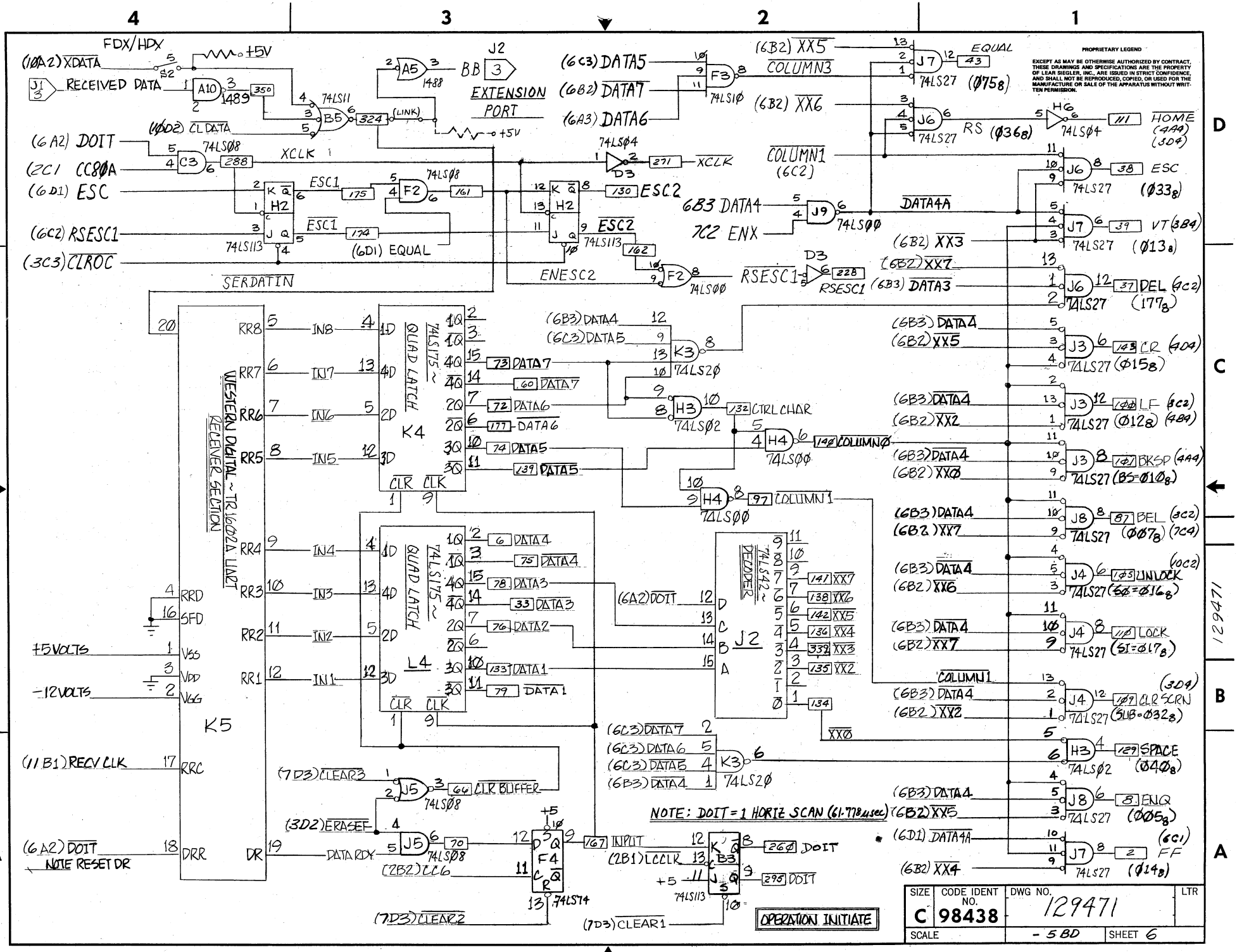


PROPRIETARY LEGEND

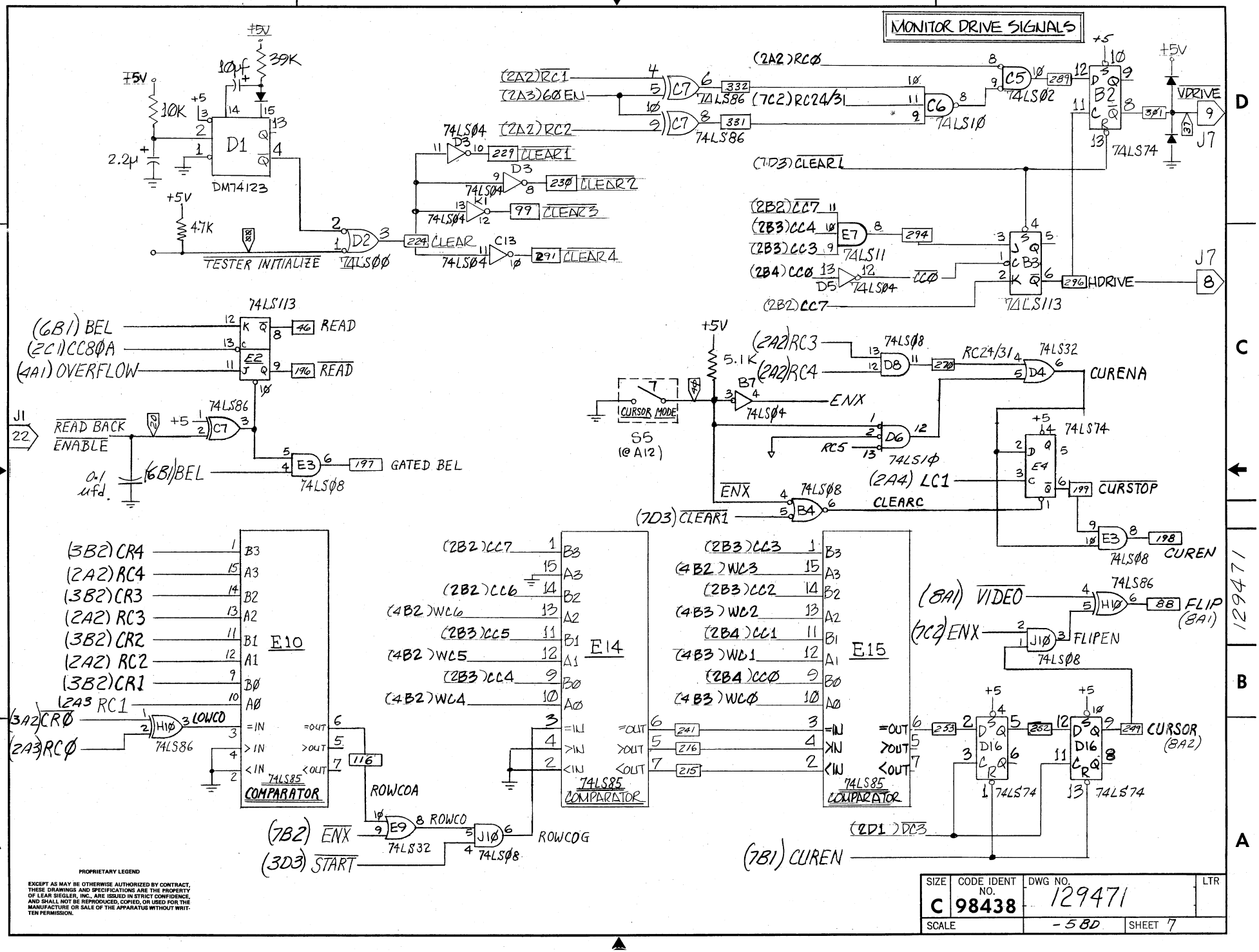
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE		-5 BD	SHEET 5

129471



FDX/HDX
(10A2) XDATA
RECEIVED DATA
(10D2) CL DATA
(6A2) DOIT
(2C1 CC80A
(6D1) ESC
(6C2) RSESC1
(3C3) CLROC
SERDATIN
XCLK
ESC1
(6D1) EQUAL
ESC2
ENESC2
EXTENSION PORT
BB
(6C3) DATA5
(6B2) DATA7
(6A3) DATA6
(6B2) XX5
COLUMN3
(6B2) XX6
EQUAL
RS (036₈)
HOME (4A4) (3D4)
COLUMN1 (6C2)
6B3 DATA4
7C2 ENX
DATA4A
ESC (033₈)
VT (3B4) (013₈)
(6B2) XX3
(6B2) XX7
(6B3) DATA3
DEL (4C2) (177₈)
RSESC1
WESTERN DIGITAL ~ TR1602A UART RECEIVER SECTION
K5
K4
L4
QUAD LATCH
74LS175 ~
74LS42 ~ DECODER
J2
CTRL CHAR
COLUMN0
COLUMN1
CR (4D4) (015₈)
LF (3C2) (012₈) (4B4)
BKSP (4A4) (BS=010₈)
BEL (3C2) (007₈) (7C4)
UNLOCK (10C2) (SO=016₈)
LOCK (SI=017₈)
CLR SCRN (3D4) (SUB=032₈)
SPACE (040₈)
ENQ (005₈)
FF (6C1) (014₈)
+5VOLTS
-12VOLTS
(11B1) RECV CLK
(6A2) DOIT
NOTE RESET DR
(7D3) CLEAR3
CLR BUFFER
(3D2) ERASEF
DATA RDY
(2B2) CC6
(7D3) CLEAR2
(7D3) CLEAR1
INPUT
(2B1) LCCLK
NOTE: DOIT = 1 HORIZ SCAN (61.778 μsec)
OPERATION INITIATE
PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
SIZE C
CODE IDENT NO. 98438
DWG NO. 129471
LTR
SCALE
-5BD
SHEET 6
129471

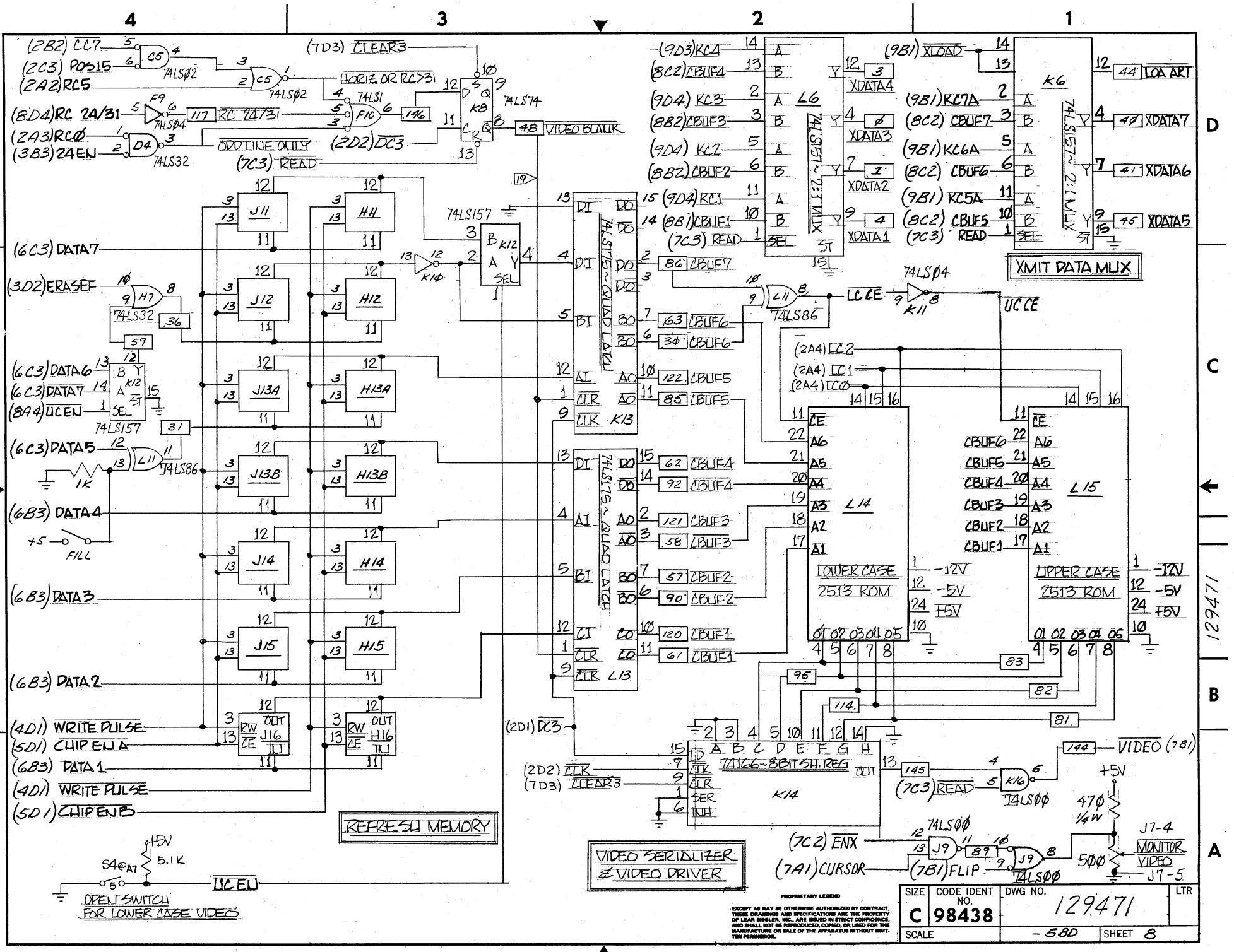


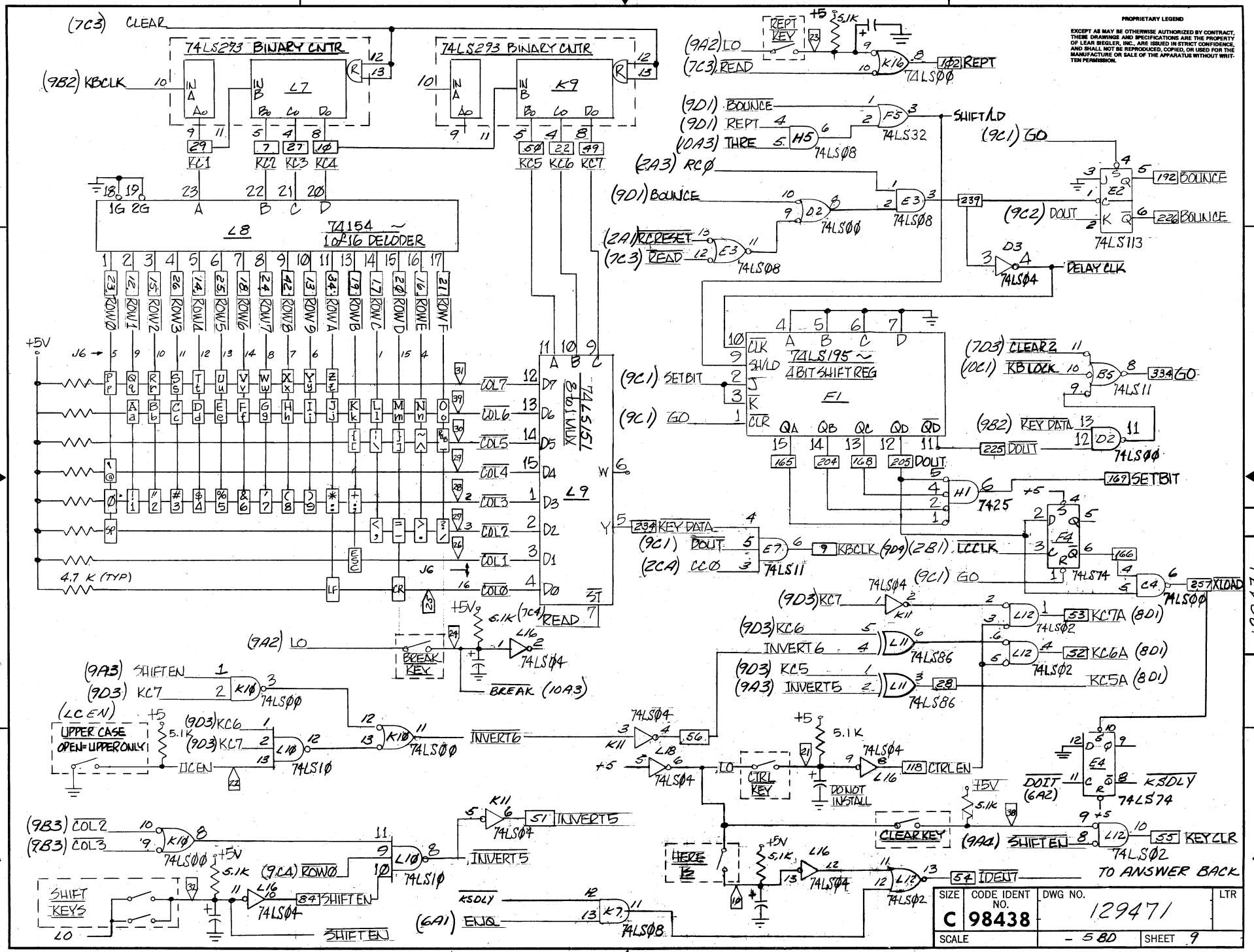
PROPRIETARY LEGEND

EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE		-58D	SHEET 7

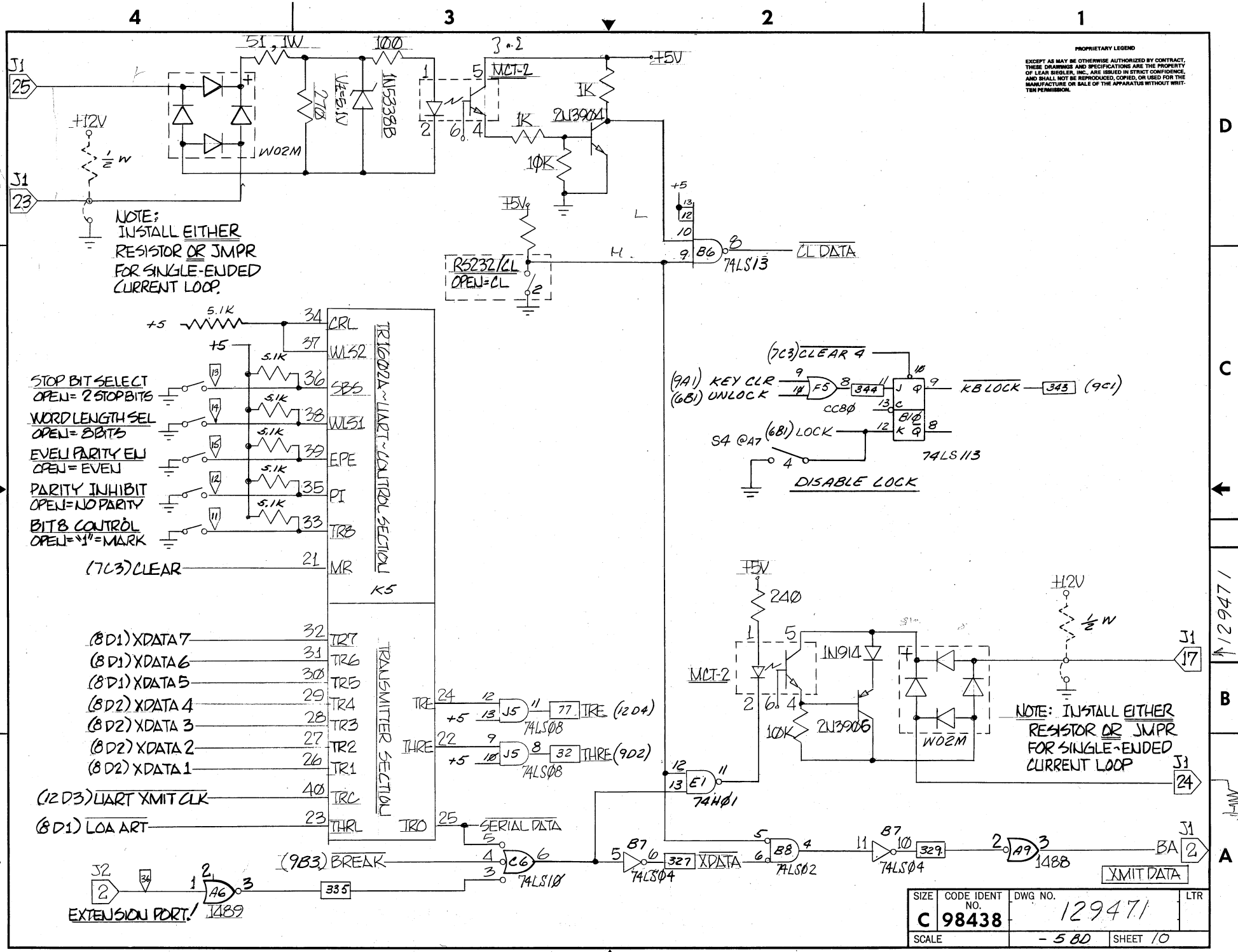
129471


REFRESH MEMORY
VIDEO SERIALIZER & VIDEO DRIVER
XMIT DATA MUX
LOWER CASE 2513 ROM
UPPER CASE 2513 ROM
OPEN SWITCH FOR LOWER CASE VIDEO
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129471
LTR
SCALE
SHEET 8

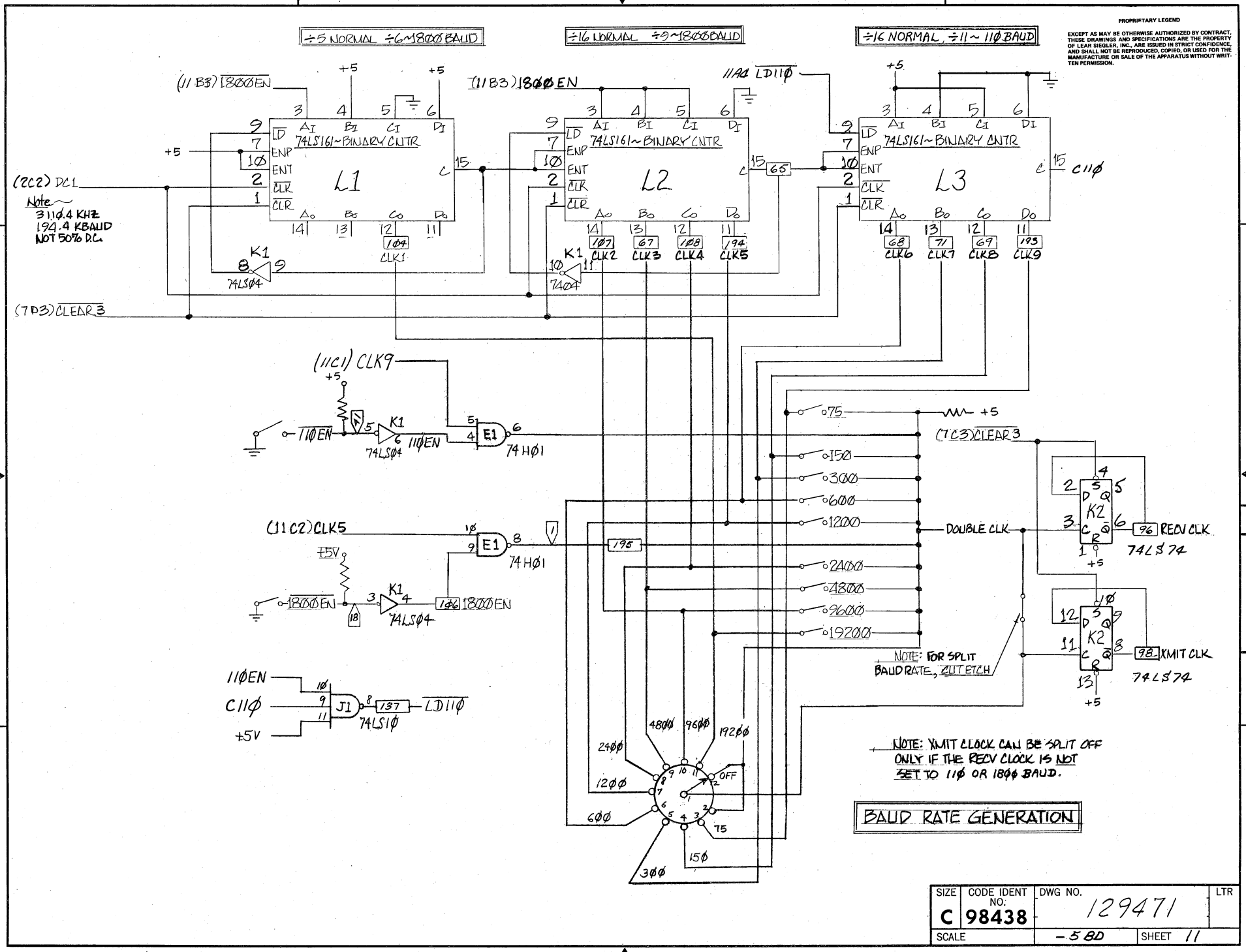


PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	12947/	
SCALE		- 5 BD	SHEET 9

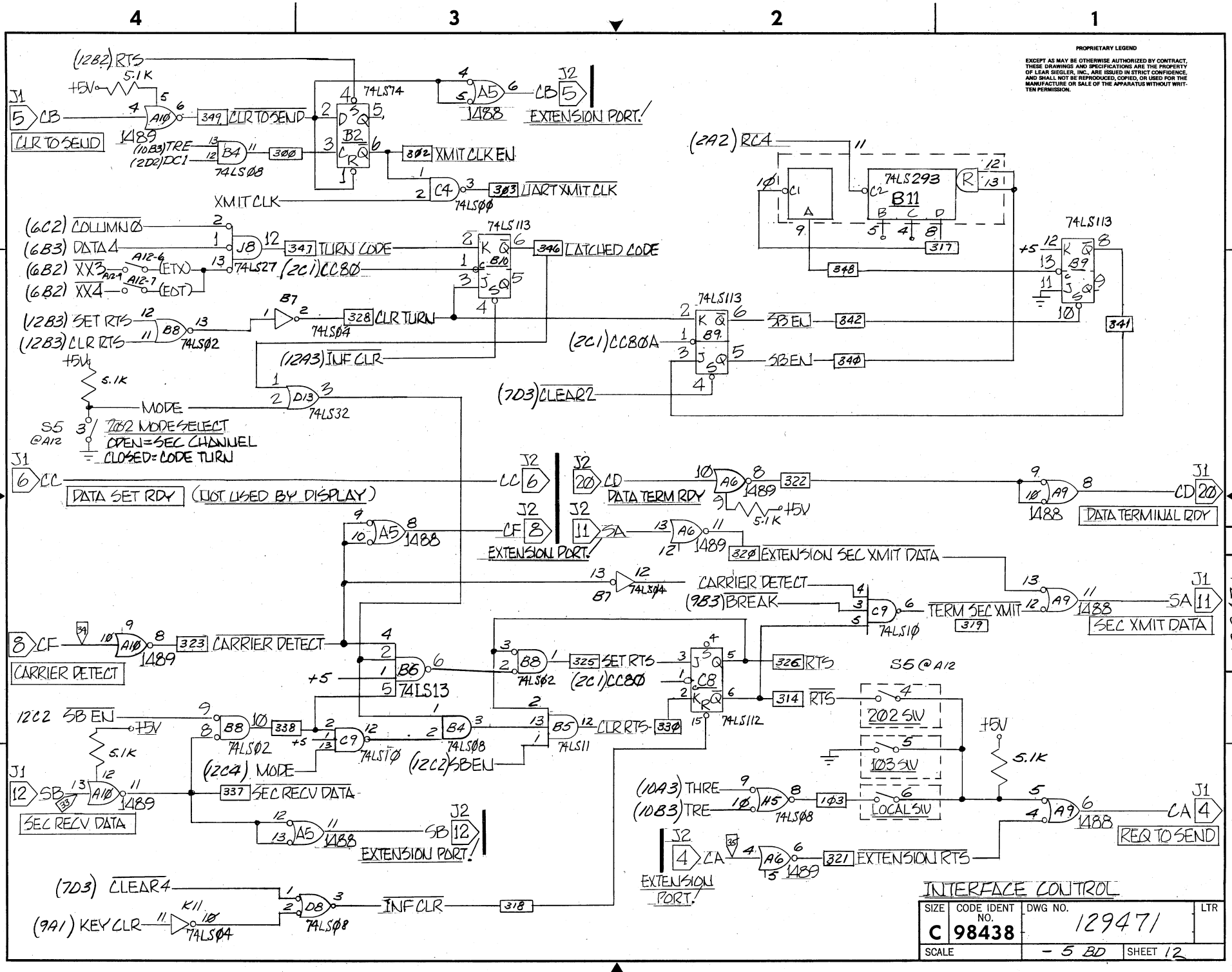


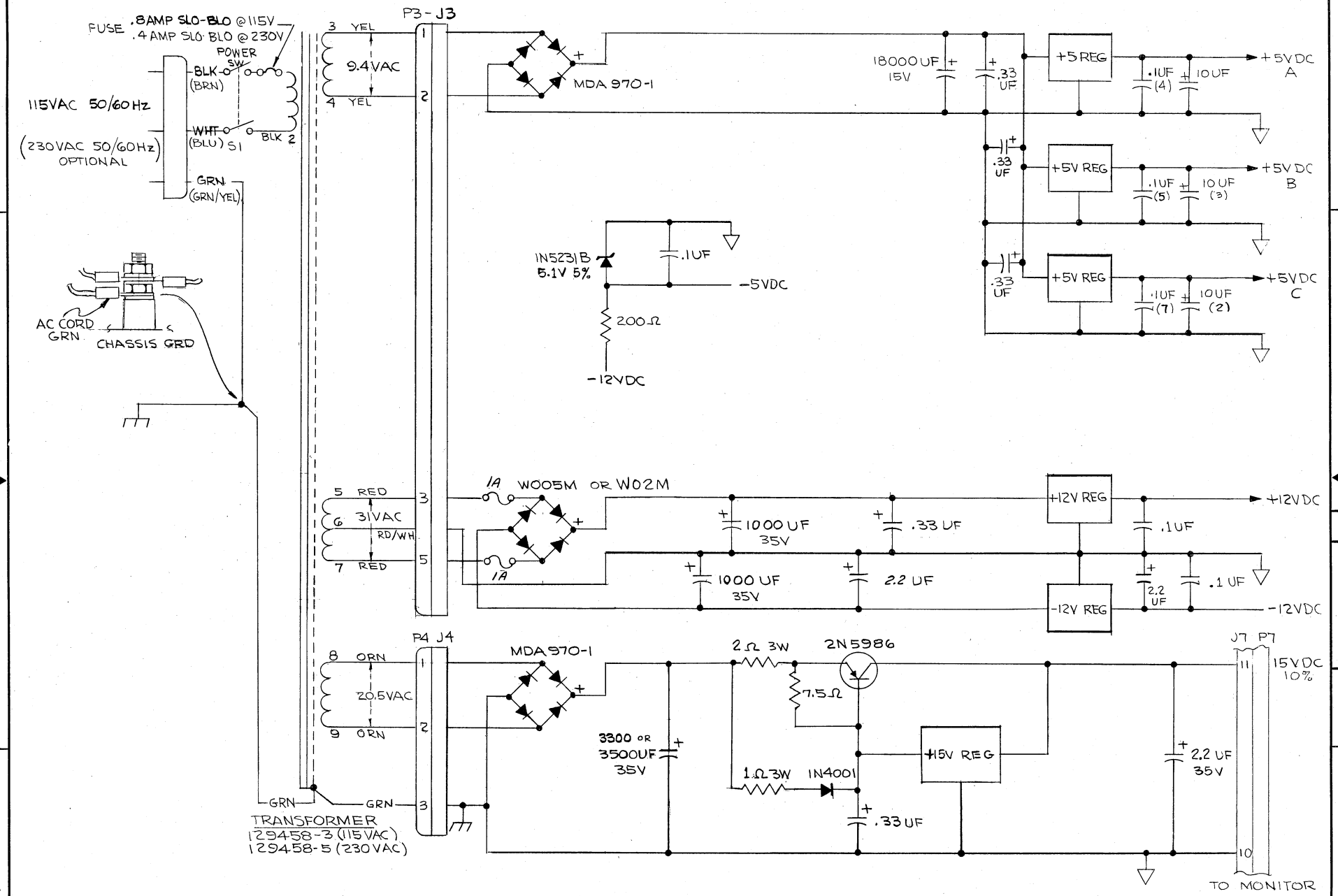
PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
J1 25
J1 23
+12V
1/2 W
51, 1W
100
270
Vz=5.1V
1N5338B
W02M
MCT-2
+5V
1K
2N3904
10K
NOTE: INSTALL EITHER RESISTOR OR JMPR FOR SINGLE-ENDED CURRENT LOOP.
RS232/CL OPEN=CL
B6 74LS13
CL DATA
5.1K
STOP BIT SELECT OPEN= 2 STOP BITS
WORD LENGTH SEL OPEN= 8 BITS
EVEN PARITY EN OPEN= EVEN
PARITY INHIBIT OPEN=NO PARITY
BIT 8 CONTROL OPEN="1"=MARK
(7C3) CLEAR
CRL
WLS2
SBS
WLS1
EPE
PI
TR8
MR
TR1602A~UART~CONTROL SECTION
K5
(8D1) XDATA 7
(8D1) XDATA 6
(8D1) XDATA 5
(8D2) XDATA 4
(8D2) XDATA 3
(8D2) XDATA 2
(8D2) XDATA 1
(12D3) UART XMIT CLK
(8D1) LOA ART
TR7
TR6
TR5
TR4
TR3
TR2
TR1
TRC
THRL
TRANSMITTER SECTION
TRE
THRE
TRO
J5 74LS08
77 TRE (12D4)
32 THRE (9D2)
SERIAL DATA
(9B3) BREAK
C6 74LS10
B7 74LS04
327 XDATA
B8 74LS02
B7 74LS04
329
A9 1488
BA
XMIT DATA
J2 2
EXTENSION PORT!
A6 1489
335
(7C3) CLEAR 4
(9A1) KEY CLR
(6B1) UNLOCK
F5 CC80
344
KB LOCK
343 (9C1)
B10
(6B1) LOCK
S4 @A7
74LS113
DISABLE LOCK
240
MCT-2
1N914
2N3906
10K
W02M
NOTE: INSTALL EITHER RESISTOR OR JMPR FOR SINGLE-ENDED CURRENT LOOP
J1 17
J1 24
J1 2
129471
SIZE C
CODE IDENT NO. 98438
DWG NO. 129471
LTR
SCALE
-5 BD
SHEET 10



SIZE	CODE IDENT NO:	DWG NO.	LTR
C	98438	129471	
SCALE		-580	SHEET 11

129471 / B


PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
(12B2) RTS
5.1K
+5V
J1 5 CB
CLR TO SEND
1489
349 CLR TO SEND
74LS74
1488
J2 5 CB
EXTENSION PORT
(10B3) TRE
(12D2) DC1
74LS08
300
302 XMIT CLK EN
XMIT CLK
74LS00
303 UART XMIT CLK
(6C2) COLUMN 0
(6B3) DATA 4
(6B2) XX3
(6B2) XX4
A12-6
A12-7
ETX
EOT
74LS27
347 TURN CODE
74LS113
(2C1) CC80
346 LATCHED CODE
(12B3) SET RTS
(12B3) CLR RTS
74LS02
328 CLR TURN
(12A3) INF CLR
(2A2) RCA
74LS293
B11
317
348
341
(2C1) CC80A
342 SB EN
340 SB EN
(7D3) CLEAR2
MODE
74LS32
S5 @ A12
7B2 MODE SELECT
OPEN = SEC CHANNEL
CLOSED = CODE TURN
J1 6 CC
DATA SET RDY
(NOT USED BY DISPLAY)
J2 6 CC
J2 20 CD
DATA TERM RDY
322
J1 20 CD
DATA TERMINAL RDY
J2 8 CF
EXTENSION PORT
J2 11 SA
320 EXTENSION SEC XMIT DATA
CARRIER DETECT
(9B3) BREAK
74LS10
TERM SEC XMIT
379
J1 11 SA
SEC XMIT DATA
8 CF
323 CARRIER DETECT
74LS13
325 SET RTS
(2C1) CC80
326 RTS
314 RTS
74LS112
S5 @ A12
202 SW
103 SW
LOCAL SW
12C2 SB EN
338
74LS00
(12C4) MODE
337 SEC RECV DATA
(12C2) SB EN
330 CLR RTS
74LS11
J1 12 SB
SEC RECV DATA
(10A3) THRE
(10B3) TRE
74LS08
1Ø3
J2 12 SB
EXTENSION PORT
J2 4 CA
EXTENSION PORT
321 EXTENSION RTS
J1 4 CA
REQ TO SEND
(7D3) CLEAR4
(9A1) KEY CLR
74LS04
74LS08
INF CLR
318
INTERFACE CONTROL
SIZE C
CODE IDENT NO. 98438
DWG NO. 12947/
LTR
SCALE
- 5 BD
SHEET 12
12947/



PROPRIETARY LEGEND

EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE		-5 BD	SHEET 13

129471

PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THIS DRAWING AND SPECIFICATIONS, ALL INFORMATION CONTAINED HEREIN, AND ALL RIGHTS IN THE INVENTIONS DISCLOSED THEREIN WHETHER OR NOT PATENTABLE, ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.

LTR	SHEET 14
DWG NO. 129471 -5 BD	
SIZE C	CODE IDENT NO. 98438
SCALE	

CLOCK PERIOD = 91.8577 nsec, FREQUENCY = 10.8864 MHZ

DC0
DC1
DC2
DC3

DOT COUNTER

VIDEO S.R. LOAD PERIOD = 643.0039 nsec, FREQUENCY = 1.5552 MHZ

1 CHAR
VIDEO TIME

CC0
CC1
CC2
CC3
CC4
CC5
CC6
CC7

POSITION COUNTER

PERIOD = 61.7284 μsec
FREQ = 16.2000 KHZ

LCCLK

COLINTER RETRACE
CBLIF RETRACE
VIDEO RETRACE

HDRIVE

PULSE WIDTH = 24.434 μsec
NOTE: HDRIVE STARTS ONE CHAR TIME (643 nsec) AFTER LAST VIDEO

LC0
LC1
LC2
LC3

LINE COUNTER

PERIOD = 555.555 μsec, FREQUENCY = 1.8000 KHZ

1 ROW TIME

ROW COUNTER

50 HZ OPERATION

RC0
RC1
RC2
RC3
RC4
RC5

PERIOD = 20ms
FREQ = 50 HZ

50 HZ VDRIVE — EDGES CLOCKED W/HDRIVE RISE

60 HZ OPERATION

RC0
RC1
RC2
RC3
RC4
RC5 (ALWAYS LOW DURING 60HZ OPERATION)

PERIOD = 16.667 msec, FREQ = 60 HZ

60 HZ VDRIVE — CLOCKED W/HDRIVE RISE

ADM-3 TIMING DIAGRAM

APPENDIX C

REVISIONS				
SYM	SHEET	DESCRIPTION	APPROVED	DATE

NOTE

1. INSTALL OPTION PACKAGE "A" (SEE SH 3) ON P.C. BOARD 129460 IF OPTION 1, 2, 3, OR 5 ARE INDICATED.

RECORD OF REVISION STATUS OF EACH SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

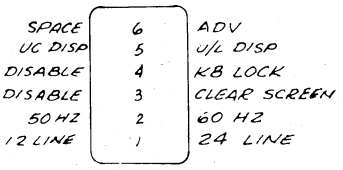
		DR	
		CHK	
		DSGN	
		ENGR	
		PROJ	
		REL	
	ADM-3	APP'D	
DASH NO.	NEXT ASSY	APP'D	
APPLICATION		DO NOT SCALE DRAWING	

LEAR SIEGLER, INC.
ELECTRONIC INSTRUMENTATION DIVISION, ANAHEIM, CALIF.

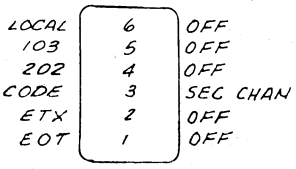
CONFIGURATION CONTROL - ADM-3

CODE IDENT NO	SIZE		REV
98438	B	129502	
SCALE			SHEET 1 OF 8
			DISTR

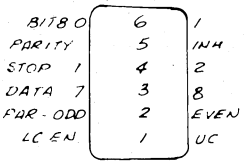
@A6

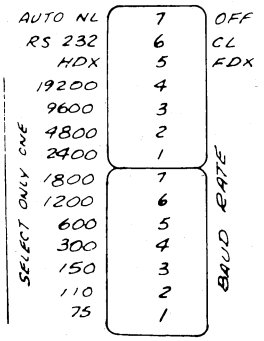


@A10



KEYBOARD





CODE IDENT NO.	SIZE		REV
98438	B	129502	
		SHEET 2	

OPTION PACKAGE A

PARTS LIST

FIND NO.	QTY REQD				PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1				✓		FOR 24 LINE			
2			✓			FOR 12 LINE			
3									
4			2	2	CA-18S-10SD	SOCKET	CIRCUIT ASSY	K6, L6	
5			2	3	CA-16S-10SD	"	" "	J8, H8 (24 LINE) CONN J6	
6			1	1	CA-24S-10SD	"	" "	J7	
7									
8			1	1	22-02-2051	CONNECTOR	MOLEX	NEAR CONN J2	A
9			1	1	22-02-2041	"	"	"	A
10									
11									

A. REMOVE TABS

THIS OPTION IS MANDITORY FOR ANY 129460 WHICH WILL CONTAIN OPTIONS 1, 2, 3 OR 5

CODE IDENT NO.	SIZE		REV
98438	B	129502	
		SHEET 3	

OPTION 1 LOWER CASE

PARTS LIST

FIND NO.	QTY REQD				PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
			/B	/A					
1				✓	1A	LOWER CASE - 12 LINE			
2			✓		1B	LOWER CASE - 24 LINE			
3									
4									
5			1	1	129323-02	CHAR GEN		J7	
6			2	1	128348-4102	RAM		J8, H8(1B)	
7									
8									
9									

INSTALL PARTS PER 129460
SEE NOTE 1 ON SHT 1

OPTION 2 ANSWER BACK

PARTS LIST

FIND NO.	QTY REQD			2	PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1				✓	2	ANSWER BACK			
2									
3				1	129489-01	P.C. BOARD ASSY			
4									
5				2	CA-D-18P02-261-CC-014	DIP INTERCONNECT	CIRCUIT ASSEMBLY		
6									
7				2	4(.123)-20 x 5/16 LG	SCREW - PLASTITE, HEX WASH HD, SLOTTED, STL, CAD PL	CONTINENTAL SCREW CO.		
8									
9									

REMOVE 2 157 I.C.'S AT L6 & K6 AND INSTALL ON F/N 3
INSTALL F/N 3 UNDER MAIN P.C. BOARD WITH F/N 7 SCREWS
INTERCONNECT WITH F/N 5 TO L6 & K6 ON MAIN BOARD
SEE NOTE 1 ON SHT 1

CODE IDENT NO.	SIZE		REV
98438	B	129502	
		SHEET 4	

OPTION 3 NUMERIC KEY PAD

PARTS LIST

FIND NO.	QTY REQD 3	PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1	✓	3				
2						
3						
4						
5	1		CABLE			
6	1	129490-01	NUMERIC KEY PAD ASSY			
7						
8						
9						

ROUTE CABLE (F/N 5) THRU BOTTOM VENTILATION HOLE
SEE NOTE 1 ON SHT 1

OPTION 4 DISPLAY TEST

PARTS LIST

FIND NO.	QTY REQD 4	PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1	✓	4				
2						
3						
4	1	MSS-104D	SWITCH	ALCO		
5						
6						
7						
8						
9						

CODE IDENT NO.	SIZE		REV
98438	B	129502	
		SHEET 5	

OPTION 5 EXTENSION PORT CURRENT LOOP

PARTS LIST

FIND NO.	QTY REQD 5	PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1	✓	5	EXT. PORT C.L.			
2						
3						
4	1	129488-01	P.C. BOARD ASSY			
5						
6						
7						
8						
9						

INSTALL IN SOCKETS NEAR J2 CONNECTOR
SEE NOTE 1 ON SHT 1

OPTION 6 SPLIT BAUD RATE

PARTS LIST

FIND NO.	QTY REQD 6	PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1	✓	6	SPLIT BAUD RATE			
2						
3						
4	–					
5	1	CTS 235-1	SWITCH, 12 POS	CTS		
6						
7						
8						
9						

INSTALL SWITCH PER 129460
CUT ETCH AT 75 BAUD SWITCH
(SEE ENGINEERING)

CODE IDENT NO.	SIZE		REV
98438	B	129502	
		SHEET 6	

OPTION 11 230 VOLT AC, EUROPEAN

PARTS LIST

FIND NO.	QTY REQD 11	PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1	✓	11				
2						
3						
4	1	129458-05	TRANSFORMER			
5						
6	1	129455-05	POWER CORD			
7						
8	1	129456-05	NAMEPLATE			
9						

OPTION 12 230 VOLT AC, AUSTRALIAN

PARTS LIST

FIND NO.	QTY REQD 12	PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1	✓	12				
2						
3						
4	1	129458-05	TRANSFORMER			
5						
6	1	129455-07	POWER CORD			
7						
8	1	129456-05	NAMEPLATE			
9						

CODE IDENT NO.	SIZE		REV
98438	B	129502	
		SHEET 7	

OPTION 21 CABLE

PARTS LIST

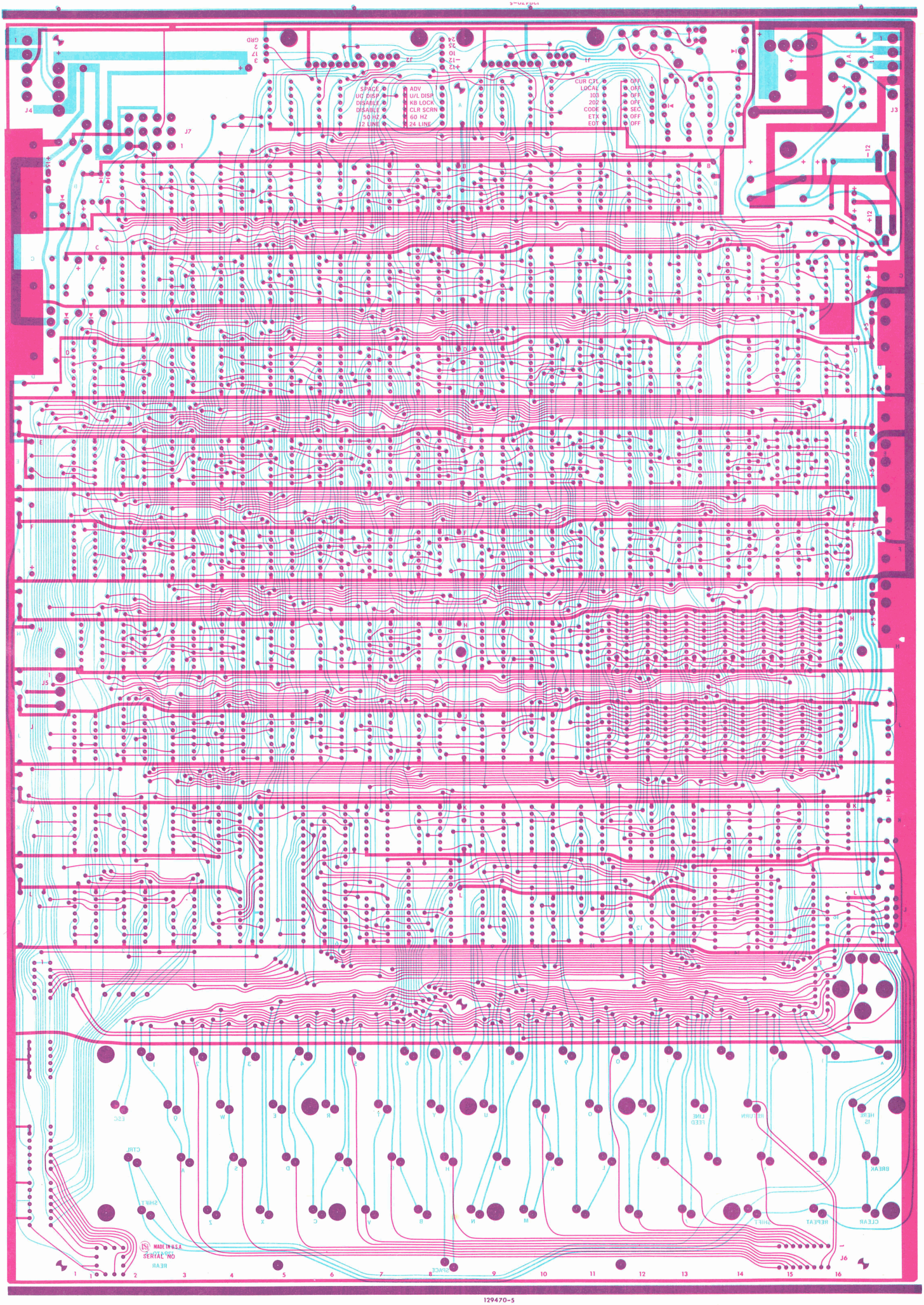
FIND NO.	QTY REQD				PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
				21					
1				✓	-21				
2									
3									
4				1	129316-11	CABLE			
5									
6									
7									
8									
9									

OPTION

PARTS LIST

FIND NO.	QTY REQD				PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1									
2									
3									
4									
5									
6									
7									
8									
9									

CODE IDENT NO.	SIZE		REV
98438	B	129502	
		SHEET 8	


SPACE
UC DISP
DISABLE
DISABLE
50 HZ
12 LINE
ADV
U/L DISP
KB LOCK
CLR SCRN
60 HZ
24 LINE
CUR CTL
LOCAL
103
202
CODE
ETX
EOT
OFF
OFF
OFF
OFF
SEC
OFF
OFF
J4
J7
J3
J5
J6
MADE IN U.S.A.
SERIAL NO

129470-5

LEAR SIEGLER, INC.

ELECTRONIC INSTRUMENTATION DIVISION
DATA PRODUCTS

714 NORTH BROOKHURST STREET
ANAHEIM, CALIFORNIA 92803
PHONE (714) 774-1010