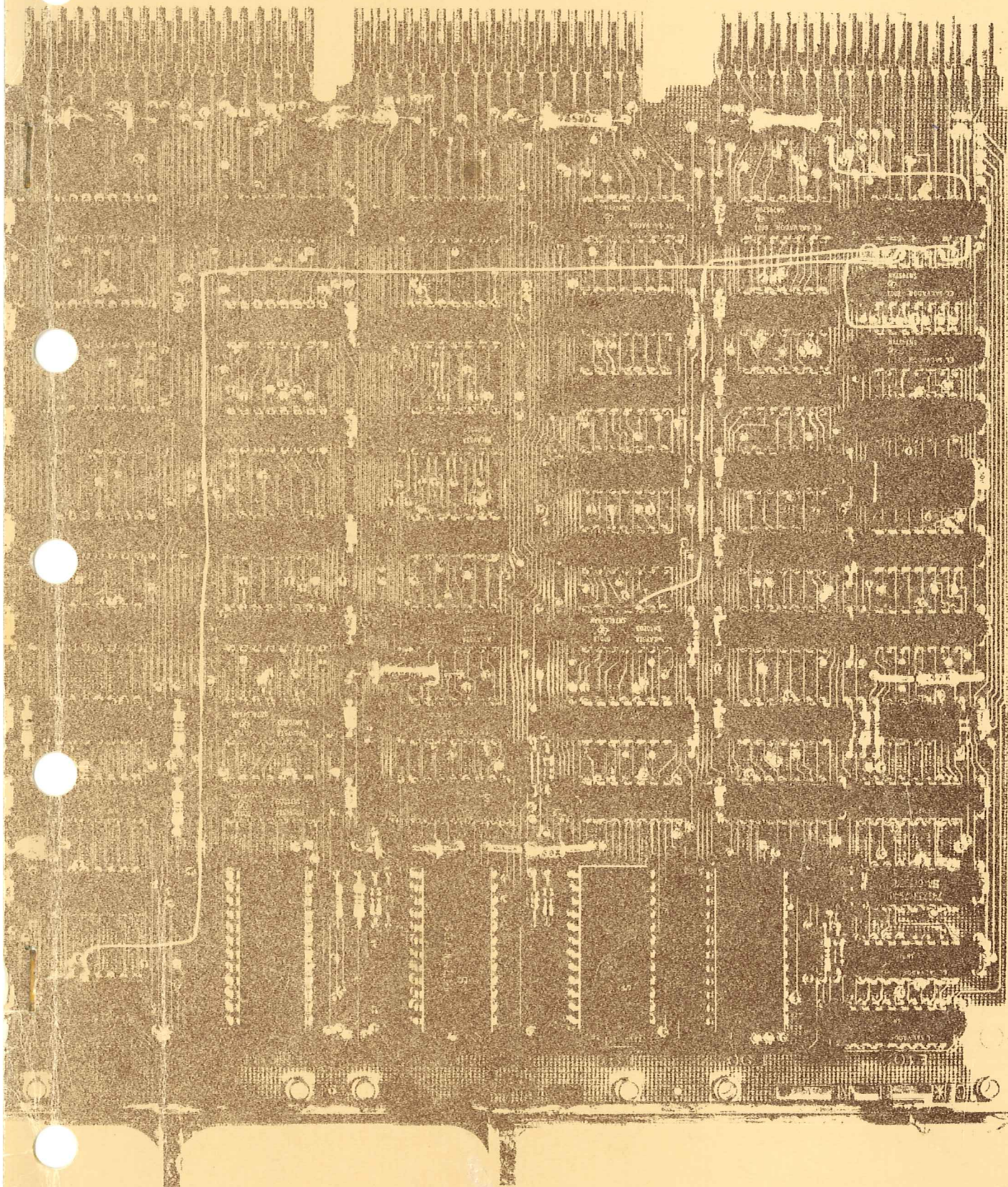


RM MASSBUS Adapter

Technical Description Manual

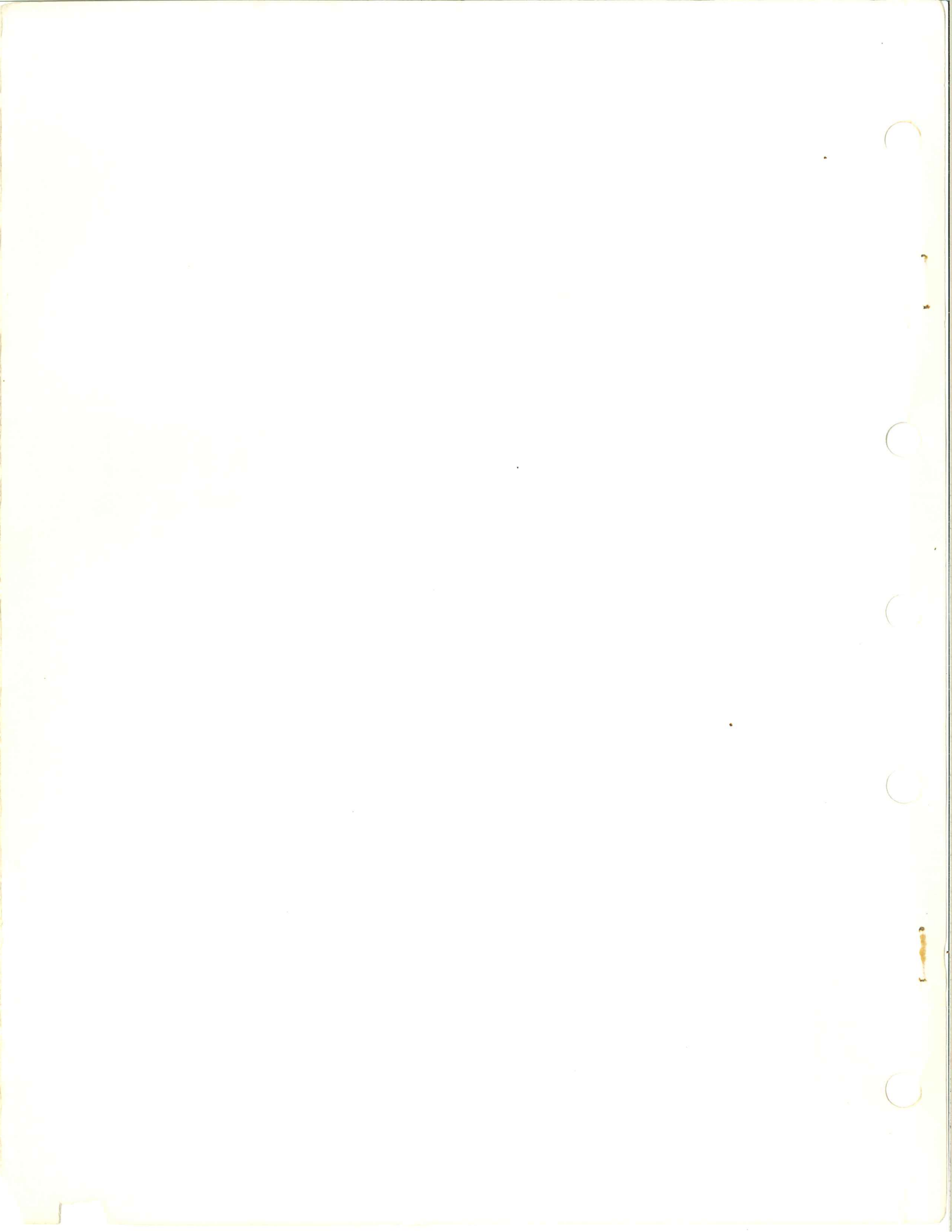


6-1
5-26
3-40

7-3
6-7
3-7

13-8
10-7
3-7

9
13-4
14-5



EK-RMADA-TD-001

RM MASSBUS ADAPTER
TECHNICAL
DESCRIPTION
MANUAL

digital equipment corporation ● colorado springs, colorado

First Edition, October 1980

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CONTENTS

CHAPTER 1 INTRODUCTION		Page
1.1	GENERAL.....	1-1
1.2	RM ADAPTER DESCRIPTION.....	1-1
1.2.1	Function.....	1-1
1.2.2	Physical Description.....	1-1
1.3	SINGLE-PORT AND DUAL-PORT CAPABILITY.....	1-3
1.4	ADAPTER MODIFICATIONS.....	1-3
1.5	RELATED DOCUMENTATION.....	1-4
CHAPTER 2 INTERFACE-LEVEL DESCRIPTION		
2.1	SYSTEM OVERVIEW.....	2-1
2.2	PHYSICAL CABLE LOCATIONS.....	2-1
2.3	MASSBUS INTERFACE.....	2-1
2.3.1	Data Lines.....	2-3
2.3.2	Control Lines.....	2-4
2.4	DRIVE INTERFACE.....	2-6
2.4.1	Interface Cable A.....	2-6
2.4.2	Interface Cable B.....	2-9
2.5	POWER SEQUENCE CABLE.....	2-10
CHAPTER 3 TECHNICAL DESCRIPTION		
3.1	INTRODUCTION.....	3-1
3.2	ADAPTER CIRCUIT MODULES.....	3-1
3.2.1	Control Interface (IF).....	3-1
3.2.2	Data Sequencer (DS).....	3-2
3.2.3	Control Sequencer (CS).....	3-2
3.2.4	Drive Interface.....	3-2
3.2.5	Port A MASSBUS Transceiver.....	3-2
3.2.6	Port B MASSBUS Transceiver.....	3-2
3.3	POWER-UP SEQUENCING.....	3-2
3.4	INITIALIZE SEQUENCE.....	3-5
3.5	DEVICE SELECTION.....	3-5
3.6	REGISTER SELECTION.....	3-8
3.7	HANDSHAKE CONTROL.....	3-8
3.7.1	Register Write.....	3-8
3.7.2	Register Read.....	3-13

CONTENTS (Cont)

		Page
3.8	DETAILED BLOCK DIAGRAM.....	3-13
3.8.1	Port Transceivers	3-13
3.8.2	RM Adapter Registers	3-16
3.8.3	RM Adapter PLAs	3-17
3.8.3.1	ATA Control/Request PLA.....	3-17
3.8.3.2	Error Sum PLA (IF9).....	3-18
3.8.3.3	ATA, RMR, INIT PLA (IF6)	3-18
3.8.3.4	Sector/Track PLA (DS11)	3-18
3.8.3.5	CYL/AOE/IAE PLA (DS12).....	3-18
3.8.4	Command Sequencer (CS1, CS2).....	3-18
3.8.5	Read/Write Sequencer (CS4).....	3-20
3.8.6	Data Sequencer Data Paths.....	3-22
3.8.6.1	Write Path	3-22
3.8.6.2	Read Path	3-22
3.9	COMMAND EXECUTION	3-22
3.9.1	Command Immediate Execution.....	3-25
3.9.1.1	No-Op Command	3-25
3.9.1.2	Drive Clear Command	3-25
3.9.1.3	Release Command.....	3-26
3.9.1.4	Read-In Preset Command	3-26
3.9.1.5	Pack Acknowledge Command.....	3-26
3.9.2	Command Immediate with ATA Execution.....	3-26
3.9.2.1	Offset Command	3-26
3.9.2.2	Return-To-Centerline Command.....	3-27
3.9.2.3	Recalibrate Command.....	3-28
3.9.2.4	Seek Command.....	3-28
3.9.2.5	Search Command	3-28
3.9.3	Data Transfer Command Execution.....	3-28
3.9.3.1	Write Data Execution.....	3-36
3.9.3.2	Read Data Execution	3-36
3.9.3.3	Write Header and Data Execution.....	3-39
CHAPTER 4	RM ADAPTER APPLICATIONS	
4.1	INTRODUCTION.....	4-1
4.2	ADAPTER DIFFERENCES.....	4-1
4.3	RM02 ADAPTER/DISK DRIVE COMBINATION	4-2
4.4	RM03 ADAPTER/DISK DRIVE COMBINATION	4-7
4.5	RM05 ADAPTER/DISK DRIVE COMBINATION	4-12
4.6	RM80 ADAPTER/DISK DRIVE COMBINATION	4-17
4.6.1	Backplane Jumper Connection	4-20
4.6.2	Adapter Register Summary.....	4-20
APPENDIX A	ADAPTER MODULE COMPATIBILITY	

FIGURES

Figure No.	Title	Page
1-1	RM Adapter Physical Configurations	1-2
1-2	Single-Port, Multi-Drive Connections.....	1-4
1-3	Dual-Port, Multi-Drive Connections.....	1-5
1-4	RM Adapter Backplane Layout.....	1-6
2-1	Disk Drive Interfaces.....	2-1
2-2	Disk Subsystem Cabling	2-2
2-3	MASSBUS Interface Lines.....	2-3
2-4	Cable A Interface Lines.....	2-7
2-5	Cable B Interface Lines.....	2-9
2-6	Power Sequence Cable Configuration	2-10
3-1	Adapter Circuit Module Locations.....	3-1
3-2	Typical Power-Up Configuration.....	3-2
3-3	Power-Up Sequence Flowchart.....	3-4
3-4	Initialize Sequence Functional Block Diagram	3-6
3-5	Drive Selection Functional Block Diagram	3-7
3-6	Register Selection Block Diagram.....	3-9
3-7	Register Read/Write Handshaking Block Diagram.....	3-10
3-8	Handshake Timing for Register Write	3-12
3-9	Handshake Timing for Register Read	3-14
3-10	RM Adapter Block Diagram	3-15
3-11	Attention Control/Request PLA	3-17
3-12	Command Sequencer Block Diagram.....	3-19
3-13	Read/Write Sequencer Block Diagram.....	3-21
3-14	Write Data Flow Path Diagram.....	3-23
3-15	Read Data Flow Path Diagram.....	3-24
3-16	Recalibrate Command Flowchart.....	3-29
3-17	Seek Command Flowchart.....	3-30
3-18	Search Command Flowchart	3-32
3-19	Data Transfer Command Flowchart.....	3-34
3-20	Write Data Command Flowchart	3-37
3-21	Read Data Command Flowchart	3-38
3-22	Write Header and Data Command Flowchart.....	3-40
4-1	RM02 Adapter Configuration	4-2
4-2	Adapter Position in Cabinet.....	4-3
4-3	RM02 Drive-Type Jumper Connections	4-4
4-4	RM02 Adapter Register Summary.....	4-5
4-5	RM03 Adapter Configuration	4-7
4-6	Adapter Position in Cabinet.....	4-8
4-7	RM03 Drive-Type Jumper Connections	4-9
4-8	RM03 Adapter Register Summary.....	4-10
4-9	RM05 Adapter Configuration	4-12
4-10	Adapter Position(s) in Cabinet.....	4-13

FIGURES (Cont)

Figure No.	Title	Page
4-11	RM05 Drive-Type Jumper Connections	4-14
4-12	RM05 Adapter Register Summary.....	4-15
4-13	RM80 Adapter Configuration	4-17
4-14	Adapter Position in Cabinet.....	4-18
4-15	RM80 Drive-Type Jumper Connections	4-19
4-16	RM80 Jumper Location on Adapter Backplane	4-20
4-17	RM80 Adapter Register Summary.....	4-21

TABLES (Cont)

Table No.	Title	Page
1-1	RM Adapter Circuit Modules	1-3
2-1	RM Adapter Registers.....	2-5
2-2	Selection of Control Commands	2-8
2-3	Tag Line and Bus Bit Decoding Arrangement.....	2-9
4-1	RM02 Adapter Circuit Modules.....	4-4
4-2	RM03 Adapter Circuit Modules.....	4-9
4-3	RM05 Adapter Circuit Modules.....	4-14
4-4	RM80 Adapter Circuit Modules.....	4-19
A-1	Adapter Module Assignments.....	A-1

CHAPTER 1 INTRODUCTION

1.1 GENERAL

This manual describes the RM adapter and its operation in a disk subsystem. The first three chapters contain a general description of the adapter and the last chapter outlines modifications that are necessary to make the adapter compatible with specific disk drives.

1.2 RM ADAPTER DESCRIPTION

1.2.1 Function

The RM adapter is an electronic assembly used to interface MASSBUS controllers with disk drive units. The adapter performs the functions listed below.

- Acts as an interface between the RH controller and the disk drive electronics
- Converts the controller command requests into drive command sequences
- Establishes the mode of operation (single-port or dual-port)
- Monitors and reports drive status to the RH controller

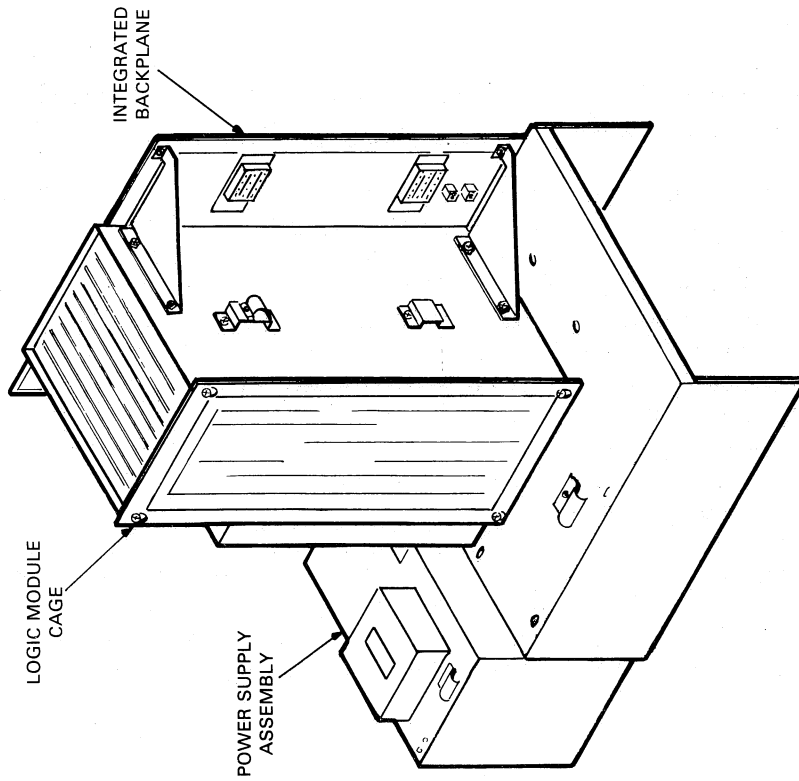
1.2.2 Physical Description

The RM adapter consists of an integrated backplane designed to accept up to eight plug-in circuit modules, a card cage, several circuit modules, and a power supply assembly.

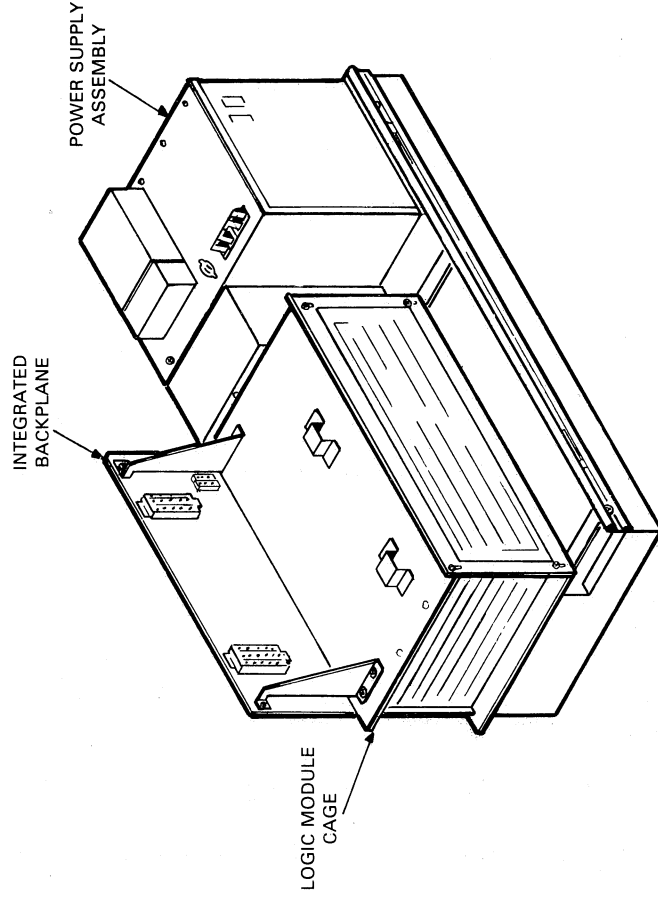
There are two physical adapter configurations (Figure 1-1). In Figure 1-1A, the adapter backplane and associated card cage are shown mounted vertically on the RM adapter chassis. Up to eight circuit modules are plugged into the card cage. The actual number of modules depends upon whether the adapter is set up for single-port or dual-port operation. (Refer to Paragraph 1.3 for an explanation of dual porting.) Table 1-1 lists the six types of modules used in the adapter. Port-A and port-B modules are used in pairs. Access to the circuit modules is gained through a removable cover on the end of the logic cage.

The power supply assembly is next to the card cage on the adapter chassis. The power supply provides all of the necessary dc operating voltages (-15 volts and $+5$ volts) for the logic circuits and includes an ac outlet to provide power for disk drive operation. Cooling for the power supply circuitry is provided by a fan built into the power supply chassis.

The second RM adapter configuration is shown in Figure 1-1B. In this configuration, the integrated backplane and the card cage are shown mounted in a horizontal position on the adapter chassis. Because of this arrangement, the physical dimensions of this unit are different from those in the configuration described previously. Except for these physical differences, however, both adapters are the same.



(A) BACKPLANE AND CARD CAGE MOUNTED VERTICALLY



(B) BACKPLANE AND CARD CAGE MOUNTED HORIZONTALLY

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Figure 1-1 RM Adapter
Physical Configurations

Table 1-1 RM Adapter Circuit Modules

Module No.	Name
M5923	Port B asynchronous
M5923	Port B synchronous
M5922	Port A asynchronous
M5922	Port A synchronous
M7686/M7686-YA*	Control interface
M7685/M7685-YA/M8685*	Data sequencer
M7687	Drive interface
M7684	Control sequencer

* Refer to Appendix A for module compatibility information.

1.3 SINGLE-PORT AND DUAL-PORT CAPABILITY

The RM adapter can operate as either a single-port or dual-port device.

In the single-port configuration, two M5922 port A transceiver modules are used and the adapter interfaces a single RH controller as shown in Figure 1-2. Up to eight disk drives can be connected to a single controller.

The dual-port configuration uses two additional port transceiver modules (M5923) and the adapter is connected as shown in Figure 1-3 to permit time-shared access of the disk drive by two RH controllers. A port select switch (located either on the front edge of the backplane or on the front door of the drive cabinet) permits selection of operation on port A, port B, or a programmable mode which allows either port to be accessed (as determined by program control).

1.4 ADAPTER MODIFICATIONS

The RM adapter can be used with a variety of disk drive models. However, because of differences in disk storage capacities, spindle speeds, number of tracks, and single and dual port options, some wiring alterations (such as changes in jumper connections) are required to make the RM adapter compatible with specific drive models. Special drive features, such as skip sectoring, also necessitate minor modifications. These modifications are usually made at the factory prior to shipment.

Figure 1-4 illustrates the layout of the RM adapter backplane and identifies some of the areas where wiring changes are required. The J1 area, for example, is where specific drive-type operating characteristics such as spindle speed, byte capacity, and single or dual port capabilities are selected.

Jumper connections are made in the J4 area to establish the drive serial number. The serial number provides a means of distinguishing between different drives with identical characteristics that are connected to the same controller.

Other modifications include the use of a special data sequencer module and in some instances the addition of a jumper connection on the adapter backplane wiring to alter the number of cylinder addresses that can be selected by the associated disk drive.

In addition to hardware modifications, there are a number of software changes related to bits in the RM adapter registers and the functions of various register bits.

Chapter 4 describes the specific modifications required to make the RM adapter compatible for operation with each applicable disk drive unit.

1.5 RELATED DOCUMENTATION

For additional information on the RM adapter subsystem, refer to the user's guide, service manual, and field maintenance print set covering the specific disk drive involved.

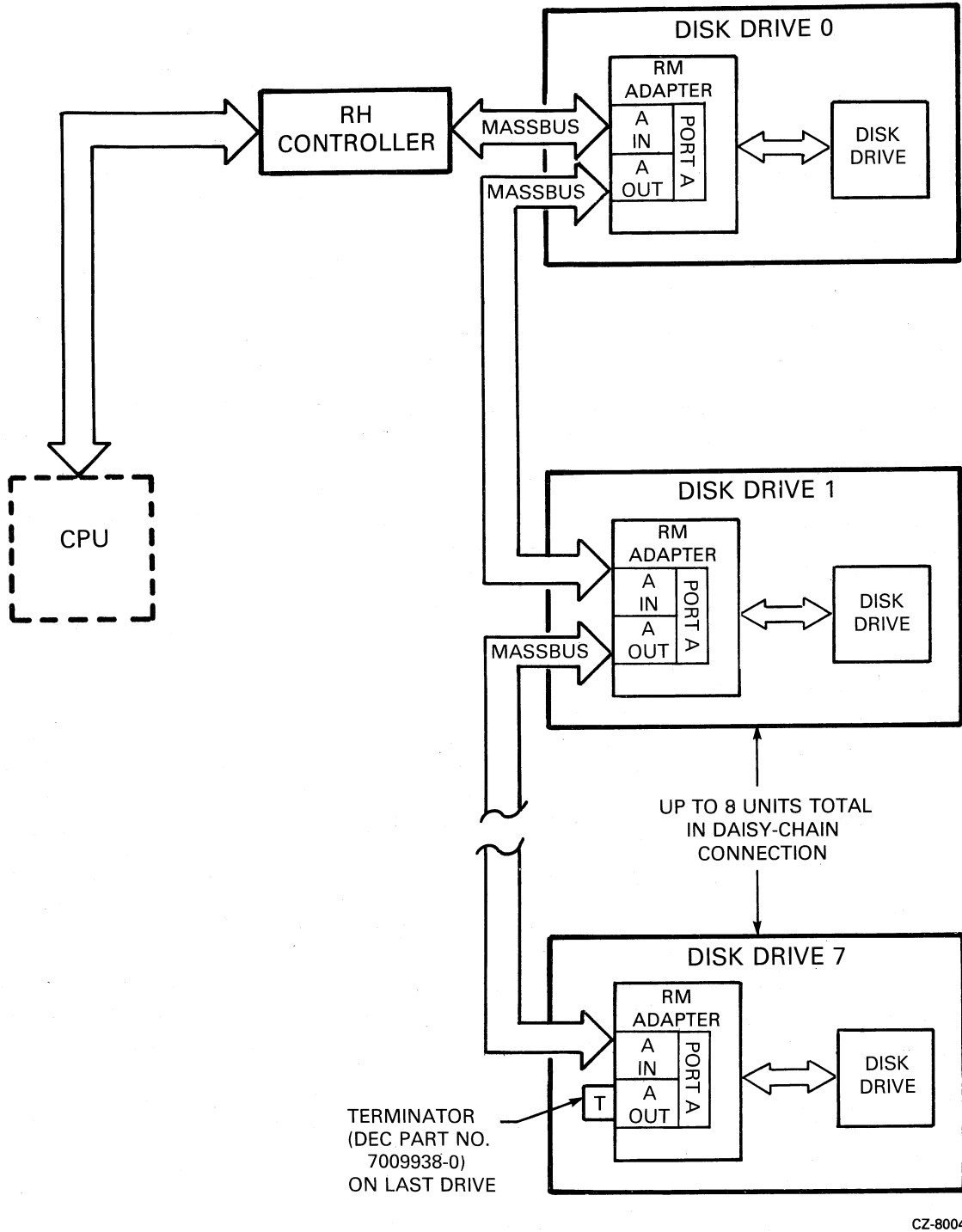
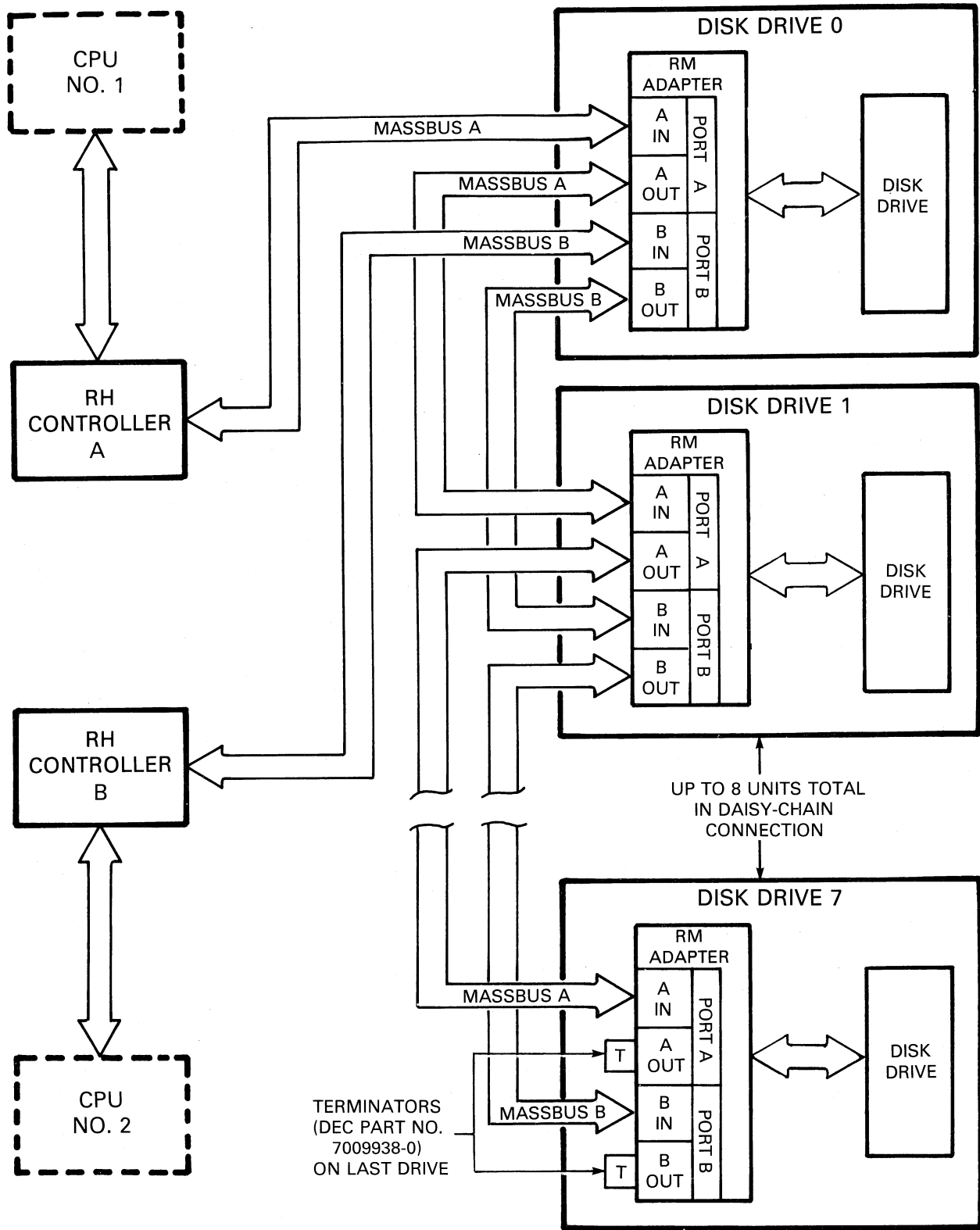


Figure 1-2 Single-Port, Multi-Drive Connections



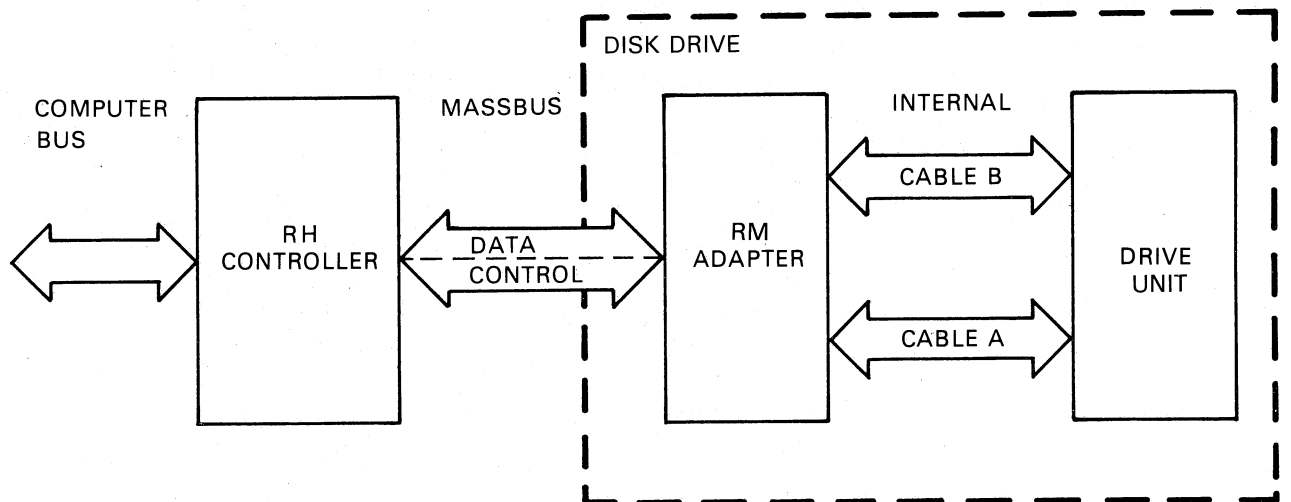
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Figure 1-3 Dual-Port, Multi-Drive Connections

CHAPTER 2 INTERFACE-LEVEL DESCRIPTION

2.1 SYSTEM OVERVIEW

There are two major interfaces in an RM disk subsystem. One is the MASSBUS interface between the RH controller and the RM adapter. The other is the internal interface between the RM adapter and the drive unit itself. Figure 2-1 shows these two interfaces but does not show interfaces for dual-port or multi-drive configurations since the only difference is an increased amount of external cabling.



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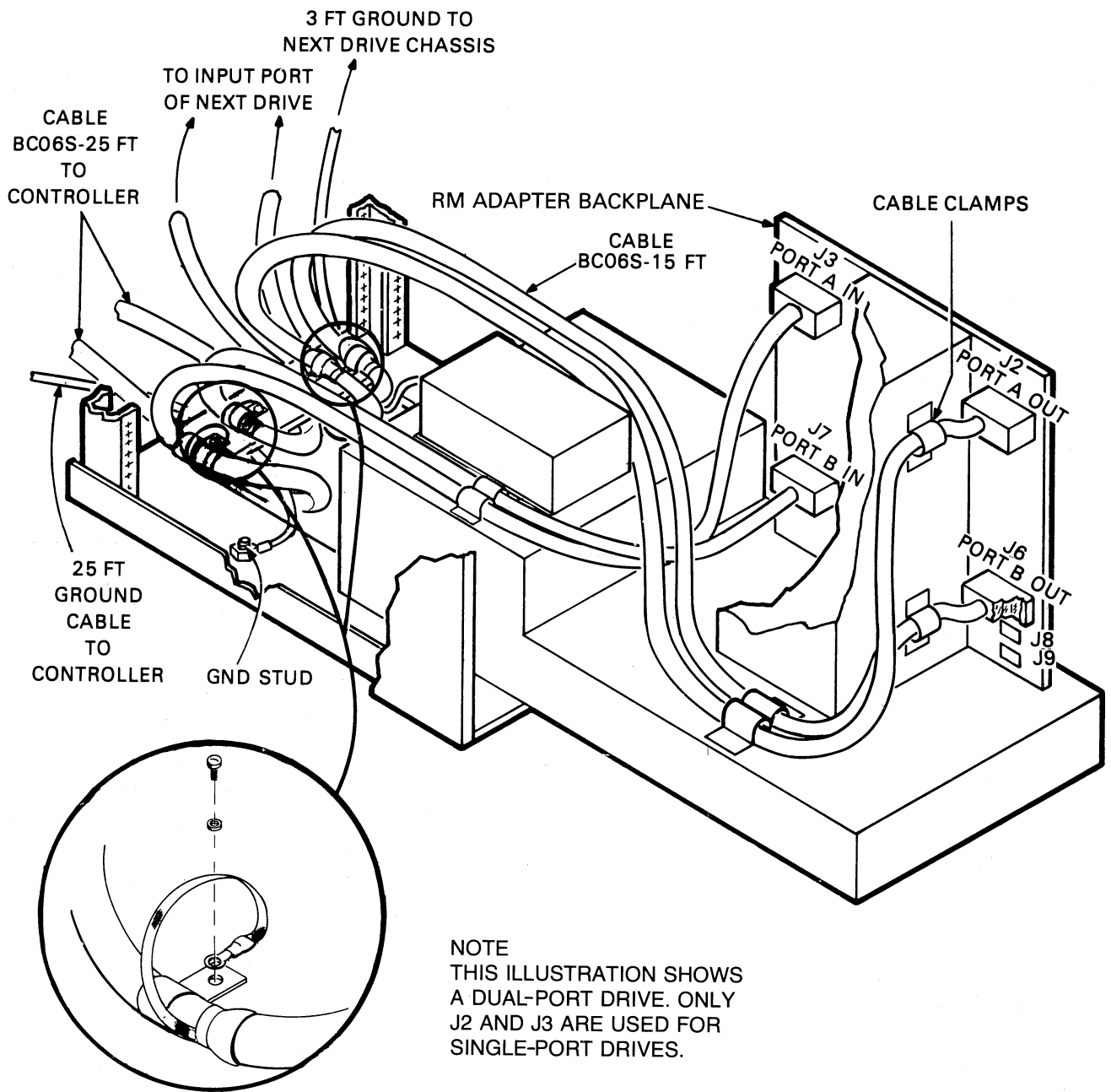
Figure 2-1 Disk Drive Interfaces

2.2 PHYSICAL CABLE LOCATIONS

Figure 2-2 shows the routing of all the cables connecting the RH controller, RM adapter, and drive unit in an RM disk drive subsystem. The MASSBUS interface cable is described in Paragraph 2.3. The drive interface cables (cable A and cable B) are described in Paragraph 2.4, and Paragraph 2.5 contains a description of the power sequence cabling.

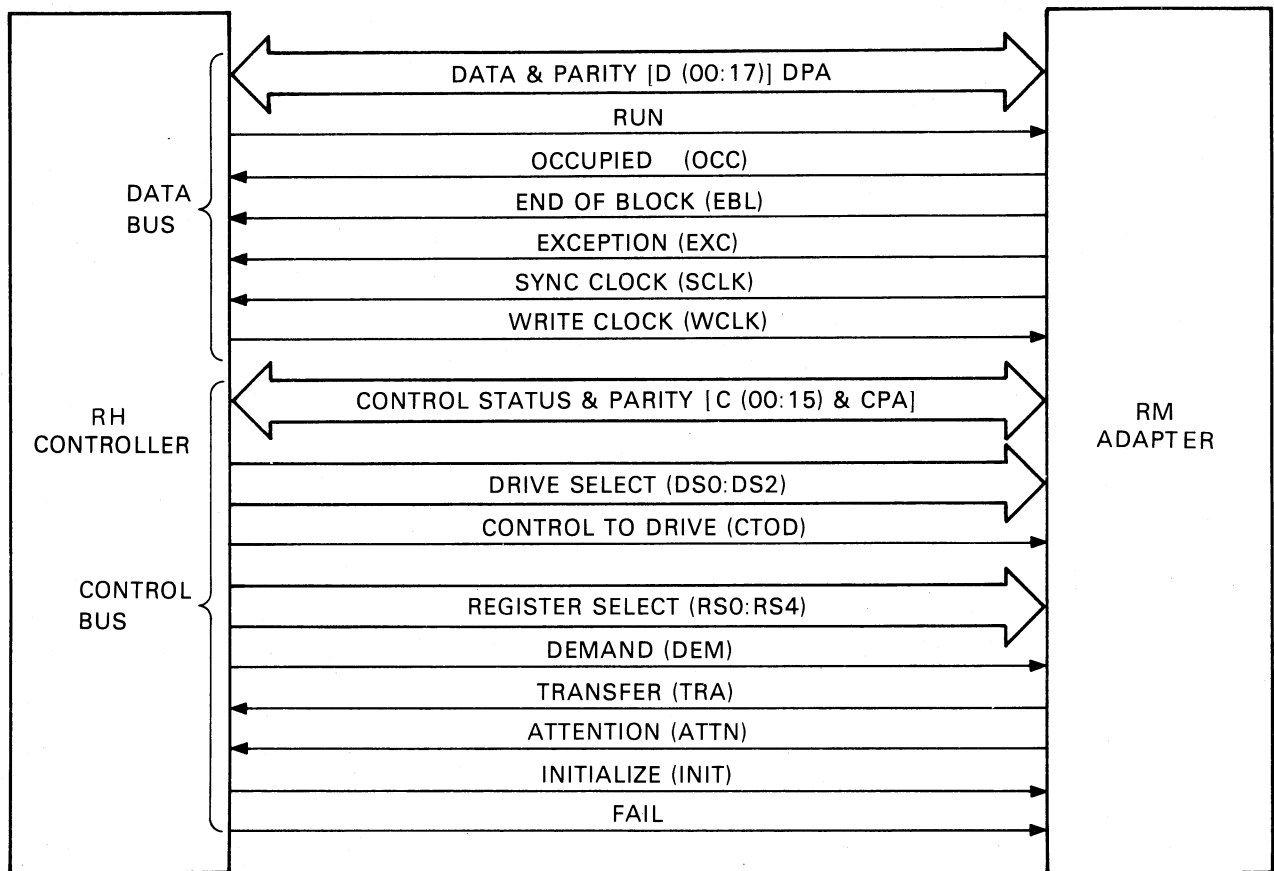
2.3 MASSBUS INTERFACE

The controller-to-adapter interface, or MASSBUS (Figure 2-3), consists of two sections; data bus lines and control bus lines.



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Figure 2-2 Disk Subsystem Cabling



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Figure 2-3 MASSBUS Interface Lines

2.3.1 Data Lines

The data bus section of the MASSBUS consists of a 19-bit (18 data bits plus parity bit) parallel data path and 6 control lines (Figure 2-3). The data bus lines are described in the following paragraphs.

Parallel Data Path – consists of an 18-bit data path designated D00 through D17 and an associated parity bit (DPA). The data path is bidirectional and employs odd parity. Data is transmitted synchronously, using a clock generated in the RM adapter and synchronized with timing from the disk drive.

RUN – asserted by the RH controller to connect the adapter to the data bus. This action occurs after a data transfer command has been decoded by the RH controller. RUN is strobed by the adapter logic on the trailing edge of the END OF BLOCK (EBL) pulse at the end of each sector. If RUN is still asserted at this time, the data transfer continues for the next sector; if it is negated, the data transfer is terminated.

OCCUPIED (OCC) – generated by the RM adapter to indicate “data bus busy.” The adapter asserts OCC as soon as a valid data transfer command is decoded and the RUN line is asserted. Errors may prevent the adapter from executing a command. An error circuit in the RH controller times out in these cases since there is no assertion of OCC or of SYNC CLOCK (SCLK). This condition then causes the MISSED TRANSFER (MXF) error to be set in the RH controller. OCC is negated when GO is negated at the end of the data transfer command.

END OF BLOCK (EBL) – asserted by the adapter at the end of each sector (the next word clock after the two ECC words). EBL is asserted prior to the normal time for the last SCLK pulse during error conditions that make it necessary to terminate operations immediately. In such cases, the data transfer is terminated prior to the end of the sector.

EXCEPTION (EXC) – asserted by the RM adapter when an abnormal condition occurs in the drive during a data transfer. The RM adapter asserts this signal to indicate an error during a data transfer command (read, write, or write-check). EXC is asserted at or prior to assertion of EBL and is negated at the negation of EBL.

SYNC CLOCK (SCLK) and WRITE CLOCK (WCLK) – timing signals used to control the strobing of data in the RH controller and/or the RM adapter. During a read operation, the RH controller strobcs the data lines when SCLK is negated and the adapter changes the data when SCLK is asserted. During a write operation, the RH controller receives SCLK and echos it back to the RM adapter as WCLK. When WCLK is asserted, the data lines are strobed; when WCLK is negated, the RH controller changes the data on the data lines. These signals are synchronized with the timing from the servo surface of a platter in the drive.

2.3.2 Control Lines

The control bus section of the MASSBUS consists of a 17-bit (16 bits plus parity bit) parallel control and status data path, and 14 control lines (Figure 2-3). The control bus lines are described in the following paragraphs.

Parallel Control – consists of a 16-bit parallel data path designated C00 through C15 and an associated parity bit (CPA). The control lines are bidirectional and employ odd parity.

Drive Select Lines [DS (0:2)] – transmit a 3-bit binary code from the RH controller to select a particular drive. The drive responds when the logical address plug on the front panel of the drive corresponds to the transmitted binary code.

CONTROLLER-TO-DRIVE (CTOD) Signal – generated by the RH controller to indicate the direction in which control and status information is to be transferred. For a controller-to-drive transfer, the RH controller asserts CTOD. For a drive-to-controller transfer, the RH controller negates this signal.

Register Select Lines [RS (0:4)] – transmit a 5-bit binary code from the RH controller to the adapter of the selected disk drive. The binary code selects one of the remote adapter registers.

NOTE

The sixteen registers in the RM adapter are designated by RM codes 00₈ through 07₈ and 10₈ through 17₈. These codes are also referred to as the octal MASSBUS addresses. Table 2-1 lists these registers and their addresses. If a register code higher than 17₈ is detected by the RM adapter hardware, an illegal register (ILR) error will occur.

DEMAND (DEM) Signal – asserted by the RH controller to indicate that a register read/write is to take place on the control bus lines. For a controller-to-drive register read/write, DEM is asserted by the RH controller when data is present on the control bus. For a drive-to-controller transfer, DEM is asserted by the RH controller to request register data and is negated when the register data has been strobed off the control bus lines. In both cases, the RS, DS, and CTOD signals are generated and allowed to settle before assertion of DEM.

Table 2-1 RM Adapter Registers

MASSBUS Address (Octal)	Register	Mnemonic	Type
00	Control (shared with controller)	RMCS1	Read/write
01	Drive status	RMDS	Read only
02	Error 1	RMER1	Read/write
03	Maintenance 1	RMMR1	Read/write
04	Attention summary	RMAS	Read/write
05	Desired sector/track address	RMDA	Read/write
06	Drive type	RMDT	Read only
07	Look ahead	RMLA	Read only
10	Serial number	RMSN	Read only
11	Offset	RMOF	Read/write
12	Desired cylinder address	RMDC	Read/write
13	Holding	RMHR	Read only
14	Maintenance 2	RMMR2	Read only
15	Error 2	RMER2	Read/write
16	ECC position	RMEC1	Read only
17	ECC pattern	RMEC2	Read only

TRANSFER (TRA) Signal – asserted by the RM adapter associated with the selected drive in response to DEM. For a controller-to-drive register read/write, TRA is asserted after the register data has been strobed and is negated after DEM is negated. For a drive-to-controller transfer, TRA is asserted after the data has been gated onto the bus lines and negated after the negation of DEM is received.

Attention (ATTN) Line – shared by all disk drives attached to an RH controller. It may be asserted by the adapter in any of the drives as a result of an abnormal condition or status change. An ATA status bit is set whenever the ATTN line is asserted. ATTN may be asserted due to any of the conditions listed below.

- When an error occurs and no data transfer is taking place (ATTN is asserted immediately)
- At the completion of a data transfer command if an error occurred during the data transfer (ATTN is asserted at the end of the data transfer)
- At the completion of a mechanical motion function (seek, recalibrate, etc.) or a search command
- As a result of the medium-on-line (MOL) bit changing states (except in the unload operation). In the dual-controller configuration, a change in the state of MOL causes the assertion of ATTN to both controllers.

The ATA bit is cleared by the actions listed below.

- Asserting initialize (INIT) on the MASSBUS (affects all drives)
- Executing a drive clear command
- Causing INIT by a system initiate operation
- Writing a 1 into the attention summary register (in the bit position for this particular drive), which clears the ATA bit, but does not clear the error
- Writing a valid command (with the GO bit asserted) into the RMCS1 register if no error occurs. Note that clearing the ATA bit of one drive does not always cause the ATTN line to be negated because other drives may also be asserting the line.

NOTE

There are three cases in which ATA is not reset when a command is written into the control register (with the GO bit set). These are: (1) if a control bus parity error occurs during the register write, (2) if an error was previously set, or (3) if an illegal function (ILF) code is written.

INITIALIZE (INIT) Signal – asserted by the RH controller to perform a system reset of all logic circuits. It is asserted when a 1 is written into the CLR bit (bit 05 of the status register in the RH controller) and when the system issues an initiate function. When an RM adapter receives the INIT pulse, the adapter immediately aborts the execution of any current command and performs all actions described for the drive clear command.

NOTE

In the dual-controller configuration, an INIT pulse is honored only from the controller that has seized the drive, or from either controller if the drive is in the unseized state.

FAIL Signal – indicates that a power-fail condition has occurred in the RH controller. While FAIL is asserted, the RM adapter logic inhibits reception of the INIT and DEM signals.

2.4 DRIVE INTERFACE

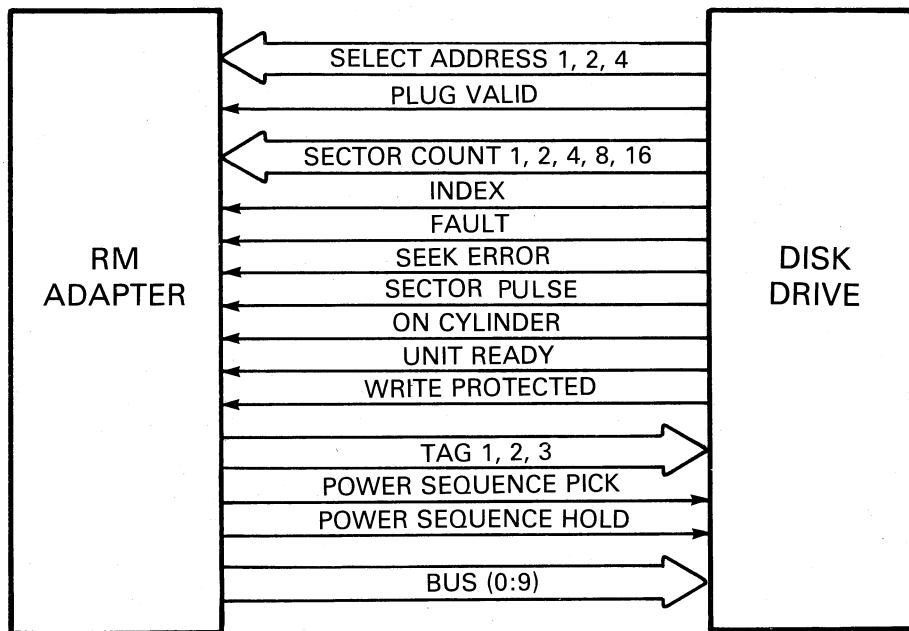
The internal signal interface between the RM adapter and the drive unit is accomplished through two cables as shown in Figure 2-1. These cables, designated cable A and cable B, route data command sequences and synchronizing timing signals between the RM adapter and the drive.

2.4.1 Interface Cable A

The cable A signal lines are shown in Figure 2-4 and are described in the following paragraphs.

Select Address (1, 2, 4) – binary encoded lines that contain a logical number representing the address of one of the eight possible disk drives. The address value (0 through 7) is front-panel selectable by means of a removable logical address plug.

The binary code on these lines is present at least 200 nanoseconds prior to the PLUG VALID signal becoming asserted and remains present until at least 200 nanoseconds after the unit number plug is removed.



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Figure 2-4 Cable A Interface Lines

PLUG VALID – indicates that a unit number plug (switch cap) is inserted in the front panel.

SECTOR COUNT 1, 2, 4, 8, 16 – represents binary encoded lines that contain a logical number corresponding to the address of the sector presently under the heads. The value changes on the leading edge of the sector pulse and clears on the leading edge of the index pulse. The maximum count is 29_{10} in 18-bit format or 31_{10} in 16-bit format.

INDEX Pulse – indicates the beginning of sector 0 and occurs once per revolution.

FAULT Signal – indicates that a fault has occurred in the drive. A fault condition immediately inhibits the write capability to prevent data destruction.

The fault condition may be cleared by a drive clear command or the fault clear switch on the operator panel (providing the fault no longer exists).

SEEK ERROR Signal – indicates that the drive is unable to complete a seek within the specified time or that the carriage has moved to a position outside the recording area. A seek error can also occur when an address greater than the maximum track address is selected and the invalid address is not detected.

A return-to-zero seek command clears the seek error condition, returns the heads to cylinder 0, and enables an on-cylinder signal to the RH controller.

SECTOR Pulse – indicates the beginning of each sector. This pulse is typically 1.25 microseconds wide.

ON CYLINDER – indicates that the servo has positioned the heads over the desired track. It is cleared with any instruction causing carriage movement.

UNIT READY – indicates that the following drive conditions have occurred.

- Disk is revolving at correct speed
- Heads are loaded
- No drive fault condition exists

WRITE PROTECTED – asserted when the WRITE PROTECT switch on the drive front panel is pressed. The WRITE PROTECT signal prevents data from being written onto the disk. Attempting any write function causes a write lock error (WLE) indication.

TAG 1, 2, 3 – selects one of three functions and also permits the bit pattern on the ten bus lines to be decoded. Only one tag line at a time is asserted. When tag 1 is asserted, the bus lines contain a binary number that represents the cylinder address to which the heads are to move. Tag 2 decodes bits 0 through 4 of the bus lines to select the drive head. Tag 3 selects one of five possible drive control commands as shown in Table 2-2.

Table 2-2 Selection of Control Commands

Command	Function
Bit 0 (Write Gate)	Enables the write driver, allowing data to be written by the selected head onto the disk.
Bit 1 (Read Gate)	Enables the read circuits and allows data read by the selected head to be sent to the RH controller.
Bit 2 (Servo Offset Plus)	Enables the read/write head to offset slightly from the nominal on-cylinder position to a new position (typically 250 microinches) toward the spindle.
Bit 3 (Servo Offset Minus)	Enables the read/write head to offset from the nominal on-cylinder position to a new position (typically 250 microinches) away from the spindle.
Bit 4	Not used.
Bit 5	Not used.
	NOTE
	This seek takes significantly longer than a normal seek to track 0, and should only be used for recalibration.
Bit 6 (RTZ)	Causes the heads to be positioned over track 0, resetting the head register, clearing the seek error flip-flop, and resetting the cylinder address register.
Bits 7-9	Not used.

Table 2-3 gives the tag line and bus bit decoding arrangement.

Table 2-3 Tag Line and Bus Bit Decoding Arrangement

Bus Bit	Tag 1 Asserted Cylinder Address	Tag 2 Asserted Head Select	Tag 3 Asserted Control Select
0	1	1	Write gate
1	2	2	Read gate
2	4	4	Servo offset plus
3	8	8	Servo offset minus
4	16	Not used*	Not used
5	32	Not used*	Not used
6	64	Not used*	Return to zero
7	128	Not used	Not used
8	256	Not used	Not used
9	512	Not used	Not used

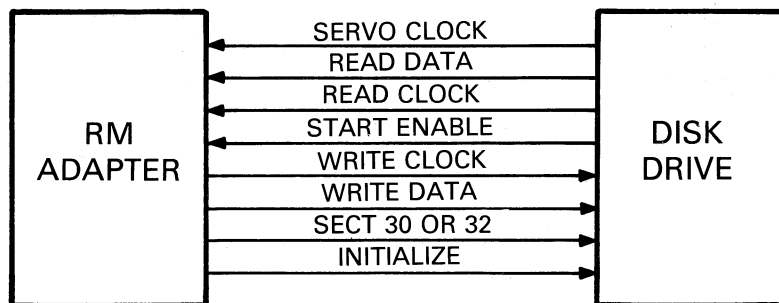
* May or may not be used depending upon number of heads

Power Sequence Pick and Power Sequence Hold – A ground on both of these lines causes the drive to energize if the following conditions have already been met.

- Both ac and dc power are on
- Start switch is turned on
- No other drive in the chain is attempting to start

2.4.2 Interface Cable B

The cable B signal lines are shown in Figure 2-5 and are described in the following paragraphs.



CZ-3078

Figure 2-5 Cable B Interface Lines

SERVO CLOCK – generates write clock and is used for data timing in the adapter. SERVO CLOCK is phase-locked and generated from the servo track bit pattern.

READ DATA Line – transmits data read from the disk.

READ CLOCK – strobes the read data from the drive to the adapter.

START ENABLE – indicates that the start switch has been activated.

WRITE CLOCK (WCLK) – strobes data from the adapter to the disk. The WRITE CLOCK is generated by the retransmission of the servo clock to the drive by the RM adapter during write data operations.

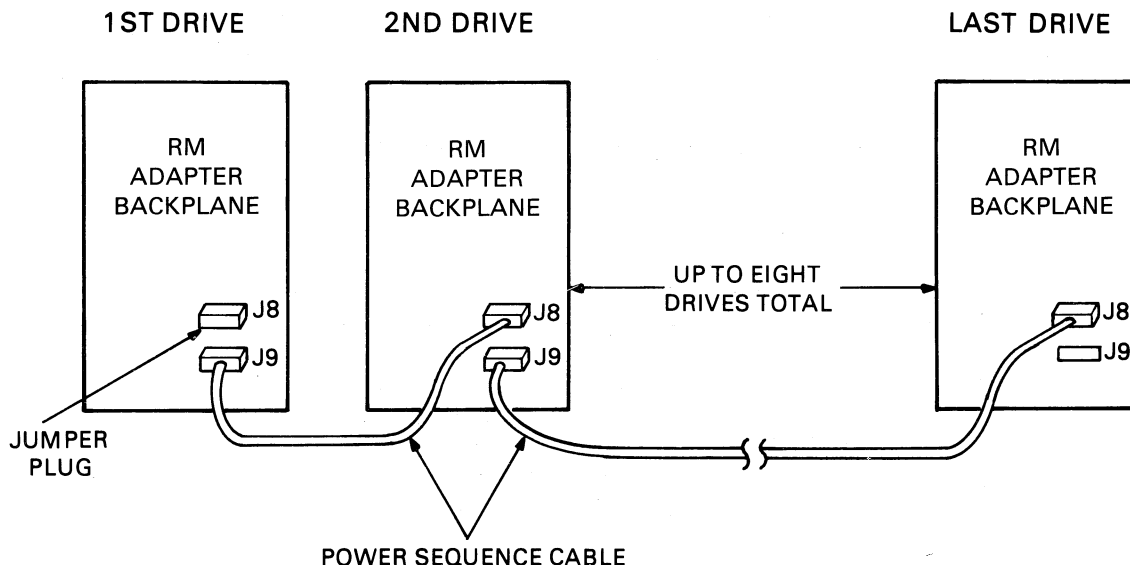
WRITE DATA Line – transmits data to be written on the disk.

SEC 30 OR 32 (Format) – configures the disk into 32 sectors per revolution when asserted. When not asserted, the configuration is for 30 sectors.

INITIALIZE (INIT) – clears all drive fault latches and seek error flip-flops (providing the fault no longer exists).

2.5 POWER SEQUENCE CABLE

The power sequence cable (Figure 2-6) prevents two or more drives from starting up simultaneously. This could happen, for example, if there is a power failure while several drives are running. If the power is restored before the drives are shut down, the current drawn by all the drive motors starting up could be enough to overload the building circuit breakers.



CZ-0265

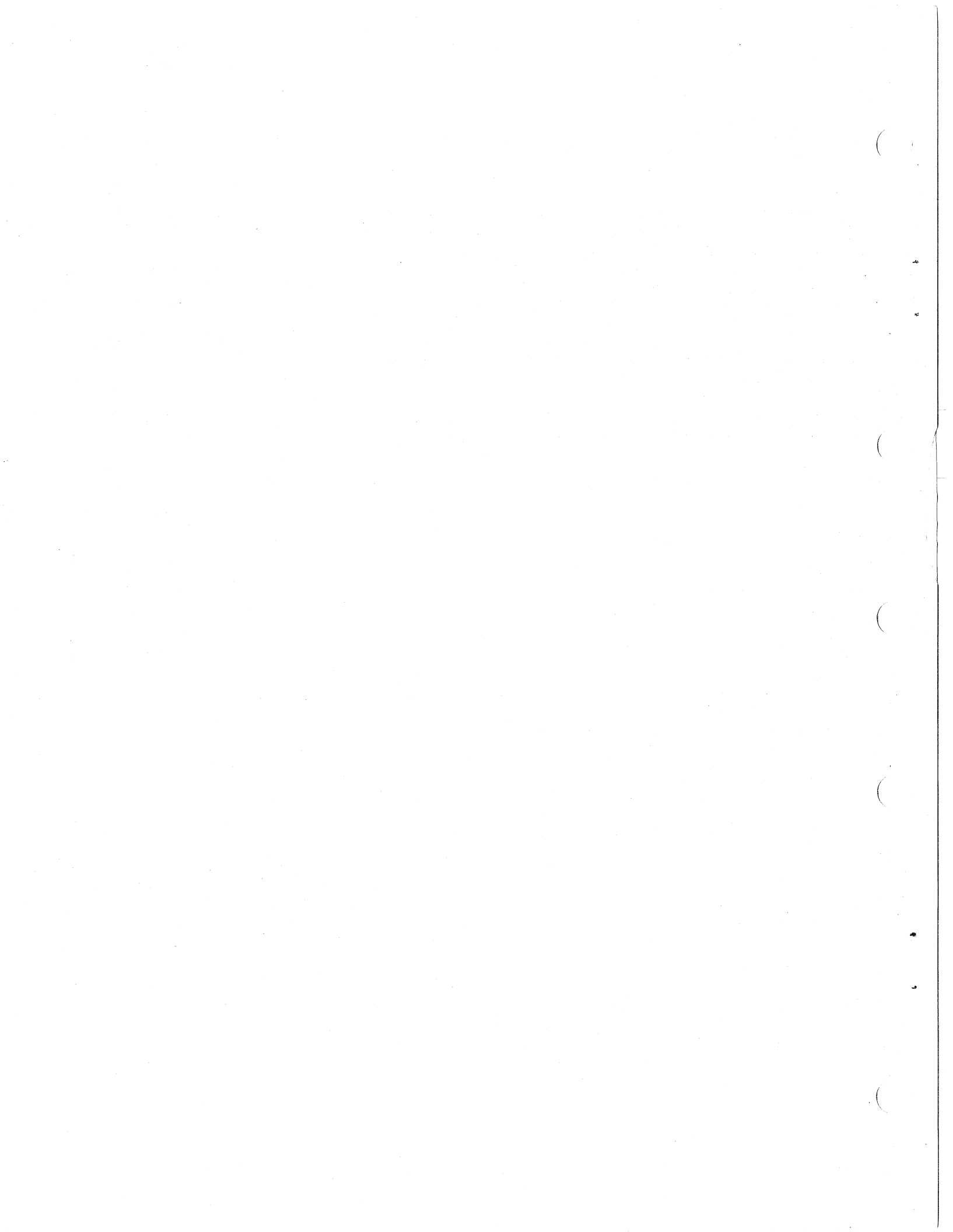
Figure 2-6 Power Sequence Cable Configuration

The cable consists of three lines: start in progress (SIP), grant, and ground. The SIP line is a parallel connection to all the drives on the power sequence cable. It is normally high. When a drive starts up, however, the drive pulls the SIP line low. No other drive will be able to start while the SIP line is low.

The grant line is connected in series through all the drives on the power sequence cable. The signal coming into a drive from the previous drive on this line is called GRANT-IN. The signal leaving a drive and entering the next drive is called GRANT-OUT. If a drive in the sequence is powered down, the grant line passes directly through that drive, so that GRANT-OUT always matches GRANT-IN. The first drive in the sequence has a jumper plug (Figure 2-6) that ties GRANT-IN to ground on the first drive. When a drive detects a low GRANT-IN, it can start if instructed to do so (assuming SIP is high).

While the first drive is going through its start cycle, it pulls its GRANT-OUT high. This is interpreted by the next drive in the sequence as a high GRANT-IN. Thus, the next drive cannot start up until the first drive has gone through its start-up cycle.

Any drive in the sequence may be stopped and then restarted, but only if all the drives before it are either running or powered down.



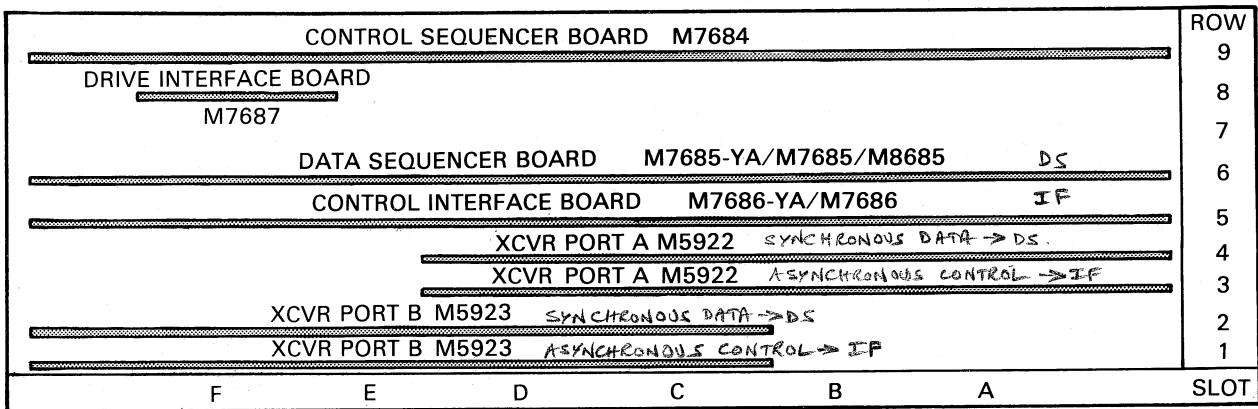
CHAPTER 3 TECHNICAL DESCRIPTION

3.1 INTRODUCTION

This chapter provides a technical description of the RM adapter. Each circuit module is described briefly and detailed block diagrams are used to illustrate the operation of various circuit elements. Command execution is described in detail with the aid of command flowcharts.

3.2 ADAPTER CIRCUIT MODULES

There are six different types of circuit modules in the RM adapter. Two of these, the port A MASSBUS transceiver module (M5922) and the port B MASSBUS transceiver module (M5923), are used in pairs. The other four modules, control interface (M7686/M7686-YA), data sequencer (7685/7685-YA/8685), control sequencer (M7684), and drive interface (M7687), are used individually in the RM adapter. Each of these boards is described briefly in the following paragraphs. Figure 3-1 shows the locations of the circuit modules in the logic card cage.



CZ-0308

Figure 3-1 Adapter Circuit Module Locations

3.2.1 Control Interface (IF)

The control interface module is used primarily for asynchronous MASSBUS handshaking and register transfer control. This circuit module also contains the RMAS, RMER1, RMER2, RMCS1, RMDT, RMDS, RMOF and RMHR registers. (Refer to Table 2-1.)

3.2.2 Data Sequencer (DS)

The data sequencer module controls the flow of data to or from the disk. The logic on this module includes bit-clock and word-clock generation logic, error correcting code logic, and cycle redundancy check logic. The RMDC, RMEC1, RMEC2 and RMDA registers are on this module.

3.2.3 Control Sequencer (CS)

The command sequencing logic on this module handles all command execution. Read/write sequencing also occurs on this board and the CS module contains the differential drivers and controls that handle data on cable A going to the drive. Registers RMMR1, RMMR2, RMSN and RMLA are on this module.

3.2.4 Drive Interface

The drive interface module is used primarily as an interface for information on cable B between the RM adapter and the drive unit. The information on this cable includes the read and write clocks and the data being transmitted.

3.2.5 Port A MASSBUS Transceiver

One of the two port A transceiver modules transmits asynchronous control signals between the MASSBUS and the IF module. The other module handles synchronous data between the MASSBUS and the DS module.

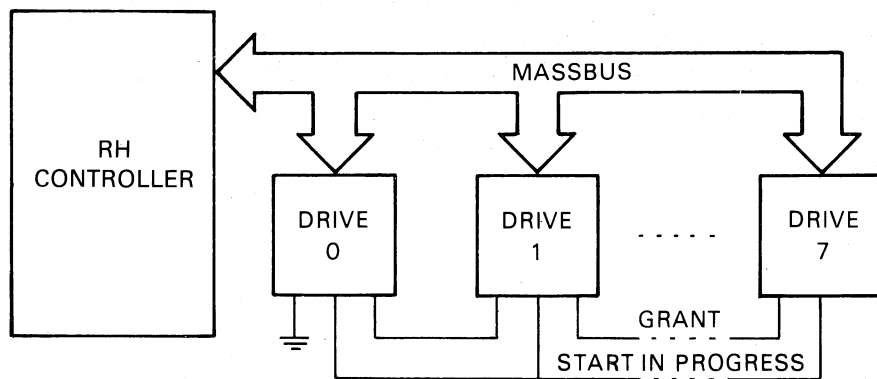
3.2.6 Port B MASSBUS Transceiver

Two port B transceivers are used when the disk drive is configured for dual-port operation. The two port B transceiver modules perform the same functions as the port A modules but are only active when the disk drive is in the port B mode.

3.3 POWER-UP SEQUENCING

In a multidrive installation, the power sequence cable that is connected between the backplanes carries three signals (GRANT-IN, GRANT-OUT, and START IN PROGRESS) used to control the power-up sequence. The power sequence cable is described in Paragraph 2.5 of this manual.

Figure 3-2 shows a typical system configuration. The grant line, which handles the GRANT-IN and GRANT-OUT signals, is connected serially through each drive. The START IN PROGRESS (SIP) line is common to all of the drives. Pin 1 of J8 on the backplane of the drive physically closest to the controller is grounded by a jumper plug (Figure 2-6). Thus, the grant signal initially appears low to all the drives on the power sequence cable.



CZ-0309

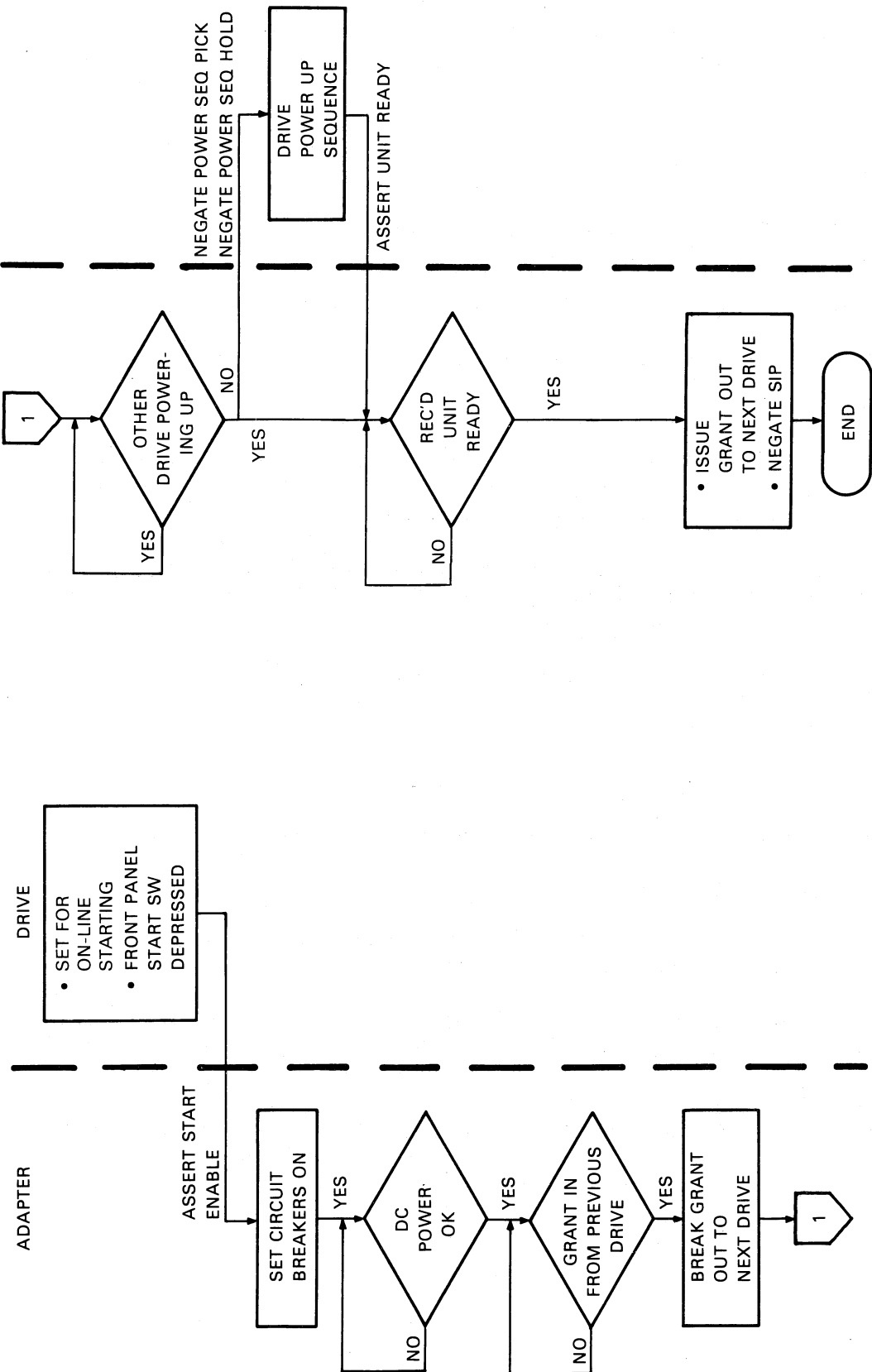
Figure 3-2 Typical Power-Up Configuration

The presence of a low GRANT-IN signal is one of two prerequisites for a drive to be able to start up. The other prerequisite (with respect to the power sequence cable) is that the SIP line be high. The SIP line is high until a drive begins its power-up sequence at which time the SIP line is pulled low. A low SIP line prevents all of the other drives from starting up.

Figure 3-3 shows the flow diagram for the power-up sequence. The sequence of events during power-up is described below.

1. With all drive switches in the appropriate position for on-line starting, the start enable line on cable B will assert when the front-panel START switch is pressed.
2. In the RM adapter, the conditions listed below are needed to start the sequence.
 - Power supply circuit breakers (CB1 and CB2) are set to ON
 - DC power is OK (from CS)
 - There is GRANT-IN signal from a drive closer to the controller than the drive trying to power up. If this is the first drive in the string, GRANT-IN will always be present because the line is grounded at the backplane.
3. The drive attempting to start tests the SIP line to see if another drive is in its power-up sequence. If another drive is already starting up, the drive attempting to start will wait for the other drive to finish its sequence.
4. If no other drive is starting up, this drive initiates the actions listed below.
 - Negates POWER SEQUENCE PICK to drive
 - Negates POWER SEQUENCE HOLD to drive
 - Asserts the SIP line to prevent other drives from trying to start-up
5. During the time the drive is starting up, it constantly tests for the UNIT READY signal.
6. Upon receipt of the UNIT READY signal, the RM adapter issues the GRANT-OUT signal to the next drive and negates the SIP line.
7. When the drive has completed its start-up cycle, UNIT READY is asserted to indicate that the spindle is up to speed, the heads are loaded, and no faults exist in the drive.

When UNIT READY is asserted, the drive has finished its start-up sequence and is considered "powered up". If, for some reason, the drive did not start, GRANT-OUT is sent to the other drives to allow them a chance to start. The drive continues sending GRANT-OUT until the fault that prevented its start-up is cleared. Then, a new start-up sequence is initiated in the drive.



CZ-0327

Figure 3-3 Power-Up Sequence Flowchart

When a drive is turned off following a successful start-up sequence, the actions listed below occur.

- The START ENABLE line is negated and both pick and hold lines are asserted.
- The start relay de-energizes but the GRANT-OUT signal is still passed along to the next drive.
- The drive starts in the normal manner after the START/RUN switch is pressed again.

NOTE

Even though a drive is stopped, other drives further out on the string can start-up because the grant line is passed through the powered-down drive.

3.4 INITIALIZE SEQUENCE

This sequence places the adapter and drive circuits in a known logic state. Figure 3-4 shows that the sequence starts with the receipt of the MASSBUS INIT signal through either port A or B transceivers.

The MASSBUS INIT signal (whether coming from port A or B) clears the ATA bit in the attention summary register (on the control interface module). The ATA/RMR/INIT PLA generates the signal INIT A/B. This signal goes to E83 (in Figure 3-4) in the control sequencer module and is converted to the MBA CLR signal. The MBA CLR signal performs the functions listed below.

- Clears bit 0 of RMMR1
- Sets on-latch flip-flop
- Clears the enable search latch
- Clears the ECC pattern register (RMEC2)
- Clears both error registers (RMER1 and RMER2)
- Clears any drive faults (if the fault has been removed)

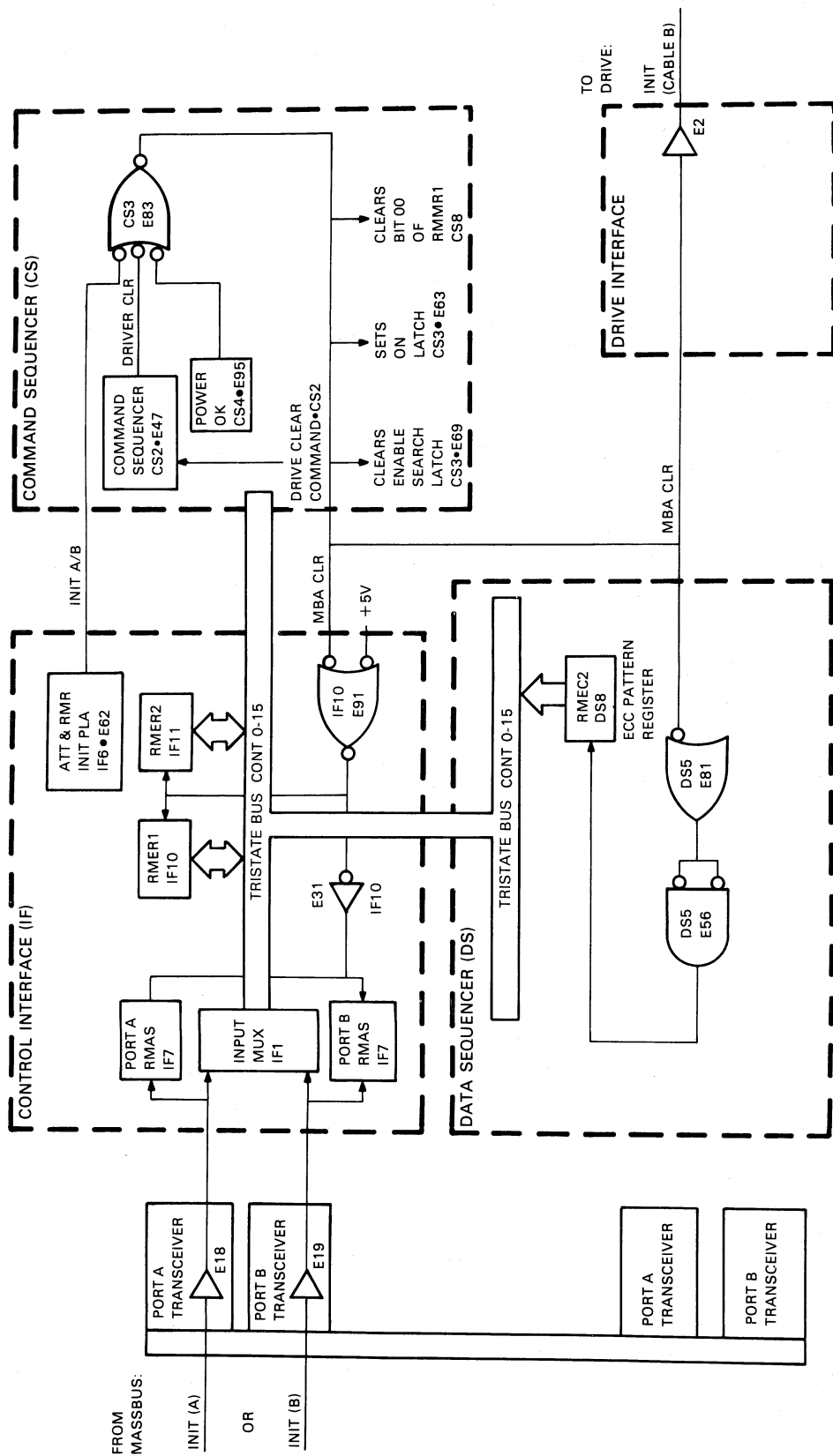
Note that POWER OK (generated at power-on time) or a drive clear command also generates the MBA CLR signal.

3.5 DEVICE SELECTION

This circuitry compares the drive select address (in control and status register 2, from the MASSBUS) with the unique code of the device address lines originating in the disk drive.

Figure 3-5 is a functional block diagram of the drive select circuitry. Note that the device select lines (DS0-DS2) utilize the port A and B transceivers and are passed on to the IF module as DRV ADDR 1, 2, 4. The drive address comparator that is used depends upon the port selected by the software. The other input to the comparator is from the disk drive and is available from interface cable A through the CS module. The actual disk address is the other input and originates at the front panel of the disk drive. The front panel has a coded logical address plug (indicating a number from 0 to 7) that is inserted into a socket. The plug output enables switches in the socket and produces three signals: DEV ADS 1, 2 and 4. The logical address plug generates an additional signal called PLUG EN. This signal enables the address comparators and indicates that a logical address plug has been properly inserted into the front panel of the drive.

When the DRIVE SELECT signal from the MASSBUS and DEV ADS signal from the drive match, the output from the address comparators will start the handshake sequence (see Paragraph 3.7), enabling register selection and access in the device.



MA-1672

Figure 3-4 Initialize Sequence Functional Block Diagram

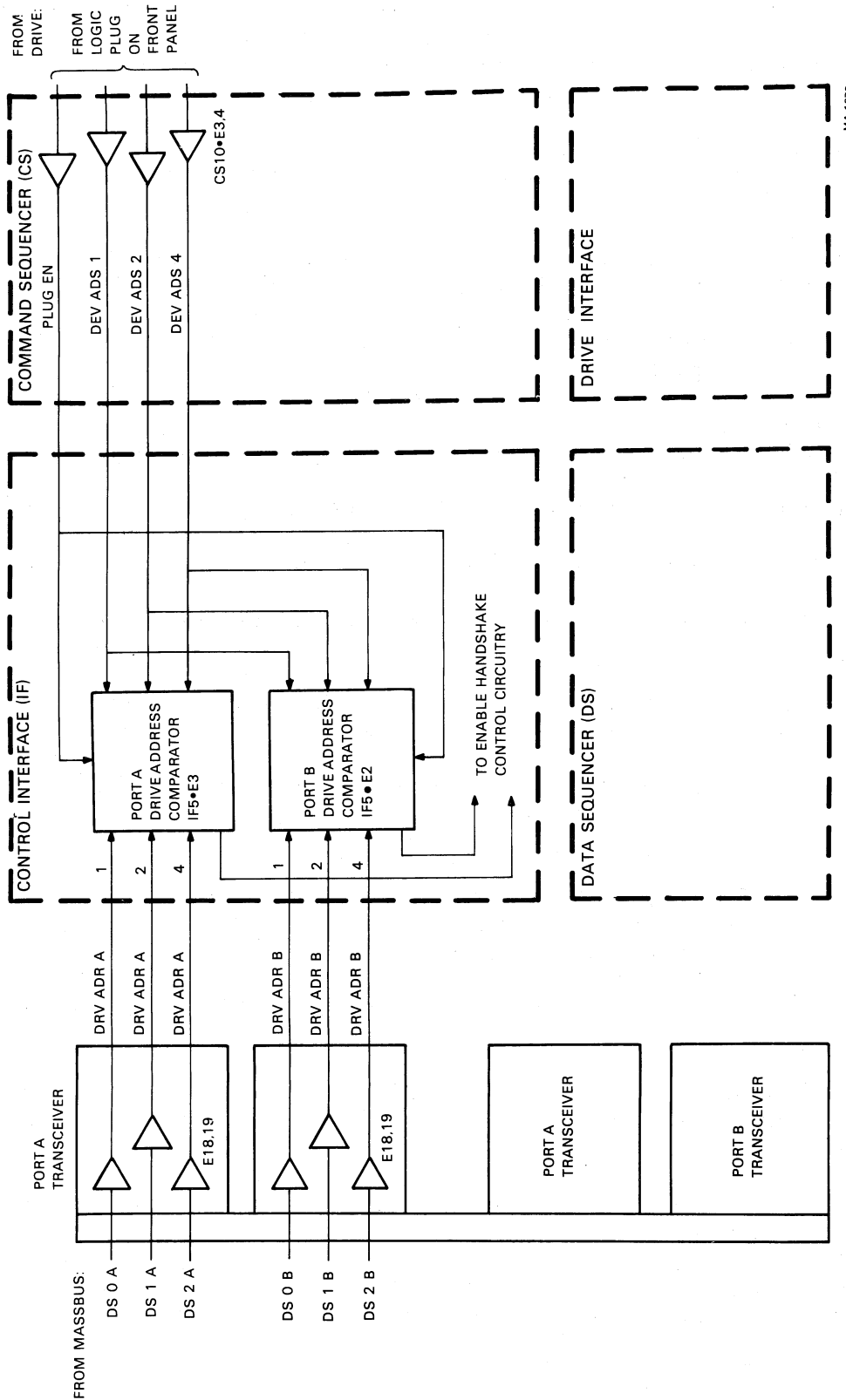


Figure 3-5 Drive Selection Functional Block Diagram

3.6 REGISTER SELECTION

The register selection circuitry (Figure 3-6) selects the RM adapter register desired by the software. The five register select lines come through the selected port transceiver and enter the control interface module. The register select lines are then routed to the ATA REQ logic and handshake control and register read/write circuits described in Paragraph 3.7.

3.7 HANDSHAKE CONTROL

These circuits (shown as a block diagram in Figure 3-7) establish the timing required during a register read or a register write.

Prior to the actual handshake sequence, the device selection logic compares the DRIVE SELECT signal with the device address and the port selection logic establishes which port is to be used.

The register information is routed to or from the selected register on the control bus lines. The control bus has 16 data lines and one parity line.

3.7.1 Register Write

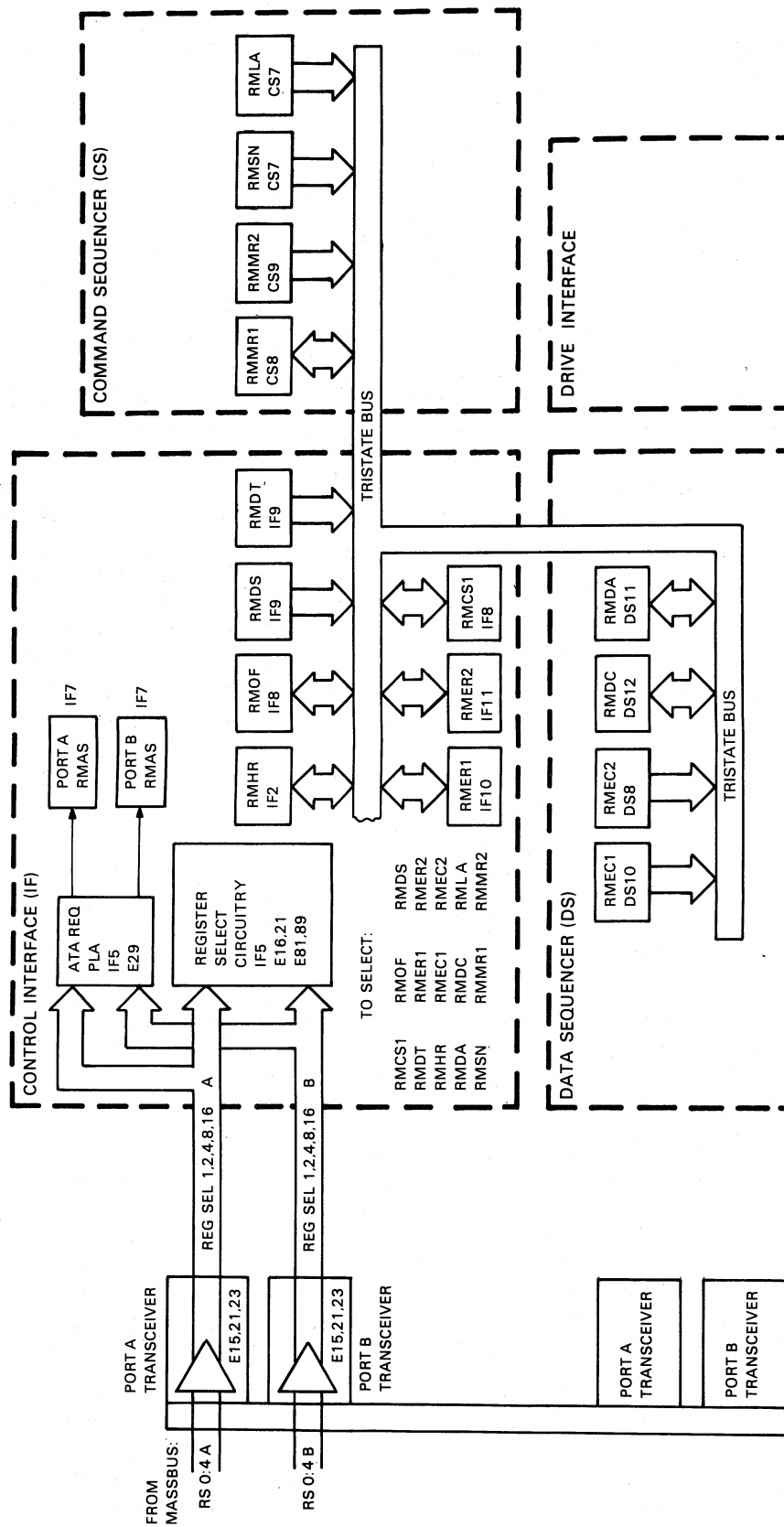
When the RH controller writes information into an RM adapter register, the following sequence occurs.

1. The device select lines select the desired drive (Figure 3-5).
2. The register select lines select the desired register (Figure 3-6).
3. The MASSBUS places the information on the 16 control bus lines and asserts the CTOD line.
4. The controller asserts demand (DEM) (Figure 3-7) and initiates the handshake sequence. The timing for this register write is shown in Figure 3-8.
5. DEM enables the gray code counter which accesses a new location in the handshake PROM during every cycle of the system clock.

NOTE

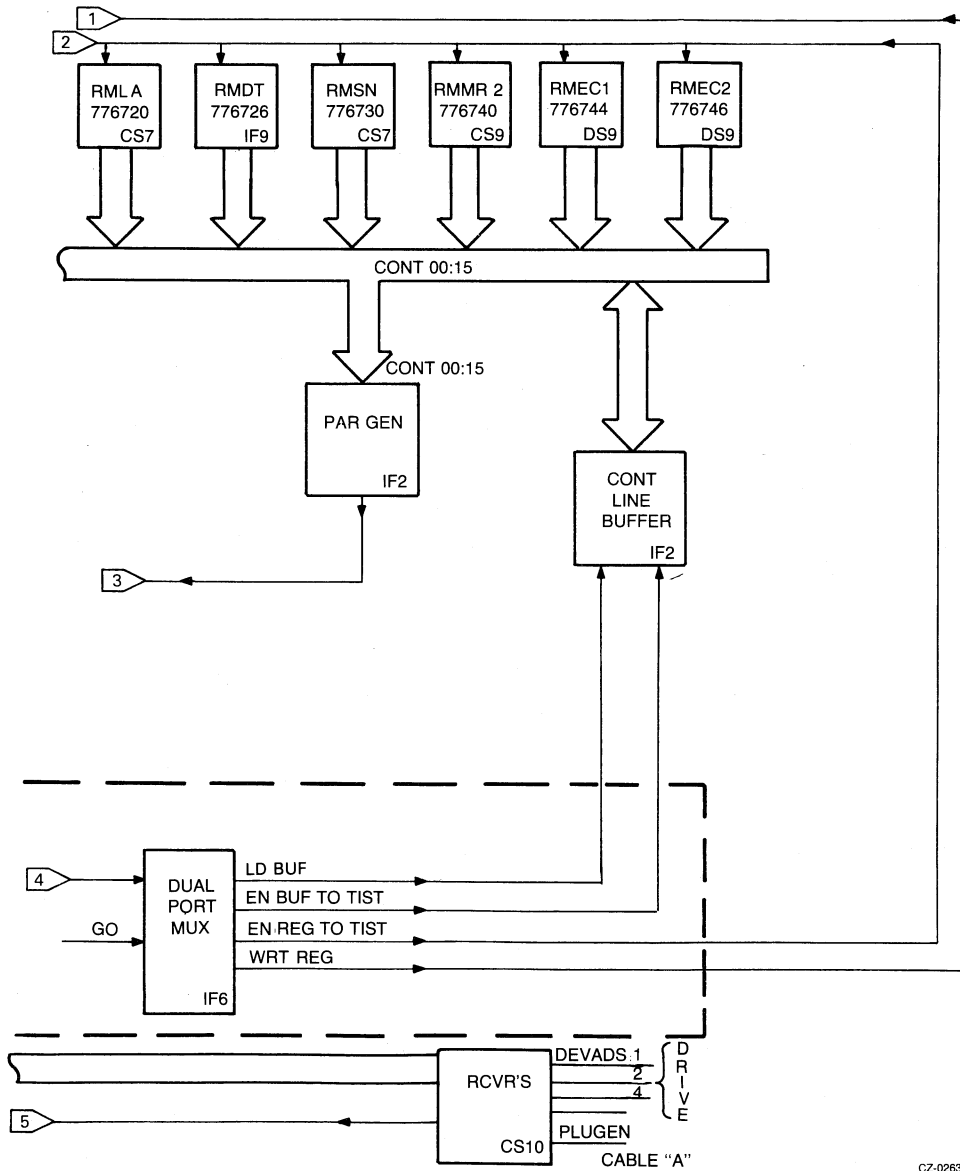
The handshake takes six clock cycles and cannot be interrupted during this time. The other port is inhibited by the TOO LATE signal from the PROM.

6. LD BUF signal loads the control bus information into the control line buffer (holding register).
7. ASY WRT signal loads the control bus information from the control line buffer into the selected register. If the control and status register 1 (RMCS1) was written, the GO bit will set on the next clock cycle.
8. The handshake PROM sends TRA to the controller to indicate that the sequence is complete and that the information has been received.
9. The controller negates DEM when it receives TRA from the drive. If the RH controller does not receive TRA within 1.5 microseconds following DEM, the non-existent drive bit will be set.
10. Negated DEM negates TRA, and the sequence is complete.



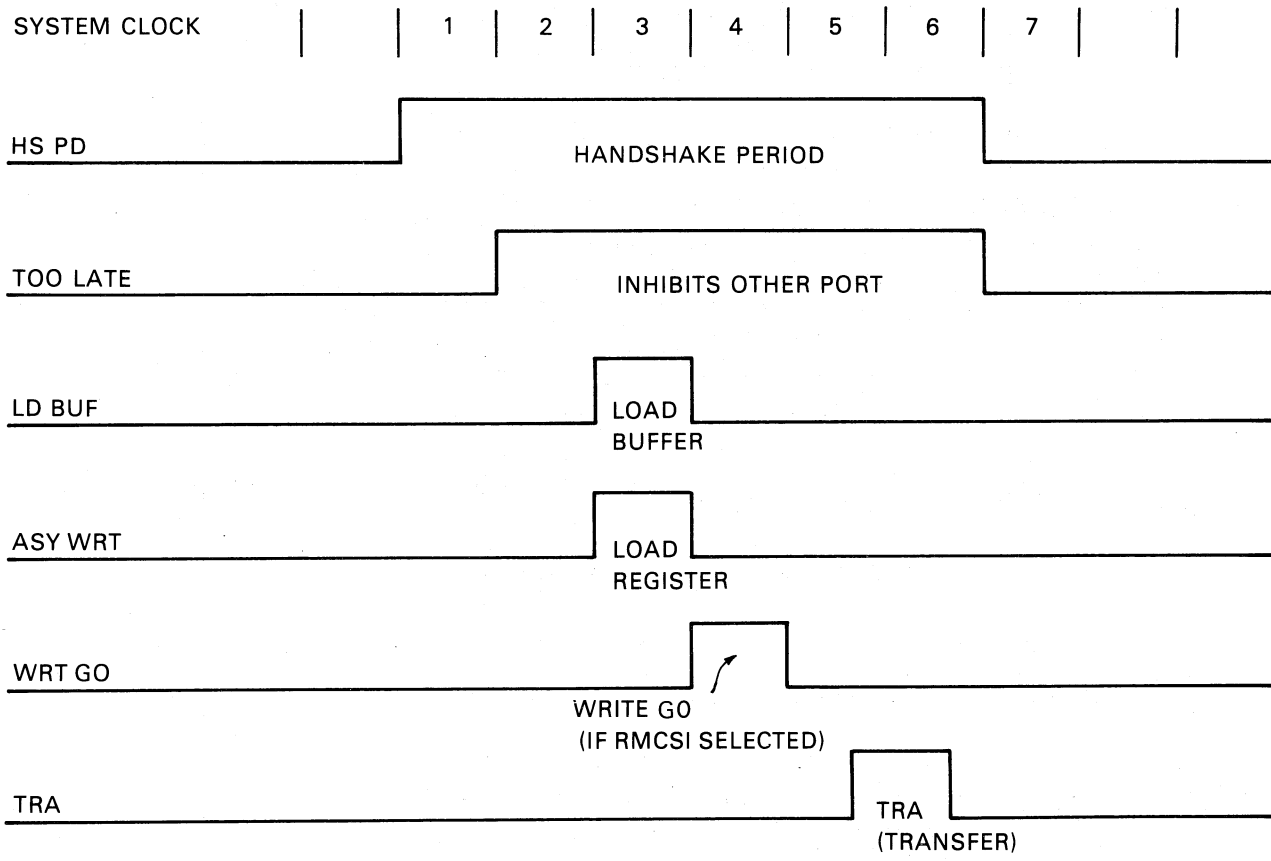
MA-1674

Figure 3-6 Register Selection Block Diagram



CZ-0263

Figure 3-7 Register Read/Write Handshaking Block Diagram (Sheet 2 of 2)



MA-1677

Figure 3-8 Handshake Timing for Register Write

3.7.2 Register Read

When the RH controller reads information from a register, the following sequence occurs.

1. The device select lines select the desired drive.
2. The register select lines select the desired register.
3. The controller negates the CTOD line and asserts DEM.
4. DEM starts the handshake sequence and the gray code counter accesses the PROM. The timing for this read sequence is shown in Figure 3-9.
5. The EN REG TO TIST signal places the information on the control bus.
6. LD BUF loads the control line buffer (holding register) from the control bus.
7. EN BUF TO TIST places the information on the control bus.
8. The handshake PROM sends TRA to the controller to indicate that the contents on the requested register are on the control bus lines.
9. The controller negates DEM when it receives the TRA signal. If the RH controller does not receive TRA within 1.5 microseconds following DEM, the non-existent drive bit will be set.
10. Negated DEM negates TRA, and the sequence is complete.

3.8 DETAILED BLOCK DIAGRAM

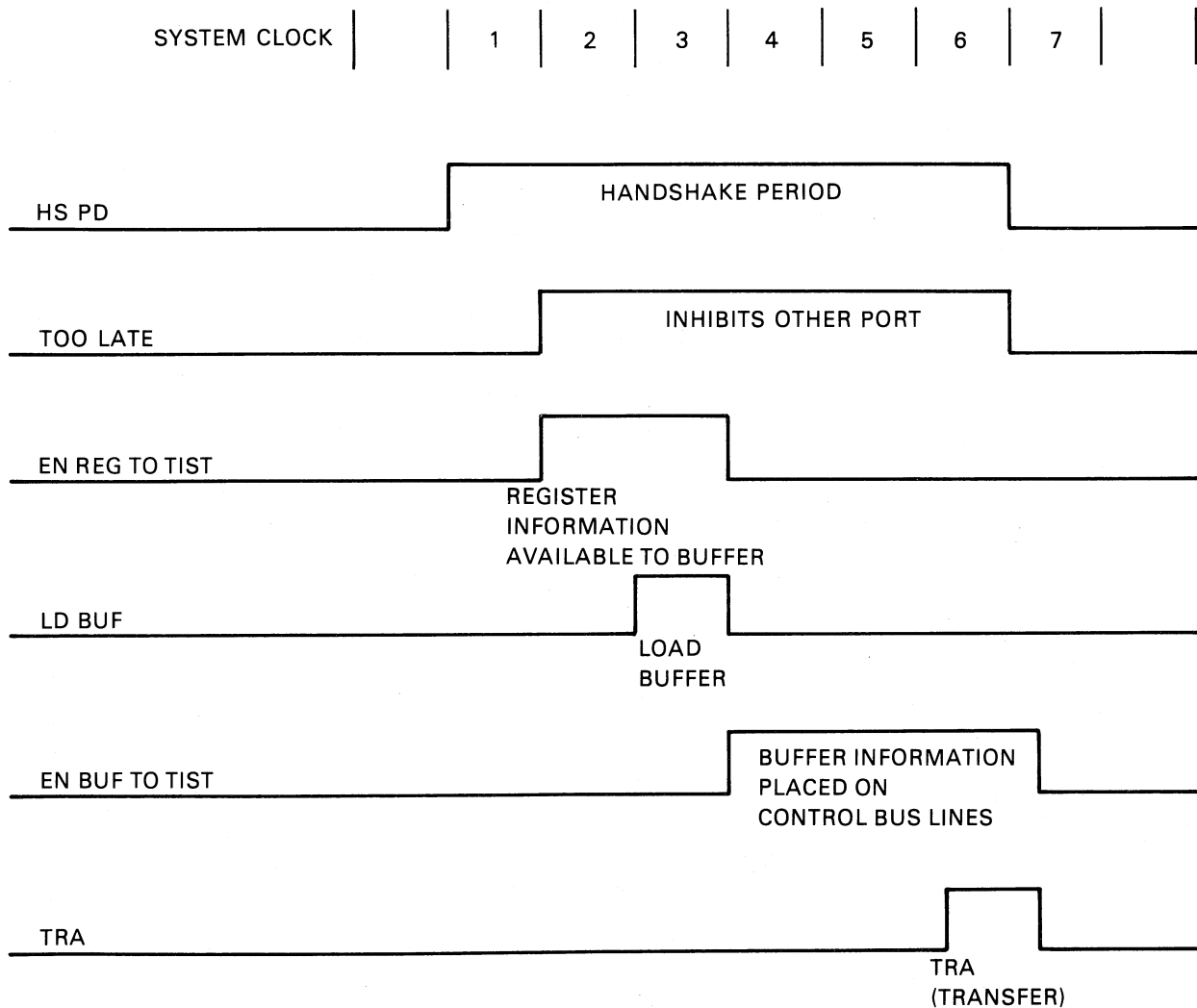
A detailed block diagram of the RM adapter is shown in Figure 3-10. This illustration is referenced throughout this chapter to describe the major functional elements used on each circuit module. Print set page numbers (IF1, DS8, etc.) are also referenced.

3.8.1 Port Transceivers

Two port A transceiver modules (M5922) are used for single-port operation. These modules must be inserted into locations on the RM adapter backplane as shown in Figure 3-1. One port A transceiver receives and transmits all of the asynchronous control signals between the MASSBUS and control interface module via the A control bus as shown in Figure 3-10. The second port A transceiver receives and transmits all the synchronous data information between the MASSBUS and data sequencer module. For dual-port operation, two port B transceivers (M5923) must also be inserted into their specific locations so that all four transceiver positions are occupied.

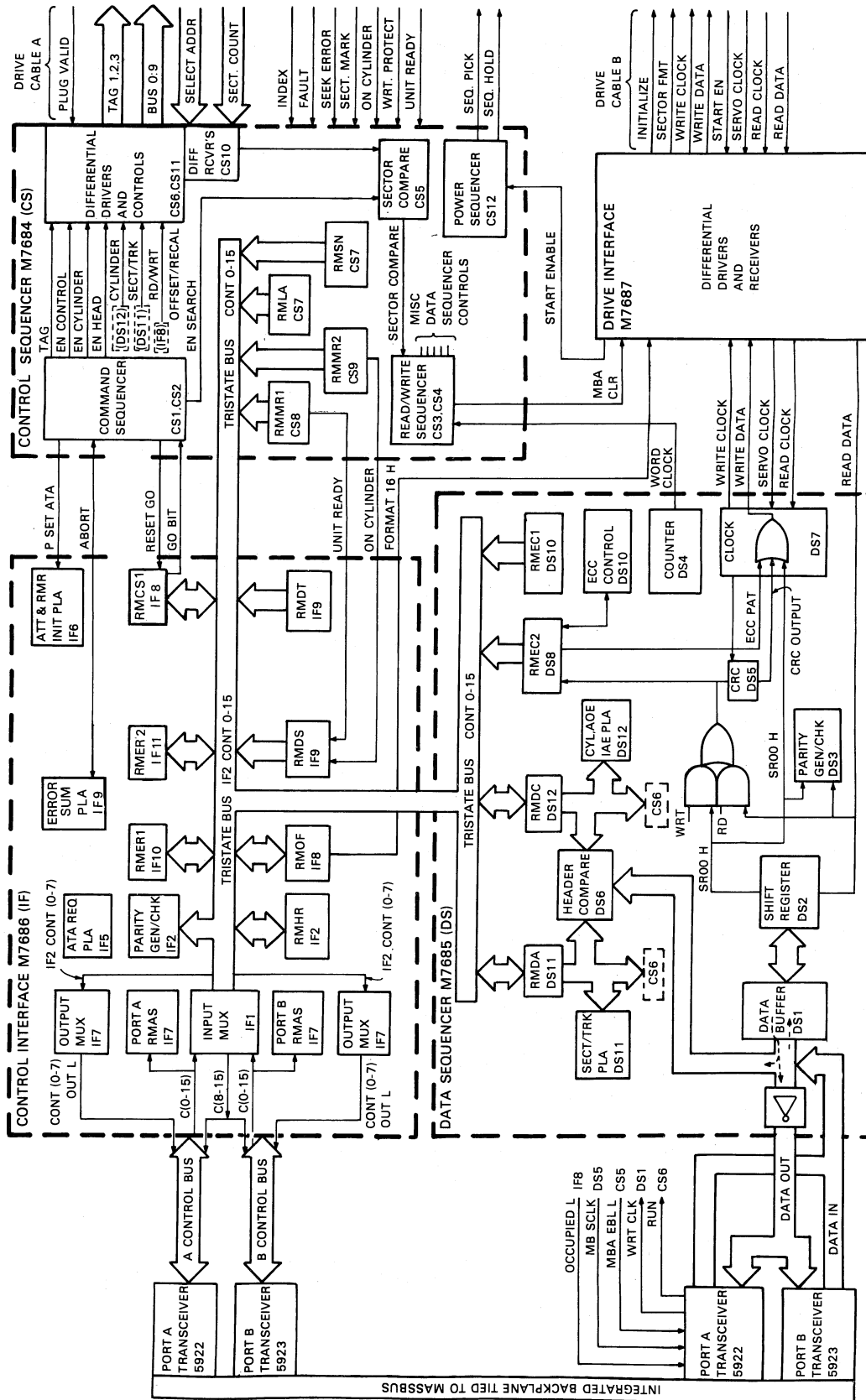
Each transceiver circuit module is equipped with a switch which allows the module to be enabled or disabled manually. Thus, the transceiver modules for both ports can be plugged into the backplane but either port can be disabled manually if desired. Figure 1-4 shows the switch positions for enabling and disabling the port transceiver modules.

The control information on the MASSBUS enters through the port transceivers into the input multiplexer (IF1). This 17-bit-wide multiplexer selects either control bus A or B for its input. If port A is selected, its 16 control bits and parity bit are placed onto the tristate bus. A parity check is made on this control data by the parity generator and checker circuit (IF2). If the control data on the bus fails the odd parity test, the parity circuit will set the parity error bit (PAR) in error register 1.



MA-1680

Figure 3-9 Handshake Timing for Register Read



CZ-0135

Figure 3-10 RM Adapter Block Diagram

3.8.2 RM Adapter Registers

There are 16 registers in the RM adapter. All of these registers are on three circuit modules (control interface, data sequencer, and control sequencer) and access to any register can be gained from the tristate control bus. (Refer to Figure 3-10.)

Attention Summary Register (RMAS) – The RMAS register is not like other addressable registers. It is composed of two flip-flops (one for port A and one for port B) located in each RM adapter. The output of these flip-flops conditions a decoder whose outputs correspond to one of the eight possible drives which can be selected by a single RH controller. Each output is connected to the control bus whose line number corresponds to the number assigned to the drive (and consequently the bit position in the register).

Holding Register (RMHR) – This is an addressable register with no drive function. It is used only by diagnostic software. Whenever writing into any legal register, the same data is concurrently loaded into the holding register. When reading this register, the complement of the register contents is read.

Offset Register (RMOF) – The RMOF register (IF8) is used to hold offset information necessary to move the heads slightly off the track centerline (typically a 250 microinch movement). This register must be loaded prior to issuing an offset command.

Error Register 1 (RMER1) – The RMER1 register (IF10) contains error status indicators for the RM adapter operations and for errors associated with the read data stream.

Error Register 2 (RMER2) – The RMER2 register (IF11) contains error information on the status and performance of the drive.

Control Register (RMCS1) – The RMCS1 register (IF8) is used by both the RM adapter and the RH controller to store the disk commands and operational status. Setting the GO bit causes the drive to recognize the function code in the register. However, actual command execution can only begin after the RUN line has been asserted by a data transfer command.

Drive Status Register (RMDS) – The RMDS register (IF9) contains the operational status indicators for the selected drive.

Drive Type Register (RMDT) – The RMDT register (IF9) allows the program to distinguish between different kinds of drives.

Maintenance Register 1 (RMMR1) – The RMMR1 register (CS8) is used to perform maintenance operations. This register has two distinct 16-bit sections: a read-only section and a write-only section. The write-only section provides a method to control the logic functions of the RM adapter. The read-only section permits monitoring of these operations.

Maintenance Register 2 (RMMR2) – The RMMR2 register (CS9) is used in conjunction with the RMMR1 register to configure the RM adapter in the maintenance mode.

Serial Number Register (RMSN) – The RMSN register (CS7) contains the lowest four digits of the drive serial number. It provides the program with a means to distinguish between different drives connected to the same RH controller. The serial number register is coded (at the factory) from 16 pairs of wirewrap posts on the RM adapter backplane.

Look Ahead Register (RMLA) – The RMLA register (CS7) contains the count of the sector that is currently positioned under the heads. The count value is reset to 0 by the index pulse and is incremented at each sector pulse.

Disk Address Register (RMDA) – The RMDA register (DS11) is used to program the sector and track on the disk to which, or from which, a transfer is desired. The register content is incremented each time a data sector/block is transferred.

Desired Cylinder Register (RMDC) – The RMDC register (DS12) contains the address of the cylinder to which the drive positioner moves the heads for a seek or search.

ECC Position Register (RMEC1) – The RMEC1 register (DS10) contains the address of the error burst within the data field.

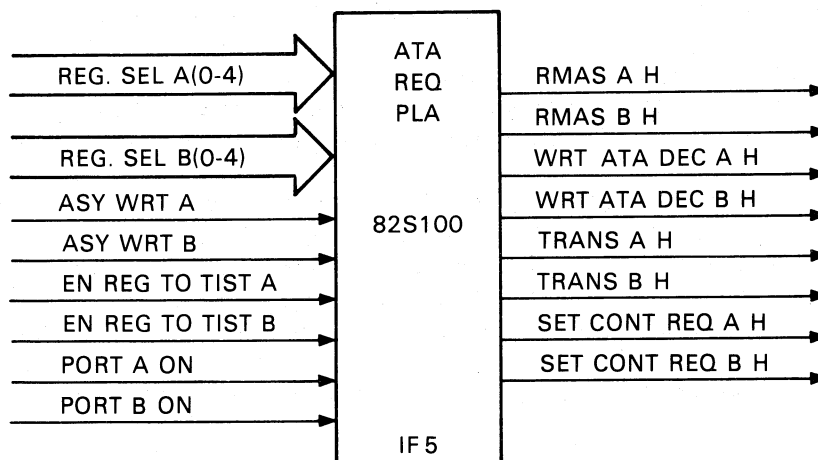
ECC Pattern Register (RMEC2) – The RMEC2 register (DS8) contains a reference pattern that a program can use to correct the incorrect data (in memory). A “1” in this register corresponds to a bad bit; a “0” corresponds to a good bit.

3.8.3 RM Adapter PLAs

The RM adapter uses five programmable logic arrays (PLAs) to perform signal testing and error decoding operations. Each PLA has 16 input lines (variables) and 8 output lines (functions). Inside each PLA is a matrix that acts as an input decoder. The particular crosspoint pattern used has been selectively connected by a factory masking procedure. Each device output bit is the product of a match between the PLA input variables with the combinational logic in the input decoder.

In a PLA, some combinations of inputs may have no effect on the output, and some groups of input combinations may generate the same output. These functions are different from a read-only memory (ROM) where all combinations of inputs cause an output to appear.

3.8.3.1 ATA Control/Request PLA – This PLA is used to control the port A or B attention summary registers and to set the port request flip-flops. Each port always has access to its RMAS register. The status of the RMAS register is read through an 8-bit-wide output multiplexer onto the port control bus via its output lines CONT (0-7) OUT L. If port A is requested, the ATA control/request PLA asserts the SET CONT REQ A H line shown in Figure 3-11. To select the port A RMAS register, the PLA asserts RMAS A H. When writing the port A RMAS register, the PLA asserts the WRT ATA DEC A H signal. To read the register, it asserts the TRANS A H signal.



MA-1678

Figure 3-11 Attention Control/Request PLA

3.8.3.2 Error Sum PLA (IF9) – The error sum PLA is used to monitor the error conditions that can occur in the RM adapter or disk drive.

This PLA generates a composite error signal whenever one or more error conditions are detected at its input. An exception error signal is produced and sent to the MASSBUS to indicate that an error condition has occurred during a data transfer. Any class-B error (catastrophic error) causes an abort signal to be asserted. This abort condition terminates any non-data transfer commands immediately and resets the GO bit.

If an abort condition occurs during a data transfer command, the PLA asserts the ABORT L line. This signal causes an END-OF-BLOCK (EBL) pulse to be generated to end the data sequence.

3.8.3.3 ATA, RMR, INIT PLA (IF6) – This PLA is used to generate the attention conditions, to initialize registers, and to detect when a register write attempt was made illegally during a data command sequence. The RMR SET signal out of this PLA indicates a register modification refused (RMR) condition. If bit 2 (RMR) of error register 1 is set, it means that an illegal attempt was made to write into a register before the completion of a data command sequence.

The attention bit in the RMAS register and RMDS register is set when any of several attention conditions are detected by the PLA. For instance, ATA is set for any error condition in the error registers or if the MOL bit changes state. It is also set at the completion of a seek, search, recalibrate, offset, or return-to-centerline command.

3.8.3.4 Sector/Track PLA (DS11) – This PLA is used in conjunction with the RMDA register to detect when one of several disk address limits are reached. At its input are the five track bits, the five sector bits, and a format bit. From this input information, the PLA indicates when the last sector is reached (sector wraparound), when the last track is reached (track address wraparound), when the last sector and last track are reached, and also whether any invalid sector or track is found in the RMDA register.

3.8.3.5 CYL/AOE/IAE PLA (DS12) – This PLA is used in conjunction with the RMDC register to indicate when the heads reach the maximum cylinder address on the disk. It also indicates when the last sector address on the disk pack or head/disk assembly (HDA) is reached. Two error conditions are provided by this PLA. It sets the invalid address error (IAE) and the address overflow error (AOE).

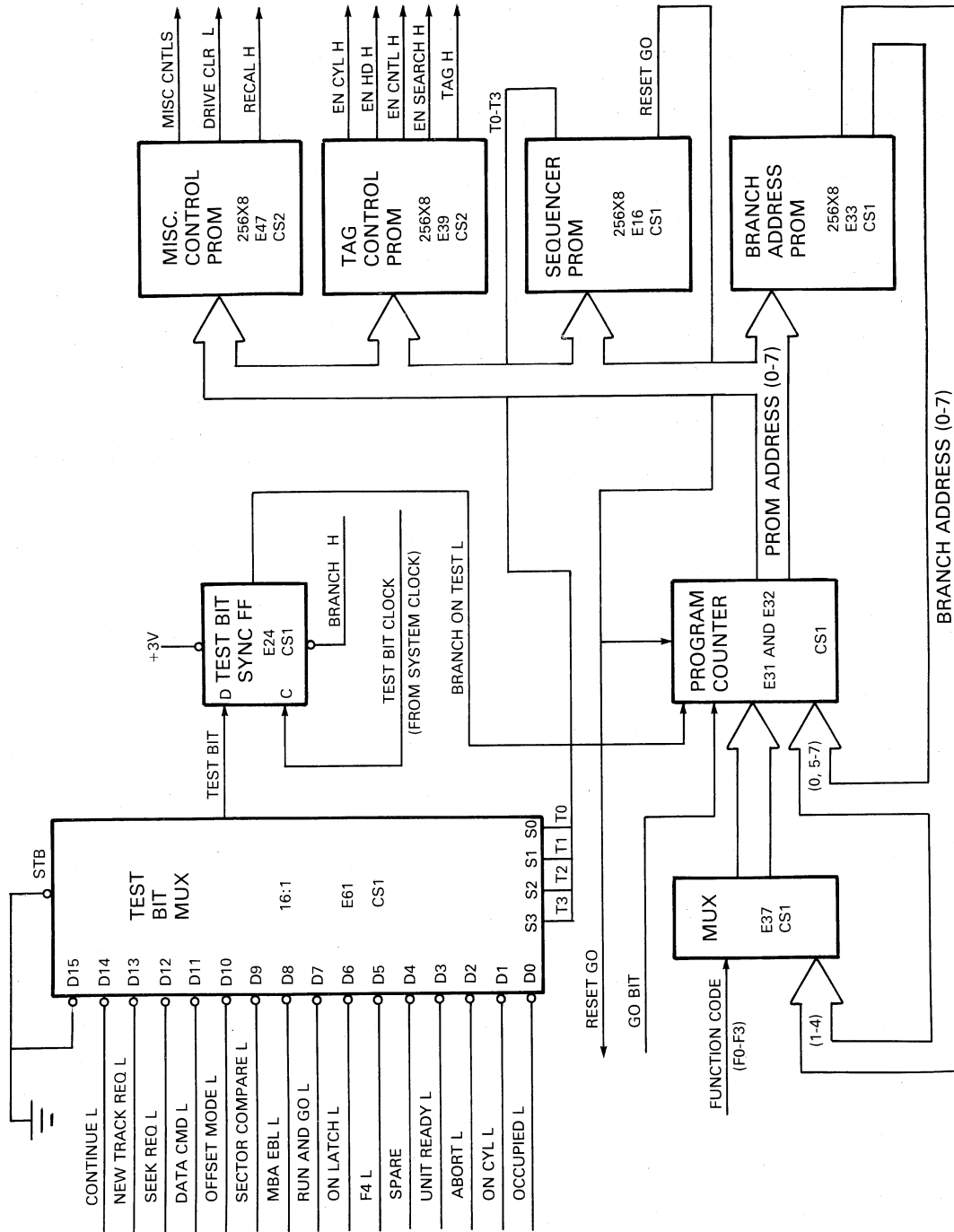
3.8.4 Command Sequencer (CS1, CS2)

The command sequencer controls most of the command operations of the RM adapter. During data handling commands, the read/write sequencer controls the data transfer portion of these functions.

The command sequencer is illustrated in Figure 3-12. It consists of a program counter and four PROMs having 256 memory locations each. The counter is used to step through the sequence and to address the PROMs. The counter is held at 0 whenever the GO bit in the control register is cleared.

A branch multiplexer feeds the program counter with address information. This multiplexer selects either the lower four bits of the function code (F0-F3) or the lower four bits of a branch address. At the beginning of any command, the multiplexer strobes the function code into the program counter setting up the command sequencer PROMs. Upon receiving another clock strobe, the multiplexer selects the branch address from the branch address PROM as an input.

The program counter receives the function codes or branch address and proceeds to establish PROM outputs.



CZ-3063

Figure 3-12 Command Sequencer Block Diagram

Various test conditions are monitored by the test bit multiplexer. The output of this multiplexer affects the program counter. If the program counter changes because of a test condition, this change either branches the program counter to a new address or sequences the PROM.

For example, if test condition 3 (D3 input) is selected and the UNIT READY signal is not asserted, a new branch address is loaded into the program counter. When branch on test occurs, the sequencer jumps to the new address and continues its program sequence from the new address.

Some of the more important signals out of the command sequencer PROMs are given below. The ENABLE SEARCH signal enables the sector compare circuit (CS5) to look for a sector match with the sector address in the disk address register. Once this match is detected, SECTOR COMPARE is issued to the read/write sequencer. The match allows this sequencer to begin controlling the reading and writing of data.

The EN CYLINDER, EN HEAD, EN CONTROL, EN OFFSET, and RECAL signals permit positioning and control information to be transmitted by the differential drivers (CS6) to the drive. The TAG signal is used in conjunction with the EN CYLINDER, EN HEAD and EN CONTROL signals to select the appropriate tag line for transmission to the drive.

3.8.5 Read/Write Sequencer (CS4)

The read/write sequencer controls the format synchronization to enable the reading and writing of data.

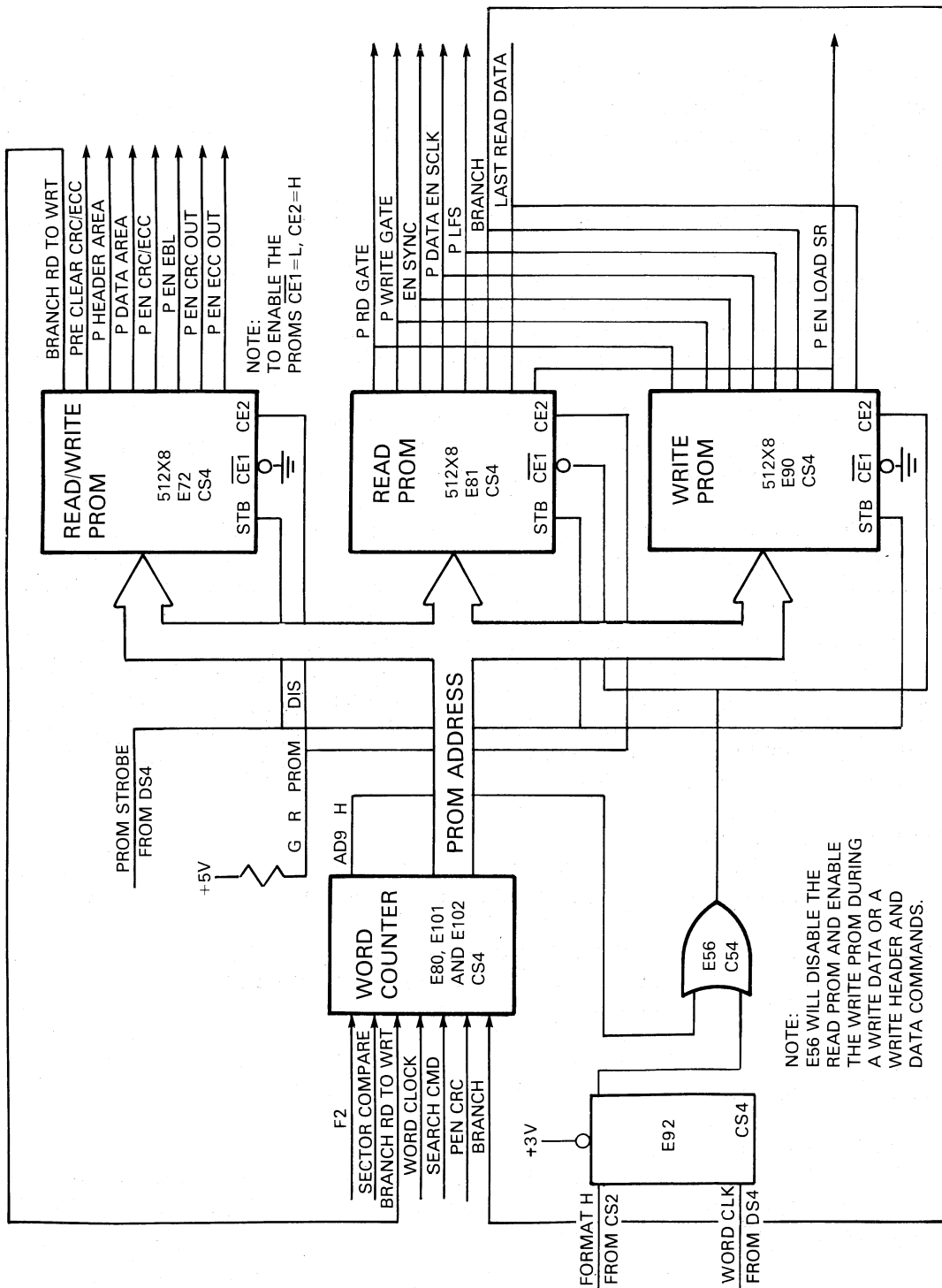
Figure 3-13 shows that the read/write sequencer consists of a word counter and three 512×8 PROMs. As long as SECTOR COMPARE H is unasserted, the counter remains cleared. As soon as SECTOR COMPARE becomes asserted, the counter increments and provides the addressing for the PROMS. Clocking for the counter is provided by the word clock. The read/write PROM (E72) generates timing for the seven major subdivisions of each sector. These subdivisions are listed below.

1. Sector gap and sync byte
2. Header area
3. CRC
4. Header gap and sync byte
5. Data area
6. ECC area
7. Postamble

The E81 and E90 PROMs control the reading or writing of a sector data area. One signal out of these PROMs is PROM LOOK FOR SYNC (PLFS). This signal inhibits the bit counter on DS4 from incrementing during the gap areas. When the sync byte in either the header or data area is detected, the BRANCH signal allows the word counter to branch to a count that corresponds to either the start of the header or data areas of a sector.

The BRANCH signal forces the counter to be in sync with the sector, so that the counter will be able to accurately keep track of the number of data words the head is into the sector. The BR RD TO WRT signal is used in a write data command to negate READ GATE (following the reading of header words) and to assert write gate.

E92 in Figure 3-13 prevents a race condition from occurring during a write header and data command (FORMAT H). FORMAT H is synchronized with the WORD CLK.



CZ-3084

Figure 3-13 Read/Write Sequencer Block Diagram

3.8.6 Data Sequencer Data Paths

Although the read/write sequencer is located on the control sequencer module (M7684), the data paths are on the data sequencer module (M7685, M7685-YA, or M8685). Paragraphs 3.8.6.1 and 3.8.6.2 describe the write and read paths, respectively.

3.8.6.1 Write Path – Figure 3-14 shows the path taken by data during a write command. Assuming port A is selected, data words requested from the MASSBUS are loaded into the data buffer (DS1) one word at a time. The shift register is parallel loaded from the data buffer register and from here the data is serially shifted to the right.

The serial output (SR00 H) from the shift register is sent to three places. One path takes the data to the CRC circuit (DS5) (for CRC generation during the header write) and to the ECC circuit (DS8, DS10) (for ECC generation during the data write), where it can be checked or corrected. The second path presents the serial data to a series of gates on DS7 that act like a multiplexer. This multiplexer can select its output data from one of three sources at its input. It can select the serial shift register data (SR00 H), or a CRC output word, or an ECC pattern out of the ECC pattern register (RMEC2). The input that is selected depends upon what portion of a sector format is being written and also which command was issued. Write data, together with write clock, is transmitted via cable B to the disk drive. The third path allows a parity check to be made on this serial data as it leaves the shift register. The logic for the parity generator and checker is shown on page DS3 of the RM adapter print set.

3.8.6.2 Read Path – Figure 3-15 shows the path taken by data during a read command. The data being read from the disk enters the RM adapter via drive cable B. The data enters and leaves the differential receivers (on module M7687) on the read data line in sync with the read clock generated by the disk. A branch of the read data is fed to the CRC (DS5) and ECC (DS8, DS10) circuits where the header words and data words can be checked for CRC and ECC errors, respectively. The read data is shifted serially into the shift register, a parity bit is added, and the data is then loaded in parallel into the data buffer (DS1). As the read data leaves the data buffer, a comparison is made between the first two header words only to be sure they match the desired cylinder, sector, and track address information stored in the RMDC and RMDA registers. The read data from the data buffer is then inverted and sent over the data out bus to whichever port is selected.

3.9 COMMAND EXECUTION

All command execution is handled by the command sequencer after the GO bit is set. As long as the GO bit in the control register is cleared, the program counter on CS1 remains reset to 0.

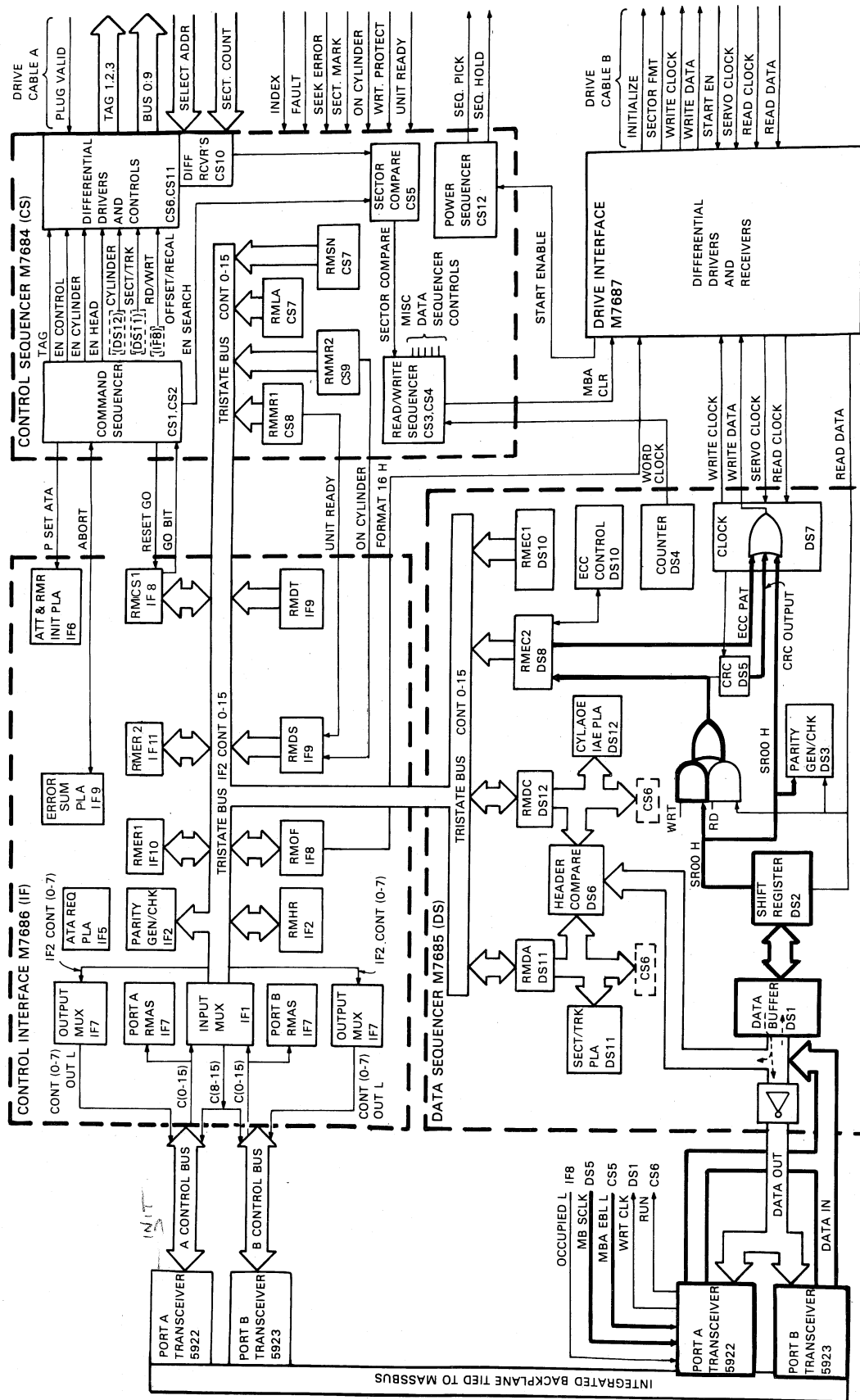
On the first clock pulse after the GO bit becomes active, the sequencer jumps to a PROM address specified by the function code excluding bit F4. Function code bit F4 indicates a data command and is monitored as 1 of the 16 test conditions later on in the microcode sequence.

After the sequencer jumps to the PROM address specified by the function code, further sequencing depends upon the type of command. There are three types of commands.

Type 1: Command Immediate

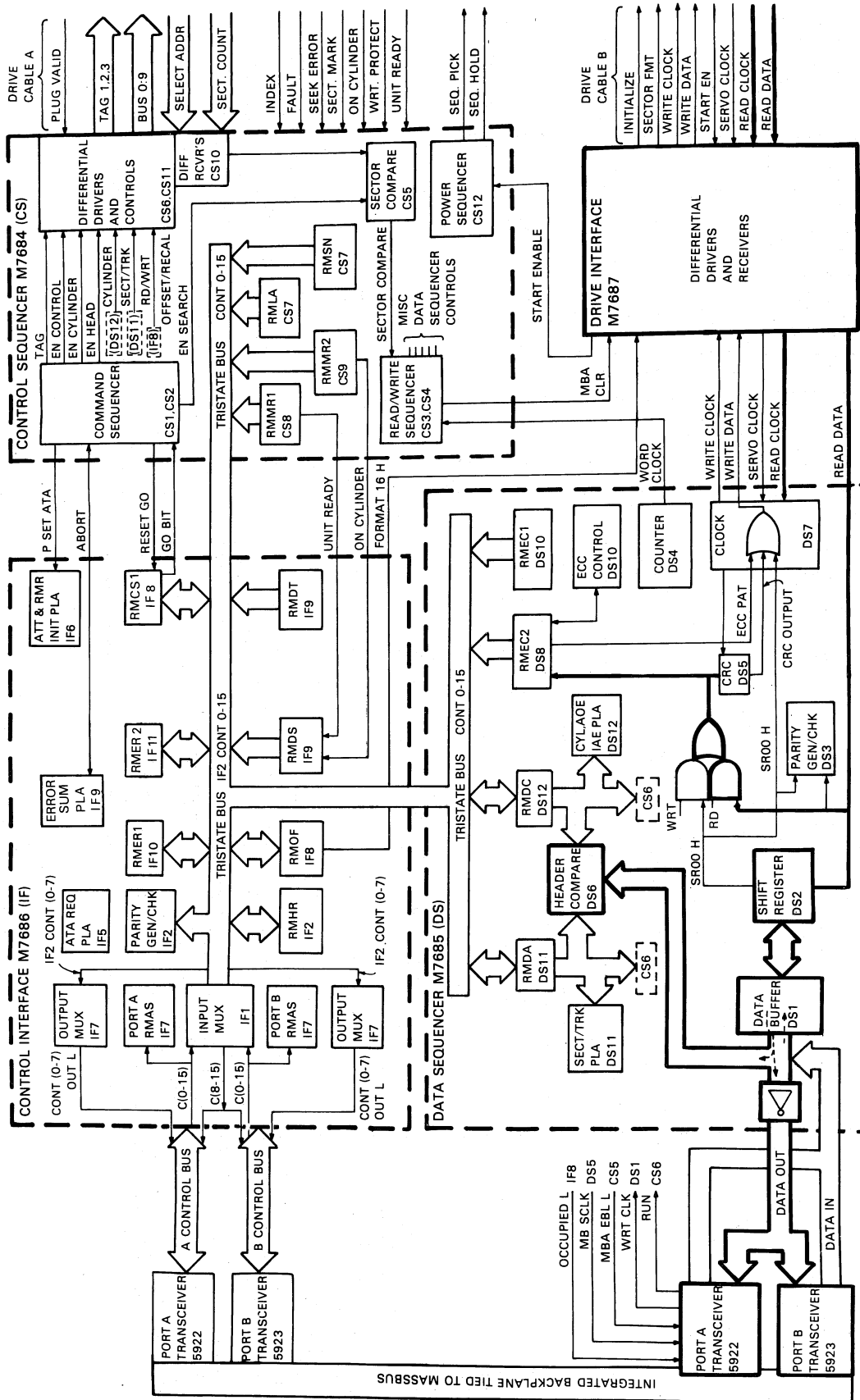
In this type of command, the sequencer jumps to the function code and then immediately ends by re-setting GO. The operation performed by the command occurs immediately on decoding the function. The following commands fall into this category.

- No-op command
- Release command
- Read-in-preset command
- Drive clear command
- Pack acknowledge command



CZ-0096

Figure 3-14 - Write Data Flow Path Diagram



02-0807

Figure 3-15 Read Data Flow Path Diagram

Type 2: Command Immediate with ATA

These are mechanical motion commands where the sequencer jumps to the function code, executes a sequence (i.e., mechanically positions the heads), sets ATA, and resets GO. The following commands fall into this category.

- Offset command
- Return-to-centerline (RTC) command
- Recalibrate command
- Seek command
- Search command

Type 3: Data Transfer Commands

These are the commands that cause data to be transferred to or from the disk. In executing these commands, the command sequencer jumps to the function code, then jumps to address 128, executes a sequence, and then loops during enable search. When the desired sector is found, the read/write sequencer synchronizes with the sector format, transfers the appropriate data, and ends the sector with an end-of-block (EBL) pulse. Upon receiving this pulse, the command sequencer continues through its program and ends by resetting GO. The following commands fit into this category.

- Read data command
- Read header and data command
- Write check data command
- Write check header and data command
- Write data command
- Write header and data command

3.9.1 Command Immediate Execution

Command immediate causes a jump directly from the function code location to the end where reset GO L is asserted. (All PROM addresses listed below are in octal.)

3.9.1.1 No-Op Command – This command simply resets the GO bit.

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start 1 = Function 176 = End	Branch to Function Branch to End Reset GO	BRANCH H SET PULSE L END RESET GO L

3.9.1.2 Drive Clear Command – This command clears any drive errors if the cause of the error is no longer present. It also clears the bits indicated in the following registers.

RMDS	Bits 14 and 15
RMER1	All bits
RMER2	All bits
RMAS	All bits
RMMR1	All bits
RMEC2	All bits

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start 11 = Function	Branch to Function Branch to DRV CLR	BRANCH H SET PULSE L BRANCH H DRIVE CLR L RESET GO L
175 = DRV CLR 176 = End	Increment Reset GO	

3.9.1.3 Release Command – This command performs a drive clear function and then releases the drive for use by the other port.

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start 13 = Function	Branch to Function Branch to End	BRANCH H SET PULSE L RELEASE CMD L END RESET GO L
176 = End	Reset GO	

3.9.1.4 Read-In Preset Command – This command sets the volume valid bit (06) in the drive status register for the port that issued the command. It also clears all bits in the RMDC and RMDA registers as well as clearing the following bits in the offset register (bits 7, 10, 11, and 12).

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start 21 = Function	Branch to Function Branch to End	BRANCH H SET PULSE L READ IN CMD L RESET GO L
176 = End	Reset GO	

3.9.1.5 Pack Acknowledge Command – This command must be issued before any data transfer or positioning command if the disk drive has gone off- and on-line again (i.e., MOL changes state). This command sets volume valid (bit 6 in the drive status register). Note that volume valid is generated from ROM (E50 on IF6).

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start 23 = Function	<u>Branch to Function</u> Branch to End	BRANCH H SET PULSE L SET VV H RESET GO H
176 = End	Reset GO	

3.9.2 Command Immediate with ATA Execution

These commands are executed exactly like a command immediate, except that the attention bit (ATA) is set while resetting the GO bit to flag the end of the command.

3.9.2.1 Offset Command – In disk drives where the offset command is used, the command sets the offset mode flip-flop in the RM adapter and conditions the adapter for an offset sequence during the next read data command. When this occurs, the ATA flip-flop is set, completing the command.

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	BRANCH H
15 = Function	Branch to ATA	SET PULSE L OFFSET CMD L
177 = ATA + End	Set ATA Reset GO	P SET ATA L RESET GO L

OFFSET CMD L sets the offset mode flip-flop.

The offset request is not sent to the drive until TAG 3 occurs during the read data transfer command. When TAG 3 and TAG BUS 2 or 3 (depending upon the direction of offset) is asserted, the drive negates ON CYL until the offset is complete. When the offset is complete, the drive asserts ON CYL. At this time, the RM adapter asserts TAG BUS 1 (READ GATE) after recognizing the sector pulse. When the data transfer is finished, TAG 3 is negated and the drive returns to centerline. As long as the offset mode flip-flop is set, the offset request is sent to the drive for each data transfer operation. At the completion of the read data transfer operation or the last sector, the drive returns the heads to track centerline.

The offset mode flip-flop is reset by the conditions listed below.

- Loading of the desired cylinder register (indicating a seek to a new cylinder)
- An implied seek
- Return-to-centerline command

3.9.2.2 Return-To-Centerline Command – This command resets the offset mode flip-flop and allows a four millisecond delay for the drive to complete the return-to-centerline movement. The ATA flip-flop is then set completing the operation.

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	BRANCH H
17 = Function	Branch to ATA	SET PULSE L
19 = Function	Branch to End	RET TO CNT L
177 = ATA + End	Set ATA Reset GO	P SET ATA L RESET GO L

RET TO CNT L resets the offset mode flip-flop.

3.9.2.3 Recalibrate Command – This command positions the heads over cylinder 0 and sets the current cylinder address register to 0. Figure 3-16 shows a flowchart of this command. The command begins by testing function code bit 4 and UNIT READY. (F4 is tested to determine if this could be a data command.) UNIT READY is tested to ensure that all interlock conditions are met in the disk drive. The sequencer then checks to see whether any abort conditions are present. The control tag, together with control bus bit 7, is then sent to the disk drive. At this point, the on latch is tested to be sure the drive has accepted the command and has initiated motion of the heads. If it passes this test, the sequencer then waits for ON CYLINDER to become active again, indicating that the heads are over the correct cylinder. It then sets the ATA bit and resets GO.

3.9.2.4 Seek Command – This command causes the heads to move to the cylinder address specified in the RMDC register. The command is complete when the current cylinder in the drive equals the desired cylinder. A flowchart of this command is provided in Figure 3-17. All commands begin by testing unit ready and F4 to see if the drive is busy and whether this function is a data command. If the sequencer passes these tests and there are no abort conditions present, it issues TAG 1 and cylinder information to the drive. The SET PULSE has already reset the on-latch flip-flop and the sequencer now waits for ON CYLINDER to become active again. When ON CYLINDER is detected, the sequencer then jumps to the end where the sequencer sets ATA and resets GO.

3.9.2.5 Search Command – This command searches for the desired cylinder and sector address and interrupts the CPU when the desired sector is under the heads. A flowchart for this command is shown in Figure 3-18. Like all other commands, it begins by testing drive UNIT READY, F4, and abort conditions. After testing ABORT, the sequencer jumps to decimal address 144 and uses the implied seek portion of a data command. It issues TAG 1 and cylinder information to the drive and then tests the occupied bit to determine if the sequence should continue the search.

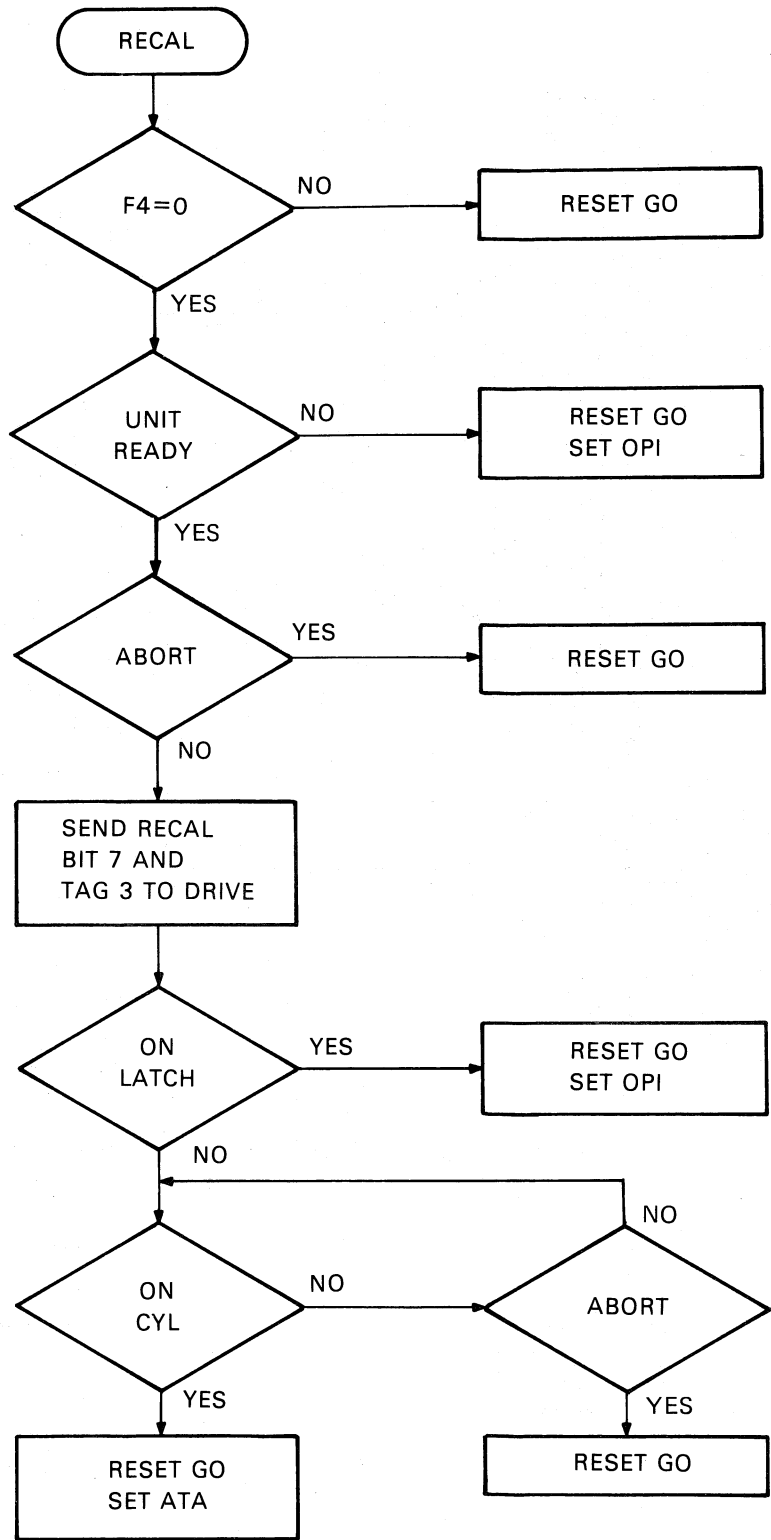
Occupied will always be 0 during a search command but will be a 1 during the implied seek/search portion of the data transfer command. If occupied = 0, the search routine continues. The SET PULSE has already reset the on latch flip-flop so the sequencer waits for ON CYLINDER to become active. When it does so, indicating that the heads are on cylinder, the sequencer then asserts the ENABLE SEARCH signal, starting the search for the correct sector. Each sector is continuously compared with the contents of the disk address register until a match is found. At this point, if no error conditions are present to cause an abort, the SECTOR COMPARE signal causes the sequencer to jump to the end of its routine, setting ATA and resetting the GO bit.

3.9.3 Data Transfer Command Execution

All data commands are executed by the same routine which starts at decimal address 128. Prior to the routine, command execution is similar to other commands. That is, the sequencer starts at 0 and jumps to the function and then to the routine.

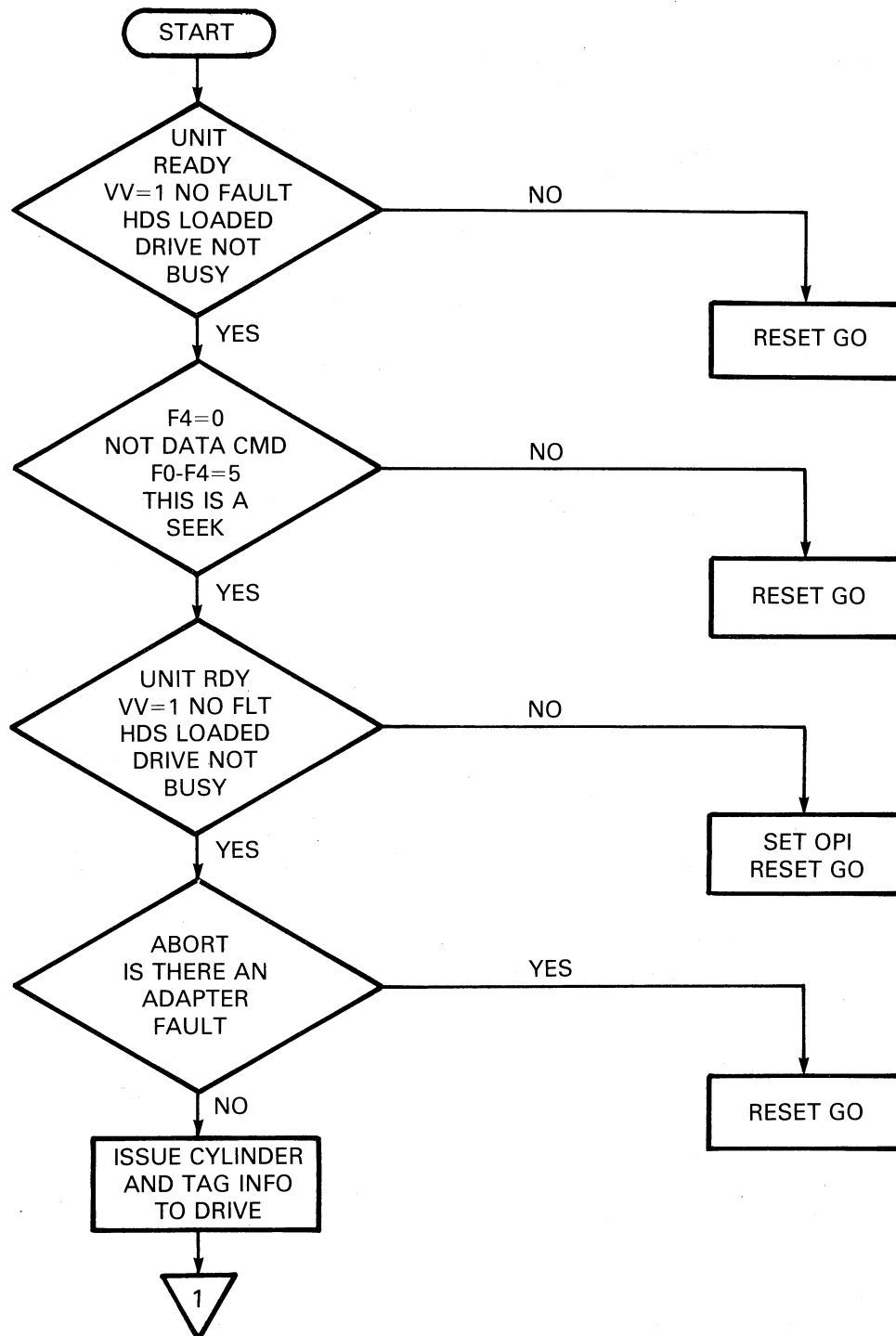
The data routine consists of five consecutive segments. They are as follows.

1. Check initial conditions
2. Execute an implied seek and head selection
3. Execute an offset (if required)
4. Execute a search and data transfer
5. Continue or terminate



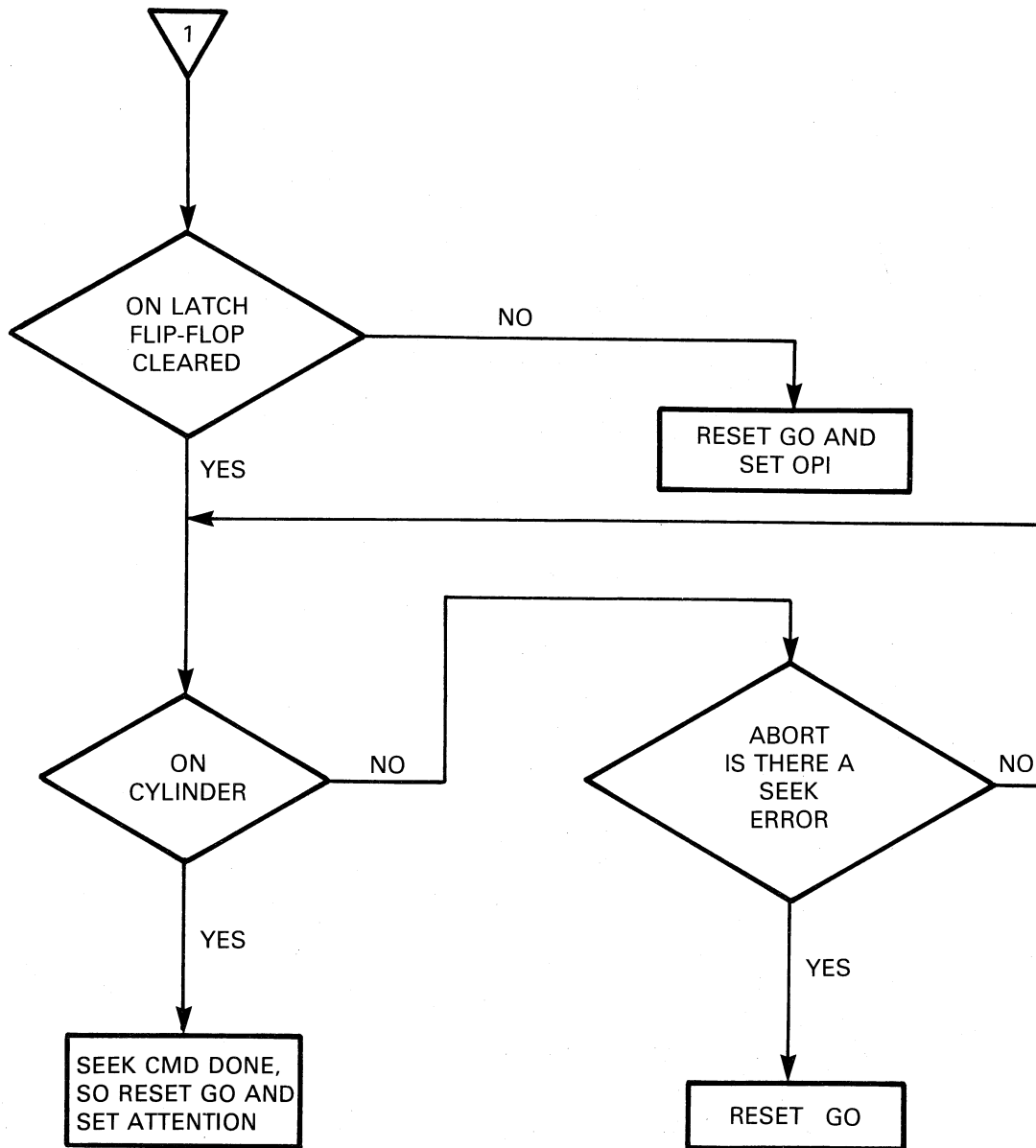
MA-1685

Figure 3-16 Recalibrate Command Flowchart



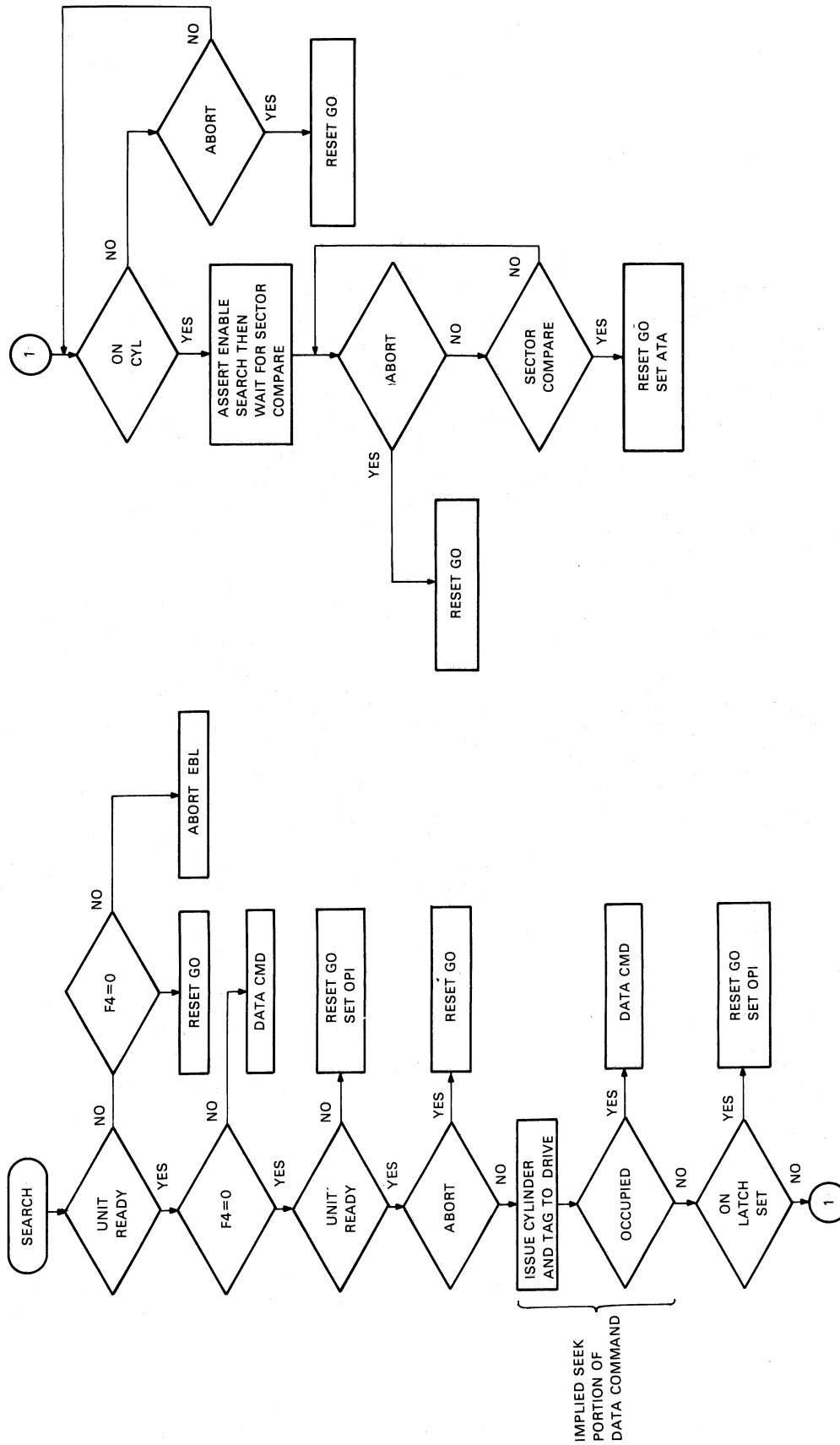
CZ-3081

Figure 3-17 Seek Command Flowchart (Sheet 1 of 2)



CZ-3082

Figure 3-17 Seek Command Flowchart (Sheet 2 of 2)



MA-1687

Figure 3-18 Search Command Flowchart

A data command flowchart is presented in Figure 3-19. Before executing the data command, the microcode checks for a drive ready condition. Next, the microcode checks for any abort conditions. If an abort is indicated, the command terminates at this point. The microcode then checks the RUN line on the MASSBUS interface. The command proceeds if the RUN line is active. If not, the program loops on checking for an abort condition or an active RUN line. If the RUN line does not become active within 50 milliseconds after the GO bit is set, a timeout causes an abort condition.

The second segment of the program involves the implied seek. Seek execution starts at decimal 144 address and increments up to location 156. During this portion of the microcode, all signals required for seek execution become active. EN CYLINDER, which becomes active first, is used to enable the outputs of the desired cylinder register onto the bus lines to the drive. The TAG H signal is gated with EN CYLINDER to generate TAG 1 to the drive. On the leading edge of TAG 1, the drive strobes the tag bus lines. On the trailing edge of TAG 1, the drive initiates the seek. The sequencer then checks the occupied bit to determine whether to perform a search command or a data command. The ON LATCH flip-flop is checked to ensure that head motion was initiated. If occupied is not asserted, the sequencer initiates a search command. If asserted, the search will still be performed, but a data transfer command will follow.

Head selection begins at decimal address 157 of the command sequencer and continues to location 165. During this period, the sequencer asserts EN HEAD to gate the output of the desired address register onto the drive bus lines. The TAG H line is asserted and gated with EN HEAD to generate TAG 2 to the drive. The drive selects the new head on the trailing edge of TAG 2. The microcode includes a five microsecond waiting period after head selection to allow the heads to settle and provide reliable data.

After head selection has been completed (and during the head settling time), ON CYLINDER is checked. If not active, the sequencer loops and checks for any aborts. The sequencer stays in this loop for 500 milliseconds. If ON CYLINDER does not become active within this time, the sequencer will abort the command.

The third segment of the microcode permits offset commands to be executed provided the offset flip-flop has been set by the offset command. When the offset flip-flop is set, the sequencer asserts EN CONTROL to move the offset direction bit from the offset register to the tag bus lines. The sequencer then asserts TAG H and gates this signal with EN CONTROL to generate TAG 3 which goes to the disk drive. ON CYLINDER is tested and allows the sequencer to advance to the next segment when ON CYLINDER becomes active at the completion of the offset operation. The sequencer causes an abort condition if ON CYLINDER does not become active within 500 milliseconds.

The fourth segment of the microcode starts the search routine when the command sequencer asserts the EN SEARCH signal. The sequencer loops until either the correct sector is found and the entire sector has been transferred, or until a timeout occurs. If a timeout occurs, the command is aborted. (The timeout occurs if there is no match between the sector count from the drive and the desired address sector within three revolutions.) When the correct sector is found (SECTOR COMPARE is true), the read/write sequencer takes control and executes a read or write sequence for one sector. At the end of that sector, an EBL pulse is generated to notify the command sequencer that it may proceed.

The fifth segment of the microcode determines whether or not the command should continue. The microcode determines this by checking to see if an implied seek is needed, a new head is to be selected, or if the sequence should proceed to the next sector. If none of these functions is required and the sequencer resets the GO bit, the command terminates.

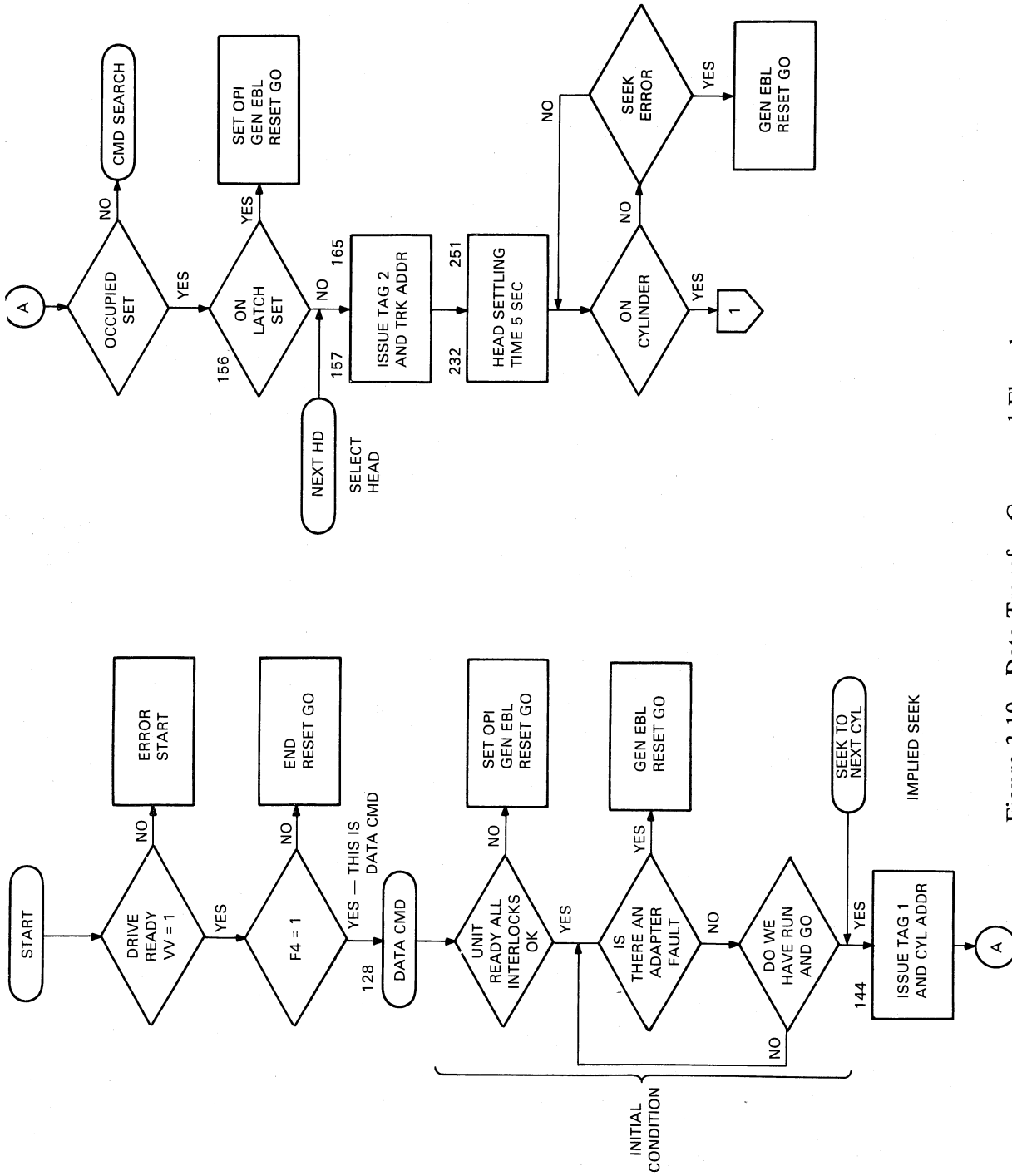
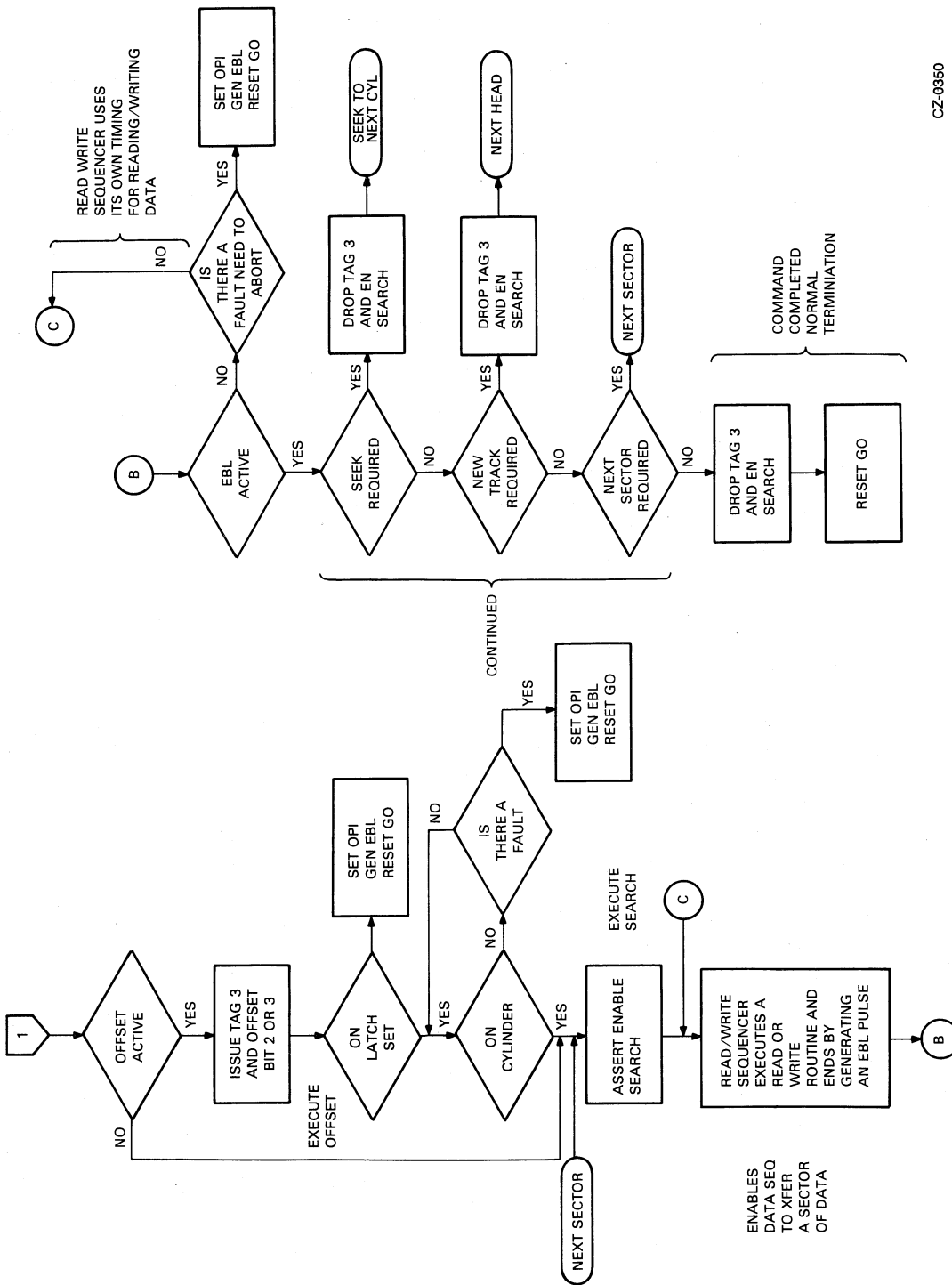


Figure 3-19 Data Transfer Command Flowchart
(Sheet 1 of 2)



CZ-0350

Figure 3-19 Data Transfer Command Flowchart (Sheet 2 of 2)

3.9.3.1 Write Data Execution – During a write data command, the RM adapter transfers 256 data words onto the disk for each sector specified by the controller. The RM adapter also generates a sync byte to precede the data field and a 32-bit ECC word after it. If the adapter detects an error (such as CRC, HCE, FMT or BSE) in the header, it aborts the command.

Figure 3-20 is a flowchart of the write data command. As with all data commands, the read/write sequencer takes control of the sector format synchronizing after a search is executed and a sector match is found. This results in the assertion of sector compare which permits the read/write PROM program counter to begin incrementing. The microcode asserts READ GATE at the word and sector count of 4 and then begins looking for the sync byte at word and sector count 11. After sync byte is detected, the first header word is read from the disk into the buffer at count 128. The header is then compared with the desired cylinder address. At count 129, the second header word is read from the disk and compared with the desired disk address register. At this point, the CRC word is read from the disk and checked for an HCRC error. This concludes the read header portion of the write command. The read gate is disabled, and write gate is enabled by the BR RD TO WRT L signal.

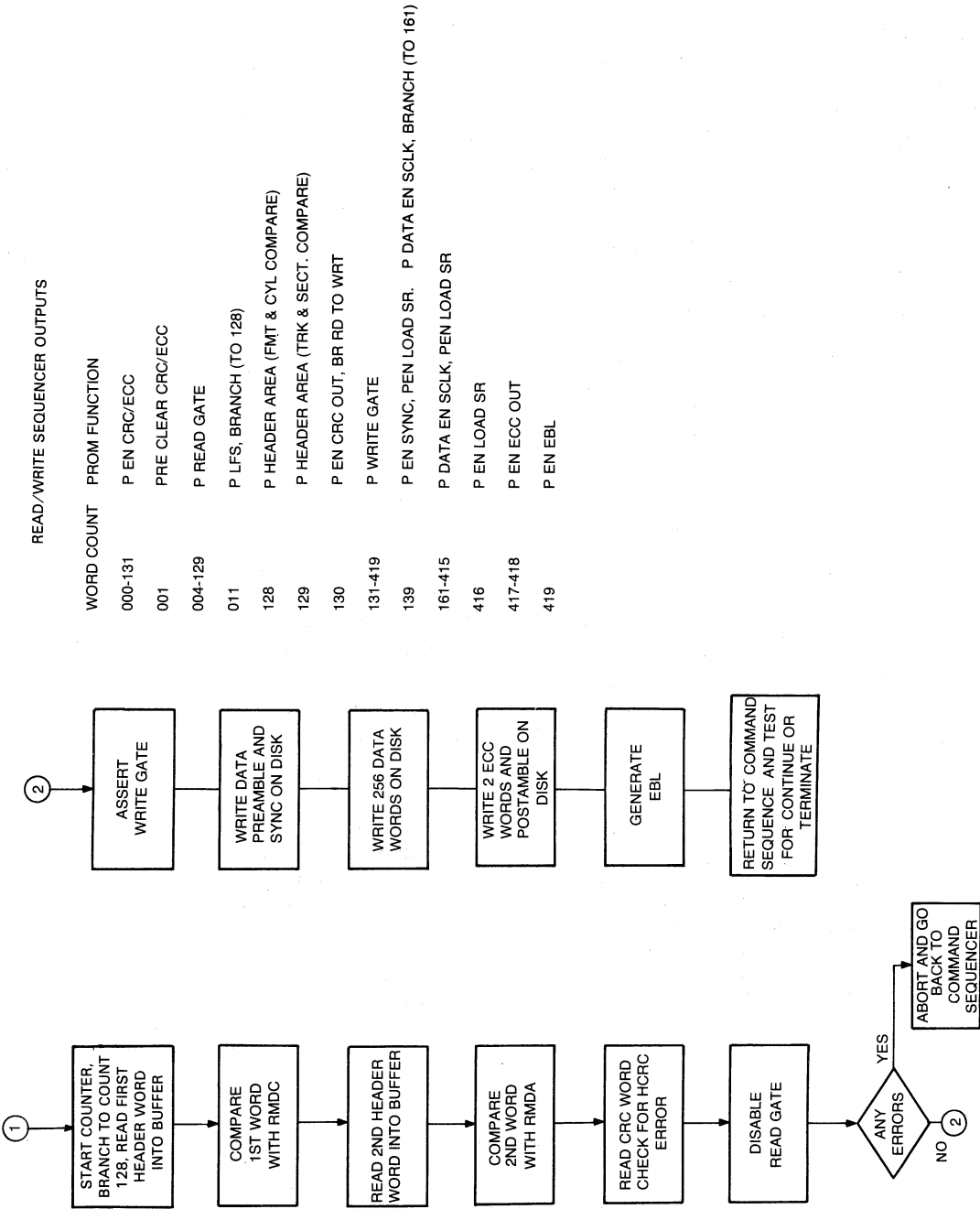
The write portion of the command begins by writing the header gap and sync byte on the disk. Data is then requested from the MASSBUS, 256 data words are written, and the data is gated to the ECC generation circuits during the writing process.

At this point, the RM adapter generates two ECC words and writes them on the disk followed by a postamble which completes the sector. The microcode then generates an EBL pulse to notify the command sequencer that it has finished the data portion of the command.

3.9.3.2 Read Data Execution – Figure 3-21 shows the flowchart for a read data command. The first 13 blocks in a read data command are the same as a write data command. Therefore, these blocks are not duplicated on this flowchart. These blocks are shown in Figure 3-20.

This flowchart deals with the operation of the read/write sequencer from the time it receives a SECTOR COMPARE signal until the end of that sector. When the command sequencer has finished the seek and head selection operations, it asserts EN SEARCH which initiates a search for the correct sector. When a sector match is found, the sequencer sets SECTOR COMPARE and the read/write sequencer begins incrementing. The READ GATE signal is enabled at word and sector count 4. At word and sector count 11, LOOK FOR SYNC is asserted and the counter is stopped. When the sync byte is detected, the word clock is started again. Beginning from clock pulse 128, the first header word is read into the data buffer and compared with the desired cylinder address. The format bit and bad sector flags are also checked at this time.

At count 129, a second header word is read from the disk and compared with the disk address register. If this is a read header and data command, both of these words are sent to the MASSBUS with SCLK pulses. At count 130, the CRC word is read and checked for HCRC errors. The read gate is disabled while testing for errors. The read gate is then enabled again at count 132 and looking for data sync begins at count 136. After sync is detected, data words are read from count 161 until a total of 256 data words are read. Each data word is shifted into the data buffer and through the ECC logic and parity generation circuitry and then onto the MASSBUS with a SCLK pulse. At count 417 and 418, two ECC words are read and compared with the words generated by the ECC logic for DCK errors. If no errors are found, an EBL pulse is generated to signal the command sequencer that the current sector has been read.



READ/WRITE SEQUENCER OUTPUTS

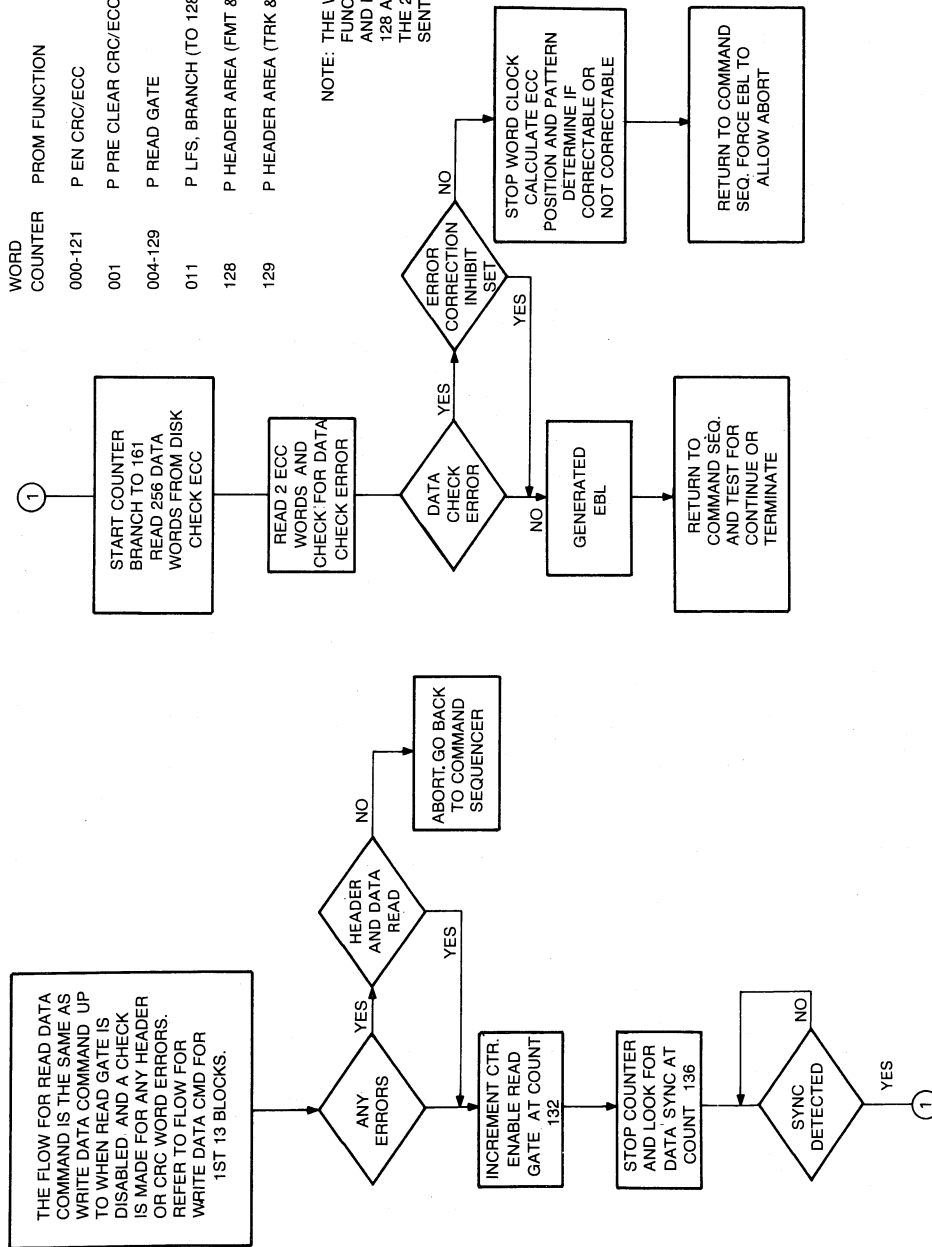
WORD COUNT	PROM FUNCTION
000-131	P EN CRC/ECC
001	PRE CLEAR CRC/ECC
004-129	P READ GATE
011	P LFS, BRANCH (TO 128)
128	P HEADER AREA (FMT & CYL COMPARE)
129	P HEADER AREA (TRK & SECT. COMPARE)
130	P EN CRC OUT, BR RD TO WRT
131-419	P WRITE GATE
139	P EN SYNC, PEN LOAD SR, P DATA EN SCLK, BRANCH (TO 161)
161-415	P DATA EN SCLK, PEN LOAD SR
416	P EN LOAD SR
417-418	P EN ECC OUT
419	P EN EBL

Figure 3-20 Write Data Command Flowchart

READ/WRITE SEQUENCER OUTPUTS

WORD COUNTER	PROM FUNCTION	130	P EN CRC OUT BR RD TO WRT
000-121	P EN CRC/ECC	132-417	P READ GATE
001	P PRE CLEAR CRC/ECC	136	P LFS, BRANCH (TO 161)
004-129	P READ GATE	161-416	P DATA EN SCLK
011	P LFS, BRANCH (TO 128)	416	LAST READ DATA
128	P HEADER AREA (FMT & CYL)	417-418	P EN ECC OUT
129	P HEADER AREA (TRK & SECTOR)	419	P EN EBL

NOTE: THE WORD COUNT AND PROM FUNCTIONS ARE THE SAME FOR READ HEADER AND DATA COMMAND, EXCEPT AT COUNTS 128 AND 129. SCLK IS GENERATED SO THE 2 HEADER WORDS CAN BE SENT TO MEMORY.



C2-0038

Figure 3-21 Read Data Command Flowchart

3.9.3.3 Write Header and Data Execution – This command formats the disk with gaps, headers, and data for specified sectors. The RH controller supplies 2 header words and 256 data words for each sector. The RM adapter generates the gaps including sync bytes, CRC word, and ECC words.

Figure 3-22 is a flowchart of the write header and data command. Once the sector compare signal is asserted, the read/write sequencer assumes control over the sector formatting. The read/write sequencer enables the word clock and write gate, and begins writing 27 bytes of 0s plus a sync byte on the disk. It then requests the two appropriate header words from the MASSBUS and writes them while generating their CRC code. Next, the read/write sequencer writes this CRC word and 17 bytes of data preamble on the disk. The preamble is ended by writing a sync byte, indicating the beginning of the data field. At this point, the RM adapter starts requesting data from the MASSBUS. A total of 256 data words are written followed by their 2-word ECC pattern. The postamble is the last to be written before generating an EBL pulse to notify the command sequencer to resume control.

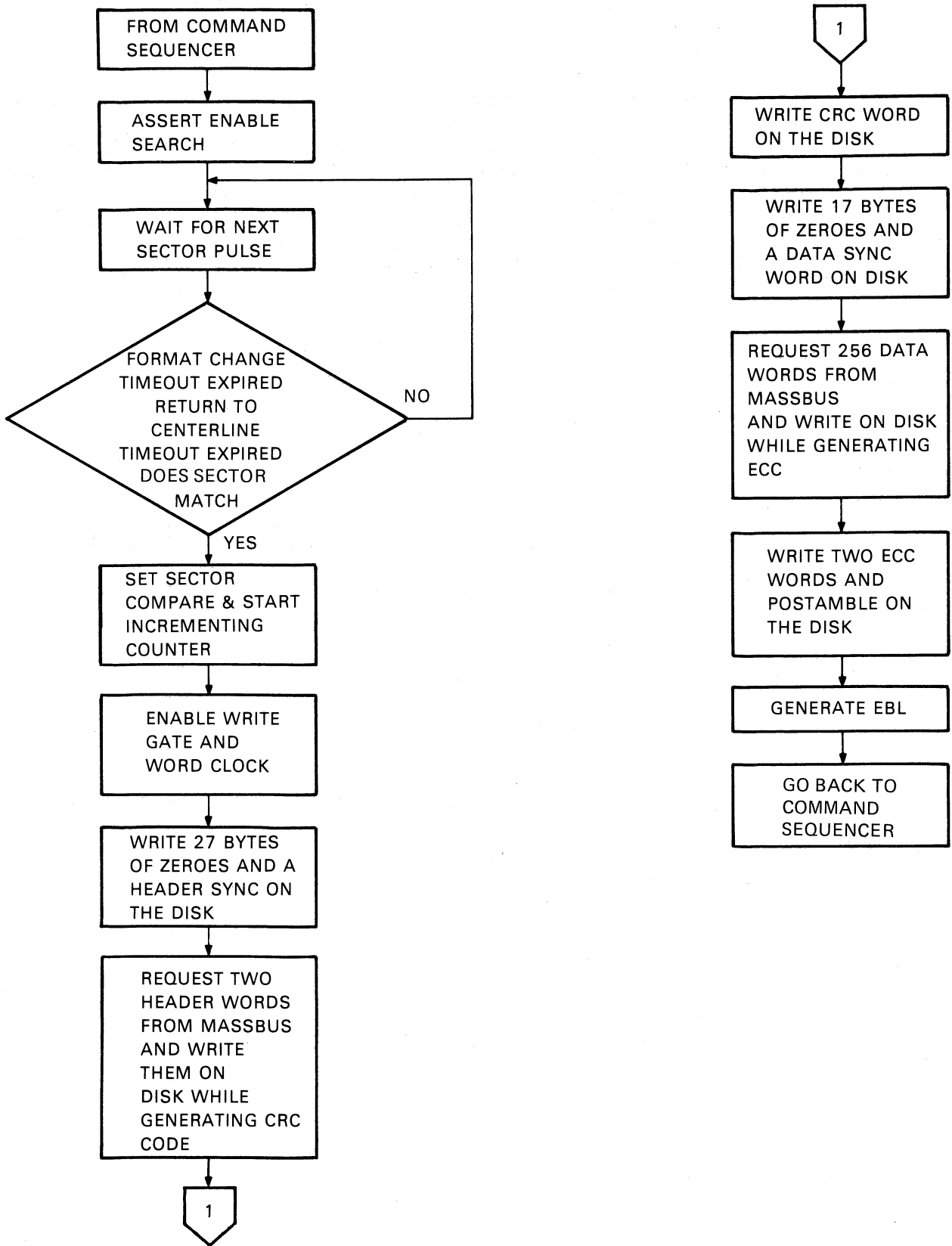


Figure 3-22 Write Header and Data Command Flowchart

MA-1693

CHAPTER 4 RM ADAPTER APPLICATIONS

4.1 INTRODUCTION

The first three chapters of this manual provide a general description of the RM adapter and its operation. This chapter, however, covers adapter modifications that must be made to compensate for different disk drive operating characteristics and special features.

4.2 ADAPTER DIFFERENCES

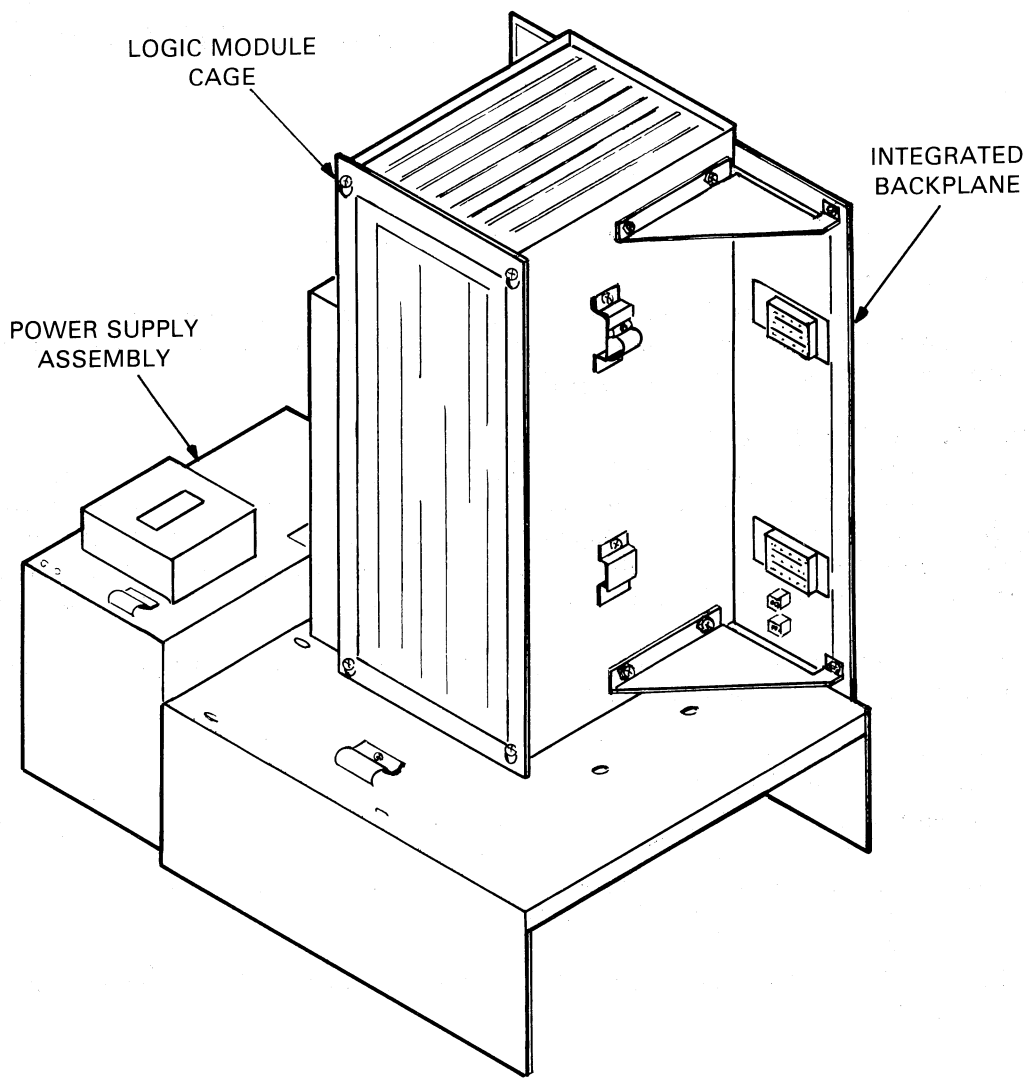
Adapter modifications are required because of differences in drive spindle speeds, disk storage capacities, number of tracks, special features such as skip sectoring, and whether or not the drive is equipped with the dual-port option. In order to compensate for these differences, the adapter changes that are required include such things as the addition or removal of jumper connections, the use of different data sequencer circuit modules, and changes in the bit assignments within the adapter registers.

The pages that follow provide separate coverage for each RM adapter/disk drive combination. Each section provides the information listed below.

- Adapter physical configuration
- Adapter mounting position within the cabinet
- Drive-type jumper connections on adapter backplane
- Circuit modules used
- Adapter register summary for specific drive involved
- Special wiring connections (if applicable)

Refer to Figure 1-4 for the locations of the drive-type connections and the circuit modules within the adapter card cage.

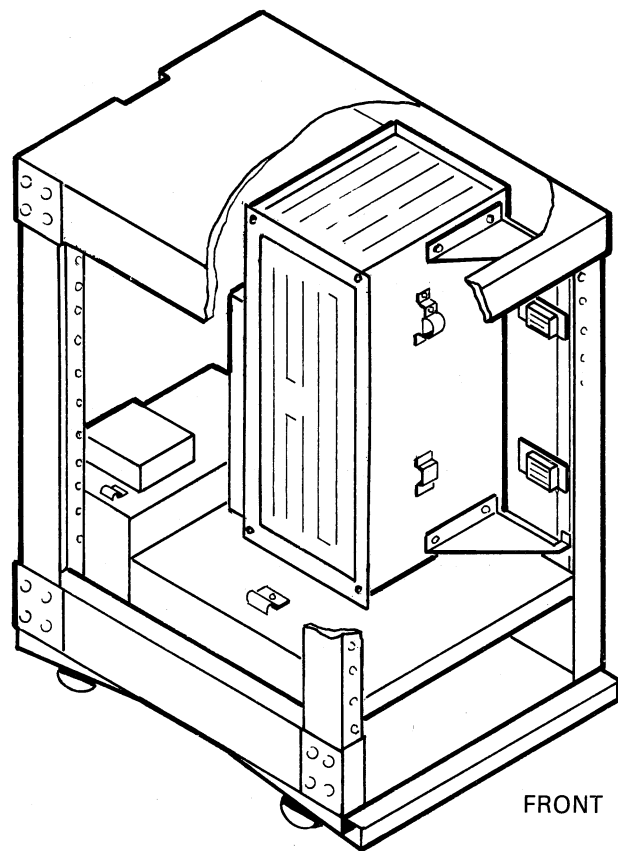
4.3 RM02 ADAPTER/DISK DRIVE COMBINATION



BACKPLANE AND CARD CAGE MOUNTED VERTICALLY

CZ-0310

Figure 4-1 RM02 Adapter Configuration

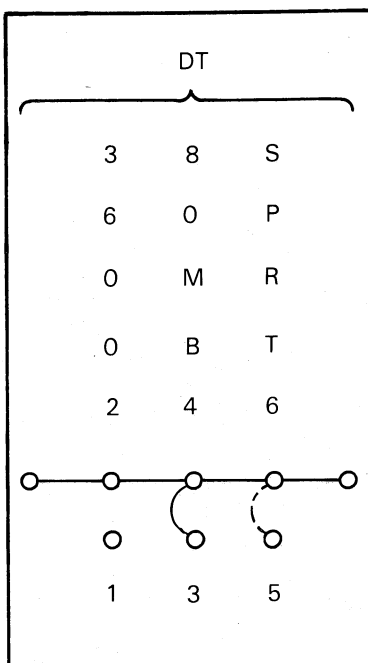


FRONT

CZ-0311

Figure 4-2 Adapter Position in Cabinet

Rear View of J1 on
Adapter Backplane



JUMPER 5-6: IN FOR PORT A ONLY;
OUT FOR EITHER PORT
OR DUAL PORT

JUMPER 3-4: IN

CZ-0312

Figure 4-3 RM02 Drive-Type Jumper Connections

Table 4-1 RM02 Adapter Circuit Modules

Module No.	Quantity	Description
M5923	2*	Port B transceiver
M5922	2	Port A transceiver
M7686/M7686-YA	1**	Control interface
M7685/M7685-YA/M8685	1***	Data sequencer
M7687	1	Drive interface
M7684	1	Control sequencer

* Used when equipped with dual-port option.

** YA version used when dual-port switches are mounted on cabinet door.

*** Any module can be used. M8685 is the newest version.

REGISTER DESIGNATION	REGISTER NAME	UNIBUS ADDRESS	MASSBUS ADDRESS	BIT ASSIGNMENTS																READ OR WRITE
				15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
RMCS1	CONTROL ①	(776700)	00	②	②	②	0	DVA	②	②	②	②	②	F4	F3	F2	F1	F0	GO	READ/WRITE
				② DEPENDS ON CONTROLLER USED																
RMDS1	DISK ADDRESS	(776706)	05	0	0	0	TA 16	TA 8	TA 4	TA 2	TA 1	0	0	0	SA 16	SA 8	SA 4	SA 2	SA 1	READ/WRITE
RMDS	DRIVE STATUS	(776712)	01	ATA	ERR	PIP	MOL	WRL	LBT	PGM	DPR	DRY	VV	0	0	0	0	0	OM	READ
RMER1	ERROR REGISTER NO. 1	(776714)	02	DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF	READ/WRITE
RMAS	ATTENTION SUMMARY	(776716)	04	0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0	READ/WRITE
RMLA	LOOK AHEAD	(776720)	07	0	0	0	0	0	SC 16	SC 8	SC 4	SC 2	SC 1	0	0	0	0	0	0	READ
RMMR1	MAINTENANCE REGISTER NO. 1	(776724)	03	OCC	R/G	EBL	REX	ESRC	PLFS	ECRC	PDA	PHA	CONT	WC	ECC	WD	LS	LST	DMD	READ
				DBCK	DBEM	DEBL	MSEN	MCLK	MRD	MUR	MOC	MSER	MDF	MS	MWP	MI	MSC	DMD	DMD	WRITE
RMDT	DRIVE TYPE	(776726)	06	0	0	MOH 1	0	DRO	0	0	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0	READ

CZ-0029

Figure 4-4 RM02 Adapter Register Summary
(Sheet 1 of 2)

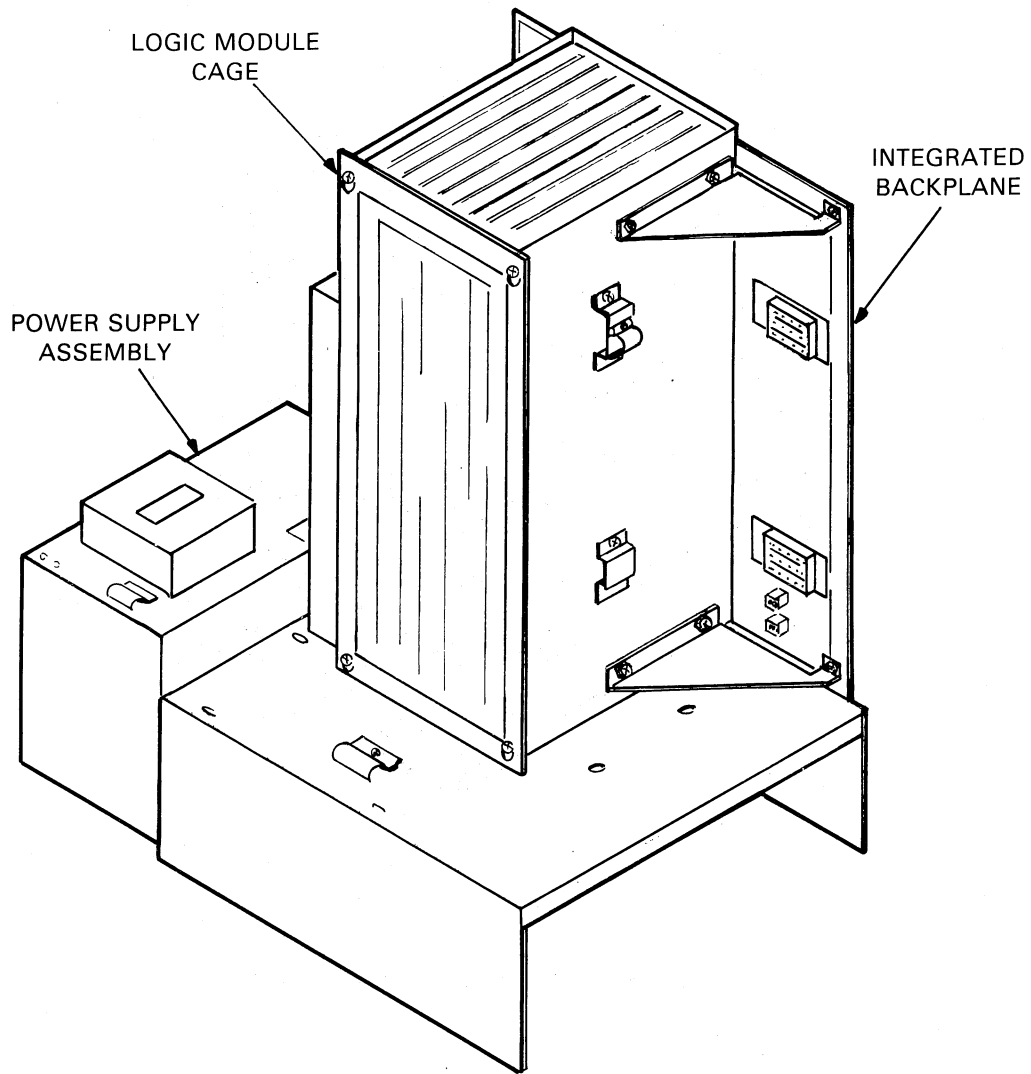
REGISTER DESIGNATION	REGISTER NAME	UNIBUS ADDRESS	MASSBUS ADDRESS	BIT ASSIGNMENTS																	
				15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		
RMSN	SERIAL NUMBER	(776730)	10	SN 8000	SN 4000	SN 2000	SN 1000	SN 800	SN 400	SN 200	SN 100	SN 80	SN 40	SN 20	SN 10	SN 8	SN 4	SN 2	SN 1	READ	
RMOF	OFFSET	(776732)	11	0	0	0	FMT 16 ^①	ECI	HCI	0	0	OFF DIR	0	0	0	0	0	0	0	0	READ/WRITE
RMDC	DESIRED CYLINDER	(776734)	12	0	0	0	0	0	0	DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1	READ/WRITE	
RMHR	HOLDING REGISTER	(776736)	13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	READ
RMMR2	MAINTENANCE REGISTER NO. 2	(776740)	14	ROA	ROB	TAG	TEST BIT	CC	CH	BB 9	BB 8	BB 7	BB 6	BB 5	BB 4	BB 3	BB 2	BB 1	BB 0	READ	
RMER2	ERROR REGISTER NO. 2	(776742)	15	BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0	READ/WRITE	
RMEC1	ECC POSITION	(776744)	16	0	0	0	P 4096	P 2048	P 1024	P 512	P 256	P 128	P 64	P 32	P 16	P 8	P 4	P 2	P 1	READ	
RMEC2	ECC PATTERN	(776746)	17	0	0	0	0	0	PAT 11	PAT 10	PAT 9	PAT 8	PAT 7	PAT 6	PAT 5	PAT 4	PAT 3	PAT 2	PAT 1	READ	

① 1 = 16-BIT WORD FORMAT; 0 = 18-BIT FORMAT

CZ-0813

Figure 4-4 RM02 Adapter Register Summary
(Sheet 2 of 2)

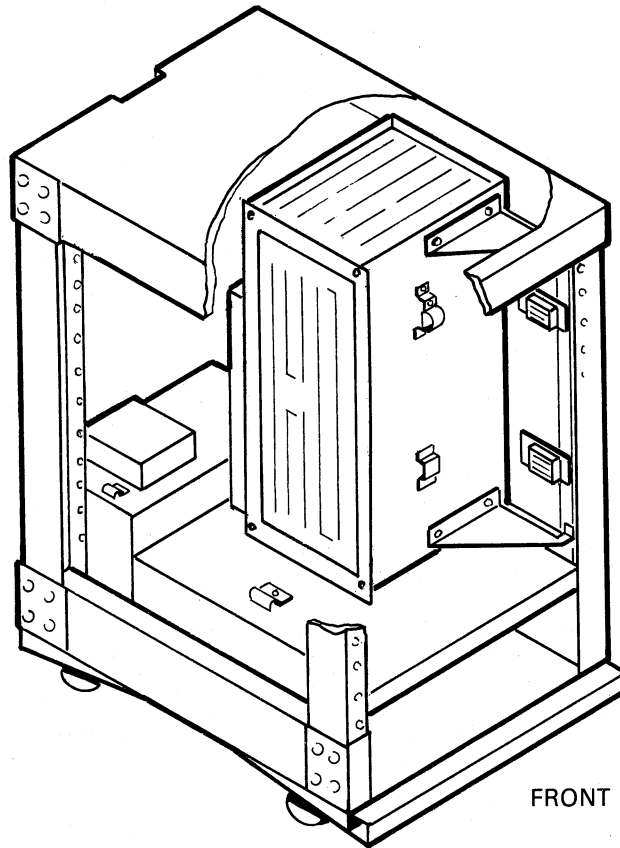
4.4 RM03 ADAPTER/DISK DRIVE COMBINATION



BACKPLANE AND CARD CAGE MOUNTED VERTICALLY

CZ-0310

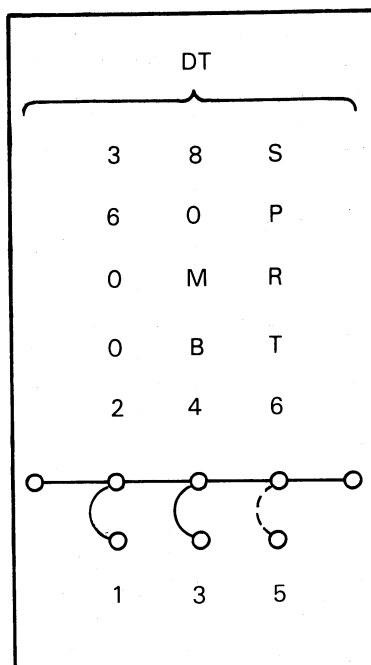
Figure 4-5 RM03 Adapter Configuration



CZ-0311

Figure 4-6 Adapter Position in Cabinet

Rear View of J1 on
Adapter Backplane



JUMPER 5-6: IN FOR PORT A ONLY;
OUT FOR EITHER PORT
OR DUAL PORT

JUMPERS 1-2, 3-4: IN

CZ-0314

Figure 4-7 RM03 Drive-Type Jumper Connections

Table 4-2 RM03 Adapter Circuit Modules

Module No.	Quantity	Description
M5923	2*	Port B transceiver
M5922	2	Port A transceiver
M7686/M7686-YA	1**	Control interface
M7685/M7685-YA/M8685	1***	Data sequencer
M7687	1	Drive interface
M7684	1	Control sequencer

* Used when equipped with dual-port option.

** YA version used when dual-port switches are mounted on the cabinet door.

*** Any module can be used. M8685 is the newest version.

REGISTER DESIGNATION	REGISTER NAME	UNIBUS ADDRESS	MSSBUS ADDRESS	BIT ASSIGNMENTS ¹																READ OR WRITE
				15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
RMCS1	CONTROL ①	(776700)	00	②	②	②	0	DVA	②	②	②	F4	F3	F2	F1	F0	GO	READ/WRITE		
② DEPENDS ON CONTROLLER USED																				
RMDA	DISK ADDRESS	(776706)	05	0	0	0	TA 16	TA 8	TA 4	TA 2	TA 1	0	0	SA 16	SA 8	SA 4	SA 2	SA 1	READ/WRITE	
RMDS	DRIVE STATUS	(776712)	01	ATA	ERR	PIP	MOL	WRL	LBT	PGM	DPR	DRY	VV	0	0	0	0	OM	READ	
RMER1	ERROR REGISTER NO. 1	(776714)	02	DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF	READ/WRITE
RMAS	ATTENTION SUMMARY	(776716)	04	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0	READ/WRITE	
RMLA	LOOK AHEAD	(776720)	07	0	0	0	0	0	SC 16	SC 8	SC 4	SC 2	SC 1	0	0	0	0	0	READ	
RMMR1	MAINTENANCE REGISTER NO. 1	(776724)	03	OCC	R/G	EBL	REX	ESRC	PLFS	ECRC	PDA	PHA	CONT	WC	EECC	WD	LS	LST	DMD	READ
				DBCK	DBEM	DEBL	MSEN	MCLK	MRD	MUR	MOC	MSER	MDF	MS	MWP	MI	MSC	DMD	DMD	WRITE
RMDT	DRIVE TYPE	(776726)	06	0	0	MOH 1	0	DRQ	0	0	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0	READ

CZ-0269

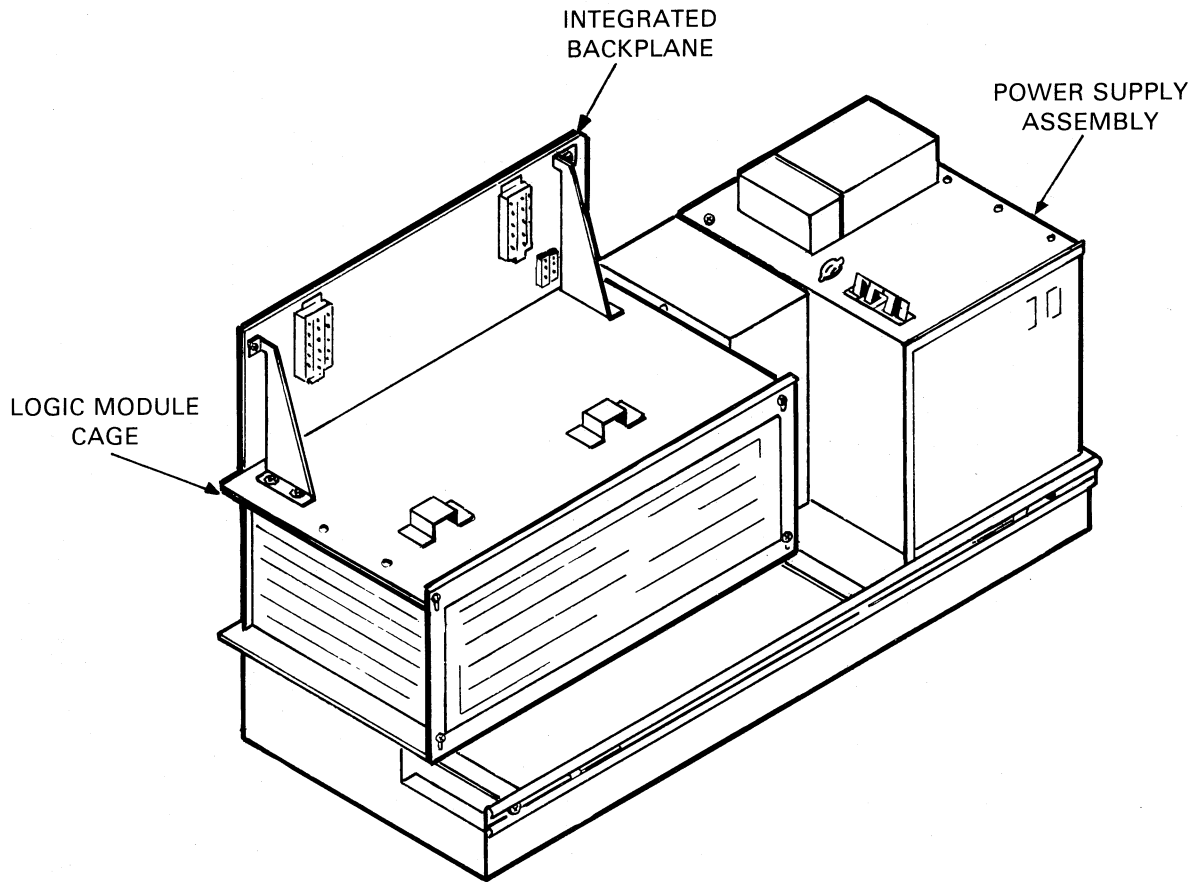
Figure 4-8 RM03 Adapter Register Summary
(Sheet 1 of 2)

REGISTER DESIGNATION	REGISTER NAME	UNIBUS ADDRESS	MASSBUS ADDRESS	BIT ASSIGNMENTS																	
				15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		
RM5N	SERIAL NUMBER	(776730)	10	SN 8000	SN 4000	SN 2000	SN 1000	SN 800	SN 400	SN 200	SN 100	SN 80	SN 40	SN 20	SN 10	SN 8	SN 4	SN 2	SN 1	READ	
RM0F	OFFSET	(776732)	11	0	0	0	FMT 16 ₀	ECI	HCI	0	0	OFF DIR	0	0	0	0	0	0	0	0	READ/WRITE
				① 1 = 16-BIT WORD FORMAT; 0 = 18-BIT FORMAT																	
RMDC	DESIRED CYLINDER	(776734)	12	0	0	0	0	0	0	DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1	READ/WRITE	
RMHR	HOLDING REGISTER	(776736)	13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	READ
RMMR2	MAINTENANCE REGISTER NO. 2	(776740)	14	ROA	ROB	TAG	TEST BIT	CC	CH	BB 9	BB 8	BB 7	BB 6	BB 5	BB 4	BB 3	BB 2	BB 1	BB 0	READ	
RMER2	ERROR REGISTER NO. 2	(776742)	15	BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0	READ/WRITE	
RMEC1	ECC POSITION	(776744)	16	0	0	0	P 4096	P 2048	P 1024	P 512	P 256	P 128	P 64	P 32	P 16	P 8	P 4	P 2	P 1	READ	
RMEC2	ECC PATTERN	(776746)	17	0	0	0	0	0	PAT 11	PAT 10	PAT 9	PAT 8	PAT 7	PAT 6	PAT 5	PAT 4	PAT 3	PAT 2	PAT 1	READ	

C2-0813

Figure 4-8 RM03 Adapter Register Summary
(Sheet 2 of 2)

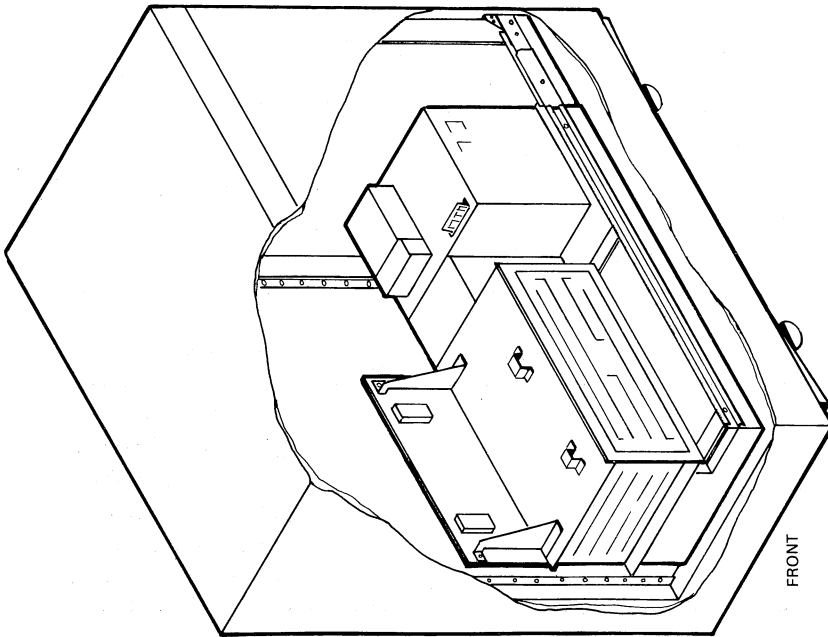
4.5 RM05 ADAPTER/DISK DRIVE COMBINATION



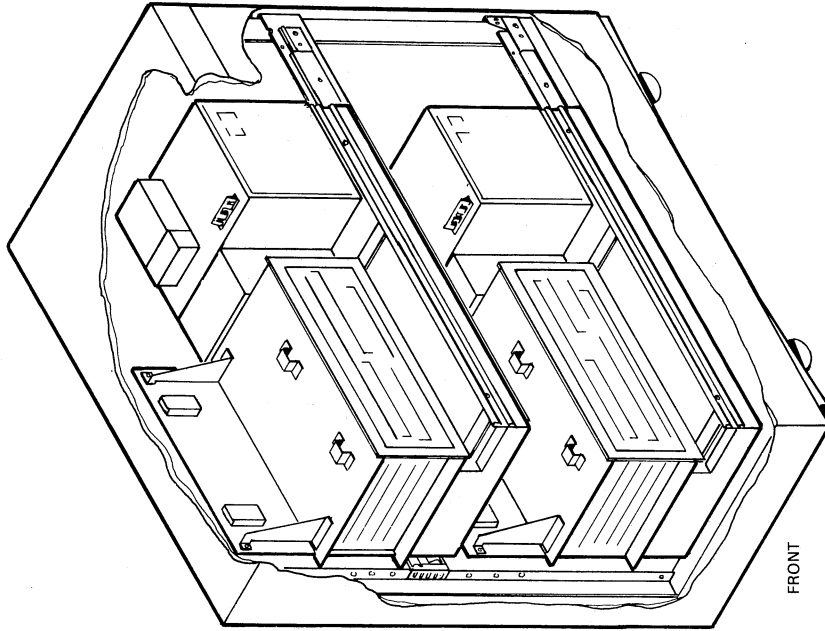
BACKPLANE AND CARD CAGE MOUNTED HORIZONTALLY

CZ-0315

Figure 4-9 RM05 Adapter Configuration



(A) One Adapter

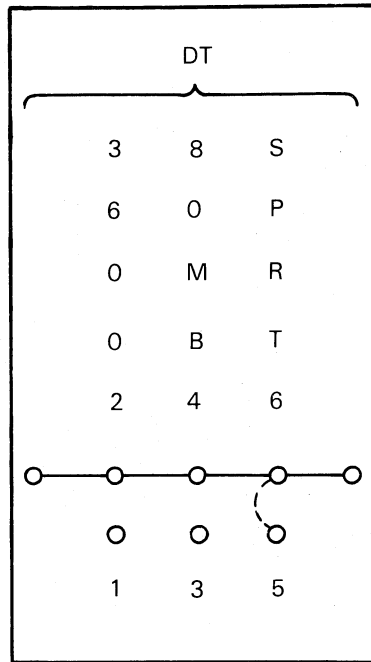


(B) Two Adapters

CZ-0316

Figure 4-10 Adapter Position(s) in Cabinet

Rear View of J1 on
Adapter Backplane



JUMPER 5-6: IN FOR PORT A ONLY;
OUT FOR EITHER PORT
OR DUAL PORT

CZ-0317

Figure 4-11 RM05 Drive-Type Jumper Connection

Table 4-3 RM05 Adapter Circuit Modules

Module No.	Quantity Per Adapter	Description
M5923	2*	Port B transceiver
M5922	2	Port A transceiver
M7686-YA	1	Control interface
M7685-YA/M8685	1**	Data sequencer
M7687	1	Drive interface
M7684	1	Control sequencer

* Used when equipped with dual-port option.

** Either module can be used. M8685 is the newer version.

REGISTER DESIGNATION	REGISTER NAME	UNIBUS ADDRESS	MASSBUS ADDRESS	BIT ASSIGNMENTS												READ OR WRITE				
				15	14	13	12	11	10	09	08	07	06	05	04		03	02	01	00
RMCS1	CONTROL ①	(776700)	00	②	②	②	0	DVA	②	②	②	②	F4	F3	F2	F1	F0	GO	READ/WRITE	
				② DEPENDS ON CONTROLLER USED																
RMDA	DISK ADDRESS	(776706)	05	0	0	0	TA 16	TA 8	TA 4	TA 2	TA 1	0	0	SA 16	SA 8	SA 4	SA 2	SA 1	READ/WRITE	
RMDS	DRIVE STATUS	(776712)	01	ATA	ERR	PIP	MOL	WRL	LBT	PGM	DPR	DRY	VV	0	0	0	0	OM	READ	
RMER1	ERROR REGISTER NO. 1	(776714)	02	DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRG	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF	READ/WRITE
RMAS	ATTENTION SUMMARY	(776716)	04	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0	READ/WRITE	
RMLA	LOOK AHEAD	(776720)	07	0	0	0	0	0	SC 16	SC 8	SC 4	SC 2	SC 1	0	0	0	0	0	READ	
RMMR1	MAINTENANCE REGISTER NO. 1	(776724)	03	OCC DBCK	R/G DBEM	EBL DEBL	REX MSEN	ESRC MCLK	PLFS MRD	ECRC MUR	PDA MOC	PHA MSER	CONT MDF	WC MS	EECC	WD MWP	LS MI	LST MSC	DMD DMD	READ WRITE
RMDT	DRIVE TYPE	(776726)	06	0	0	MOH 1	0	DRQ	0	0	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0	READ

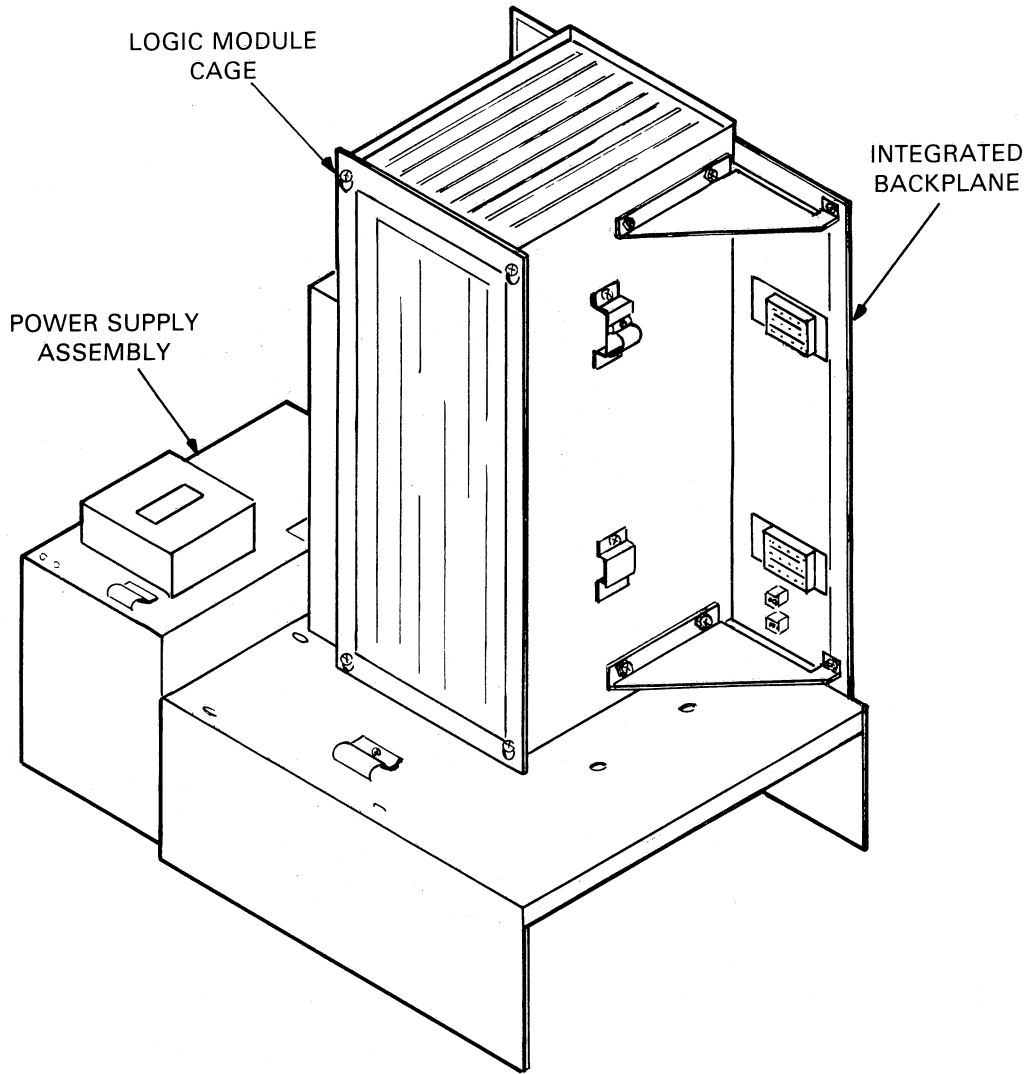
CZ-0351

Figure 4-12 RM05 Adapter Register Summary
(Sheet 1 of 2)

REGISTER DESIGNATION	REGISTER NAME	UNIBUS ADDRESS	MASSBUS ADDRESS	BIT ASSIGNMENTS																	
				15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		
RMSN	SERIAL NUMBER	(776730)		SN 8000	SN 4000	SN 2000	SN 1000	SN 800	SN 400	SN 200	SN 100	SN 80	SN 40	SN 20	SN 10	SN 8	SN 4	SN 2	SN 1	READ	
RMOF	OFFSET	(776732)		0	0	0	FMT 16 ^①	ECI	HCI	0	0	OFF DIR	0	0	0	0	0	0	0	0	READ/WRITE
				① 1 = 16-BIT WORD FORMAT, 0 = 18-BIT FORMAT																	
RMDC	DESIRED CYLINDER	(776734)		0	0	0	0	DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1	READ/WRITE			
RMHR	HOLDING REGISTER	(776736)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	READ
RMMR2	MAINTENANCE REGISTER NO. 2	(776740)		ROA	ROB	TAG	TEST BIT	CC	CH	BB 9	BB 8	BB 7	BB 6	BB 5	BB 4	BB 3	BB 2	BB 1	BB 0	READ	
RMER2	ERROR REGISTER NO. 2	(776742)		BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0	READ/WRITE	
RMEC1	ECC POSITION	(776744)		0	0	0	P 4096	P 2048	P 1024	P 512	P 256	P 128	P 64	P 32	P 16	P 8	P 4	P 2	P 1	READ	
RMEC2	ECC PATTERN	(776746)		0	0	0	0	0	PAT 11	PAT 10	PAT 9	PAT 8	PAT 7	PAT 6	PAT 5	PAT 4	PAT 3	PAT 2	PAT 1	READ	

Figure 4-12 RM05 Adapter Register Summary (Sheet 2 of 2)

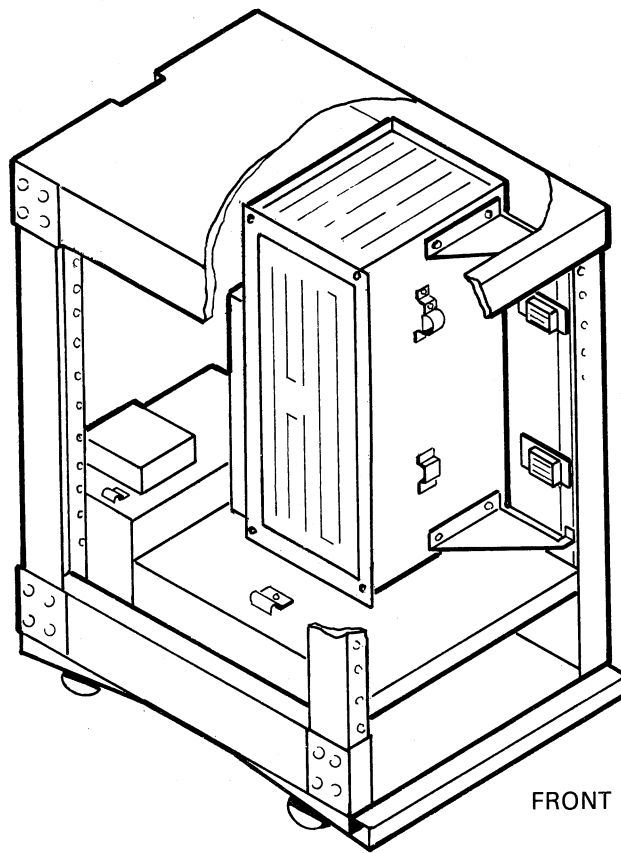
4.6 RM80 ADAPTER/DISK DRIVE COMBINATION



BACKPLANE AND CARD CAGE MOUNTED VERTICALLY

CZ-0310

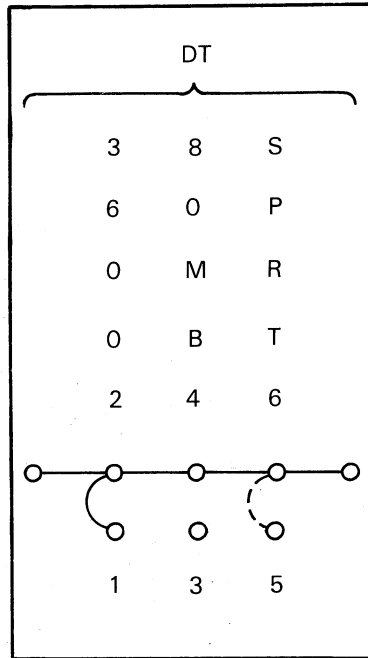
Figure 4-13 RM80 Adapter Configuration



CZ-0311

Figure 4-14 Adapter Position in Cabinet

Rear View of J1 on
Adapter Backplane



JUMPER 5-6: IN FOR PORT A ONLY;
OUT FOR EITHER PORT
OR DUAL PORT

JUMPER 1-2: IN

CZ-0318

Figure 4-15 RM80 Drive-Type Jumper Connections

Table 4-4 RM80 Adapter Circuit Modules

Module No.	Quantity	Description
M5923	2*	Port B transceiver
M5922	2	Port A transceiver
M7686/M7686-YA	1**	Control interface
M8685	1	Data sequencer
M7687	1	Drive interface
M7684	1	Control sequencer

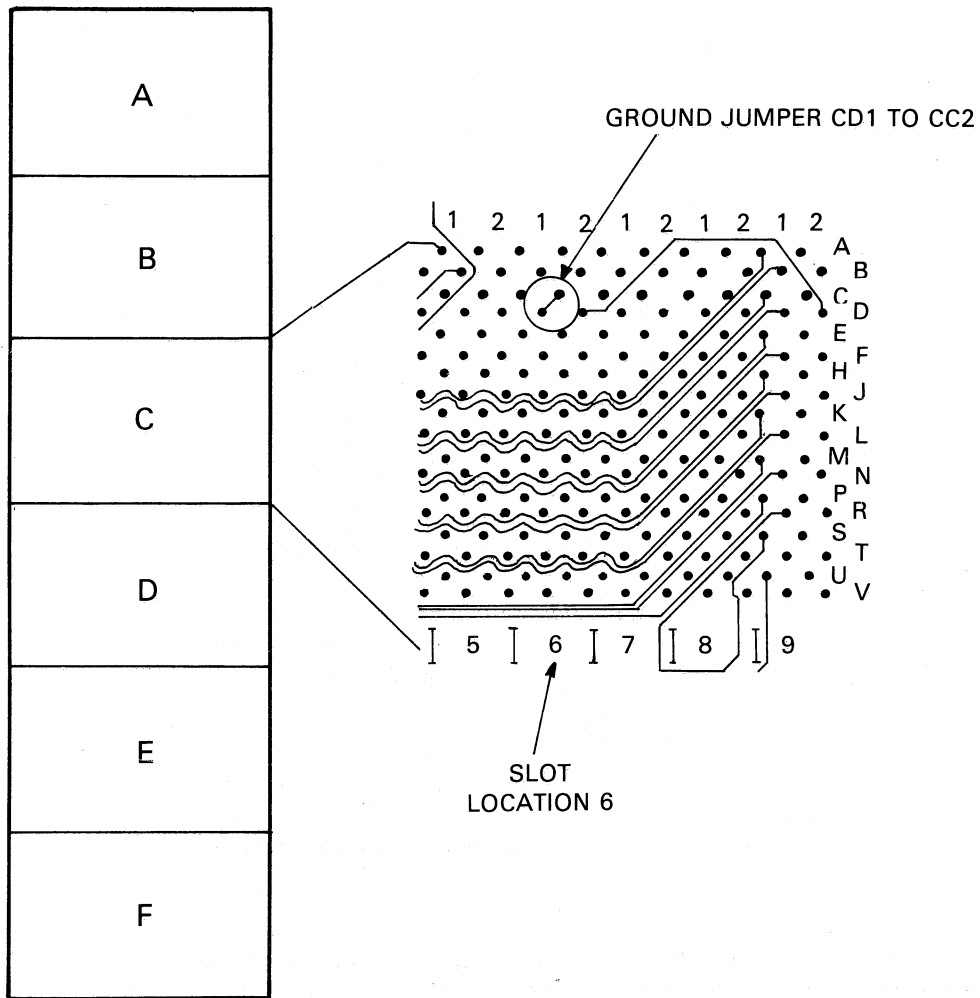
* Used when equipped with dual-port option.

** YA version used when dual-port switches are mounted on cabinet door.

4.6.1 Backplane Jumper Connection

A special jumper connection is required on the backplane of the RM80 Adapter. This jumper modifies the cylinder addressing arrangement so that the adapter will be compatible with the R80 drive unit. The jumper must be connected on the rear of the backplane between CD1 and CC2 (ground). Refer to Figure 4-16.

SIX MAJOR PIN FIELDS
ON REAR OF
ADAPTER BACKPLANE



CZ-0204

Figure 4-16 RM80 Jumper Location on Adapter Backplane

4.6.2 Adapter Register Summary

Figure 4-17 illustrates the bit assignments in the RM80 Adapter registers. The major difference between these bit assignments and those associated with other drives is the addition of the SSE1 bit in the offset register and the SSE bit in error register 2. Both of these bits are related to a special skip-sector feature used exclusively in the RM80.

REGISTER DESIGNATION	REGISTER NAME	UNIBUS ADDRESS	MASSBUS ADDRESS	BIT ASSIGNMENTS												READ OR WRITE																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
				15	14	13	12	11	10	09	08	07	06	05	04		03	02	01	00																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																													
RMCS1	CONTROL ①	(776700)	00	②	②	②	②	②	②	②	②	②	②	②	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20	F21	F22	F23	F24	F25	F26	F27	F28	F29	F30	F31	F32	F33	F34	F35	F36	F37	F38	F39	F40	F41	F42	F43	F44	F45	F46	F47	F48	F49	F50	F51	F52	F53	F54	F55	F56	F57	F58	F59	F60	F61	F62	F63	F64	F65	F66	F67	F68	F69	F70	F71	F72	F73	F74	F75	F76	F77	F78	F79	F80	F81	F82	F83	F84	F85	F86	F87	F88	F89	F90	F91	F92	F93	F94	F95	F96	F97	F98	F99	F100	F101	F102	F103	F104	F105	F106	F107	F108	F109	F110	F111	F112	F113	F114	F115	F116	F117	F118	F119	F120	F121	F122	F123	F124	F125	F126	F127	F128	F129	F130	F131	F132	F133	F134	F135	F136	F137	F138	F139	F140	F141	F142	F143	F144	F145	F146	F147	F148	F149	F150	F151	F152	F153	F154	F155	F156	F157	F158	F159	F160	F161	F162	F163	F164	F165	F166	F167	F168	F169	F170	F171	F172	F173	F174	F175	F176	F177	F178	F179	F180	F181	F182	F183	F184	F185	F186	F187	F188	F189	F190	F191	F192	F193	F194	F195	F196	F197	F198	F199	F200	F201	F202	F203	F204	F205	F206	F207	F208	F209	F210	F211	F212	F213	F214	F215	F216	F217	F218	F219	F220	F221	F222	F223	F224	F225	F226	F227	F228	F229	F230	F231	F232	F233	F234	F235	F236	F237	F238	F239	F240	F241	F242	F243	F244	F245	F246	F247	F248	F249	F250	F251	F252	F253	F254	F255	F256	F257	F258	F259	F260	F261	F262	F263	F264	F265	F266	F267	F268	F269	F270	F271	F272	F273	F274	F275	F276	F277	F278	F279	F280	F281	F282	F283	F284	F285	F286	F287	F288	F289	F290	F291	F292	F293	F294	F295	F296	F297	F298	F299	F300	F301	F302	F303	F304	F305	F306	F307	F308	F309	F310	F311	F312	F313	F314	F315	F316	F317	F318	F319	F320	F321	F322	F323	F324	F325	F326	F327	F328	F329	F330	F331	F332	F333	F334	F335	F336	F337	F338	F339	F340	F341	F342	F343	F344	F345	F346	F347	F348	F349	F350	F351	F352	F353	F354	F355	F356	F357	F358	F359	F360	F361	F362	F363	F364	F365	F366	F367	F368	F369	F370	F371	F372	F373	F374	F375	F376	F377	F378	F379	F380	F381	F382	F383	F384	F385	F386	F387	F388	F389	F390	F391	F392	F393	F394	F395	F396	F397	F398	F399	F400	F401	F402	F403	F404	F405	F406	F407	F408	F409	F410	F411	F412	F413	F414	F415	F416	F417	F418	F419	F420	F421	F422	F423	F424	F425	F426	F427	F428	F429	F430	F431	F432	F433	F434	F435	F436	F437	F438	F439	F440	F441	F442	F443	F444	F445	F446	F447	F448	F449	F450	F451	F452	F453	F454	F455	F456	F457	F458	F459	F460	F461	F462	F463	F464	F465	F466	F467	F468	F469	F470	F471	F472	F473	F474	F475	F476	F477	F478	F479	F480	F481	F482	F483	F484	F485	F486	F487	F488	F489	F490	F491	F492	F493	F494	F495	F496	F497	F498	F499	F500	F501	F502	F503	F504	F505	F506	F507	F508	F509	F510	F511	F512	F513	F514	F515	F516	F517	F518	F519	F520	F521	F522	F523	F524	F525	F526	F527	F528	F529	F530	F531	F532	F533	F534	F535	F536	F537	F538	F539	F540	F541	F542	F543	F544	F545	F546	F547	F548	F549	F550	F551	F552	F553	F554	F555	F556	F557	F558	F559	F560	F561	F562	F563	F564	F565	F566	F567	F568	F569	F570	F571	F572	F573	F574	F575	F576	F577	F578	F579	F580	F581	F582	F583	F584	F585	F586	F587	F588	F589	F590	F591	F592	F593	F594	F595	F596	F597	F598	F599	F600	F601	F602	F603	F604	F605	F606	F607	F608	F609	F610	F611	F612	F613	F614	F615	F616	F617	F618	F619	F620	F621	F622	F623	F624	F625	F626	F627	F628	F629	F630	F631	F632	F633	F634	F635	F636	F637	F638	F639	F640	F641	F642	F643	F644	F645	F646	F647	F648	F649	F650	F651	F652	F653	F654	F655	F656	F657	F658	F659	F660	F661	F662	F663	F664	F665	F666	F667	F668	F669	F670	F671	F672	F673	F674	F675	F676	F677	F678	F679	F680	F681	F682	F683	F684	F685	F686	F687	F688	F689	F690	F691	F692	F693	F694	F695	F696	F697	F698	F699	F700	F701	F702	F703	F704	F705	F706	F707	F708	F709	F710	F711	F712	F713	F714	F715	F716	F717	F718	F719	F720	F721	F722	F723	F724	F725	F726	F727	F728	F729	F730	F731	F732	F733	F734	F735	F736	F737	F738	F739	F740	F741	F742	F743	F744	F745	F746	F747	F748	F749	F750	F751	F752	F753	F754	F755	F756	F757	F758	F759	F760	F761	F762	F763	F764	F765	F766	F767	F768	F769	F770	F771	F772	F773	F774	F775	F776	F777	F778	F779	F780	F781	F782	F783	F784	F785	F786	F787	F788	F789	F790	F791	F792	F793	F794	F795	F796	F797	F798	F799	F800	F801	F802	F803	F804	F805	F806	F807	F808	F809	F810	F811	F812	F813	F814	F815	F816	F817	F818	F819	F820	F821	F822	F823	F824	F825	F826	F827	F828	F829	F830	F831	F832	F833	F834	F835	F836	F837	F838	F839	F840	F841	F842	F843	F844	F845	F846	F847	F848	F849	F850	F851	F852	F853	F854	F855	F856	F857	F858	F859	F860	F861	F862	F863	F864	F865	F866	F867	F868	F869	F870	F871	F872	F873	F874	F875	F876	F877	F878	F879	F880	F881	F882	F883	F884	F885	F886	F887	F888	F889	F890	F891	F892	F893	F894	F895	F896	F897	F898	F899	F900	F901	F902	F903	F904	F905	F906	F907	F908	F909	F910	F911	F912	F913	F914	F915	F916	F917	F918	F919	F920	F921	F922	F923	F924	F925	F926	F927	F928	F929	F930	F931	F932	F933	F934	F935	F936	F937	F938	F939	F940	F941	F942	F943	F944	F945	F946	F947	F948	F949	F950	F951	F952	F953	F954	F955	F956	F957	F958	F959	F960	F961	F962	F963	F964	F965	F966	F967	F968	F969	F970	F971	F972	F973	F974	F975	F976	F977	F978	F979	F980	F981	F982	F983	F984	F985	F986	F987	F988	F989	F990	F991	F992	F993	F994	F995	F996	F997	F998	F999	F1000	F1001	F1002	F1003	F1004	F1005	F1006	F1007	F1008	F1009	F1010	F1011	F1012	F1013	F1014	F1015	F1016	F1017	F1018	F1019	F1020	F1021	F1022	F1023	F1024	F1025	F1026	F1027	F1028	F1029	F1030	F1031	F1032	F1033	F1034	F1035	F1036	F1037	F1038	F1039	F1040	F1041	F1042	F1043	F1044	F1045	F1046	F1047	F1048	F1049	F1050	F1051	F1052	F1053	F1054	F1055	F1056	F1057	F1058	F1059	F1060	F1061	F1062	F1063	F1064	F1065	F1066	F1067	F1068	F1069	F1070	F1071	F1072	F1073	F1074	F1075	F1076	F1077	F1078	F1079	F1080	F1081	F1082	F1083	F1084	F1085	F1086	F1087	F1088	F1089	F1090	F1091	F1092	F1093	F1094	F1095	F1096	F1097	F1098	F1099	F1100	F1101	F1102	F1103	F1104	F1105	F1106	F1107	F1108	F1109	F1110	F1111	F1112	F1113	F1114	F1115	F1116	F1117	F1118	F1119	F1120	F1121	F1122	F1123	F1124	F1125	F1126	F1127	F1128	F1129	F1130	F1131	F1132	F1133	F1134	F1135	F1136	F1137	F1138	F1139	F1140	F1141	F1142	F1143	F1144	F1145	F1146	F1147	F1148	F1149	F1150	F1151	F1152	F1153	F1154	F1155	F1156	F1157	F1158	F1159	F1160	F1161	F1162	F1163	F1164	F1165	F1166	F1167	F1168	F1169	F1170	F1171	F1172	F1173	F1174	F1175	F1176	F1177	F1178	F1179	F1180	F1181	F1182	F1183	F1184	F1185	F1186	F1187	F1188	F1189	F1190	F1191	F1192	F1193	F1194	F1195	F1196	F1197	F1198	F1199	F1200	F1201	F1202	F1203	F1204	F1205	F1206	F1207	F1208	F1209	F1210	F1211	F1212	F1213	F1214	F1215	F1216	F1217	F1218	F1219	F1220	F1221	F1222	F1223	F1224	F1225	F1226	F1227	F1228	F1229	F1230	F1231	F1232	F1233	F1234	F1235	F1236	F1237	F1238	F1239	F1240	F1241	F1242	F1243	F1244	F1245	F1246	F1247	F1248	F1249	F1250	F1251	F1252	F1253	F1254	F1255	F1256	F1257	F1258	F1259	F1260	F1261	F1262	F1263	F1264	F1265	F1266	F1267	F1268	F1269	F1270	F1271	F1272	F1273	F1274	F1275	F1276	F1277	F1278	F1279	F1280	F1281	F1282	F1283	F1284	F1285	F1286	F1287	F1288	F1289	F1290	F1291	F1292	F1293	F1294	F1295	F1296	F1297	F1298	F1299	F1300	F1301	F1302	F1303	F1304	F1305	F1306	F1307	F1308	F1309	F1310	F1311	F1312	F1313	F1314	F1315	F1316	F1317	F1318	F1319	F1320	F1321	F1322	F1323	F1324	F1325	F1326	F1327	F1328	F1329	F1330	F1331	F1332	F1333	F1334	F1335	F1336	F1337	F1338	F1339	F1340	F1341	F1342	F1343	F1344	F1345	F1346	F1347	F1348	F1349	F1350	F1351	F1352	F1353	F1354	F1355	F1356	F1357	F1358	F1359	F1360	F1361	F1362	F1363	F1364	F1365	F1366	F1367	F1368	F1369	F1370	F1371	F1372	F1373	F1374	F1375	F1376	F1377	F1378	F1379	F1380	F1381	F1382	F1383	F1384	F1385	F1386	F1387	F1388	F1389	F1390	F1391	F1392	F1393	F1394	F1395	F1396	F1397	F1398	F1399	F1400	F1401	F1402	F1403	F1404	F1405	F1406	F1407	F1408	F1409	F1410	F1411	F1412	F1413	F1414	F1415	F1416	F1417	F1418	F1419	F1420	F1421	F1422	F1423	F1424	F1425	F1426	F1427	F1428	F1429	F1430	F1431	F1432	F1433	F1434	F1435	F1436	F1437	F1438	F1439	F1440	F1441	F1442	F1443	F1444	F1445	F1446	F1447	F1448	F1449	F1450	F1451	F1452	F1453	F1454	F1455	F1456	F1457	F1458

REGISTER DESIGNATION	REGISTER NAME	UNIBUS ADDRESS	MASSBUS ADDRESS	BIT ASSIGNMENTS																	
				15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		
RMSN	SERIAL NUMBER	(776730)	10	SN 8000	SN 4000	SN 2000	SN 1000	SN 800	SN 400	SN 200	SN 100	SN 80	SN 40	SN 20	SN 10	SN 8	SN 4	SN 2	SN 1	READ	
RMOF	OFFSET	(776732)	11	0	0	0	FMT 16 [ⓐ]	ECI	HCI	SSEI [ⓐ]	0	OFF DIR	0	0	0	0	0	0	0	0	READ/WRITE
				ⓐ 1 = 16-BIT WORD FORMAT; 0 = 18-BIT FORMAT																	
				ⓑ USED ONLY IN 16-BIT FORMAT																	
RMDC	DESIRED CYLINDER	(776734)	12	0	0	0	0	0	0	DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1	READ/WRITE	
RMHR	HOLDING REGISTER	(776736)	13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	READ	
RMHR2	MAINTENANCE REGISTER NO. 2	(776740)	14	ROA	ROB	TAG	TEST BIT	CC	CH	BB 9	BB 8	BB 7	BB 6	BB 5	BB 4	BB 3	BB 2	BB 1	BB 0	READ	
RMER2	ERROR REGISTER NO. 2	(776742)	15	BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	SSE [ⓐ]	0	DPE	0	0	0	READ/WRITE	
				ⓐ ACTIVE ONLY IN 16-BIT FORMAT																	
RMEC1	ECC POSITION	(776744)	16	0	0	0	P 4096	P 2048	P 1024	P 512	P 256	P 128	P 64	P 32	P 16	P 8	P 4	P 2	P 1	READ	
RMEC2	ECC PATTERN	(776746)	17	0	0	0	0	0	PAT 10	PAT 9	PAT 8	PAT 7	PAT 6	PAT 5	PAT 4	PAT 3	PAT 2	PAT 1	PAT 0	READ	

CZ-0819

Figure 4-17 RM80 Adapter Register Summary
(Sheet 2 of 2)

APPENDIX A ADAPTER MODULE COMPATIBILITY

Table A-1 shows the adapter module revisions that are used with the various disk drives.

CS designates circuit schematic.

WL designates wire list.

WT designates wire table. This term is used in manufacturing facilities only.

The letter following CS, WL or WT designates the revision level of the module or backplane.

Table A-1 Adapter Module Assignments

Module	RM02/03	RM80	RM05
M7684	CS = R	yes	yes
M7685	CS = C	no	no
M7685-YA	yes	no	CS = D
M8685	yes	yes	CS = B
M7686	CS = J	yes	no
M7686-YA*	yes	yes	yes
M7687	CS = C	yes	yes
M5922	CS = E	yes	yes
M5923	CS = E	yes	yes
70-13398	WL = C	WL = D	WL = D
Backplane	WT = D	WT = E	WT = E

*If dual port switches are mounted on the front door, M7686-YA must be used.

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What features are most useful? _____

What faults or errors have you found in the manual? _____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

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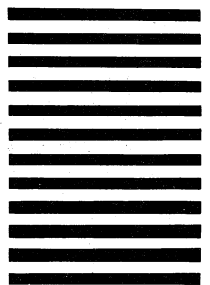
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