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MM11-D/DP core memory manual

digital

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MM11-D/DP core memory manual

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CONTENTS

ILLUSTRATIONS

TABLES

TABLES (Cont)

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

This manual describes the MM11-D/DP Magnetic Core Memory, manufactured by Digital Equipment Corporation and provides the information needed to install and maintain the memory; in addition, it presents the detailed theory of operation of both the logic circuits and the 3-wire, 3-D memory configuration.

The manual is intended to be used by DEC Field Service representatives and customers having PDP-11 training. Readers who are familiar with digital computer theory and who have some knowledge of the PDP-11 Unibus principles can also benefit from this manual (a detailed description of the Unibus can be found in DEC manual DEC-11-HIAB-D).

1.2 GENERAL DESCRIPTION

The MM11-D/DP core memory is a low-cost, low-power, high-reliability memory designed to be used with the PDP-11 family Unibus. It assumes the role of a slave device to the PDP-11 processor or to any peripheral device that is designated bus master. The memory provides storage for 16- or 18-bit data words (two parity bits are included in the 18-bit word), and has a capacity of 16,384 (16K) words. The starting address of the MM11-D/DP can be set on any 8K boundary within the 124K Unibus address space (112K is the highest possible starting address); a special feature of the memory allows the user to assign part of the I/O page (124K–128K) to the MM11-D/DP. Another feature of the MM11-D/DP – interleaving – permits the user to decrease the effective memory cycle time. Two memory modules are used, one being assigned the odd addresses within a 32K block of Unibus addresses, the other being assigned the even addresses within the same block. Thus, for consecutive word addresses, the memories are accessed alternately; hence, memory cycles can partially overlap, reducing the effective cycle time.

1.3 PHYSICAL DESCRIPTION

The MM11-D/DP consists of an 8-1/2 in. × 15 in. hex multilayer motherboard (G652) and a hex stack (H222) that is attached to the motherboard. The G652 motherboard is inserted into a Unibus backplane; it contains the Unibus interface logic, the timing and control logic, the X and Y driver circuits, and the sense/inhibit circuits. The H722 stack contains the core plane, stack diodes, stack charge circuits, and temperature-sensing circuitry that facilitates compensation of core driving currents over the operating temperature range. Figures 1-1 and 1-2 show the separate memory modules; Figure 1-3 shows the two modules joined.

A Parity Control module (M7850) is used with the MM11-DP memory and must be inserted into the same backplane as the memory (the MM11-DP can be used as a non-parity memory). Refer to the M7850 Parity Controller maintenance manual for a description of the controller.

Table 1-1
MM11-D/DP Specifications

Memory Type	Magnetic core, read/write, random-access
Core Configuration and Size	Planar, 3W-3D, 18 mil O.D.
Capacity	MM11-D: 16,384 16-bit words MM11-DP: 16,384 18-bit words (2 byte parity bits)
Maximum Access Time	MM11-D: 425 ns MM11-DP: 560 ns (when used with a Parity Control module)
Maximum Cycle Time	MM11-D: 1 μs MM11-DP: 1 μs
Voltage Requirements	+20 Vdc, ±3% +5 Vdc, ±5% -5 Vdc, ±5%
Current Requirements	**dc Supply — Active* — Standby** MM11-D/DP +20 Vdc — 4.0 A — 0.8 A +5 Vdc — 4.0 A — 4.0 A -5 Vdc — 0.5 A — 0.5 A
Maximum Power Dissipation	**dc Supply — Active — Standby** MM11-D/DP +20 Vdc — 80 W — 16 W +5 Vdc — 20 W — 20 W -5 Vdc — 2.5 W — 2.5 W
X–Y Current Margins	±5%
Ambient Temperature Operating Range	In accordance with DEC STD 102, Class C
Relative Humidity Operating Range	In accordance with DEC STD 102, Class C

*Active is defined as running all 0s at 1.0 μs repetition rate (worst case).

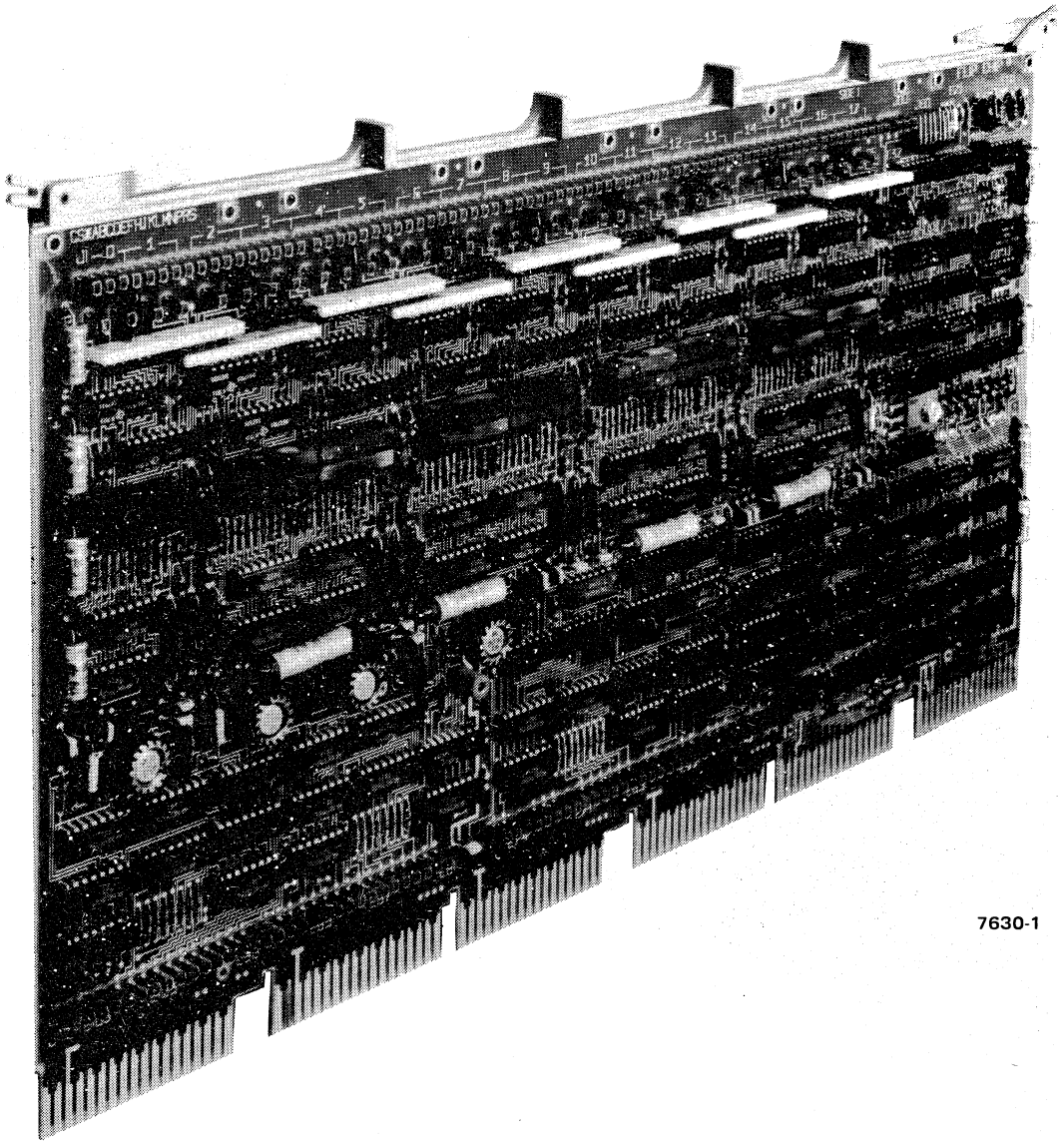


Figure 1-1 G652 Module

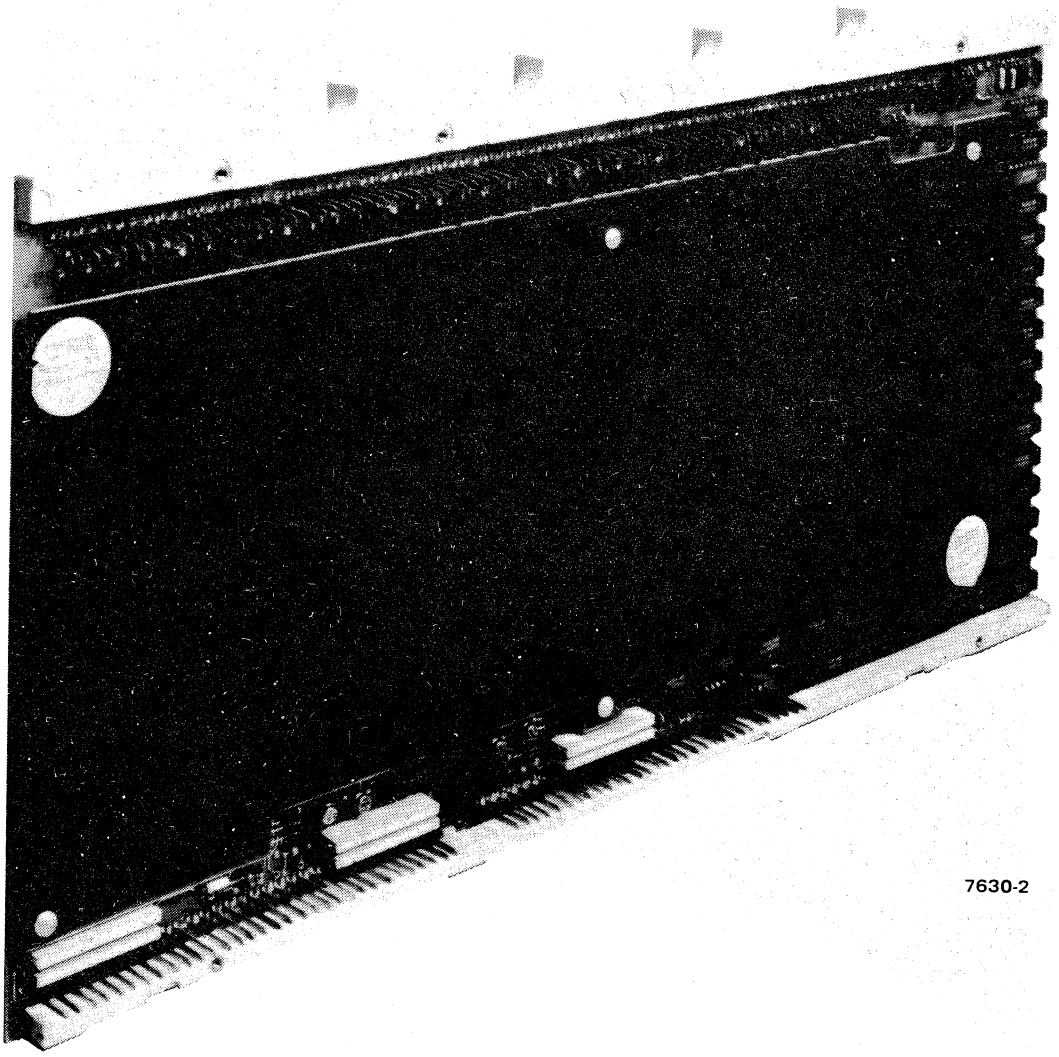


Figure 1-2 H222 Module

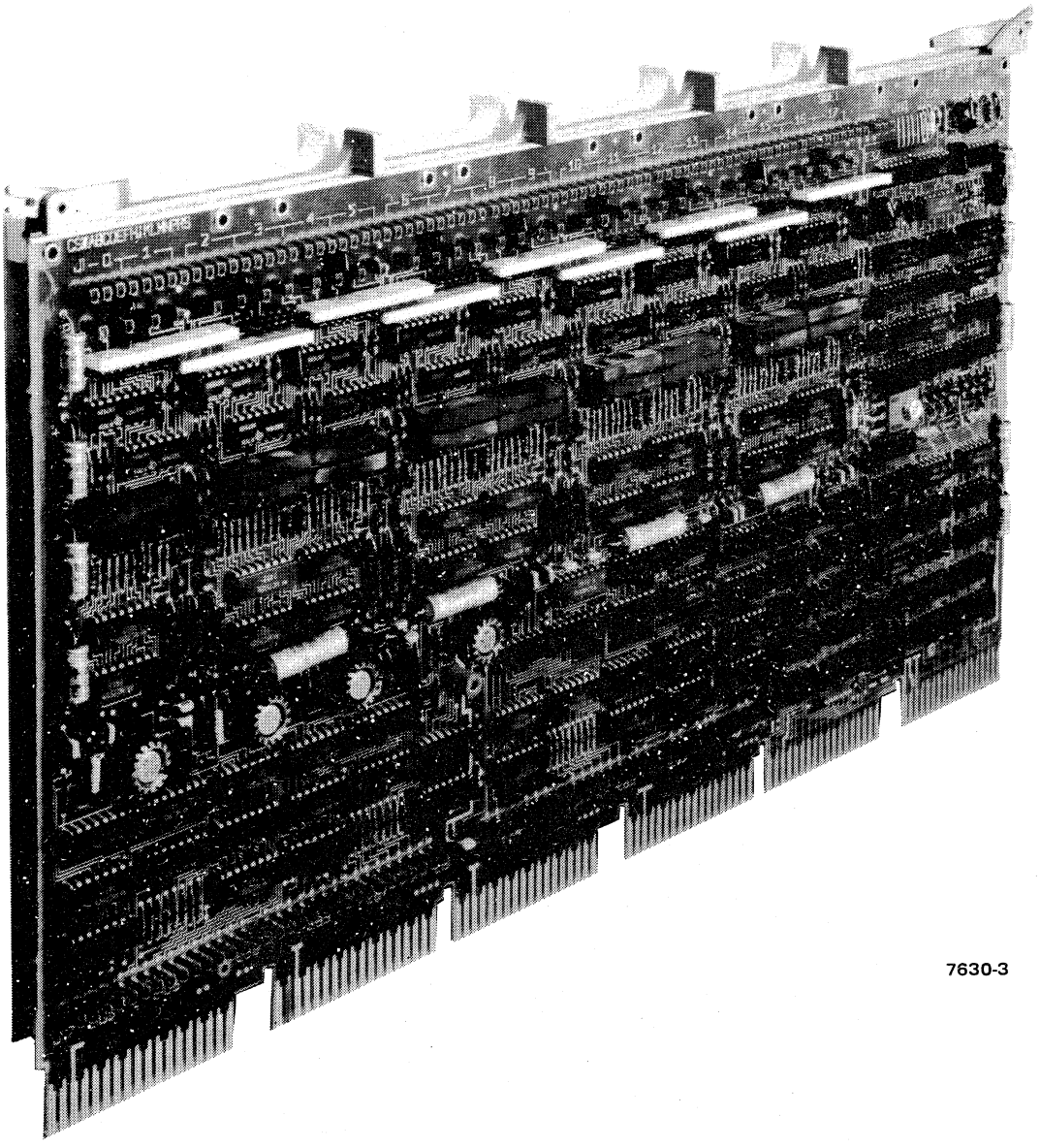


Figure 1-3 MM11-D/DP

CHAPTER 2
INSTALLATION

The MM11-D/DP can be installed easily. After removing the memory modules from the shipping cartons, use the procedure that follows to prepare the memory for system operation.

1. Select the starting address. Jumpers W1 – W8 on the G652 module are involved in this process. Paragraph 3.4.2 discusses the starting address determination; *read this paragraph before installing or removing any of the jumper wires.*

2. Check the backplane assembly to ensure that the correct dc voltages are present (Table 2-1 lists the DD11-F "modified Unibus" backplane pins and the signal available on each pin). The voltages and their limits are listed below; if they must be adjusted, use the procedure given in Paragraph 4.2.1.

Voltage (dc)	Backplane Pin
+20 Vdc ±3%	A1U, A1V, A2V
+5 Vdc ±5%	A2A, B2A, C2A, D2A, F2A
-5 Vdc ±5%	B2V

3. Ensure that the H222 module is firmly attached to the G652 module. Insert the G652 into the DD11-F backplane; any one of slots 2 – 7 can be used. If a parity controller is used, it can be inserted in connectors A and B in any of slots 2 – 8 (parity and non-parity memory cannot be mixed on the same backplane).

4. Connect the BC11-A Unibus cable to the memory. If this is the last device on the bus, terminate the Unibus by placing a 9302 terminator in the BUS OUT slot. If the memory is not the last device, continue the bus by placing an M920 jumper module or the BC11-A cable connector in the BUS OUT slot.

5. If the system uses an M7850 Parity Controller, refer to the controller manual for information concerning the installation and adjustment of the M7850 module.

6. Load and run the MM11-D/DP diagnostic programs. Verify that the program printout agrees with the total memory in the system.

7. Connect the Unibus Voltage Margin Tester to the memory at connector J180 on the G652 module. Run two passes of the 0–124K Memory Exerciser Diagnostic (MAINDEC-11-DZQMB) with the margin tester switches set at each of the four possible "on" positions:

   XY CURRENT HIGH – allows high (+5%) memory drive current;
   XY CURRENT LOW – allows low (–5%) memory drive current;
   STROBE EARLY – allows an early sense strobe (–15 ns);
   STROBE LATE – allows a late sense strobe (+15 ns).

NOTE

Only margin the memory with one parameter at a time. Even good memories may fail under some combinations of drive and strobe margins.

8. Disconnect the margin tester. Run the DZQMB diagnostic to verify normal operation.

Table 2-1
DD11-F Backplane Pin Assignments

	A		B		C		D		E		F	
	1	2	1	2	1	2	1	2	1	2	1	2
A	INIT L	+5 V	DATIP CLR PAUSE L	+5 V	--	+5 V	--	+5 V	--	--	--	--
B	INTR L	T.P.	--	T.P.	--	--	--	--	--	--	--	--
C	D00 L	GND	BR5 L	GND	--	GND	--	GND	--	GND	--	GND
D	D02 L	D01 L	BATTERY +5	BR4 L	--	--	--	--	--	--	--	--
E	D04 L	D03 L	INT SSYN L	PARITY DETECT L	STACK VREF	--	--	--	--	--	--	--
F	D06 L	D05 L	ACLO L	DCLO L	--	--	--	--	--	--	--	--
H	D08 L	D07 L	A01 L	A00 L	--	--	--	--	--	--	--	--
J	D10 L	D09 L	A03 L	A02 L	--	--	--	--	--	--	--	--
K	D12 L	D11 L	A05 L	A04 L	--	--	--	BUS G7 SO H	--	--	--	--
L	D14 L	D13 L	A07 L	A06 L	--	--	--	BUS G7 OUT H	--	--	--	--
M	PA L	D15 L	A09 L	A08 L	--	--	--	BUS G6 SO H	--	--	--	--
N	PARITY P1 L	PBL	A11 L	A10 L	--	--	--	BUS G6 OUT H	--	--	--	--
P	PARITY P0 L	BBSY L	A13 L	A12 L	--	--	--	BUS G5 SO H	--	--	--	--
R	--	SACK L	A15 L	A14 L	--	--	--	BUS G5 OUT H	--	--	--	--
S	--	NPR L	A17 L	A16 L	--	--	--	BUS G4 SO H	--	--	--	--
T	GND	BR7 L	GND	C1 L	GND	--	GND	BUS G4 OUT H	GND	--	GND	--
U	+20 V	BR6 L	SSYN L	C0 L	--	--	--	--	--	--	--	--
V	+20 V	+20 V	MSYN L	-5 V	--	--	--	--	--	--	--	--

CHAPTER 3
LOGIC DESCRIPTION

3.1 CORE ARRAY DESCRIPTION

3.1.1 General Core Description

The ferrite core memory consists of 16 memory mats (18 for the MM11-DP) arranged in a planar configuration. Each mat, representing a single bit position of a word, contains 16,384 ferrite cores arranged in a 128 × 128 array. This planar configuration provides a total of 16,384 16-bit word locations (18 for the MM11-DP). Each core can assume a stable magnetic state corresponding to either logic 1 or logic 0. Even if power is removed from the memory, the core retains its state until changed by appropriate control signals.

Each core is threaded by 3 wires, which provide the means for selecting and switching the core. X-axis read/write windings pass through the cores in each horizontal row; Y-axis read/write windings pass through the cores in each vertical row; sense/inhibit windings pass through all the cores in a given mat.

Figure 3-1 represents a single core with an X winding, a Y winding, and a sense/inhibit winding passing through it. If a current of magnitude Im/2 flows in both the X and Y windings in the direction indicated, a magnetic field is produced in the core. The flux lines of the magnetic field encircle the core in the direction shown by the arrows. If the direction of current flow is reversed, the magnetic field also reverses direction. This change in flux induces a voltage pulse in the sense winding that can be detected by a sense amplifier.

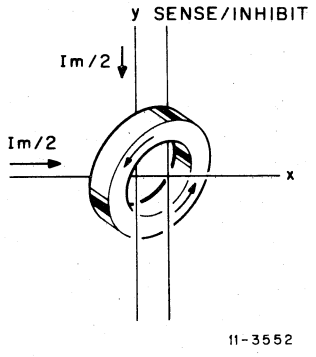


Figure 3-1 Core Windings

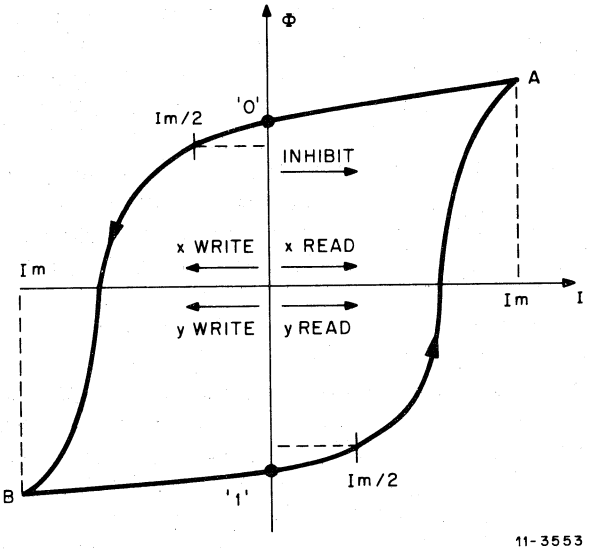


Figure 3-2 Core Hysterisis Loop

Figure 3-2 shows a hysterisis loop that relates the magnetic flux in the core to the magnetizing current in the X and Y windings. The point designated "0" on the Φ axis represents the magnitude and direction of the flux for logic 0. If current is passed through the X and Y windings in the "write" direction (the direction indicated by the arrows in Figure 3-1), the magnetic field reverses direction, and the flux assumes the magnitude represented by point B. When the currents cease, the flux decreases to point "1" and a logic 1 is now stored in the core. To "read" this logic 1, the magnetizing currents are reversed and the flux assumes the magnitude represented by point A. When the currents cease, the flux decreases to point 0 and the core now holds logic 0. The hysterisis loop must be traversed in the direction indicated by the arrows. Thus, if a core has logic 0 stored in it, no significant change occurs in the magnetic field when the core is read. Figure 3-3 shows waveforms that represent the core voltage output and the current through the core. If the core is in the logic-1 state, full-select read current (Im) will produce a core voltage output of approximately 40 mV. A half-select read current (Im/2) also produces an output voltage, approximately 2 mV (the 0-output waveforms in Figure 3-3 represent the sum of the outputs from the half-selected core and all the unselected cores); however, the core does not change state and the voltage output is not detected by the sense amplifiers.

3.1.2 MM11-D Core Array Description

Figure 3-4 illustrates a typical portion of a 16K core memory; X and Y wires pass through each core in the mat. The current passing through any one winding is such that no single winding produces a magnetic field strong enough to cause a core to change its magnetic state. Only the reinforcing magnetic field, caused by the coincident current of both an X and a Y winding, can cause the core located at the point of intersection to change states. It is this principle that allows the relatively simple wiring arrangement to select *one* (and only one) memory core out of the possible 16,384 contained on each mat. The current passing through either an X or Y winding is referred to as a half-select current.

A half-select current passing through the X3 winding from left to right produces a magnetic field that tends to change all cores in that horizontal row from the 1 to 0 state. The field produced by the current is, however, insufficient to complete the state transition in any core. Simultaneously passing a half-select current through the Y2 winding from top to bottom produces the same effect on all cores in that particular vertical row.

Note, however, that both currents pass through only one core which is located at the intersection of the X3 and Y2 windings. This is the selected core, and the combined current values are sufficient to change the state of the core. The arrows in Figure 3-4 show current direction for the read cycle.

In the MM11-D/DP, the X3 windings in all 16 (or 18) mats are connected in series, as are the Y2 windings. Therefore, whenever a full-select current flows through a selected core on one mat, it also flows through an identical core on the other 15 (or 17) mats. The X3-Y2 cores on all mats switch to a logic 0, causing each of the 16 cores to become one bit of a 16-bit storage cell, or word.

Because of the serial nature of the X-Y windings, a method must be employed to set certain cores to the 0 state; otherwise, every 16-bit word selected would be all 1s. The method used in the MM11-D/DP is to first clear all cores to the 0 state by reading. During the write operation, cores on particular mats are inhibited by an inhibit winding. The inhibited cores remain 0s even when identical cores on other mats are set to 1s.

The half-select current for the inhibit lines is supplied by one of two transformers, driven by an inhibit current driver, which consists of a pair of switches and a current source. The current in the inhibit line flows in the opposite direction from the write current in all Y lines and cancels out the write current in any Y line. Each mat, representing one bit position of a word, has an inhibit current driver; thus, selected bits can be inhibited to produce any combination of binary 1s and 0s desired in the 16-bit word. Remember that the inhibit function is active only during write time. (The inhibit winding interchanges in the Y direction for noise cancellation; this interchange is shown for illustrative purposes only as occurring between rows X4 and X5 in Figure 3-4. In the MM11-D, the actual interchange occurs between rows X63 and X64 – see Figure 3-6).

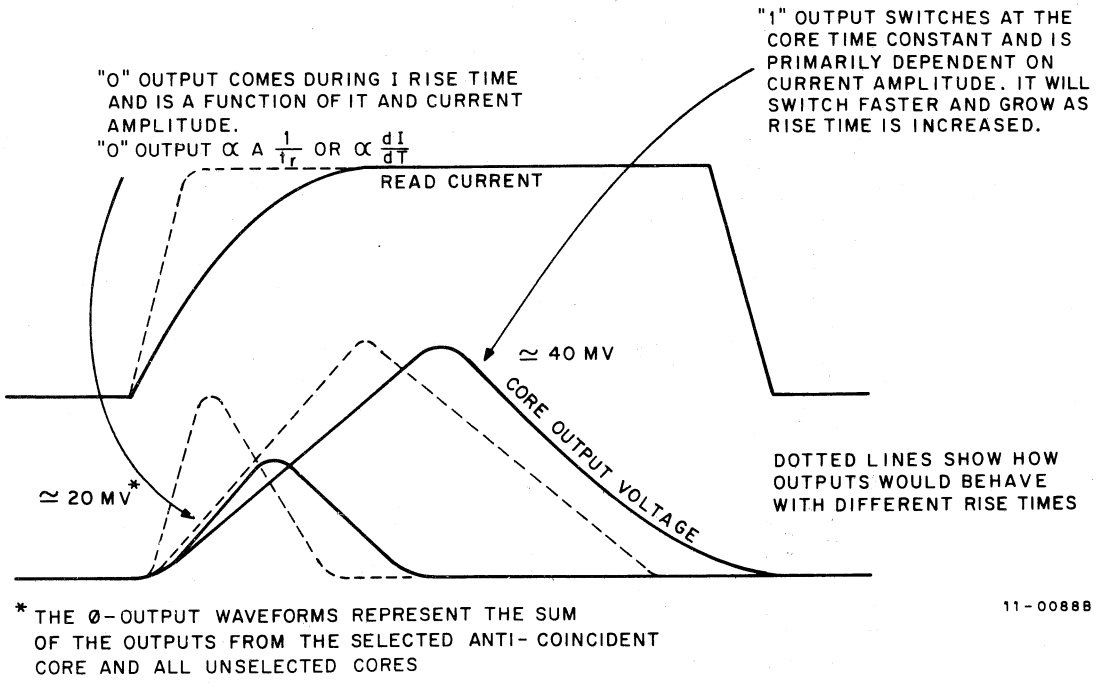


Figure 3-3 Core Current/Voltage Output Relationship

The sense/inhibit lines are also used to read out information in a selected 16-bit memory cell. The specific core is selected at read time in the same manner as during the write cycle, with one notable exception: the X and Y currents are in the opposite direction than they are for the write operation. These opposite half-select currents cause all cores previously set to 1 to change to 0; cores previously set to 0 are not affected. Whenever the core changes from 1 to 0, the flux change induces a voltage in the sense winding of that mat. This voltage is detected and amplified by a sense amplifier. The amplifier output is strobed into the data register for eventual transfer to the Unibus.

With a core array of 128 × 128, the 128 X windings and 128 Y windings can be used to select any one of 16,384 cores on a mat. However, for space economy, the MM11-D/DP makes use of the principle of coincident and anti-coincident cores; hence, although 128 X windings are used, only 64 Y windings link the cores in the vertical direction.

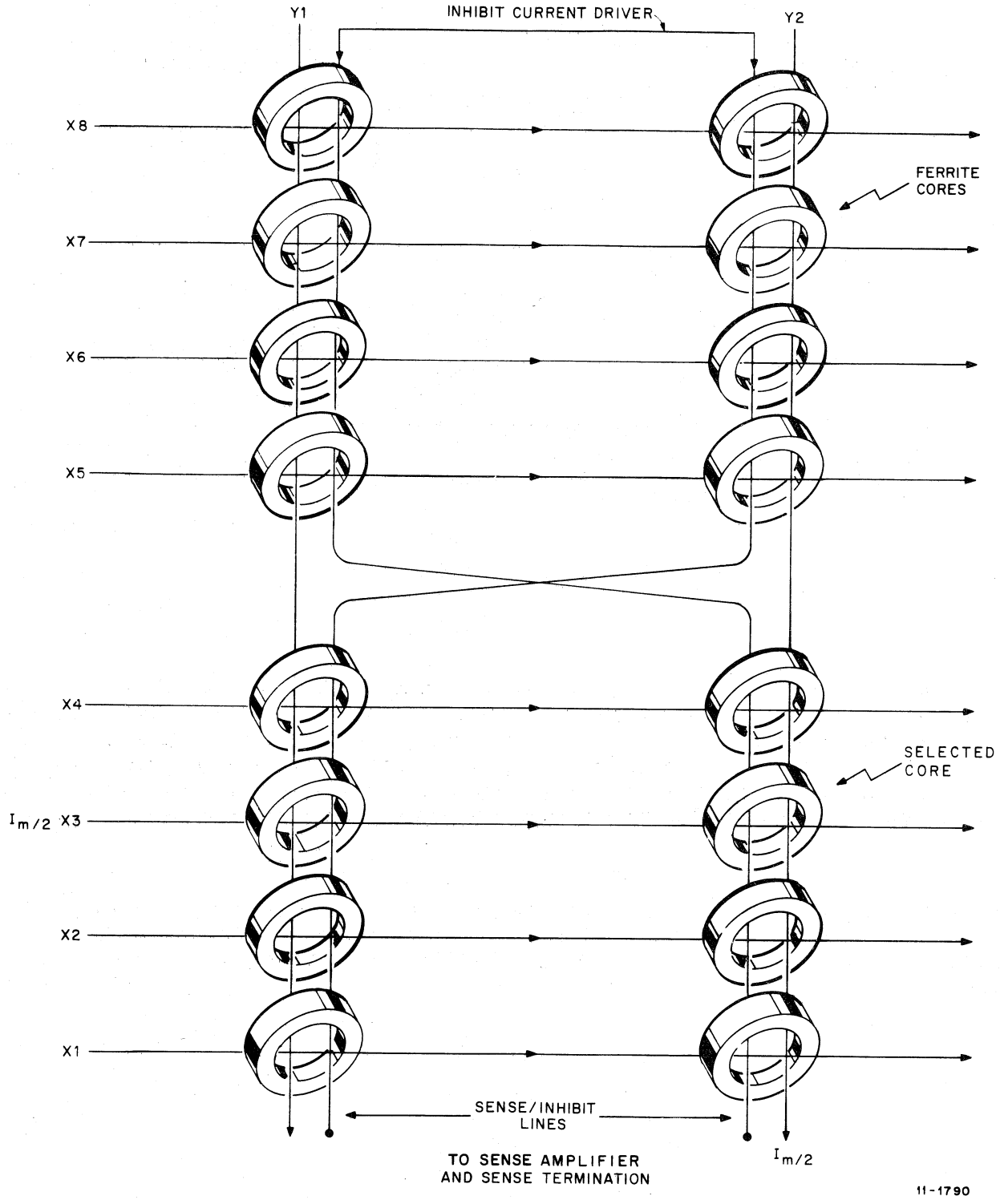


Figure 3-4 3-Wire Configuration

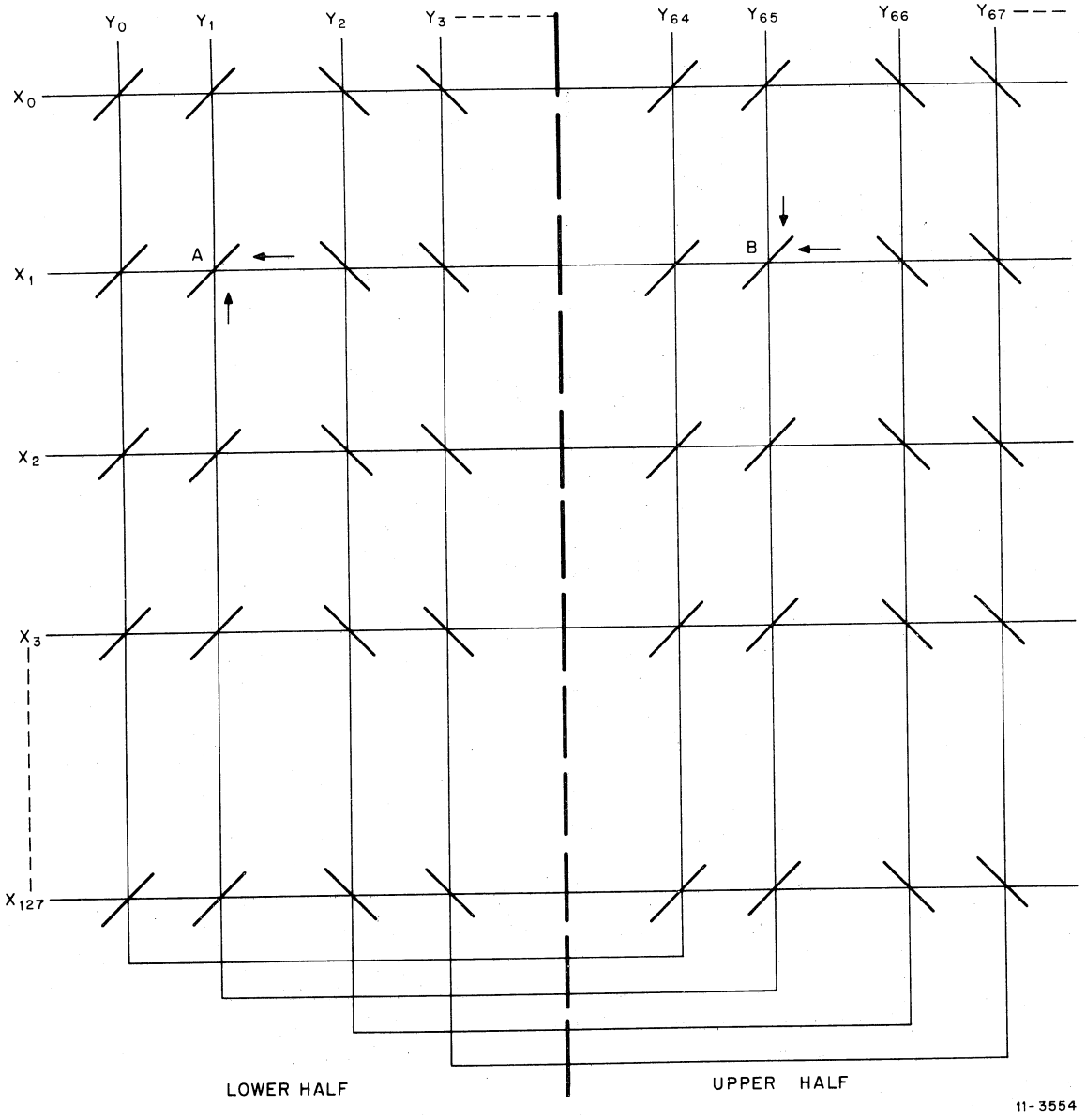


Figure 3-5 MM11-D Mat

Figure 3-5 illustrates a portion of a mat in the MM11-D/DP. The mat is divided, for descriptive purposes only, into an upper and a lower half. The cores in column Y0 and those in column Y64 are linked by the same winding; the same is true for columns Y1 and Y65, Y2 and Y66, etc. If magnetizing currents flow in the X1 winding and in the Y1–Y65 winding in the directions indicated, both currents pass through core A and core B. However, the currents reinforce each other – they are coincident – only in core A; hence, this core is selected. The currents in core B are anti-coincident; thus, core B is not selected. If the current in the Y1–Y65 winding is reversed, core B becomes the coincident core and is selected, while A is not.

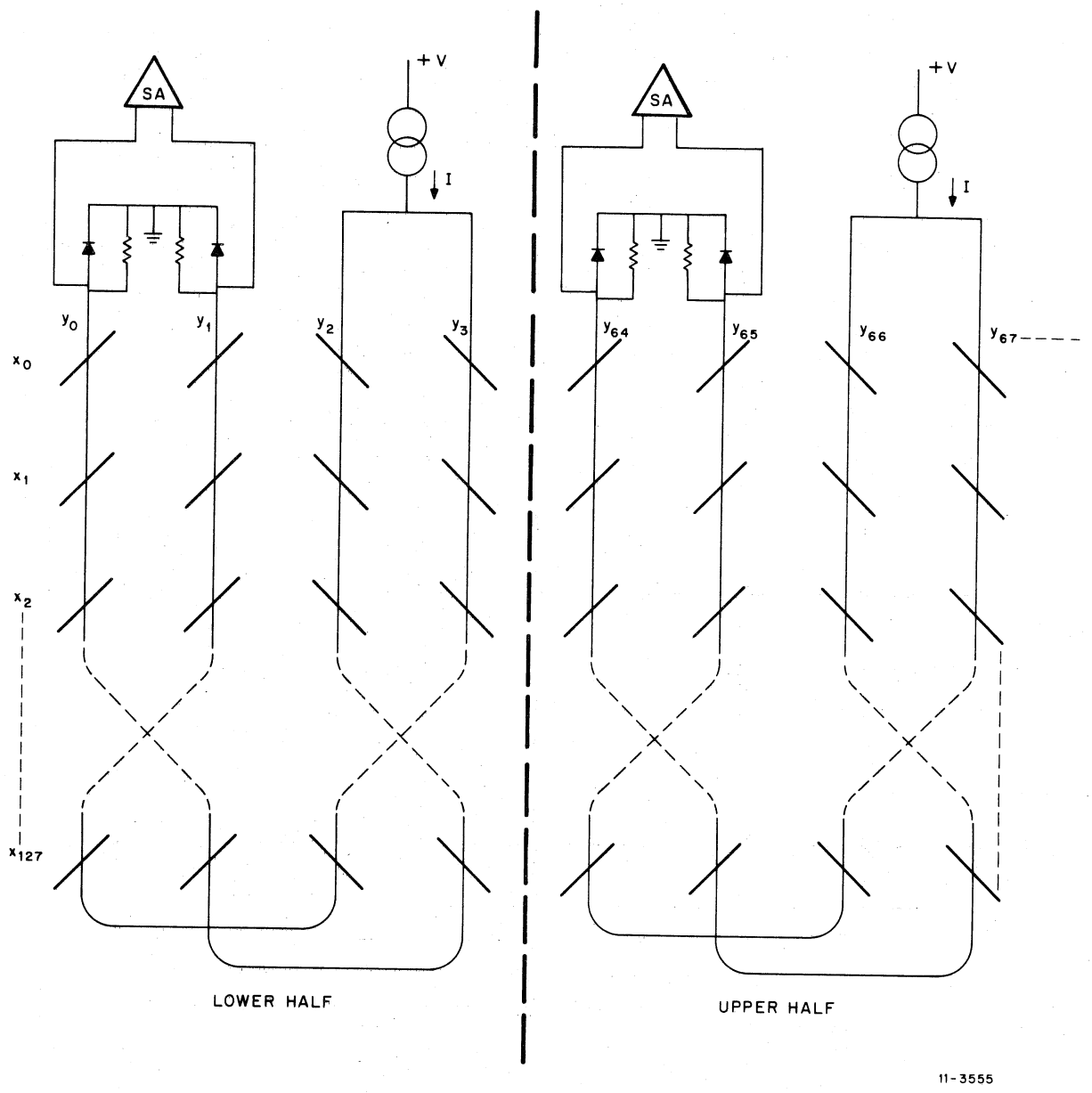


Figure 3-6 Mat Sense/Inhibit Windings

Consider the X winding current to be a write current. Thus, current in the Y winding can flow in either direction during a write operation. If the X winding current is reversed, to flow in the read direction, Y winding current can again flow in either direction. Consequently, Y axis current is not termed read or write current in the MM11-D logic description. Rather, it is defined in terms of its source in the Y Driver/Switch circuit; these definitions are discussed subsequently.

Because it is possible to select either of two cores in a mat during both a read and a write operation, two sense/inhibit windings are required for each mat, one for the upper half, another for the lower half. Each winding passes through all the cores in its half of the mat, as illustrated in Figure 3-6 (for clarity, X and Y windings are not shown; the sense/inhibit winding interchanges between rows X63 and X64 for noise cancellation).

3.2 MM11-D BLOCK DIAGRAM

A functional block diagram of the MM11-D is shown in Figure 3-7. The blocks are described briefly to relate each to the others; each block is described in detail in a subsequent section.

Voltage Monitor Circuit

The Voltage Monitor circuit checks the status of the BUS DCLO L signal and the +5 Vdc supply voltage. If BUS DCLO L is negated, the circuit generates MSYN H when BUS MSYN L is asserted on the Unibus, and provides a voltage (+20SW) that is used in the core selection process. If the +5 Vdc voltage drops below a minimum value, the +20SW voltage is removed to prevent unwanted switching of core states.

Address Decoding Logic

Each Unibus address that is placed on the bus by the master is examined by the Address Decoding logic; if the address is one that has been assigned to the MM11-D, the logic decodes bits A<17:11> L and generates the BANK SEL H signal. This signal allows MSYN to start the timing chain in the Read Control logic and a read or write operation is carried out.

Control Bit Logic

The bus master places Control Bit information on the Unibus along with the address data. The Control Bit signals – A0 L, C0 L, and C1 L – specify the type of data transfer that is to be carried out. The Control Bit logic decodes these three signals and asserts WRITE BYTE 0 L and WRITE BYTE 1 L in various combinations. These two signals direct the Read Control logic to assert the signals needed for the specified type of transfer. Table 3-1 lists the type of Unibus data transfers that can be made and relates the control bit logic levels to the data transfers.

Memory Address Register (MAR) Logic

While address bits A<17:11> L are being decoded by the Address Decoding logic, bits A<14:01> L are applied to the MAR logic. If the BANK SEL H signal is asserted, the Read Control logic will generate the LOCK MAR 1 L and LOCK MAR 2 L signals; these signals will latch the 15 address bits into the MAR. The MAR outputs are applied to the X and Y Driver/Switch logic to select the appropriate cores for the data transfer.

Read Control Logic

During the read half of a timing cycle, the Read Control logic generates signal(s) that:

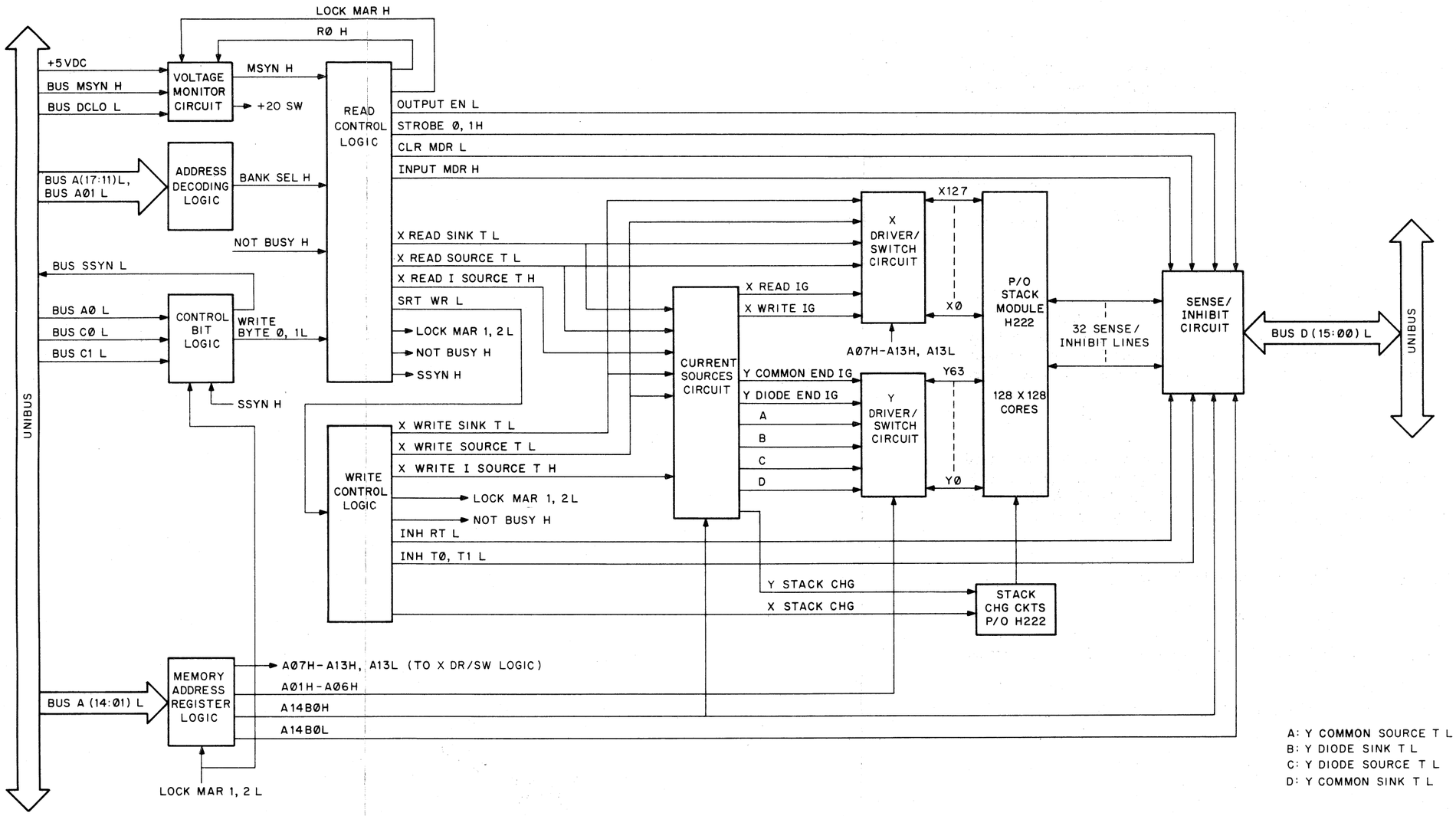
Turn on the read current generators in the Current Sources circuit;

Control the X and Y driver/switches so that read current flows through the selected windings in the proper direction;

Conditions the Sense/Inhibit circuit for an input or output data transfer;

Latches the memory address into the MAR;

Starts the Write Control logic.



A: Y COMMON SOURCE T L
B: Y DIODE SINK T L
C: Y DIODE SOURCE T L
D: Y COMMON SINK T L

11-3571

NOTE:
Logic is part of G652 Module unless noted.

Figure 3-7 MM11-D Block Diagram

Table 3-1
Unibus Data Transfers

Type of Transfer	Control Bit Logic Level C0 L	C1 L	A0 L	Operation Effected
Data in (DATI)	HI	HI	X	Data transfer from memory to master; memory performs read/restore operation.
Data In Pause (DATIP)	LO	HI	X	Normally different from DATI, but in DATIP mode the MM11-D performs a DATI operation.
Data Out (DATO)	HI	LO	X	Data transfer from master to memory.
Data Out, Byte (DATOB)	LO	LO	LO	Data transfer from master to memory; the 8 most significant data bits are transferred via the D<15:08> lines.
	LO	LO	HI	Data transfer from master to memory; the 8 least significant data bits are transferred via the D<07:00> lines.

Note: X represents "don't care" state.

Write Control Logic
During the write half of a timing cycle, the Write Control logic generates signal(s) that:

Turn on the write current generators in the Current Sources circuit;

Control the X and Y Driver/Switches so that write current flows through the selected windings in the proper direction;

Latches the memory address into the MAR;

Enables the Sense/Inhibit circuit to generate an inhibit current, if necessary.

Current Sources Circuit
The Current Sources circuit contains the X and Y current generators, which are turned on by control signals from the Read and Write Control logic. The Current Sources circuit generates control signals that direct current through the Y windings in the direction that reflects the selected core's location in the mat. (Because the Y winding passes through 2 cores, one in the upper-half of the mat, the other in the lower-half, coincident current in one core is anti-coincident current in the other core; thus, current can flow through the winding in either direction during each half of the timing cycle.)

X Driver/Switch Circuit
The X Driver/Switch circuit decodes address bits a<13:07 to select one of the 128 X windings. Read and write currents supplied by the Current Sources circuit are applied to the selected winding and flow (in the direction specified by the Read and Write Control logic signals) from the X Driver/Switch circuit, through the 128 × 16(18) cores on the selected winding, and back to the Driver/Switch circuit.

Y Driver/Switch Circuit

The Y Driver/Switch circuit decodes address bits A <06:01> to select one of 64 Y windings. Read and write currents are applied to the winding and flow through the 256 × 16(18) cores and back to the circuit.

Sense/Inhibit Circuit

The Sense/Inhibit circuit is an interface between the Unibus D<15:00> lines and the stack cores. During the read half of a memory-read timing cycle (DATI), differential amplifiers sense the output of the selected cores (1 core on each of the 16 mats). Logic levels representing the core outputs are strobed into a Memory Data Register (MDR) and gated on the D<15:00> lines. During the write half of the timing cycle the cores are restored to their original states; selected inhibit drivers might have to be turned on to accomplish the restoration correctly. In a memory-write cycle (DATO), the cores are also sensed, but the differential amplifiers are not strobed during the read half of the cycle. Instead, data on the D<15:00> lines is gated into the MDR. During the write half of the cycle, the data in the MDR is written into the selected cores; once again, selected inhibit drivers might have to be turned on to accomplish the write operation (a DATOB operation is performed in the same way as the DATO for the selected byte; however, the unselected byte is handled as a simple read-restore operation).

Stack Charge Circuits

The Stack Charge circuits – one for the X diode matrix, one for the Y diode matrix – are located on the stack module. The circuits help the stack capacitance to recover, shorten the rise time of the stack current, and reduce unwanted currents in the unselected lines associated with the selected driver.

3.3 VOLTAGE MONITOR CIRCUIT

The Voltage Monitor circuit, shown in Figure 3-8, monitors the BUS DCLO L signal and the +5 V supply line. If the +5 V supply drops below a specified value, transistor Q1 is turned on, bringing the +20SW voltage near ground. If BUS DCLO L goes low, indicating a problem in the dc power supply, Q1 is again turned on. In addition, after the on-going timing cycle is completed, the circuit prevents BUS MSYN L from asserting MSYN H; thus, no new timing cycle can begin until the system is powered again.

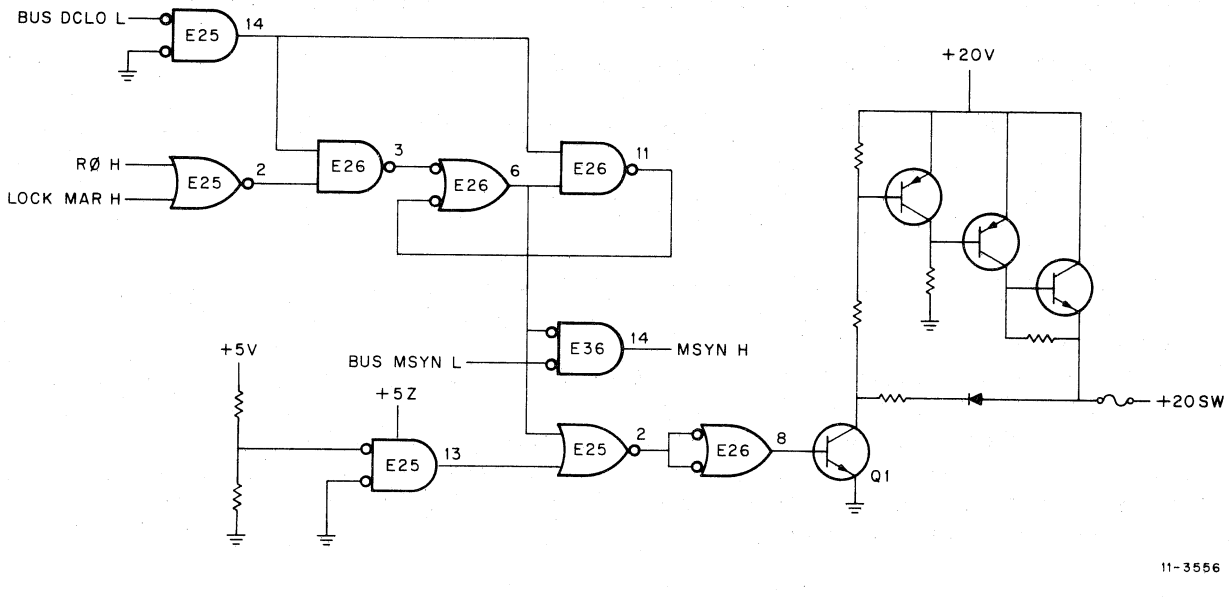


Figure 3-8 Voltage Monitor Circuit

Figure 3-9 is a timing diagram that illustrates how BUS MSYN L is locked out and +20SW is turned off when BUS DCLO L is asserted on the Unibus. The BUS DCLO L signal is assumed to be asserted after the memory cycle has begun. Because both R0 H and LOCK MAR H have been asserted by the Read Control logic, the timing cycle will proceed to completion. When LOCK MAR H goes low, however, NOR gate E26 (output pin 6) is latched high. This level disables NAND gate E36, preventing BUS MSYN L from generating MSYN H. Note that if BUS DCLO L returns high before LOCK MAR H is negated, BUS MSYN L is not locked out and the +20SW voltage is not cut off.

The circuit shuts off the +20SW voltage to prevent any of the cores from accidently changing state when BUS DCLO L is asserted because power is removed. Such an accidental change of state might occur when the +5 V power supply is turning off and spurious timing signals are generated. The +5 V line is monitored so that, even if the BUS DCLO L signal fails, protection is afforded to circuit components, which otherwise might be subjected to excessive power dissipation due to spurious control signals.

3.4 ADDRESS DECODING LOGIC

3.4.1 Memory Organization and Addressing Conventions

Prior to a detailed discussion of the address decoding logic, PDP-11 memory organization and addressing conventions should be considered.

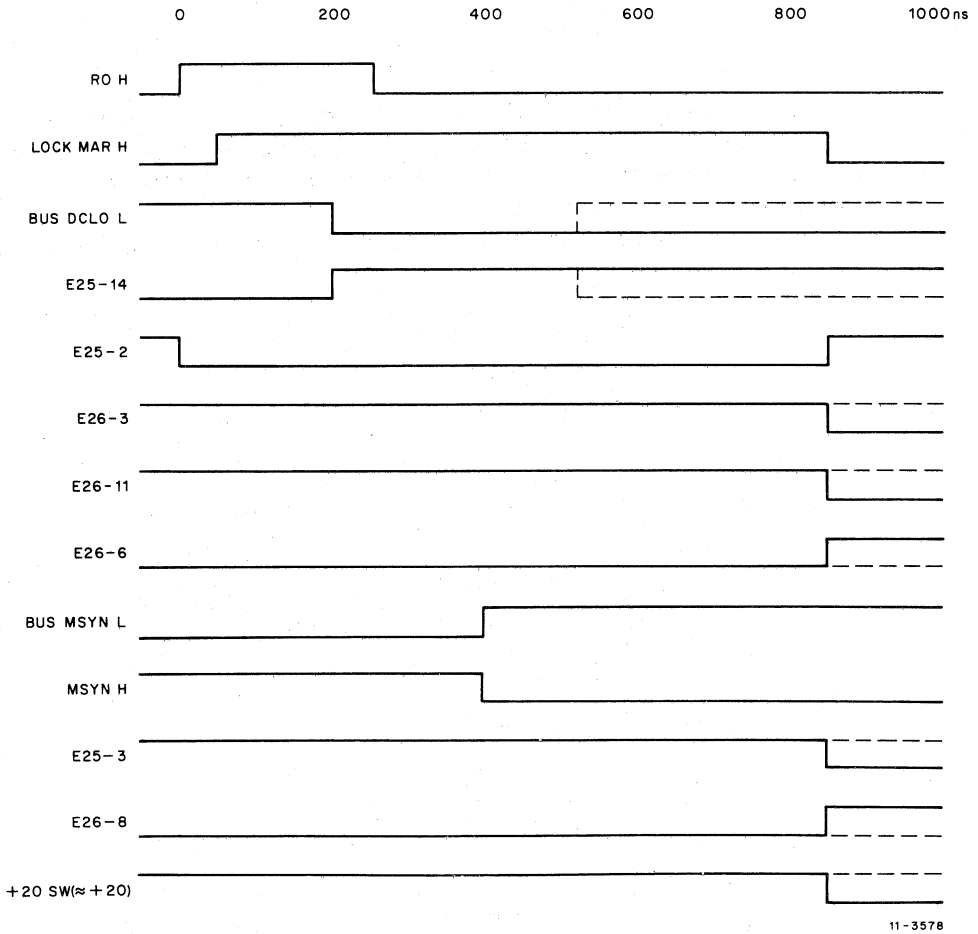
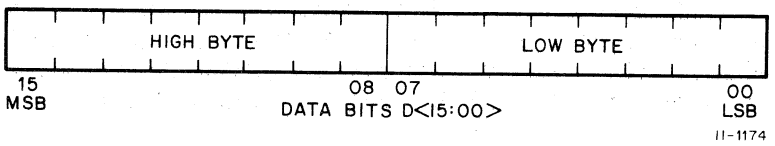


Figure 3-9 Voltage Monitor Timing (DATI Operation)

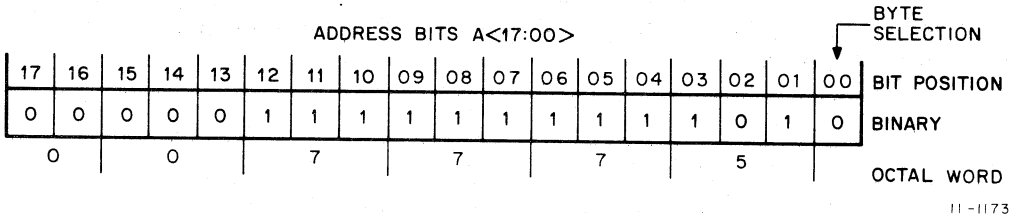
Memory is organized into 16-bit words, each consisting of two 8-bit bytes. The bytes are identified as low and high, as shown below.



Each byte is addressable and has its own address location; low bytes are even numbered – high bytes are odd numbered. Words are addressed at even-numbered locations only; the high (odd) byte is automatically included.

For example, a 16K word memory has 16,384 words or 32,768 bytes; therefore, 32,768 locations are assigned. The address locations are specified as 6-digit octal numbers. The 32,768 locations are designated 000000 – 077777, as shown in Figure 3-10.

The address decoding logic responds to the binary equivalent of the octal address. The binary equivalent of 017772 is shown below as an example.



Each memory bank requires its own unique device address. For example, assume that a system contains three 16K memory banks, as shown in Figure 3-11. The device selector for the 16K non-interleaved memory decodes five address lines, A(17:13). Examination of the binary states of these lines for the three memory banks shows that the changes in the states of bits A15 and A16 allow the selection of a unique combination for each bank. The combination, which is the device address, is hardware-selected by jumpers in the device selector.

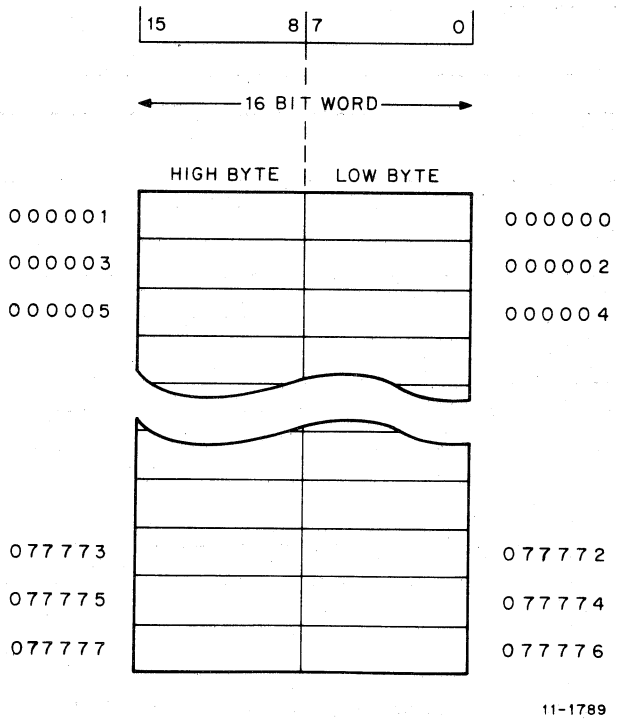


Figure 3-10 Memory Organization

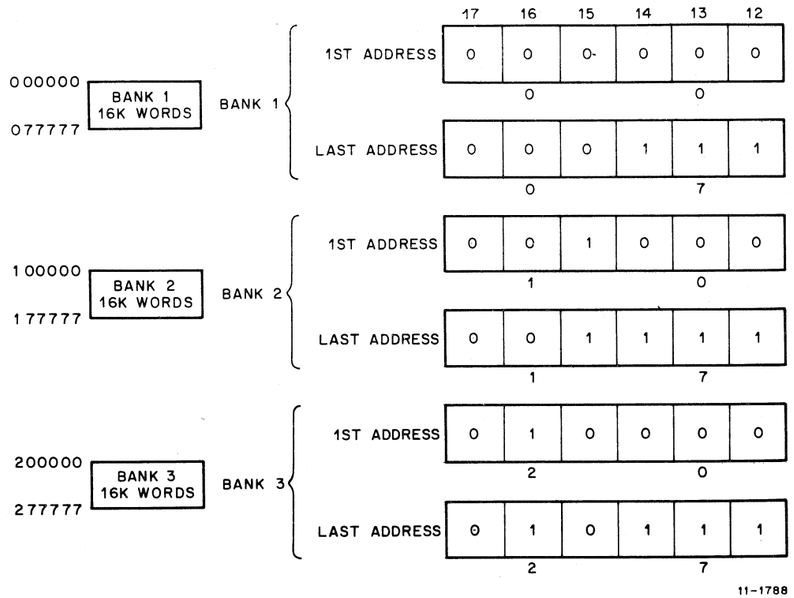


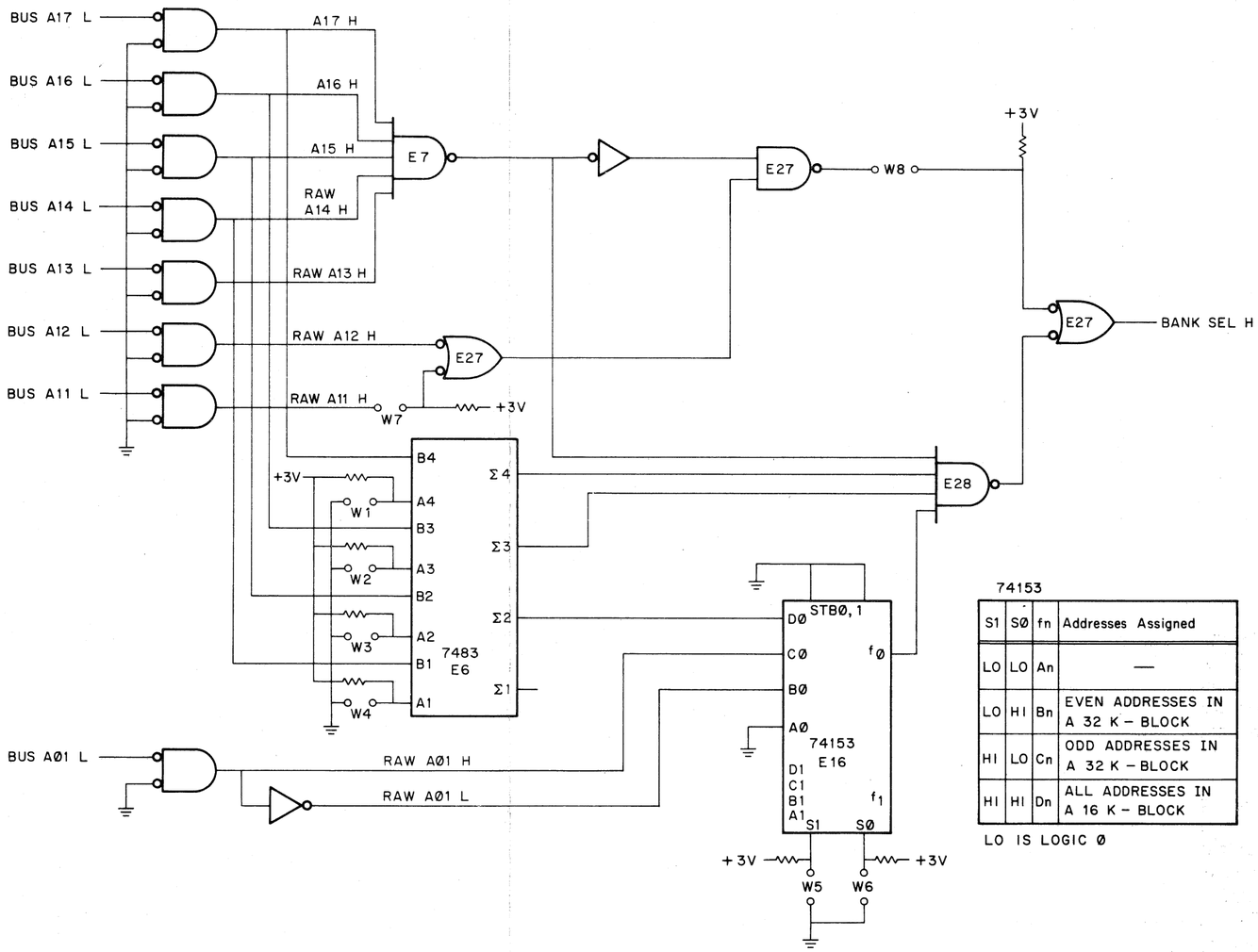
Figure 3-11 Address Assignments for Three Banks of 16K Words Each

3.4.2 Address Selection

The Unibus address space assigned to the MM11-D depends on what address is selected as the MM11 starting address. This starting address can be any one that begins an 8K block of addresses; for example, 000000_8 (0K), 040000_8 (8K), 140000_8 (24K). The starting address is assigned by inserting jumper wires at specified locations in the Address Decoding logic (Figure 3-12). When the starting address appears on the Unibus address bus, the Address Decoding logic asserts the BANK SEL H signal. If both the Unibus and the MM11 timing logic are not busy, the BANK SEL H signal enables BUS MSYN L to start the timing chain.

The BANK SEL H signal can be asserted when either NAND gate E27 or E28 is enabled. However, during normal operation, wherein the uppermost 4K of Unibus address space is reserved for peripheral devices, there is no jumper wire installed at location W8; consequently, only NAND gate E28 need be considered. This gate is enabled whenever an address from the assigned 16K block appears on the Unibus address lines. The starting address of this block is determined by the arrangement of jumpers at locations W1 – W4. Jumpers are inserted at these four locations in such a way that any assigned address causes the outputs from adder E6 to be high. Two of these outputs, $\sum 3$ and $\sum 4$, go directly to NAND gate E28. A third, $\sum 2$, goes to multiplexer E16; during non-interleaved operation, the $\sum 2$ output is gated through the multiplexer to NAND gate E28. The fourth input to the gate is from NAND gate E7, which is enabled only for addresses within the 4K reserved area.

Table 3-2 lists the possible starting address for the MM11-D memory, the ending address (plus 1) corresponding to each starting address, and the disposition of jumper wires at locations W1 – W4. For example, an MM11-D memory can be assigned address space beginning at address 040000_8 (8K) if a jumper is inserted at location W3. The ending address will be 137777_8 (24K – 1). Each address in this 16K block will cause NAND gate E28 to be enabled, resulting in the assertion of BANK SEL H.



74153

S1	SØ	fn	Addresses Assigned
LO	LO	An	—
LO	HI	Bn	EVEN ADDRESSES IN A 32 K – BLOCK
HI	LO	Cn	ODD ADDRESSES IN A 32 K – BLOCK
HI	HI	Dn	ALL ADDRESSES IN A 16 K – BLOCK

LO IS LOGIC Ø

11-3557

Figure 3-12 Address Decoding Logic

Table 3-2
Jumper Assignments for MM11-D Starting Addresses

Starting Address	Ending Address +1	W1	W2	W3	W4
0	16K	OUT	OUT	OUT	IN
8K	24K	OUT	OUT	IN	OUT
16K	32K	OUT	OUT	IN	IN
24K	40K	OUT	IN	OUT	OUT
32K	48K	OUT	IN	OUT	IN
40K	56K	OUT	IN	IN	OUT
48K	64K	OUT	IN	IN	IN
56K	72K	IN	OUT	OUT	OUT
64K	80K	IN	OUT	OUT	IN
72K	88K	IN	OUT	IN	OUT
80K	96K	IN	OUT	IN	IN
88K	104K	IN	IN	OUT	OUT
96K	112K	IN	IN	OUT	IN
104K	120K	IN	IN	IN	OUT
112K	124K	IN	IN	IN	IN

Note: OUT = logic 1, IN = logic 0.

As mentioned earlier, in normal operation the upper 4K of memory addresses is reserved for peripheral devices on the Unibus. In special applications, where the number of peripheral devices is small, some of these reserved addresses can be used by the MM11-D. Thus, if a jumper is inserted at location W8, Unibus addresses from 124K to 126K-1 (760000_8 – 767777_8) will cause NAND gate E27 to be enabled and BANK SEL H will be asserted. If a jumper is inserted at W7, in addition to one at W8, addresses from 124K to 127K-1 (760000_8 – 774000_8) will be assigned to the MM11. Note that for systems without Memory Management, the useful address space can be extended from 28K to 30K-1, or 31K-1.

NOTE

If use of the reserved I/O page of addresses is being considered, check carefully to ensure that, first, no peripheral devices (including bootstrap ROMs) are assigned any of the reserved addresses, and second, all DEC software is compatible with the reduced peripheral address space.

Two MM11-D memories can be interleaved, i.e., one memory can be assigned the odd addresses within a 32K block of addresses, while the other can be assigned the even addresses within the same block. Interleaving is accomplished by inserting jumpers at locations W5 and W6 of each memory's Address Decoding logic and assigning each memory the same starting address (the starting address for interleaved memories is assigned differently than is the starting address for a single memory; Table 3-3 relates interleaved starting addresses and the disposition of jumpers at locations W1 – W4). For example: to interleave two memories so that they cover Unibus address space from 0K – 32K, first insert a jumper at locations W3 and W4 of each memory's Address Decoding logic, thereby setting the starting address at 0K; then, insert jumpers at locations W5 and W6 to assign one memory the even addresses (W5 in, W6 out) and the other memory the odd addresses (W5 out, W6 in). Any address in the assigned 32K block causes adder outputs $\Sigma 3$ and $\Sigma 4$ to be high. However, the $\Sigma 2$ output is not gated through multiplexer E16 to NAND gate E28; instead, the f0 output of the multiplexer represents the state of the BUS A01 L signal. Thus, an odd address (BUS A01 L is asserted) causes f0 of the odd-address-memory multiplexer to be high; BANK SEL H is asserted by this memory. Alternately, an even address (BUS A01 L is negated) causes f0 of the even-address-memory multiplexer to be high and BANK SEL H is asserted by this memory.

Table 3-3
Jumper Assignments for MM11-D Starting Addresses
(Interleaved-Memory Operation)

Starting Address	Ending Address +1	W1	W2	W3	W4
0	32K	OUT	OUT	IN	IN
8K	40K	OUT	IN	OUT	OUT
16K	48K	OUT	IN	OUT	IN
24K	56K	OUT	IN	IN	OUT
32K	64K	OUT	IN	IN	IN
40K	72K	IN	OUT	OUT	OUT
48K	80K	IN	OUT	OUT	IN
56K	88K	IN	OUT	IN	OUT
64K	96K	IN	OUT	IN	IN
72K	104K	IN	IN	OUT	OUT
80K	112K	IN	IN	OUT	IN
88K	120K	IN	IN	IN	OUT
96K	124K	IN	IN	IN	IN

3.5 CONTROL BIT LOGIC

The Control Bit logic is shown in Figure 3-13. Table 3-4 relates the control bits and the write byte bits to the data transfer modes, viz., DATI, DATO, and DATOB (DATIP and DATI are the same in the MM11-D).

Table 3-4
Operating Mode Selection

Mode	BUS C0L	BUS C1L	BUS A0L	WRITE BYTE 1L	WRITE BYTE 0L
DATI	HIGH	HIGH	- -	HIGH	HIGH
DATIP	LOW	HIGH	- -	HIGH	HIGH
DATO	HIGH	LOW	- -	LOW	LOW
DATOB	LOW	LOW	HIGH	HIGH	LOW
			LOW	LOW	HIGH

3.6 MAR LOGIC

The logic shown in Figure 3-14 latches the memory address throughout the memory timing cycle. Address bits A01 L – A13 L and A13 H are used to select the addressed locations. Bits A14 B0/1 H and A14 B0/1 L are used throughout the MM11-D logic to specify the upper and lower halves of the mats.

Note that the signal LEAST BIT H is derived from either BUS A01 L or BUS A15 L. In non-interleaved operation, LEAST BIT H reflects the state of BUS A01 L. However, during interleaved-memory operation, BUS A01 L is used to generate BANK SEL H; consequently, it cannot be used to specify the 14-bit address. In this case, BUS A15 L is selected to generate LEAST BIT H.

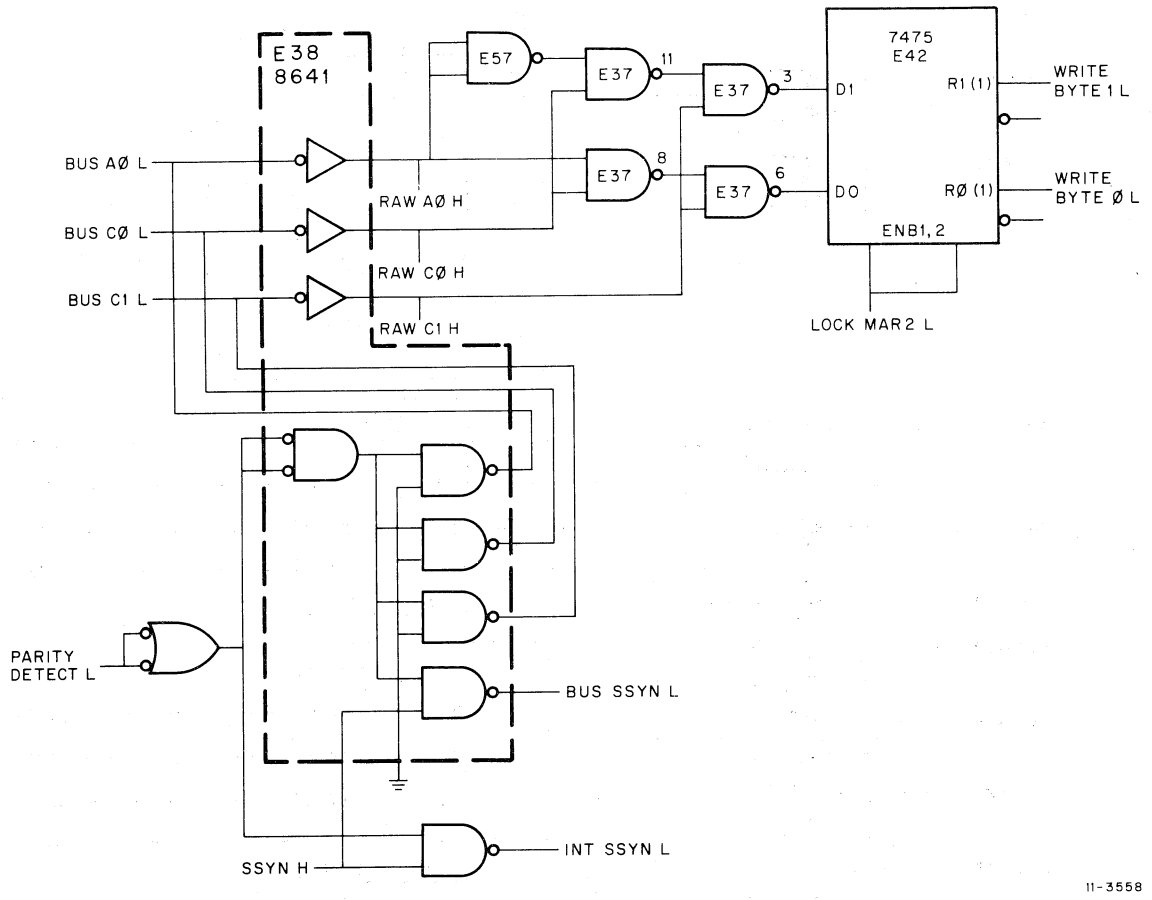


Figure 3-13 Control Bit Logic

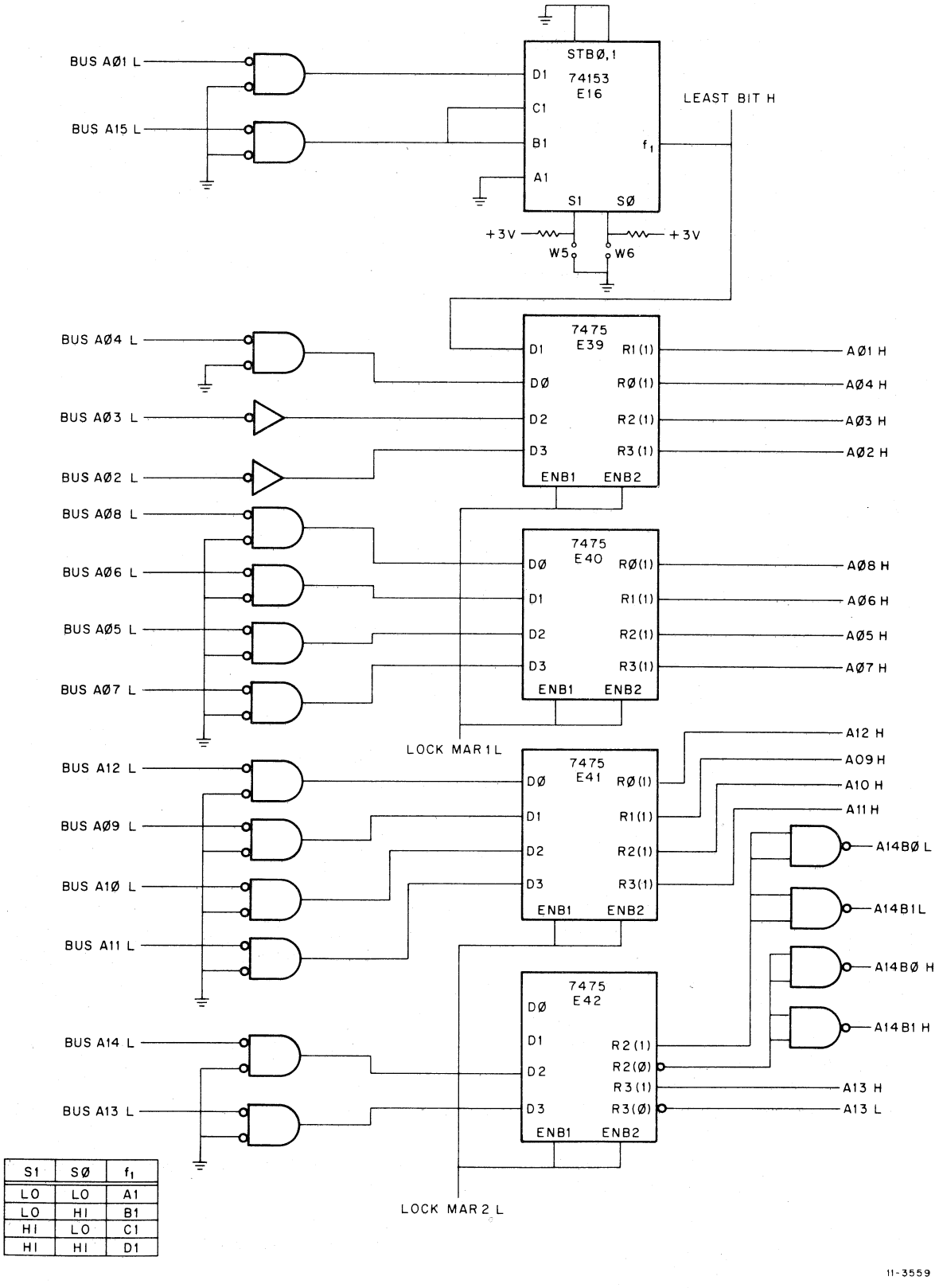
3.7 CONTROL LOGIC

3.7.1 Read Control Logic

The Read Control logic is shown in Figure 3-15. Central to the logic is a 250-ns delay line, E9. A positive edge applied to the input travels down the delay line; when the edge appears at the output, 250 ns later, it is returned to the input circuit, causing the input signal to go low. Hence, a 250 ns positive pulse is available at each output tap, the taps appearing at 25 ns intervals along the line.

When the Address Decoding logic asserts BANK SEL H, the read control timing begins, providing that four conditions are met:

1. The BUS MSYN L signal must be asserted
2. The MSYN H signal must have been generated by the Voltage Monitor circuit, indicating that the dc voltages are within the specified tolerance
3. The NOT BUSY H signal must be asserted, indicating that the memory is not currently executing a memory operation
4. SSYN L must be negated, indicating that the SSYN flip-flop is clear.



S1	SØ	f_1
LO	LO	A1
LO	HI	B1
HI	LO	C1
HI	HI	D1

Figure 3-14 MAR Logic

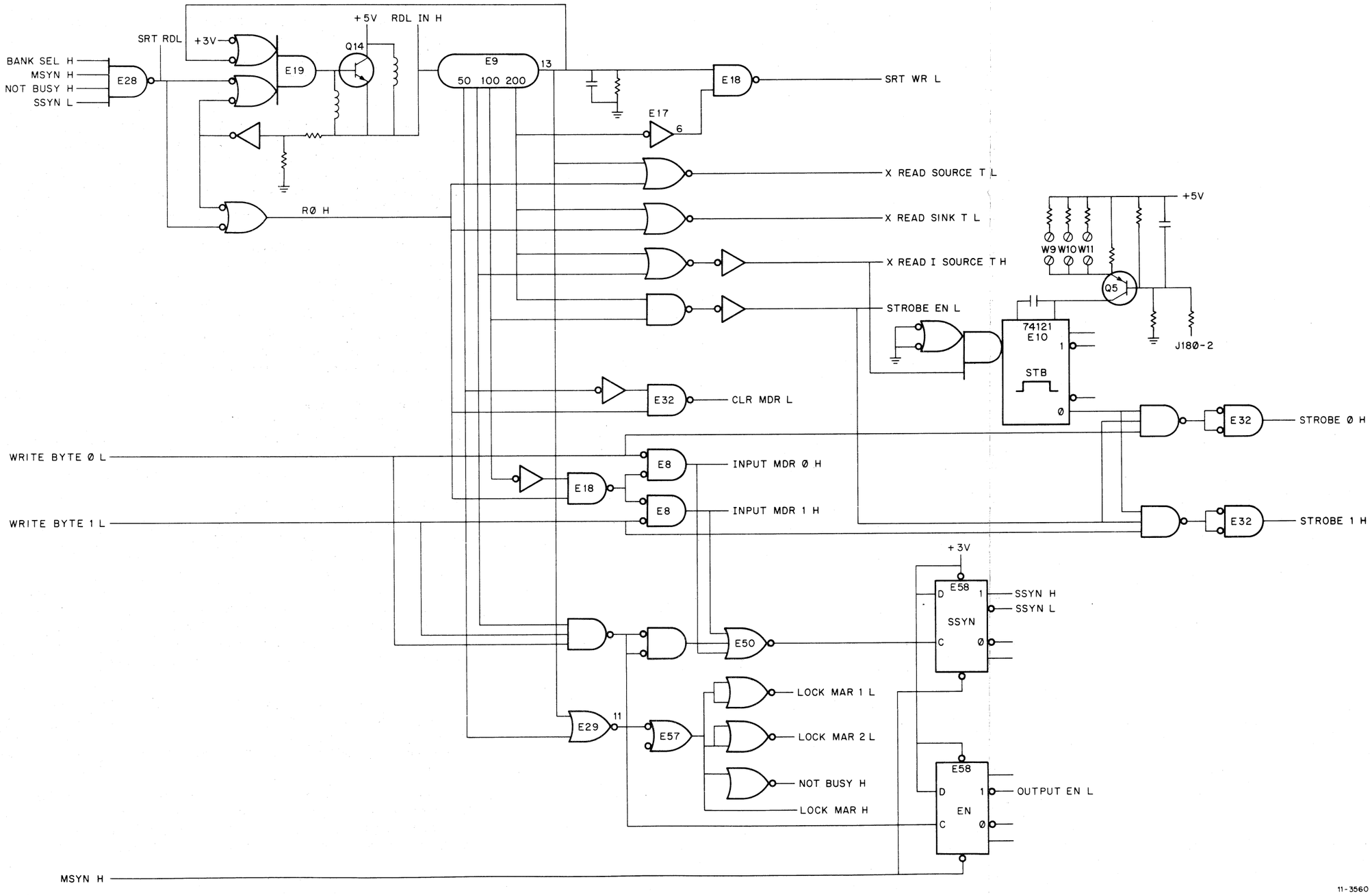


Figure 3-15 Read Control Logic

With these conditions satisfied, the BANK SEL H signal enables NAND gate E28, asserting SRT RD L (Start Read). Transistor Q14 is turned on and RDL IN H (Read Delay Line In) goes high. In approximately 250 ns, the delay line output, pin 13, goes high; the output signal is returned to gate E19, disabling it. Thus, Q14 turns off and the delay line input goes low.

The Read Control timing signals are derived from a number of gates and flip-flops that are contolled by the various delay line taps. Table 3-5 lists the significant signals by name and briefly describes the function of each signal. Figure 3-16 is a timing diagram that relates not only the Read Control signals, but also the Write Control signals, which are described in the following section. The timing is shown completely for a DATI operation. For a DATO operation, most of the signals are the same as the DATI; only the exceptions are shown above the heading DATO. A DATOB operation differs from a DATO only in the WRITE BYTE 0/1L, STROBE 0/1 H, and INPUT MDR 0/1 H signals; these differences are explained in Table 3-5.

Note that the timing of the STROBE 0/1 H signals is variable. These signals are generated, in part, by the STB one-shot (the trailing edge of the one-shot output asserts the STROBE 0/1 H signals). The one-shot output is controlled by a current generator, Q5, which can be varied for margining of the memory by connecting J180-2 to ground or to +5 V. Jumpers can be inserted at locations W9, W10, and W11 to compensate for stack differences and, hence, to achieve the optimum STB one-shot output pulse width. When the optimum pulse width is achieved, the STROBE 0 H and/or STROBE 1 H signals will be generated at such a time that they strobe the sense amplifiers very near the maximum of the voltage output. *The jumpers are inserted at W9, W10, and W11 at the factory and must not be tampered with in the field.*

3.7.2 Write Control Logic

The Write Control logic is shown in Figure 3-17. This logic also features a 250 ns delay line, E31, that operates like E9 of the Read Control logic. The SRT WR L (Start Write) signal begins the write-signal timing; the write signals are derived from a number of gates that are controlled by the various delay line taps. Table 3-6 lists the significant signals by name and briefly describes the function of each signal.

3.8 CURRENT SOURCES CIRCUIT

The circuit shown in Figure 3-18 contains the X and Y current generators; in addition, the circuit generates the Y winding Driver/Switch timing signals. The Driver/Switch control signals turn on the appropriate drivers and switches, enabling read and write currents to flow in the directions that produce coincidence in the selected cores. In the X windings, read currents flow in one direction, write currents flow in the opposite direction. However, because the memory has coincident and anti-coincident cores, the relative direction of the Y currents must be reversed to select the upper 8K of addresses. This reversal of Y current is controlled by multiplexer E72, a 74157 IC. The X read and write timing signals are multiplexed by signal A14B0 H to turn on Y currents that are coincident in "A" cores (lower 8K addresses) when A14B0 H is not asserted, and to turn on Y currents that are coincident in "B" cores (upper 8K addresses) when A14B0 H is asserted.

Figure 3-19 illustrates this concept. Figure 3-19(a) represents two cores, A and B, with both an X and a Y winding passing through each; Figure 3-19(b) depicts relative polarities of the currents in the two windings. If the arrows shown in Figure 3-19(a) represent positive read currents Ix and Iy, there will be coincidence of currents in core A and anti-coincidence in core B. Write currents have the opposite polarity for X and Y and occur later.

To address the upper 8K of memory addresses, the read and write timing is interchanged by the multiplexer. At read time, the source-and-sink combination that had previously been turned on to write into core A is now turned on to read core B. The relative Y current polarities (Iy) are shown as dotted lines in Figure 3-19(b). Once again, write currents for X and Y are opposite in direction from the read currents for the selected address, and occur later.

Two identical sense/inhibit windings carry the inhibit current when data zeros are being written. The reversal of relative polarity indicated for INH B in 3-19(b) is determined by core stack wiring connections internal to the memory system.

Table 3-5
Read Control Signals

Signal Name	Function
X READ SOURCE T L X READ SINK T L	These two signals turn on the selected driver/switch pair in the X Driver/Switch circuit, enabling read current to flow thru the selected X-winding; in the Current Sources circuit they help generate the Y Driver/Switch control signals.
X READ I SOURCE T H	Turns on the X read current generator in the Current Sources circuit; the X read current generator output is named X READ I.G. Turns on the STB 1-shot in the Read Control Signal logic.
STROBE EN L	Instrumental in generating the STROBE 0/1 H signals; when STROBE EN L is high, the STB 1-shot output and the WRITE BYTE 0/1 L signals will assert either, both, or neither of the STROBE 0/1 H signals, depending on the type of data transfer. The trailing edge of STROBE EN H is used to terminate STROBE 0/1 H.
STROBE 0 H STROBE 1 H	These signals strobe the output of the sense amplifier in the Sense/Inhibit circuit into the Memory Data Register (MDR); STROBE 0 H is used with the 8 least significant data bits (0–7), while STROBE 1 H is used with the 8 most significant (8–15). For a DATI operation both signals are generated; for a DATO neither is generated, while for a DATOB one or the other is asserted depending on which data byte is to be simply read and restored.
CLR MDR L	(Clear Memory Data Register) – This signal is applied to the MDR at the beginning of each timing cycle. The signal clears the MDR for a DATI operation, setting the internal data bus (DATA XX H) to logic 0; for a DATO or DATOB operation, the CLR MDR L signal is over-ridden by the data gated to the MDR from the Unibus data lines.
INPUT MDR 0 H INPUT MDR 1 H	These two signals gate data from the Unibus into the MDR; INPUT MDR 0 H is used with data bits 0–7, while INPUT MDR 1 H is used with bits 8–15. For a DATI operation neither signal is asserted; for a DATO, both are asserted, while for a DATOB one or the other, depending on which data byte is to be written, is generated.
OUTPUT EN L	When this signal is asserted during a DATI operation, the output from the MDR is gated onto the Unibus D<15:00> lines.
LOCK MAR 1 L LOCK MAR 2 L	(Lock Memory Address Register) – These signals are applied to the MAR in the MAR logic. When the address is one that has been assigned to the memory, these signals latch the address on the A<14:01> lines into the MAR. The address remains in the register throughout the timing cycle until the signals are negated.

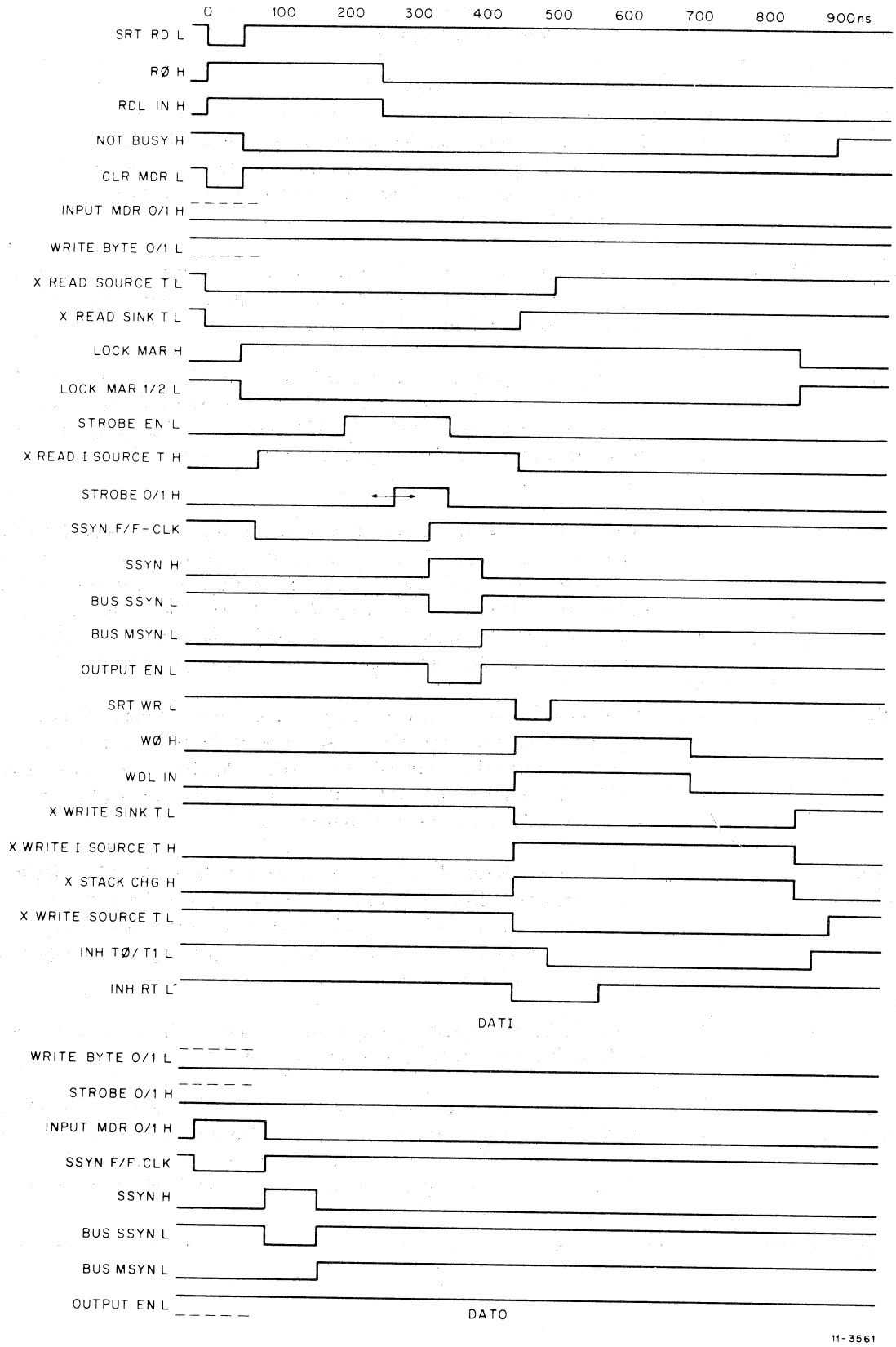


Figure 3-16 Read/Write Timing (DATI and DATO)

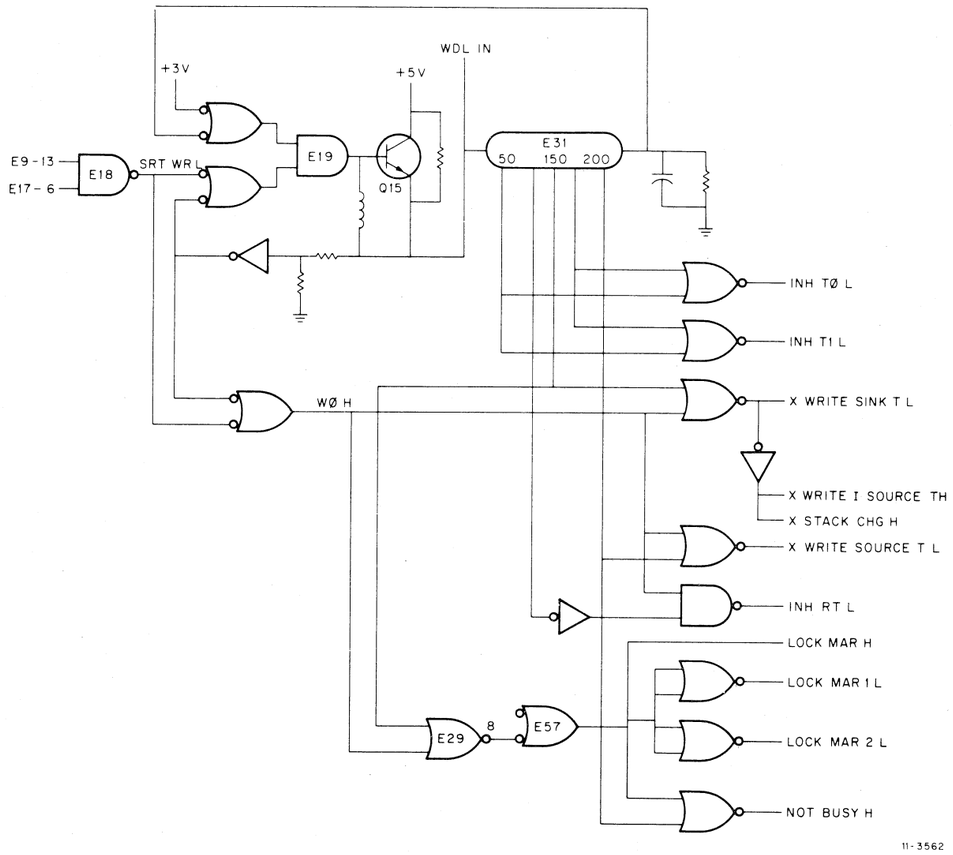
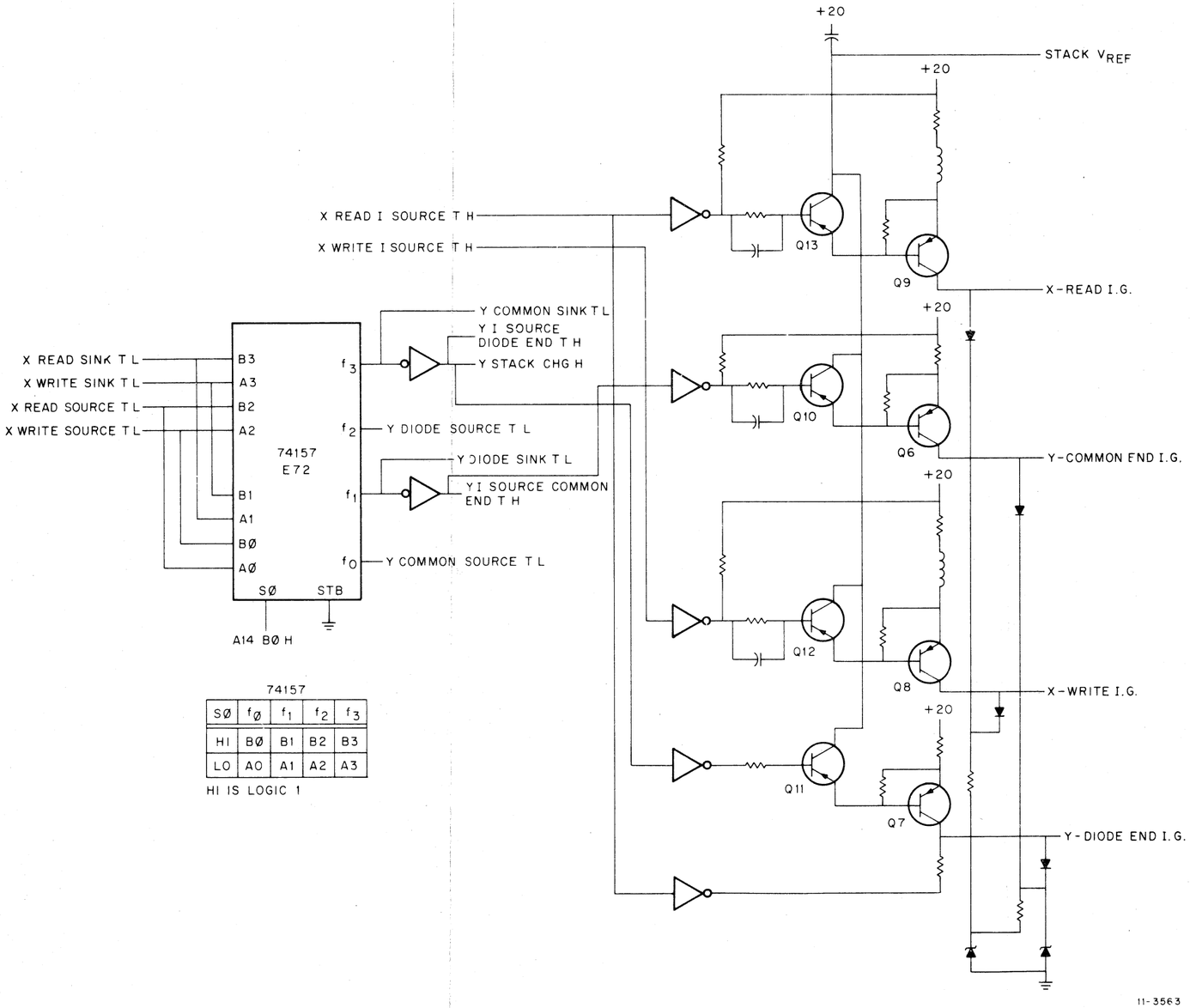


Figure 3-17 Write Control Logic



74157

SØ	$f_Ø$	f_1	f_2	f_3
HI	BØ	B1	B2	B3
LO	AO	A1	A2	A3

HI IS LOGIC 1

Figure 3-18 Current Sources Circuit

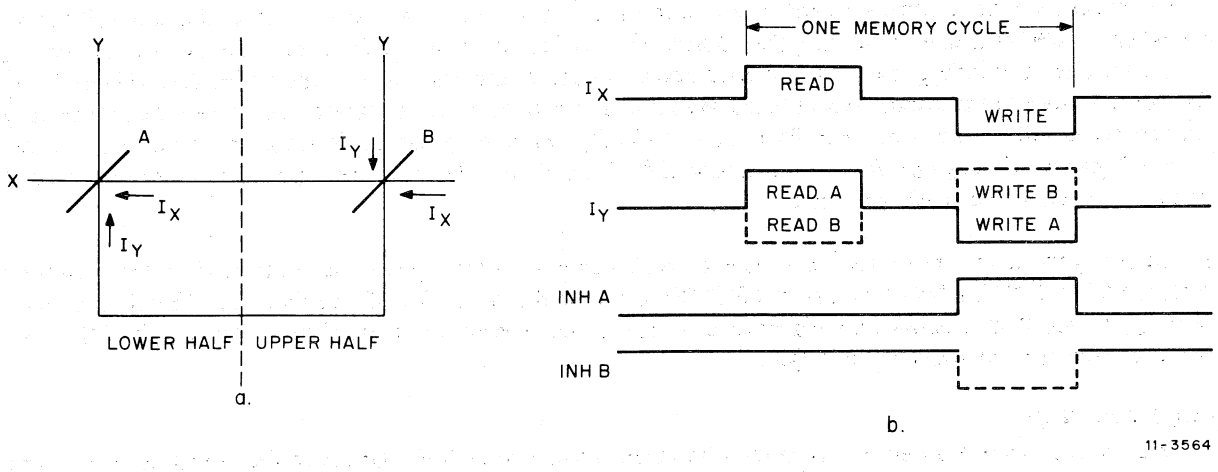


Figure 3-19 Phase Selection

Table 3-6
Write Control Signals – Name and Function

Signal Name	Function
X WRITE SOURCE T L X WRITE SINK T L	These two signals turn on the selected driver/switch pair in the X Driver/Switch circuit, enabling write current to flow through the selected X winding; in the Current Sources circuit they help generate the Y Driver/Switch control signals.
X WRITE I SOURCE T H	Turns on the X write current generator in the Current Sources circuit; the X write current generator output is named X WRITE I.G.
INH RT L	(Inhibit Rise Time) – Whenever a logic 0 must be written into a selected core, the INH RT L signal conditions the Inhibit logic so that the current in the Inhibit winding exhibits the needed characteristics.
INH T0 L INH T1 L	(Inhibit Time) – These signals turn on the inhibit drivers in the Inhibit circuit, enabling current to begin flowing in the Inhibit winding. INH T0 L is used with bits 0–7, while INH T1 L is used with bits 8–15.
X STACK CHG H	Turns on the Stack Charge circuit associated with the X diode matrix.
LOCK MAR 1 L LOCK MAR 2 L	See Table 3-5.

Table 3-7 indicates which X timing signal is transmitted to the Y selection circuitry via multiplexer E72. For example, when A14B0 H is low, indicating the addressed word is in the lower-half of the memory, Y read current flows in the selected Y winding from the common source to the diode sink. Write current for this address flows from the diode source to the common sink (common and diode refer to the common and diode sides of the core stack; the meaning will become clearer in Paragraph 3.10). If the memory address is in the upper 8K of addresses (A14B0 H is high) the timing signals are interchanged for Y, and the relative current polarities in the selected Y drive lines are reversed for read and write.

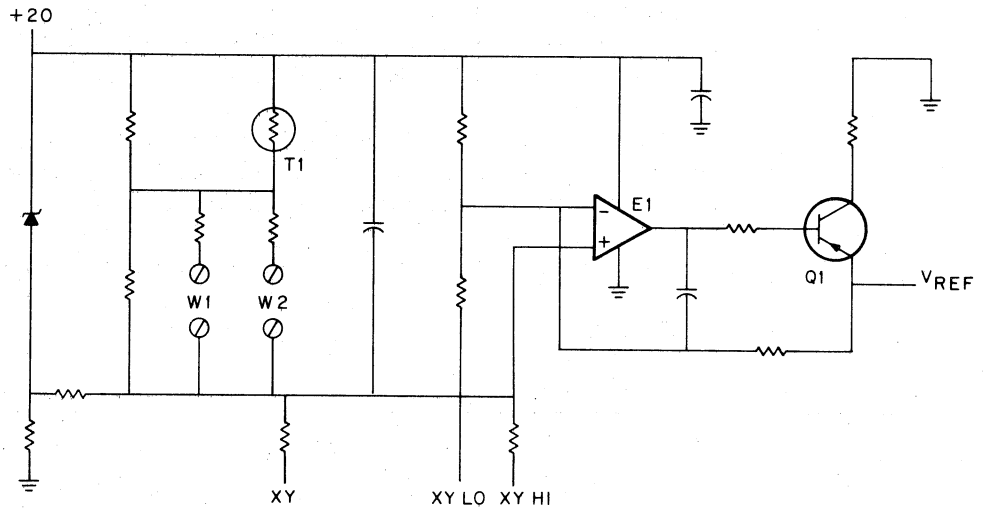
The four current generators are turned on by the X and Y current source signals (the multiplexer outputs include the Y I SOURCE DIODE END T H and Y I SOURCE COMMON END T H signals). Each signal turns on a transistor (Q10 – Q13) that applies a temperature-compensated reference voltage (Vref – Paragraph 3.9) to the base of a constant-current source (Q6 – Q9).

3.9 VREF CIRCUIT

The reference voltage (Vref) is derived from the circuit shown in Figure 3-20. Although the output is taken from Q1, the reference voltage is generated by the operational amplifier (E1) that is biased by a temperature-compensated resistor network.

Table 3-7
Core Location X/Y Control Signals

A14 L	Core Location In Mat	A14B0H	X Control Signals	Y Control Signals
High	Lower Half (Addresses $X00000_8$–$X37777_8$)	Low	X READ SOURCE TL X READ SINK TL X WRITE SOURCE TL X WRITE SINK TL	Y COMMON SOURCE TL Y DIODE SINK TL Y DIODE SOURCE TL Y COMMON SINK TL
Low	Upper Half (Addresses $X40000_8$–$X77777_8$)	High	X READ SOURCE TL X READ SINK TL X WRITE SOURCE TL X WRITE SINK TL	Y DIODE SOURCE TL Y COMMON SINK TL Y COMMON SOURCE TL Y DIODE SINK TL



NOTE: Logic is P/O H222 module

11-3565

Figure 3-20 Vref Circuit

Temperature compensation is provided by thermistor T1. The bias voltage for E1 is adjusted at the factory for the proper stack current using jumpers at location W1 and W2. The XY signal is used for external control of Vref, only by factory test equipment. XY LO and XY HI are brought out to the Field Service connector (J180) and are used to margin the XY stack currents.

3.10 DRIVER/SWITCH CIRCUIT

3.10.1 X Driver/Switch Circuit

The X Driver/Switch circuit is partially illustrated in Figure 3-21. The circuit consists of 7442 decoders and 75325 memory drivers. Each decoder output connects to two memory drivers; for clarity, drivers are shown only at output f0 of each decoder. Part of the diode matrix is also shown in the figure; two X windings, with their 128 ferrite cores and 2 diodes per data bit, are represented.

When an assigned memory location is addressed to take part in a data transfer, the timing logic generates Read Control signals, followed by Write Control signals. During the read half of the timing cycle, current must pass through the addressed core in one X direction; during the write half of the cycle the current direction must be reversed. Figure 3-21 shows how the direction of current flow through the core is controlled.

Any MM11-D address that has bits A<13:07> L negated (logic 0) causes output f0 of decoders E88 and E82 to go low. During the read half of the timing cycle, control signals X READ SOURCE T L and X READ SINK T L are asserted; thus, NOR gates E89 and E104 are enabled. These two gates turn on the transistors at their outputs. Current from the read current generator, represented by signal X READ IG, flows through source transistor "A", through the cores in the direction indicated, through diode "B", and through sink transistor "B" to ground. During the write half of the timing cycle, control signals X WRITE SOURCE T L and X WRITE SINK T L are asserted; thus, NOR gates E107 and E81 are enabled, turning on the transistors at their outputs. Write current, represented by signal X WRITE IG, flows through diode A and to ground through the transistor at the output of E81.

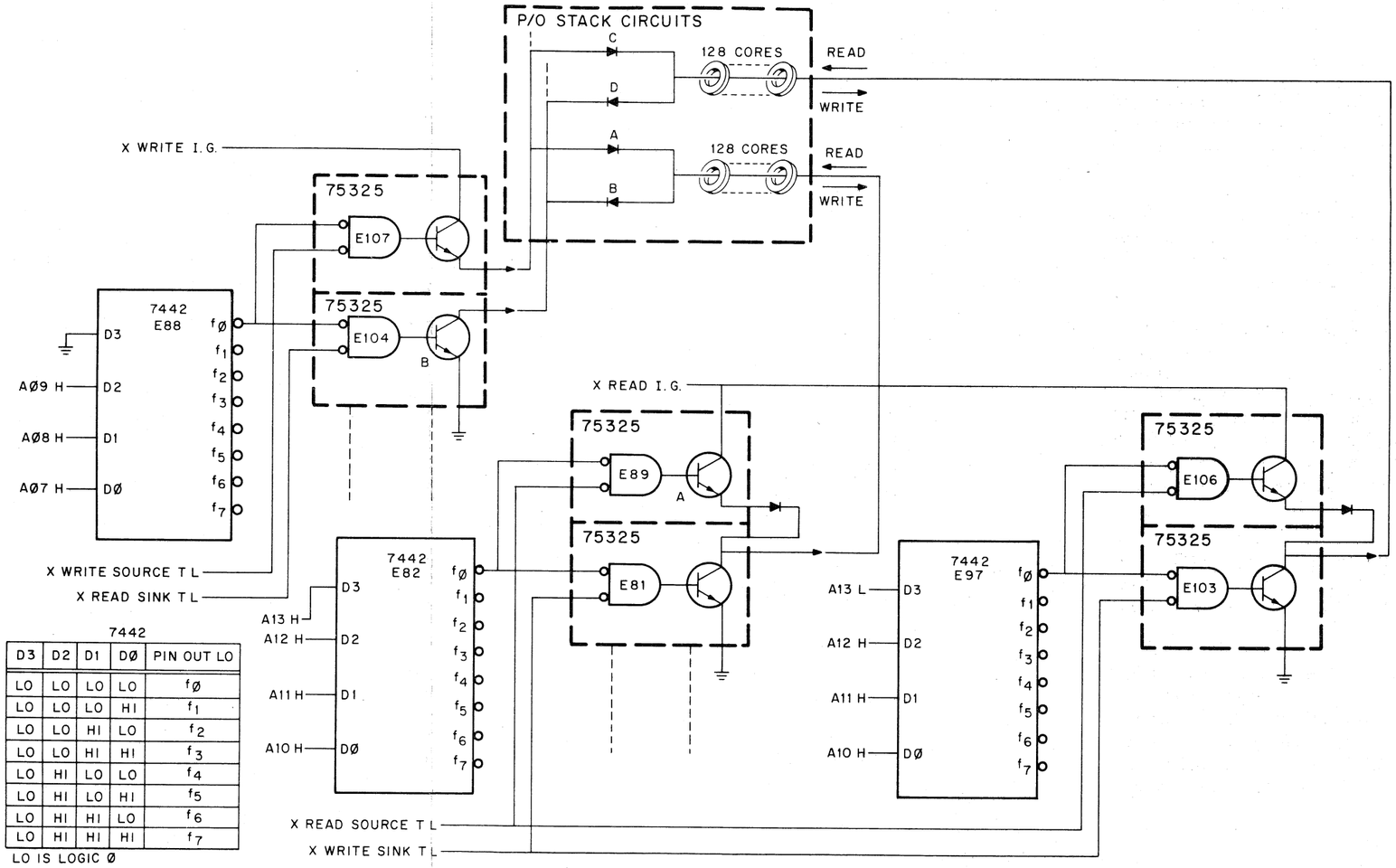
Assume that an address having bits A<12:07> L negated and bit A13 L asserted is decoded by the MM11-D. Now, output f0 of decoder E97 goes low. Drivers E106 and E103 become part of the read/write current paths, operating exactly as E89 and E81. However, the current now passes through the upper winding and includes diodes C and D, rather than A and B.

The memory drivers, 75325, can be described in relation to their functions (for X-drive selection, only). Thus, driver E107 is designated a positive write driver, while E81 is designated a negative write switch. Conversely, E104 is designated a negative read driver, while E89 is termed a positive read switch. There are 8 positive write drivers and 8 negative read drivers; there are 16 negative write switches and 16 positive read switches. Each pair of drivers connects to 16 X windings of 128 cores, and to 16 pairs of switches; consequently, 128 X windings can be addressed by the complete X driver logic shown in logic drawing D-CS-G652-0-1. Table 3-8 relates the read and write functions to the various driver/switch enabling signals.

3.10.2 Y Driver/Switch Circuit

The Y Driver/Switch circuit is partially illustrated in Figure 3-22. This circuit is similar to the X Driver/Switch circuit, i.e., it consists of decoders, drivers, and switches. However, since there are only 64 separate Y windings, only two decoders are needed to accommodate the 6 address bits, A<06:01> L.

Remember that the MM11-D has coincident and anti-coincident cores on the Y windings. Each winding, such as that illustrated in Figure 3-22, passes through 256 cores per data bit (one group of 128 cores is labelled A, the other B). When current flows through the cores in either Y direction, a single core in one group will experience coincident X and Y currents, while a single core in the other group experiences anti-coincident currents.



7442

D3	D2	D1	DØ	PIN OUT LO
LO	LO	LO	LO	fØ
LO	LO	LO	HI	f1
LO	LO	HI	LO	f2
LO	LO	HI	HI	f3
LO	HI	LO	LO	f4
LO	HI	LO	HI	f5
LO	HI	HI	LO	f6
LO	HI	HI	HI	f7

LO IS LOGIC Ø

Figure 3-21 X-Driver Circuit

Table 3-8
X Driver/Switch Enable Signals

Function	Current Source	Enable Signals	Driver/Switch Enabled
Read	X READ I.G.	X READ SOURCE T L X READ SINK T L	Positive Read Switch Negative Read Driver
Write	X WRITE I.G.	X WRITE SOURCE T L X WRITE SINK T L	Positive Write Driver Negative Write Switch

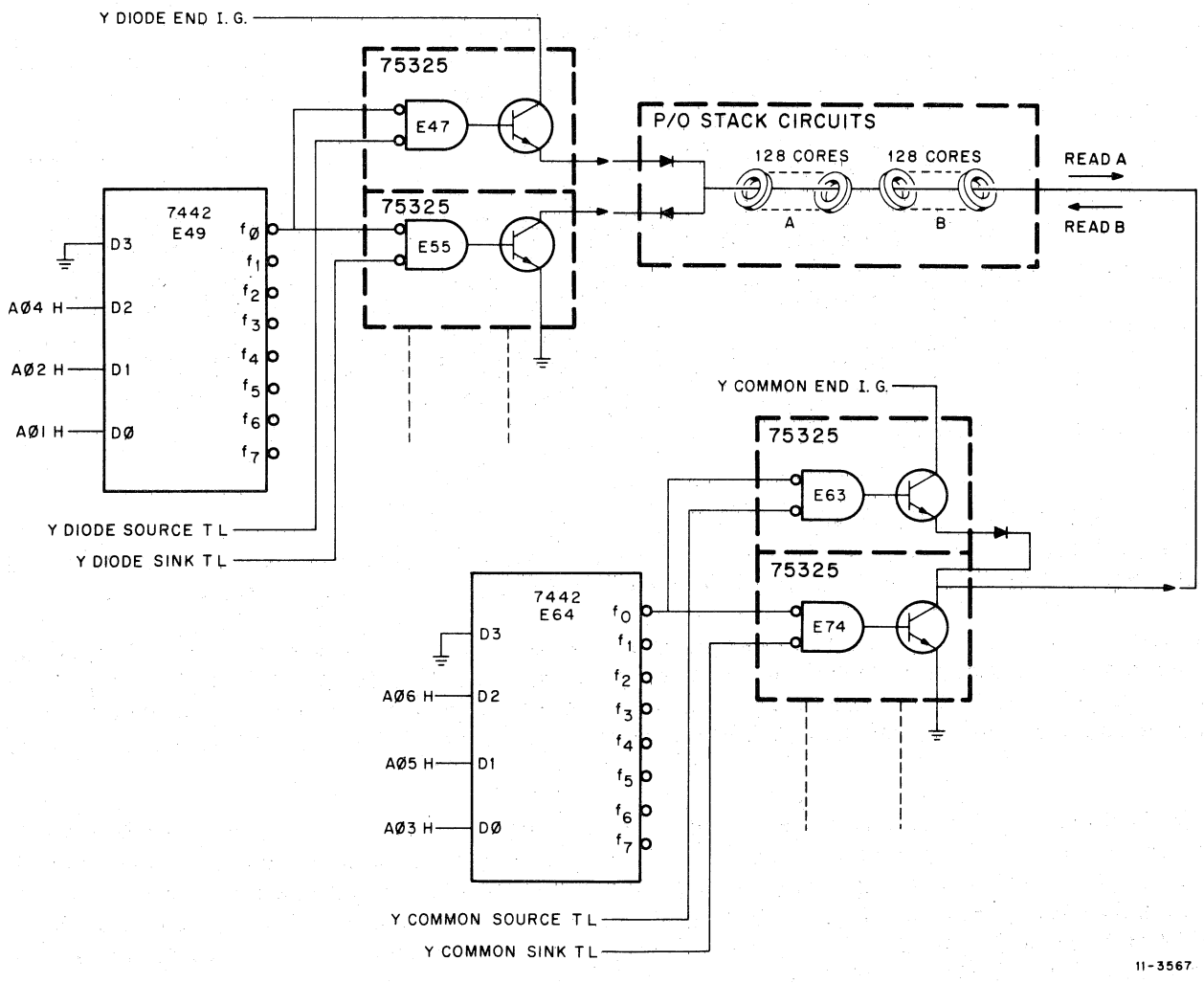


Figure 3-22 Y-Driver Circuit

The direction of current in the Y winding depends on whether the core to be selected is located in the upper or lower-half of the mat. If the core is in the lower-half of the mat, i.e., the core address is between $X00000_8$ and $X37777_8$, current flows from right to left (in Figure 3-22) during the read half of the timing cycle; current flows from left to right during the write half of the timing cycle. Conversely, if the core is located in the upper-half of the mat, i.e., the core address is between $X40000_8$ and $X77777_8$, current flows from left to right during the read half of the timing cycle; current flows from right to left during the write half of the cycle. Table 3-9 summarizes not only the relationship between core address and current direction in the Y winding, but also the relationship of the read and write functions to the various driver/switch enabling signals. The relationships expressed in the table are developed from the Current Sources circuit, which was described in Paragraph 3.8.

Note that the 75325 drivers have been designated drivers and switches, as were those of the X Driver/Switch logic. Each pair of drivers connects to 8 Y windings of 256 cores, and to 8 pairs of switches; consequently, 64 Y windings can be addressed by the complete Y driver logic, shown in logic drawing D-CS-G652-0-1.

Table 3-9
Y Winding Signal Relationship

Core Mat Location	Function	Current Source	Enable Signals	Driver/Switch Enabled
Upper Half	Read	Y DIODE END I.G.	Y DIODE SOURCE TL Y COMMON SINK TL	Positive Diode Driver Negative Diode Switch
	Write	Y COMMON END I.G.	Y COMMON SOURCE TL Y DIODE SINK TL	Positive Common Switch Negative Common Driver
Lower Half	Read	Y COMMON END I.G.	Y COMMON SOURCE TL Y DIODE SINK TL	Positive Common Switch Negative Common Driver
	Write	Y DIODE END I.G.	Y DIODE SOURCE TL Y COMMON SINK TL	Postive Diode Driver Negative Diode Switch

3.11 SENSE/INHIBIT CIRCUIT

The Sense/Inhibit circuit is shown in Figure 3-23. The logic transfers information between the selected core and the Unibus data lines. The logic illustrated is for data bit D00; all other data bits have identical circuits.

Consider a DATI operation – the logic state represented by the selected core must be gated to the BUS D00 line. At the start of the timing cycle, the timing logic asserts CLR MDR L (Clear Memory Data Register); this signal disables gate C of the 7520 sense amplifier, which provides one input of gate B. Since gates A are disabled until the STROBE 0 H signal is generated later in the cycle, gate B is disabled and the DATA 00 H signal is latched low.

When the read currents are generated, the selected core may or may not change state. If the core represented logic 1 before current coincidence, it switches state at coincidence, a voltage is induced in the sense winding, and the Sense Amplifier (SA) output goes high (depending on which half of the mat the core is in, either SA A or B provides the output). When the STROBE 0 H signal is asserted, gate A is enabled, causing gate B to assert the DATA 00 H signal. Because CLR MDR L is now high, gate C is enabled and one input of the 8641 NAND gate A goes high. When OUTPUT EN L goes low, the BUS D00 L signal is asserted.

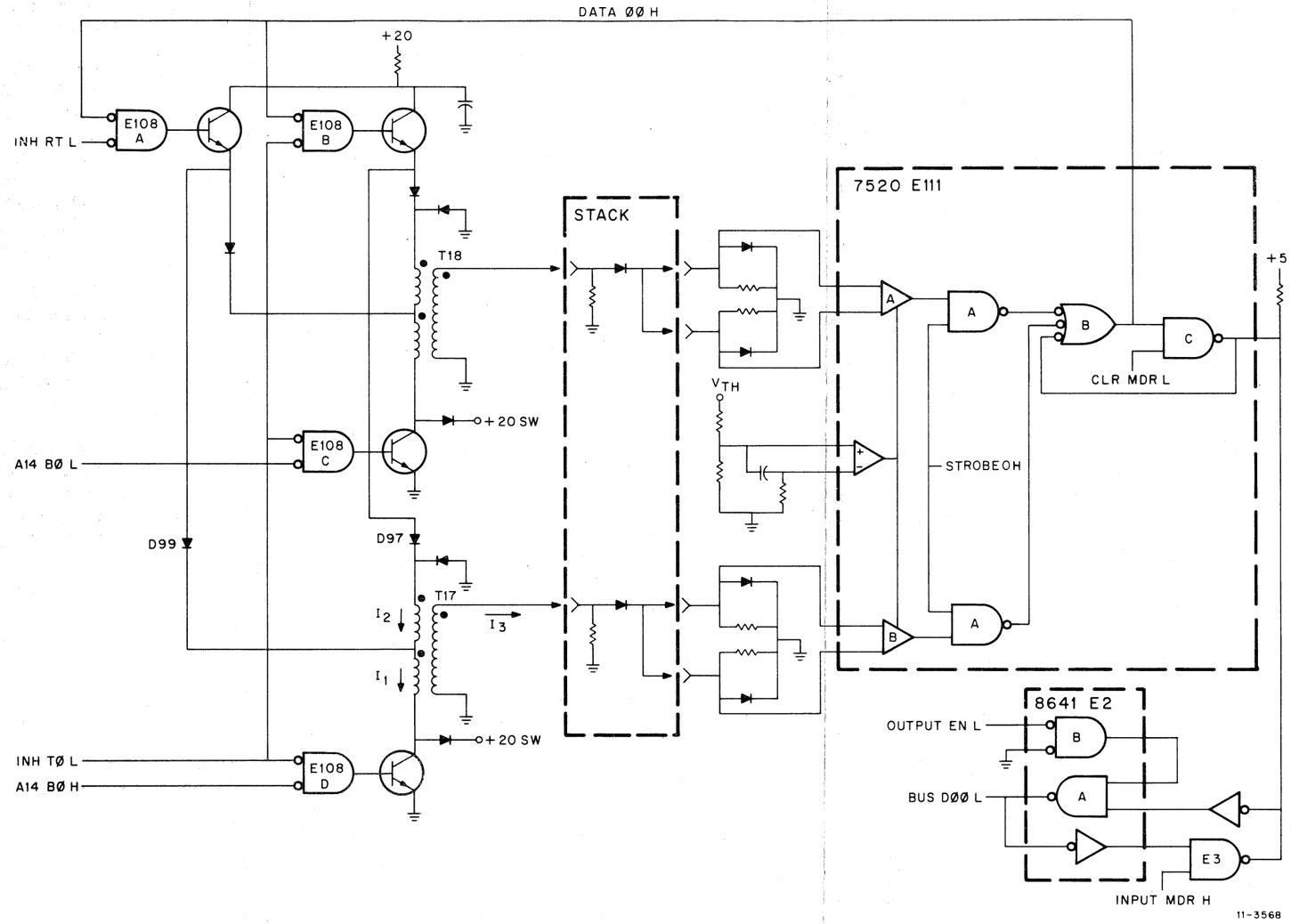


Figure 3-23 Sense/Inhibit Circuit (Bit 00)

When the core switched state at read current coincidence it was left in the 0-state. During the write half of the timing cycle, current coincidence will cause the core to switch back to the 1-state, restoring the information. However, if the core had been in the 0-state before read current coincidence, write current coincidence would cause the core to be restored to a logic 1-state, rather than to a logic 0-state. Hence, in this situation an inhibit current must be generated during the write half of the cycle; the inhibit current will oppose the Y winding current and thus prevent the core from being switched to the 1-state.

If the DATA 00 H signal is low at the start of the write half of the timing cycle, indicating that the selected core was in the 0-state before read coincidence, the INH RT L (Inhibit Rise Time) signal will enable inhibit driver E108A. None of the other gates – E108B, C, and D – is enabled as yet; hence, no current flows through the transformer windings. When the INH T0 L (Inhibit Time) signal is asserted, E108B and either E108C or D are enabled. (If the core is in the upper half of the mat, for example, A14B0 H is negated and E108D is enabled.) Current flows through the transistor of E108A, through diode D99, through the lower primary winding of T17, and through the transistor of E108D to ground. No current flows in the upper primary winding yet, even though E108B is enabled, because the transformer voltage characteristics result in diode D97 being reverse-biased. The lower primary current (I1) increases, as illustrated in Figure 3-24.

When INH RT L is negated, D97 becomes forward-biased; current I2 starts to flow through the transistor of E108B, through D97, through both primary windings, and through the transistor of E108D to ground. I2 flows until INH T0 L is negated and reaches a maximum of approximately 350 mA. The secondary current (I3) flows as illustrated in Figure 3-24, attaining a maximum of approximately 700 mA. The current that flows in each half of the inhibit winding is about 350 mA, enough to counteract the current in the Y winding, thus, preventing the net current through the selected core from exceeding the switching threshold of the core.

The technique used to generate the inhibit current results in a desirable balance of fast current rise time and low power supply drain. That is, as long as INH RT L is asserted, the 1:1 transformer ratio produces a rapid rise time of the secondary current to near-maximum value; when INH RT L is negated, the 2:1 transformer ratio produces a secondary current twice the primary value, obviating the necessity of drawing the entire current from the +20 V power supply.

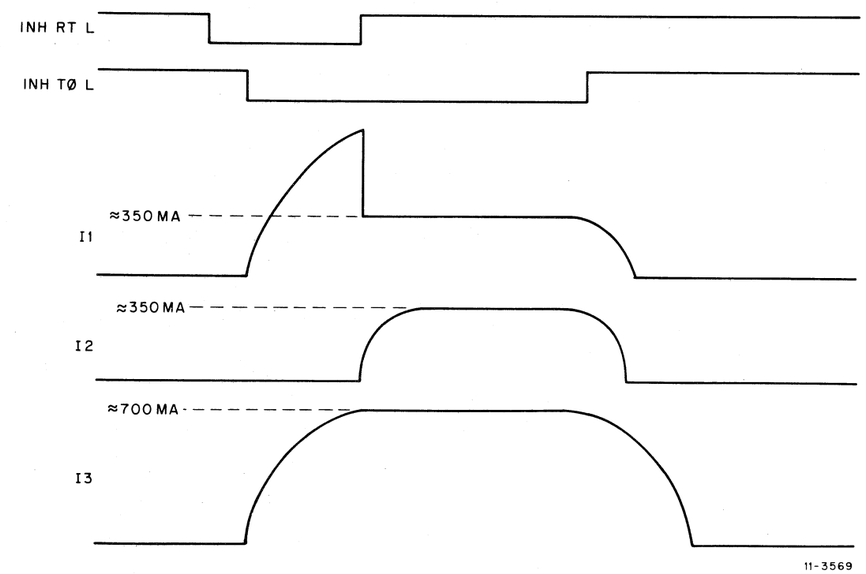


Figure 3-24 Inhibit Current Timing

If a DATO operation is programmed, CLR MDR L is asserted at the beginning of the timing cycle. However, INPUT MDR H is also asserted; consequently, the data placed on the BUS D00 line by the bus master is gated to the MDR and latched onto the DATA 00 line. The selected core is sensed by the SA but STROBE 0 H is not generated; hence, the state of the core before read current coincidence has no bearing on the DATA 00 H signal. If the BUS D00 L signal is logic 1 (low), the DATA 00 H signal is asserted. The core will be switched to the logic 1-state at write coincidence; if BUS D00 L is logic 0, the inhibit current must be generated to prevent the core from being switched.

A DATOB operation is similar to a DATO. The byte specified by the BUS A00 L signal is operated on as described for the DATO; the other byte is handled as a simple read-restore operation.

3.12 STACK CHARGE CIRCUIT

The Stack Charge circuits are located on the H222 module. There is a separate circuit for the X diode matrix and the Y diode matrix. The X Stack Charge circuit is shown in Figure 3-25, along with part of the X Driver/Switch circuit *(jumper W5 is removed for in-plant testing; it should not be removed in the field)*. The Y Stack Charge circuit is similar and is not shown.

The Stack Charge circuit assists the stack capacitance in recovering and shortens the rise time of the stack current [the effective stack capacitance associated with each line is shown as C (STACK)]. It also reduces unwanted currents in the unselected lines associated with the selected driver.

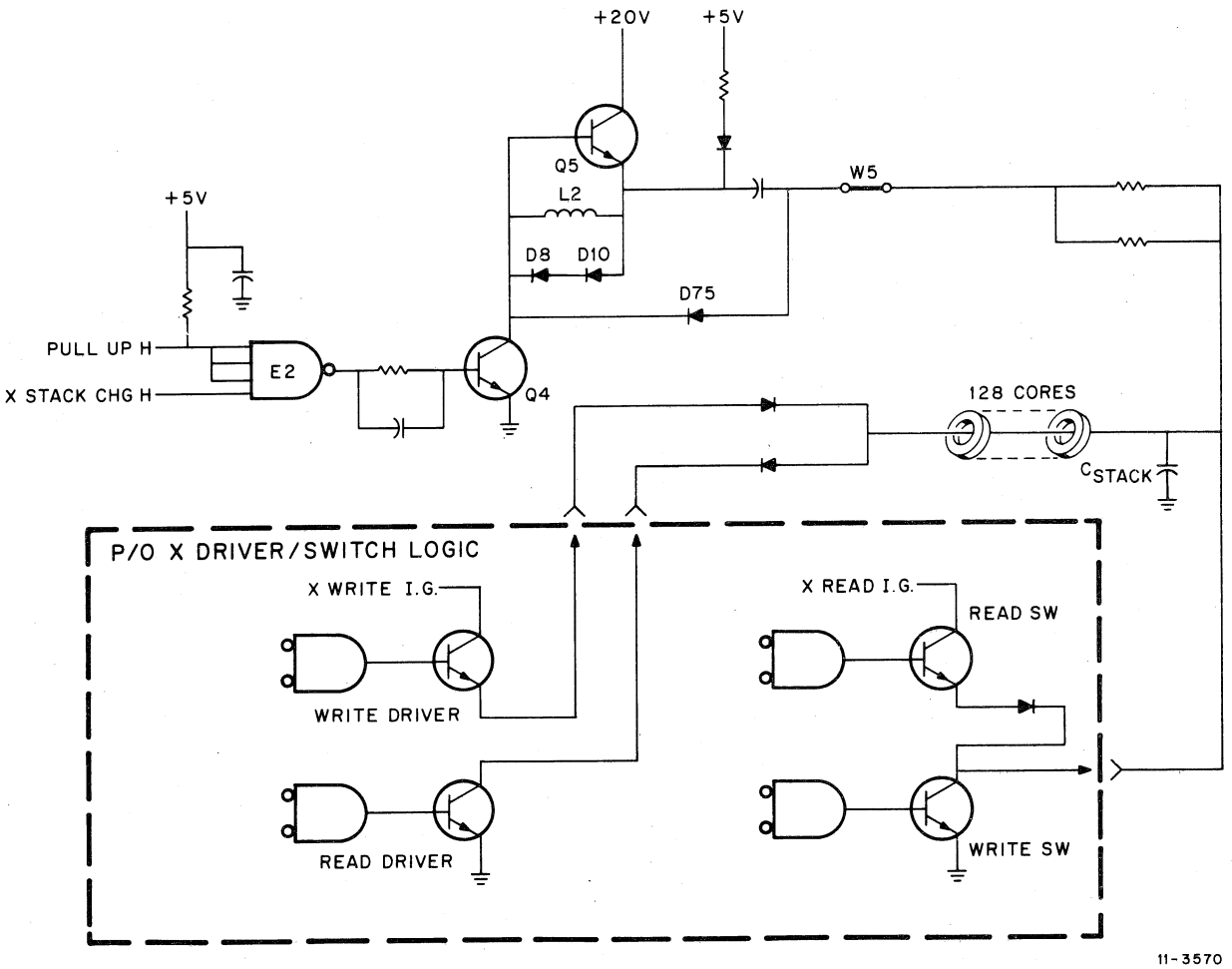


Figure 3-25 X Stack Charge Circuit

The output of the Stack Charge circuit is taken from the emitter of Q5 and goes to the junction of each X read/write switch pair via a resistor. During a read operation, the emitter voltage [V(E)] of Q5 should be approximately 20 volts. During a read operation, X STACK CHG H is low, turning on Q4. V(E) is held low by the parallel combination of L2 and D8/D10. Current flows through L2; thus, Q5 is off, since its base-emitter junction is reverse-biased.

During a write operation, X STACK CHG H is asserted, causing Q4 to turn off. The current flowing through L2 is forced to flow into the base of Q5, turning it on and taking V(E) to near +20 volts.

The Y-axis charge circuit operates in a similar way; however, the phase selection of Y addresses requires that the charge circuit operation be interchanged for half the addresses, the interchange being controlled by multiplexer E72 and address bit A14. Thus, the stack Y common end will be pulled toward +20 volts during write for addresses in the lower 8K (BUS A14 L not asserted) and will be pulled toward +20 volts during read for addresses in the upper 8K (BUS A14 L asserted).

CHAPTER 4
MAINTENANCE

4.1 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks, performed at intervals, to detect conditions that could lead to subsequent performance deterioration or malfunction. The following tasks are considered preventive maintenance and are recommended to be performed every six months.

1. Visual Inspection
2. Voltage measurements
3. SSYN DLY check (for parity memories)
4. Strobe and Drive current margins
5. MAINDEC testing

The two pieces of test equipment recommended for checking and troubleshooting the memory are the Tektronix 453 Dual Trace Oscilloscope (or equivalent) and the Weston Schlumberger Model 4443 Digital Voltmeter (or equivalent) with 0.5 % accuracy.

CAUTION

Make sure all power is off before installing or removing modules.

4.1.1 Visual Inspection

Visually inspect the modules and backplane for broken wires, connectors, or other obvious defects.

NOTE

All tests and adjustments must be performed in an ambient temperature range of 20 to 30 degrees C (68 to 86 degrees F).

4.1.2 Voltage Measurements

Turn on the primary power and measure the +20 V, +5 V and -5 V voltages at the option backplane. All voltages must be within ±5% tolerance.

4.1.3 SSYN DLY Check (for parity memories only)

Refer to M7850 parity controller manual.

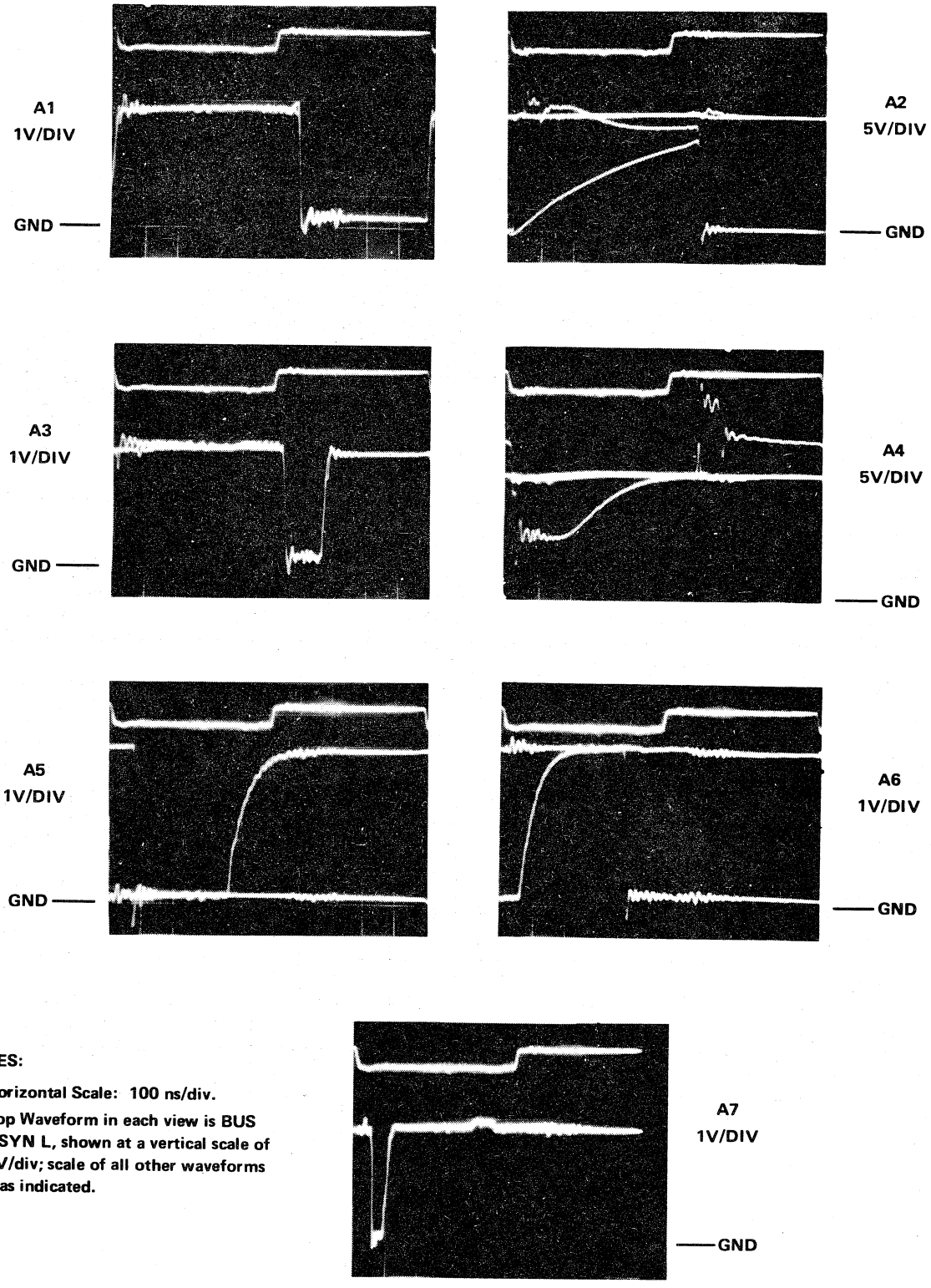
4.1.4 Strobe and Drive Current Margins

A Field Service connector (J180) is provided on the front of the G652 module for margining a given memory while running a diagnostic program.

Symptom \ Possible Location(s) of Problem	-5 V	Device Selection Jumpers	Delay Flip Flop or Delay Line	MSYN Flip Flop	SSYN Flip Flop	STROBE 0/1 H	CLR MDR L	INPUT MDR 0/1 H	INH RT L, INH T0/T1 L, A14 0/1 H	Bus Driver Receiver	Sense Terminator	Data Register	Inhibit Driver	Threshold Circuit	Power ON/OFF Circuit	Stack Sense/Inhibit Line	Stack X-Y Line	Stack Diode	Stack Thermistor	XY Voltage REF Circuit	Stack Discharge Circuit	X Current Source	Y Current Source	Y DR	Y SS	X DR	X SS	Read/Write Timing	Backplane	+5 V	+20 V	Sense Amplifiers
Memory Does Not Respond To MSYN		X	X	X	X					X					X														X	X		
Memory Hangs Bus					X																											
DATO Fails							X	X		C01		X	X															X	X			
Many Bits Fail	X					X	X	X	X					X						X	X							X		X	X	
Picks Bits	LO					LO						X	X	LO						X	X	HI	HI					X			LO	
Drops Bits	HI					HI								HI						X	X	LO	LO					X				
Byte Failures						X	X	X	X	A0																						
2 Bits Fail											X	X		X																		
1 Bit Fails										X	X	X	X			X													X	X		X
Fails All Addresses	X	X													X				X	X	X	X	X					X	X	X	X	
A1, A2, A4 Common																	X	X						X								
A3, A5, A6 Common																	X	X							X							
A7–A9 Common																	X	X								X						
A10–A13 Common																	X	X									X					
No Inhibit									X				X																			

X: Circuit Not Operable
LO: Measured Parameter Too Low or Early
HI: Measured Parameter Too High or Late

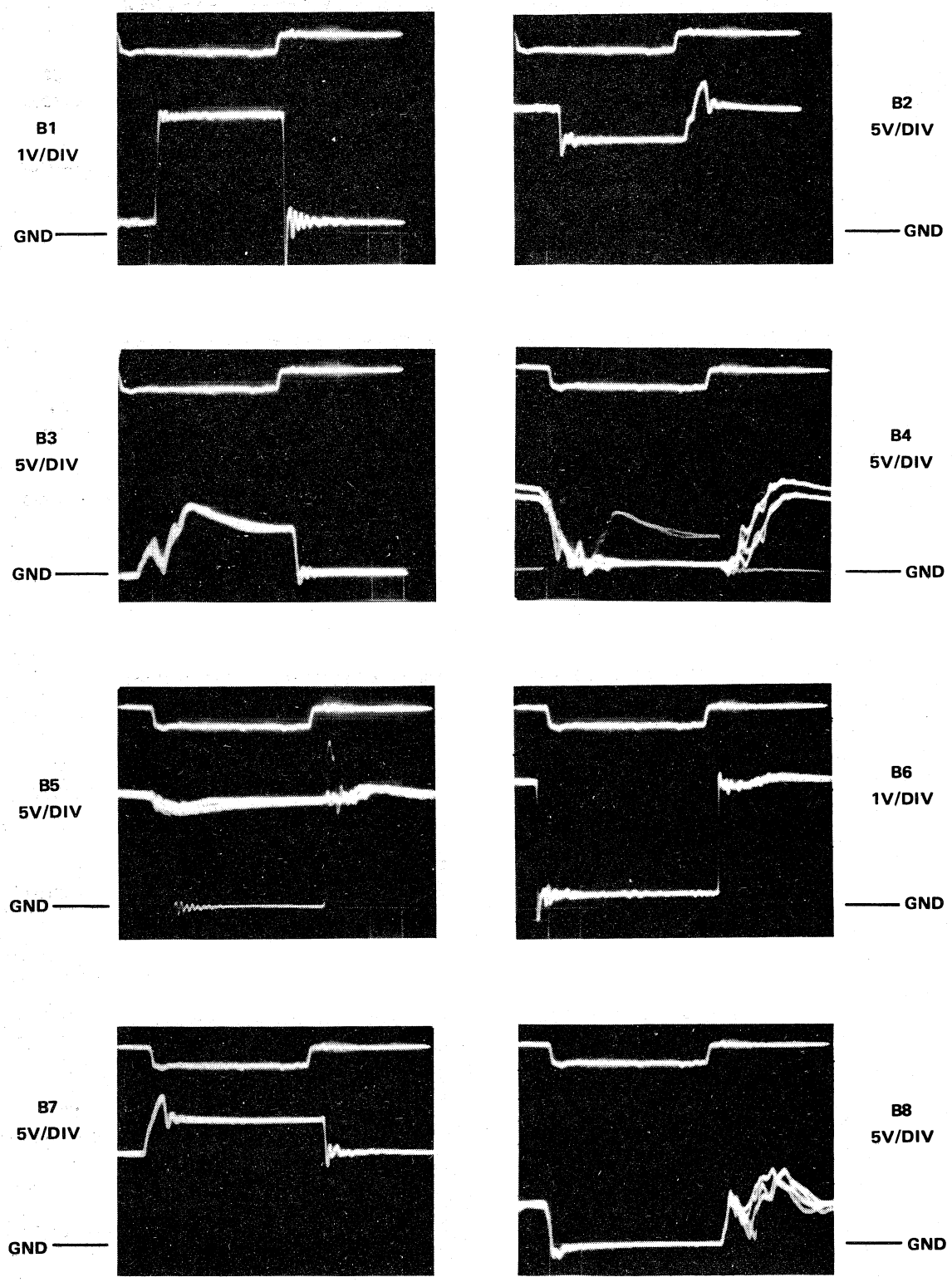
Figure 4-1 Troubleshooting Chart



NOTES:

1. **Horizontal Scale: 100 ns/div.**
2. **Top Waveform in each view is BUS MSYN L, shown at a vertical scale of 5 V/div; scale of all other waveforms is as indicated.**

Figure 4-2 MM11-D Waveforms (A)

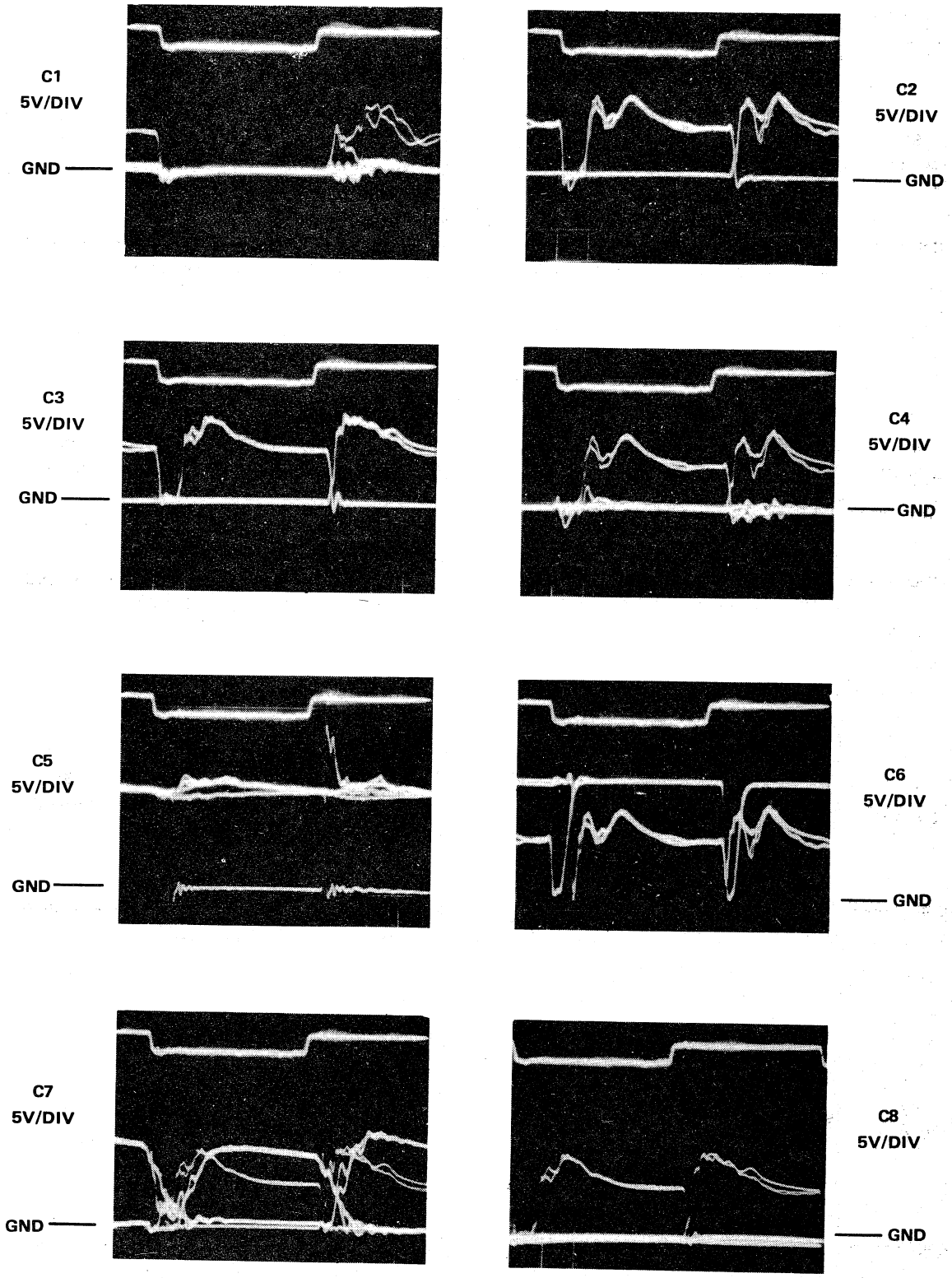


NOTES:

1. Horizontal Scale: 100 ns/div.
2. Top Waveform in each view is BUS MSYN L, shown at a vertical scale of 5V/div; scale of all other waveforms is as indicated.

MI 0286

Figure 4-3 MM11-D Waveforms (B)



NOTES:

1. Horizontal Scale: 100 ns/div.
2. Top Waveform in each view is BUS MSYN L, shown at a vertical scale of 5V/div; scale of all other waveforms is as indicated.

MI 0287

Figure 4-4 MM11-D Waveforms (C)

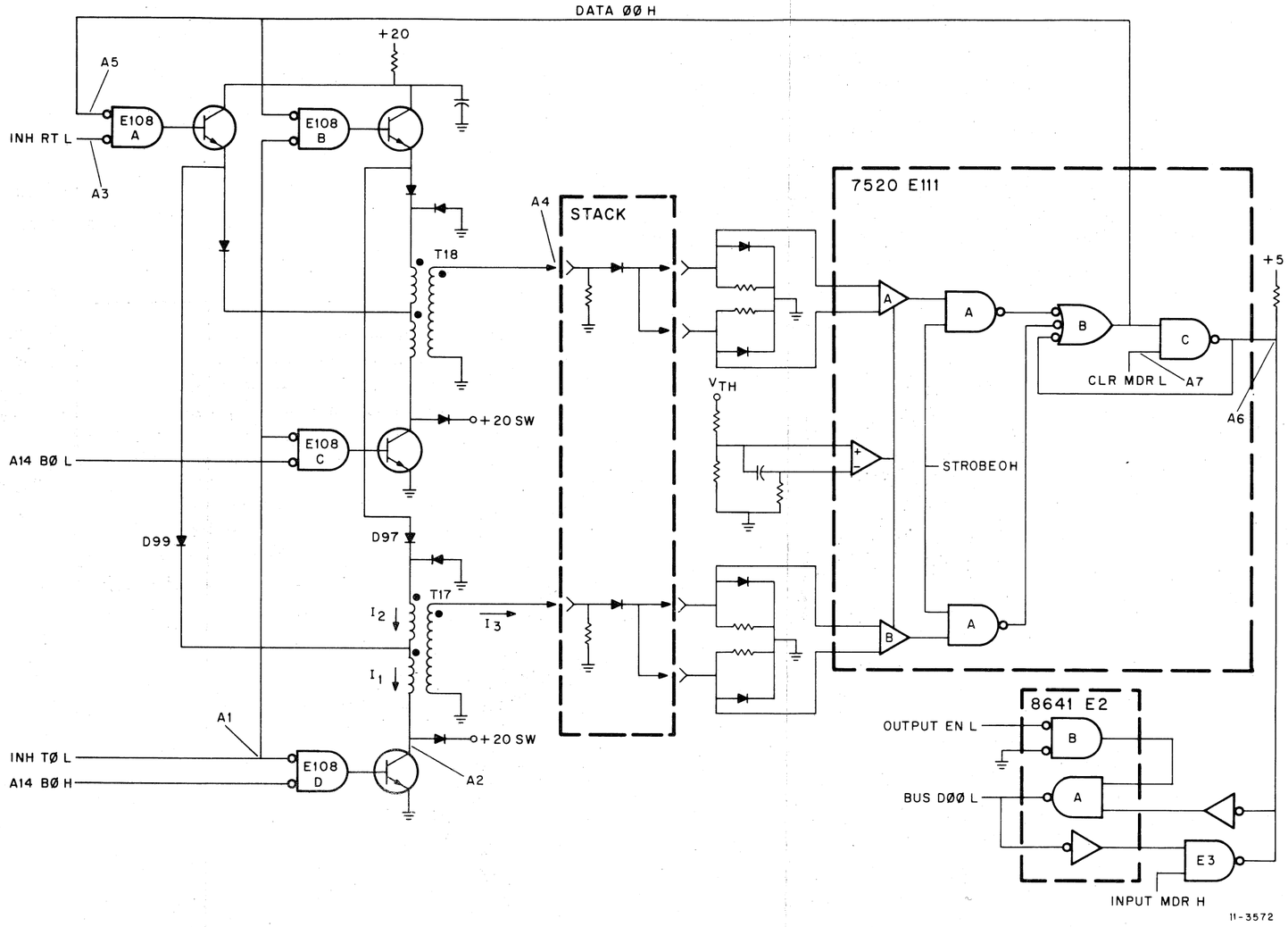


Figure 4-5 Waveform Key A (Sense/Inhibit Circuit)

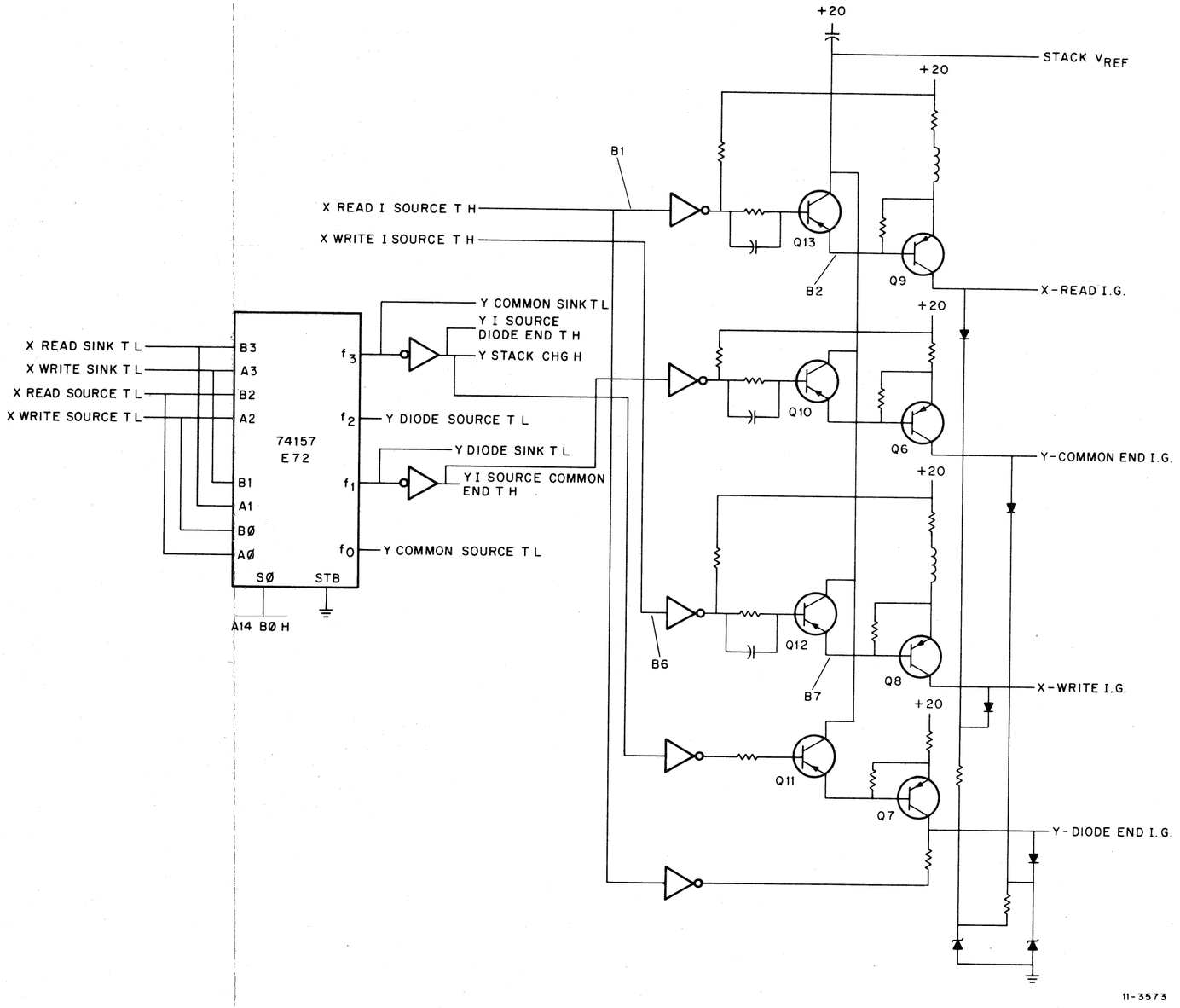


Figure 4-6 Waveform Key B (Current Sources Circuit)

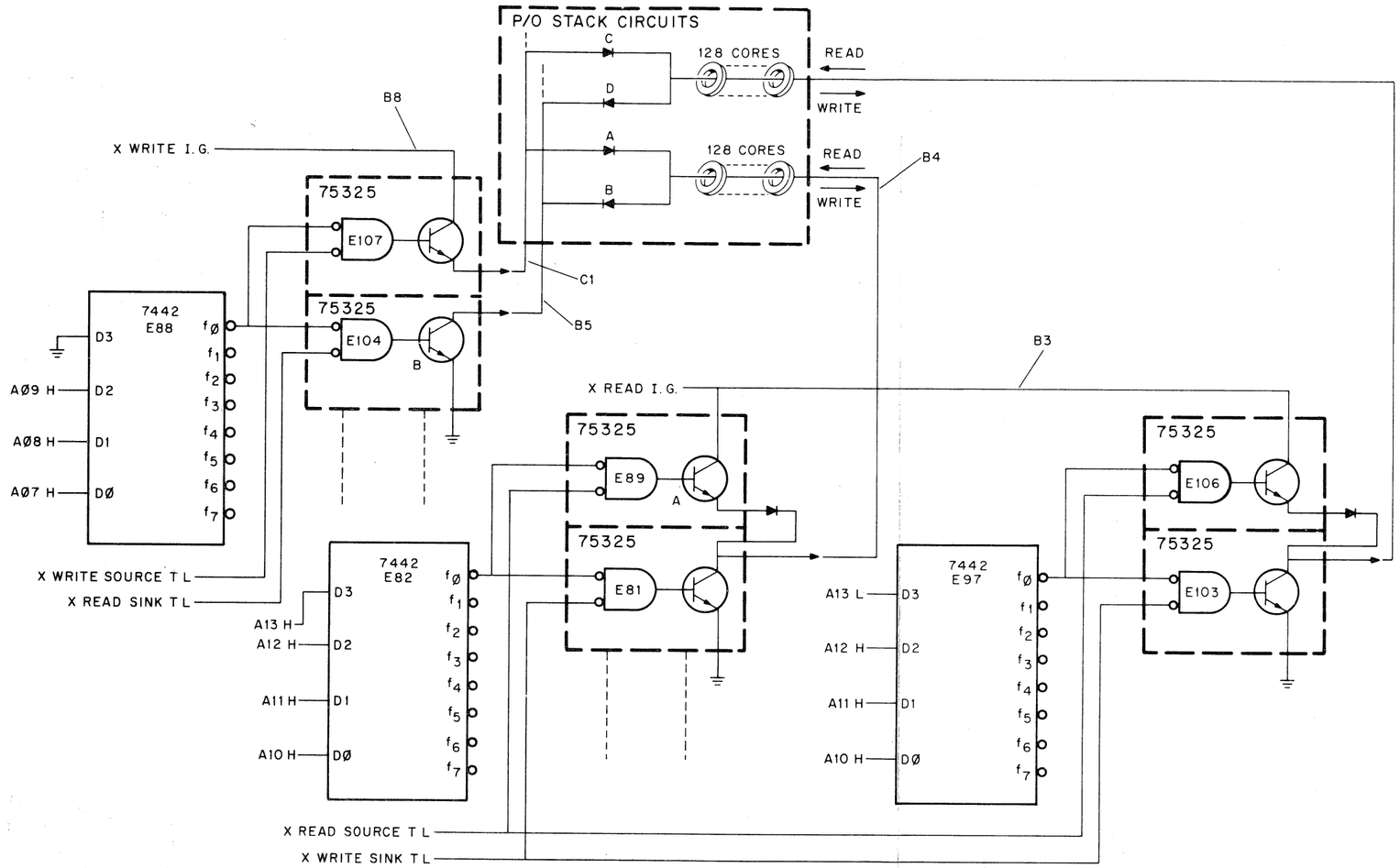


Figure 4-7 Waveform Key C (X-Driver Circuit)

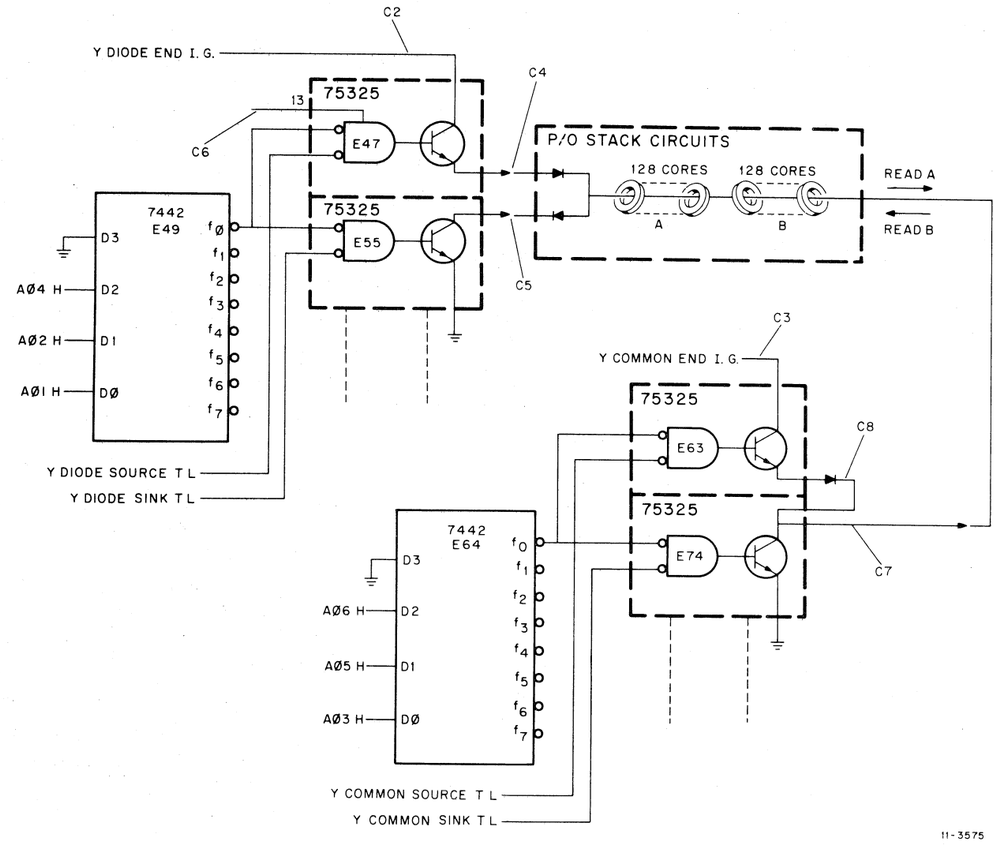


Figure 4-8 Waveform Key D (Y-Driver Circuit)

4.3 MAINDEC TESTING

Certain DEC programs can be used to test various memory operations as an aid to troubleshooting. The purpose of each of these memory-related test programs, as well as the program abstract, is given in the following paragraphs. Each program contains instructions for use.

4.3.1 0-124K Memory Exerciser (MAINDEC-11-DZQMB)

The purpose of the 0–124K Memory Exerciser program is to test contiguous memory addresses from 000000 to 757776. It verifies that each address is unique (address test) and that each memory location can be read or written reliably (worst case noise test). If Memory Management is available, all testing is performed with memory management enabled (unless disabled). This program may be used to adjust/margin memory.

4.3.2 0–124K Memory I/O Exerciser (MAINDEC-11-DZQMA)

The purpose of the 0–124K Memory I/O Exerciser is to test sequentially all locations of core memory, or any 4K section of core memory, using any NPR device specified. The program checks bank selection, effective address bits, and memory. It can run alone or with a Memory Management device to access extended memory. Worst case noise patterns are used with the NPR device to test memory. Printouts of NPR device errors are provided and include designation of the device under test, the content of its control and status register, and the content of its error register. Data error printouts include the address of the bad data, the true data sent, and the bad data received.

4.3.3 Combined Parity Memory Tests (MAINDEC-11-DCMFA)

The purpose of the Combined Parity Memory Tests is to locate the parity memory registers and perform a check of the bits in each. A map showing the memory controlled by each parity register is created by the program. The parity registers and memory are tested using the information in the map.

Several bit patterns are written into each parity memory location to ensure that no parity errors are created. Each byte of parity memory is written with both good and bad parity to ensure that the parity bits can be toggled and sensed.

APPENDIX A
IC DESCRIPTIONS

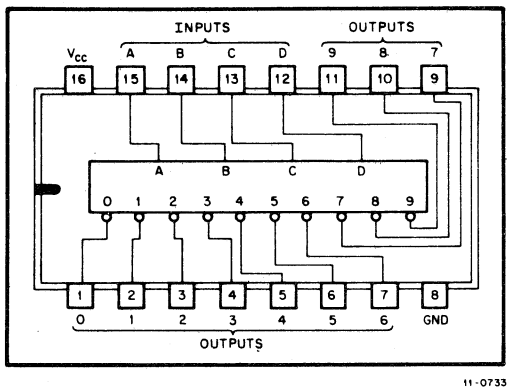
This appendix contains descriptions of several integrated circuits (ICs) used in the MM11-D logic. Only those ICs of an unusual nature are described; the more common types, i.e., NAND gates, inverters, flip-flops, etc., are familiar to the reader.

7442 4-LINE TO 1-LINE DECODER

The 7442 is a BCD-to-decimal decoder consisting of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. A logic diagram, a truth table, and a pin locator are shown in Figure A-1.

TRUTH TABLE

BCD Input					Decimal Output									
D	C	B	A		0	1	2	3	4	5	6	7	8	9
0	0	0	0		0	1	1	1	1	1	1	1	1	1
0	0	0	1		1	0	1	1	1	1	1	1	1	1
0	0	1	0		1	1	0	1	1	1	1	1	1	1
0	0	1	1		1	1	1	0	1	1	1	1	1	1
0	1	0	0		1	1	1	1	0	1	1	1	1	1
0	1	0	1		1	1	1	1	1	0	1	1	1	1
0	1	1	0		1	1	1	1	1	1	0	1	1	1
0	1	1	1		1	1	1	1	1	1	1	0	1	1
1	0	0	0		1	1	1	1	1	1	1	1	0	1
1	0	0	1		1	1	1	1	1	1	1	1	1	0
1	0	1	0		1	1	1	1	1	1	1	1	1	1
1	0	1	1		1	1	1	1	1	1	1	1	1	1
1	1	0	0		1	1	1	1	1	1	1	1	1	1
1	1	0	1		1	1	1	1	1	1	1	1	1	1
1	1	1	0		1	1	1	1	1	1	1	1	1	1
1	1	1	1		1	1	1	1	1	1	1	1	1	1



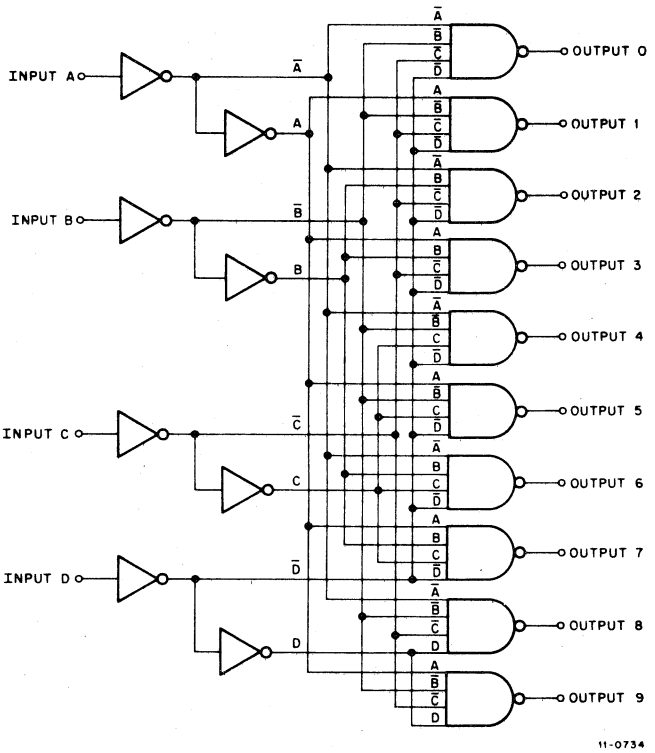
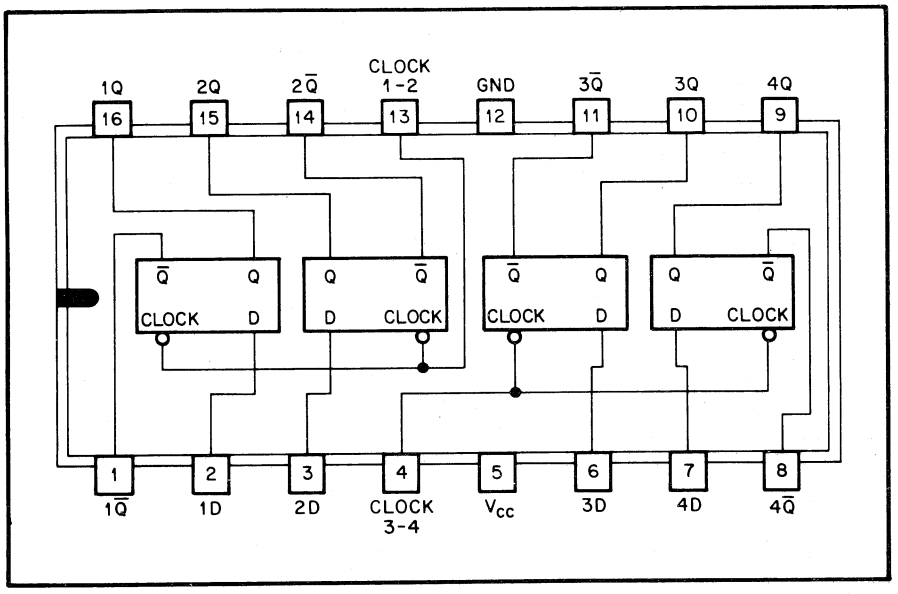


Figure A-1 7442 Illustrations

7475 4-BIT BISTABLE LATCH

The 7475 is used for temporary storage of binary data. Information applied to a Data (D) input is transferred to the Q output when the clock input is high; the Q output follows the D input as long as the clock remains high. When the clock goes low, the information present at the D input prior to the clock transition is retained at the Q output until the clock again goes high. A logic diagram, a circuit diagram, a truth table, and a pin locator are shown in Figure A-2.



IC-7475

Truth Table
(Each Latch)

t_n	t_{n+1}
D	Q
1	1
0	0

NOTES:

1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

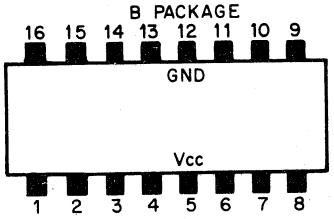
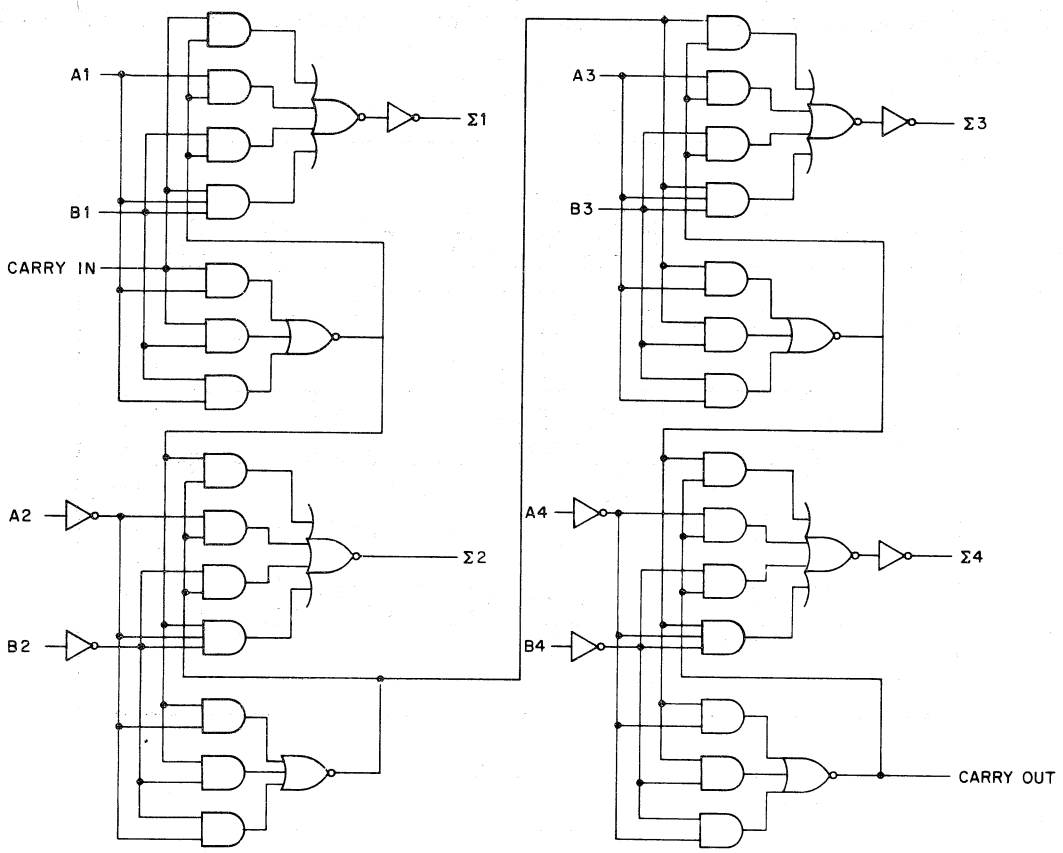


Figure A-2 7475

7483 4-BIT BINARY ADDER

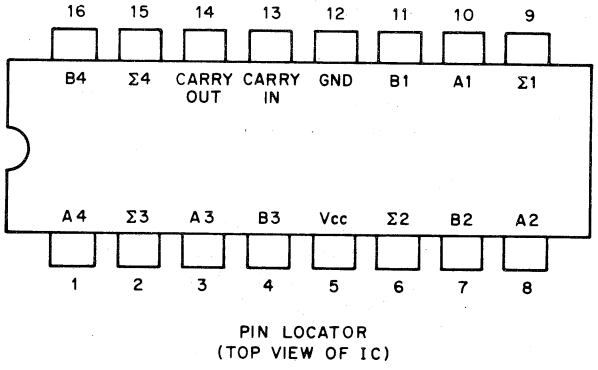
The 7483 adds two 4-bit binary numbers and a carry-in bit. Sum outputs are provided for each bit and a carry-out bit is available from the fourth bit. A logic diagram, a truth table, and a pin locator are shown in Figure A-3.



LOGIC DIAGRAM

INPUT							OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 0$					
						WHEN $C_0 = 1$						WHEN $C_0 = 1$
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4			
0	0	0	0	0	0	0	1	0	0			
1	0	0	0	1	0	0	0	1	0			
0	1	0	0	1	0	0	0	1	0			
1	1	0	0	0	1	0	1	1	0			
0	0	1	0	0	1	0	1	1	0			
1	0	1	0	1	1	0	0	0	1			
0	1	1	0	1	1	0	0	0	1			
1	1	1	0	0	0	1	1	0	1			
0	0	0	1	0	1	0	1	1	0			
1	0	0	1	1	1	0	0	0	1			
0	1	0	1	1	1	0	0	0	1			
1	1	0	1	0	0	1	1	0	1			
0	0	1	1	0	0	1	1	0	1			
1	0	1	1	1	0	1	0	1	1			
0	1	1	1	1	0	1	0	1	1			
1	1	1	1	0	1	1	1	1	1			

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.



PIN LOCATOR
(TOP VIEW OF IC)

IC-7483

Figure A-3 7483

7520 DUAL CORE MEMORY SENSE AMPLIFIER

The 7520 converts bipolar millivolt-level memory sense signals to saturated logic levels. A common reference input allows the input threshold voltage level of both amplifiers to be adjusted. Separate strobe inputs provide time discrimination for each channel. A connection diagram is shown in Figure A-4.

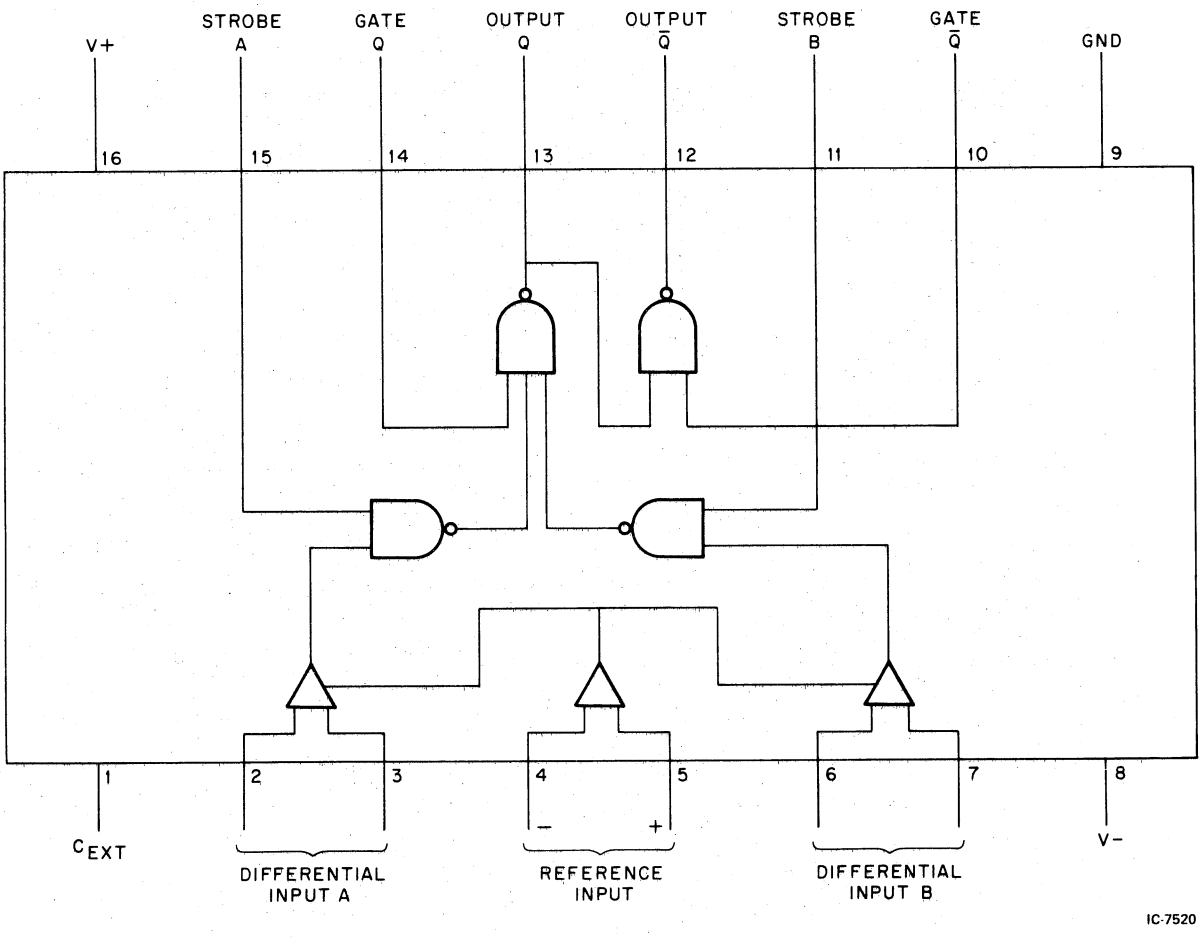


Figure A-4 7520

74121 MONOSTABLE MULTIVIBRATOR

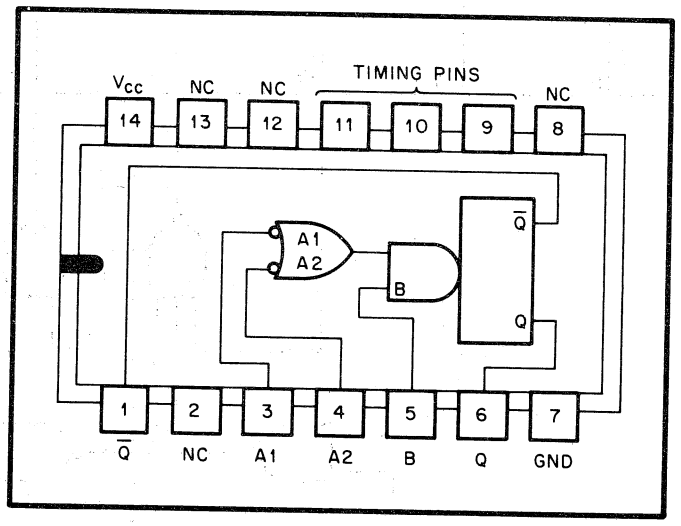
The 74121 Multivibrator features dc triggering from positive-going or gated negative-going inputs. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Once fired, the outputs are independent of the input pulses and depend only on the timing components on the chip. Input pulses may be of any duration relative to the output pulse. A logic diagram/pin locator and a truth table are shown in Figure A-5.

TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	0	1	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

1 = $V_{in(1)} \geq 2V$

0 = $V_{in(0)} \leq 0.8V$



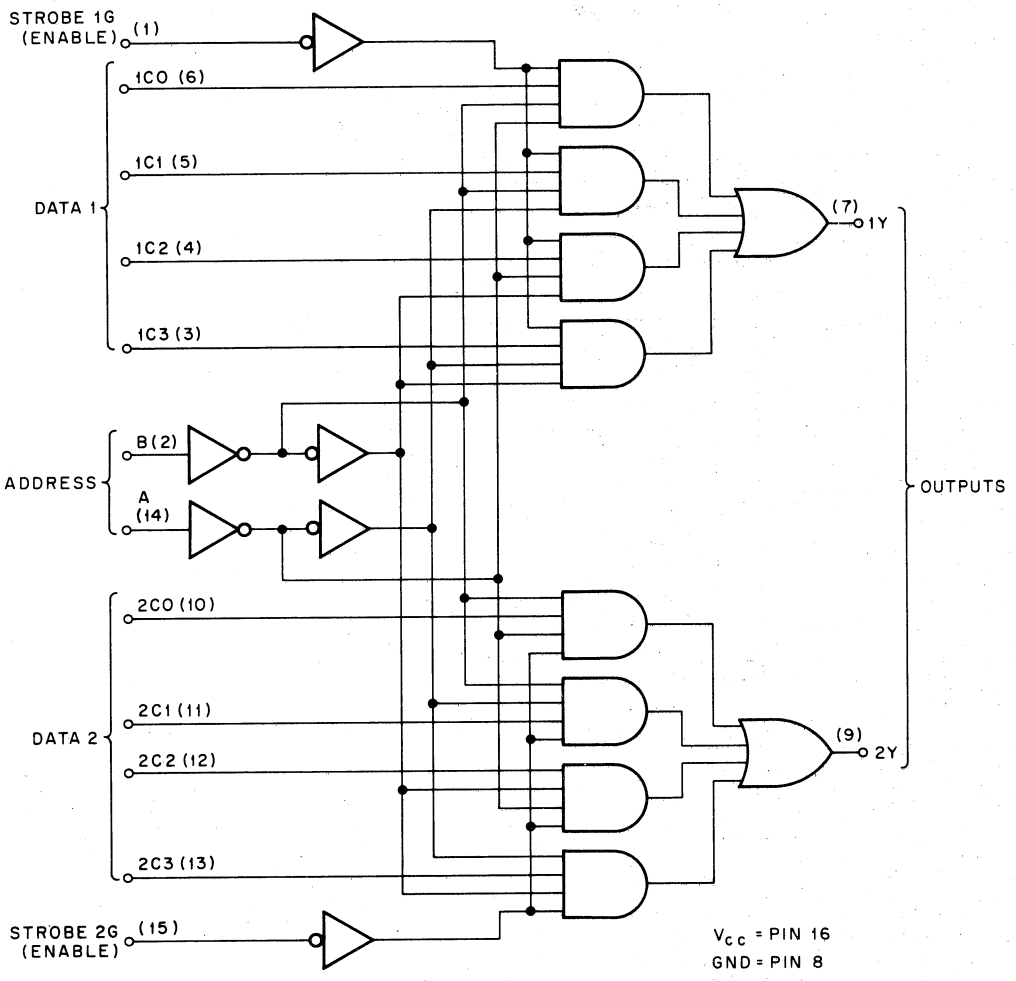
1. t_n = Time before input transition.
2. t_{n+1} = Time after transition.
3. X indicates that either a logical 0 or 1 may be present.

IC-SN74121

Figure A-5 74121

74153 DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

The 74153 acts as a double-pole, four-throw switch. Two select inputs, A and B, determine which of the four inputs is chosen; the same input of both four-line sections is selected. A logic diagram, a truth table, and a pin locator are shown in Figure A-6.



LOGIC DIAGRAM

SELECT INPUT		STROBE	OUTPUT
A	B	G	Y
LOW	LOW	LOW	C0
HIGH	LOW	LOW	C1
LOW	HIGH	LOW	C2
HIGH	HIGH	LOW	C3
DONT CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)

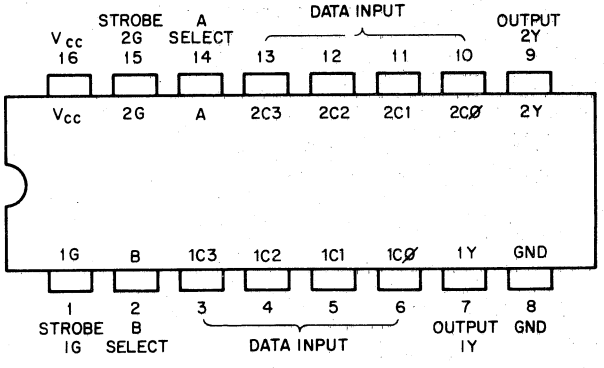
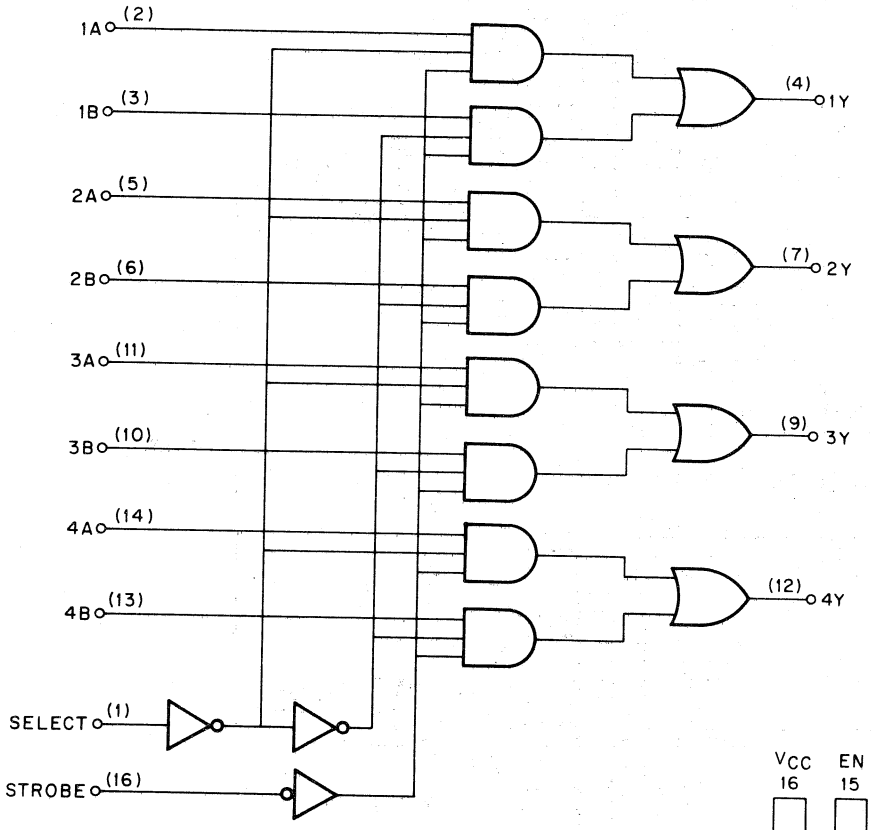


Figure A-6 74153

74157 QUAD 2-INPUT DATA SELECTOR/MULTIPLEXER

The 74157 consists of four 2-input multiplexers with common input select logic and common output disable circuitry. It allows two groups of four bits each to be multiplexed to four parallel outputs. A logic diagram, a truth table, and a pin locator are shown in Figure A-7.

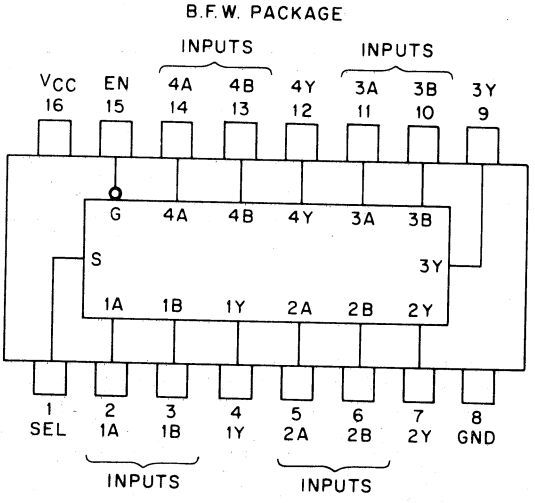
LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

B.F.W. PACKAGE

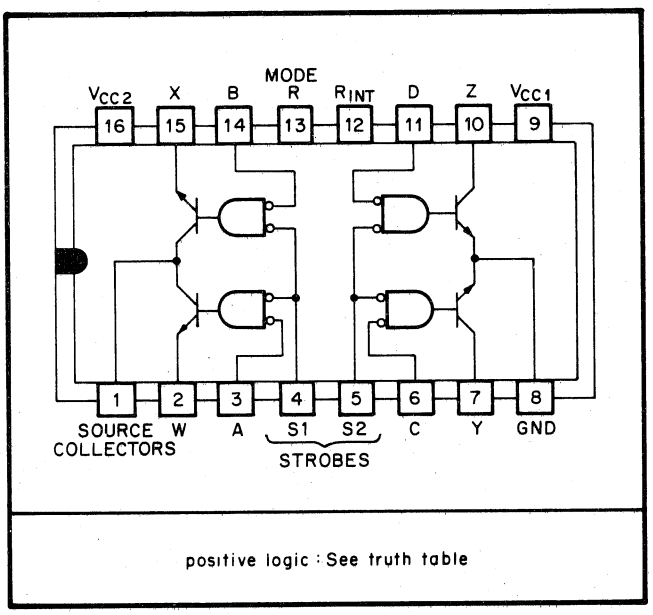


IC-74157

Figure A-7 74157

75325 MEMORY DRIVER

The 75325 contains two source-switch transistors and two sink-switch transistors. Selection logic in the IC permits external control circuits to choose one or more of the switches for circuit operation. A logic diagram/pin locator and a truth table are shown in Figure A-8.



TRUTH TABLE

Address Inputs				Strobe Inputs		Outputs			
Source		Sink		Source	Sink	Source		Sink	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

Reader's Comments

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EK-MM11D-TM-001

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