

pdp11

**MM11-D/DP
core memory
user's manual**

digital

**MM11-D/DP
core memory
user's manual**

Copyright © 1976 by Digital Equipment Corporation

The material in this manual is for informational purposes and is subject to change without notice.

Digital Equipment Corporation assumes no responsibility for any errors which may appear in this manual.

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

The following are trademarks of Digital Equipment Corporation, Maynard, Massachusetts:

DEC	DECtape	PDP
DECCOMM	DECUS	RSTS
DECsystem-10	DIGITAL	TYPESET-8
DECSYSTEM-20	MASSBUS	TYPESET-11
		UNIBUS

CONTENTS

		Page
CHAPTER 1	INTRODUCTION	
1.1	INTRODUCTION	1-1
1.2	GENERAL DESCRIPTION	1-1
1.3	PHYSICAL DESCRIPTION	1-1
CHAPTER 2	INSTALLATION	
2.1	UNPACKING	2-1
2.2	ADDRESS SELECTION	2-1
2.3	BACKPLANE VOLTAGE CHECK	2-3
2.4	MODULE INSERTION	2-5
2.5	CABLE CONNECTION	2-5
2.6	PARITY CONTROLLER	2-5
2.7	DIAGNOSTIC ACCEPTANCE TESTS	2-5
2.7.1	MM11-D/DP Diagnostics	2-5
2.7.2	Memory Exerciser Diagnostic	2-6
2.7.3	DZQMB Diagnostic	2-6

ILLUSTRATIONS

Figure No.	Title	Page
1-1	G652 Module	1-3
1-2	H222 Module	1-4
1-3	MM11-D/DP	1-5
2-1	Address Decoding Logic	2-2

TABLES

Table No.	Title	Page
1-1	MM11-D/DP Specifications	1-2
2-1	Jumper Assignments for MM11-D Starting Addresses	2-3
2-2	Jumper Assignments for MM11-D Starting Addresses (Interleaved-Memory Operation)	2-4
2-3	DD11-F Backplane Pin Assignments	2-4
2-4	Voltage Adjustment Procedure	2-5

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

This manual describes the MM11-D/DP Magnetic Core Memory, manufactured by Digital Equipment Corporation and provides the information needed to install and operate memory.

1.2 GENERAL DESCRIPTION

The MM11-D/DP core memory is a low-cost, low-power, high-reliability memory designed to be used with the PDP-11 family Unibus. It assumes the role of a slave device to the PDP-11 processor or to any peripheral device that is designated bus master. The memory provides storage for 16- or 18-bit data words (two parity bits are included in the 18-bit word), and has a capacity of 16,384 (16K) words. The starting address of the MM11-D/DP can be set on any 8K boundary within the 124K Unibus address space (112K is the highest possible starting address); a special feature of the memory allows the user to assign part of the I/O page (124K-128K) to the MM11-D/DP. Another feature of the MM11-D/DP - interleaving - permits the user to decrease the effective memory cycle time. Two memory modules are used, one being assigned the odd addresses within a 32K block of Unibus addresses, the other being assigned the even addresses within the same block. Thus, for consecutive word addresses, the memories are accessed alternately; hence, memory cycles can partially overlap, reducing the effective cycle time.

1.3 PHYSICAL DESCRIPTION

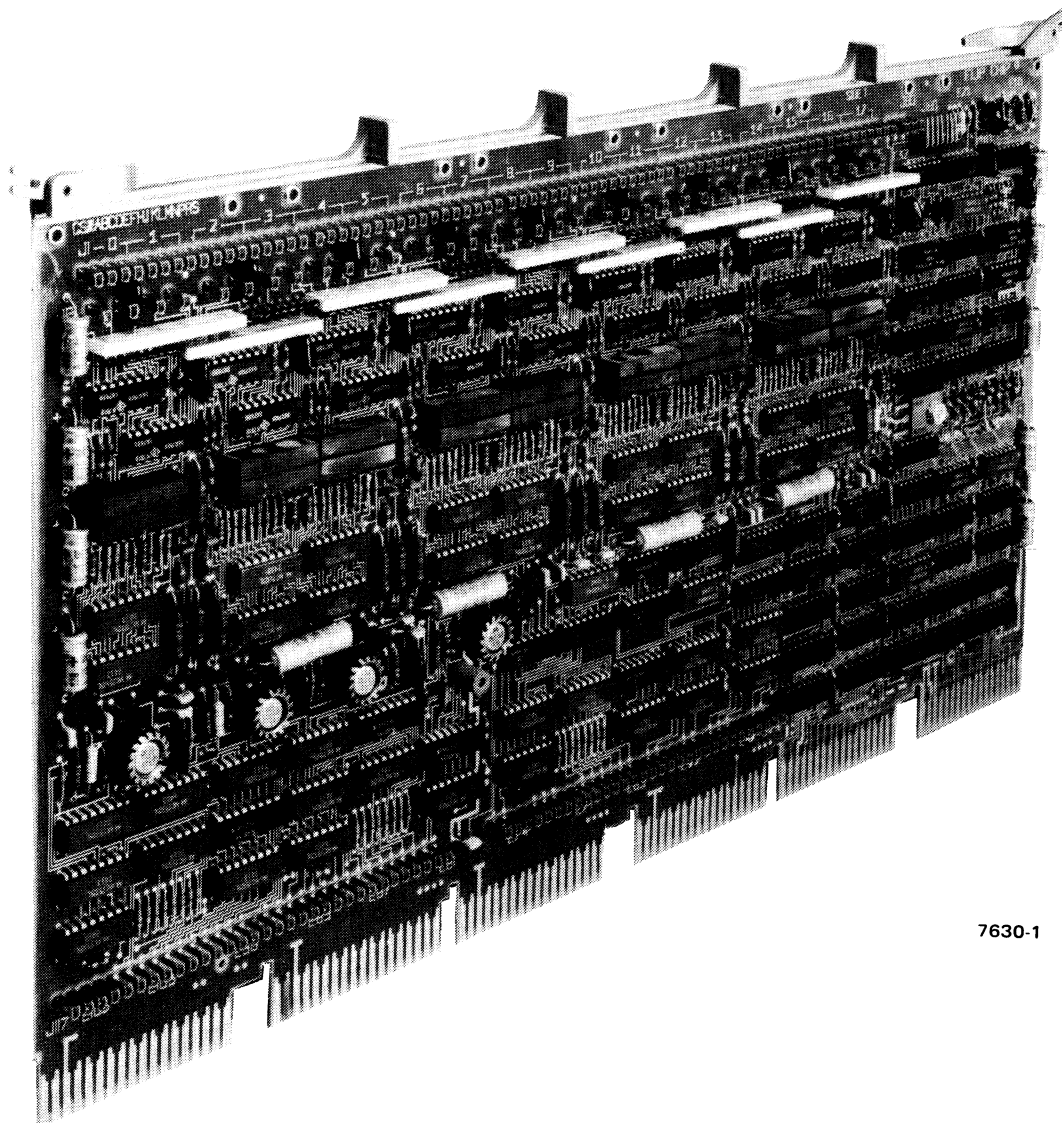
The MM11-D/DP consists of an 8-1/2 in. × 15 in. hex multilayer motherboard (G652) and a hex stack (H222) that is attached to the motherboard. The G652 motherboard is inserted into a Unibus backplane; it contains the Unibus interface logic, the timing and control logic, the X and Y driver circuits, and the sense/inhibit circuits. The H722 stack contains the core plane, stack diodes, stack charge circuits, and temperature-sensing circuitry that facilitates compensation of core driving currents over the operating temperature range. Figures 1-1 and 1-2 show the separate memory modules; Figure 1-3 shows the two modules joined.

A Parity Control module (M7850) is used with the MM11-DP memory and must be inserted into the same backplane as the memory (the MM11-DP can be used as a non-parity memory). Refer to the M7850 Parity Controller maintenance manual for a description of the controller.

**Table 1-1
MM11-D/DP Specifications**

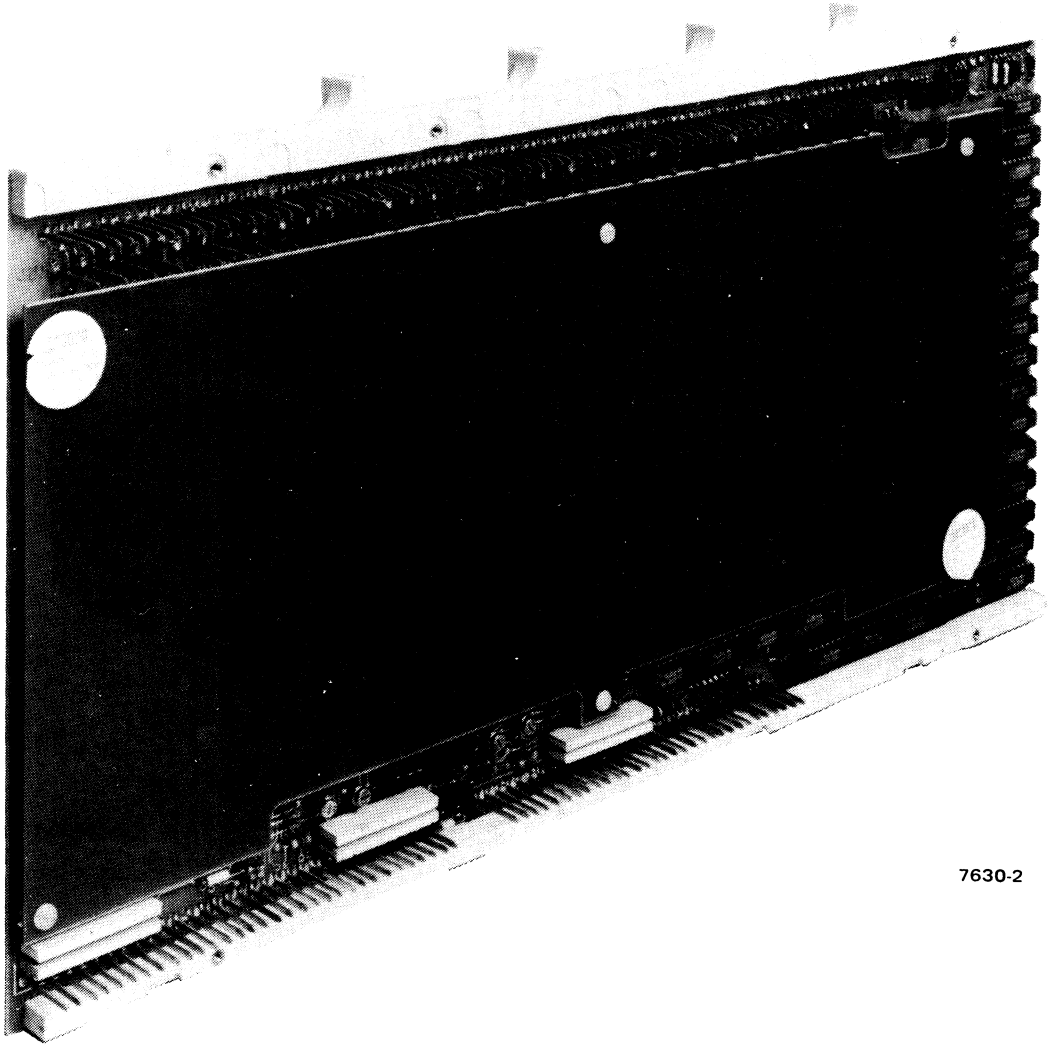
Memory Type	Magnetic core, read/write, random-access		
Core Configuration and Size	Planar, 3W-3D, 18 mil O.D.		
Capacity	MM11-D: 16,384 16-bit words MM11-DP: 16,384 18-bit words (2 byte parity bits)		
Maximum Access Time	MM11-D: 425 ns MM11-DP: 560 ns (when used with a Parity Control module)		
Maximum Cycle Time	MM11-D: 1 μ s MM11-DP: 1 μ s		
Voltage Requirements	+20 Vdc, $\pm 3\%$ +5 Vdc, $\pm 5\%$ -5 Vdc, $\pm 5\%$		
Current Requirements	dc Supply	Active*	Standby
	MM11-D/DP +20 Vdc	4.0 A	0.8 A
	+5 Vdc	4.0 A	4.0 A
	-5 Vdc	0.5 A	0.5 A
Maximum Power Dissipation	dc Supply	Active	Standby
	MM11-D/DP +20 Vdc	80 W	16 W
	+5 Vdc	20 W	20 W
	-5 Vdc	2.5 W	2.5 W
X-Y Current Margins	$\pm 5\%$		
Ambient Temperature Operating Range	In accordance with DEC STD 102, Class C		
Relative Humidity Operating Range	In accordance with DEC STD 102, Class C		

*Active is defined as running all 0s at 1.0 μ s repetition rate (worst case).



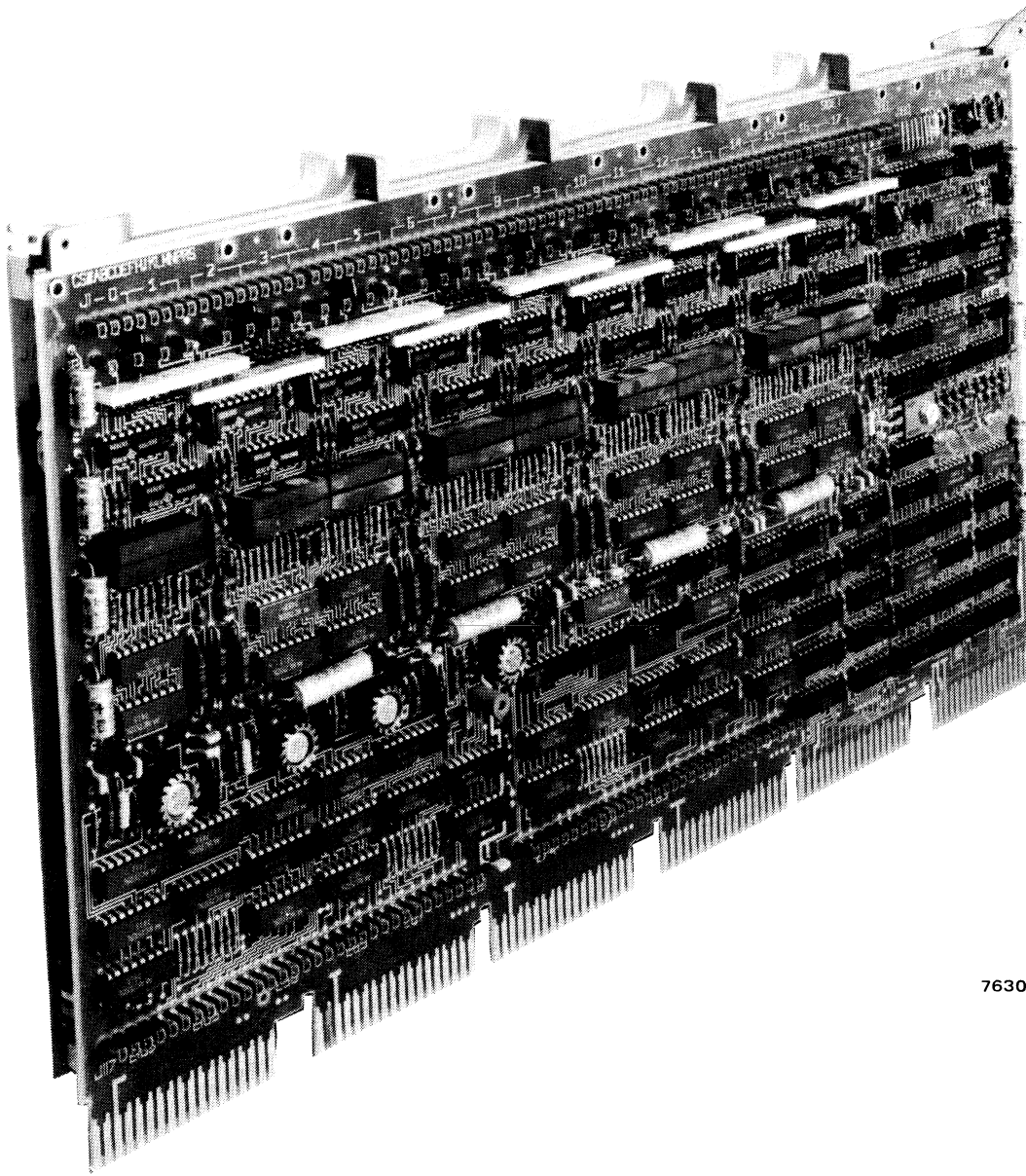
7630-1

Figure 1-1 G652 Module



7630-2

Figure 1-2 H222 Module



7630-3

Figure 1-3 MM11-D/DP

CHAPTER 2 INSTALLATION

The MM11-D/DP installation is simple and straightforward. Follow the steps outlined in Paragraphs 2.1 through 2.7 below.

2.1 UNPACKING

Carefully remove the memory modules from the shipping carton.

2.2 ADDRESS SELECTION

Jumpers W1–W8 on the G652 module are involved in this procedure. The Unibus address space assigned to the MM11-D depends on what address is selected as the MM11 starting address. This starting address can be any one that begins an 8K block of addresses; for example, 000000₈ (0K), 040000₈ (8K), 140000₈ (24K). The starting address is assigned by inserting jumper wires at specified locations in the Address Decoding logic (Figure 2-1). When the starting address appears on the Unibus address bus, the Address Decoding logic asserts the BANK SEL H signal. If both the Unibus and the MM11 timing logic are not busy, the BANK SEL H signal enables BUS MSYN L to start the timing chain.

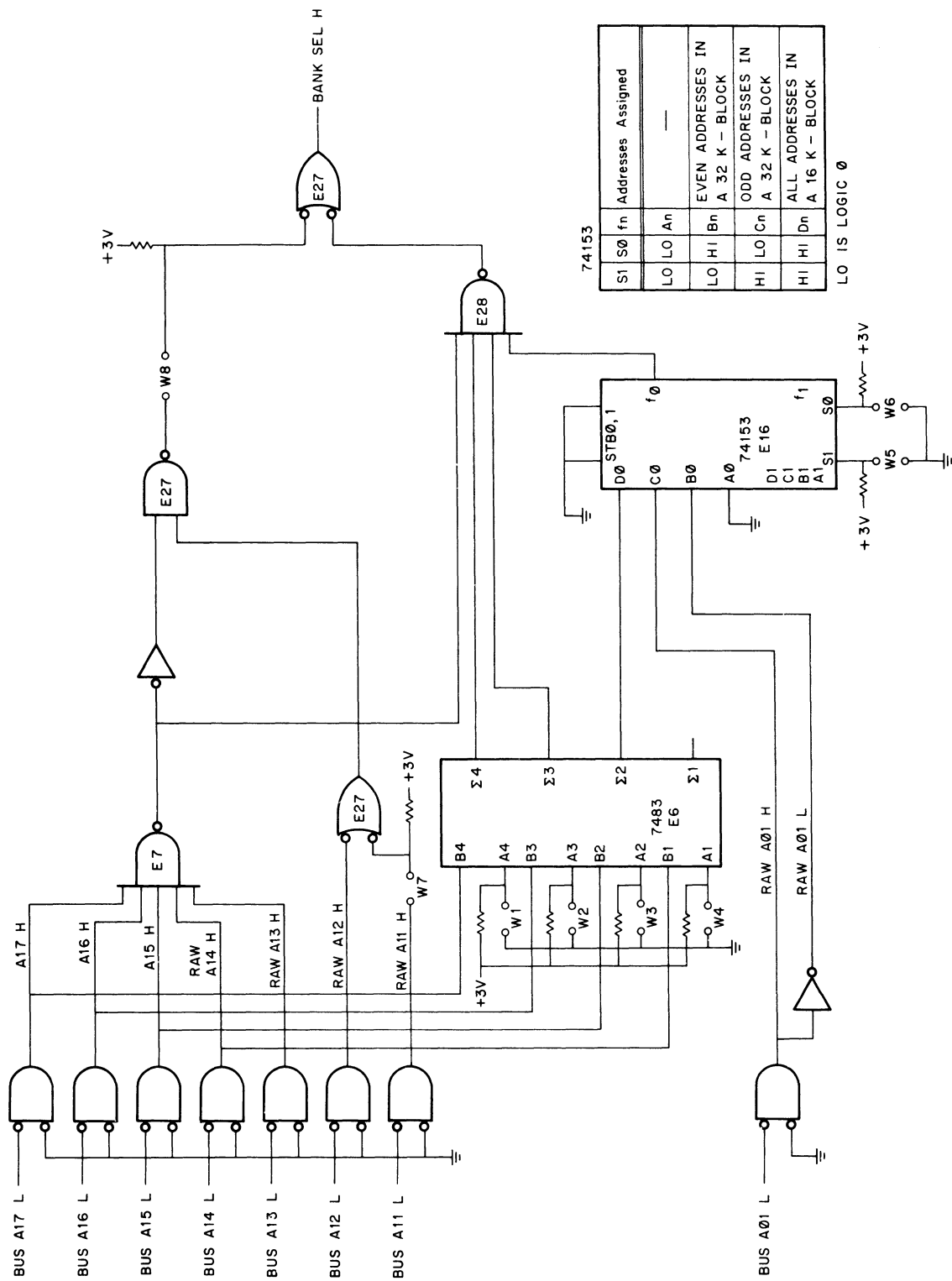
The BANK SEL H signal can be asserted when either NAND gate E27 or E28 is enabled. However, during normal operation, wherein the uppermost 4K of Unibus address space is reserved for peripheral devices, there is no jumper wire installed at location W8; consequently, only NAND gate E28 need be considered. This gate is enabled whenever an address from the assigned 16K block appears on the Unibus address lines. The starting address of this block is determined by the arrangement of jumpers at locations W1–W4. Jumpers are inserted at these four locations in such a way that any assigned address causes the outputs from adder E6 to be high. Two of these outputs, $\Sigma 3$ and $\Sigma 4$, go directly to NAND gate E28. A third, $\Sigma 2$, goes to multiplexer E16; during noninterleaved operation, the $\sigma 2$ output is gated through the multiplexer to NAND gate E28. The fourth input to the gate is from NAND gate E7, which is enabled only for addresses within the 4K reserved area.

Table 2-1 lists the possible starting address for the MM11-D memory, the ending address (plus 1) corresponding to each starting address, and the disposition of jumper wires at locations W1–W4. For example, an MM11-D memory can be assigned address space beginning at address 040000₈ (8K) if a jumper is inserted at location W3. The ending address will be 137777₈ (24K-1). Each address in this 16K block will cause NAND gate E28 to be enabled, resulting in the assertion of BANK SEL H.

As mentioned earlier, in normal operation the upper 4K of memory addresses is reserved for peripheral devices on the Unibus. In special applications, where the number of peripheral devices is small, some of these reserved addresses can be used by the MM11-D. Thus, if a jumper is inserted at location W8, Unibus addresses from 124K to 126K-1 (760000₈ – 767777₈) will cause NAND gate E27 to be enabled and BANK SEL H will be asserted. If a jumper is inserted at W7, in addition to one at W8, addresses from 124K to 127K-1 (760000₈ – 774000₈) will be assigned to the MM11. Note that for systems without Memory Management, the useful address space can be extended from 28K to 30K-1, or 31K-1.

NOTE

If use of the reserved I/O page of addresses is being considered, check carefully to ensure that, first, no peripheral devices (including bootstrap ROM's) are assigned any of the reserved addresses, and second, all DIGITAL software is compatible with the reduced peripheral address space.



74153

SI	S0	fn	Addresses Assigned
LO	LO	An	—
LO	HI	Bn	EVEN ADDRESSES IN A 32 K - BLOCK
HI	LO	Cn	ODD ADDRESSES IN A 32 K - BLOCK
HI	HI	Dn	ALL ADDRESSES IN A 16 K - BLOCK

LO IS LOGIC 0

Figure 2-1 Address Decoding Logic

Table 2-1
Jumper Assignments for MM11-D Starting Addresses

Starting Address	Ending Address +1	W1	W2	W3	W4
0	16K	OUT	OUT	OUT	IN
8K	24K	OUT	OUT	IN	OUT
16K	32K	OUT	OUT	IN	IN
24K	40K	OUT	IN	OUT	OUT
32K	48K	OUT	IN	OUT	IN
40K	56K	OUT	IN	IN	OUT
48K	64K	OUT	IN	IN	IN
56K	72K	IN	OUT	OUT	OUT
64K	80K	IN	OUT	OUT	IN
72K	88K	IN	OUT	IN	OUT
80K	96K	IN	OUT	IN	IN
88K	104K	IN	IN	OUT	OUT
96K	112K	IN	IN	OUT	IN
104K	120K	IN	IN	IN	OUT
112K	124K	IN	IN	IN	IN

Note: OUT = logic 1, IN = logic 0.

Two MM11-D memories can be interleaved, i.e., one memory can be assigned the odd addresses within a 32K block of addresses, while the other can be assigned the even addresses within the same block. Interleaving is accomplished by inserting jumpers at locations W5 and W6 of each memory's Address Decoding logic and assigning each memory the same starting address (the starting address for interleaved memories is assigned differently than is the starting address for a single memory; Table 2-2 relates interleaved starting addresses and the disposition of jumpers at locations W1-W4). For example: to interleave two memories so that they cover Unibus address space from 0K-32K, first insert a jumper at locations W3 and W4 of each memory's Address Decoding logic, thereby setting the starting address at 0K; then, insert jumpers at locations W5 and W6 to assign one memory the even addresses (W5 in, W6 out) and the other memory the odd addresses (W5 out, W6 in). Any address in the assigned 32K block causes adder outputs $\Sigma 3$ and $\Sigma 4$ to be high. However, the $\Sigma 2$ output is not gated through multiplexer E16 to NAND gate E28; instead, the f0 output of the multiplexer represents the state of the BUS A01 L signal. Thus, an odd address (BUS A01 L is asserted) causes f0 of the odd-address-memory multiplexer to be high; BANK SEL H is asserted by this memory. Alternately, an even address (BUS A01 L is negated) causes f0 of the even-address-memory multiplexer to be high and BANK SEL H is asserted by this memory.

2.3 BACKPLANE VOLTAGE CHECK

Check the backplane assembly to ensure that the correct dc voltages are present (Table 2-3 lists the DD11-F "modified Unibus" backplane pins and the signal available on each pin). The voltages and their limits are listed below; if they must be adjusted, use the procedure shown in table 2-4.

Voltage (dc)	Backplane Pin
+20 Vdc $\pm 3\%$	A1U, A1V, A2V
+5 Vdc $\pm 5\%$	A2A, B2A, C2A, D2A, F2A
-5 Vdc $\pm 5\%$	B2V

Table 2-2
Jumper Assignments for MM11-D Starting Addresses
(Interleaved-Memory Operation)

Starting Address	Ending Address +1	W1	W2	W3	W4
0	32K	OUT	OUT	IN	IN
8K	40K	OUT	IN	OUT	OUT
16K	48K	OUT	IN	OUT	IN
24K	56K	OUT	IN	IN	OUT
32K	64K	OUT	IN	IN	IN
40K	72K	IN	OUT	OUT	OUT
48K	80K	IN	OUT	OUT	IN
56K	88K	IN	OUT	IN	OUT
64K	96K	IN	OUT	IN	IN
72K	104K	IN	IN	OUT	OUT
80K	112K	IN	IN	OUT	IN
88K	120K	IN	IN	IN	OUT
96K	124K	IN	IN	IN	IN

Table 2-3
DD11-F Backplane Pin Assignments

A		B		C		D		E		F		
1	2	1	2	1	2	1	2	1	2	1	2	
A	INIT L	+5 V	DATIP CLR PAUSE L	+5 V	--	+5 V	--	+5 V	--	--	--	--
B	INTR L	T.P.	--	T.P.	--	--	--	--	--	--	--	--
C	D00 L	GND	BR5 L	GND	--	GND	--	GND	--	GND	--	GND
D	D02 L	D01 L	BATTERY +5	BR4 L	--	--	--	--	--	--	--	--
E	D04 L	D03 L	INT SSYN L	PARITY DETECT L	STACK VREF	--	--	--	--	--	--	--
F	D06 L	D05 L	ACLO L	DCLO L	--	--	--	--	--	--	--	--
H	D08 L	D07 L	A01 L	A00 L	--	--	--	--	--	--	--	--
J	D10 L	D09 L	A03 L	A02 L	--	--	--	--	--	--	--	--
K	D12 L	D11 L	A05 L	A04 L	--	--	--	BUS G7 SO H	--	--	--	--
L	D14 L	D13 L	A07 L	A06 L	--	--	--	BUS G7 OUT H	--	--	--	--
M	PA L	D15 L	A09 L	A08 L	--	--	--	BUS G6 SO H	--	--	--	--
N	PARITY PI L	PBL	A11 L	A10 L	--	--	--	BUS G6 OUT H	--	--	--	--
P	PARITY PO L	BBSY L	A13 L	A12 L	--	--	--	BUS G5 SO H	--	--	--	--
R	--	SACK L	A15 L	A14 L	--	--	--	BUS G5 OUT H	--	--	--	--
S	--	NPR L	A17 L	A16 L	--	--	--	BUS G4 SO H	--	--	--	--
T	GND	BR7 L	GND	C1 L	GND	--	GND	BUS G4 OUT H	GND	--	GND	--
U	+20 V	BR6 L	SSYN L	C0 L	--	--	--	--	--	--	--	--
V	+20 V	+20 V	MSYN L	-5 V	--	--	--	--	--	--	--	--

Table 2-4
Voltage Adjustment Procedure

NOTE
The following steps must be performed sequentially.

Step No.	Procedure
1.	Power down the equipment.
2.	Disconnect the load from the power supply.
3.	Power up the equipment.
4.	Connect the digital voltmeter to the +20 V and -5 V outputs of the power supply.
5.	Adjust the +20 V potentiometer for a 25 V reading.
6.	Connect the digital voltmeter between the -5 V output and ground.
7.	Adjust the -5 V potentiometer for -5 V. This procedure is necessary because the +20 V potentiometer sets the overall output of the regulator (25 V from +20 V to -5 V) while the -5 V adjustment controls the -5 V to ground output.
8.	Power down and then reconnect the load.
9.	Power up, recheck the voltages at the option backplane, and if necessary, adjust the outputs again.

2.4 MODULE INSERTION

Ensure that the H222 module is firmly attached to the G652 module. Insert the G652 into the DD11-F backplane; any one of slots 2-7 can be used. If a parity controller is used, it can be inserted in connectors A and B in any of slots 2-8 (parity and non-parity memory cannot be mixed on the same backplane).

2.5 CABLE CONNECTION

Connect the BC11-A Unibus cable to the memory. If this is the last device on the bus, terminate the Unibus by placing a 9302 terminator in the BUS OUT slot. If the memory is not the last device, continue the bus by placing an M920 jumper module or the BC11-A cable connector in the BUS OUT slot.

2.6 PARITY CONTROLLER

If the system uses an M7850 Parity Controller, refer to the controller manual for information concerning the installation and adjustment of the M7850 module.

2.7 DIAGNOSTIC ACCEPTANCE TESTS

2.7.1 MM11-D/DP Diagnostics

Load and run the MM11-D/DP diagnostic programs. Verify that the program printout agrees with the total memory in the system.

2.7.2 Memory Exerciser Diagnostic

Connect the Unibus Voltage Margin Tester to the memory at connector J180 on the G652 module. Run two passes of the 0-124K Memory Exerciser Diagnostic (MAINDEC-11-DZQMB) with the margin tester switches set at each of the four possible "on" positions:

XY CURRENT HIGH – allows high (+5%) memory drive current;
XY CURRENT LOW – allows low (-5%) memory drive current;
STROBE EARLY – allows an early sense strobe (-15 ns);
STROBE LATE – allows a late sense strobe (+15 ns).

NOTE

**Only margin the memory with one parameter at a time.
Even good memories may fail under some combinations of
drive and strobe margins.**

2.7.3 DZQMB Diagnostic

Disconnect the margin tester. Run the DZQMB diagnostic to verify normal operation.

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

What features are most useful? _____

What faults do you find with the manual? _____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

Would you please indicate any factual errors you have found. _____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

CUT OUT ON DOTTED LINE

digital

digital equipment corporation