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KY11-LB programmer's console/interface module operation and maintenance manual

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KY11-LB programmer's console/interface module operation and maintenance manual

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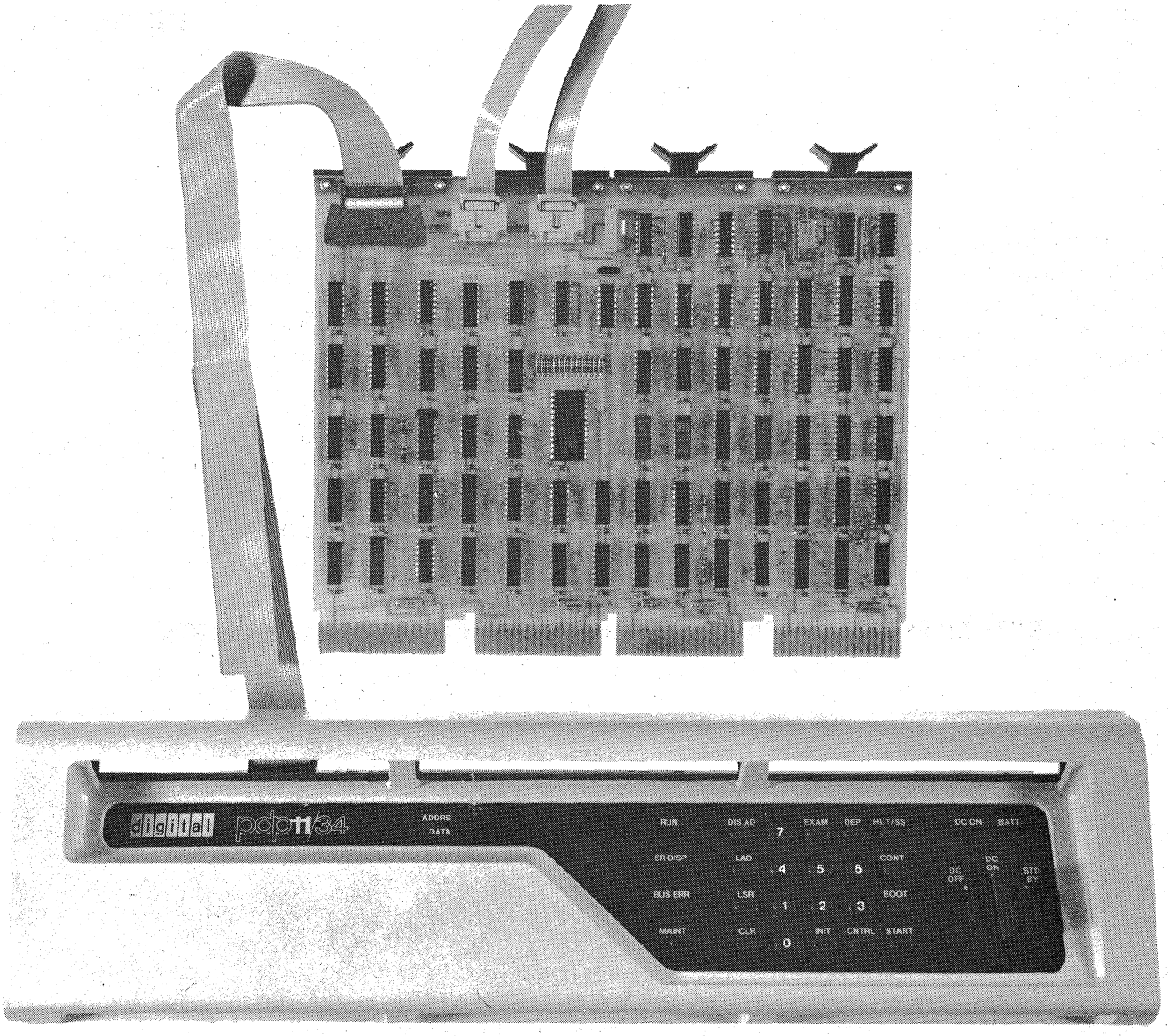
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PREFACE

The *KY11-LB Programmer's Console/Interface Module Operation and Maintenance Manual* provides the information required to operate this option in console or maintenance mode. The manual also presents a detailed theory of operation of the interface module hardware and software components, data on the utilization of the programmer's console as a maintenance tool for the PDP-11/04/34 processors, and information on the troubleshooting and maintenance of the interface module itself. The information is presented in nine chapters:

Chapter 1	Provides an inroduction, general description, and overview of electrical and mechanical specifications.
Chapter 2	Presents a functional description of the console, operating modes, controls and indicators, and a general discussion of interface module hardware organization and software facilities.
Chapter 3	Describes, on a detailed block diagram level, interface module functions, registers and controls, and the functions of the MOS/LSI microprocessor.
Chapter 4	Describes the microprocessor instruction set.
Chapter 5	Presents a description of the M7859 Interface module to the logic level.
Chapter 6	Provides operating information on console utilization in console mode.
Chapter 7	Contains procedures for using the console in maintenance mode (maintenance of PDP-11/04/34 processor).
Chapter 8	Covers some maintenance techniques for the KY11-LB interface module.
Chapter 9	Describes installation procedures for various options.

NOTES

In the material presented in this manual, the term "processor" refers to the KD11-D, KD11-E, and KD11-EA PDP-11/04/34 processors.

If the operator is not familiar with console functions, Chapter 6 should be consulted.

CHAPTER 1
OPERATING CHARACTERISTICS

1.1 INTRODUCTION

The PDP-11/04/34 Programmer's Console and Interface module (KY11-LB) provides all the functions now offered with the PDP-11/05. The Programmer's console interfaces to the Unibus (Figure 1-1) through a quad SPC module. To use this option, the normally provided KY11-LA Programmer's Console must be removed and the KY11-LB Console installed in its place. The KY11-LB Console contains a 7-segment LED display and a 20-key keypad for generating the console commands. Several indicators are also provided for additional convenience in monitoring system status.

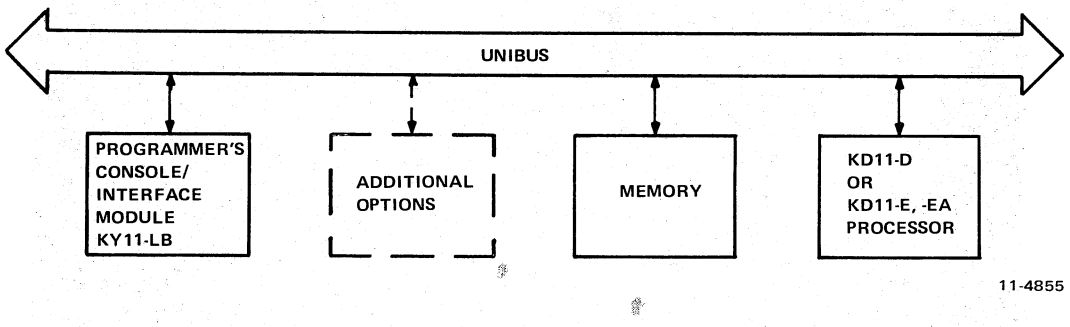

Figure 1-1 Programmer's Console/Interface – PDP-11/04/34 Configuration

The KY11-LB Programmer's Console/Interface module comprises an INTEL 8008 single-chip, large scale integration (LSI) microprocessor and associated registers, Unibus control logic, and auxiliary memory. The unit is also provided with a 20-key keypad for operator/programmer interaction with the KD11-D, -E, -EA via the interface module, six indicator LEDs, a 6-digit, 7-segment display for address or data, and a dc power switch. The microprocessor communicates with a read-only memory (ROM) which contains a number of fixed routines for use during normal console and maintenance operation.

1.2 GENERAL DESCRIPTION

The M7859 Interface module (Figure 1-2) functions as the interface between the programmer's console and the KD11-D, KD11-E, or KD11-EA processor, via the Unibus. The unit consists of solid state integrated circuits with TTL-compatible input and output lines. The heart of the interface module is a single-chip, large scale integration (LSI) microprocessor which executes designated keyboard functions via programs stored in ROM memory. Auxiliary logic functions including clock, decoding and timing circuitry, and addressing and Unibus drivers/receivers comprise the remaining logic of the board.

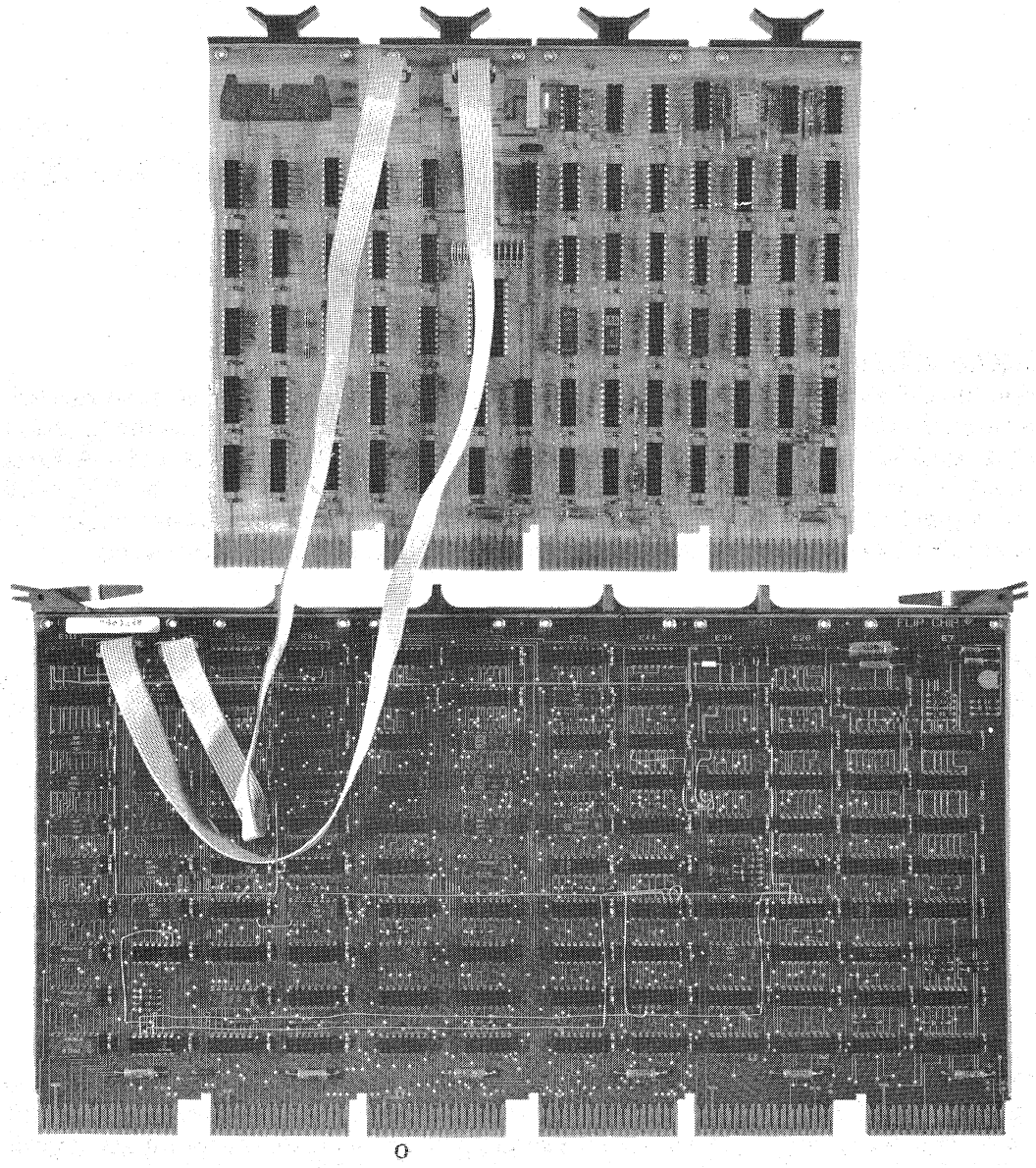

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Figure 1-2 Interface Module (M7859)

The microprocessor chip is an 8-bit, parallel control element packaged as a single metal oxide silicon circuit in an 18-pin, dual in-line package. With the addition of external clock driving circuitry and decoding elements, plus memory and data bus control, the unit is capable of performing as a powerful, general-purpose, central processing unit. Internal logic of the microprocessor chip is structured around an 8-bit internal data bus and includes instruction decoding, memory control, accumulator and scratchpad memory, arithmetic and logical capability, program stack, and condition code indicators. Data transfer between the microprocessor chip and the remaining logic functions of the interface module is accomplished through an 8-bit, bidirectional data port which is an integral part of the microprocessor. An internal stack (scratchpad memory) contains a 14-bit program counter (PC) and an additional complement of seven 14-bit registers for nesting up to seven levels of subroutines. The 14-bit addressing capacity allows the microprocessor to access up to 16K memory locations which may comprise any mix of ROM or RAM.

1.3 FUNCTIONAL DESCRIPTION

The KY11-LB Programmer's Console permits the implementation of a variety of functions through a 20-key keypad located on the front panel of the programmer's console. Keypad functions are divided into two distinct modes: console mode and maintenance mode. In console mode operation, a number of facilities exist for displaying addresses and data, for depositing data in and examining the content of Unibus addresses including processor registers for entering data into a temporary buffer for use as address or data, and for single instruction stepping the processor. The latter feature is especially useful during program debugging functions.

Normal console keyboard functions are not available during maintenance mode. This mode permits sampling and display of the Unibus address lines and Unibus data lines, and may allow the console to take control of the Unibus to examine and deposit Unibus addresses if a processor is not present in the system or is malfunctioning. Additionally, the maintenance function permits assertion of the manual clock enable and display of the current processor microprogram counter (MPC). Single-clock cycling of the MPC is also possible to facilitate step by step checkout of processor op codes and control logic during maintenance functions. In conjunction with this function, assertion of manual clock enable permits the processor to be stepped through its power-up routine. The manual clock enable may be dropped via the START key at any time with a resulting dislay of the current MPC. Exit from maintenance mode to console mode may be accomplished at any time by depressing the CLR key on the keypad.

1.4 SPECIFICATIONS

1.4.1 M7859 Interface Module Performance Specifications

Operating Speed at 500 kHz	
Two-Phase Clock Period	2 μs
Time State (SYNC)	4 μs
Instruction Time (Microprocessor)	12–44 μs
Word Size	
Data	8-bit word
Instruction	1, 2, or 3 8-bit words
Address	14 bits
Memory Size	
ROM	4 512 × 4 organized as 1024 8-bit words
RAM	16 words by 8 bits

Input/Output Lines	
Memory Data	16 bits
Address	18 bits
Control (Address)	2 bits
Unibus Control	5 bits
Microprocessor Instruction Repertoire	
48 Basic Instructions	
Instruction Categories	Register Operation Accumulator PC and Stack Control I/O Machine

1.4.2 Electrical Specifications

Power Supply	+5 V at 3.0 A −15 V at 60 mA
Input Logic Levels (all modules)	
TTL Logic Low	0.0 to 0.8 Vdc
TTL Logic High	2.0 to 3.6 Vdc
Output Logic Levels (all modules)	
TTL Logic Low	0.0 to 0.4 Vdc
TTL Logic High	2.4 to 3.6 Vdc
Power Consumption	
Interface Module	14 W
Monitor/Control Panel	1 W

1.4.3 Mechanical Specifications

M7859 Interface Module	
Board Type	Quad SPC
Dimensions	
Height	21.44 cm (8.44 in)
Length	26.08 cm (10.44 in)
Programmer's Console (Overall Panel Dimensions)	
Width	47.63 cm (18.75 in)
Height	13.02 cm (5.125 in)
Depth	6.76 cm (2.66 in)

1.4.4 Environmental Specifications

Ambient Operating Temperature	5° to 50° C (41° to 122° F)
Humidity	10% to 95% maximum, wet bulb 32° C (90° F)

CHAPTER 2
FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

Logical organization of the KY11-LB Interface module is centered around a microprocessor and a bidirectional data bus (Figure 2-1). The 8-bit data and address bus (D0–D7) is time multiplexed to permit control signals, 14-bit addresses, and data to be transmitted between the microprocessor, memory, and additional buffer registers. Two registers, the switch register and the bus address register, contain data and addresses (respectively) to be routed to the Unibus. The transceivers permit 16-bit data words to be loaded into the microprocessor from the Unibus via the 2-way data bus. Data flow depends on the type of operation indicated by the keypad and the instruction the microprocessor is executing at a given time.

In a typical operation involving an instruction fetch, for example, the microprocessor program counter contents are transferred to the address register in two successive 8-bit bytes. The address register outputs activate the appropriate ROM location containing the instruction. The instruction is routed back via the tristate transceivers and the bidirectional bus to the microprocessor for decoding and subsequent execution. Instructions range from one to three bytes in length; the state counter decoding is capable of discriminating between the op code types and the resulting instruction length. The microprocessor is driven by a nominal 500-kHz, symmetrical, two-phase, nonoverlapping clock and is capable of responding to externally generated interrupt conditions. The data interface is a bidirectional 8-bit bus and the unit also provides four control outputs which include three state control signals and a sync signal. The control signals are applied to external decoding logic to generate system timing states and are subsequently distributed to the remaining interface module control circuitry. The state control signals are also utilized in the chip for sequencing data processing operations.

2.2 PROGRAMMER'S CONSOLE KEYPAD FUNCTIONS/CONTROLS AND INDICATORS

Operator/programmer control of the KY11-LB is accomplished through a 20-key keypad located on the console panel (Figure 2-2). A summarized description of the key functions and other controls and indicators is contained in Table 2-1. The table first presents those functions involved in console mode which are primarily of interest to the programmer. A second portion of the table describes entry into maintenance mode and presents facilities useful for processor checkout and maintenance. The CNTRL key functions primarily as an interlock which prevents accidental inerference with other console operations.

2.2.1 Console Mode

Detailed presentation of console mode keypad functions and their use in program debugging is reserved for a later chapter; the various functions are outlined and briefly described in Table 2-1. The operator indicators available for both modes are also described. Upon power-up, the programmer's console is in console mode. If in maintenance mode, pressing the CLR key causes a reversion to console mode through a HALT.

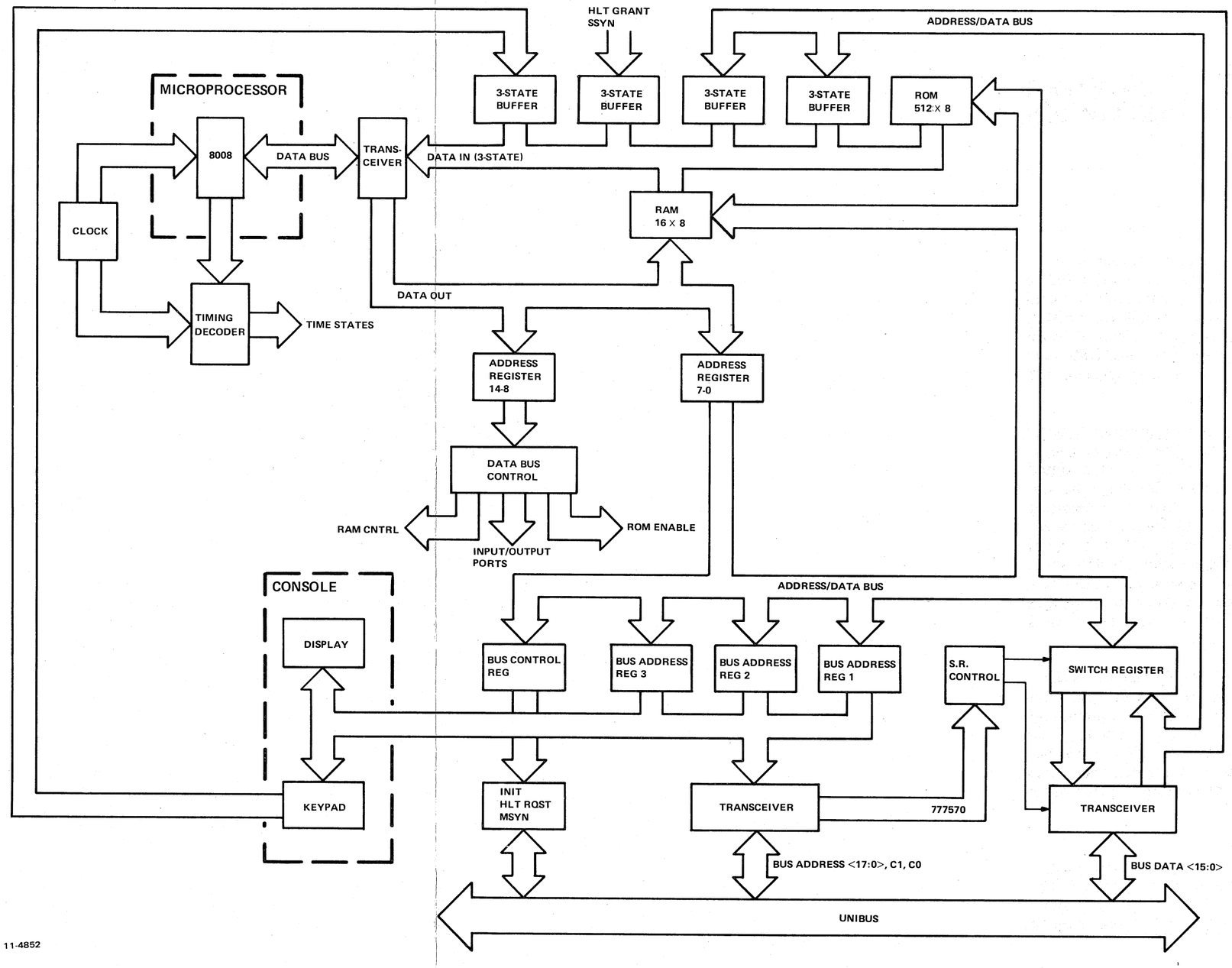

Figure 2-1 KY11-LB Logical Organization

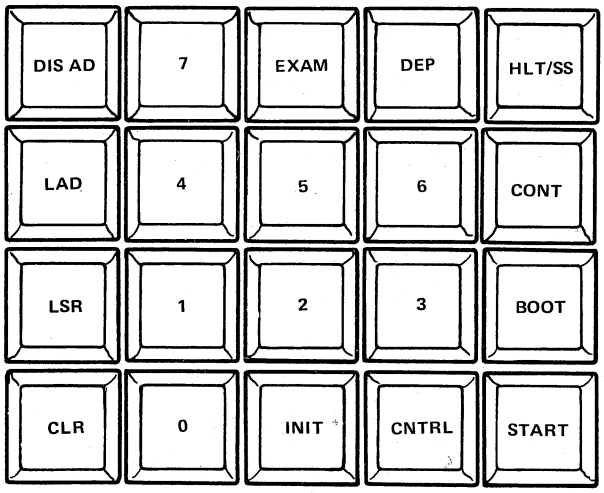

Figure 2-2 KY11-LB Keypad

Table 2-1 KY11-LB Controls and Indicators

Control/Indicator	Function
	Keyboard – Console Mode
LAD	Load Address – Moves the 18-bit number in the temporary register into the Unibus address pointer. The temporary register is then cleared and displayed.
LSR	Load Switch Register – Moves the 16 lower bits of the temporary register to a register which can be read via Unibus address 777570. The switch register contents will be displayed.
DEP	Deposit – Causes the console to do a DATO on the bus address pointed to, using the data in the temporary register (two MSBs are truncated). Sequential deposits cause the address pointer to be incremented. This key is operative only if the processor is halted.
0–7	Numerics – These keys are used to enter data into a temporary data buffer prior to use as either address or data. Use of a numeric key forces the console to display the data held in the temporary buffer. A 6-digit number is generated as octal digits are entered from the right and left shifted.
CNTRL	Control – This key is used only in conjunction with other keys either to prevent accidental operation of certain functions or to provide entry into maintenance mode or other features. When used, the CNTRL key must be pressed first and held down while the second key is pressed. Those keys which are interlocked with the CNTRL key are indicated by "CNTRL-second key" (e.g., CNTRL-START).

Table 2-1 KY11-LB Controls and Indicators (Cont)

Control/Indicator	Function
CNTRL-INIT	Initialize – Operative only if the processor is halted. Causes BUS INIT L to be generated for 150 ms.
DIS AD	Display Address – This key causes the current Unibus address pointer to be displayed. The next examine or deposit will occur at the address displayed.
EXAM	Examine – Causes the console to do a DATI on the bus address pointed to and stores the data in the temporary register which is then displayed. Sequential examines cause the address pointer to be incremented by 2 or by 1 if the address is in the range 777700–777717. This key is operative only if the processor is halted.
CLR	Clear Entry – Clears the current contents of the temporary register which is then displayed.
CNTRL-BOOT	Causes M9301 bootstrap terminator to be activated if present in the system. Console will boot only if the processor is halted.
CNRL-HALT/SS	Halt/Single Step – Halts the processor if the processor is running. If the processor is already halted it will single-instruction step the processor. It also retrieves and displays the contents of R7 (program counter). The CNTRL key is not required to Single-Instruction Step the machine.
CNTRL-CONT	Continue – Allows processor to continue using its current program counter from a halted state. The contents of the switch register are displayed.
CNTRL-START	Operative only if halted, this causes the program counter (R7) to be loaded with the contents of the Unibus address pointer. BUS INIT L is then generated and the processor is allowed to run. Switch register contents are then displayed.
CNTRL-7	Causes the Unibus address pointer to be added to the temporary data buffer which is also incremented by 2. This allows the console to calculate the correct offset address when mode 6 or 7, register 7 PIC (Position Independent Code) instructions are encountered.
CNTRL-6	This causes the switch register to be added to the temporary data buffer. This is useful when mode 6 or 7 instructions are encountered not using R7.
CNTRL-1	Maintenance Mode – This combination puts the console into maintenance mode with certain maintenance features available. When the console is in maintenance mode, the normal console mode keypad functions are not available. The CLR key causes the console to exit from maintenance mode into console mode via a processor halt.

Table 2-1 KY11-LB Controls and Indicators (Cont)

Control/Indicator	Function
Keyboard – Maintenance Mode	
	NOTE **In maintenance mode the keypad functions are redefined with the following definitions.**
DIS AD	Causes the Unibus address lines to be sampled and displayed.
CLR	Returns the console to console mode via a console halt.
EXAM	Causes the console to sample the Unibus data lines and display the data.
5	Causes the console to take control of the Unibus. Should be used only when a processor is not present in the system.
HLT/SS	Asserts manual clock enable and displays the current microprogram counter (MPC).
CONT	Asserts manual clock enable, generates a manual clock pulse, and displays the current MPC.
BOOT	Boots the M9301. If manual clock enable is asserted, this will allow the processor to be stepped through the power-up routine.
START	Drops manual clock enable and displays the current MPC.
Indicator LEDs – Any Mode	
DC ON	All dc power (+5 V) to logic is on.
BATT	Battery monitor indicator, operative only in machines having the battery back-up option. This indicator has four states: Off – Indicates either no battery present or battery failure if a battery is present. On (continuous) – Indicates that a battery is present and charged. Flashing (slow) – Indicates ac power is ok and battery is charging. Flashing (fast) – Indicates loss of ac power and that battery is discharging while maintaining MOS memory contents.
RUN	Indicates the state of the processor, either running or halted.

Table 2-1 KY11-LB Controls and Indicators (Cont)

Control/Indicator	Function
SR DISP	Indicates that the content of the switch register is being displayed.
MAINT	Indicates that console is in maintenance mode.
BUS ERR	Indicates that an examine or deposit resulted in a SSYN time-out or that HALT REQUEST failed to receive a HALT GRANT.
DC Power Switch	
DC OFF	All dc power to logic is off.
DC ON	All dc power to logic is on.
STNBY	DC power is provided to MOS memory only.*

*Available in all BA11-C machines. Available in BA11-K boxes which have Battery Backup Option only.

Table 2-1 refers to certain registers which are located in the scratchpad RAM. These include the following:

1. Display Data
2. Keypad Image
3. Temporary Data Buffer
4. Unibus Address Pointer
5. Switch Register Image
6. EXAM, DEP, ENB and C1 flags

Detailed discussion of the scratchpad RAM and its registers is set forth in Chapter 5.

2.2.2 Maintenance Mode

Mantenance mode is entered by pressing the CNTRL key and the 1 key simultaneously. Note that the functions performed by the appropriate keys are quite different from console mode. This mode offers the ability to assert the manual clock enable and thus to single-clock cycle the processor while monitoring the contents of the processor microprogram counter.

2.3 HARDWARE ORGANIZATION

A detailed block diagram of the interface module showing data flow and control is indicated in Figure 2-3. The control functions shown include those for the Unibus interface and the internal data bus with the microprocessor. The latter controls include those for reading from and writing into the RAM, enabling ROMs 1 and 2, and reading the Unibus temporary buffer register or loading the bus address and switch registers. All of these functions occur on appropriate control from the stored program and keypad.

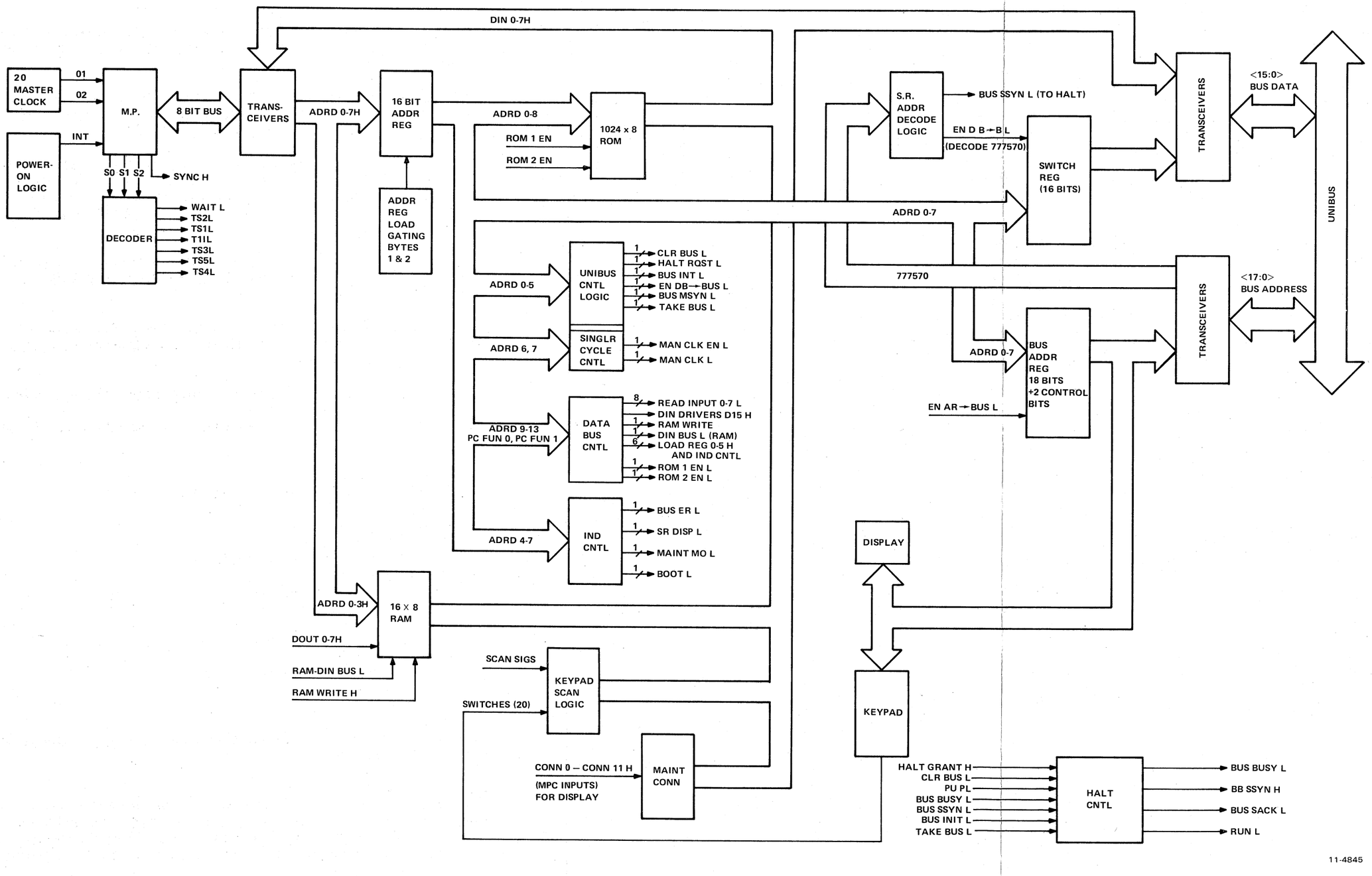

Figure 2-3 Interface Module Detailed Block Diagram

Under microprogram control, the data bus control logic develops the loading or reading signal for the appropriate register and thus determines the selected input/output port via the data bus control and the function currently being executed.

As shown in Chapter 3 when the detailed microprocessor cycle is presented, the microprocessor executes four basic machine cycles. They are summarized here to show their relation to interface module functions.

1. *PCI* – This is always the first cycle of a microprocessor instruction and initiates the instruction fetch. The program counter is transferred in two bytes from the microprocessor to the 16-bit interface module address register (14 bits of address, 2 control bits) to fetch the instruction data from either the ROM or RAM. A single byte of instructions is retrieved during this cycle.

2. *PCR* – This cycle may retrieve an additional byte of instruction (if the instruction is a 2- or 3-byte instruction) or it may fetch a data byte if the indicated instruction contains only one byte.

3. *PCC* – This cycle specifies the function as an I/O operation. This machine cycle reads and loads the address and data registers which cause information to be read from or written into the microprocessor.

4. *PCW* – This cycle controls the memory write function according to the designated address.

Figure 2-3 shows that the basic satellite logic and control for the microprocessor chip consists of the following elements:

2-phase master clock
Decoder for interface module time states
Power-up logic
16-bit address register
16-word × 8-bit RAM
1024-word × 8-bit RAM (four – 512 × 4)
Switch register (16 bit)
Switch register address decoding
Bus address register (20 bit)
Tristate transceivers
Keypad scan and display logic
Data bus control
Unibus control and single-cycle control
Indicator control
Halt control

These major functions are briefly described in the following paragraphs; detailed theory of operation is presented in Chapter 5.

2-Phase Master Clock
The master clock drives the microprocessor internal logic and generates the system states for instruction sequencing. The nominal 1 MHz clock frequency is toggled down to two nonoverlapping, 500-kHz pulses known as phase 1 (01) and phase 2 (02). Phase 1 is normally used to pre-charge data lines and memories while phase 2 controls data transfers within the microprocessor.

Decoder for Timing States
The decoder element receives the state outputs S0, S1, and S2 from the microprocessor and generates the time states for the operation of the interface module. A sync pulse corresponding to two phase clock periods (1 time state) is also provided by the microprocessor.

Power-up Logic
This circuitry activates the microprocessor, clearing its various registers and generating a clear line to all the registers of the interface module. There are separate clears for the address register and all other registers.

Address Register
This 16-bit register is the principal buffer between the microprocessor and the remainder of the logic of the interface module. Although designated as an address register, the element also handles control data for the Unibus, data bus, and other control functions and outputs to the bus address and switch registers. One of its major functions is to receive the microprocessor program counter contents for fetching new instructions from the ROM or RAM.

RAM
The 16-word by 8-bit RAM gives the interface module a scratchpad memory which may be read or whose contents may be modified under program control.

ROM
The ROM, consisting of four 512 × 4-bit ROMs, makes a total of 1024 8-bit bytes available for the stored programs which execute the console functions.

Switch Register Address Decoding
This logic decodes 777570, an 18-bit address defining the switch register and a DATI on the Unibus to cause the switch register to be enabled onto the Unibus.

Switch Register
This 16-bit buffer register handles the data word to the Unibus.

Bus Address Register
This 20-bit register buffers address information between the interface module and the Unibus. Eighteen bits are allocated for the actual address, and two control bits indicate the direction of data flow. Scan signals for the keypad and NUM lines for the display logic are specified by this register.

Tristate Gates
These units are used to gate buffered Unibus data (16 bits) and Unibus address (18 bits) lines onto the tristate data bus by asserting an appropriate read input line. Keypad outputs and those maintenance lines provided for display of the processor microprogram counter are similarly buffered and gated. The outputs are all wire ORed onto the internal data bus and applied as input to the tristate transceivers.

Keypad Scan and Display Logic
This circuitry develops read and drive signals for the keypad and LED display respectively. Five read signals developed from the scan signals are used to scan the keypad switch closures in groups of four. The drive signals are applied to the LED displays whose values are determined by the 3-bit NUM input.

Data Bus Control
This circuitry performs all internal interface module control functions including RAM control, ROM enable, and selection of input/output ports. The logic also determines system operation during instruction, data fetch, or data out (TS3) via a 32- × 8-bit ROM.

Unibus Control
The Unibus control register supervises data transfers between the interface module and the Unibus. According to the input bit patterns to the register, data transfer from the interface module to the Unibus, halt request, bus master sync, and other functions may be generated as required for proper interfacing of the two elements. Two other signals generated in the Unibus control register permit single stepping of the processor clock.

Indicator Logic
This 4-bit register drives appropriate console indicators to show certain console states or errors. An indicator is turned on to show the existence of a bus error, when the switch register is being displayed or when in maintenance mode.

Halt Logic
This circuitry halts the processor under various conditions and performs handshaking functions when the console takes complete control of the bus. When a HALT from the console is detected by the processor, the processor recognizes it as an interrupt request. The processor then inhibits its clock and returns a recognition signal to the console causing the console to assert an acknowledge. The console now has complete control of the Unibus and processor and may maintain this condition, with the processor halted, as long as desired.

2.4 MICROPROCESSOR INSTRUCTION SET

The interface module microprocessor has a repertoire of 48 basic instructions. According to the instruction type, these may range from 1 to 3 bytes (8 to 24 bits) in length. The successive bytes of a given instruction must be located in sequential memory locations. Instructions fall into one of five categories:

Index Register
Accumulator (Arithmetic/Logical)
Program Counter and Stack Control
Input/Output
Machine

A description of the microprocessor instructions and the number of time states required for their execution is given in Chapter 4.

CHAPTER 3
INTERFACE MODULE

3.1 MICROPROCESSOR

3.1.1 General Organization

The microprocessor sends and receives data over an 8-bit data and address bus (D_0 to D_7) and utilizes four input and four output lines (Figure 3-1). The microprocessor contains six 8-bit data registers, an 8-bit accumulator, two 8-bit temporary registers, four flag bits, and an 8-bit parallel binary arithmetic unit. The arithmetic element is capable of performing addition, subtraction, and logical operations. Additionally, a memory stack containing a 14-bit program counter and seven 14-bit words is used to store program and subroutine addresses. The microprocessor machine cycle usually requires five sequential states: TS1, TS2, TS3, TS4, and TS5. During time states TS1 and TS2, the external memory is addressed by a lower and an upper address byte respectively to form a 14-bit address. Also at TS1 time, the program counter (PC) is incremented for the next instruction fetch cycle. During time state TS3, the instruction addressed during states TS1 and TS2 is fetched and during the final two cycles, TS4 and TS5, it is executed. Figure 3-2 shows the possible number and sequence of the instruction states. Note that for this application of the microprocessor, the interrupt function is utilized only during the power-on sequence.

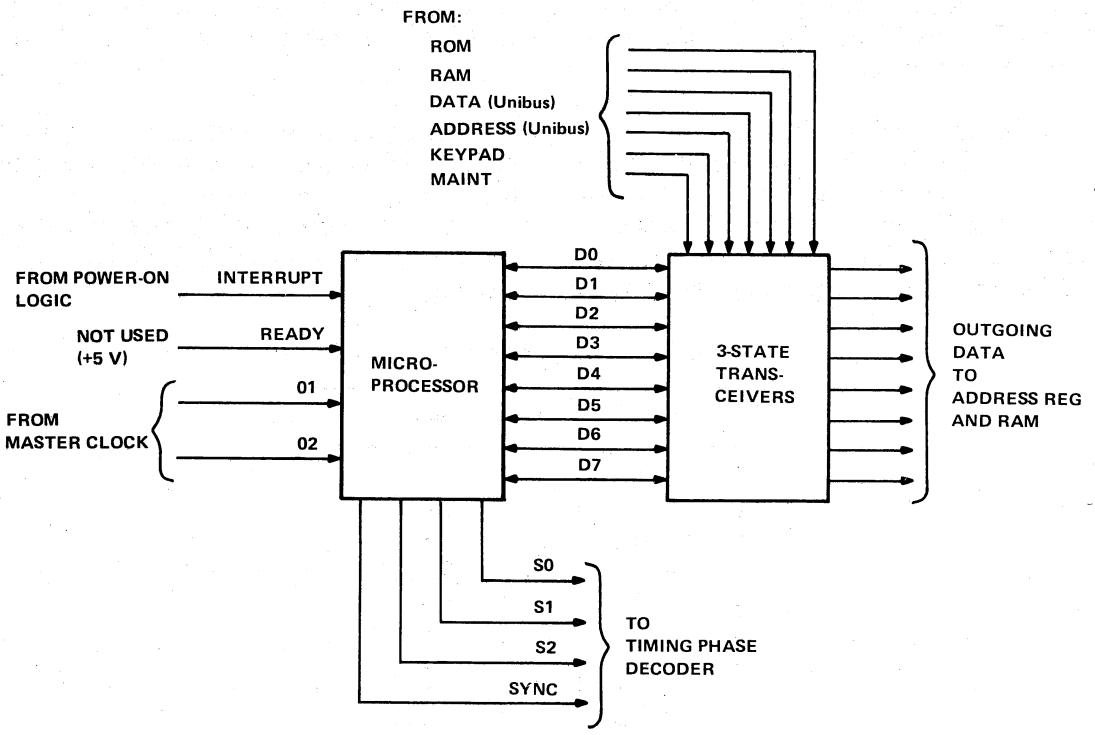

Figure 3-1 Microprocessor Signal Interface

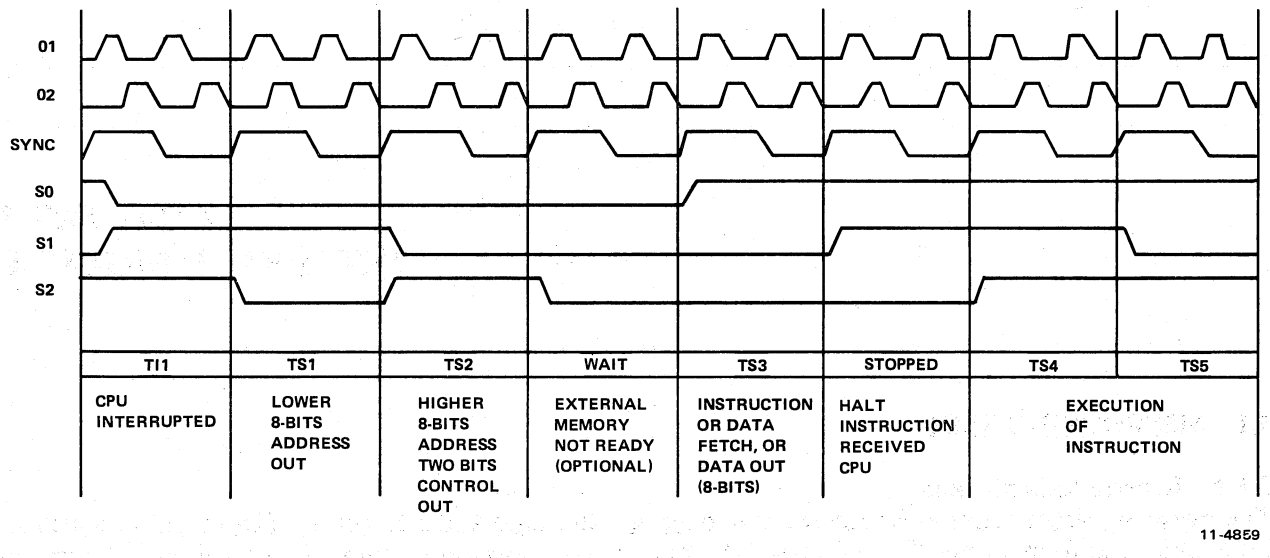

Figure 3-2 Timing Diagram – Microprocessor Instruction

3.1.2 State Control

The microprocessor operates as a sequential state machine, controls the use of the data bus, and, according to its stored program, determines whether it sends or receives data. Output state signals S0, S1, and S2 are decoded externally and distributed to the peripheral control logic. Table 3-1 shows the coding of the state bits to yield a given phase.

3.1.3 Microprocessor Timing

The microprocessor machine cycle is shown in Figure 3-2. Since machine operation is asynchronous, the exact timing sequences depend on the instruction executed. A typical cycle may consist of five states. During T1 and T2, an address is sent to memory; at T3 time, instruction or data fetch occurs; T4 and T5 provide execution time.

A number of microprocessor instructions may require up to three cycles and do not require the two execution states T4 and T5. As a result, cycle length is variable and the state counter determines whether T4 and T5 are to be executed or omitted. This is accomplished via the cycle control coding (Table 3-2) in bits D6 and D7. Cycle 1 is always an instruction fetch cycle (PCI). The second and third cycles are for data reading (PCR), data writing (PCW), or I/O operations (PCC). The cycle type bits D6 and D7 are present on the data bus during T2 time only.

Table 3-1 State Control Coding

S0	S1	S2	State
0	1	0	T1
0	1	1	T11
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOPPED
1	1	1	T4
1	0	1	T5

Table 3-2 Cycle Coding

D_6	D_7	Cycle	Function
0	0	PCI	Designates the address is for a memory read (first byte of instruction).
0	1	PCR	Designates the address is for a memory read data (additional bytes of instruction or data).
1	0	PCC	Designates the data is a command I/O operation.
1	1	PCW	Designates the address is for a memory write data.

3.1.4 Transition State Diagram

Possible state transitions within the processor are shown in Figure 3-3. Note that a normal machine cycle would begin at cycle 1, run from T1–T5, and revert back to cycle 1 again. The state counter within the microprocessor operates as a 5-bit feedback shift register with the feedback path controlled by the current instruction. The number of states normally required by each instruction is discussed in Chapter 4.

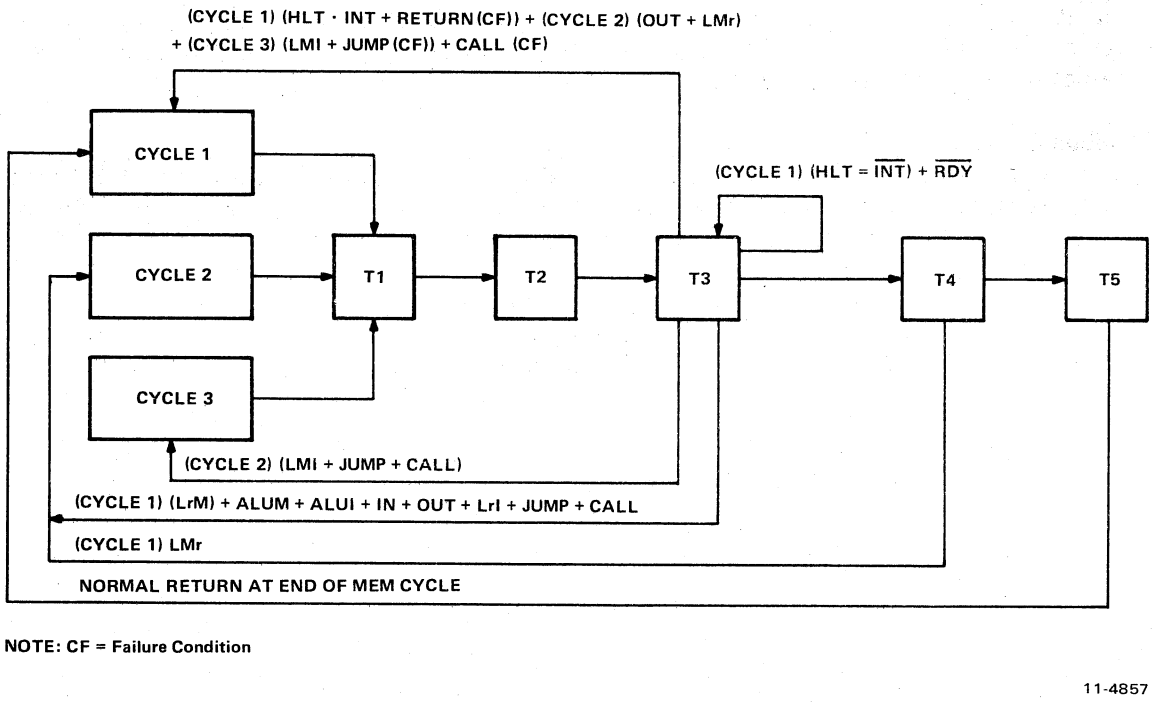

Figure 3-3 Transition State Diagram

3.1.5 System Start-Up

The microprocessor of the interface module is running any time power is applied to the system. When power (VDD) and clocks (01, 02) are first turned on, a flip-flop internal to the microprocessor is set by sensing the rise of VDD. This internal signal forces a HALT (00000000) into the instruction register and the microprocessor is then in the stopped state. The next 16 clock periods are required to clear internal chip memories and other external logic and registers. Upon clearing the registers the system is ready for operation. If for any reason during operation, the microprocessor decodes a HALT, the system reverts to the beginning of the program after 16 clock periods.

3.2 INTERFACE MODULE REGISTERS AND CONTROLS (Figure 2-1)

3.2.1 Address Register

This is the principal buffer register between the microprocessor and the rest of the interface module logic. It has a capacity of 16 bits (two 8-bit bytes). The low order byte is loaded by time state TS1 and the high order byte by time state TS2 during each cycle.

3.2.2 Bus Address Register

The bus address register buffers address data between the interface module and the Unibus. Address information may be loaded into this register at time state TS3.

3.2.3 Switch Register

Similar to the bus address register, the switch register buffers outgoing data. This element may also be loaded at TS3.

3.2.4 Data Bus Control

The principal function of the data bus control is to determine interface module operation during TS3 time. It determines, through input bit coding, the type of function to be performed (i.e., RAM control, ROM enable) or programs any of its other I/O in accordance with the stored program.

3.2.5 Unibus Control

This register is also loaded at TS3 and is selected by the data bus control for activation at that time. According to its input coding, U.C.R. may issue a HALT request, BUS INIT, enable-data bus-to-bus, or generate a bus master sync in addition to other functions.

CHAPTER 4
MICROPROCESSOR INSTRUCTION DESCRIPTION

4.1 DATA AND INSTRUCTION FORMATS

Data in the CPU is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference I/O arithmetic or logical, rotate or return instructions.

Two Byte Instructions

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Immediate mode instructions.
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	

Three Byte Instructions

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS	JUMP or CALL instructions
X X D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS*	

*For the third byte of this instruction, D_6 and D_7 are "don't care" bits.

4.2 MICROPROCESSOR INSTRUCTIONS

4.2.1 Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

Mnemonic	Minimum States Required	Instruction Code D_7D_6 $D_5D_4D_3$ $D_2D_1D_0$	Description of Operation
(1) Lr_1r_2	(5)	1 1 D D D S S S	Load index register r_1 with the content of index register r_2.
(2) LrM	(8)	1 1 D D D 1 1 1	Load index register r with the content of memory register M.
LMr	(7)	1 1 1 1 1 S S S	Load memory register M with the content of index register r.
(3) LrI	(8)	0 0 D D D 1 1 0 B B B B B B B B	Load index register r with data B . . . B.
LMI	(9)	0 0 1 1 1 1 1 0 B B B B B B B B	Load memory register M with data B . . . B.
INr	(5)	0 0 D D D 0 0 0	Increment the content of index register r ($r \neq A$).
DCr	(5)	0 0 D D D 0 0 1	Decrement the content of index register r ($r \neq A$).

4.2.2 Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

Mnemonic	Minimum States Required	Instruction Code D_7D_6 $D_5D_4D_3$ $D_2D_1D_0$	Description of Operation
ADr	(5)	1 0 0 0 0 S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADM	(8)	1 0 0 0 0 1 1 1	
ADI	(8)	0 0 0 0 0 1 0 0 B B B B B B B B	
ACr	(5)	1 0 0 0 1 S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ACM	(8)	1 0 0 0 1 1 1 1	
ACI	(8)	0 0 0 0 1 1 0 0 B B B B B B B B	

Mnemonic	Minimum States Required	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Description of Operation
SUr	(5)	1 0 0 1 0 S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUM	(8)	1 0 0 1 0 1 1 1	
SUI	(8)	0 0 0 1 0 1 0 0 B B B B B B B B	
SBr	(5)	1 0 0 1 1 S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBM	(8)	1 0 0 1 1 1 1 1	
SBI	(8)	0 0 0 1 1 1 0 0 B B B B B B B B	
NDr	(5)	1 0 1 0 0 S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
NDM	(8)	1 0 1 0 0 1 1 1	
NDI	(8)	0 0 1 0 0 1 0 0 B B B B B B B B	
XRr	(5)	1 0 1 0 1 S S S	Compute the Exclusive OR of the content of index register r, memory M, or data B . . . B with the accumulator.
XRM	(8)	1 0 1 0 1 1 1 1	
XRI	(8)	0 0 1 0 1 1 0 0 B B B B B B B B	
ORr	(5)	1 0 1 1 0 S S S	Compute the Inclusive OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
ORM	(8)	1 0 1 1 0 1 1 1	
ORI	(8)	0 0 1 1 0 1 0 0 B B B B B B B B	
CPr	(5)	1 0 1 1 1 S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CPM	(8)	1 0 1 1 1 1 1 1	
CPI	(8)	0 0 1 1 1 1 0 0 B B B B B B B B	
RLC	(5)	0 0 0 0 0 0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0 0 0 1 0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0 0 1 0 0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0 0 1 1 0 1 0	Rotate the content of the accumulator right through the carry.

4.2.3 Program Counter and Stack Control Instructions

Mnemonic	Minimum States Required	Instruction Code D_7D_6 $D_5D_4D_3$ $D_2D_1D_0$	Description of Operation
(4) JMP	(11)	0 1 X X X 1 0 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$.
(5) JFc	(9 or 11)	0 1 0 C_4 C_3 0 0 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
(5) JTc	(9 or 11)	0 1 1 C_4 C_3 0 0 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
(4) CAL	(11)	0 1 X X X 1 1 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$. Save the current address (up one level in the stack).
(5) CFc	(9 or 11)	0 1 0 C_4 C_3 0 1 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop c is false, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
(5) CTc	(9 or 11)	0 1 1 C_4 C_3 0 1 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop c is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
(4) RET	(5)	0 0 X X X 1 1 1	Unconditionally return (down one level in the stack).
(5) RFc	(3 or 5)	0 0 0 C_4 C_3 0 1 1	Return (down one level in the stack) if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
(5) RTc	(3 or 5)	0 0 1 C_4 C_3 0 1 1	Return (down one level in the stack) if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0 A A A 1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).

4.2.4 Input/Output Instructions

Mnemonic	Minimum States Required	Instruction Code D_7D_6 $D_5D_4D_3$ $D_2D_1D_0$	Description of Operation
INP	(8)	0 1 0 0 M M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1 R R M M M 1	Write the content of the accumulator into the selected output port (RRMMM) (RR ≠ 00).

4.2.5 Machine Instruction

Mnemonic	Minimum States Required	Instruction Code D_7D_6 $D_5D_4D_3$ $D_2D_1D_0$	Description of Operation
(4) HLT	(4)	0 0 0 0 0 0 0 X	Enter the STOPPED state and remain there until interrupted.
HLT	(4)	1 1 1 1 1 1 1 1	Enter the STOPPED state and remain there until interrupted.

NOTES:

(1) SSS = Source Index Register
DDD = Destination Index Register
These registers, r_1, are designated A (accumulator–000). B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by C_4C_3: carry (00 overflow or underflow), zero (01-result is zero), sign (10 MSB of result is "1"), parity (11-parity is even).

CHAPTER 5
INTERFACE MODULE DETAILED LOGIC DESCRIPTION

5.1 INTRODUCTION

Keypad operation initiates appropriate microprocessor routines which perform certain data transfers within the interface module, between the interface module and the Unibus, and between the interface module and the programmer's console display. Prior to discussing the interface module logic, the sequences (i.e., register transfer, I/O operations, etc.) which occur after pressing a given key are briefly described.

Figure 5-1 shows the 16-word by 8-bit scratchpad RAM and its address allocations. This data is also summarized in Table 5-1. The keypad image within the RAM is shown in Figure 5-2.

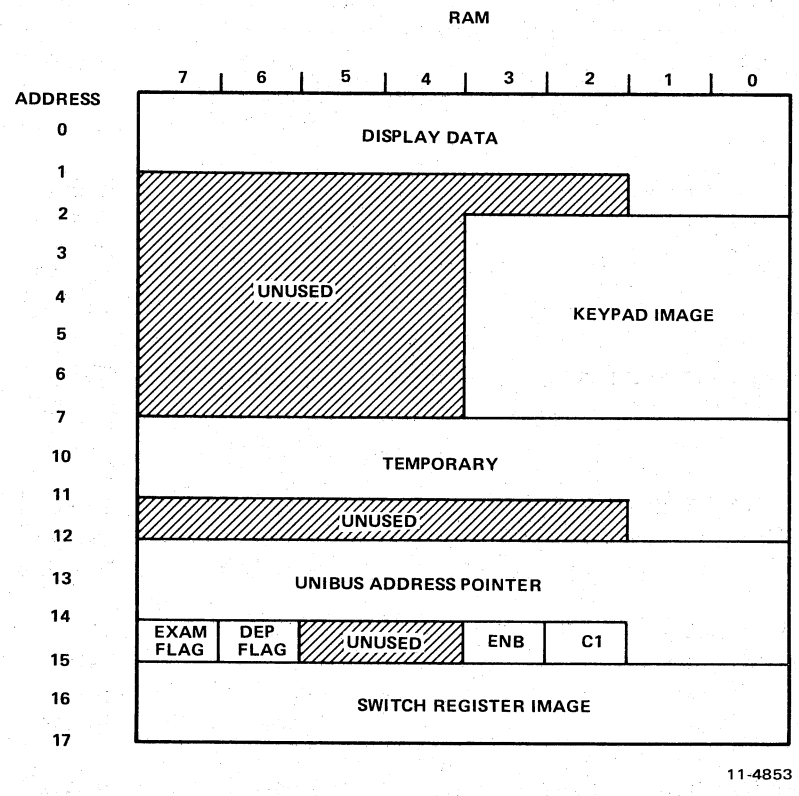

Figure 5-1 RAM Address Allocations

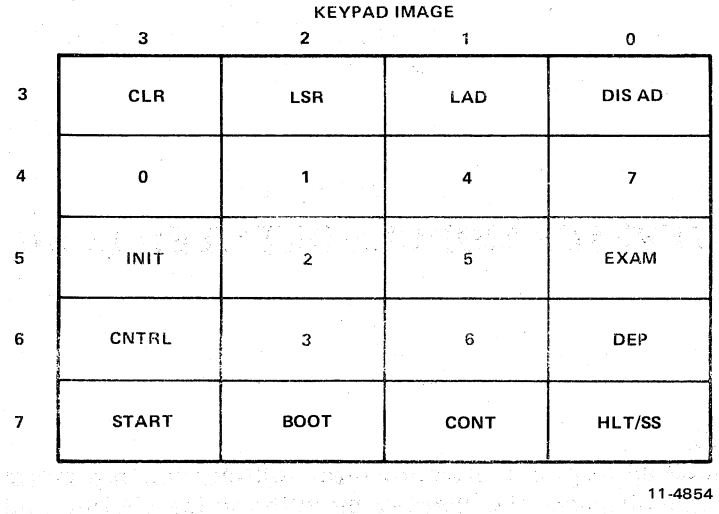

Figure 5-2 Keypad Image

Table 5-1 RAM Function Address Assignments

Function	Address (Octal)	Address Bits
Display Data (18 bits)	Word 0	Bits 0–7
	Word 1	Bits 0–7
	Word 2	Bits 0, 1
Keypad Image (20 bits)	Word 3	Bits 0–3
	Word 4	Bits 0–3
	Word 5	Bits 0–3
	Word 6	Bits 0–3
	Word 7	Bits 0–3
Temporary Data Buffer (18 bits)	Word 10	Bits 0–7
	Word 11	Bits 0–7
	Word 12	Bits 0, 1
Unibus Address Pointer (18 bits)	Word 13	Bits 0–7
	Word 14	Bits 0–7
	Word 15	Bits 0, 1
EXAM FLAG	Word 15	Bit 7
DEP FLAG	Word 15	Bit 6
ENB FLAG	Word 15	Bit 3
C1 FLAG	Word 15	Bit 2
Switch Register Image (16 bits)	Word 16	Bits 0–7
	Word 17	Bits 0–7

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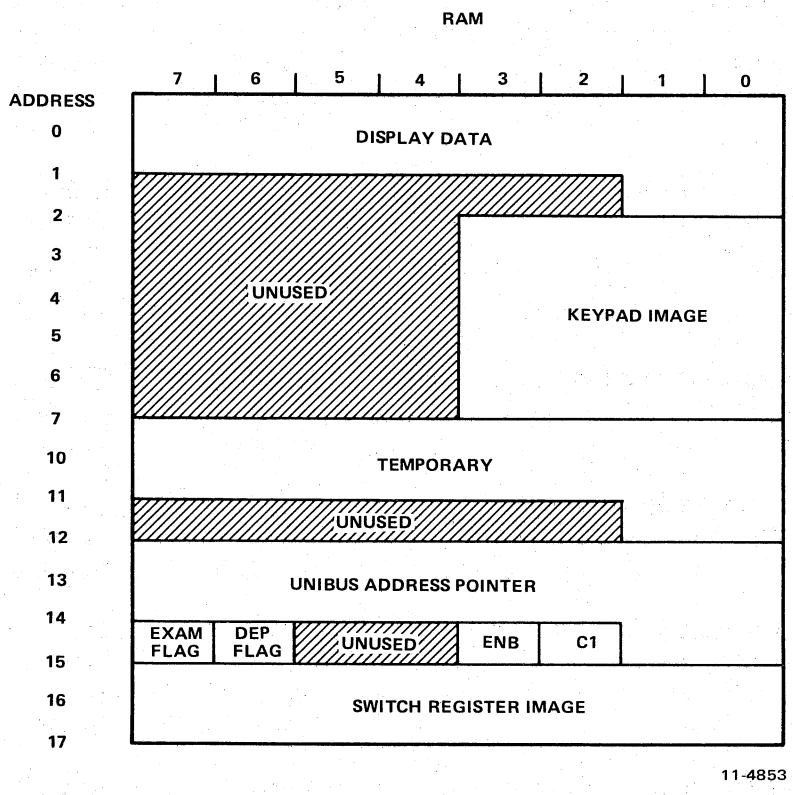
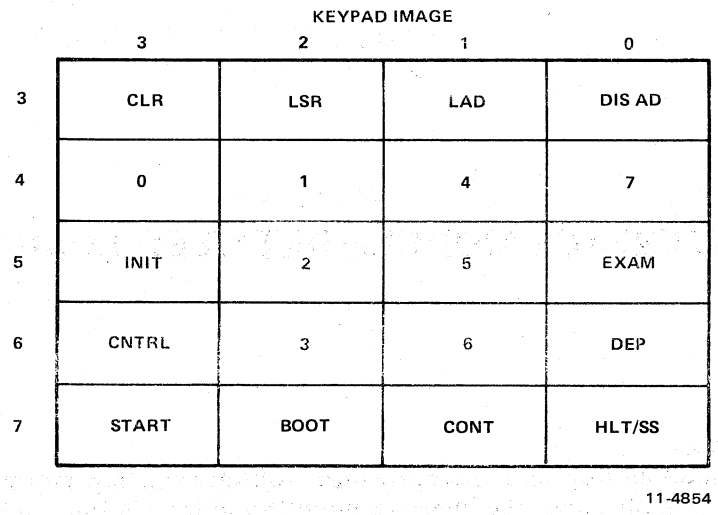


Figure 5-1 RAM Address Allocations



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	Word 5	Bits 0–3
	Word 6	Bits 0–3
	Word 7	Bits 0–3
Temporary Data Buffer (18 bits)	Word 10	Bits 0–7
	Word 11	Bits 0–7
	Word 12	Bits 0, 1
Unibus Address Pointer (18 bits)	Word 13	Bits 0–7
	Word 14	Bits 0–7
	Word 15	Bits 0, 1
EXAM FLAG	Word 15	Bit 7
DEP FLAG	Word 15	Bit 6
ENB FLAG	Word 15	Bit 3
C1 FLAG	Word 15	Bit 2
Switch Register Image (16 bits)	Word 16	Bits 0–7
	Word 17	Bits 0–7

5.2 PROGRAMMER'S CONSOLE KEYPAD FUNCTION SEQUENCES

5.2.1 Console Mode Key Functions

NUMERICS (0–7)

1. Value of Key $\xrightarrow{\text{(left shifted)}}$ Temporary Data Buffer
2. Temporary → Display
3. Clear indicators.

LAD

1. Temporary → Unibus Address Pointer
2. Zero → Temporary
3. Temporary → Display
4. Clear/Indicators.

LSR

1. Temporary → Switch Register Image
2. Switch Register Image → Switch Register
3. SR DISP indicator is set.

CLR

1. Zero → Temporary
2. Temporary → Display
3. Clear indicators.

EXAM

1. Pre-increment Unibus address pointer if the EXAM flag is set.
2. Unibus Address Pointer → Bus Address Register
3. Bus Address Register → Unibus Address
4. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μs, the transfer is aborted and the BUS ERR indicator is set.

5. Unibus Data → Temporary
6. Temporary → Display
7. Set EXAM flag.

DEP

1. Pre-increment Unibus address pointer if the DEP flag is set.
2. Unibus Address Pointer → Bus Address Register with C1 = 1.
3. Bus Address Register → Unibus Address
4. Temporary → Switch Register
5. Switch Register → Unibus Data
6. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μs, the transfer is aborted and the BUS ERR indicator is set.

7. Set DEP flag.
8. Switch Register Image → Switch Register

DIS AD

1. Unibus Address Pointer → Display
2. Clear EXAM or DEP flag if set.

CNTRL–INIT

1. Set BUS INIT and HALT REQUEST for 150 ms.

CNTRL–HLT/SS

1. Clears BUS SACK/BUS BUSY if set and sets HALT REQUEST
2. When HALT BUSY is active, sets 777707 → Bus Address Register
3. Bus Address Register → Unibus Address
4. Assert MSYN

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μs, the transfer is aborted and the BUS ERR indicator is set.

5. Unibus Data → Temporary
6. Temporary → Display

CNTRL–CONT

1. Clears BUS SACK and BUS BUSY.
2. Switch Register Image → Display
3. Set SR DISP indicator.

CNTRL–BOOT

1. Sets and clears BOOT signal
2. Switch Register Image → Display
3. Set SR DISP indicator.

CNTRL–START

1. 777707 → Bus Address Register with C1 = 1
2. Bus Address Register → Unibus Address
3. Unibus Address Pointer → Switch Register
4. Switch Register → Unibus Data
5. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μs, the transfer is aborted and the BUS ERR indicator is set.

6. Switch Register Image → Switch Register
7. Assert BUS INIT for 150 ms.
8. Switch Register Image → Display
9. Set SR DISP indicator.

CNTRL–7

1. Unibus Address Pointer + Temporary +2 → Temporary

CNTRL–6

1. Temporary + Switch Register Image → Temporary

CNTRL–1

1. Set maintenance indicator.
2. MPC Lines (sampled) → Display

5.2.2 Maintenance Mode Key Functions

CLR

1. Clears indicators.
2. Clears manual clock enable, if set.
3. Goes to halt condition.

DIS AD

1. Unibus Address (sampled) → Display

EXAM

1. Unibus Data (sampled) → Display

HLT/ISS

1. Sets manual clock enable.
2. Clears BUS SACK and BUS BUSY.
3. MPC (sampled) → Display

CONT

1. Sets and clears manual clock
2. MPC (sampled) → Display

BOOT

1. Sets and clears BOOT signal.

START

1. Clears manual clock enable, if set.
2. MPC (sampled) → Display

No. 5

1. Sets TAKE BUS signal, forcing console to assert BUS BUSY.

5.3 DETAILED LOGIC DESCRIPTION

5.3.1 Clock Circuitry

The M7859 Interface board is driven by an MC 4024 (E42) 1-MHz clock (drawing CS M7859-0-1, sheet 2). The 1-MHz output at E42-8 is toggled down to two nonoverlapping 500-kHz pulses at E12-5, 6, and E30, and these pulses are applied to the microprocessor (E18) input as 01 and 02. The 02 clock, designated as KY1 CK2 H and KY1 CK2 L, is also used as a control pulse to clear system registers and together with the sync pulse to define the end of a timing cycle.

Figure 5-1 shows the relation between the two clock pulses.

5.3.2 Power-Up Logic/Interrupt (Drawing CS M7859, Sheet 2)

The power-up logic/interrupt circuitry is comprised of E1-6, E40-10, E1-4, E36, E12, E29-1, E6, and E26. These elements sense when the system turns on, generate the interrupt to the microprocessor needed to start it, and clear registers to force program startup at location 0.

BUS DC LO at E1-3 initiates the function by clearing E36 which is configured as an 8-bit counter and generates KY1 PUP 1 L. This signal is routed to the Unibus control, indicator control, switch register, and bus address register as a master clear line. The address register is provided with its own clear line, KY1 ADR CLR L.

BUS DC LO L puts the microprocessor in the STOP state. The counter starts counting in the STOP state (E6, E36). KY1 STOP L and KY1 C2 L at E29-1 clock E6. E6 is a divide by two on the clock, while E36 counts from 0–7. Sixteen clock periods are thus counted. At the transition of E36 from 7 to 0, the interrupt is generated at E12-8 and the microprocessor goes into the T1I state (Interrupt). KY1 T1I L and KY1 CK2 L then reset E12 and clear the address register via E6-6 and the system is initialized.

5.3.3 Microprocessor (Drawing CS M7859, Sheet 2)

The 8008 Microprocessor Chip (E18) was discussed in detail in Chapter 3. According to drawing CS M7859, sheet 2, the unit communicates over an 8-bit bidirectional data bus via 8833 tristate transceivers E16 and E17, with the satellite logic of the interface module. A single interrupt line is received from the power-up logic to initiate microprocessor operations. Driven by a 2-phase, 500-kHz clock (Figure 5-1), the element yields a 3-bit state output code, S0, S1, and S2, plus a sync pulse, to drive a 7442 Timing Phase Decoder. The latter element provides eight separate timing cycles for the sequencing of interface module data transfers and other discrete operations.

5.3.4 Timing State Decoder

The timing state decoder (E23) receives the state outputs S0, S1, and S2 from the microprocessor and generates the timing states for the interface modules (drawing CS M7859, sheet 2). This unit is a 7442 4-line to 10-line decoder, with two unused outputs, that yields an 8-output sequence according to its 3-input state code. State control coding is presented in Chapter 3. State control inputs are determined in the microprocessor and depend on an internal 5-bit feedback shift register with the feedback path controlled by the instruction being executed.

5.3.5 Address Register (Drawing CS M7859, Sheet 2)

The address register, the principal buffer between the microprocessor and the remainder of the interface module logic, consists of four 74175 quad, D-type, double rail output latches. The low order bits are handled by E5 and E4 which generate KY1 ADRD 0 L through KY1 ADRD 3 L (E5) and their complements (for RAM addressing), and KY1 ADRD 4 H through KY1 ADRD 7 H (E4), respectively. This 8-bit byte is the low order unit of the address or data with E10 and E28 containing the high order information ADRD 08–13 and PC FUN 1 and 0.

The data contained in the address register is routed to the following locations according to direction by the stored program:

1. ROM (address of next instruction)(KY1 ADRD 0 L → KY1 ADRD 8 L plus ROM 1 EN L or ROM 2 EN L)
2. RAM (address of data to be read or written) (KY1 ADRD 0 L → KY1 ADRD 3 L)
3. Unibus Control (KY1 ADRD 0 H → KY1 ADRD 3 H)
4. Indicator Control (KY ADRD 4 H → KY1 ADRD 7 H)
5. Data Bus Control (KY1 ADRD 9 H → KY1 ADRD 13 H, KY1 PC FUN 0 H, KY1 PC FUN 1 H)
6. Switch Register (KY1 ADRD 0 H → KY1 ADRD 7 H)
7. Bus Address Register (KY ADRD 0 H → KY1 ADRD 7 H)

The address register is loaded with a low order byte (E4 and E5) by signal KY1 LD AD 1 H, generated by AND E22-12 at time state TS1. The high order byte is gated in E28 and E10 by KY1 LD AD 2 H generated at E22-6 at timing state TS2.

5.3.6 ROM

The interface module ROM consists of E3, E21, E33, and E39 (drawing CS M7859, sheet 3). The four 512-word by 4-bit elements are addressed so that the ensemble looks like two 512- × 8-bit RMs. E3 and E21 are activated by KY4 ROM 1 EN L and E33 and E39 by KY4 ROM 2 EN L. Address bits KY1 ADRD 0 H through KY1 ADRD 8 H are routed to all four ROM elements with the enable 1 or 2 determining the address activated and thus yielding 1024 8-bit locations. Outputs are wire ORed with various inputs to give the KY2 DIN 0 H through KY2 DIN 7 H inputs to the tristate transceivers, E16 and E17.

The ROM 1 or RM 2 enables are generated by the data bus control logic.

5.3.7 RAM

The scratchpad RAM consists of E11 and E27 (drawing CS M7859, sheet 3). These units effectively comprise a 16-word by 8-bit read/write memory, and serve as working storage for the microprocessor programs in storing addresses and data. Data is routed to the RAM (KY1 DOUT 0 H through KY1 DOUT 7 H) directly from the tristate transceivers of the microprocessor bidirectional data bus during RAM write operations. The 4-bit address lines KY1 ADRD 0 L through KY1 ADRD 3 L specify the address to be read from or written into during read/write.

Selection of the RAM for read or write is determined by the stored program via the data bus control. Either KY4 RAM → DIN BUS L or KY4 RAM WRITE H must be true to select the RAM. Output lines are wire ORed with various other microprocessor input ports to be routed to the 8833 tristate transceivers.

5.3.8 Switch Register (Drawing CS M7859, Sheet 6)

The switch register contains the 16-bit data used and consists of four 74175 quad, D-type, double rail output latches. The four elements comprising the register are E9, E19, E2, and E15. These units feed the 8641 bus transceivers E7, E25, E8, and E13 (respectively). Incoming 16-bit data (KY5 BB D00 H through KY5 BB D15 H) is applied to the 8093 tristate buffers and gated by an appropriate read line from the data bus control. Outgoing data (BUS D00 L through BUS D15 L) is gated by KY4 EN DB L, a signal generated in the switch register address decoding logic (sheet 5).

The switch register is addressable from the Unibus as address 777570 as described in Paragraph 5.3.9.

5.3.9 Switch Register Address Decode Logic (Drawing CS M7859, Sheet 5)

The switch register address decoding logic allows the Unibus to address the switch register via a decoding of address 777570. The logic has two outputs:

1. BUS SSYN L
2. KY4 EN DB → BUS L

K44 EN DB → BUS L at E43-10 gates the data lines onto the Unibus (CS M7859, sheet 6) while the assertion of BUS SSYN L designates that the slave device has completed its part of the data transfer. The second stage of the address decode at E32 is gated by assertion of BUS MSYN L at E32-10. Assertion of MSYN requests that the slave defined by the A (address) lines perform the function required by the C lines. In this case, KY7 BB C1 H at invertor E40-9 specifies that the data is to be transferred to the Unibus data lines.

5.3.10 Bus Address Register (Drawing CS M7859, Sheets 7 and 8)

The bus address register consists of five 74175 quad, D-type, double rail output latches. The five elements comprising the register are E67, E57, E73, E58, and E51. Input to the bus address register is from the address register (KY1 ADRD 0 H through KY1 ADRD 7 H). Outputs are routed to the display and keypad logic and to the 8641 Unibus transceivers E61, E56, E65, E55, and E50.

A Unibus address is enabled to the Unibus via the bus address transceivers from the bus address register by KY7 EN AR L generated at E51-11. The switch register is available to the Unibus as address 777570 via the bus address transceivers and the switch register decode logic. The latter function is discussed in Paragraph 5.3.9.

E67 and E57 contain the keypad scan signals (KY6 SCAN 1 L through KY6 SCAN 6 L) while E73 drives the display (KY6 NUM 1 H through KY6 NUM 3 H).

Incoming 18-bit address information (KY6 BB A00 H through KY7 BB A17 H) is applied to the 8093 tristate buffers and gated by an appropriate read line from the data bus control.

5.3.11 Data Bus Control Logic (Drawing CS M7859, Sheet 5)

The data bus control directs the reading and loading of the various interface module registers, the reading of the ROMs, and the reading/writing of the RAM. It also determines the direction of data flow in the interface module and between the interface module and the Unibus, i.e., whether data will be read from or be routed to the Unibus. A list of I/O functions and associated select signals follows:

Select Signal	Function
READ INPUT 0 L READ INPUT 1 L	UNIBUS DATA
READ INPUT 2 L READ INPUT 3 L READ INPUT 4 L	UNIBUS ADDRESS
READ INPUT 5 L	KEYPAD REG
READ INPUT 6 L READ INPUT 7 L	MAINTENANCE
LD REG 0 H LD REG 1 H LD REG 2 H	BUS ADDR REG
LD REG 3 H LD REG 4 H	SWITCH REG
LD REG 5 H	UNIBUS CONT LOGIC
EN ROM 1 L EN ROM 2 L	ROM SELECT
RAM WRITE H	RAM WRITE
RAM DIN BUS L	ENABLE RAM DATA
DIN DRIVERS DIS H	DISABLE DATA IN

Specifically, the data bus control logic decodes memory references into three areas (ROM 1, ROM 2, and RAM) and determines whether the access is a read or write. The logic also decodes I/O instructions and generates loading or gating signals depending on the direction of data transfer and the port selected.

In order to facilitate understanding of the logic, the following explanation of memory address allocation and I/O instruction operation is included.

ROM 2 (E33 and E39)
Memory addressing space spans locations 0 through 777.

ROM 1 (E3 and E21)
Memory addressing space spans locations 4000 through 4777.

RAM (E11 and E27)
Memory addressing space spans locations 20000 through 20017.

The two bus control signals provided by the microprocessor and latched with the upper byte of the address register, KY1 PC FUN 0 H and KY1 PC FUN 1 H, determine data transfer direction and I/O operations. The following table explains the decoding of these signals.

PC FUN 0	PC FUN 1	
L	L	Memory read of first byte of instruction only (fetch)
L	H	Memory read of additional bytes of instruction or data.
H	H	Memory write (used only to write into RAM).
H	L	I/O operation

Memory reads and writes signify that the address register (KY1 ADRD 0 H through KY1 ADRD 13 H) contains the address of the location in memory to be accessed.

The code for I/O operations, however, signifies a very different situation. This is due to the following occurring after the initial instruction fetch cycle:

1. During TS1 the content of the A register (accumulator) in the microprocessor is available on the data lines and is latched into the low byte of the address register.

2. During TS2 the content of the instruction register (containing the I/O instruction) is available on the data lines and is latched into the high byte of the address register.

3. During TS3 of an INP (input) instruction, data on the data lines is loaded into the A register. On OUT (output) instructions, the data is strobed out of the low byte of the address register.

   I/O Instruction Code:

   INP 01 OOMMM1
   OUT 01 RRMMM1

Note that the two most significant bits of the instruction will correspond to PC FUN 0 = 1 and PC FUN 1 = 0 when loaded into the high byte of the address register, thus denoting an I/O operation. Therefore, the data bus control logic determines whether to gate data into the microprocessor during TS3 (INP) or to load the data from the low byte of the address register into an output port during TS3 (OUT).

The 32 × 8 PROM (E34) does the initial decoding of the type of transfer (read, write, or I/O) from the signals KY1 PC FUN 0 H and KY1 PC FUN 1 H. If the transfer is a memory read or write, it is decoded into one of the following four signals. KY4 RAM → DIN BUS L (RAM read), KY4 ROM 1 EN L (memory read in address range 4000–4777), KY4 ROM 2 EN L (memory read in address range 000–777), and an enable which is ANDed with KY1 SYNC H, KY1 TS3 L, and KY1 CK2 L to provide a write pulse, KY4 RAM WRITE H, to the RAM.

Another enable from the PROM is ANDed with KY1 TS3 L to provide the signal KY4 DIN DRIVER DIS H. This signal is normally high, disabling the driver portions of the 8833 transceivers (E16 and E17). It will be low only during TS3 and when data transfer is into the microprocessor.

Two other outputs of the PROM are used for I/O operations. One output of the PROM (E34-7), when low, enables the 74154 4-to-16 decoder on all I/O instructions. The second output (E34-9) determines whether the I/O instruction is INP or OUT. If the instruction is OUT, then the signal will be high.

Note that address register bits KY1 ADRD 11, KY1 ADRD 10 H, and KY1 ADRD 9 H, are applied to the low order inputs of the 74154. This selects which of the possible ports will be used. The fourth input, the highest order input, determines if it is an INP or OUT instruction. This input is the ANDed condition of the PROM output (E34-9), KY1 SYNC H, KY1 TS3, and KY1 CK2. Thus, if the instruction is an INP, then the input gating signal will be one of the lower order eight outputs of the 74154 (KY4 READ IN 0 L through KY4 READ IN 7 L).

If the PROM signal (E34-9) is high, signifying an OUT instruction, then initially a low order output is selected (does not substantially affect anything) and then a high order output will be pulsed as the gated clock pulse is applied to the high order input of the 74154. Thus, the high order outputs are pulsed and buffered to provide loading pulses to the selected registers (KY4 LD REG 0 H, etc.).

5.3.12 Unibus Control (Drawing CS M7859, Sheet 5)

Unibus control is accomplished via two 74175 quad, D-type, double rail output latches, E52 and E64. The stored program input bit configurations are read in under control of an appropriate data bus control signal, LD REG 5 H. E64 D2 and D3 latches are utilized for the manual clock enable and manual clock lines while the other six lines are Unibus control signals.

5.3.13 Keypad Scan Logic (Drawing CS 5411800-0-1)

The logic and driving circuitry for the keypad and display elements is located on a circuit board in the rear of the programmer's console panel.

Scan signals for the keypad are generated at the interface module (bus address register). These six lines (KY6 SCAN 1 L through KY6 SCAN 6 L) are then routed through hex 7417 buffer drivers to the console circuit board where they are designated as READ and DRIVE signals. As indicated by CS 5411800-0-1, sheet 2, READ 1 through READ 5 signals continuously scan the keypad in groups of 4. As each READ signal is applied to check for a pressed key, a corresponding DRIVE signal is simultaneously generated and applied to the appropriate transistor in the LED display circuitry (CS 11800-0-1, sheet 3).

A pressed key thus results in activation of 1 to 4 lines. This information is routed out through J1 to the interface module and applied to the data bus for eventual read-in to the miroprocessor.

5.3.14 Indicator Logic (Drawing CS M7859, Sheet 5)

The indicator control consists of a single quad, D-type, latch configuration, 74175 (E68) and four 7417 open collector inverters (E69) for driving the panel indicators. Input bit coding KY1 ADRD 4 H through KY1 ADRD 7 H via the stored program determines which of the following panel indicators are turned on:

1. BUS ERR
2. SR DISP
3. MAINT
4. BOOT

5.3.15 Halt Logic (Drawing CS M7859-0-1, Sheet 9)

The halt logic allows the console to obtain control of the Unibus in order to perform Unibus transactions. Control of the Unibus is passed to the KY11-LB from the PDP-11 processor via a HALT REQUEST and HALT GRANT sequence. Use of the HALT/SS key initiates a program sequence within the KY11-LB to issue a HALT REQUEST to the PDP-11 processor. The procesor will arbitrate the request and at the appropriate time will respond with HALT GRANT. The reception of HALT GRANT H by the halt logic direct sets the HALT SACK flip-flop on E63-4, causing BUS SACK L to be generated at E62-13. The set output of the HALT SACK flip-flop (E63-5) sets up the data input of the HALT BUSY flip-flop (E63-12).

The reception of BUS SACK L by the PDP-11 processor will cause it to drop HALT GRANT H. When the Unibus becomes free (unasserted BUS BUSY L and BUS SSYN L), the E63-11 will be clocked, setting the HALT BUSY flip-flop. This, in turn, asserts BUS BUSY L through E62-10 and causes the RUN indicator to be turned off via the 7417 buffer (E66-12). This logic operates in the same manner if the HALT GRANT is generated not by a HALT REQUEST from the KY11-LB but by a HALT instruction in the PDP-11 processor. The output of the HALT BUSY flip-flop (KYB HALT BUSY H) can be tested by the microprocessor program to check if the console has control of the Unibus before performing Unibus transactions.

The HALT SACK and HALT BUSY flip-flops are direct cleared by either BUS INIT L from the Unibus or by the signal KY4 CLR BUS L which can be generated by the microprocessor program. Clearing these flip-flops relinquishes control of the Unibus to the PDP-11 processor.

The signal KY4 TAKE BUS L, which can direct set the HALT BUS flip-flop, allows the microprocessor program to perform Unibus operations without first obtaining the Unibus through a legal request. This signal is only used during maintenance mode operation of the KY11-LB to bypass a failing or hung processor.

5.3.16 Buffers (Drawing CS M7859, Sheet 4)

5.3.16.1 Tristate Buffers (8093) – The following units, which are gated by read input signals from the data bus control, buffer input data from several sources.

1. Unibus Data
2. Unibus Address
3. Keypad Register
4. Maintenance Inputs (from processor microprogram counter).

Outputs from the 8093s are wire ORed and sent to the tristate transceivers with the ROM and RAM data as KY2 DIN 0 H through KY2 DIN 7 H.

5.3.16.2 Tristate Transceivers (8833) – These units buffer data between the microprocessor bidirectional data bus and the satellite logic of the interface module.

CHAPTER 6
CONSOLE MODE OPERATION

6.1 INTRODUCTION

This chapter is a recapitulation of all console key and indicator functions. Operation, use, and examples of the utilization of each key are presented. Key operations are divided into console mode and maintenance mode. Examples of console sequences to demonstrate the proper use of the KY11-LB are presented together with further notes and hints on operation.

6.2 CONSOLE KEY OPERATIONS

This section describes the operation of each key in a step-by-step procedure. The reader is assumed to have read earlier chapters as some descriptions include the use of keys previously described.

A notation for each key will be introduced in each description and is enclosed in angle brackets < >. These notations are used extensively in Paragraph 6.4 to describe various sequences of key operations.

<CLR> – Used to clear an incorrect entry or existing data.

1. Press and release the CLR key.
2. The display (six digits) will be all zeros.
3. Clears the SR DISP, BUS ERR, or MAINT indicators if on.

Numerics 0–7 – Used to key in an octal numeric digit (0 through 7).

1. Press a numeric key (0 through 7).
2. The corresponding digit will be left shifted into the 6-digit octal display with the previously displayed digits also being left shifted.
3. Release the numeric key.

To enter the number <xxxxxx>, e.g., 123456:

1. Press and release the CLR key (000000 will be displayed).
2. Press and release the 1 key (000001 will be displayed).
3. Press and release the 2 key (000012 will be displayed).
4. Press and release the 3 key (000123 will be displayed).
5. Press and release the 4 key (001234 will be displayed).
6. Press and release the 5 key (012345 will be displayed).
7. Press and release the 6 key (123456 will be displayed).

The number has now been entered. Leading zeros do not have to be entered.

<LSR> – Used to load the switch register (accessible as Unibus address 777570).

1. Press and release the LSR key.
2. The display will show the data loaded and the SR DISP indicator will be on.

To load the number 777 i.e., <LSR 777>, into the switch register:

1. Press and release the CLR key.
2. Key in the number 777.
3. Press and release the LSR key.
4. 777 will be displayed and the SR DISP indicator will be on.

<LAD> – Used to load the Unibus address pointer prior to performing an EXAMINE, DEPOSIT, or START.

1. Press and release the LAD key.
2. Display will be all zeros.

To load address 200, i.e., <LAD 200>:

1. Press and release the CLR key.
2. Key in 200.
3. Press and release the LAD key.
4. Display is all zeros.

<DIS AD> – Displays the current contents of the Unibus address pointer.

1. Press and release the DIS AD key.
2. Display will show the current Unibus address pointer.

To perform the sequence:

LAD 400
DIS AD

1. Press and release the CLR key.
2. Key in 400.
3. Press and release the LAD key (display is all zeros).
4. Press and release the DIS AD key.
5. Display shows the 400 from the Unibus address pointer.

<DEP> – Used to deposit a number into the location pointed to by the Unibus address pointer.

1. Processor must be halted (RUN indicator off); otherwise key is ignored.
2. Press and release the DEP key.
3. Display shows the data deposited.

To deposit <DEP xxxx> (e.g., 5252) into location 1000, the sequence is as follows:

```
LAD 1000
DEP 5252
```

1. Press and release the CLR key.
2. Key in 1000.
3. Press and release the LAD key.
4. Key in 5252.
5. Press and release the DEP key.

<EXAM> – Used to examine the contents of a location pointed to by the Unibus address pointer.

1. Machine must be halted.
2. Press and release the EXAM key.
3. Display shows the contents of the location examined.

To examine general-purpose register R7 (program counter) at Unibus address 777707, the following sequence is used:

```
LAD 777707
EXAM
```

1. Press and release the CLR key.
2. Key in 777707.
3. Press and release the LAD key.
4. Press and release the EXAM key.
5. The contents of R7 will be displayed.

<CNTRL> – The CNTRL key is always used in conjunction with some other key. When it is used it must be pressed and held down while the second key is pressed and released.

<CNTRL–HLT/SS> – Used to halt the processor.

1. Press and hold down the CNTRL key.
2. Press and release the HLT/SS key.
3. Display will show the current contents of R7 (program counter) and the RUN indicator will be off.
4. Release the CNTRL key.

If the processor is already halted, the use of the HLT/SS key will single-instruction step the processor. (The CNTRL key is not required to single-instruction step the processor once halted.)

1. Press and release the HLT/SS key.
2. Processor will perform one instruction and halt.
3. Display will show the new current contents of R7 (program counter).

<CNTRL-CONT> - Used to allow the processor to begin running from a halt.

1. Press and hold down the CNTRL key.
2. Press and release the CONT key.
3. Processor will run unless a program halt instruction is encountered. The RUN and SR DISP indicators should be on and the contents of the switch register should be displayed. If a halt instruction was encountered, the indicators will be off and the program counter will be displayed.
4. Release the CNTRL key.

NOTE

If the processor is already running, use of <CNTRL-CONT> will result in the switch register being displayed; there will be no other effect on the processor.

<CNTRL-BOOT> - Used to initiate running of M9301 Bootstrap program.

1. Processor must be halted.
2. Press and hold down the CNTRL key.
3. Press and release the BOOT key.
4. Processor should start running (RUN indicator on) the bootstrap program selected on the M9301.

NOTE

For more information concerning the M9301 Bootstrap program, consult the system users guide.

5. Release the CNTRL key.

<CNTRL-START> - Used to start the processor running a program from a given starting address.

1. Processor must be halted; otherwise key is ignored.
2. Press and hold down CNTRL key.
3. Press and release the START key.
4. RUN indicator will be on unless a halt instruction is encountered. The SR DISP indicator should also be on and the contents of the switch register should be displayed.
5. Release the CNTRL key.

To start running a program at location 1000, the following sequence is used:

1. Press and release the CLR key.
2. Key in 1000.
3. Press and release the LAD key.
4. Press and hold down the CNTRL key.
5. Press and release the START key.
6. Release the CNTRL key.

<CNTRL-INIT> - Generates a Bus Initialize without the processor starting.

1. Processor must be halted.
2. Press and hold down the CNTRL key.
3. Press and release the INIT key.
4. Bus Initialize will be generated for 150 ms.
5. Release the CNTRL key.

<CNTRL-7> – Used to calculate the correct address when a mode 6 or 7 register R7 instruction is encountered.

1. Press and hold down the CNTRL key.
2. Press and release the 7 key.
3. Display will show the new temporary register which contains the old temporary register plus the Unibus address point or plus 2.

See Paragraph 6.4 for an example.

<CNTRL-6> – Used to calculate the offset address when mode 6 or 7 instructions other than register R7 are encountered.

1. Press and hold down the CNTRL key.
2. Press and release the 6 key.
3. Display shows the new temporary register, which contains the old temporary plus the switch register.
4. Release the CNTRL key.

See Paragraph 6.4 for an example.

<CNTRL-1> – Used to enter the console into maintenance mode. Maintenance mode should only be used as an aid to troubleshooting hardware problems. Maintenance mode provides no help in debugging software problems.

1. Press and hold down the CNTRL key.
2. Press and release the 1 key.
3. MAINT indicator will be on and the MPC (microprogram counter) will be sampled and displayed.
4. Release the CNTRL key.

6.3 NOTES ON OPERATION

An erroneous display will result if, while the processor is running and the switch register is being displayed, a numeric key is pressed. Although the SR DISP indicator will remain on, the display no longer reflects the actual contents of the switch register. If at any time while the processor is running, it is desired that the switch register contents be displayed, the CNTRL–CONT keys should be used.

As a general practice, prior to entering a new 6-digit number and if the display is nonzero, the CLR key should be used to initially zero the display.

In order to single-instruction step the processor from a given starting address, the program counter (R7) must be loaded with the starting address using the Unibus address of R7 (777707) i.e., to single-instruction step from the beginning of a program starting at location 1000, the following sequence is necessary:

```
LAD 777707
DEP 1000
CNTRL–INIT (if desired)
HLT/SS
HLT/SS
etc.
```

The console requires an 18-bit address. This is especially important to remember when accessing device registers (i.e., 777560 instead of 177560). Otherwise an erroneous access to memory or to a nonexistent address will occur.

The Unibus addresses for the general-purpose registers can only be used by the console. A PDP-11 program using the Unibus addresses for the general-purpose registers will trap as a nonexistent address. Also, internal registers R10 through R17, which are used for various purposes (depending upon processor), may be accessed by the console through Unibus addresses 777710 through 777717.

The BUS ERR indicator on the console reflects a bus error by the console only. The indicator will not reflect bus errors due to other devices succh as the processor.

6.4 EXAMPLES OF CONSOLE SEQUENCES

This section combines key operations with example sequences to demonstrate the proper use of the KY11-LB Programmer's Console.

The following sequences use the notations for key operations as described in Paragraph 6.2.

The angle brackets < > will be used in the sequences to identify the display contents after the operation is performed, i.e., LAD 200 <0>

1. Press and release the CLR key.
2. Press and release 2 key.
3. Press and release 0 key.
4. Press and release 0 key.
5. Press and release the LAD key.
6. 000000 will be displayed in the 6-digit readout.

Example 1

This sequence uses the examine function and the switch register Unibus address 777570 to read the contents of the switch register.

LSR 123456	<123456>
LAD 777570	<0>
EXAM	<123456>
DIS AD	<777570>
LSR 777	<777>
EXAM	<777>

Example 2

This sequence demonstrates the use of the following keys: LAD, DIS AD, LSR, EXAM, DEP, CNTRL-START, CNTRL-CONT, and CNTRL-HLT/SS.

This example loads the following program into memory, which is then run to demonstrate various operations.

Program	**Memory Location/Contents**
1000/13737	;Move the contents of
1002/177570	the switch register to
1004/1014	memory location 1014
1006/0000	;Halt
1010/137	;Jump to location 1000
1012/1000	
1014/0000	

Sequence

LAD 1000	<0>
DEP 13737	<13737>
DEP 177570	<177570>
DEP 1014	<1014>
DEP 0	<0>
DEP 137	<137>
DEP 1000	<1000>
DEP 0	<0>
LAD 1000	<0>
EXAM	<13737>
EXAM	<177570>
EXAM	<1014>
EXAM	<0>
EXAM	<137>
EXAM	<1000>
EXAM	<0>
DIS AD	<1014>
LSR 123456	<123456>
LAD 1000	<0>
CNTRL-START	<1010>
LAD 1014	<0>
EXAM	<123456>
DEP 0	<0>
EXAM	<0>
DIS AD	<1014>
LSR 125252	<125252>
CNTRL-CONT	<1010>
LAD 1014	<0>
EXAM	<125252>
DEP 0	<0>
LAD 1006	<0>
DEP 240	<240>
EXAM	<240>
LAD 1000	<0>
CNTRL-START	<125252>
LSR 70707	<10707>
CNTRL-HLT/SS	
LAD 1014	<0>
EXAM	<10707>
HLT/SS	
HLT/SS	
HLT/SS	
•	
•	
•	
LSR 05252	<052525>
HLT/SS	
LAD 1014	<0>
EXAM	<052525>

Example 3
This sequence demonstrates the use of CNTRL-7 and CNTRL-6. The following data are loaded into memory:

1000/177
1002/100
1004/000
1006/5060
1010/1020

1104/1006

RO = 777760

The sequence to load the data is as follows:

LAD 1000	<0>
DEP 177	<177>
DEP 100	<100>
DEP 0	<0>
DEP 5060	<5060>
DEP 1020	<1020>
LAD 1104	<0>
DEP 1006	<1006>
LAD 777700	<0>
DEP 777760	<777760>

Sequence

LAD 1000	<0>
EXAM	<177>
EXAM	<100>
CNTRL-7	<1104>
LAD	<0>
EXAM	<1006>
LAD	<0>
EXAM	<5060>
EXAM	<1020>
LSR	<1020>
LAD 777700	<0>
EXAM	<777760>
CNTRL-6	<100006>
LAD	<0>
EXAM	<177>

CHAPTER 7
MAINTENANCE MODE OPERATION

7.1 INTRODUCTION

This chapter covers the keypad facilities of the programmer's console available for hardware maintenance of the processor.

7.2 MAINTENANCE MODE KEY OPERATIONS

The following definitions apply to a subset of the same keys used in console mode; however the functions and operations differ from those in console mode. In general, console mode functions are not available while in maintenance mode, and many keys have no function in maintenance mode.

NOTE

Maintenance mode operation is indicated by the MAINT indicator being on.

In order to use the hardware maintenance features available in maintenance mode, the maintenance cable (11/04) or cables (11/34) must be connected between the KY11-LB interface board (M7859) and the corresponding processor board (M7263-11/04, M7266-11/34, M8266-11/34A, or M8267-FP11A). An exception to this is the 5 (maintenance mode) operation which allows the console to examine or deposit into memory or device registers without the processor being either present or functional.

DIS AD (Maintenance Mode) – Used to display Unibus address lines.

1. Press and release the DIS AD key.
2. Unibus address lines will be sampled (read once) and displayed, i.e., display will not be updated as address lines change.

EXAM (Maintenance Mode) – Used to display Unibus data lines.

1. Press and release the EXAM key.
2. Unibus data lines will be sampled and displayed.

HLT/SS (Maintenance Mode) – Asserts manual clock enable and displays MPC (microprogram counter).

1. Press and release the HLT/SS key.
2. Manual clock enable will be asserted.
3. MPC will be sampled and displayed.

CONT (Maintenance Mode) – Single microsteps the processor through one microstate and displays the MPC.

1. Press and release the CONT key.
2. Manual clock will be pulsed.
3. New MPC will be sampled and displayed.

BOOT (Maintenance Mode) – Boots the M9301. If manual clock enable is asserted, the M9301 routine will not be entered but because the M9301 simulates a power fail the processor will power up through location 24.

1. Press and release the BOOT key.
2. The display is not affected. If manual clock enable is asserted, the MPC is now at the beginning of the power-up sequence. To see the new MPC, use the HLT/SS key.

START (Maintenance Mode) – Drops manual clock enable.

1. Press and release the START key.
2. Manual clock enable is released.
3. MPC will be sampled and displayed.

CLR (Maintenance Mode) – Returns console to console mode operation.

1. Press and release the CLR key.
2. MAINT indicator is off.
3. Processor should halt.
4. Program counter should be displayed.

5 (Maintenance Mode) – Allows the console to take control of the Unibus if a processor is not in the system.

1. Press and release the 5 key.
2. The MAINT indicator will be off (console mode operation now).
3. Console attempts to read the program counter which is not present and therefore the BUS ERR indicator will be on.

7.3 NOTES ON OPERATION

If the single-microstep feature in maintenance mode is to be used, it is preferable that the processor be halted prior to entering maintenance mode, if it is possible. This is because the assertion of manual clock enable, which turns off the processor clock if it is running, cannot be synchronized with the processor clock. Therefore, if the processor is not halted, the clock may be running and the assertion of manual clock enable may cause an erroneous condition to occur.

In order to single-microstep the processor from the beginning of the power-up sequence, the following steps may be used:

1. Halt the processor if possible.
2. Use CNTRL 1 to enter maintenance mode.
3. Use HLT/SS to assert manual clock enable (RUN indicator should come on).
4. Use BOOT to generate a simulated power-fail (will not work if M9301 is not present in the system).

5. Use HLT/SS to display the MPC (microprogram counter) for the first microstep in the power-up routine.

6. Use CONT to single-microstep the processor through the power-up routine. (The new MPC will be displayed at each step.)

7. Unibus address lines and Unibus data (see NOTE below) lines may be examined at any microstep by using DIS AD and EXAM, respectively. Use of these keys does not advance the microprogram. To redisplay the current MPC without advancing the microprogram, use the HLT/SS key.

8. To return from maintenance mode, use the CLR key.

9. To single-microstep through a program, the program counter (R7) must first be loaded with the starting address of the program as in single-instruction stepping the processor prior to entering maintenance mode.

NOTE

Because the data transfer occurs asynchronously with the processor clock, Unibus data will not be displayed on DATI in maintenance mode when using the console with an 11/04 processor. Unibus data on DATO on the 11/04 and both DATI and DATO on the 11/34 will be displayed.

Due to hardware changes, the M8266 module will gate the AMUX lines onto the Unibus when manual clock enable is asserted and a Unibus transaction is not occurring.

CHAPTER 8
KY11-LB MAINTENANCE

8.1 PRELIMINARY CONSIDERATIONS

The following is a guide to locating possible problems on the KY11-LB.

1. Power Switch Failure – If the power switch fails to control the power supply, check cable 7011414-2-2 (BA11-L) at J2 or cable 7011992-0-0 (BA11-K) at Faston tabs TB4 and TB5 on the bezel-mounted board to ensure that cable(s) are securely and correctly installed.

2. If the power switch does turn on the power supply (fans turn) but the DC ON indicator does not come on, check cable 7011992-0-0 (BA11-K) at tabs TB6 and TB7 on the bezel-mounted board.

3. If the four indicators on the left side of the keypad are all on, then the cable 7012214-0-0 connecting the bezel-mounted board to the interface board (M7859) is probably plugged in backward on one end.

4. If no display and none of the four indicators are on, then check cable 7012214-0-0 at J1 on the bezel-mounted board and M7859 board to ensure that it is correctly and securely installed.

5. Note that there should be no cables from either the bezel-mounted board or the M7859 board attached to the backplane. The connection at the backplane is for use by the KY11-LA Operator Console only.

6. If the RUN indicator is on but there is no display and no response from the keypad, the problem is probably at the M7859 Interface module. Check the module to ensure that the microprocessor chip (E18) is securely installed in its socket.

7. If the display works and the console responds to the keypad except for the BOOT key, check that cable 7011413-0-0 is properly connected to the M9301 and to the bezel-mounted board at tabs TB1 and TB2.

8. If the display MPC, single microstep, etc. functions in maintenance mode do not work correctly, check that the cable(s) from J2 and J3 of the M7859 are properly installed.

NOTE

These cables should be installed only for maintenance of the processor. By disconnecting these cables for normal operation, the effect is that the maintenance functions are nonoperative except for the TAKE BUS function.

8.2 M7859 FAILURES

In general, there are two levels of possible failures on the M7859 module. The first level and most difficult to fix is the microprocessor and its support logic which constitutes about 1/3 of the logic. The second level is failures which occur in the peripheral logic constituting the Unibus interface and the display/keypad interface. These are generally easier to troubleshoot.

Generally, a first level failure is readily apparent and will usually be indicated when no display is on and the only indicators on are DC ON and RUN.

A second level failure, although easier to troubleshoot, is not always readily apparent as it may only occur on certain key functions or may be data dependent. A failure on the display/keypad interface would be indicated by odd displays, row, or column failures on the keypad. The Unibus interface can be tested with a good confidence level by loading the switch register with a 123456 data pattern and then reading it back over the Unibus by examining location 777570.

The following is a guide to troubleshooting a failing M7859 module. Generally, the minimum equipment needed is a dual-trace oscilloscope with delayed sweep.

1. Check that 9 V is available at pin 1 of the microprocessor, E18.

2. Check that the clock frequency is 1.0 MHz ± 2% at the test point, TP1. The frequency can be corrected if needed by adjusting the variable resistor at the top of the module.

3. Check that the two clock signals are at E18-15 and E18-16. These clocks should be 500 kHz frequency with nonoverlapping positive pulses of 0.5 ms duration (Figure 8-1).

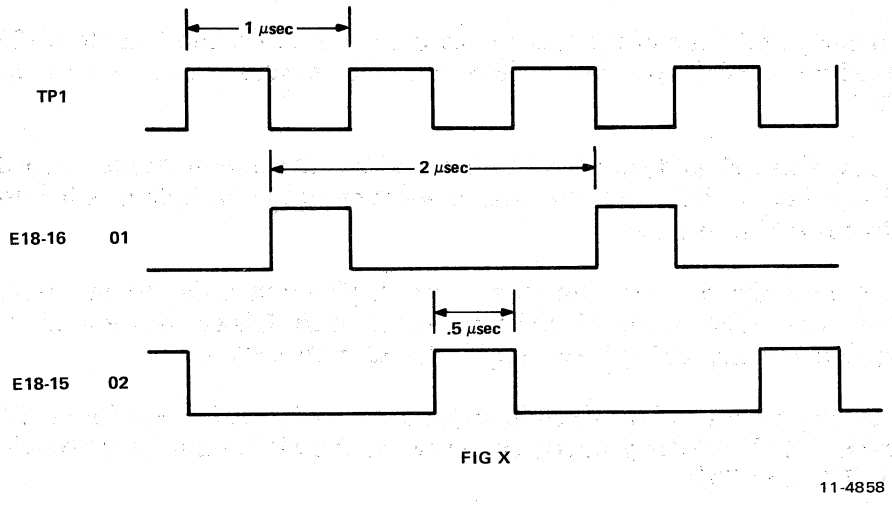

Figure 8-1 Clock Waveforms

4. Check the signal at E18-18 which should be at logic low. If the signal is high the microprocessor may not have responded to the interrupt request on power-up. If the signal is toggling, this may be indicative of a different class of problems discussed in the following paragraphs.

5. The M7859 logic is such that if the microprocessor encounters a HALT instruction and goes to the STOP state, peripheral logic will automatically try to restart the microprocessor from location 0. Hence, if there are problems in the microprocessor support logic, such as address or data failures, time state decoding failures, etc., the microprocessor will not follow the program and generally encounters a HALT instruction.

   The general technique to solve this class of problems is to sync off of the signal STOP L and to use delayed sweep to track addresses backward to find the specific failing address. A quick check of the number of times TS1 L is true between the times that STOP L is true will give an idea of how far into the program the failure occurs. In general the easiest technique is to use the TS3 L signal as a visual key on one channel while using the other channel to probe addresses, data, timing signals, etc.

CHAPTER 9
KY11-LB INSTALLATION

9.1 KY11-LB DESCRIPTION

The KY11-LB is a programer's console option for both the 11/04 and 11/34 CPUs. It replaces the KY11-LA (operator's console) which is the standard console on 11/04s and 11/34s. The hardware in the KY11-LB option is exactly the same for both the 11/04 and 11/34. The KY11-LB contains a bezel assembly (consisting of a keypad, 7-segment display, indicator lamps, and ON/OFF switch) and a separate SPC quad interface module (M7859). Also, three loose piece cables: two 10-conductor, 45.7 cm (18 inch) long cables and one 20-conductor cable. The two 10-connector cables are not required for normal console functions and should only be installed when using the console in maintenance mode.

9.2 CPU BOX TYPE

PDP-11/04s and 11/34s are available in both the BA11-L 13.4 cm (5-1/4 inch) box and BA11-K 26.7 cm (10-1/2 inch) box. The difference between these two boxes creates the only difference in installing the KY11-LB. In all cases, the 10-conductor cable, running from the operator's console to the CPU backplane, is not used and must be removed when the KY11-LB is installed. It is extremely important not to connect this cable to the KY11-LB as a short circuit may result.

9.3 CPU DIFFERENCES

The 11/04 is a single-module CPU (M7263). The 11/34 is a 2-module CPU (M7265 and M7266). Maintenance mode connections between KY11-LB and 11/04 are made on the M7263. Maintenance mode connections between KY11-LB and 11/34 are made on the M7266 (Figures 9-1 and 9-2). Note that all figures in this procedure show the M7266 module (11/34). This is done because the hook-up for normal KY11-LB operation is the same for both CPUs.

To identify cables and part numbers for cables, refer to Figure 9-3.

9.4 BA11-L 13.3 CM (5-1/4 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connections will be to the same tabs on the KY11-LB. The cable from H777 Power Supply plugged into J2 on the KY11-LA will plug into J2 on the KY11-LB. The cable from the CPU backplane to J1 on the KY11-LA must be removed. No connection is made from the backplane to the KY11-LB.

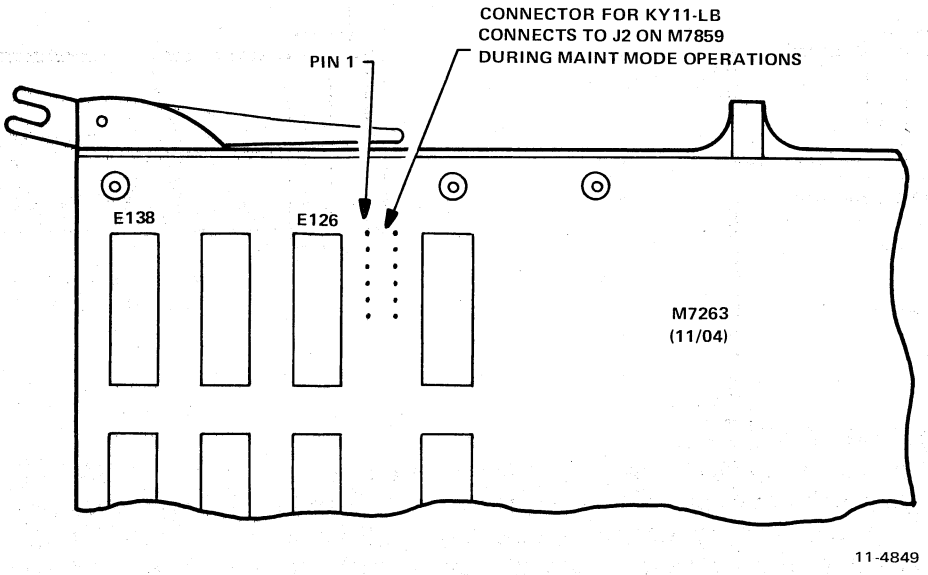

Figure 9-1 M7263

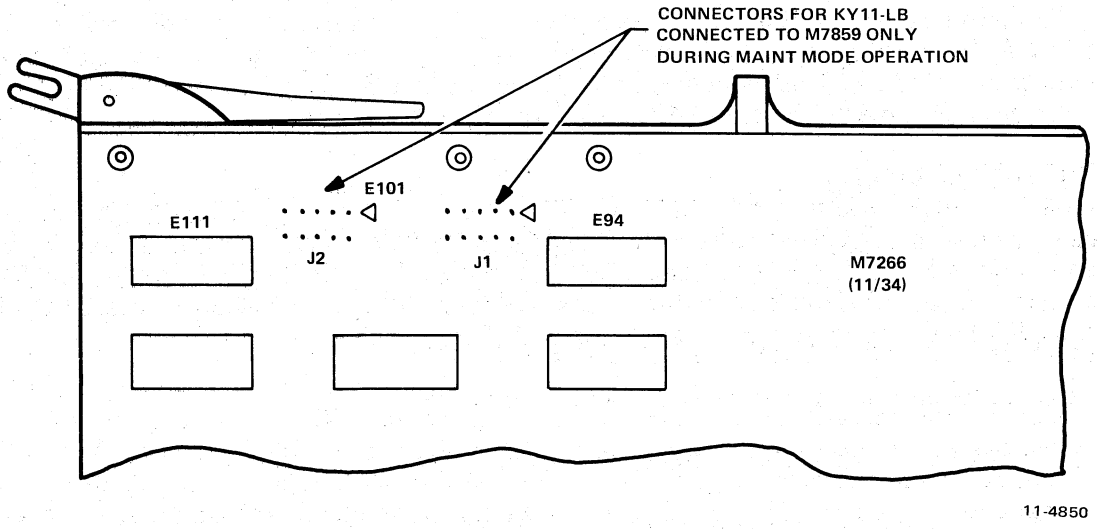

Figure 9-2 M7266

CHAPTER 9
KY11-LB INSTALLATION

9.1 KY11-LB DESCRIPTION

The KY11-LB is a programer's console option for both the 11/04 and 11/34 CPUs. It replaces the KY11-LA (operator's console) which is the standard console on 11/04s and 11/34s. The hardware in the KY11-LB option is exactly the same for both the 11/04 and 11/34. The KY11-LB contains a bezel assembly (consisting of a keypad, 7-segment display, indicator lamps, and ON/OFF switch) and a separate SPC quad interface module (M7859). Also, three loose piece cables: two 10-conductor, 45.7 cm (18 inch) long cables and one 20-conductor cable. The two 10-connector cables are not required for normal console functions and should only be installed when using the console in maintenance mode.

9.2 CPU BOX TYPE

PDP-11/04s and 11/34s are available in both the BA11-L 13.4 cm (5-1/4 inch) box and BA11-K 26.7 cm (10-1/2 inch) box. The difference between these two boxes creates the only difference in installing the KY11-LB. In all cases, the 10-conductor cable, running from the operator's console to the CPU backplane, is not used and must be removed when the KY11-LB is installed. It is extremely important not to connect this cable to the KY11-LB as a short circuit may result.

9.3 CPU DIFFERENCES

The 11/04 is a single-module CPU (M7263). The 11/34 is a 2-module CPU (M7265 and M7266). Maintenance mode connections between KY11-LB and 11/04 are made on the M7263. Maintenance mode connections between KY11-LB and 11/34 are made on the M7266 (Figures 9-1 and 9-2). Note that all figures in this procedure show the M7266 module (11/34). This is done because the hook-up for normal KY11-LB operation is the same for both CPUs.

To identify cables and part numbers for cables, refer to Figure 9-3.

9.4 BA11-L 13.3 CM (5-1/4 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connections will be to the same tabs on the KY11-LB. The cable from H777 Power Supply plugged into J2 on the KY11-LA will plug into J2 on the KY11-LB. The cable from the CPU backplane to J1 on the KY11-LA must be removed. No connection is made from the backplane to the KY11-LB.

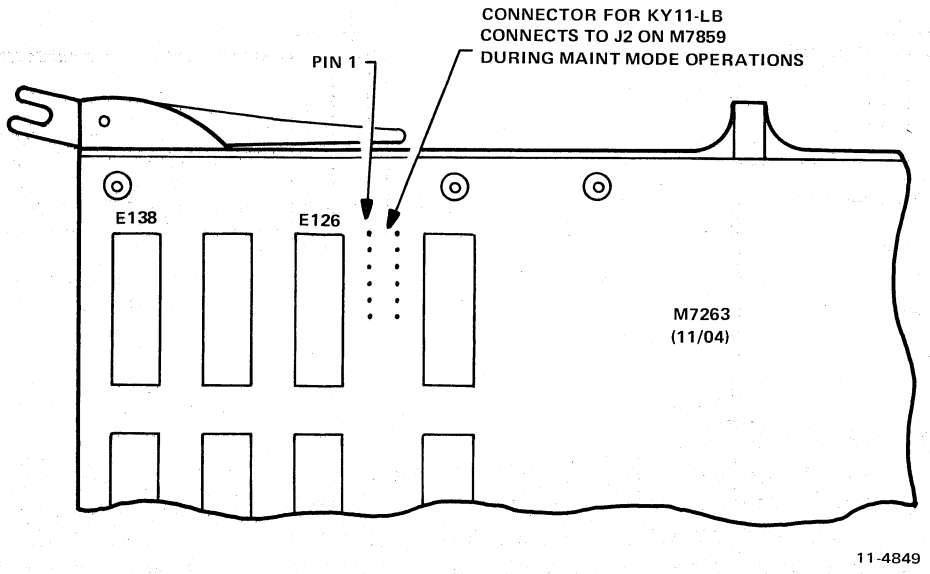

Figure 9-1 M7263

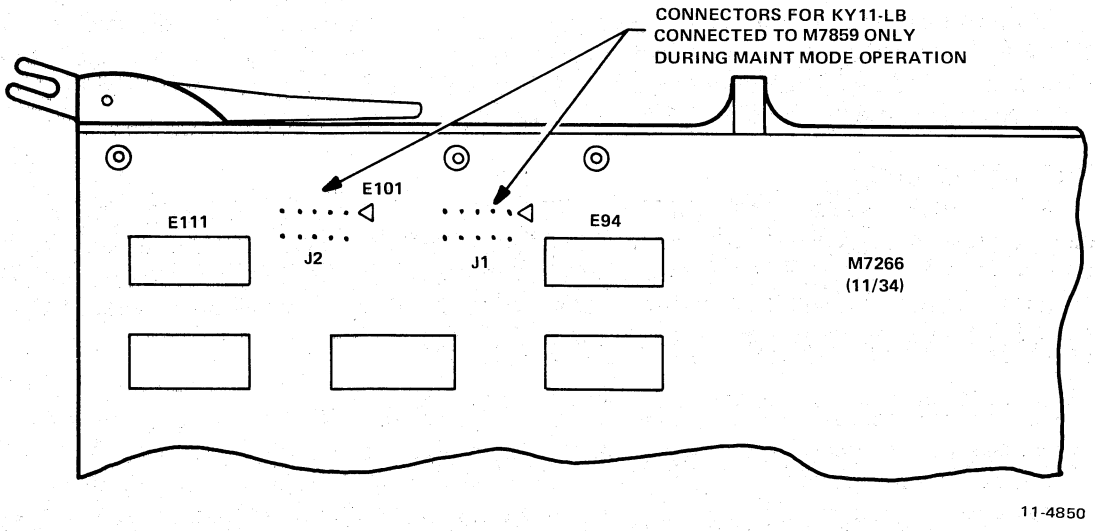

Figure 9-2 M7266

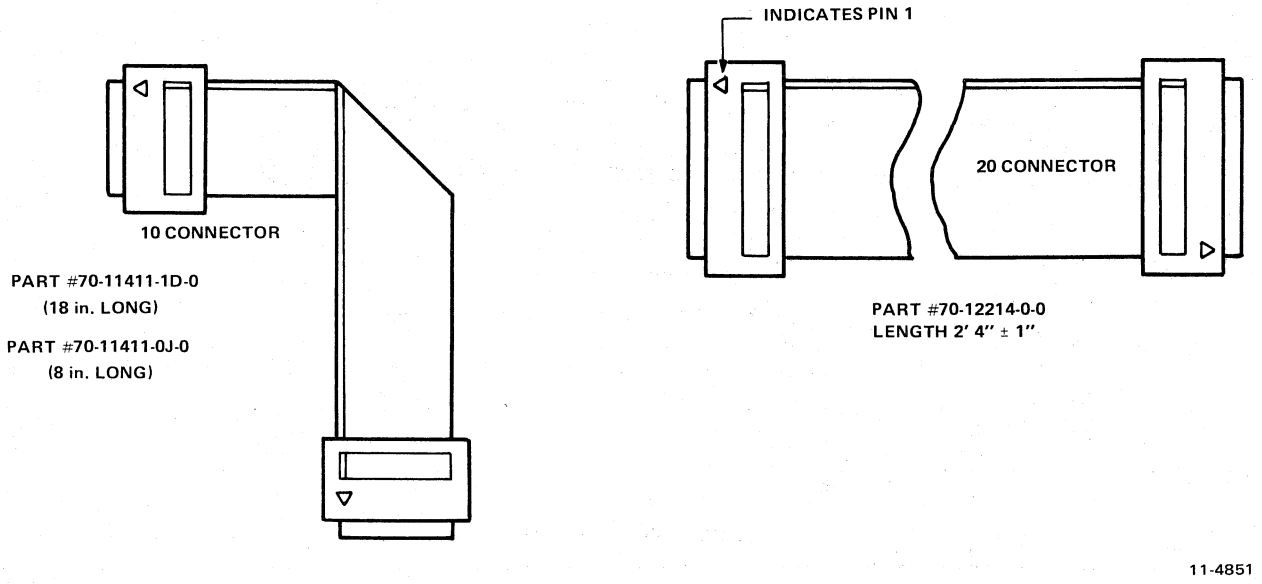

Figure 9-3 Cables

2. Install M7859 (KY11-LB interface) in any SPC slot (within CPU backplane) and connect it to the KY11-LB bezel as shown in Figure 9-4.

CONFIGURATION NOTE

The M7859 consumes 2A at +5 V and can only be plugged into the CPU backplane.

WARNING

When doing any reconfigurating of the CPU backplane that might be necessary to make room for the M7859, be sure that the M9302 is never installed in a modified Unibus slot (which results in short circuits).

9.5 BA11-K 26.7 CM (10-1/2 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connection will be the same tabs on the KY11-LB (Figure 9-5). You will notice that J2 on the operator's console is not used on the BA11-K box. The signals and voltages that come in on this jack in the BA11-L box come in on Faston tabs in the BA11-K box. The cable connecting the CPU backplane to J1 on the operator's console must be removed and no connection from the backplane to the KY11-LB is made.

2. Install M7859 (KY11-LB interface) in any SPC slot (with CPU backplane) and connect to KY11-LB bezel as shown in Figure 9-5.

WARNING

When doing any reconfigurating of the CPU backplane that might be necessary to make room for the M7859, be sure that the M9302 is never installed in a modified Unibus slot (which results in short circuits).

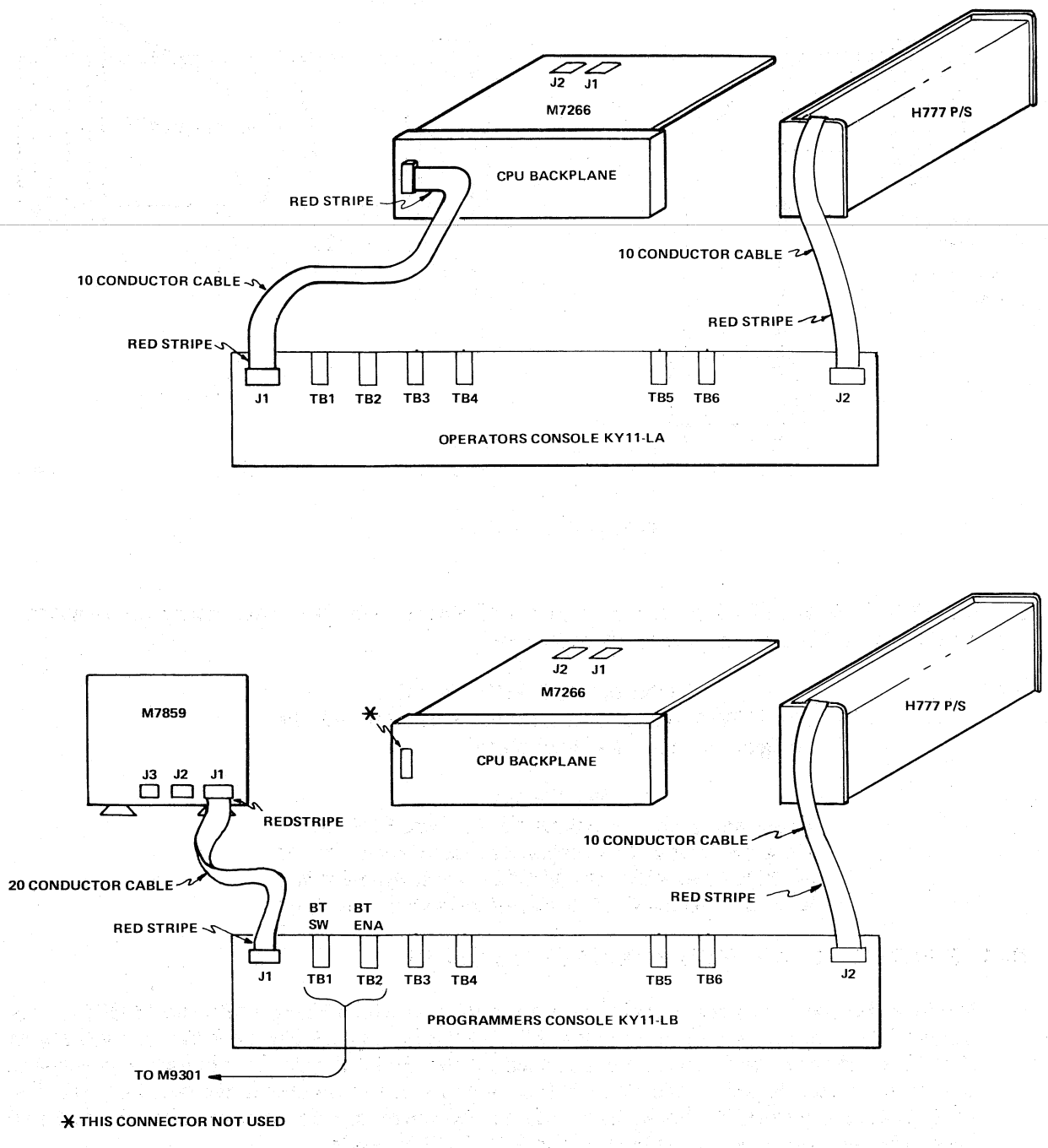

Figure 9-4 BA11-L

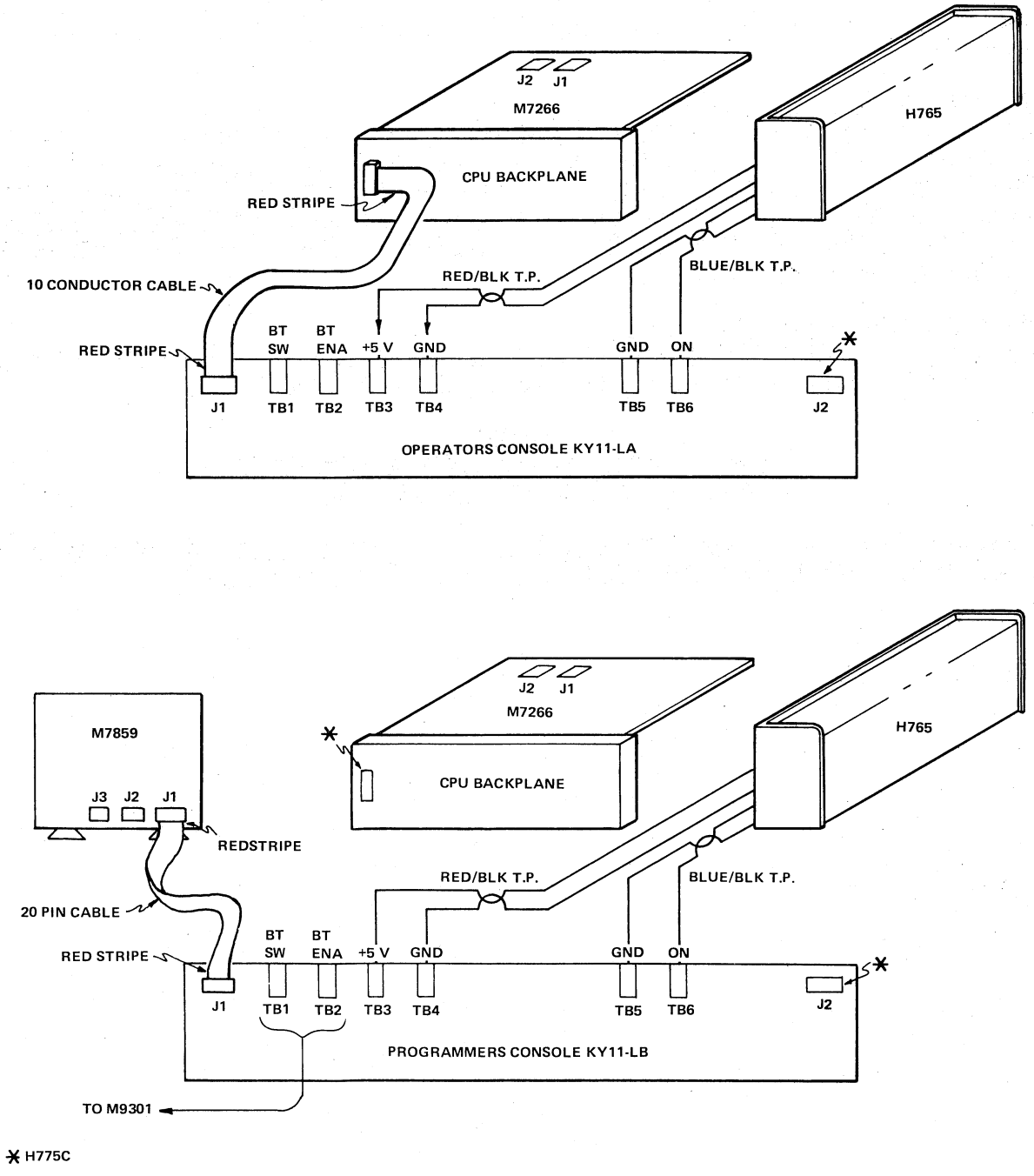

Figure 9-5 BA11-K

9.6 MAINTENANCE MODE HOOK-UP

To utilize the KY11-LB as a maintenance tool for troubleshooting the CPU or system, additional cable(s) must be installed. The 11/04 requires one additional cable and the 11/34 requires two additional cables.

PDP-11/04 (Maintenance Mode Cabling)

The 11/04 requires only one additional cable for maintenance mode operation. This 10-conductor cable (Part No. 70-11411-1D-0) connects J2 of the M7859 to the unmarked male connector on the M7263 (11/04 CPU). The cable (70-11411-1D-0) has a pointer on each end to indicate pin 1 as shown in Figure 9-3. Install the cable with the pointer on the end of the cable lined up with pin 1 on the CPU module (M7263). Pin 1 on M7263 is called out on Figure 9-1. Points on J2 (M7859) and the cable should also be lined up.

PDP-11/34 (Maintenance Mode Cabling)

The 11/34 requires two additional cables for maintenance mode operation. Both cables are the same and are the same part as is used on the 11/04. See Figure 9-3 for part number.

NOTE

Maintenance cables for both 11/04 and 11/34 are all 45.7 cm (18 inch) long, 10-conductor cables.

When installing maintenance cables connect J2 (M7859) to J1 (M7266) and J3 (M7859) to J2 (M7266). The pointers on the cable and board must be matched at both ends of the cables.

APPENDIX A
KY11-LB MICRO-CODE LISTINGS

```
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 1

1               ;MACROS FOR 8008                9/9/74          PAGE 1
2
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 7


5
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8


1
3         000000          .ASECT
4         000000          .=0
5                         .TITLE KY11LB PROGRAM
6         000000          REG0=0
7         000001          REG1=1
8         000002          REG2=2
9         000003          REG3=3
10        000004          REG4=4
11        000005          REG5=5
12        000006          REG6=6
13        000007          REG7=7
14        000003          SRLB=3
15        000004          SRHB=4
16        000405          NUM0=NUM0X
17        000403          NUM2=NUM2X
18        000402          NUM3=NUM3X
19        000401          NUM4=NUM4X
20        000400          NUM5=NUM5X
21        000005          KEYS=5
22        000001          DBHB=1
23        000000          DBLB=0
24 00000          START:  RST 10          ;INITIALIZE PC TO 10.
   00000    015
25 00001          BEGIN:  LHI 240         ;PRESET H REGISTER TO POINT TO RAM (40) AND TO SET
   00001    056
   00002    240
26                                        ;A FLAG (200) TO ENABLE ADDRESS 777570 TO BE DISPLAYED
27                                        ;ON PROGRAMMED HALT.
28 00003                  LLI 20          ;PRESET L REGISTER TO POINT TO RAM.
   00003    066
   00004    020
29 00005                  JMP OVER
   00005    104
   00006    013
   00007    000
30 00010                  JMP BEGIN
   00010    104
   00011    001
   00012    000
31 00013          OVER:   LEI 0           ;ZERO REGISTER E.
   00013    046
   00014    000
32 00015                  LA E            ;ZERO REGISTER A.
   00015    304
33 00016          BEG1:   LM A            ;ZERO MEMORY LOCATION (RAM) POINTED TO BY REGISTERS H & L.
   00016    370
34 00017                  DC L            ;DECREMENT REGISTER L.
   00017    061
35 00020                  JFS BEG1        ;JUMP BACK UNTIL RAM IS ALL ZEROED.
   00020    120
   00021    016
   00022    000
36 00023          DISP1:  CAL DISP15      ;CALL DISPLAY SUBROUTINE.STAYS IN DISPLAY SUBROUTINE
   00023    106
   00024    031
   00025    000
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
```

```
37
38 00026                    JMP KEYSEV      ;UNTIL A KEY IS DEPRESSED OR A PROGRAM HALT OCCURS.
   00026    104                            ;RETURNS FROM DISPLAY SUBROUTINE TO
   00027    175
   00030    000
39                                          ;JUMP TO KEY SERVICE ROUTINE.
40
41
42 00031        DISP15: LA H                ;DISPLAY SUBROUTINE.
   00031    305
43                                          ;LOAD H REGISTER INTO REGISTER A AND MASK
44                                          ;FOR PROGRAMMED HALT FLAG BIT.
45 00032                    NDI 200         ;IF BIT IS NOT SET DO NOT TEST FOR PROGRAM
   00032    044
   00033    200
46 00034                    JTZ NXT         ;HALT.
   00034    150
   00035    052
   00036    000
47 00037                    INP REG5        ;OTHERWISE CHECK FOR HALT BUSY BEING SET.(KY11-LB
   00037    113
48 00040                    NDI 40          ;IS ASSERTING BUS BUSY).
   00040    044
   00041    040
49 00042                    JTZ NXT
   00042    150
   00043    052
   00044    000
50 00045                    LHI 40          ;CLEAR FLAG BIT TO PREVENT FURTHER SERVICING
   00045    056
   00046    040
51                                          ;OF THE HALT BUSY FLAG.
52 00047                    JMP HLT3        ;JUMP TO THE HALT SERVICE ROUTINE.
   00047    104
   00050    067
   00051    010
53 00052        NXT:    LCI 6               ;OTHERWISE CONTINUE THE DISPLAY ROUTINE.
   00052    026
   00053    006
54
55 00054                    LA E            ;LOAD REGISTER C WITH A 6 AS A DISPLAY DIGIT COUNTER.
   00054    304                            ;MASK OFF THE KEYSERVICE FLAG STORED IN REGISTER
56 00055                    NDI 200         ;E. THIS BIT WHEN SET INDICATES THAT A KEY HAS
   00055    044
   00056    200
57 00057                    LE A            ;BEEN SERVICED BUT IS STILL DEPRESSED.
   00057    340
58 00060                    LDI 1           ;PRESET REGISTER D WITH A 1 TO BE USED AS A STROBE BIT.
   00060    036
   00061    001
59 00062        DISP2:  LAI 0               ;PRESET REGISTER A WITH A ZERO.
   00062    006
   00063    000
60 00064                    OUT REG0        ;OUTPUTS THE ZERO TO TURN OFF THE DISPLAY.
   00064    121
61 00065                    LLI 0           ;PRESET MEMORY POINTER REGISTER L TO ZERO
   00065    066
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
```

```
   00066    000
62                                      ;TO PICK UP THE CONTENTS OF THE FIRST LOCATION IN RAM.
63 00067                LA M            ;GET THE CONTENTS OF THE FIRST LOCATION IN RAM.
   00067    307
64 00070                NDI 7           ;MASK OFF THE LOWEST 3 BITS AND
   00070    044
   00071    007
65 00072                OUT REG1        ;OUTPUT TO THE DISPLAY.
   00072    123
66 00073                LA D            ;LOAD THE D REGISTER INTO A REGISTER AND OUTPUT IT
   00073    303
67 00074                OUT REG0        ;TO TURN ON THE PROPER DIGIT OF THE DISPLAY.THIS
   00074    121
68                                      ;WILL ALSO SELECT A PARTICULAR COLUMN OF THE KEYPAD
69                                      ;TO BE READ BACK LATER.
70 00075                LA D            ;GET THE CONTENTS OF REGISTER D AND ROTATE LEFT
   00075    303
71 00076                RLC             ;TO SET UP TO TURN ON THE NEXT DIGIT.
   00076    002
72 00077                LD A
   00077    330
73 00100                LBI 3           ;LOAD REGISTER B WITH A 3 TO PASS TO THE SHIFT
   00100    016
   00101    003
74 00102                CAL SHFT1       ;SUBROUTINE WHICH WILL SHIFT THE DIPLAY DATA 3
   00102    106
   00103    335
   00104    000
75                                      ;POSITIONS.
76 00105                LA C            ;ON RETURN FROM SHIFT SUBROUTINE, LOAD REGISTER
   00105    302
77 00106                CPI 1           ;A WITH REGISTER C AND CHECK FOR A 1 TO SEE IF LAST
   00106    074
   00107    001
78                                      ;DIGIT IS BEING DISPLAYED.
79 00110                JTZ DISP45      ;IF LAST DIGIT IS BEING DISPLAYED JUMP OVER KEYPAD
   00110    150
   00111    137
   00112    000
80                                      ;INPUT ROUTINE .
81 00113                ADI 1           ;OTHERWISE ADD A 1 TO REGISTER A (CONTAINING REGISTER C)
   00113    004
   00114    001
82 00115                LL A            ;AND LOAD MEMORY POINTER TO POINT TO KEYPAD IMAGE
   00115    360
83                                      ;AREA OF THE RAM.
84 00116                INP KEYS        ;INPUT A COLUMN FROM THE KEYPAD AND
   00116    113
85 00117                NDI 17          ;MASK FOR SIGNIFIGANT BITS.
   00117    044
   00120    017
86 00121                JTZ DISP4       ;CHECK FOR NO KEYS DEPRESSED,OTEHERWISE
   00121    150
   00122    136
   00123    000
87 00124                XR M            ;COMPARE AGAINST THE CONTENTS OR THE RAM(KEYPAD IMAGE)
   00124    257
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
```

```
88 00125                    JTZ DISP3       ;TO CHECK THAT THE KEYPAD IS STABLE.
   00125    150
   00126    132
   00127    000
89 00130                    IN E            ;INCREMENT REGISTER E BY THREE IF THE KEY IS DEPRESSED.
   00130    040
90 00131                    IN E            ;DOES NOT MATCH THE RAM CONTENTS.  REGISTER E WILL
   00131    040
91 00132        DISP3:      IN E            ;BE INCREMENTED BY ONE IF THERE IS A MATCH.
   00132    040
92 00133                    INP KEYS        ;INPUT THE COLUMN OF KEYPAD AGAIN AND
   00133    113
93 00134                    NDI 17          ;MASK FOR SIGNIFICANT BITS.
   00134    044
   00135    017
94 00136        DISP4:      LM A            ;STORE IN KEYPAD IMAGE AREA OF RAM FOR NEXT TIME.
   00136    370
95 00137        DISP45:     DC C            ;DECREMENT THE DISPLAY COUNTER AND
   00137    021
96 00140                    JFZ DISP2       ;IF NOT DONE JUMP BACK AND DISPLAY NEXT DIGIT.
   00140    110
   00141    062
   00142    000
97 00143                    LAI 0           ;IF ALL DIGITS HAVE BEEN DISPLAYED AND KEYPAD HAS
   00143    006
   00144    000
98 00145                    OUT REG0        ;BEEN READ, LOAD REGISTER A WITH A ZERO AND OUTPUT
   00145    121
99                                          ;TO TURN DISPLAY OFF.
100 0146                    LBI 6           ;LOAD REGISTER B WITH A 6 TO BE PASSED TO THE SHIFT
    0146    016
    0147    006
101 0150                    CAL SHFT1       ;SUBROUTINE.  SIX MORE SHIFTS ARE NECESSARY TO
    0150    106
    0151    335
    0152    000
102                                         ;FINISH SHIFTING AN 18 BIT NUMBER (SIX DIGITS)
103                                         ;THROUGH 24 BITS OF MEMORY IN THE RAM (3 WORDS).
104 0153                    LA E            ;GET THE CONTENTS OF REGISTER E AND CHECK
    0153    304
105 0154                    CPI 200
    0154    074
    0155    200
106 0156                    JFZ DISP5       ;IF ONLY KEYSERVICE FLAG IS SET (KEY NO LONGER DEPRESSED)
    0156    110
    0157    163
    0160    000
107 0161                    LEI 0           ;IF NO KEYS ARE DEPRESSED KEYSERVICE FLAG IS CLEARED.
    0161    046
    0162    000
108 0163        DISP5:      LA E            ; OTHERWISE, CHECK REGISTER E FOR A 1 OR A 2
    0163    304
109 0164                    CPI 1           ;(1 OR 2 KEYS ARE DEPRESSED AND ARE STABLE)
    0164    074
    0165    001
110 0166                    RTZ             ;AND IF TRUE RETURN FROM DISPLAY SUBROUTINE TO SERVICE
    0166    053
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
```

```
111 0167                CPI 2           #THE KEY BEING DEPRESSED.
    0167    074
    0170    002
112 0171                RTZ
    0171    053
113 0172                JMP DISP15      #STAY IN DISPLAY SUBROUTINE.
    0172    104
    0173    031
    0174    000
114
115                                     #KEY SERVICE ROUTINE.
116                                     #THIS ROUTINE DECODES THE CONSOLE MODE KEYS
117                                     #TO JUMP TO THE PROPER ROUTINE TO PERFORM
118                                     #THE PARTICULAR FUNCTION ASSOCIATED
119                                     #WITH EACH KEY.
120 0175        KEYSEV: LBI 0           #RESET REGISTER B TO ZERO.
    0175    016
    0176    000
121 0177                LEI 200         #SET KEYSERVICE FLAG TO INDICATE THAT KEY HAS BEEN SERVICED.
    0177    046
    0200    200
122 0201                LLI 3           #SET UP MEMORY POINTER TO THE KEYPAD IMAGE AREA.
    0201    066
    0202    003
123 0203                LA M            #GET THE FIRST COLUMN OF KEYS FROM THE KEYPAD IMAGE
    0203    307
124 0204                RAR             #AREA OF RAM.  ROTATE THE VALUE OF THE FIRST KEY IN THAT
    0204    032
125 0205                JTC DISPAD      #COLUMN INTO THE CARRY BIT AND JUMP TO THE SERVICE
    0205    140
    0206    344
    0207    010
126 0210                RAR             #ROUTINE FOR THAT KEY IF THE C BIT IS SET.  OTHERWISE
    0210    032
127 0211                JTC LAD1        #ROTATE IN THE VALUE OF THE NEXT KEY AND SO ON UNTIL
    0211    140
    0212    305
    0213    010
128 0214                RAR             #THE WHOLE COLUMN HAS BEEN CHECKED.
    0214    032
129 0215                JTC LSR1
    0215    140
    0216    230
    0217    010
130 0220                RAR
    0220    032
131 0221                JTC CLR1
    0221    140
    0222    327
    0223    010
132 0224                IN L            #AFTER WHOLE COLUMN HAS BEEN CHECKED INCREMENT THE
    0224    060
133 0225                LA M            #MEMORY POINTER AND GET THE VALUES OF THE NEXT COLUMN
    0225    307
134 0226                RAR             #OF KEYS FROM THE KEYPAD IMAGE AREA.  DECODE THESE
    0226    032
135 0227                JTC NUM7        #KEYS IN THE SAME MANNER.
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```

```
     0227    140
     0230    220
     0231    011
136  0232                    RAR
     0232    032
137  0233                    JTC NUM4
     0233    140
     0234    001
     0235    001
138  0236                    RAR
     0236    032
139  0237                    JTC NUM1
     0237    140
     0240    371
     0241    010
140  0242                    RAR
     0242    032
141  0243                    JTC NUM0
     0243    140
     0244    005
     0245    001
142  0246                    IN L
     0246    060
143  0247                    LA M
     0247    307
144  0250                    RAR
     0250    032
145  0251                    JTC EXAM1
     0251    140
     0252    107
     0253    001
146  0254                    RAR
     0254    032
147  0255                    JTC NUM5
     0255    140
     0256    000
     0257    001
148  0260                    RAR
     0260    032
149  0261                    JTC NUM2
     0261    140
     0262    003
     0263    001
150  0264                    RAR
     0264    032
151  0265                    JTC INIT1
     0265    140
     0266    111
     0267    010
152  0270                    IN L
     0270    060
153  0271                    LA M
     0271    307
154  0272                    RAR
     0272    032
155  0273                    JTC DEP1
     0273    140
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```

```
     0274    271
     0275    001
156  0276                RAR
     0276    032
157  0277                JTC NUM6
     0277    140
     0300    253
     0301    011
158  0302                RAR
     0302    032
159  0303                JTC NUM3
     0303    140
     0304    002
     0305    001
160  0306                IN L            ;NOTE THAT THE CNTRL KEY IS NOT DECODED HERE
     0306    060
161  0307                LA M            ;BECAUSE IT IS USED IN CONJUNCTION WITH KEYS YET TO
     0307    307
162  0310                RAR             ;BE DECODED.
     0310    032
163  0311                JTC HLT1
     0311    140
     0312    023
     0313    010
164  0314                RAR
     0314    032
165  0315                JTC CONT1
     0315    140
     0316    212
     0317    010
166  0320                RAR
     0320    032
167  0321                JTC BOOT1
     0321    140
     0322    063
     0323    001
168  0324                RAR
     0324    032
169  0325                JTC STRT1
     0325    140
     0326    150
     0327    010
170  0330                LEI 0           ;IT IS ASSUMED THAT THE CNTRL KEY HAS BEEN DEPRESSED
     0330    046
     0331    000
171  0332                JMP DISP1       ;SINCE ALL OTHER KEYS HAVE BEEN DECODED.  KEYSERVICE
     0332    104
     0333    023
     0334    000
172                                      ;FLAG IS CLEARED SO THAT A SECOND KEY MAY BE
173                                      ;DECODED IN CONJUNCTION WITH THE CNTRL KEY.
174
175
176                                      ;SHIFT SUBROUTINE.
177                                      ;THIS SUBROUTINE IS USED TO SHIFT THE DISPLAY
178                                      ;DATA AREA OF THE RAM (FIRST 3 LOCATIONS)
179                                      ;THE NUMBER OF BIT POSITIONS PASSED THROUGH
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```

```
180                                     ;REGISTER B.
181 0335        SHFT1:  LLI 3
    0335    066
    0336    003
182 0337                LAI 0           ;SET UP MEMORY POINTER TO THE MOST SIGNIFICANT WORD
    0337    006
    0340    000
183 0341                RAR             ;PLUS ONE.  ZERO REGISTER A AND ROTATE TO CLEAR THE
    0341    032
184 0342                DC L            ;CARRY BIT.
    0342    061
185 0343        SHFT2:  LA M            ;DECREMENT THE MEMORY POINTER AND GET THE FIRST
    0343    307
186 0344                RAR             ;WORD TO BE SHIFTED.
    0344    032
187 0345                LM A            ;ROTATE TO THE RIGHT SAVING THE LSB IN THE C BIT.
    0345    370
188 0346                DC L            ;RESTORE TO MEMORY THE SHIFTED VALUE.
    0346    061
189 0347                JFS SHFT2       ;DECREMENT MEMORY POINTER TO NEXT WORD AND
    0347    120
    0350    343
    0351    000
190 0352                LLI 2           ;IF NOT DONE JUMP BACK.
    0352    066
    0353    002
191 0354                LA M            ;THE LSB OF THE LEAST SIGNIFICANT WORD IS NOW IN THE
    0354    307
192 0355                RAL             ;C BIT BUT SHOULD BE IN MSB OF MOST SIGNIFICANT WORD.
    0355    022
193 0356                RRC             ;MEMORY POINTER IS RESET TO MOST SIGNIFICANT WORD
    0356    012
194 0357                LM A            ;AND C BIT SHIFTED INTO LSB.  THE WORD
    0357    370
195 0360                DC B            ;IS THEN ROTATED TO PUT LSB INTO MSB POSITION.
    0360    011
196 0361                JFZ SHFT1       ;SHIFT COUNTER IS DECREMENTED AND IF DONE RETURN
    0361    110
    0362    335
    0363    000
197 0364                RET             ;FROM SUBROUTINE.
    0364    007
198
199
200                                     ;MODE TEST SUBROUTINE.
201                                     ;THIS SUBROUTINE IS USED BY VARIOUS KEY
202                                     ;SERVICE ROUTINES TO CHECK IF THE CNTRL KEY
203                                     ;HAS BEEN DEPRESSED PRIOR TO SERVICING THOSE
204                                     ;KEYS WHICH REQUIRE THE CNTRL TO
205                                     ;BE USED.
206 0365        MDTST:  LLI 6           ;SET MEMORY POINTER TO KEYPAD IMAGE AREA AND
    0365    066
    0366    006
207 0367                LA M            ;GET WORD CONTAINING THE VALUE OF THE CNTRL KEY.
    0367    307
208 0370                NDI 10          ;TEST FOR THE CNTRL KEY AND IF NOT DEPRESSED
    0370    044
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```
     0371    010
209  0372                JTZ DISP1       ;RETURN TO DISPLAY ROUTINE.  OTHERWISE RETURN TO SERVICE
     0372    150
     0373    023
     0374    000
210  0375                RET             ;ROUTINE WHICH CALLED.
     0375    007
211
212
213                                      ;NUMERIC ROUTINE.
214                                      ;THIS ROUTINE GENERATES THE PROPER 3 BIT
215                                      ;DIGIT WHEN A NUMERIC KEY IS DEPRESSED AND
216                                      ;LEFT SHIFTS IT INTO THE TEMPORARY AREA
217                                      ;OF THE RAM.
218  0376        NUM7X:  IN B            ;INCREMENT THE B REGISTER THE CORRECT NUMBER
     0376    010
219  0377        NUM6X:  IN B            ;OF TIMES DEPENDING UPON THE NUMERIC KEY DEPRESSED.
     0377    010
220  0400        NUM5X:  IN B            ;NOTE THE B REGISTER WAS CLEARED AT THE BEGINNING
     0400    010
221  0401        NUM4X:  IN B            ;OF THE KEY SERVICE ROUTINE.
     0401    010
222  0402        NUM3X:  IN B
     0402    010
223  0403        NUM2X:  IN B
     0403    010
224  0404        NUM1X:  IN B
     0404    010
225  0405        NUM0X:  LCI 3           ;PRESET REGISTER C WITH A 3 AS A SHIFT COUNTER.
     0405    026
     0406    003
226  0407        NUMX:   LLI 10          ;SET THE MEMORY POINTER TO THE TEMPORARY AREA IN THE RAM.
     0407    066
     0410    010
227  0411                LA M            ;ROTATE THE THREE WORDS OF THE TEMPORARY AREA ONE
     0411    307
228  0412                RAL             ;BIT AT A TIME, THREE TIMES AROUND SO THAT ALL THREE WORDS
     0412    022
229  0413                LM A            ;HAVE BEEN SHIFTED THREE TIMES.
     0413    370
230  0414                IN L
     0414    060
231  0415                LA M
     0415    307
232  0416                RAL
     0416    022
233  0417                LM A
     0417    370
234  0420                IN L
     0420    060
235  0421                LA M
     0421    307
236  0422                RAL
     0422    022
237  0423                LM A
     0423    370
238  0424                DC C
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```
     0424    021
239  0425                JFZ NUMX
     0425    110
     0426    007
     0427    001
240  0430                LLI 10          ;RESET MEMORY POINTER TO LEAST SIGNIFICANT WORD.
     0430    066
     0431    010
241  0432                LA M            ;GET THE WORD AND ZERO THE LEAST THREE SIGNIFICANT
     0432    307
242  0433                NDI 370         ;BITS.
     0433    044
     0434    370
243  0435                AD B            ;ADD IN THE THREE BIT DIGIT FROM REGISTER B AND
     0435    201
244  0436                LM A            ;RESTORE IN MEMORY.
     0436    370
245  0437                LAI 0           ;CLEAR DISPLAY INDICATORS.
     0437    006
     0440    000
246  0441                OUT REG6
     0441    135
247
248
249                                      ;MOVE ROUTINE.
250                                      ;THIS ROUTINE IS USED TO MOVE THE TEMPORARY
251                                      ;AREA OR THE SWITCH REGISTER IMAGE AREA OF
252                                      ;THE RAM TO THE DISPLAY AREA OF THE RAM.
253  0442        MOV1:   LLI 10          ;SET UP MEMORY POINTER TO TEMPORARY AREA OF RAM.
     0442    066
     0443    010
254  0444        MOV2:   LB M            ;LOAD THE NEXT THREE WORDS FROM RAM INTO REGISTERS
     0444    317
255  0445                IN L            ;B, C, AND D.
     0445    060
256  0446                LC M
     0446    327
257  0447                IN L
     0447    060
258  0450                LD M
     0450    337
259  0451                LLI 0           ;RESET MEMORY POINTER TO THE DISPLAY AREA OF THE
     0451    066
     0452    000
260  0453                LM B            ;RAM AND LOAD REGISTERS B, C, AND D BACK INTO MEMORY.
     0453    371
261  0454                IN L
     0454    060
262  0455                LM C
     0455    372
263  0456                IN L
     0456    060
264  0457                LM D
     0457    373
265  0460                JMP DISP1       ;GO BACK TO DISPLAY ROUTINE.
     0460    104
     0461    023
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```
     0462    000
266
267
268                                         ;BOOT ROUTINE.
269                                         ;THIS ROUTINE SETS AND CLEARS THE BOOT BIT
270                                         ;JUMPS TO SWITCH REGISTER DISPLAY ROUTINE.
271 0463         BOOT1:  CAL MDTST          ;CALL SUBROUTINE TO CHECK IF CNTRL KEY IS DEPRESSED.
     0463    106
     0464    365
     0465    000
272 0466                 CAL HLTST          ;CALL SUBROUTINE TO CHECK IF PROCESSOR IS HALTED.
     0466    106
     0467    362
     0470    010
273 0471                 LHI 240            ;SET BIT IN H REGISTER (200) TO LOOK FOR PROGRAM
     0471    056
     0472    240
274                                         ;HALTS.
275 0473                 LAI 200            ;SET THE BOOT BIT.
     0473    006
     0474    200
276 0475                 OUT REG6
     0475    135
277 0476                 LAI 0
     0476    006
     0477    000
278 0500                 OUT REG6           ;CLEAR THE BOOT BIT.
     0500    135
279 0501                 CAL TIMER          ;WAIT.
     0501    106
     0502    133
     0503    010
280 0504                 JMP SRDISP         ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
     0504    104
     0505    261
     0506    010
281
282
283                                         ;EXAM ROUTINE.
284                                         ;THIS ROUTINE IS USED TO SERVICE THE EXAM
285                                         ;KEY.
286 0507         EXAM1:  CAL HLTST
     0507    106
     0510    362
     0511    010
287 0512                 LLI 15             ;CHECK THAT PROCESSOR IS HALTED.
     0512    066
     0513    015
288 0514                 LA M               ;GET LOCATION 15 FROM THE RAM AND CHECK IF
     0514    307
289 0515                 NDI 200            ;THE EXAM FLAG IS SET. IF IT IS SET THEN
     0515    044
     0516    200
290 0517                 JTZ EXAM2          ;THE UNIBUS ADDRESS WILL BE INCREMENTED BEFORE
     0517    150
     0520    130
     0521    001
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```
291 0522                        CAL GPRT1       ;BEING USED. CHECK TO SEE IF IT SHOULD BE INCREMENTED
    0522    106
    0523    174
    0524    001
292 0525                        CAL INCAD       ;BY ONE (GENERAL REGISTER) OR BY TWO.
    0525    106
    0526    151
    0527    001
293 0530            EXAM2:      CAL BADLD       ;LOADS BUS ADDRESS POINTER (RAM) INTO THE UNIBUS
    0530    106
    0531    344
    0532    001
294 0533                        LLI 15          ;ADDRESS  REGISTER.
    0533    066
    0534    015
295 0535                        LA M            ;MASK OFF THE TWO DATA BITS AND SET THE EXAM FLAG
    0535    307
296 0536                        NDI 3           ;(200 IN LOCATION 15).
    0536    044
    0537    003
297 0540                        ORI 200
    0540    064
    0541    200
298 0542                        LM A
    0542    370
299 0543                        CAL DATI1       ;CALL THE DATI ROUTINE AND JUMP TO THE MOVE ROUTINE
    0543    106
    0544    230
    0545    001
300 0546                        JMP MOV1        ;TO DISPLAY THE NEW DATA.
    0546    104
    0547    042
    0550    001
301
302
303                                             ;INCREMENT ADDRESS SUBROUTINE.
304                                             ;THIS SUBROUTINE INCREMENTS THE UNIBUS ADDRESS
305                                             ;POINTER IN THE RAM BY   1.
306 0551            INCAD:      LLI 13          ;ADDS A 1 TO THE LEAST SIGNIFIGANT WORD
    0551    066
    0552    013
307 0553                        LA M            ;OF THE UNIBUS ADDRESS POINTER (LOCATION 13)
    0553    307
308 0554                        ADI 1           ;AND THEN ADDS THE CARRY BIT INTO THE NEXT TWO
    0554    004
    0555    001
309 0556                        LM A            ;WORDS. THE TWO LSB'S IN THE LAST WORD ARE MASKED
    0556    370
310 0557                        IN L            ;AS SIGNIFIGANT (18 BIT ADDRESS).
    0557    060
311 0560                        LAI 0
    0560    006
    0561    000
312 0562                        AC M
    0562    217
313 0563                        LM A
    0563    370
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```
314 0564                IN L
    0564    060
315 0565                LAI 0
    0565    006
    0566    000
316 0567                AC M
    0567    217
317 0570                NDI 3
    0570    044
    0571    003
318 0572                LM A
    0572    370
319 0573                RET
    0573    007
320
321
322                                     ;GENERAL REGISTER TEST SUBROUTINE.
323                                     ;THIS SUBROUTINE TESTS THE UNIBUS ADDRESS
324                                     ;POINTER TO SEE IF IT IS IN THE RANGEOF
325                                     ;GENERAL PURPOSE ADDRESSES (777700-777717).
326                                     ;IF IT IS NOT A GENERAL REGISTER ADDRESS
327                                     ;THEN THIS SUBROUTINE WILL INCREMENT THE
328                                     ;ADDRESS BY ONE.IF IT IS IN THE RANGE IT
329                                     ;WILL NOT INCREMENT AT ALL.
330 0574        GPRT1:  LA M
    0574    307
331 0575                NDI 3
    0575    044
    0576    003
332 0577                CPI 3           ;ARE ADDRESS BITS 17 AND 16 ONES?
    0577    074
    0600    003
333 0601                JFZ GPRT2       ;NO.
    0601    110
    0602    224
    0603    001
334 0604                DC L            ;YES.
    0604    061
335 0605                LA M
    0605    307
336 0606                CPI 377         ;ARE ADDRESS BITS 15 THRU 8 ONES?
    0606    074
    0607    377
337 0610                JFZ GPRT2       ;NO.
    0610    110
    0611    224
    0612    001
338 0613                DC L            ;YES.
    0613    061
339 0614                LA M
    0614    307
340 0615                NDI 360         ;ARE ADDRESS BITS 7 AND 6 ONES AND
    0615    044
    0616    360
341 0617                CPI 300         ;BITS 5 AND 4 ZEROES?
    0617    074
    0620    300
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```
342 0621                JTZ GPRT3       ;YES.
    0621    150
    0622    227
    0623    001
343 0624        GPRT2:  CAL INCAD       ;NO. INCREMENT ADDRESS BY ONE.
    0624    106
    0625    151
    0626    001
344 0627        GPRT3:  RET
    0627    007
345
346
347                                     ;DATI SUBROUTINE.
348                                     ;THIS SUBROUTINE PERFORMS A DATI ON THE
349                                     ;UNIBUS ADDRESS POINTED TO BY THE UNIBUS ADDRESS
350                                     ;REGISTER.THE RECEIVED DATA IS LOADED INTO
351                                     ;THE TEMPORARY AREA IN RAM.
352 0630        DATI1:  LLI 10          ;SET UP MEMORY POINTER TO TEMPORARY.
    0630    066
    0631    010
353 0632                LAI 10          ;SET BUS MSYN BIT.
    0632    006
    0633    010
354 0634                OUT REG5
    0634    133
355 0635                INP REG5        ;HAS BUS SSYN BEEN RETURNED?
    0635    113
356 0636                NDI 20
    0636    044
    0637    020
357 0640                JTZ BUSERR      ;NO, REPORT BUS ERROR.
    0640    150
    0641    257
    0642    001
358 0643        DATI2:  INP DBLB        ;YES, PROCEED.   GET LOW BYTE OF UNIBUS
    0643    101
359 0644                LM A            ;DATA AND STORE IN MEMORY.
    0644    370
360 0645                IN L
    0645    060
361 0646                INP DBHB        ;GET HIGH BYTE OF UNIBUS DATA AND
    0646    103
362 0647                LM A            ;STORE IN MEMORY.
    0647    370
363 0650                IN L
    0650    060
364 0651                LAI 0
    0651    006
    0652    000
365 0653                LM A            ;ZERO LAST WORD OF TEMPORARY.
    0653    370
366 0654                OUT REG5        ;CLEAR BUS MSYN BIT.
    0654    133
367 0655                OUT REG2        ;DROP UNIBUS ADDRESS LINES.
    0655    125
368 0656                RET
    0656    007
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```

```
369
370
371                                     ;UNIBUS ERROR SUBROUTINE.
372                                     ;THIS SUBROUTINE SETS THE BUS ERROR
373                                     ;INDICATOR AND TERMINATES THE UNIBUS TRANSACTION.
374 0657         BUSERR: LAI 20
    0657    006
    0660    020
375 0661                 OUT REG6       ;SET BUS ERROR INDICTOR.
    0661    135
376 0662                 LAI  0
    0662    006
    0663    000
377 0664                 OUT REG5       ;DROP BUS MSYN.
    0664    133
378 0665                 OUT REG2       ;DROP UNIBUS ADDRESS LINES.
    0665    125
379 0666                 JMP CLR2       ;GO CLEAR THE DISPLAY.
    0666    104
    0667    332
    0670    010
380
381
382                                     ;DEPOSIT SUBROUTINE.
383                                     ;THIS ROUTINE SERVICES THE DEPOSIT KEY.
384 0671         DEP1:   CAL HLTST      ;CHECK FOR PROCESSOR HALTED.
    0671    106
    0672    362
    0673    010
385 0674                 LAI 0
    0674    006
    0675    000
386 0676                 OUT REG6       ;CLEAR THE INDICATORS.
    0676    135
387 0677                 LLI 15         ;SET UP MEMORY POINTER AND CHECK DEPOSIT FLAG.
    0677    066
    0700    015
388 0701                 LA M
    0701    307
389 0702                 NDI 100        ;FIRST DEPOSIT?
    0702    044
    0703    100
390 0704                 JTZ DEP2       ;YES.
    0704    150
    0705    315
    0706    001
391 0707                 CAL GPRT1      ;NO. CHECK FOR GENERAL REGISTER.
    0707    106
    0710    174
    0711    001
392 0712                 CAL INCAD      ;INCREMENT UNIBUS ADDRESS POINTER.
    0712    106
    0713    151
    0714    001
393 0715         DEP2:   LA M
    0715    307
394 0716                 ORI 10         ;SET THE BUS C1 BIT (IN RAM) TO DO A DATO.
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```
     0716    064
     0717    010
395  0720                LM A
     0720    370
396  0721                CAL BADLD       ;LOAD THE UNIBUS ADDRESS REGISTER.
     0721    106
     0722    344
     0723    001
397  0724                LLI 15
     0724    066
     0725    015
398  0726                LA M
     0726    307
399  0727                NDI 3
     0727    044
     0730    003
400  0731                ORI 100         ;SET THE DEPOSIT FLAG.
     0731    064
     0732    100
401  0733                LM A
     0733    370
402  0734                LLI 10          ;RESET MEMORY POINTER TO TEMPORARY AREA OF RAM.
     0734    066
     0735    010
403  0736                CAL DATO1       ;CALL THE DATO SUBROUTINE USING THE TEMORARY AREA
     0736    106
     0737    361
     0740    001
404  0741                JMP MOV1        ;AS DATA. DISPLAY TEMPORARY AREA.
     0741    104
     0742    042
     0743    001
405
406
407                                     ;UNIBUS ADDRESS REGISTER LOAD SUBROUTINE.
408                                     ;THIS SUBROUTINE LOADS THE UNIBUS ADDRESS
409                                     ;POINTER FROM RAM INTO THE UNIBUS ADDRESS
410                                     ;REGISTER AND ENABLES THE REGISTER ONTO
411                                     ;THE UNIBUS.
412  0744        BADLD:  LLI 13         ;SET UP MEMORY POINTER TO UNIBUS ADDRESS POINTER.
     0744    066
     0745    013
413  0746                LA M
     0746    307
414  0747                OUT REG0        ;MOVE FIRST WORD TO UNIBUS ADDRESS REGISTER.
     0747    121
415  0750                IN L
     0750    060
416  0751                LA M
     0751    307
417  0752                OUT REG1        ;MOVE NEXT WORD TO REGISTER.
     0752    123
418  0753                IN L
     0753    060
419  0754                LA M
     0754    307
420  0755                ORI 4           ;SET THE ENABLE BIT.
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```
    0755    064
    0756    004
421 0757                OUT REG2        ;LOAD LAST PART OF REGISTER.
    0757    125
422 0760                RET
    0760    007
423
424
425                                     ;DATO SUBROUTINE.
426                                     ;THIS SUBROUTINE PERFORMS THE DATO
427                                     ;SEQUENCE FOR DEPOSIT AND START KEY FUNCTIONS.
428 0761        DATO1:  LA M            ;GET FIRST WORD FROM MEMORY(FROM TEMPORARY ON DEPOSITS
    0761    307
429 0762                OUT SRLB        ;AND UNIBUS ADDRESS POINTER ON STARTS) AND LOAD
    0762    127
430 0763                IN L            ;LOW BYTE OF SWITCH REGISTER.
    0763    060
431 0764                LA M            ;GET SECOND WORD OF DATA AND LOAD INTO
    0764    307
432 0765                OUT SRHB        ;HIGH BYTE OF SWITCH REGISTER.
    0765    131
433 0766                LAI 4           ;SET BIT TO ENABLE SWITCH REGISTER ONTO
    0766    006
    0767    004
434 0770                OUT REG5        ;THE UNIBUS.
    0770    133
435 0771                LAI 14
    0771    006
    0772    014
436 0773                OUT REG5        ;ASSERT BUS MSYN.
    0773    133
437 0774                INP REG5        ;BUS SSYN RETURNED?
    0774    113
438 0775                JMP MEM2        ;JUMP OVER ROM MEMORY BOUNDARY.
    0775    104
    0776    001
    0777    010
439 1000                NOP
    1000    300
440 1001        MEM2:   NDI 20
    1001    044
    1002    020
441 1003                JTZ BUSERR      ;NO.
    1003    150
    1004    257
    1005    001
442 1006                LAI 4           ;YES.
    1006    006
    1007    004
443 1010                OUT REG5        ;DROP BUS MSYN.
    1010    133
444 1011                LAI 0
    1011    006
    1012    000
445 1013                OUT REG5        ;DROP THE SWITCH REGISTER ENABLE.
    1013    133
446 1014                OUT REG2        ;CLEAR THE UNIBUS ADDRESS REGISTER AND REMOVE
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```

```
     1014    135
447  1015                OUT REG1        ;FROM THE UNIBUS.
     1015    123
448  1016                OUT REG0
     1016    121
449  1017                CAL SRLD        ;CALL ROUTINE TO REPLACE THE CONTENTS OF SWITCH REGISTER.
     1017    106
     1020    250
     1021    010
450  1022                RET
     1022    007
451
452
453                                     ;HALT ROUTINE.
454                                     ;THIS ROUTINE SERVICES THE HALT/SINGLE STEP
455                                     ;KEY FUNCTION AND ALSO SERVICES A PROGRAM
456                                     ;HALT BY THE PROCESSOR.
457  1023        HLT1:   INP REG5
     1023    113
458  1024                NDI 40          ;IS PROCESSOR ALREADY HALTED?
     1024    044
     1025    040
459  1026                JFZ SS1         ;YES. DO SINGLE STEP FUNCTION.
     1026    110
     1027    034
     1030    010
460  1031                CAL MDTST       ;NO. IS CNTRL KEY DEPRESSED?
     1031    106
     1032    365
     1033    000
461  1034        SS1:    LAI 41          ;YES.SET HALT REQUEST AND CLEAR BUS BITS.IF PROCESSOR
     1034    006
     1035    041
462  1036                OUT REG5        ;IS HALTED IT WILL PROCEED ONE INSTRUCTION.
     1036    133
463  1037        HLT15:  LAI 1           ;DROP THE CLEAR BUS BIT.
     1037    006
     1040    001
464  1041                OUT REG5
     1041    133
465  1042        HLT2:   LCI 0           ;SET UP A TIMING LOOP TO WAIT FOR HALT
     1042    026
     1043    000
466  1044                LBI 12          ;GRANTS IN CASE PROCESSOR IS DOING A RESET .
     1044    016
     1045    012
467  1046        HLT25:  INP REG5
     1046    113
468  1047                NDI 40          ;HALT GRANT RECEIVED?
     1047    044
     1050    040
469  1051                JFZ HLT3        ;YES.
     1051    110
     1052    067
     1053    010
470  1054                DC C            ;NO.DECREMENT COUNTER.
     1054    021
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```

```
471 1055                JFZ HLT25       ;DONE COUNT?NO.
    1055    110
    1056    046
    1057    010
472 1060                DC B            ;DECREMENT COUNTER.
    1060    011
473 1061                JFZ HLT25       ;TIMED OUT? NO.
    1061    110
    1062    046
    1063    010
474 1064                JMP BUSERR      ;YES. GO TO BUS ERROR ROUTINE.
    1064    104
    1065    257
    1066    001
475 1067        HLT3:   LAI 0           ;RECEIVED GRANT.NOW CLEAR INDICATORS.
    1067    006
    1070    000
476 1071                OUT REG6
    1071    135
477 1072                LAI 307         ;LOAD UNIBUS ADDRESS OF PC (R7) (777707)
    1072    006
    1073    307
478 1074                OUT REG0        ;INTO THE UNIBUS ADDRESS REGISTER AND
    1074    121
479 1075                LAI 377         ;ENABLE ONTO THE UNIBUS.
    1075    006
    1076    377
480 1077                OUT REG1
    1077    123
481 1100                LAI 7
    1100    006
    1101    007
482 1102                OUT REG2
    1102    125
483 1103                CAL DATI1       ;CALL THE DATI SUBROUTINE.
    1103    106
    1104    230
    1105    001
484 1106                JMP MOV1        ;DISPLAY THE PC.
    1106    104
    1107    042
    1110    001
485
486
487                                     ;INIT KEY SERVICE ROUTINE.
488                                     ;THIS ROUTINE SERVICES THE INIT KEY
489                                     ;FUNCTION.
490 1111        INIT1:  CAL MDTST       ;CHECK THAT CNTRL KEY HAS BEEN DEPRESSED AND
    1111    106
    1112    365
    1113    000
491 1114                CAL HLTST       ;THAT THE PROCESSOR IS HALTED.
    1114    106
    1115    362
    1116    010
492 1117                CAL INITX       ;CALL THE INITIALIZE SUBROUTINE.
    1117    106
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```

```
     1120    130
     1121    010
493  1122                LAI 1           ;DROP THE BUS INIT BIT LEAVING THE HALT REQUEST
     1122    006
     1123    001
494  1124                OUT REG5        ;BIT SET.
     1124    133
495  1125                JMP DISP1
     1125    104
     1126    023
     1127    000
496
497
498                                      ;INITIALIZE SUBROUTINE.
499                                      ;THIS SUBROUTINE SETS THE BUS INIT
500                                      ;BIT FOR 150 MILLISECONDS. THIS IS USED
501                                      ;BY THE START AND INIT KEY FUNCTIONS.
502  1130        INITX:  LAI 3
     1130    006
     1131    003
503  1132                OUT REG5        ;SET BOTH BUS INIT AND HALT REQUEST BITS.
     1132    133
504  1133        TIMER:  LBI 12          ;PRESET COUNTERS FOR A 150 MILLISECOND DELAY.
     1133    016
     1134    012
505  1135                LCI 0
     1135    026
     1136    000
506  1137        INITX2: DC C            ;DECREMENT COUNTERS AND RETURN WHEN DONE.
     1137    021
507  1140                JFZ INITX2
     1140    110
     1141    137
     1142    010
508  1143                DC B
     1143    011
509  1144                JFZ INITX2
     1144    110
     1145    137
     1146    010
510  1147                RET
     1147    007
511
512
513                                      ;START ROUTINE.
514                                      ;THIS ROUTINE SERVICES THE START KEY FUNCTION
515                                      ;BY LOADING THE PC (R7) WITH THE UNIBUS
516                                      ;ADDRESS POINTER,GENERATING BUS INIT, AND
517                                      ;ALLOWING THE PROCESSOR TO CONTINUE.
518  1150        STRT1:  CAL MDTST       ;CHECK THAT CNTRL KEY IS DEPRESSED AND
     1150    106
     1151    365
     1152    000
519  1153                CAL HLTST       ;THAT PROCESSOR IS HALTED.
     1153    106
     1154    362
     1155    010
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```

```
520 1156                LHI 240         ;RESET PROGRAMMED HALT FLAG (200).
    1156    056
    1157    240
521 1160                LAI 307         ;LOAD ADDRESS OF PC (777707) INTO THE
    1160    006
    1161    307
522 1162                OUT REG0        ;UNIBUS ADDRESS POINTER.
    1162    121
523 1163                LAI 377
    1163    006
    1164    377
524 1165                OUT REG1
    1165    123
525 1166                LAI 17          ;SET THE ENABLE BIT (4) AND THE
    1166    006
    1167    017
526 1170                OUT REG2        ;BUS C1 BIT (10).
    1170    125
527 1171                LLI 13          ;SET THE MEMORY POINTER TO UNIBUS ADDRESS POINTER
    1171    066
    1172    013
528 1173                CAL DATO1       ;AND CALL THE DATO SUBROUTINE.
    1173    106
    1174    361
    1175    001
529 1176                CAL INITX       ;CALL THE INITIALIZE SUBROUTINE TO GENERATE
    1176    106
    1177    130
    1200    010
530 1201                LAI 2           ;BUS INITIALIZE.
    1201    006
    1202    002
531 1203                OUT REG5        ;DROP BUS INIT AND HALT REQUEST BITS AND SET BUS
    1203    133
532 1204                LAI 0           ;CLEAR BIT. THEN DROP BUS CLEAR BIT.
    1204    006
    1205    000
533 1206                OUT REG5
    1206    133
534 1207                JMP SRDISP      ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
    1207    104
    1210    261
    1211    010
535
536
537                                     ;CONTINUE ROUTINE.
538                                     ;THIS ROUTINE SERVICES THE CONT KEY FUNCTION.
539 1212        CONT1:  CAL MDTST       ;CHECK IF THE CNTRL KEY IS DEPRESSED.
    1212    106
    1213    365
    1214    000
540 1215                LHI 240         ;RESET PROGRAMMED HALT FLAG.
    1215    056
    1216    240
541 1217                LAI 40          ;SET THE BUS CLEAR BIT TO ALLOW PROCESSOR
    1217    006
    1220    040
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```

```
542 1221                        OUT REG5        ;TO CONTINUE. IF THE PROCESSOR IS ALREADY
    1221    133
543 1222                        LAI 0           ;RUNNING THIS WILL HAVE NO EFFECT.
    1222    006
    1223    000
544 1224                        OUT REG5
    1224    133
545 1225                        JMP SRDISP      ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
    1225    104
    1226    261
    1227    010
546
547
548                                             ;LOAD SWITCH REGISTER ROUTINE.
549                                             ;THIS ROUTINE SERVICES THE LSR KEY FUNCTION.
550                                             ;LOADS TEMPORARY AREA INTO THE SWITCH
551                                             ;REGISTER IMAGE AREA THEN LOADS THE SWITCH
552                                             ;REGISTER AND SETS SR DISP INDICATOR.
553 1230        LSR1:   LLI 10          ;SET MEMORY POINTER TO TEMPORARY AREA AND
    1230    066
    1231    010
554 1232                        LA M            ;MOVE TWO WORDS TO REGISTERS A AND B.
    1232    307
555 1233                        IN L
    1233    060
556 1234                        LB M
    1234    317
557 1235                        LLI 16          ;RESET MEMORY POINTER TO SWITCH REGISTER
    1235    066
    1236    016
558 1237                        LM A            ;IMAGE AREA AND LOAD MEMORY FROM REGISTERS
    1237    370
559 1240                        IN L            ;A AND B.
    1240    060
560 1241                        LM B
    1241    371
561 1242                        CAL SRLD        ;CALL THE SR LOAD SUBROUTINE AND
    1242    106
    1243    250
    1244    010
562 1245                        JMP SRDISP      ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
    1245    104
    1246    261
    1247    010
563
564
565                                             ;SR LOAD SUBROUTINE.
566                                             ;THIS SUBROUTINE LOADS THE SWITCH REGISTER
567                                             ;WITH THE CONTENTS OF THE SWITCH REGISTER
568                                             ;IMAGE AREA IN RAM.THIS SUBROUTINE IS USED
569                                             ;BY THE LOAD SWITCH REGISTER ROUTINE AND
570                                             ;AFTER DATO'S TO RESTORE THE SWITCH REGISTER.
571 1250        SRLD:   LLI 16          ;SET MEMORY POINTER TO SWITCH REGISTER IMAGE AREA
    1250    066
    1251    016
572 1252                        LB M            ;AND LOAD THE LOW BYTE OF THE SWITCH REGISTER
    1252    317
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```

```
573 1253                LA B            ;WITH THE FIRST WORD.
    1253    301
574 1254                OUT SRLB
    1254    127
575 1255                IN L
    1255    060
576 1256                LA M            ;LOAD THE HIGH BYTE OF THE SWITCH REGISTER
    1256    307
577 1257                OUT SRHB        ;WITH THE NEXT WORD FROM MEMORY.
    1257    131
578 1260                RET
    1260    007
579
580
581                                     ;SWITCH REGISTER DISPLAY ROUTINE.
582                                     ;THIS ROUTINE MOVES THE CONTENTS OF THE
583                                     ;SWITCH REGISTER IMAGE AREA OF RAM TO THE
584                                     ;DISPLAY AREA OF RAM AND SETS THE SWITCH
585                                     ;REGISTER DISPLAYED (SR DISP) INDICATOR.
586 1261        SRDISP: LLI 16
    1261    066
    1262    016
587 1263                LCI 0
    1263    026
    1264    000
588 1265                LA M
    1265    307
589 1266                IN L
    1266    060
590 1267                LB  M
    1267    317
591 1270                LLI 0
    1270    066
    1271    000
592 1272                LM A
    1272    370
593 1273                IN L
    1273    060
594 1274                LM B
    1274    371
595 1275                IN L
    1275    060
596 1276                LM C
    1276    372
597 1277                LAI 40
    1277    006
    1300    040
598 1301                OUT REG6
    1301    135
599 1302                JMP DISP1
    1302    104
    1303    023
    1304    000
600
601
602                                     ;LOAD ADDRESS ROUTINE.
603                                     ;THIS ROUTINE SERVICES THE LAD KEY FUNCTION
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
```

```
542 1221                    OUT REG5        ;TO CONTINUE. IF THE PROCESSOR IS ALREADY
    1221    133
543 1222                    LAI 0           ;RUNNING THIS WILL HAVE NO EFFECT.
    1222    006
    1223    000
544 1224                    OUT REG5
    1224    133
545 1225                    JMP SRDISP      ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
    1225    104
    1226    261
    1227    010
546
547
548                                         ;LOAD SWITCH REGISTER ROUTINE.
549                                         ;THIS ROUTINE SERVICES THE LSR KEY FUNCTION.
550                                         ;LOADS TEMPORARY AREA INTO THE SWITCH
551                                         ;REGISTER IMAGE AREA THEN LOADS THE SWITCH
552                                         ;REGISTER AND SETS SR DISP INDICATOR.
553 1230        LSR1:   LLI 10              ;SET MEMORY POINTER TO TEMPORARY AREA AND
    1230    066
    1231    010
554 1232                    LA M            ;MOVE TWO WORDS TO REGISTERS A AND B.
    1232    307
555 1233                    IN L
    1233    060
556 1234                    LB M
    1234    317
557 1235                    LLI 16          ;RESET MEMORY POINTER TO SWITCH REGISTER
    1235    066
    1236    016
558 1237                    LM A            ;IMAGE AREA AND LOAD MEMORY FROM REGISTERS
    1237    370
559 1240                    IN L            ;A AND B.
    1240    060
560 1241                    LM B
    1241    371
561 1242                    CAL SRLD        ;CALL THE SR LOAD SUBROUTINE AND
    1242    106
    1243    250
    1244    010
562 1245                    JMP SRDISP      ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
    1245    104
    1246    261
    1247    010
563
564
565                                         ;SR LOAD SUBROUTINE.
566                                         ;THIS SUBROUTINE LOADS THE SWITCH REGISTER
567                                         ;WITH THE CONTENTS OF THE SWITCH REGISTER
568                                         ;IMAGE AREA IN RAM.THIS SUBROUTINE IS USED
569                                         ;BY THE LOAD SWITCH REGISTER ROUTINE AND
570                                         ;AFTER DATO'S TO RESTORE THE SWITCH REGISTER.
571 1250        SRLD:   LLI 16              ;SET MEMORY POINTER TO SWITCH REGISTER IMAGE AREA
    1250    066
    1251    016
572 1252                    LB M            ;AND LOAD THE LOW BYTE OF THE SWITCH REGISTER
    1252    317
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```
573 1253                LA B            #WITH THE FIRST WORD.
    1253    301
574 1254                OUT SRLB
    1254    127
575 1255                IN L
    1255    060
576 1256                LA M            #LOAD THE HIGH BYTE OF THE SWITCH REGISTER
    1256    307
577 1257                OUT SRHB        #WITH THE NEXT WORD FROM MEMORY.
    1257    131
578 1260                RET
    1260    007
579
580
581                                     #SWITCH REGISTER DISPLAY ROUTINE.
582                                     #THIS ROUTINE MOVES THE CONTENTS OF THE
583                                     #SWITCH REGISTER IMAGE AREA OF RAM TO THE
584                                     #DISPLAY AREA OF RAM AND SETS THE SWITCH
585                                     #REGISTER DISPLAYED (SR DISP) INDICATOR.
586 1261        SRDISP: LLI 16
    1261    066
    1262    016
587 1263                LCI 0
    1263    026
    1264    000
588 1265                LA M
    1265    307
589 1266                IN L
    1266    060
590 1267                LB  M
    1267    317
591 1270                LLI 0
    1270    066
    1271    000
592 1272                LM A
    1272    370
593 1273                IN L
    1273    060
594 1274                LM B
    1274    371
595 1275                IN L
    1275    060
596 1276                LM C
    1276    372
597 1277                LAI 40
    1277    006
    1300    040
598 1301                OUT REG6
    1301    135
599 1302                JMP DISP1
    1302    104
    1303    023
    1304    000
600
601
602                                     #LOAD ADDRESS ROUTINE.
603                                     #THIS ROUTINE SERVICES THE LAD KEY FUNCTION
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
```

```
604                                     ;BY MOVING THE CONTENTS OF THE TEMPORARY
605                                     ;AREA OF RAM TO THE UNIBUS ADDRESS POINTER
606                                     ;AREA OF RAM AND BY ZEROING THE TEMPORARY
607                                     ;AREA.
608 1305          LAD1:   LAI 0         ;CLEAR ANY INDICATORS.
    1305    006
    1306    000
609 1307                  OUT REG6
    1307    135
610 1310                  LLI 10        ;MOVE TEMPORARY TO UNIBUS ADDRESS POINTER.
    1310    066
    1311    010
611 1312                  LC M
    1312    327
612 1313                  IN L
    1313    060
613 1314                  LB M
    1314    317
614 1315                  IN L
    1315    060
615 1316                  LA M
    1316    307
616 1317                  NDI 3
    1317    044
    1320    003
617 1321                  IN L
    1321    060
618 1322                  LM C
    1322    372
619 1323                  IN L
    1323    060
620 1324                  LM B
    1324    371
621 1325                  IN L
    1325    060
622 1326                  LM A
    1326    370
623 1327          CLR1:   LAI 0
    1327    006
    1330    000
624 1331                  OUT REG6
    1331    135
625 1332          CLR2:   LLI 10        ;CLEAR THE TEMPORARY AREA.
    1332    066
    1333    010
626 1334                  LM A
    1334    370
627 1335                  IN L
    1335    060
628 1336                  LM A
    1336    370
629 1337                  IN L
    1337    060
630 1340                  LM A
    1340    370
631 1341                  JMP MOV1
    1341    104
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```

```
    1342    042
    1343    001
632
633
634                                     ;DISPLAY ADDRESS ROUTINE.
635                                     ;THIS ROUTINE SERVICES THE DIS AD KEY
636                                     ;FUNCTION. IT MOVES THE UNIBUS ADDRESS POINTER
637                                     ;TO THE DISPLAY AREA OF RAM.
638 1344        DISPAD: LAI 0
    1344    006
    1345    000
639 1346                OUT REG6        ;CLEAR INDICATORS.
    1346    135
640 1347                LLI 15
    1347    066
    1350    015
641 1351                LA M
    1351    307
642 1352                NDI 3           ;CLEAR EXAMINE AND DEPOSIT FLAGS.
    1352    044
    1353    003
643 1354                LM A
    1354    370
644 1355                LLI 13          ;SET MEMORY POINTER TO UNIBUS ADDRESS POINTER AND
    1355    066
    1356    013
645 1357                JMP MOV2        ;JUMP TO MOVE ROUTINE TO MOVE THE DATA INTO DISPLAY.
    1357    104
    1360    044
    1361    001
646
647
648                                     ;HALT TEST SUBROUTINE.
649                                     ;THIS ROUTINE TESTS TO SEE IF THE
650                                     ;PROCESSOR IS HALTED.
651 1362        HLTST:  INP REG5
    1362    113
652 1363                NDI 40          ;IS HALT BUSY SET?
    1363    044
    1364    040
653 1365                JTZ DISP1       ;NO. GO TO DISPLAY.
    1365    150
    1366    023
    1367    000
654 1370                RET             ;YES. RETURN.
    1370    007
655 1371        NUM1:   LLI 6
    1371    066
    1372    006
656 1373                LA M
    1373    307
657 1374                NDI 10          ;CNTRL KEY DEPRESSED?
    1374    044
    1375    010
658 1376                JTZ NUM1X       ;NO. GO TO DIGIT 1 ROUTINE.
    1376    150
    1377    004
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```

```
    1400    001
659 1401        MAINT1: LHI 40          ;YES. MAINTENANACE MODE!!!
    1401    056
    1402    040
660 1403                LAI 100         ;DO NOT LOOK FOR PROGRAMMED HALTS AND
    1403    006
    1404    100
661 1405                OUT REG6        ;SET THE MAINTENANCE MODE INDICATOR.
    1405    135
662 1406                LLI 0           ;READ IN 12 BITS OF MPC AND DISPLAY.
    1406    066
    1407    000
663 1410                INP REG6
    1410    115
664 1411                LM A
    1411    370
665 1412                IN L
    1412    060
666 1413                INP REG7
    1413    117
667 1414                NDI 17
    1414    044
    1415    017
668 1416                LM A
    1416    370
669 1417                IN L
    1417    060
670 1420                LMI 0
    1420    076
    1421    000
671 1422        MAINT2: CAL DISP15      ;CALL THE DISPLAY SUBROUTINE.
    1422    106
    1423    031
    1424    000
672 1425                LBI 0           ;THE FOLLOWING IS THE KEYSERVICE ROUTINE
    1425    016
    1426    000
673 1427                LEI 200         ;FOR THOSE KEY FUNCTIONS AVAILABLE IN
    1427    046
    1430    200
674 1431                LLI 3           ;MAINTENANCE MODE.
    1431    066
    1432    003
675 1433                LA M
    1433    307
676 1434                RAR
    1434    032
677 1435                JTC MDISAD
    1435    140
    1436    107
    1437    011
678 1440                RAR
    1440    032
679 1441                RAR
    1441    032
680 1442                RAR
    1442    032
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```

```
681 1443                        JTC MCLR
    1443    140
    1444    154
    1445    011
682 1446                        IN L
    1446    060
683 1447                        IN L
    1447    060
684 1450                        LA M
    1450    307
685 1451                        RAR
    1451    032
686 1452                        JTC MDSDAT
    1452    140
    1453    126
    1454    011
687 1455                        RAR
    1455    032
688 1456                        JTC TAKBUS
    1456    140
    1457    201
    1460    011
689 1461                        IN L
    1461    060
690 1462                        IN L
    1462    060
691 1463                        LA M
    1463    307
692 1464                        RAR
    1464    032
693 1465                        JTC MHLT
    1465    140
    1466    162
    1467    011
694 1470                        RAR
    1470    032
695 1471                        JTC MCONT1
    1471    140
    1472    143
    1473    011
696 1474                        RAR
    1474    032
697 1475                        JTC MBOOT
    1475    140
    1476    207
    1477    011
698 1500                        RAR
    1500    032
699 1501                        JTC MSTRT1
    1501    140
    1502    173
    1503    011
700 1504                        JMP MAINT2
    1504    104
    1505    022
    1506    011
701 1507        MDISAD: LLI 0           ;READ IN UNIBUS ADDRESS LINES AND DISPLAY.
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```

```
     1507    066
     1510    000
 702 1511                INP REG2
     1511    105
 703 1512                LM A
     1512    370
 704 1513                IN L
     1513    060
 705 1514                INP REG3
     1514    107
 706 1515                LM A
     1515    370
 707 1516                IN L
     1516    060
 708 1517                INP REG4
     1517    111
 709 1520                NDI 3
     1520    044
     1521    003
 710 1522                LM A
     1522    370
 711 1523                JMP MAINT2
     1523    104
     1524    022
     1525    011
 712 1526        MDSDAT: LLI 0           ;READ IN UNIBUS DATA LINES AND DISPLAY.
     1526    066
     1527    000
 713 1530                INP DBLB
     1530    101
 714 1531                LM A
     1531    370
 715 1532                IN L
     1532    060
 716 1533                INP DBHB
     1533    103
 717 1534                LM A
     1534    370
 718 1535                IN L
     1535    060
 719 1536                LMI 0
     1536    076
     1537    000
 720 1540                JMP MAINT2
     1540    104
     1541    022
     1542    011
 721 1543        MCONT1: LAI 300         ;ASSERT MANUAL CLOCK ENABLE AND MANUAL
     1543    006
     1544    300
 722 1545                OUT REG5        ;CLOCK BITS.
     1545    133
 723 1546                LAI 100         ;CLEAR MANUAL CLOCK BIT.
     1546    006
     1547    100
 724 1550                OUT REG5
     1550    133
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
```

```
725 1551                    JMP MAINT1
    1551    104
    1552    001
    1553    011
726 1554        MCLR:   LAI 0           ;CLEAR THE MAINTENANCE MODE INDICATOR AND
    1554    006
    1555    000
727 1556                    OUT REG6        ;JUMP OUT OF MAINTENANCE MODE VIA THE HALT ROUTINE.
    1556    135
728 1557                    JMP HLT15
    1557    104
    1560    037
    1561    010
729 1562        MHLT:   LAI 140         ;ASSERT MANUAL CLOCK ENABLE AND CLEAR BUS BITS.
    1562    006
    1563    140
730 1564                    OUT REG5
    1564    133
731 1565                    LAI 100         ;DROP CLEAR BUS BIT.
    1565    006
    1566    100
732 1567                    OUT REG5
    1567    133
733 1570                    JMP MAINT1
    1570    104
    1571    001
    1572    011
734 1573        MSTRT1: LAI 0           ;DROP MANUAL CLOCK ENABLE.
    1573    006
    1574    000
735 1575                    OUT REG5
    1575    133
736 1576                    JMP MAINT1
    1576    104
    1577    001
    1600    011
737 1601        TAKBUS: LAI 20          ;SET TAKE BUS BIT AND
    1601    006
    1602    020
738 1603                    OUT REG5        ;JUMP OUT OF MAINTENANCE MODE.
    1603    133
739 1604                    JMP MCLR
    1604    104
    1605    154
    1606    011
740 1607        MBOOT:  LAI 200         ;SET AND CLEAR THE BOOT BIT.
    1607    006
    1610    200
741 1611                    OUT REG6
    1611    135
742 1612                    LAI 0
    1612    006
    1613    000
743 1614                    OUT REG6
    1614    135
744 1615                    JMP MAINT1
    1615    104
KY11LB PROGRAM  RT-11 MACRO VM02-10     00:13:25 PAGE 8+
```

```
     1616    001
     1617    011
745  1620        NUM7:   LLI 6
     1620    066
     1621    006
746  1622                LA M
     1622    307
747  1623                NDI 10          ;CNTRL KEY DEPRESSED?
     1623    044
     1624    010
748  1625                JTZ NUM7X       ;NO. GO TO DIGIT 7 ROUTINE.
     1625    150
     1626    376
     1627    000
749  1630                LCI 2           ;OFFSET ADDRESS CALCULATED BY ADDING THE
     1630    026
     1631    002
750  1632                LLI 14          ;UNIBUS ADDRESS POINTER TO TEMPORARY PLUS
     1632    066
     1633    014
751  1634        ADD:    LB M            ;TWO.
     1634    317
752  1635                DC L
     1635    061
753  1636                LA M
     1636    307
754  1637                LLI 10
     1637    066
     1640    010
755  1641                AD C
     1641    202
756  1642                AD M
     1642    207
757  1643                LM A
     1643    370
758  1644                IN L
     1644    060
759  1645                LA B
     1645    301
760  1646                AC M
     1646    217
761  1647                LM A
     1647    370
762  1650                JMP MOV1        ;DISPLAY ANSWER IN TEMPORARY.
     1650    104
     1651    042
     1652    001
763  1653        NUM6:   LLI 6
     1653    066
     1654    006
764  1655                LA M
     1655    307
765  1656                NDI 10          ;CNTRL KEY DEPRESSED?
     1656    044
     1657    010
766  1660                JTZ NUM6X       ;NO. GO TO DIGIT 6 ROUTINE.
     1660    150
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
```

```
    1661    377
    1662    000
767 1663                LCI 0           ;YES. SET UP MEMORY POINTER TO ADD
    1663    026
    1664    000
768 1665                LLI 17          ;THE SWITCH REGISTER IMAGE TO TEMPORARY
    1665    066
    1666    017
769 1667                JMP ADD         ;PLUS ZERO.
    1667    104
    1670    234
    1671    011
770                                     ;THATS IT FOLKS!!!!
771      000001'        .END
KY11LB PROGRAM  RT-11 MACRO VM02-10    00:13:25 PAGE 8+
SYMBOL TABLE

A     = 000000          ADD     001634          B     = 000001
BADLD   000744          BEGIN   000001          BEG1    000016
BOOT1   000463          BUSERR  000657          C     = 000002
CLR1    001327          CLR2    001332          CONT1   001212
D     = 000003          DATI1   000630          DATI2   000643
DATO1   000761          DBHB  = 000001          DBLB  = 000000
DEP1    000671          DEP2    000715          DISPAD  001344
DISP1   000023          DISP15  000031          DISP2   000062
DISP3   000132          DISP4   000136          DISP45  000137
DISP5   000163          E     = 000004          EXAM1   000507
EXAM2   000530          GPRT1   000574          GPRT2   000624
GPRT3   000627          H     = 000005          HLTST   001362
HLT1    001023          HLT15   001037          HLT2    001042
HLT25   001046          HLT3    001067          INCAD   000551
INITX   001130          INITX2  001137          INIT1   001111
KEYS  = 000005          KEYSEV  000175          L     = 000006
LAD1    001305          LSR1    001230          M     = 000007
MAINT1  001401          MAINT2  001422          MBOOT   001607
MCLR    001554          MCONT1  001543          MDISAD  001507
MDSDAT  001526          MDTST   000365          MEM2    001001
MHLT    001562          MOV1    000442          MOV2    000444
MSTRT1  001573          NUMX    000407          NUM0  = 000405
NUM0X   000405          NUM1    001371          NUM1X   000404
NUM2  = 000403          NUM2X   000403          NUM3  = 000402
NUM3X   000402          NUM4  = 000401          NUM4X   000401
NUM5  = 000400          NUM5X   000400          NUM6    001653
NUM6X   000377          NUM7    001620          NUM7X   000376
NXT     000052          OVER    000013          REG0  = 000000
REG1  = 000001          REG2  = 000002          REG3  = 000003
REG4  = 000004          REG5  = 000005          REG6  = 000006
REG7  = 000007          SHFT1   000335          SHFT2   000343
SRDISP  001261          SRHB  = 000004          SRLB  = 000003
SRLD    001250          SS1     001034          START   000000
STRT1   001150          TAKBUS  001601          TIMER   001133

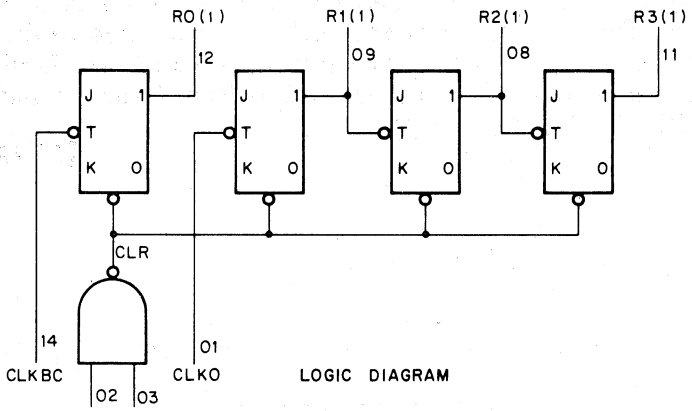
. ABS.  001672     000
        000000     001
ERRORS DETECTED: 0
FREE CORE: 15380. WORDS

TEXT,TEXT=M8008E,TEXT

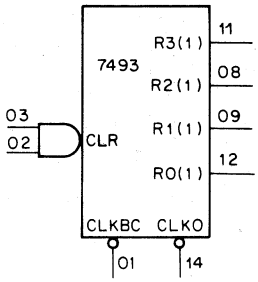
*
```

APPENDIX B
IC DESCRIPTIONS

7493 BINARY COUNTER



LOGIC DIAGRAM



V_{CC} = PIN 05
GND = PIN 10

7493 TRUTH TABLE
(SEE NOTES)

CLKBC INPUT PULSE	OUTPUT			
	(1)	R1 (1)	R2 (1)	R3 (1)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

0 = LOW 1= HIGH

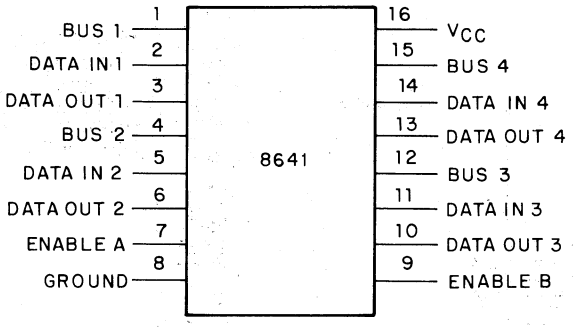
Notes:

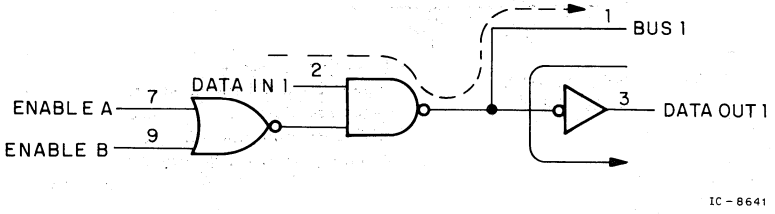
1. Truth table applies when 7493 is used as 4-bit ripple – through counter.
2. Output RO(1) connected to input CLK0.
3. To reset all outputs to logical 0 both pins 02 and 03 inputs must be high.
4. Either (or both) reset inputs $R_{0(1)}$ (pins 02 and 03) must be low to count.

IC-7493

8641 QUAD BUS TRANSCEIVER

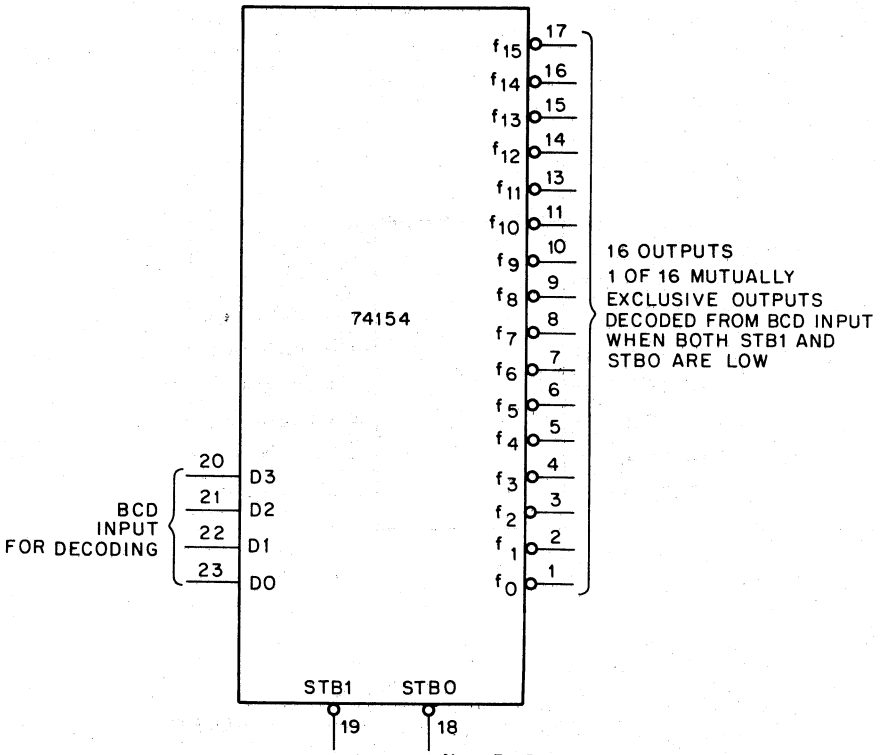
The 8641 consists of four identical receiver/drivers and a single enabling gate in one package for interfacing with the PDP-11 Unibus. The transceiver drivers are enabled when ENABLE A and ENABLE B are both low. The other input of each driver is connected to the data to be sent to the Unibus. For example, when enabled, DATA IN 1 (pin 2) is read to the Unibus via BUS 1 (pin 1). During a write operation, data comes from the Unibus as BUS 1 (pin 1) and is passed through the receiver to the device as DATA OUT 1 (pin 3).





74154 4-LINE TO 16-LINE DECODER

The 74154 4-Line to 16-Line Decoder decodes four binary-coded inputs into one of 16 mutually-exclusive outputs when both strobe inputs (G1 and G2) are low. The decoding function is performed by using the four input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.



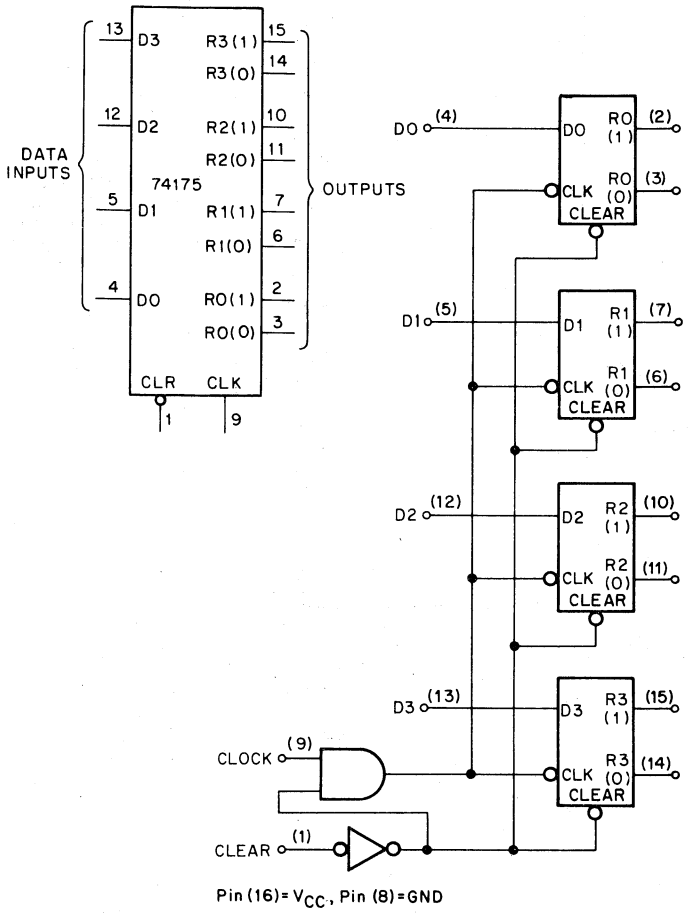
74175 QUAD STORAGE REGISTER

TRUTH TABLE

INPUT t_n	OUTPUTS t_{n+1}
D	R(1) R(0)
H	H L
L	L H

t_n = Bit time before clock pulse.

t_{n+1} = Bit time after clock pulse.



Pin (16) = V_{CC}, Pin (8) = GND

IC-74175

Reader's Comments

KY11-LB Programmer's Console/Interface
Module Operation and Maintenance Manual
EK-KY1LB-MM-001

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