DFC11-A EIA level converter/clock recovery module maintenance manual

EK-DFC11-MM-002

DFC11-A EIA level converter/clock recovery module maintenance manual

digital equipment corporation · maynard. massachusetts

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ILLUSTRATIONS

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual contains information concerning the DFC11-A EIA Level Converter/Clock Recovery module (M5942). Included is a list of specifications covering the module's performance and I/O requirements, instructions for its installation in various systems, the theory of operation, and maintenance information.

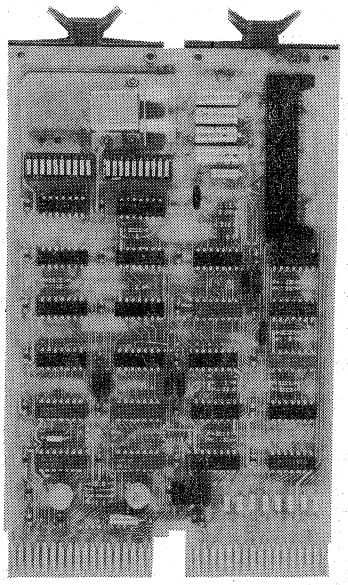
This chapter consists of a general description of the module's purpose and use, a physical description, and a list of specifications.

1.2 GENERAL DESCRIPTION

The DFC11-A is an EIA level converter that is compatible with the DF11-A specifications for synchronous interfaces and with the RS-232-C/CCITT for baud rates up to 10,000 and cable lengths up to 50 feet. The unit has provision for either a synchronous clock option that provides a clock source on EIA/CCITT transmit element timing lead (DTE), pin 24, or a clock recovery option. Baud rates are 300, 600, 1200, 2400, 4800, and 9600. Frequencies are crystal-controlled to 0.05 percent at a crystal frequency of 614.4 kHz.

The clock recovery option is used with EIA synchronous interfaces when connected to an asynchronous data set or equivalent. A crystal clock source is provided for the transmitter and receiver. In addition, the receiver clock source is synchronized with the incoming data by the carrier detector.

The DFC11-A will operate with a DP11, DU11, or any other synchronous interface which has access to a DF11 slot. It will not operate in a DM11 or DH11 distribution panel.



7406-1

Figure 1-1 DFC11-A EIA Level Converter/Clock Recovery Module

1.3 PHYSICAL DESCRIPTION

The DFC11-A consists of an 8-1/2 inch by double module (type M5942). Pinning is per DF11 specifications. The module, shown in Figure 1-1, accepts either a BC05C-25 or a BC05C-50 cable.

Power requirements are +5 Vdc at 400 mA, +15 Vdc at 22 mA, and -15 Vdc at 20 mA. The temperature range is 10° to 50° C at 90 percent humidity (noncondensing).

All DFC11-A operating power is derived from the mounting panel in which it is installed.

1.4 SPECIFICATIONS

I/O Specifications

Data Set Side

Meets failsafe RS-232-C/CCITT for baud rates up to 10,000 and cable lengths to 50 feet.

Interface Side

TTL compatible

General

TTL/EIA voltage level relationships are noninverting.

Performance Specifications

Baud Rates

300, 600, 1200, 2400, 4800, 9600, and 19,200 baud (0.05% tolerance) (switch selectable)

Transmit (TX) Clock

With Clock Recovery: Taken from pin 15 of EIA/CCITT cable connector, sourced to pin 24.

Without Clock Recovery: Internal transmit clock always ON to interface.

NOTE

Interface should change transmitted data only on positive edges (0 to +3 V) of transmit clock.

Receive (RX) Clock

With Clock Recovery: Reconstructed clock from a source clock. No more than 6.25% distortion from shifted strobe time from bit center.

Without Clock Recovery: Taken from pin 17 of EIA/CCITT cable connector.

By switch selection, may be turned on either by first received data Mark-to-Space transition, or by a carrier Off-to-On transition.

By switch selection, may be resynchronized by any data Mark-to-Space transition, or not synchronized from turn-on.

By switch selection, may be turned off by no data transition for 0.5 second, or by a carrier On-to-Off transition.

NOTE

Received data should be strobed on negative edge of clock (+3 to 0 V).

Request To Send

May be switched to always ON (EIA).

Clear To Send

By switch selection, may be forwarded to interface at delays of 0, 0.1, 0.2, or 0.3 second.

Ring

Contains extra capacitors and threshold adjustments for an unterminated connection.

NOTE

The DFC11-A is capable of functioning as a normal DF11-A.

CHAPTER 2
INSTALLATION

2.1 GENERAL

Installation of the DFC11-A consists of unpacking, inspection, connection, and checkout of the unit in a system. At present, the module is intended for use with two configurations: systems using a DU11 Synchronous Interface and systems using a DP11-A Synchronous Line Interface. This chapter covers installation of the DFC11-A in these configurations. As future options become available, instructions pertaining to DFC11-A installation will appear in documents covering those options.

2.2 UNPACKING AND INSPECTION

Unpack the DFC11-A and check the contents of the package against the shipping list. It should contain an M5942 module, a maintenance manual, and a diagnostic tape MAINDEC-11-DZDFA-A-D.

Check exposed leads for apparent damage. Inspect the module for damage during shipment, such as loose components or abrasions to the module itself.

2.3 INSTALLATION AND CHECKOUT

There are two applications in which the DFC11-A can be installed. One is in a system with a DU11-A and a DD11-B peripheral mounting panel, in which the DU11-A interfaces the Bell 201 synchronous modem or equivalent; the other is with a DP11 and a 200 series modem. In the latter configuration, power is derived either from the computer or from a BA11 mounting box.

2.3.1 DU11 Installation Procedure

If the DFC11-A is to be used in a system with a DU11, a DD11-B mounting panel or equivalent (with DD11-B ECO No. 3 or higher) is required. Proceed as follows:

1. Remove power from the system and install the DU11 in module slots C, D, E, and F2 and/or C, D, E, and F3 (Figure 2-1).

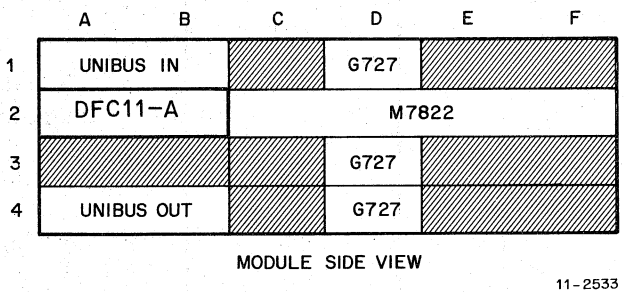


Figure 2-1 DFC11-A Location in DU11 System

2. Mount the DFC11-A in slots AB2 and/or AB3.

NOTE

Grant Continuity module (G727) is inserted in each slot that does not receive an interface logic module.

3. Plug the BC05C cable (which comes with the DU11) into the Berg connector on the DFC11-A module and into the H315 test connector at the other end.
4. Set the switches on the module per the requirements of the installation (Table 2-1). Software documentation also contains these settings.
5. On the A portion of the board, cut jumpers EIA (2) and 811 (1).
6. Once installed, return power to the system and check out by running MAINDEC-11-DZDFA-A-D for 15 minutes. It should run error free.
7. When checked out, remove power, remove the H315 test connector, and connect the cable to the modem.
8. Return power and restore the system to normal.

Table 2-1
DFC11-A Switch Position/Function

Switch	Position	Function
S1-2	ON	Enable DFC11-A. **NOTE** **This switch must be ON for the module to operate; one switch of S2-3 through 10 must also be ON to select the clock for clock recovery.**
S1-2	OFF	Disable DFC11-A. **NOTE** **In this position the module operates as a DF11-A. S1-8 ON supplies the external clock.**
S1-1	ON	RX clock turned on by carrier Off-to-On transition.
S1-3	ON	RX clock turned on by first receive data Mark-to-Space transition.
S1-4	ON	RX clock resynchronized by any Mark-to-Space data transition.
S1-5	OFF	RX clock turned off by no data transition after a period of 0.5 second.
S1-5	ON	RX clock turned off by On-to-Off carrier transition.
S1-10	OFF	Request To Send always on.
S1-9	ON	Clear To Send with no delay.
S1-9 OFF S1-6 ON		Clear To Send with 0.1-second delay.
S1-9 OFF S1-7 ON		Clear To Send with 0.2-second delay.
S1-9 OFF S1-6 ON S1-7 ON		Clear To Send with 0.3-second delay.
S2-3– S2-10		Select baud rate.

2.3.2 DP11 Installation Procedure

If the DFC11-A is to be used in a system with a DP11, a BC05C cable is required. Proceed as follows:

1. Remove power from the system and install the DFC11-A in slot CD4 (Figure 2-2).

2. Plug the BC05C cable into the Berg connector on the DFC11-A module and into the DP11 test connector at the other end.

3. Set switches on the DFC11-A per Table 2-1. The software documentation also contains these settings.

4. On the A portion of the board, cut jumpers EIA (2), 811 (1), and BUSY (1).

5. Once installed, return power to the system and check out by running MAINDEC-11-DZDFA-A-D for 15 minutes. It should run error free.

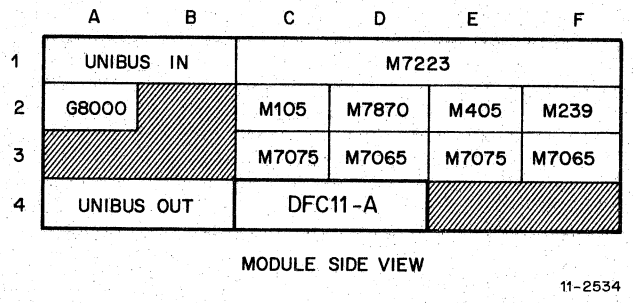


Figure 2-2 DFC11-A Location in DP11 System

6. When checked out, remove power, remove the test connector, and connect the cable to the modem.

7. Return power and restore the system to normal.

CHAPTER 3
THEORY OF OPERATION

3.1 FUNCTIONAL BLOCK DIAGRAM DISCUSSION

A functional block diagram of the DFC11-A is shown in Figure 3-1. This should be referenced to Schematic Drawing D-CS-5942-0-1 (Chapter 5).

The DFC11-A is an EIA/TTL and TTL/EIA level converter that contains a crystal clock with a chain of dividers. Circuits are included to enable the DFC11-A to function as a clock source or as a synchronizer for the incoming data.

The option consists of the following functional blocks of logic (Figure 3-1):

1. Two noninverting level converters that transform the signals to and from both the modem and the interface.
2. An internal clock that feeds a divider.
3. A divider chain that feeds the transmit and receive clock logic.
4. Clock synchronization logic that is activated by either received data or a Carrier Detect signal.
5. Clear To Send logic with provision to vary the amount of delay.

3.2 DETAILED LOGIC DISCUSSION

The following discussions are keyed to the blocks contained in Figure 3-1 and Drawing D-CS-5942-0-1. For detailed information concerning integrated circuits (ICs), refer to Appendix A.

3.2.1 Clock Generation Logic

A block diagram of the clock logic is shown in Figure 3-2. This is a standard clock configuration using a 614.4 kHz crystal, a pair of 380s, and a 74121 one-shot set for 40-ns. C35 and C36 control the circuit range. The circuit as configured can oscillate over a wide range of frequencies, but the range of crystals that can be utilized is limited by the response of the 1489 EIA receivers.

3.2.2 Clock Divider Logic

The clock divider logic is shown in Figure 3-3. The output of the basic clock oscillator is fed to a pair of 74197 frequency dividers in tandem. The 614.4 kHz is sequentially divided by two to produce the range of frequencies equal to 19,200 to 150 baud. The common points of eight switches may be selectively closed to the desired rate and fed to a pair of 74197s, where the signal is divided by 16 and separated into transmit and receive clocks.

3.2.3 Level Converter Logic

There are two sets of level converters in the DFC11-A. Level conversion is achieved by the use of EIA receivers (1489) and drivers (1488).

Figure 3-4 shows a typical EIA/TTL conversion circuit. The EIA signal is brought in and the TTL output is inverted by 7404s. These interface the Bell modems to the computer logic. All EIA level signals of +6 to +25 V (logic 0) and -6 to -25 V (logic 1) are converted to +3 V (logic 1) and 0 V (ground), representing a logic 0.

Figure 3-5 shows a typical TTL/EIA converter. These convert the logic level signals to the operating voltage levels of the Bell modems. All logic signals of 3 V or more are converted to -6 V or less. All ground (0 V) logic signals are converted to +6 V or more. The level converter threshold voltage is 3.0 V. Any inputs less than 3.0 V will not cause the converter to switch.

3.2.4 Clock Synchronization Logic

The clock synchronization logic is shown in Figure 3-6. With this circuit, the receiver clock may be resynchronized

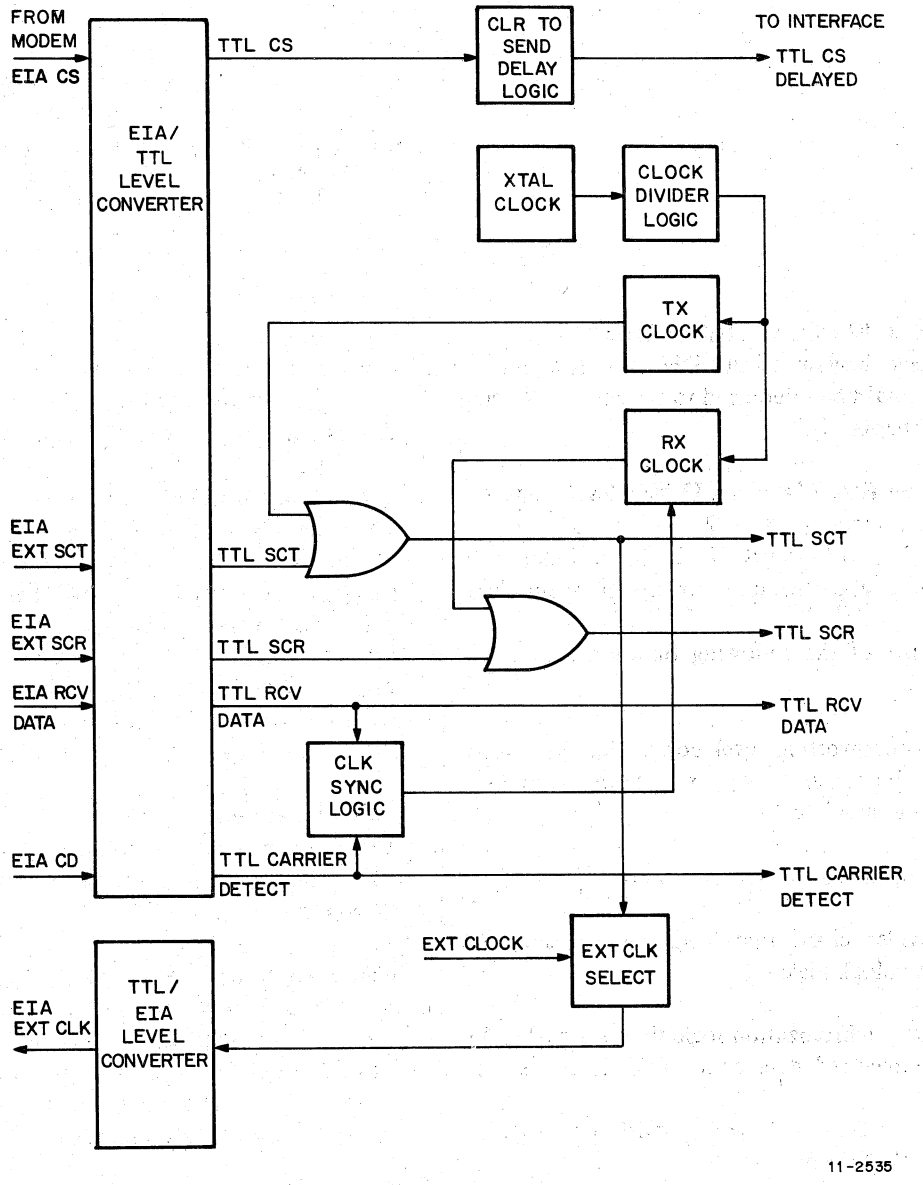


Figure 3-1 DFC11-A Functional Block Diagram

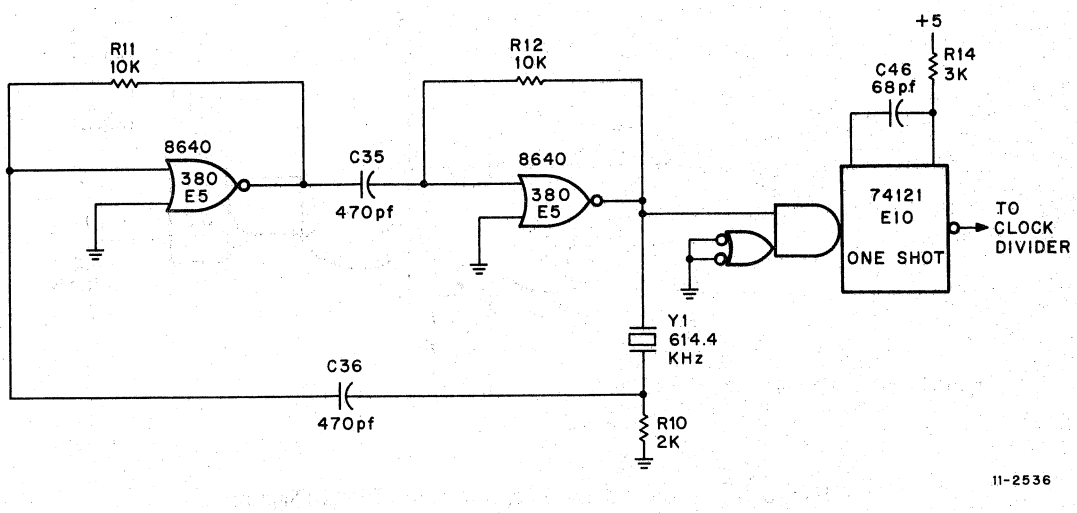


Figure 3-2 Clock Logic Block Diagram

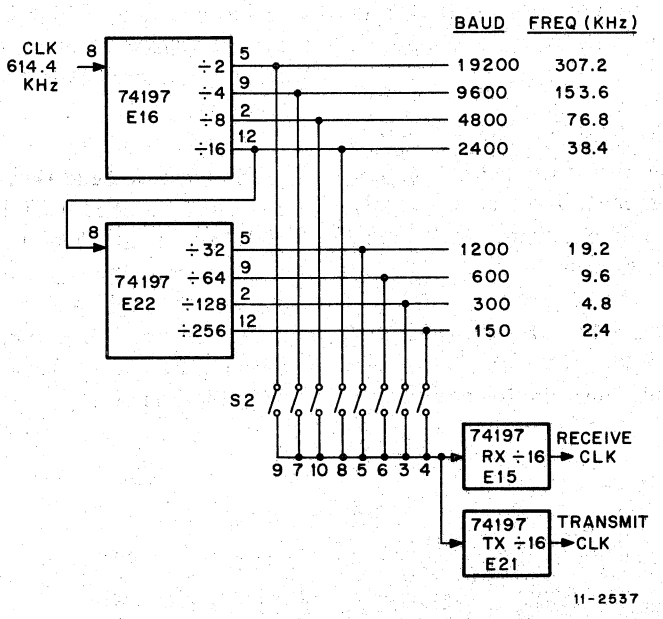


Figure 3-3 Baud Rate Selection

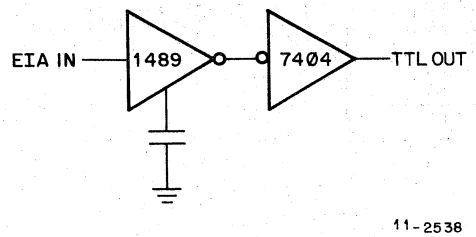


Figure 3-4 EIA/TTL Level Converter

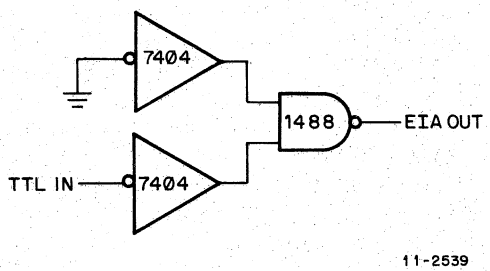


Figure 3-5 TTL/EIA Level Converter

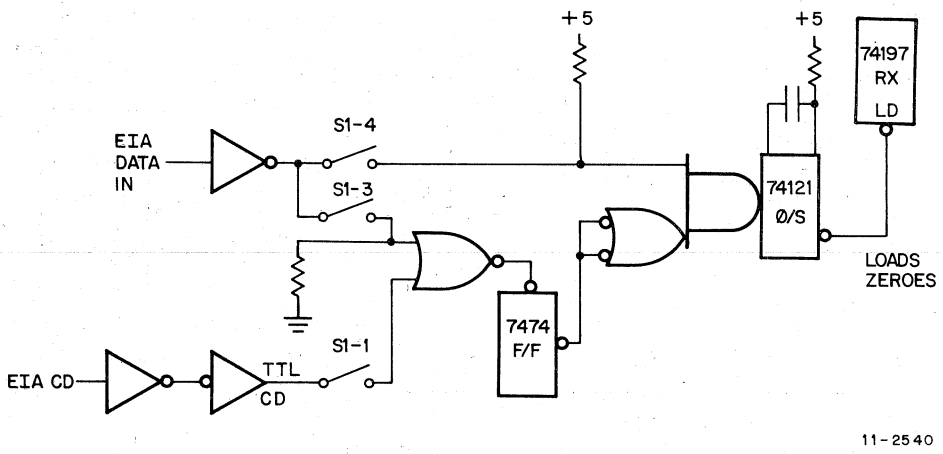


Figure 3-6 Clock Synchronization Logic Block Diagram

by any Mark-to-Space transition of data, by a Carrier Detect transition of Off-to-On, or not synchronized from turn-on. Selection of this option is by switches S1-3, S1-4, and S1-1.

This is the sync recovery feature of the DFC11-A. It is useful in situations in which the two clocks are not matched, or in systems using a modem that does not supply a clock. Without this feature, a free running clock would not guarantee accurate character timing.

As can be seen from the figure, when S1-3 is closed, any transition from high to low at the EIA input causes the one-shot to fire and, as a result, loads the Receiver Clock register (74197 at E15) with zeros. After this initial synchronization, if S1-4 is also closed, the receiver clock is resynchronized at every high-to-low transition. If S1-1 is closed, a Carrier Detect transition will perform the same function.

3.2.5 Clear To Send Delay Logic

The Clear To Send (CS) delay logic is shown in Figure 3-7. With this circuit, Clear To Send can be manipulated by sets of switches in the logic. With S1-9 closed, CS is propagated through the logic with no delay other than gate delays. If S1-9 is opened, CS is forced through the 74121 one-shot at E6 and, after a set delay, to the TTL CS output via the 7474 flip-flop at E7.

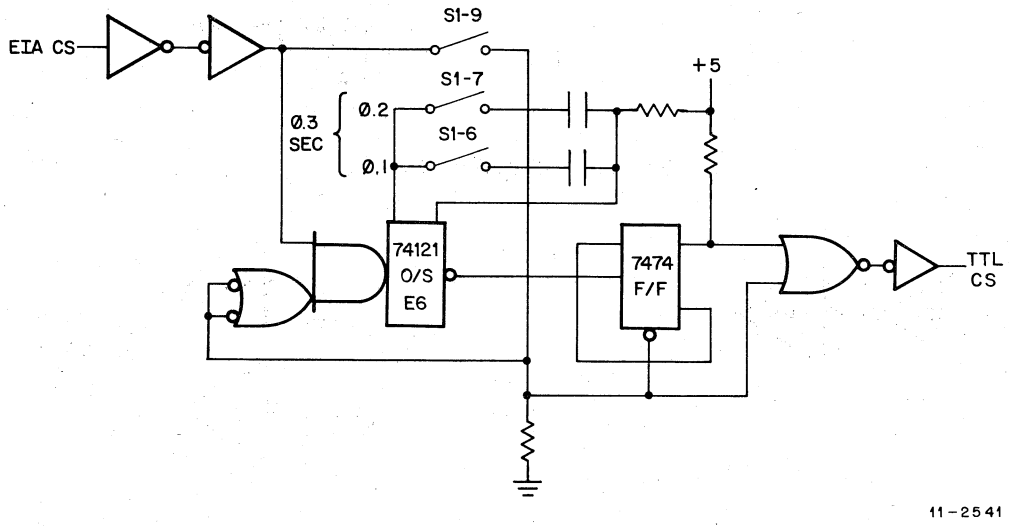


Figure 3-7 Clear To Send Delay Logic Block Diagram

Under these conditions, combinations of S1-6 and S1-7 control the amount of delay applied to the appearance of CS. Closing S1-6 applies a 0.1-second delay. Closing S1-7 increases the delay to 0.2 second. With both switches closed, the delay is set at 0.3 second. These figures are approximate and the timing here is not critical.

3.2.6 Clock Source Selection Logic

This is the clock recovery option (Figure 3-8) of the DFC11-A. This option is either enabled by S1-2 being closed, or disabled by S1-2 being open. When it is closed, EXT CLOCK (INT) is sourced from the DFC11-A internal clock source from the Transmit Clock register (TX). When it is open, the serial external clocks for transmit and receive are allowed to pass through at a TTL level.

When S1-8 is closed, the EXT CLK INT from the DFC11-A is sent out as EIA EXT CLOCK. With S1-8 open, the EXT CLK from outside is sent through as EIA EXT CLOCK.

3.2.7 DC Regulator

The dc regulator, composed of Q1, Q2, and zeners D1 and D2, serves to maintain the voltage supplied at 10 V.

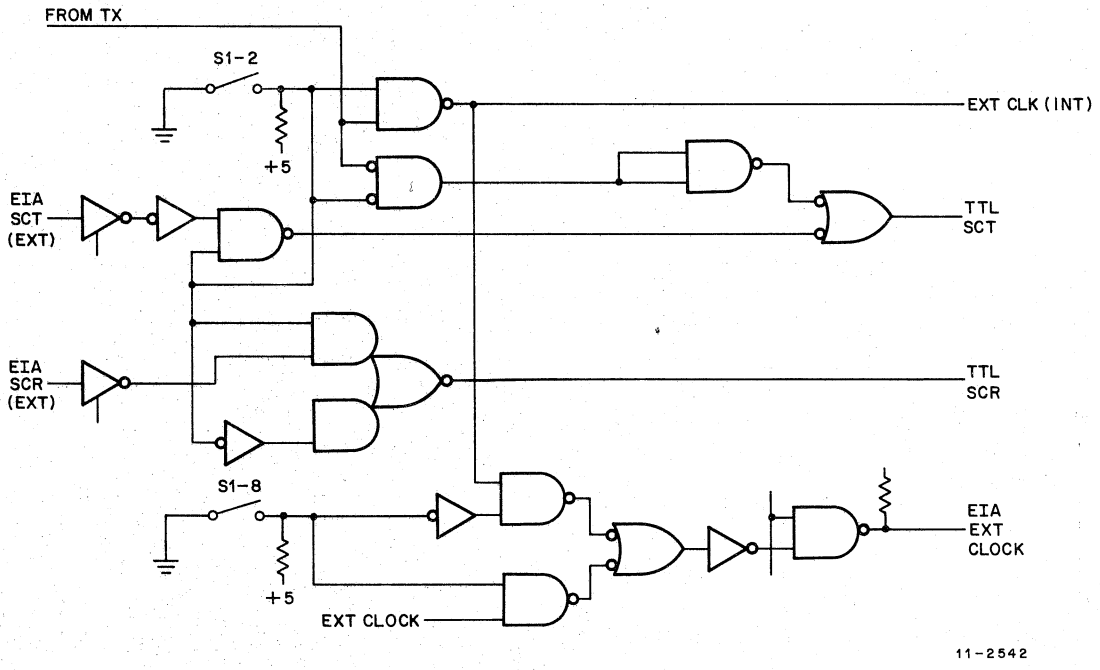


Figure 3-8 Clock Recovery Logic Block Diagram

CHAPTER 4
MAINTENANCE

4.1 MAINTENANCE PHILOSOPHY

Maintenance of the DFC11-A consists of running the DFC11-A diagnostic, MAINDEC-11-DZDFA-A-D, and following the instructions contained in the document supplied with the tape. The tape has provision for testing the DFC11-A with either a DU11 or a DP11.

4.2 MAINTENANCE PROCEDURES

If running the diagnostic indicates that a malfunction exists in the system in which the DFC11-A is installed, a check should be made to determine if the problem exists in the DU11 or DP11 interface. The diagnostic should indicate this. (Refer to the applicable maintenance manuals for procedures.) It should then be determined if the system modem is operating properly. Instructions for this can be found in the manuals supplied with the equipment.

Once the malfunction has been isolated to the DFC11-A, the next step is to swap cables to see if that corrects the problem. If it does not, troubleshooting techniques should be performed on the M5942, after a module that is known to be good has been swapped from spares.

It is beyond the scope of this manual to give detailed troubleshooting procedures for the M5942. The module is sufficiently unsophisticated so that standard techniques can be utilized.

A visual inspection can be performed to check for broken connectors, frayed or broken insulation, improper seating of the module, worn or bent contacts in the mounting panel, or overheated components.

Power supply voltages should be checked at the mounting panel source pins. Refer to the manual covering the particular panel for the specific system to determine the proper voltages, pins, and tolerances.

4.3 REPAIR PROCEDURES

When the M5942 module is to be repaired, standard troubleshooting techniques should be utilized in isolating the defective component using the theory discussions in Chapter 3 and the logic block schematics supplied as part of the manufacturing drawing set (Chapter 5).

A multimeter can be used to check for continuity or to measure the resistance of suspected components.

CAUTION

The X10 multimeter range is recommended for checking semiconductor devices.

Most multimeters apply a positive voltage to the common lead when adjusted for measuring resistance. Therefore, the polarity of the multimeter leads should be checked before measuring the resistance of semiconductor devices.

Only the input, output, and power terminals are available on ICs; thus, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is best done under dynamic conditions using a module extender to make terminals readily accessible.

When soldering semiconductor devices (transistors, diodes, rectifiers, or integrated circuits) that can be damaged by heat, physical shock, or excessive electrical current, use a heat sink, such as a pair of pliers, to grip the lead between the joint and device being soldered. Use a 6-V pencil--pointed-tip iron with an isolation transformer. The smallest iron adequate for the work should be used.

Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module etch.

To remove ICs, use a solder sucker to remove all excess solder from the contacts. Then, by straightening the leads, lift the IC from its terminal points. If it is not desired to save the defective component for test purposes, clip the IC leads close to the chip and remove the chip portion of the IC. Then apply heat to individual leads (side 2) and remove leads from side 1, using a pair of needlenose pliers. Do not hold the lead with pliers while applying heat; the pliers will act as a heat sink.

If the IC is to be saved, heat each hole individually (side 2), removing excess solder with a desoldering tool. Insert the new component, bending appropriate leads. (Only leads with tear drop lands should be bent. They should be bent in the direction of the point.) Clip protruding component leads from side 2. *Do not cut flush with the board.* Leads and solder joints should not exceed 1/16 inch from the bottom of the board.

Solder all leads on side 2 and clean flux from both sides of the board with trichlorethylene, Freon, or equivalent.

CAUTION

These cleaning agents will damage plastic handles.

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excess solder or flux on adjacent parts or service lines. When repair has been completed, remove all excess flux by washing the junction with a solvent such as trichlorethylene. Be very careful not to expose paint or plastic surfaces to this solvent.

CAUTION

Never attempt to remove solder from the terminal points by heating and rapping the module against another surface. This practice can result in module or component damage. Remove solder with a solder sucking tool or solderwick.

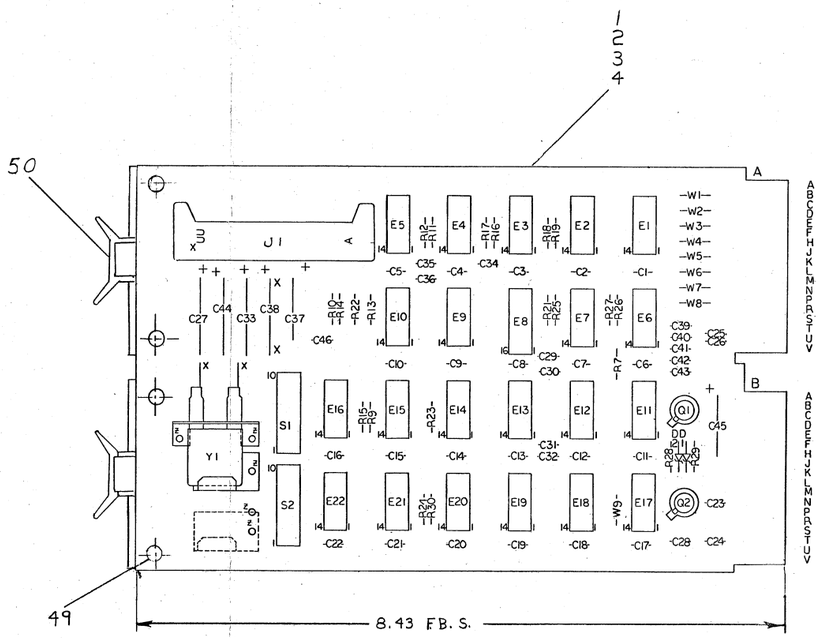
When removing any part for replacement, all leads or wires that are unsoldered or otherwise disconnected should be legibly tagged or marked for identification with their respective terminals. Always replace defective components with parts of equal or better quality and equal tolerance.

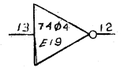
CHAPTER 5
MANUFACTURING DRAWING SET

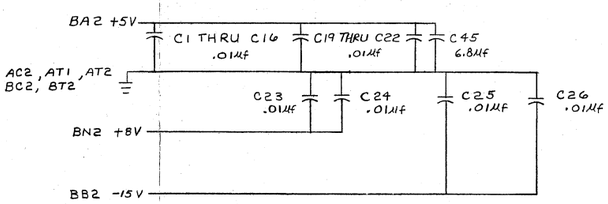
This chapter contains key manufacturing drawings for the DFC11-A. These drawings represent the levels of revision in existence at the time of this manual's publication. Further revisions will not be supplied until the manual is reprinted or revised. If in doubt about the revision of the equipment in use, contact Digital Equipment Corporation for the latest revisions of drawings.

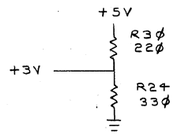
NOTES:

1. DEC 8640 REPLACES THE OBSOLETE DEC 380









DEC	86-10	1	8
IC TYPE		GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DEC FORM NO. DRD 135-0

REF				
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M5942-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M5942-0-5	2
REF		MODULE ECO HISTORY	B-MH-M5942-0-6	3
1		ETCHED CIRCUIT BOARD	5010815	4
2	C34,46	CAP 68 PF 100V 5%	1000014	5
9	C29,30,31,32,35,36,39,40,42	CAP 470 PF 100V 5%	1000024	6
1	C41	CAP 1000 PF 100V 5%	1000042	7
1	C33	CAP 68 UF 15V 10%	1000082	8
28	C1-26,28,43	CAP .01 UF 100V 20%	1001610-01	9
2	C27,44	CAP 22 UF 35V 20%	1002433	10
1	C38	CAP 20 UF 50V 10%	1002839	11
1	C37	CAP 10 UF 20V 10%	1004813	12
1	C45	CAP 6.8 UF 35V 10%	1005306	13
2	D1,2	DIODE IN758A	1100125	14
2		CRYSTAL SOCKET (8000 PG 1)	1202812	15
1	J1	CONN 40 PIN	1209941	16
2	S1,S2	SWITCH (10 POSITION)	1211164-06	17
2		SWITCH COVER	1211284-06	18
1	R30	RES 220 1/4W 5%	1300271	19
3	R24,28,29	RES 330 1/4W 5%	1300295	20
3	R18,19,27	RES 470 1/4W 5%	1300316	21
6	R9,13,16,21,23,26	RES 1K 1/4W 5%	1300365	22
2	R14,17	RES 3K 1/4W 5%	1300432	23
2	R11,12	RES 10K 1/4W 5%	1300479	24
1	R25	RES 15K 1/4W 5%	1300496	25
1	R7	RES 33K 1/4W 10%	1300510	26
1	R15	RES 750 1/4W 5%	1301401	27
1	R10	RES 2K 1/4W 5%	1302388	28
1	R22	RES 24K 1/4W 5%	1304837	29
1	Q1	TRANS. 2N2904	1501742	30
1	Q2	TRANS. 2N2219	1501881	31
1	Y1	CRYSTAL 614.4 KHZ	1805505-01	32
1	E7	I.C. DEC 7474	1905547	33
2	E1,4	I.C. DEC 7400	1905575	34
1	E9	I.C. DEC 7450	1905580	35
1	E2	I.C. DEC 7402	1909004	36
1	E5	I.C. DEC 8640	1911469	37
4	E13,14,19,20	I.C. DEC 7404	1909686	38
4	E15,16,21,22	I.C. DEC 74197	1910035	39
3	E3,6,10	I.C. DEC 74121	1910230	40
2	E17,E18	I.C. DEC 1488	1910322	41
2	E11,12	I.C. DEC 1489	1910323	42
1	E8	I.C. DEC 74123	1910436	43
1		REAR SUPPORT BRACKET	5302825	44
1		BRACKET FOR CRYSTAL	5303154	45
3		SCR PHIL PAN HD #2-56X.25	9006001-1	46
3		NUT KEX #2-56	9006555	47
9	W1-W9	JUMPER INSULATED	9009185	48
4		EYELET #GS4-7	9006732	49
2		HANDLE FLIP CHIP, MAGENTA	9008337-06	50
				51
2		CAP TRANSISTOR PLASTIC	9008351-00	52
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: DFC11-A

ETCH BOARD REV: D

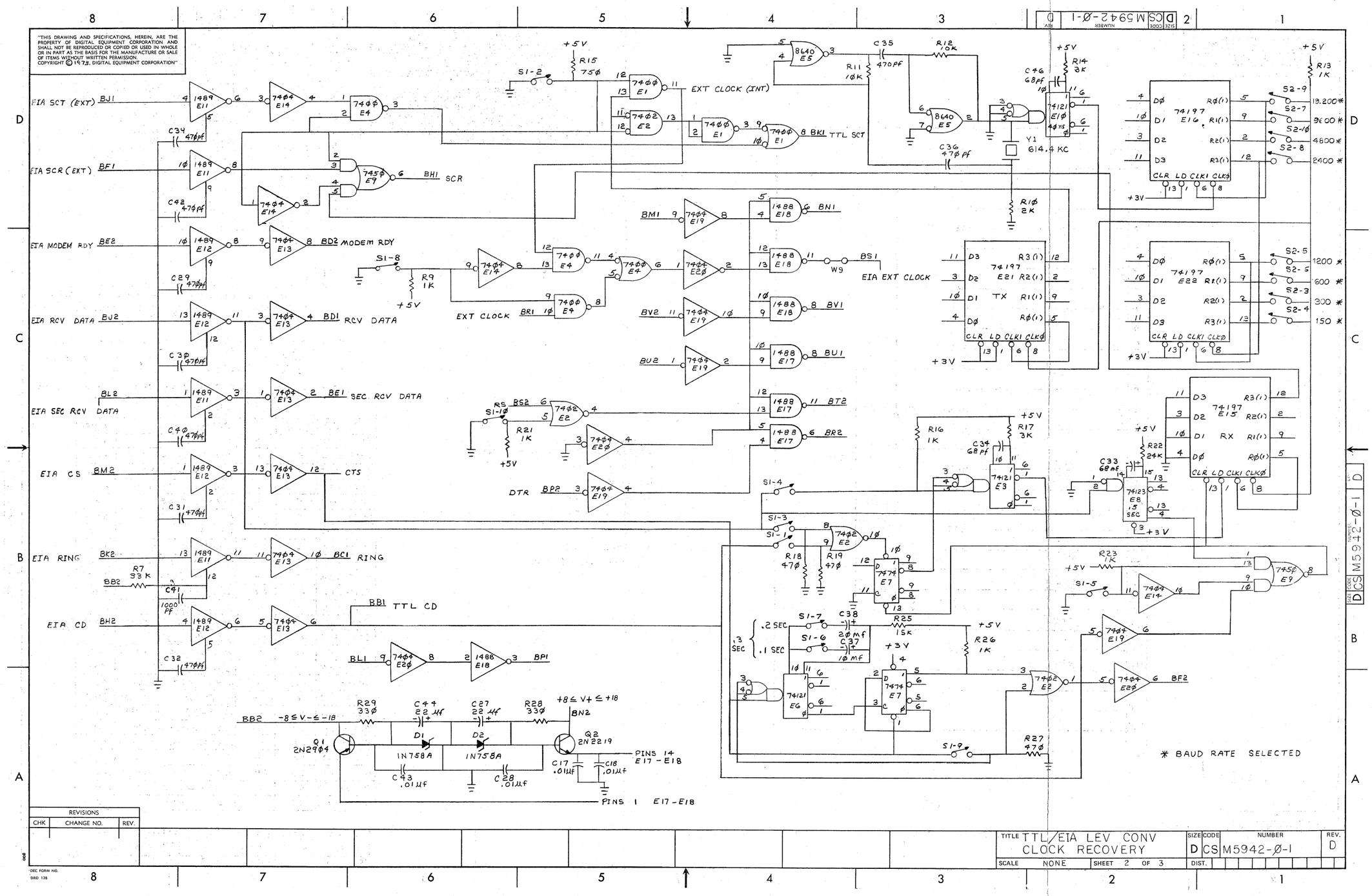
REV	CHANGE NO.	CHK	
C	ORIGINATED	M5942-00001	S. SHAMMAS 6/28/74
D	M5942-00002	W. BANAZICK	12-30-74

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

DRN. E. Wilson	DATE 1/16/74	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	
CHK'D. [illegible]	DATE 5/13/74	TITLE TTL/EIA LEV CONV CLOCK RECOVERY	
ENG. S. Shammas	DATE 5/16/74		
PROJ. ENG. S. Shammas	DATE 5/16/74		
PROD. [illegible]	DATE 5/17/74		
NEXT HIGHER ASSY: D-UA-DFC11-A-0		SIZE D CODE CS NUMBER M5942-0-1	REV. D
SCALE NONE		DIST.	
SHEET 1 OF 3			

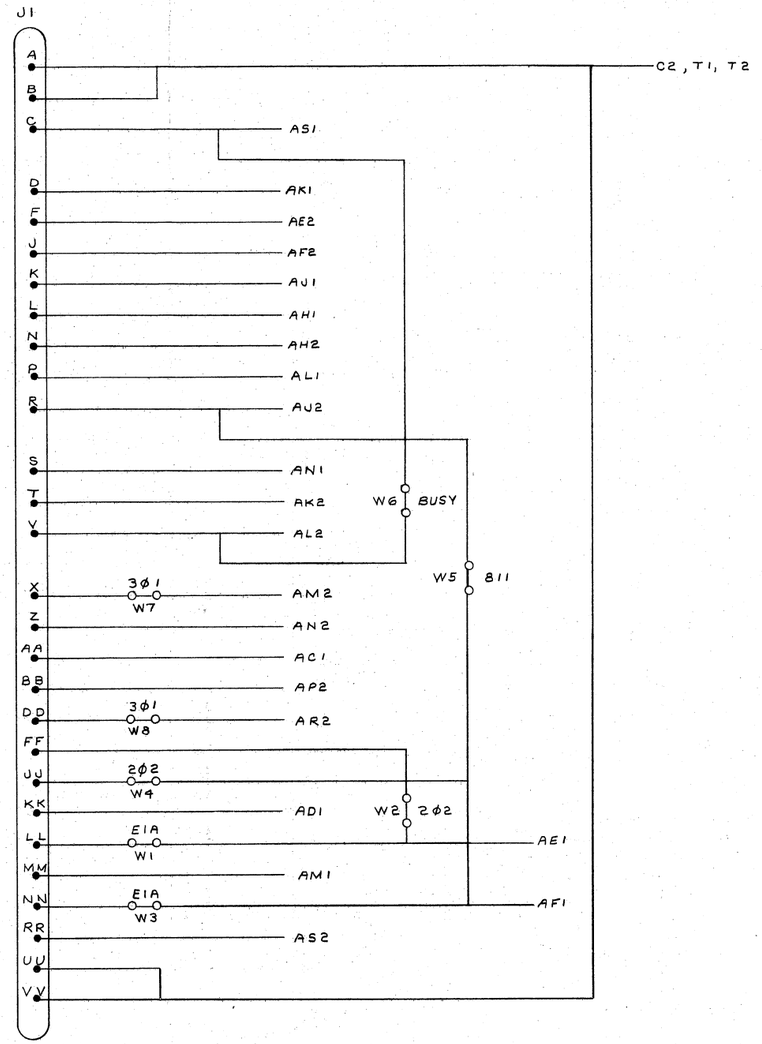
DEC CODE DCS M5942-0-1 REV D



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
TTL/EIA LEV CONV CLOCK RECOVERY	D	CS	M5942-Ø-1	D
SCALE NONE	SHEET 2 OF 3		DIST.	

DEC FORM NO. DRD 138



JUMPER FUNCTIONS

FUNCTIONS OF MODEM JUMPERS (WHEN INSTALLED)

A. EIA- SECONDARY TRANSMIT & RECEIVE DATA LINES TO EIA PINS 14 & 16.

B. 202- SECONDARY TRANSMIT & RECEIVE DATA LINES TO EIA PINS 11 & 12

C. 301- ALLOW OPERATION OF RING AND DATA TERMINAL READY FUNCTIONS WITH BELL 303 SERIES. REMOVE FOR 301

D. 811- BELL 811B RESTRAINT FUNCTION IS MONITORED BY SECONDARY RECEIVE.

E. BUSY- BELL 811B FORCE BUSY FUNCTION ANDED WITH REQUEST TO SEND.

OPTION SHIP IS AS FOLLOWS, UNLESS SPECIFIED OTHERWISE:

1. S1-1 ON
2. S1-2 ON
3. S1-4 ON
4. S1-9 ON
5. S1-10 ON
6. S2-9 ON

ALL OTHERS OFF.

SWITCH FUNCTIONS

S1-2	ON *	ENABLE DFC11-A
S1-2	OFF **	DISABLE DFC11-A
S1-1	ON	RX CLOCK TURNED ON BY CARRIER OFF-TO-ON TRANSITION.
S1-3	ON	RX CLOCK TURNED ON BY FIRST RECEIVE DATA MARK-TO-SPACE TRANSITION.
S1-4	ON	RX CLOCK RESYNCHRONIZED BY ANY MARK-TO-SPACE DATA TRANSITION.
S1-5	OFF	RX CLOCK TURNED OFF BY NO DATA TRANSITION FOR .5 SEC.
S1-5	ON	RX CLOCK TURNED OFF BY ON-TO-OFF CARRIER TRANSITION.
S1-10	OFF	REQUEST TO SEND ALWAYS ON.
S1-9	ON	CLEAR TO SEND WITH NO DELAY.
S1-9	OFF	CLEAR TO SEND WITH .1 SEC. DELAY.
S1-6	ON	
S1-9	OFF	CLEAR TO SEND WITH .2 SEC. DELAY.
S1-7	ON	
S1-9	OFF	CLEAR TO SEND WITH .3 SEC. DELAY.
S1-6	ON	
S1-7	ON	
S2-3-10		SELECT BAUD RATE.

NOTE:

* S1-2 MUST BE ON FOR OPTION TO FUNCTION AS A DFC11-A TOGETHER WITH ONE OF S2-3 THRU 10. SWITCHES ON TO SELECT THE CLOCK. ALL OTHER SWITCH SETTINGS MUST BE IN THEIR PROPER POSITIONS.

** S1-2 OFF WILL MAKE THE OPTION FUNCTION AS A DF11-A; S1-8 ON WILL MAKE M5942 SUPPLY EXTERNAL CLOCK. ALL OTHER SWITCH SETTINGS, EXCEPT S2-3 THRU 10, DO NOT APPLY.

*** CINCH CONNECTOR PINS AT END OF BLOSC CABLE

WIRE TABLE

COLOR	*** PI-PIN	J1	SIGNAL NAME	M5942
BLU-WHT	1	A	GROUND	AC2
WHT-BLU	2	F	TRANSMITTED DATA	AE2
ORN-WHT	3	J	RECEIVED DATA	AF2
WHT-ORN	4	V	REQUEST TO SEND	AL2
GRN-WHT	5	T	CLEAR TO SEND	AK2
WHT-GRN	6	Z	DATA SET READY	AN2
BRN-WHT	7	B	GROUND	AC2
WHT-BRN	8	BB	CARRIER	AP2
SLA-WHT	9	——	+ POWER (NOT USED)	
WHT-SLA	10	——	- POWER (NOT USED)	
BLU-RED	11	LL	BELL 202 SEC. TRANS. DATA	AE1
RED-BLU	12	NN	BELL 202 SEC. RECV. DATA	AF1
ORN-RED	13	D	SEC CLEAR TO SEND	AK1
SLA-RED	14	LL	EIA SECONDARY TRANS. DATA	AE1
SLA-GRN	15	N	SERIAL CLOCK TRANS.	AH2
RED-BRN	16	NN	EIA SECONDARY RECV DATA	AF1
SLA-	17	R	SERIAL CLOCK RECV	AJ2
RED-SLA	18	——	UNASSIGNED NOT USED	
BLU-BLK	19	P	SECONDARY REQUEST TO SEND	AL1
BLK-BLU	20	DD	DATA TERMINAL READY	AR2
ORN-BLK	21	MM	SIGNAL QUALITY DETECT	AM1
BLK-ORN	22	X	RING	AM2
GRN-BLK	23	RR	SIGNAL RATE SELECT	AS2
BRN-RED	24	L	EXTERNAL CLOCK	AH1
RED-ORN	25	C	FORCE BUSY	AS1

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	TTL/EIA LEV CONV CLOCK RECOVERY		
SIZE	CODE	NUMBER	REV.
D	CS	M5942-Ø-1	D
SCALE	NONE	SHEET 3 OF 3	DIST.

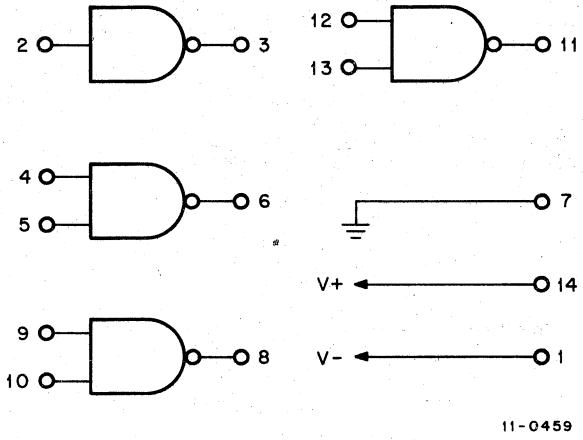
DEC-FORM NO. DRD 138

APPENDIX A
INTEGRATED CIRCUIT DESCRIPTIONS

This section provides diagrams, truth tables, pin assignments, and some descriptions of the integrated circuit units used in the DFC11-A logic. The ICs covered in this section are:

1488	Quad Line Drivers
1489	Quad Line Receivers
74121	Monostable Multivibrator
74123	Retriggerable Monostable Multivibrator with Clear
74197	50-MHz Presettable Decode and Binary Counters/Latches

MC1488L QUAD LINE DRIVER



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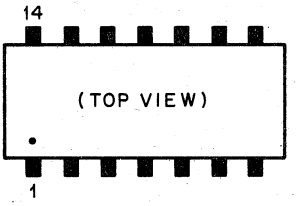

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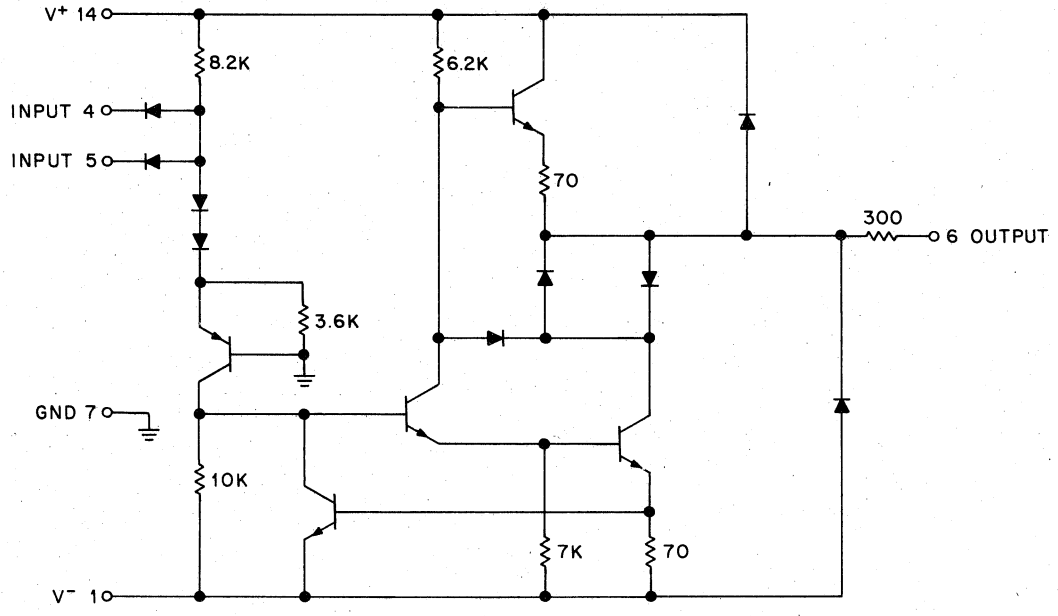
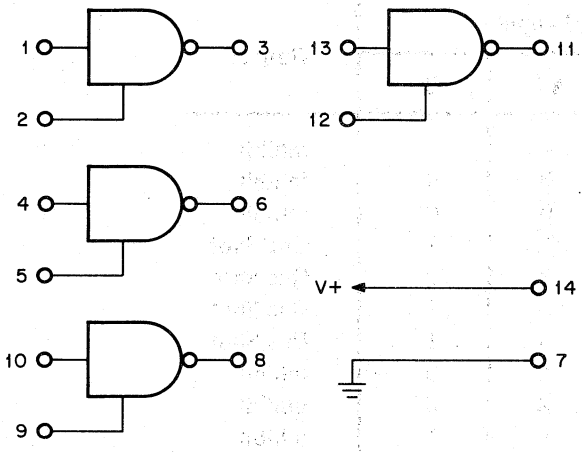


NOTE:
1/4 of circuit shown.

11-0760



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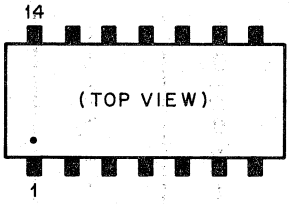

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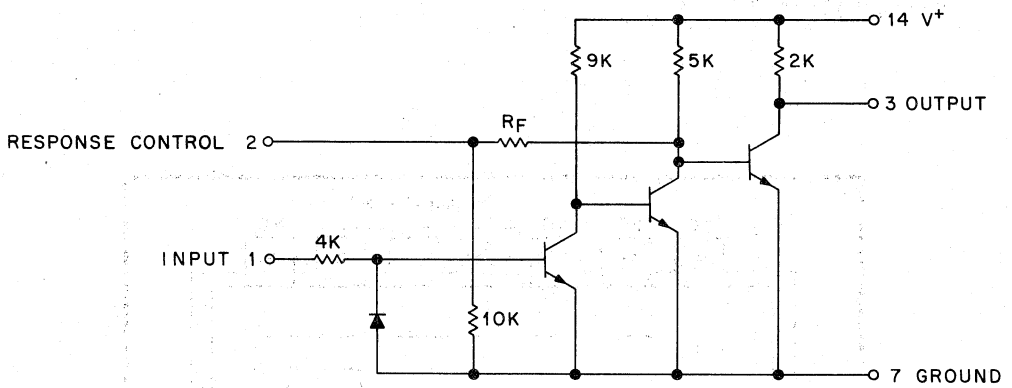


NOTE:
1/4 of circuit shown.

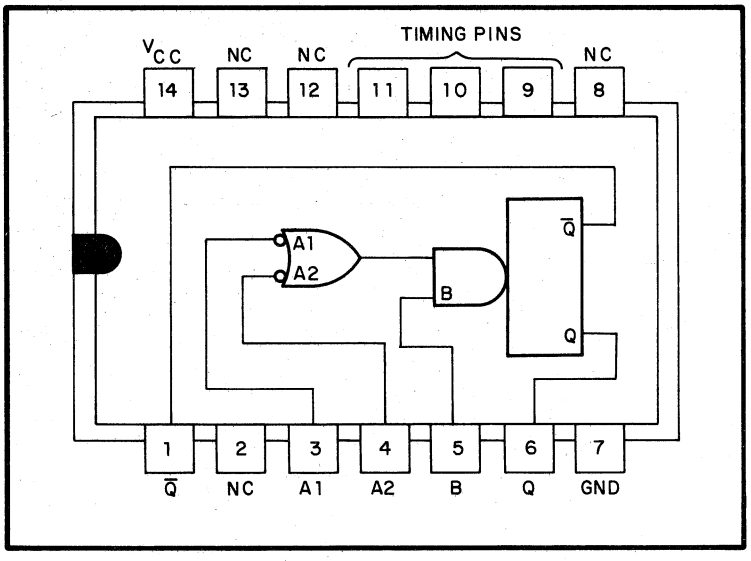
11-0761

Truth Table

t_n Input			t_n+1 Input			Output
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_{in(1)} \geq 2\ V$

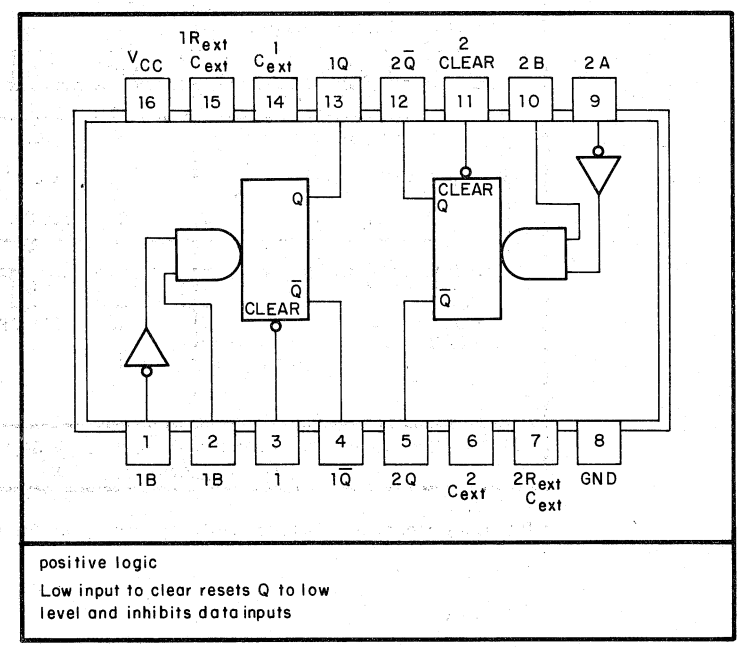
$0 = V_{in(0)} \leq 0.8\ V$



11-1863

74123 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



TRUTH TABLE

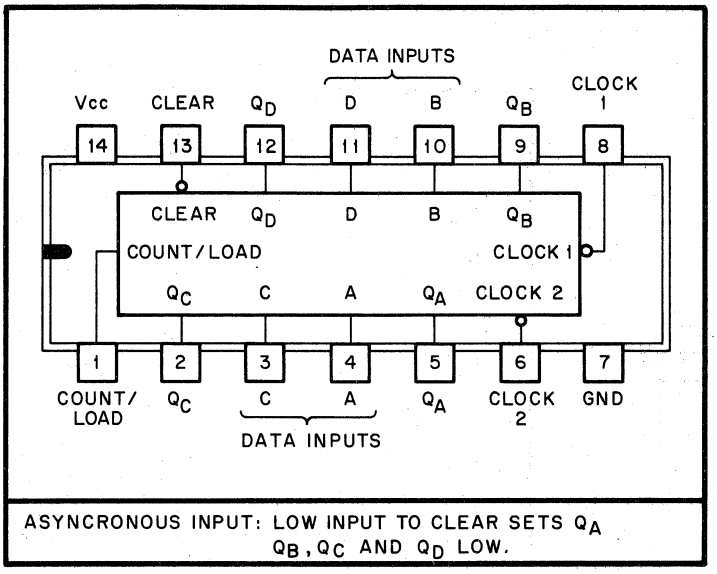
INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎍
↑	H	⎍	⎍

positive logic

Low input to clear resets Q to low level and inhibits data inputs

11-1864

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE
(TOP VIEW)*



ASYNCRONOUS INPUT: LOW INPUT TO CLEAR SETS Q_A Q_B, Q_C AND Q_D LOW.

*Pin assignments for these circuits are the same for all packages.

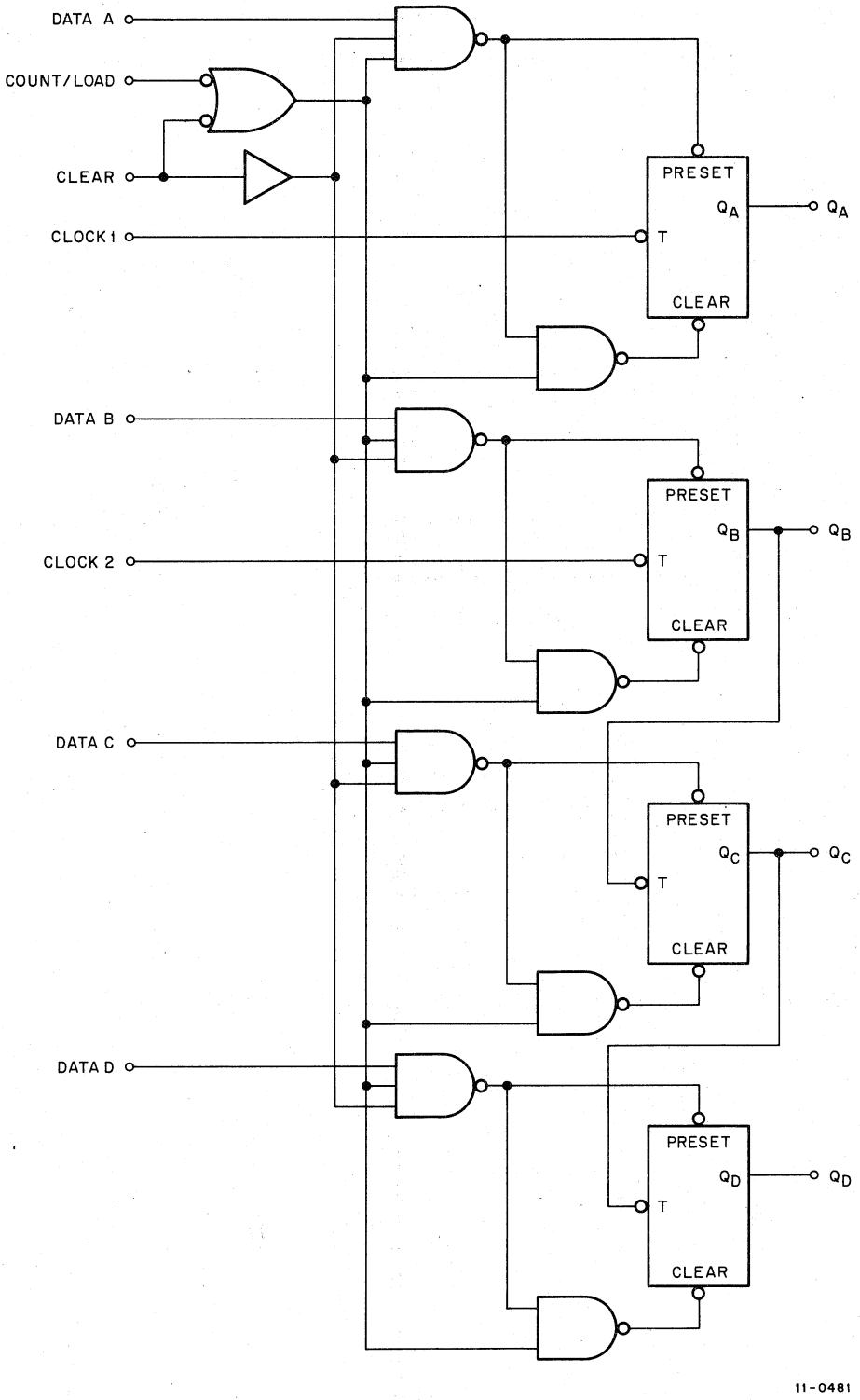
11-0482

SN74197 TRUTH TABLE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.

74197 50-MHZ PRESETTABLE DECODE AND BINARY COUNTERS/LATCHES (Cont)



DFC11-A EIA LEVEL
CONVERTER/CLOCK RECOVERY
MODULE MAINTENANCE MANUAL
EK-DFC11-MM-002

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