Digital Equipment Corporation
Maynard, Massachusetts

PDP—15 Systems

Module Manual

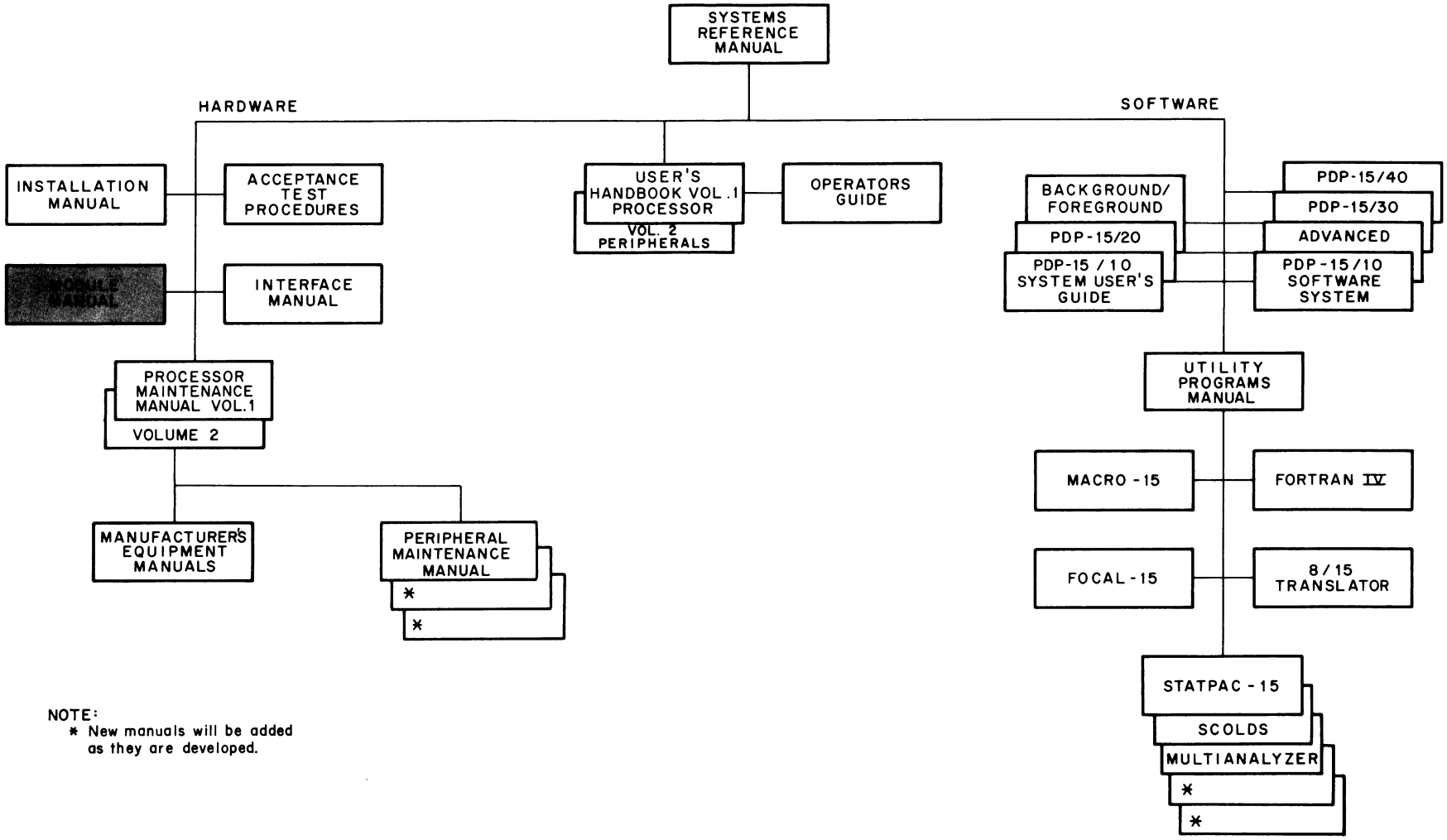
DEC-15-H2EB-D

PDP-15
MODULE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Edition July 1970
2nd Printing November 1970
3rd Printing (Rev) November 1972

PDP-15 FAMILY OF MANUALS



NOTE:
* New manuals will be added as they are developed.

15-0040

SYSTEMS REFERENCE MANUAL – Provides overview of PDP-15 hardware and software systems and options, instruction repertoire, expansion features, and descriptions of system peripherals. (DEC-15-BRZD)

USER'S HANDBOOK VOLUME 1, PROCESSOR – Principal guide to system hardware includes system and subsystem features, functional descriptions, machine-language programming considerations, instruction repertoire, and system expansion data. (DEC-15-H2DC-D)

VOLUME 2, PERIPHERALS – Features functional descriptions and programming considerations of peripheral devices. (DEC-15-H2DC-D)

OPERATOR'S GUIDE – Lists procedural data, including operator maintenance, for using the operator's console and the peripheral devices associated with PDP-15 Systems. (DEC-15-H2CB-D)

PDP-15/10 SYSTEM USER'S GUIDE – Features COMPACT and Basic I/O Monitor operating procedures. (DEC-15-GG1A-D)

PDP-15/20 SYSTEM USER'S GUIDE – Lists Advanced Monitor System operating procedures. (DEC-15-MG2B-D)

BACKGROUND/FOREGROUND MONITOR SYSTEM USER'S GUIDE – Lists operating procedures for the DECtape and disk-oriented Background/Foreground monitors. (DEC-15-MG3A-D)

PDP-15/10 SOFTWARE SYSTEM – Describes COMPACT software system and Basic I/O Monitor System. (DEC-15-GR1A-D)

PDP-15/20/30/40 ADVANCED MONITOR SOFTWARE SYSTEM – Describes Advanced Monitor System; programs include system monitor language, utility, and application types; operation, core organization, and input/output operations within the monitor environment are discussed. (DEC-15-MR2B-D)

PDP-15/30 BACKGROUND/FOREGROUND MONITOR SOFTWARE SYSTEM – Describes Background/Foreground Software System including the associated language, utility, and applications program. (DEC-15-MR3A-D)

PDP-15/40 DISK-ORIENTED BACKGROUND/FOREGROUND MONITOR SOFTWARE SYSTEM – Describes Background/Foreground Monitor in disk-oriented environment; programs include language, utility, and application types. (DEC-15-MR4A-D)

MAINTENANCE MANUAL VOLUME 1, PROCESSOR – Provides block diagram and functional theory of operation of the processor logic; lists preventive and corrective maintenance data. (DEC-15-H2BB-D)

VOLUME 2, ENGINEERING DRAWINGS –Provides engineering drawings and signal glossary for the basic processor and options. (DEC-15-H2BB-D)

INSTALLATION MANUAL – Provides power specifications, environmental considerations, cabling, and other information pertinent to installing PDP-15 Systems. (DEC-15-H2AB-D)

ACCEPTANCE TEST PROCEDURES – Lists step-by-step procedures designed to insure optimum PDP-15 Systems operation.

PDP-15 MODULE MANUAL – Provides characteristics, specifications, timing and functional descriptions of modules used in PDP-15 Systems. (DEC-15-H2EB-D)

INTERFACE MANUAL – Provides information for interfacing devices to a PDP-15 System. (DEC-15-H0AC-D)

UTILITY PROGRAMS MANUAL – Provides utility programs common to PDP-15 Monitor Systems. (DEC-15-YWZA-D)

MACRO-15 – Provides MACRO assembly language for the PDP-15. (DEC-15-AMZA-D)

FORTRAN IV – Describes PDP-15 version of the FORTRAN IV compiler language. (DEC-15-KFZB-D)

FOCAL-15 – Describes an algebraic interactive compiler level language developed by Digital Equipment Corporation. (DEC-15-KJZB-D)

List of Modules

A124	Analog Multiplexer
A222	Selectable Gain Amplifier
A405	Sample and Hold Amplifier
A607	10-Bit D/A Converter, Single Buffered
A708	Dual Voltage Regulator
A877	Analog-to-Digital Converter
G085	Disk Read Amplifier
G100	Sense Amplifier and Inhibit Driver
G222	Memory Selector
G223	Read/Write Driver
G285	Series Switch
G286	Center Tap Selector
G290	Writer Flip-Flop
G613	X Diode Matrix
G614	Y Diode Matrix
G681	Track Matrix
G711	Terminator Board
G775	Indicator Panel
G821	+5V Regulator
G822	-6V Regulator
G823	-24V Regulator
G825	-24V Pass Element
G827	Power Sequence Detector and Delays
G829	Power Connector
G858	Teletype® Connector
K303	Timer
M002	Logic 1 Source
M101	Bus Data Interface
M103	Device Selector
M104	I/O Bus Multiplexer
M111	Inverters
M112	NOR Gates
M113	NAND Gates
M115	NAND Gates
M117	NAND Gates
M119	NAND Gates
M121	AND/NOR Gates
M127	AND/NOR Gates
M129	AND/NOR Gates
M133	NAND Gates
M135	NAND Gates
M139	NAND Gates
M149	NAND-Wired OR Matrix
M159	4-Bit Arithmetic Logic Unit
M161	Binary-to-Octal/Decimal Decoder
M162	Parity Circuit
M164	6-Bit Parallel Adder
M182	Parity Circuit
M191	Carry Look-Ahead Generator

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List of Modules (Cont)

M205	D Flip-Flops
M206	D Flip-Flops
M207	Flip-Flop
M211	Binary Up/Down Counter
M212	6-Bit Left/Right Shift Register
M214	Data Storage Register (6-Bit)
M216	D Flip-Flops
M218	MQ Register (9-Bit)
M219	Step Counter and Control
M223	MA and MB Register (4-Bit)
M226	Register (7-Bit)
M227	AC Shifter (9-Bit)
M238	Synchronous Up/Down Counter
M240	R-S Flip-Flops
M242	J-K Flip-Flops
M248	Right Shift Parallel Load Register
M302	Dual Delay Multivibrator
M311	Tapped Delay Lines
M312	Delay Lines
M401	Variable Clock
M402	Photo Mod Clock
M420	Phase-Lock Clock
M452	Variable Clock
M500	Converter-I/O Bus Receiver
M510	I/O Bus Receiver
M515	Real Time Clock
M602	Pulse Amplifiers
M606	Pulse Generators
M611	High-Speed Power Inverters
M617	Power NAND Gates
M621	Data Bus Drivers
M622	I/O Bus Drivers
M627	NAND Power Amplifiers
M628	Block-Bank Address Card
M632	Converter-I/O Bus Driver
M706	Teletype Receiver
M707	Teletype Transmitter
M717	Display Control VP15
M770	EAE Control
M771	Internal IOT Decoder
M772	Console Control No. 1
M773	Console Control No. 2
M775	Time State Generator
M776	Reader Register
M901	Flexprint® Cable Connector
M902	Terminator Card
M904	Coaxial Cable Connector
M909	Terminator Card
M910	CP Terminator Card

List of Modules (Cont)

M911	Memory Bus CP Terminator Card
M912	I/O Bus Connector
M915	Console Cable Connector
M1701	Data Selector
M1713	16-to-1 Data Selector
W010	Clamped Loads
W028	Cable Connector for Levels and Pulses
W076	Teletype Connector
W714	Switches
W850	I/O Connector

General Description

This manual provides descriptions of modules used in the PDP-15 System and its associated peripherals. A schematic diagram is included with each module description. Parts location diagrams are supplied for those modules that have numerous discrete components.

DEC builds three series of compatible below-ground logic (the B-, R- and S-series), two series of compatible above-ground logic (K- and M-series), an extensive line of modules to interface different types of logic (W-series), a line of special-purpose modules (G-series), and a line of support hardware for its module line (H-series).

With few exceptions, the DEC below-ground logic operates with logic levels of ground to -0.3V (upper level) and -3.2V to -3.9V (lower level), using diode gates that draw input current at ground and supply output current at ground. Figure 1 shows the voltage spectrum of negative logic systems.

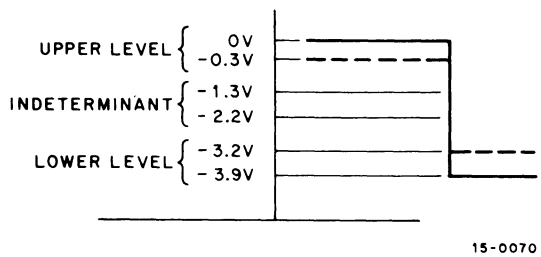


Figure 1 Voltage Spectrum of Negative Logic Systems

The compatible above-ground logic generally operates with levels of ground to +0.4V (lower level) and +2.4 to +3.6V (upper level), using TTL or TTL-compatible circuits with inputs that supply current at ground and outputs that sink current at ground. Figure 2 shows the TTL logic voltage spectrum.

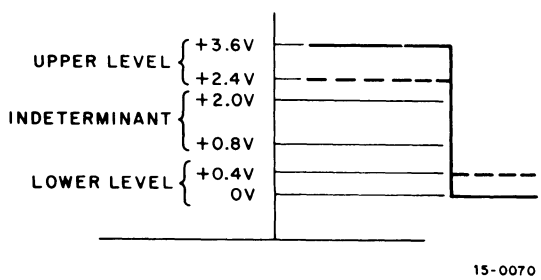


Figure 2 Voltage Spectrum of TTL Logic

A set of special modules designed to operate on the PDP-15 I/O bus is also available. Figure 3 indicates the voltage spectrum in which these special modules operate.

The use of DEC's **Digital Logic Handbook** is recommended for readers of this manual who are not familiar with the basic principles of digital logic and the type of circuits used in DEC logic modules.

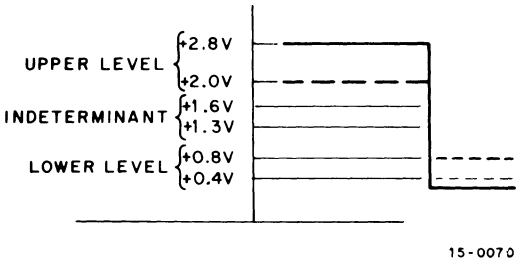


Figure 3 Voltage Spectrum for Positive PDP-15 I/O Bus Logic

MEASUREMENT DEFINITIONS

Timing is measured with the input driven by a gate or pulse amplifier of the series under test and with the output loaded with gates of the same series (unless otherwise specified). Percentages are assigned with 0 percent indicating the initial steady-state level and 100 percent indicating the final steady-state level, regardless of the direction of change.

Input/output delay is the time difference between input change and output change, measured from 50 percent input change to 50 percent output change. Rise and fall delays for the same module are usually specified separately.

Risetime and falltime are measured from 10 percent to 90 percent of waveform change, either rising or falling.

LOADING

Input loading and output driving are specified in "units", with one unit equivalent to 1.6 mA. The inputs to low-speed gates usually draw 1 unit of load. High-speed gates draw 1.25 units, or 2 mA.

PARTS LOCATION

A parts location diagram is provided for those modules that contain numerous discrete components and integrated circuits. The location of parts on integrated circuit modules can be determined by visual inspection and circuit schematic reference.

"E" designators are assigned to integrated circuits according to the following convention: looking at the component side of the module, "E" numbers are assigned from right-to-left within each horizontal row, starting with the top row. Figure 4 illustrates this convention and typical symbols used in the parts location diagrams.

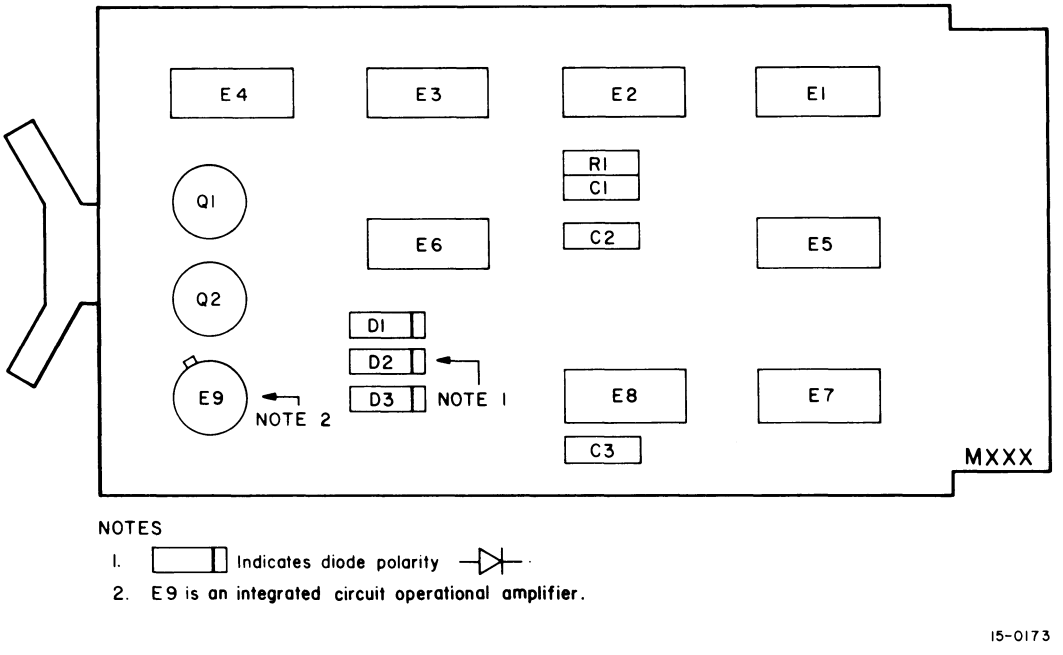


Figure 4 Sample Parts Location Diagram

A124
Analog Multiplexer

The A124 Analog Multiplexer consists of four MOSFET switches and four driver gates used for selection of single-ended analog inputs in the range of ±10V. This module is also used for gain selection with the A222 Selectable Gain Amplifier in the AD15 Analog Subsystem.

Isolated grounds are used in the module to help prevent program noise from causing analog signal acquisition errors. Analog and logic grounds may differ by as much as 9V without malfunction.

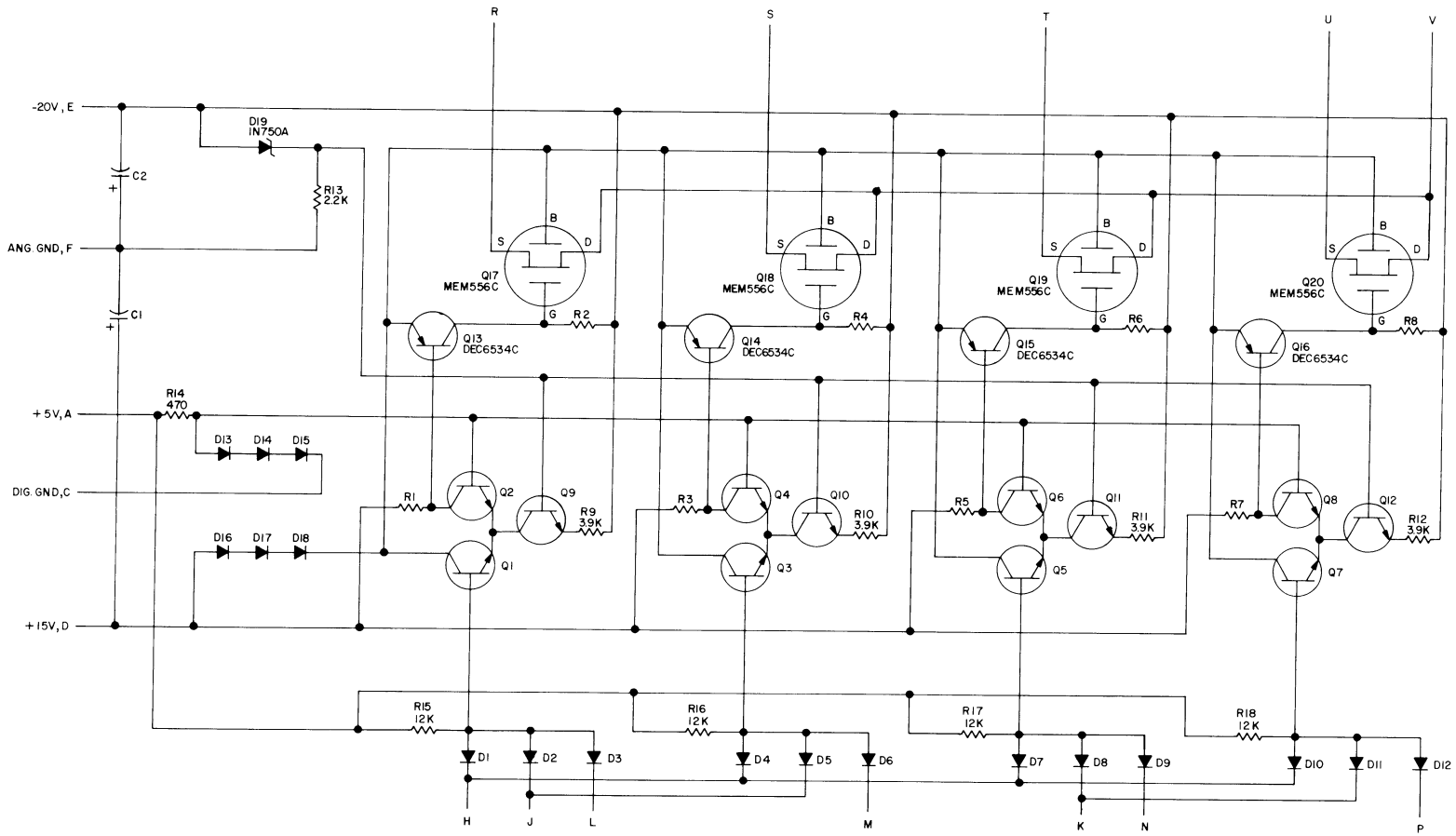
Each drive consists of 2-bit input decoding and a common enable input. All inputs are de-activated when power is removed.

INPUTS: Digital: Pin H (enable) presents 1 unit load; pins J, K, L, M, N and P present 1/2-unit load each.

Analog: Pins R, S, T, and U – ±10V normal, ±20V maximum.

OUTPUTS: Analog: Pin V series resistance < 2200 ohms, 3 mA max. load.
Response time to logic input change < 1.2 μsec.

POWER: +15V at pin D, 25 mA
-20V at pin E, 30 mA
+5V at pin A, 8 mA



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 8.2K, 1/4W, 5%
CAPACITORS ARE 1MFD, 35V, 10%
DIODES ARE D664
TRANSISTORS ARE 2N3568B

A124-2

REVISIONS			
CHK	CHG NO	REV	
[illegible]	10001	A	

DRN	E. Talley	DATE 12-16-69
CHK'D	[illegible]	DATE 12-17-69
ENG	[illegible]	DATE 2-25-70
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606		
IN750A	SAME		
2N3568	2N3568		
MEM556C	SAME		
DEC6534C	NONE		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE FOUR INPUT MULTIPLEXER SWITCH A124

SIZE	CODE	NUMBER	REV.
C	CS	A124-0-1	A

PRINTED CIRCUIT REV. A B

SIZE C | CODE CS | NUMBER A124-0-1 | REV. A

DEC FORM NO. DRC 102

A124-0-1

5

DIST: 324, 434, 433 PMR

A222
Selectable Gain Amplifier

The A222 is a non-inverting operational amplifier with high input impedance. A precision voltage divider is connected between output and ground with taps at ratios of 1.0, 0.5, 0.25, and 0.125. This module is used with an A124 Analog Multiplexer in the AD15 Analog Subsystem to provide computer-controlled gain selection in the AD15. An IOT instruction causes two AC bits to be transferred to an AD15 buffer register. These bits are decoded by the A124 to select one of four available gains: 1, 2, 4, or 8.

INPUTS: Inverting input (pin S) – Connect to the desired feedback tap through a series resistance of 3000 ohms or less (A124 Analog Multiplexer).

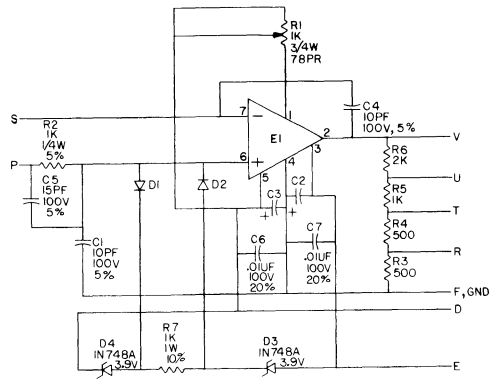
Non-inverting input (pin P) – Gain of 1, 2, 4, or 8 ±.02% with .02% linearity error over a ±10V output range. Input impedance greater than 1000 megohms in parallel with 10 pF. Protected against overload up to ±20V.

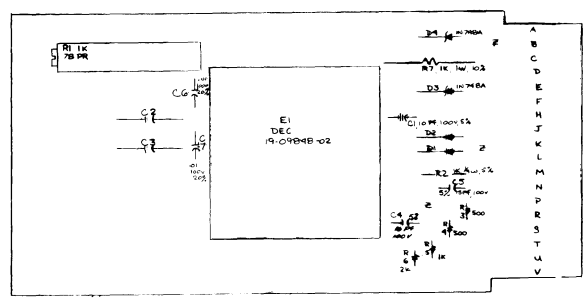
OUTPUTS:

Analog Input Range	Selected Gain	Output Selected
±1.25V	8	Pin V
±2.5V	4	Pin U
±5.0V	2	Pin T
±10.0V	1	Pin R

POWER: +15V, ±1%, 20 mA, max. (Pin D)
-15V, ±1%, 20 mA, max. (Pin E)

A222-2





UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 1UF, 35V, 10%
DIODES ARE D664
RESISTORS ARE .3W, .01% MF
E1 IS DEC 1909848-02
USE ETCH OF A220

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1		HANDLE, FLIPCHIP, AMBER	9008337-0	20
2		EYELET HANDLE	9006732	19
4		EYELET FEED THRU	9006751	18
1	E1	AMPLIFIER 3278-1/4 OR AMP	1909848-02	17
2	R3, R4	RES. 500, .3W, .01% MF	1309985-0	16
1	R1	RES. 1K, 3/4W, 78 PR	1309862	15
1	R6	RES. 2K, .3W, .01% MF	1305510	14
1	R5	RES. 1K, .3W, .01% MF	1305509	13
1	R7	RES. 1K, 1W, 10%	1101499	12
1	R2	RES. 1K, 1W, 5%	1360365	11
2	D3, D4	DIODE, IN 748A 3.9V	1100122	10
2	D1, D2	DIODE, D664	1100114	9
2	C2, C3	CAP. 1UF, 35V, 10% TANT	1001776	8
2	C6, C7	CAP. 01UF, 100V, 20% DISC	1001610	7
1	C5	CAP. 15PF, 100V, 5%, DM	1000007	6
2	C1, C4	CAP. 10PF, 100V, 5%, DM	1000006	5
1		ETCHED CIRCUIT BOARD (A220)	5008806	4
		MODULE ECO HISTORY	B-MI-A222-0-6	3
		ASSY/DRILLING HOLE LAYOUT	C-AH-A222-0-5	2
		X-Y COORDINATE HOLE LOCATION	K-CO-A222-0-4	1
QTY	REF. DESIGNATION	DESCRIPTION	DEC. PART NO.	ITEM NO.

PARTS LIST

ETCH BOARD REV B

REV	CHANGE NO.	CHK
A	0000	

REVISIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.
D664	IN 3606		
IN 748A	SAME		

SEMICONDUCTOR CONVERSION CHART

DRN. Roger J Doucette DATE 11-6-71
CHK'D. Nancy Moore DATE 11-11-71
ENG. [illegible] DATE 12-27-71
PROJ ENG. [illegible] DATE 12-27-71
PROD. DATE
NEXT HIGHER ASSY
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE
SELECTABLE GAIN BUFFER AMPLIFIER

SIZE	CODE	NUMBER	REV.
D	CS	A222-0-1	A

DIST.

DEC FORM NO. DRD-135

A405
Sample and Hold Amplifier

The A405 Sample and Hold Amplifier is used in the AD15 Analog Subsystem to sample the rapidly varying analog input (25 kHz, minimum) and store the signal level at a particular time to allow an A/D converter to convert the signal to a digital word. The amplifier provides acquisition of a 10V step input to within 1 mV in less than 2 μs.

Two digital Track Control inputs are provided to control the sample/hold function: pin BF for positive logic and pin BH for negative logic. In positive logic applications, the amplifier will sample (track) when the level at pin BF is high and hold when the level at pin BF is low. For pulsed RS flip-flop control, jumper W1 is removed and jumper W2 is connected. Then, a positive pulse at pin BF sets the flip-flop for tracking and a positive pulse at pin BH resets the flip-flop to hold the signal.

A voltage offset circuit is provided at the input to allow the output signal to be shifted more positive. To use this offset, pin AU is jumpered to pin BJ and pin BM is jumpered to pin AE. (-15V). This circuit is not used on the AD15 Analog Subsystem application.

INPUTS: Analog input: ±10V range, 2000 ± 1% ohms

Digital inputs: Positive logic Track Control at pin BF presents 1 unit load.

Pulse input to set hold at pin BH presents 1 unit load.

OUTPUTS: Analog output: ±10V at 10 mA, 0.1 ohm maximum output impedance at pin AV.

POWER: +15V at 35 mA at pin AD
-15V at 40 mA at pin AE (plus additional 11 mA if offset circuit is connected)
+5V at 15 mA at pin AA

A607
10—Bit D/A Converter, Single Buffered

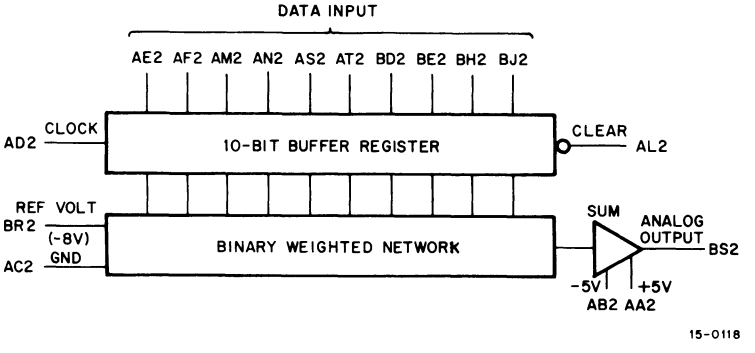
The A607 module contains a 10-bit D/A converter that consists of a 10-bit buffer register, a binary weighting network, and a current summing amplifier. The reference voltage used in the binary weighting network is externally supplied for greater efficiency and optimum scale factor matching in multi-channel applications. Data on register input lines must be settled 20 ns before the leading edge (positive-going voltage of the CLOCK pulse passes the threshold voltage and should remain stable 5 ms afterward. The duration of the positive CLOCK pulse should be at least 50 ns, and the duration of the negative CLEAR pulse should be at least 30 ns. Data present at the input of the register is transferred to the output when the leading edge of the CLOCK pulse passes the threshold. The analog output voltage is unipolar and varies from 0V to 2.0V (in two millivolt increments) in accordance with the binary input data.

The following are the input, output, and power characteristics of the A607 module.

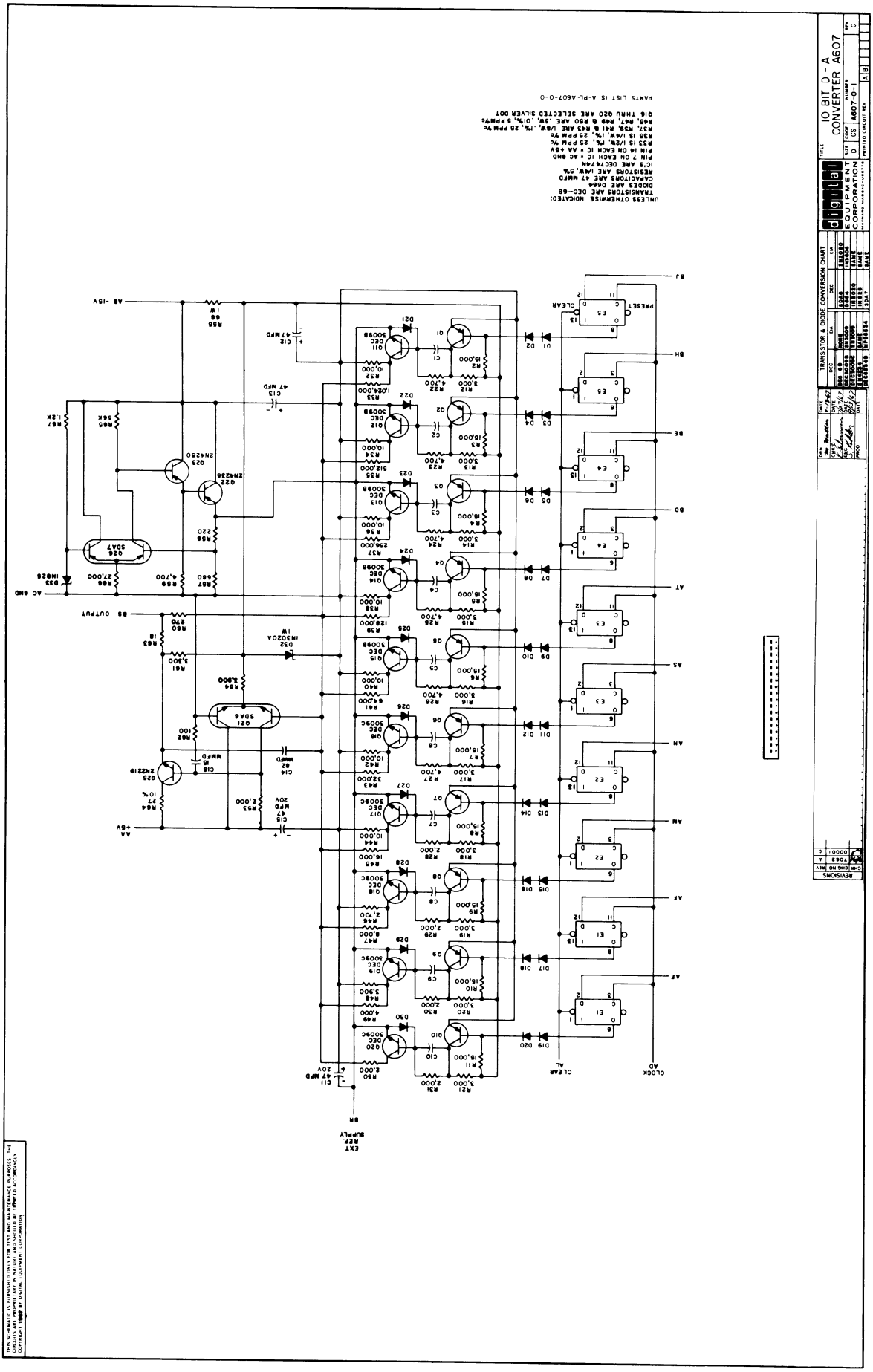
INPUTS: Each DATA input presents one TTL unit load. The CLOCK input presents 2 unit loads, and the CLEAR input presents 3 unit loads.

OUTPUTS: The analog output voltage is capable of driving a 10 mA load (maximum).

POWER: Power dissipation of the A607 is 5V at 200 mA (maximum) and -15V at 100 mA (maximum).



A607 Simplified Diagram


10 BIT D - A
CONVERTER A607
digital
EQUIPMENT
CORPORATION
A607-0-1
TRANSISTOR & DIODE CONVERSION CHART
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC-68
DIODES ARE D664
RESISTORS ARE 1/4W 5%
CAPACITORS ARE 47 MMFD
IC'S ARE DEC74AN
PIN 7 ON EACH IC = AC GND
PIN 14 ON EACH IC = AA +5V
R35 IS 1/4W, 1%, 25 PPM/°C
R53 IS 1/2W, 1%, 25 PPM/°C
R37, R38, R61 & R63 ARE 1/8W, 1%, 25 PPM/°C
R40, R47, R48 & R50 ARE .3W, .01%, 5 PPM/°C
Q16 THRU Q20 ARE SELECTED SILVER DOT
PARTS LIST IS A-PL-A607-0-0
CLOCK
CLEAR
PRESET
EXT REF SUPPLY
AA +5V
AB -15V
AC GND
BS OUTPUT
THIS SCHEMATIC IS PROVIDED ONLY FOR USE AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
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A607
15-0156
E1
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Q13
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Q11
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D28
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D26
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D24
D23
D22
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R49
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R45
R43
R41
R39
R37
R35
R33
C14
R64
R62
R63
R61
R54
R48
R46
R44
R42
R40
R38
R36
R34
R32
C15
C16
R53
Q21
Q25

A708
Dual Voltage Regulator

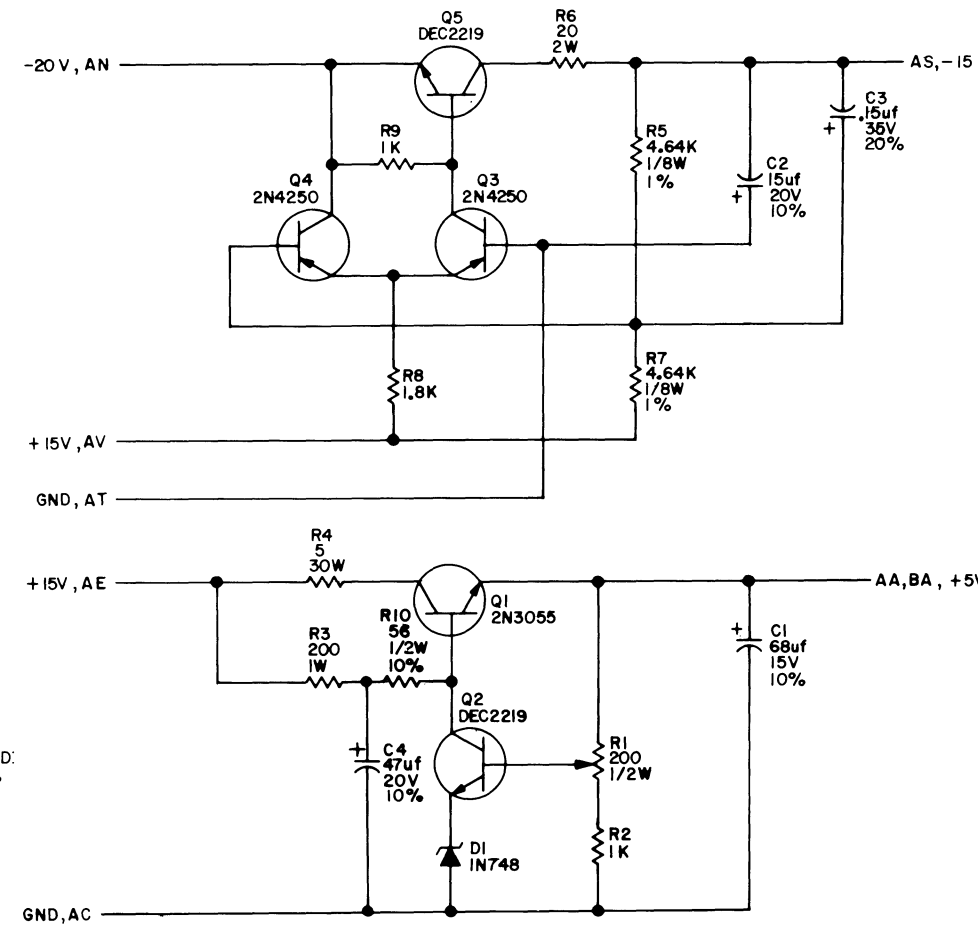
The A708 Dual Voltage Regulator is used in the AD15 Analog Subsystem to provide regulated -15V and +5V output voltages.

In the -15V regulator circuit, Q3 and Q4 control the forward bias on series regulator Q5 to maintain the -15V output within ±1%. In the +5V regulator, any change in the +5V output is sensed at the base of Q2, which controls forward bias on Q1 to maintain the +5V output with ±5%.

INPUTS: Less than 20 mV ripple.
-20V, ±1%, 0.25A max. Pin N2
+15V, ±1%, 1.25A max. Pin E2, V2

OUTPUTS: -15V, ±0.5%, 0.2A max. Pin S2
+5V, ±1%, 1.2A max. Pin A2

SIZE	CODE	NUMBER	REV
B	CS	A708-0-1	F



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%

REVISIONS				
CHK	CHG NO.	REV.		
DW	00001	A	P. SEVERINO	
EJ	00002	B	E.J. Nale 4-21-72	
JM	00003	C	P. SEVERINO	
EJ	00004	D	E.J. Nale 4-21-72	
	00004	E	E.J. Nale 6-14-72	
	00004	F	E.J. Nale 9-17-72	
			P. SEVERINO	

DRN.	ALLAN RITCEY	DATE 2-12-70
CHK		DATE 2-19-70
ENG.		DATE 3-11-70
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
1N748	1N748		
DEC2219	2N2219		
2N4250	SAME		
2N3055	SAME		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE DUAL VOLTAGE REGULATOR A708

SIZE	CODE	NUMBER	REV.
B	CS	A708-0-1	F

PRINTED CIRCUIT REV. D

DEC FORM NO.
DRB 102

4

DIST. 324,434,435 2

Pink

A877
Analog-to-Digital Converter

The A877 Analog-to-Digital Converter is used in the AD15 Analog Subsystem to convert the A405 Sample and Hold Amplifier output to a 13-bit digital word (12 bits plus a sign bit). A comparator amplifier compares the analog input voltage with a programmed sequence of internally-generated reference voltages to determine the polarity and amplitude of the input signal. The result is stored in a 13-bit data register. An A/D DONE signal is provided when the conversion is complete.

MAINTENANCE NOTE

The A877 uses special matched components to achieve specified measurement accuracy. If a fault is isolated to the A877, do not attempt to replace components in the field. Substitute a spare module and return the faulty module to DEC for service.

ANALOG INPUT SIGNAL:	Full scale range: ±10V Connections: Single-ended Impedance: 28K ohms Overvoltage limit: ±15V, maximum Settling time: 1 μs
ENCODING PROCESS:	Digitalizing resolution: 1 part in 8,190 (2.5 mV) Encoding word time: 36 μs, typical Encoding word rate: 28,000s, typical Code: Parallel, binary 2's complement
MEASUREMENT ACCURACY:	Full range: 0.015% Temperature coefficient: ±0.0020%/°C (over full operating temperature range)
CONTROL SIGNALS:	Input: Command to Convert (CTC) initiates encoding process on a logic 1-to-0 transition Output: End of Conversion (EOC) pulse is 100 ns logic 1 pulse
DATA OUTPUTS:	13 bits, held in storage until next CTC input.
POWER REQUIREMENTS:	+15V, ±5%, 100 mA, typical, pin AD -15V, ±5%, 50 mA, typical, pin AE +5V, ±10%, 400 mA, typical, pin BA

CONNECTOR PIN ASSIGNMENTS

Pin	Function	Pin	Function
AD1/2	+15V	BL2	Data Bit 4
AE1/2	-15V	BM2	Data Bit 5
AF1/2	±15V Common	BN2	Data Bit 6
AJ2	Analog Input	BP2	Data Bit 7
AK2	Analog Return	BR2	Data Bit 8
AU1	Command to Convert (CTC)	BS2	Data Bit 9
BA2	+5V	BT2	Data Bit 10
BC2	Logic Ground	BU2	Data Bit 11
BE2	Sign Bit, Complemented	BV2	Data Bit 12
BF2	Sign Bit	BJ1	Data Bit 13 (LSB)
BJ2	Data Bit 2	BF1	End of Conversion (EOC)
BK2	Data Bit 3		

ADJUSTMENT AND CALIBRATION

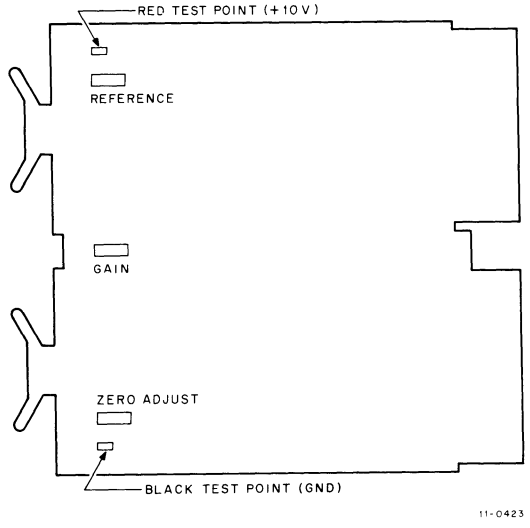
NOTE

Do not attempt to adjust any potentiometers other than the reference, gain, and zero adjust potentiometers at the rear of the module (see illustration).

Adjust the A877 while it is installed in slot C11 of the AD15. Remove the A405 module and allow 15 minutes warmup.

Reference Voltage Adjustment

Use Fluke 585A voltmeter (or equivalent voltmeter with 0.005% accuracy) to measure voltage between +10V test point (red) and ground (black). Adjust reference potentiometer (top) to obtain 10.000V, ±1 mV.



Gain Adjustment

Connect EDC voltage standard (or equivalent voltage standard with 0.005% accuracy) between pins C11J2 and C11F2 (See drawing D-AD-7007029-0-0 in AD15 manual).

Run MAINDEC-15-D6GA-D(D), with any channel and gain setting. Adjust the EDC to find the most positive switching point (007776-007777). Record the voltage. Reverse the polarity of the EDC connections to find the most negative switching point. Record the voltage. The difference between the voltages should be 19.9995V, ±2 mV. Adjust the gain potentiometer and repeat these measurements until the difference is within the specified tolerance.

Zero Adjust

Short-circuit pins C11J2 and C11F2 and note the conversion value. If the reading is outside the range 77776-000002, adjust the zero adjust potentiometer (bottom) to bring it within range. This adjustment interacts with the gain adjustment and several passes may be required to bring both adjustments within their specified tolerances.

G085
Disk Read Amplifier

The G085 Disk Read Amplifier is a double-height module consisting of an ac-coupled amplifier with a bandwidth (-3 dB) from 20 kHz to approximately 1 MHz, followed by a slicer. The G085 module is used to detect and amplify timing tracks and data signals for the RS09 DECdisk. The maximum voltage gain (under potentiometer control) is approximately 60 dB (1000). Common mode rejection ratio is approximately 40 dB. The amplifier is insensitive to any power supply ripple voltage less than 5 percent. Pin AM increases the gain by approximately 20 percent when its input is low. The nonrectified slice output is gateable, and the slice point can be varied by logic inputs. A potentiometer is provided to adjust the slice. Pins at AT and AV are provided as amplifier test points. Proper grounding is critical in this module. G085 ground pins should not be bussed. Pins AS and AC should be connected to analog ground, and BF and BC should be connected to logical ground. All amplifier connections must be isolated from fast rise-time signals.

INPUTS: Voltage levels are 0 and -3V, except at the input to pins AE and AF.

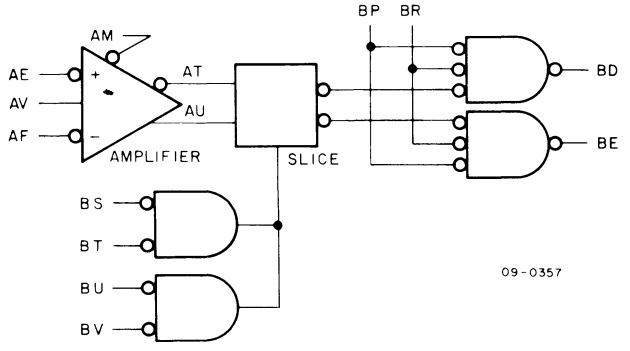
Pin	Function	Load or Input Voltage
AE,AF	Read Head Input	approx. 15 mV peak-to-peak
AM	Read Gain Control	2 mA
BU,BV	Read Slice Control	2 mA
BS,BT	Read Slice Control	2 mA
BP,BR	Enable Output	2 mA

OUTPUTS: Voltage levels are 0 and -3V except at AV, which provides +20V for the timing track center taps.

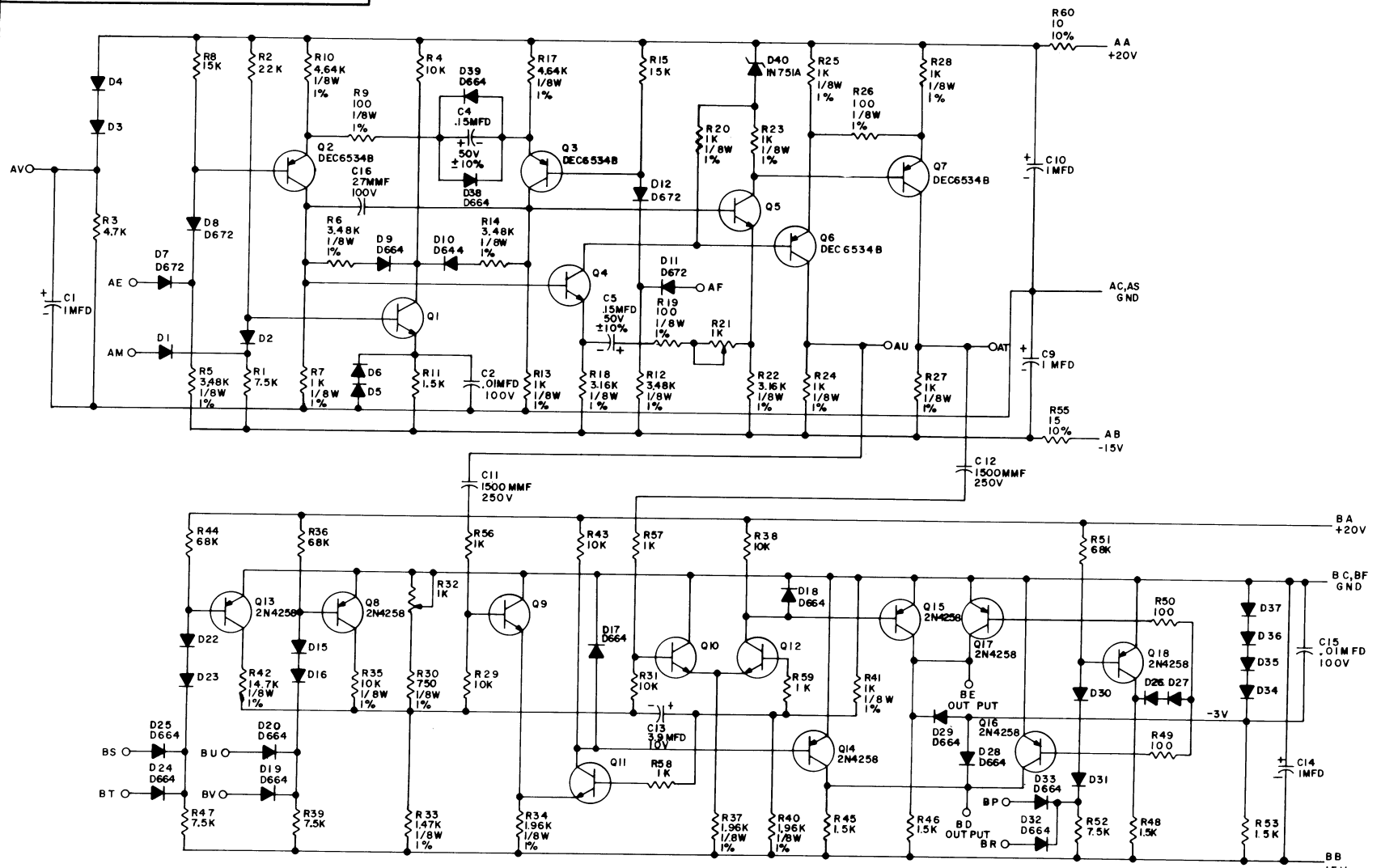
Pin	Function	Drive
BE,BD	Signal Output	10 mA

INPUT/OUTPUT DELAY: 120 ns

POWER DISSIPATION: 2W at +20V
1.5W at -15V



G085 Disk Read Amplifier and Slice, Block Schematic



UNLESS OTHERWISE INDICATED
CAPACITORS ARE 35V
RESISTORS ARE 1/4W, 5%
DIODES ARE D662
TRANSISTORS ARE DEC3009B
R21, R32 ARE POTS 76 PR 1K HELITRIM
1/8W, 1% RESISTORS ARE 100MF

G085-2

REVISIONS	CHK	CHG NO.	REV.
MM		00001	A
REV. & REDR.		00002	D
		00003	
		00004	E
		00005	F

DRN. M. HALLER	DATE	10-23-68
CHK'D MULLEN	DATE	10-24-68
ENG. S. SAMBERT	DATE	1-10-69
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606	DEC6534B	MPS6534B
D662	IN645	IN751A	SAME
D672	IN3653		
2N4258	NONE		
DEC3009B	*2N3009B		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DISC READ AMP AND SLICE G085

SIZE	CODE	NUMBER	REV.
C	CS	G085-0-1	F

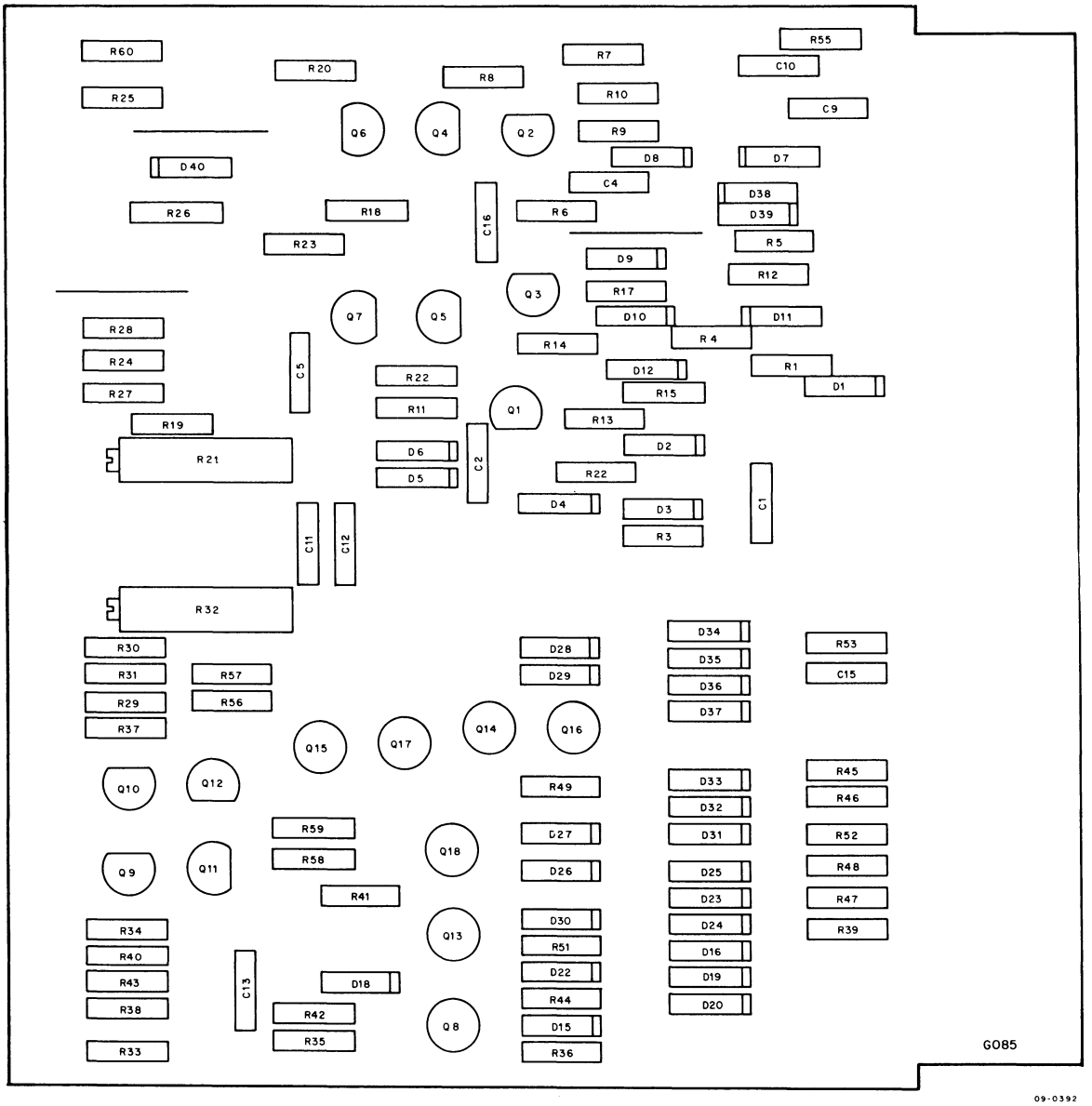
PRINTED CIRCUIT REV. E

DEC FORM NO. DRC 102

PINK

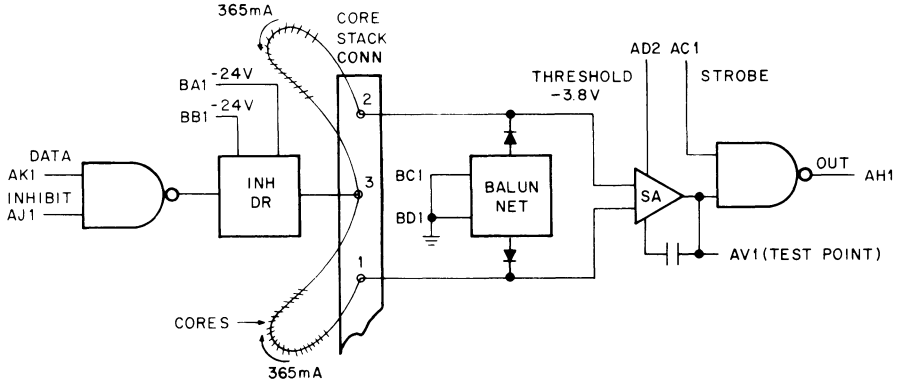
DIST. 324, 434, 435

SIZE	CODE	NUMBER	REV.
C	CS	G085-0-1	F


R60
R25
R20
R8
R7
R55
C10
C9
R10
R9
Q6
Q4
Q2
D40
D8
D7
C4
D38
D39
R26
R18
C16
R6
R23
R5
D9
R12
Q3
R17
Q7
Q5
D10
D11
R28
R14
R4
R24
C5
D12
R1
R22
R15
D1
R27
R11
Q1
R13
R19
D6
D2
R21
C2
D5
R22
D4
D3
C1
R3
C11
C12
R32
D34
R53
R30
D28
D35
C15
R31
R57
D29
D36
R29
R56
D37
R37
Q15
Q17
Q14
Q16
R45
Q10
Q12
R49
D33
R46
D32
R59
D27
R52
Q18
D31
Q9
Q11
R58
D26
D25
R48
R41
D23
R47
R34
D30
Q13
D24
R39
R40
R51
D16
C13
D22
D19
R43
D18
R44
D20
R38
R42
D15
Q8
R33
R35
R36
G085
09-0392

G100
Sense Amplifier and Inhibit Driver

The G100 module contains four sense amplifiers and four inhibit drivers. Five of these modules are used in the PDP-15 for each 4K memory stack. (Refer to Engineering Drawings D-BS-MM15-0-10 through D-BS-MM15-0-15). Each inhibit driver consists of a two-input NAND gate and a high-speed current switch. One driver is used for each bit plane of the memory array. An inhibit signal is received by all inhibit drivers only during a write operation.



G100 Simplified Diagram

Each driver also receives a signal indicating the state of the corresponding bit in the MB. Inhibit drivers that receive a signal indicating a 0 state in the MB bit are gated on and cause inhibit current to be applied to the associated bit plane of the memory array. Each inhibit driver employs a discharge network to speed up inhibit current cut-off. The output of the inhibit driver is connected to the middle of one core sensing string, which represents one bit plane of the memory array. The balun network at the front end of the sense amplifier ensures equal current at all times through both sides of the core string. In addition to the balun network, the sense amplifier consists of a differential amplifier and output driver. One sense amplifier is used for each bit plane of the memory array. During a read operation only the signal induced on the sense winding of a core plane by a core-changing state is received by the differential amplifier. The differential amplifier has a nominal threshold of 17 mV. Output pulses of standard amplitude and duration are supplied by the output driver when the sense amplifier reads a logic 1 from the associated core, which in turn is strobed by a standard positive going pulse at AC1. Propagation delay from the input to the sense amplifier to the buffered output is 25 ns (maximum) and from strobe input to buffered output is 15 ns (maximum). These output pulses are used to direct set the MB register.

The following are the input, output, and power characteristics of the G100 module.

INPUTS: Inhibit driver DATA inputs present 1.25 TTL unit loads and INHIBIT inputs present 5 unit loads. Sense amplifier inputs are 0-9 mV for a logic 0 and 31-35 mV for a logic 1.

OUTPUTS: Inhibit driver inhibit current is 730 mA.

POWER: Power dissipation of the G100 module is +5V at 130 mA (maximum), -6V at 60 mA (maximum), and -24V at 800 mA (maximum).

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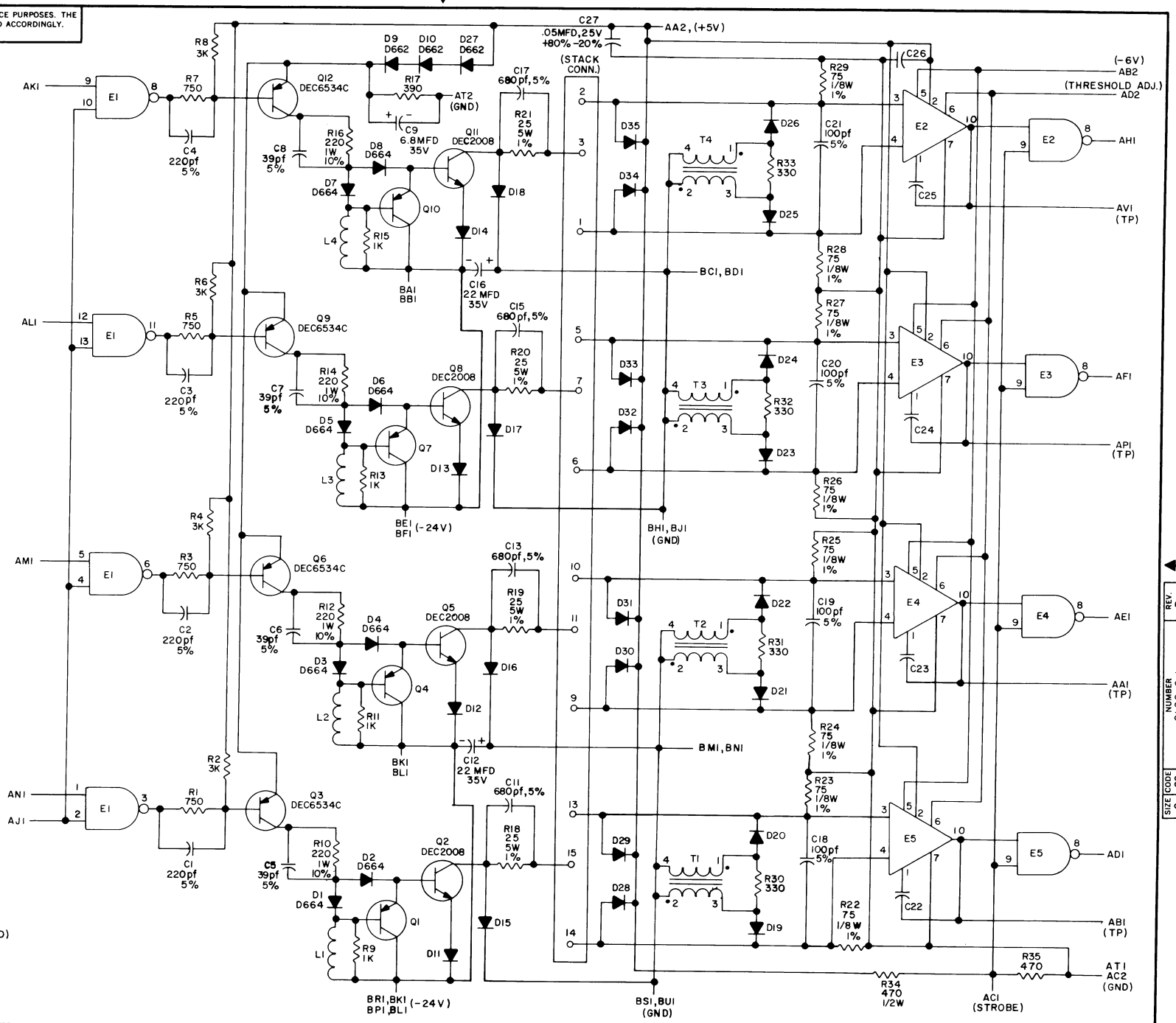


UNLESS OTHERWISE INDICATED:
DIODES ARE D672
CAPACITORS ARE .01MFD,100V, 20%
RESISTORS ARE 1/4W, 5%
TRANSISTORS ARE DEC3639B
E1 IS DEC74H00N
E2, E3, E4, E5, ARE DEC1540G
PIN 7 ON E1 IS TIED TO AT1, AC2 (GND)
PIN 7 ON E2, E3, E4, E5 IS TIED TO AT1, AC2 (GND)
PIN 2 ON E2, E3, E4, E5 = +5V
PIN 14 ON E1 = +5V
TRANSFORMERS ARE 1609478
HOUSING IS DEC #1209482
INDUCTORS L1 - L4 ARE 10MH

G100-4

REVISIONS			
CHK	CHG NO	REV.	
	00001	A	
	00002	B	
	00006	C	
	00007	D	

DEC FORM NO. DRC 102

DRN. BUTLER DATE 9/8/69
CHK'D L.O. Applette DATE 9/12/69
ENG. DATE 11/3/69
DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D662	IN645	DEC6534C	MPS6534
D664	IN3606		
D672	IN3653		
DEC3639	2N3639		
DEC2008	NONE		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

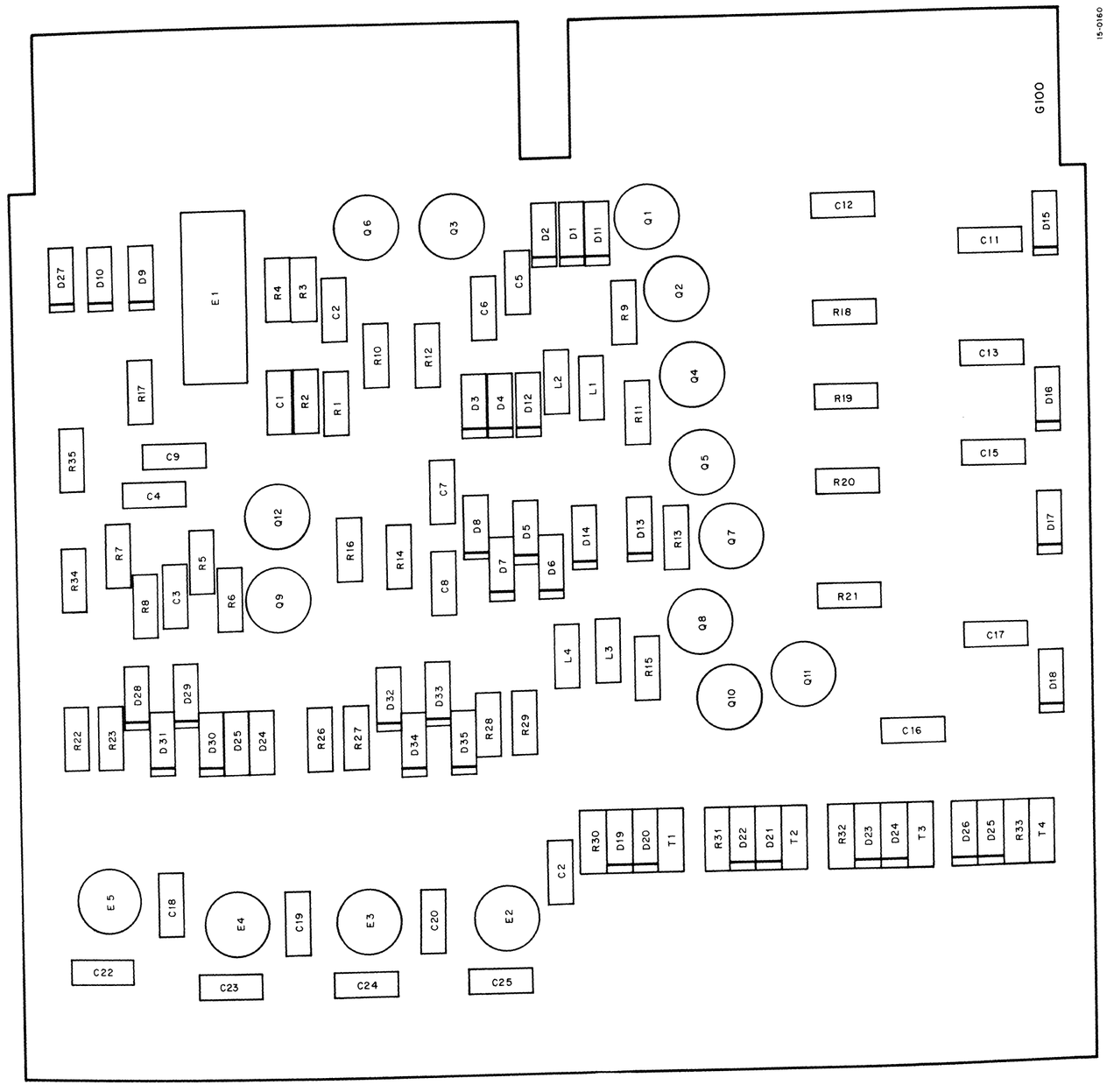
TITLE SENSE AMP AND INHIBIT DRIVER G100

SIZE	CODE	NUMBER	REV.
C	CS	G100-0-1	D.

PRINTED CIRCUIT REV.

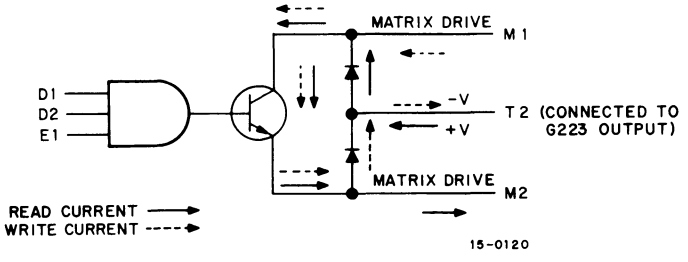
DIST. 324, 434, 435

4


15-0160
G100
C12
C11
D15
R18
C13
D16
R19
C15
R20
D17
R21
C17
D18
C16
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D27
E1
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R34
R35
C1
C2
C3
C4
C5
C6
C7
C8
C9
L1
L2
L3
L4
D28
D29
D30
D31
D32
D33
D34
D35
D24
D25
R22
R23
R26
R27
R28
R29
E2
E3
E4
E5
C18
C19
C20
C22
C23
C24
C25
R30
D19
D20
T1
R31
D22
D21
T2
R32
D23
D24
T3
D26
D25
R33
T4

G222
Memory Selector

The G222 module contains four memory selectors. Eight of these modules are used in the PDP-15 for each 4K memory stack. (Refer to Engineering Drawings D-BS-MM15-0-6 and D-BS-MM15-0-7.) The modules are used to decode the memory address to obtain the X- and Y-axis select signals for accessing the core memory. Each memory selector consists of a 3-input NAND gate and a bidirectional current switch network for both read and write current. An 8 x 8 matrix (see G613 and G614) is used for each of the X and Y selection paths. Thus, two switches must be energized to establish the path in the X plane, and another two switches must be energized to establish the path in the Y plane. In a 4K system a total of four G222 modules are used to decode the first six bits of the memory address. This provides one out of 64 states for the Y plane. Similarly, four G222 modules are used to decode the remaining six bits of the memory address in order to establish the selection path in the X plane.



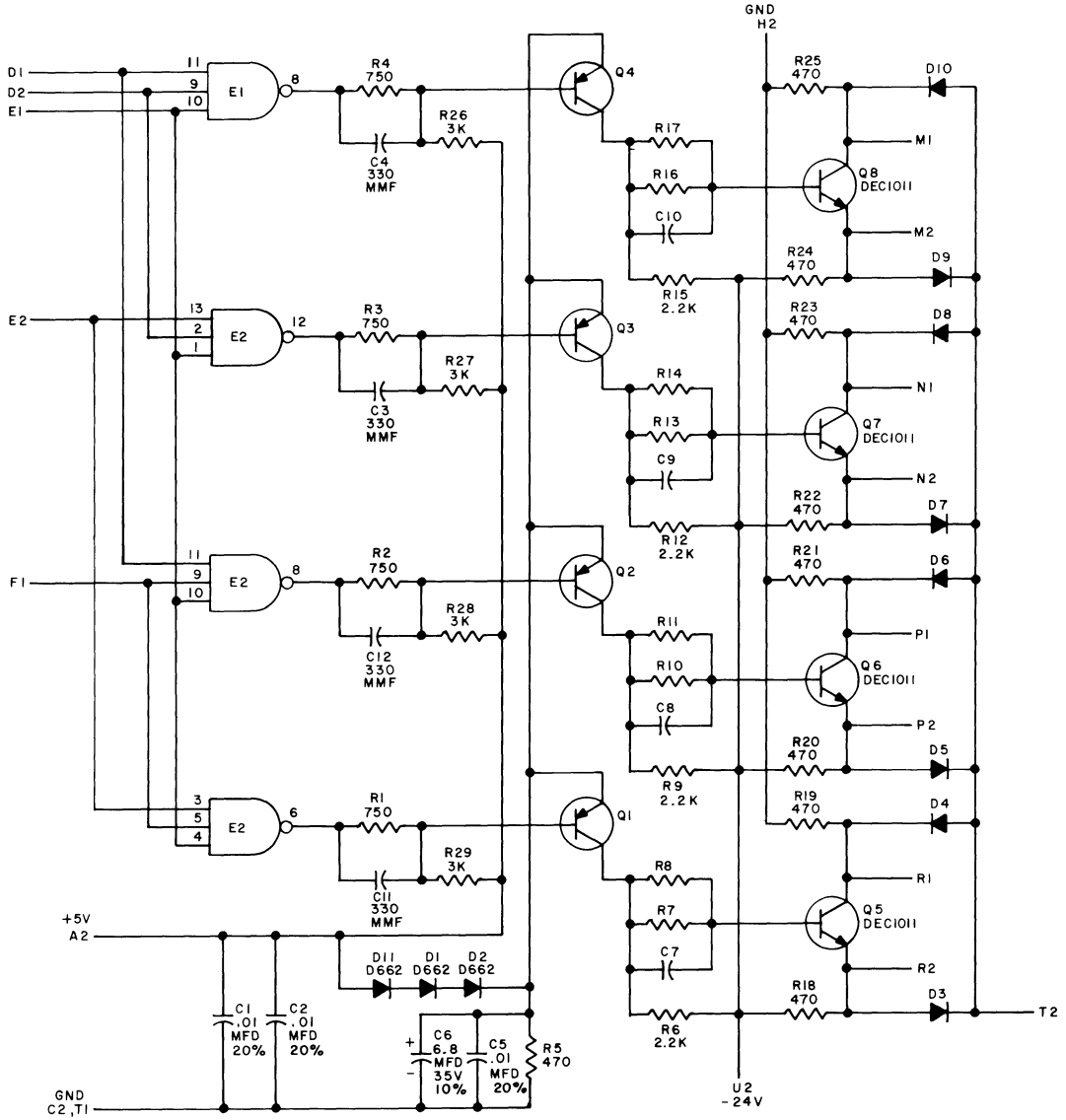
G222 Simplified Diagram

The following are the input and output characteristics of the G222 modules.

INPUTS: Each NAND gate input presents 2.5 TTL unit loads.

OUTPUTS: Each matrix selector switch handles 400 mA (typical).

G222-2



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC6534C
DIODES ARE D672
RESISTORS ARE 1.5K
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE 47 PF, 100V, 5%
IC'S ARE DEC74H10N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

SIZE	CODE	NUMBER	REV.
C	CS	G222-0-1	D

REVISIONS			
CHK	CHG NO.	REV.	
ek	00001	B	
	00002	C	
	00003	D	

DRN M. Weller DATE 4-7-69
CHK'D DATE 4-8-69
ENG DATE 4/14/69
DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC6534C	MPS6534		
D662	IN645		
D672	IN3653		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE MEMORY SELECTOR G222

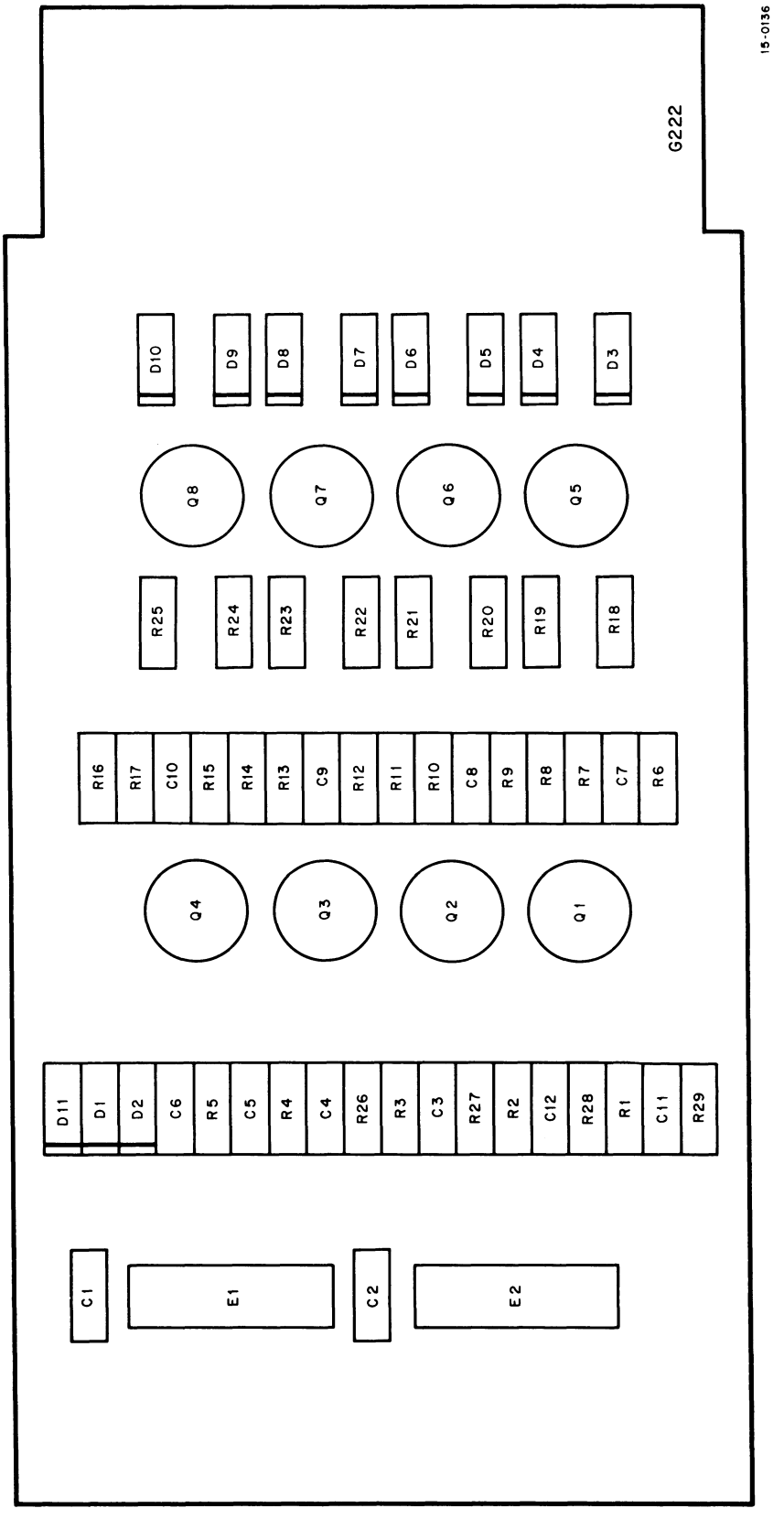
SIZE C | CODE CS | NUMBER G222-[illegible] | REV. D

PRINTED CIRCUIT REV.

DEC FORM NO. DRC 102

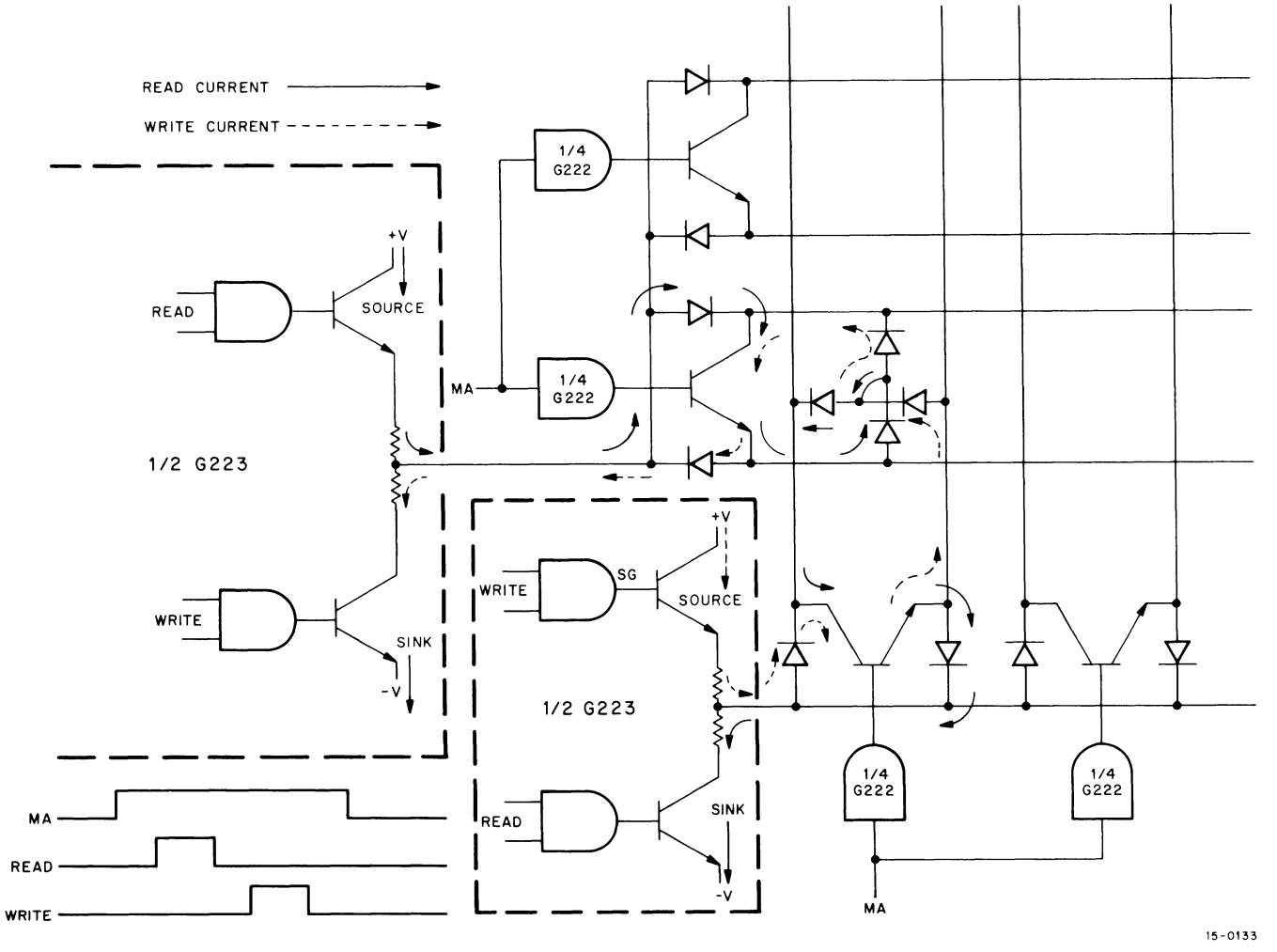
4 DIST. 324, 434, 435

PINK


G222
15-0136
D10
D9
D8
D7
D6
D5
D4
D3
Q8
Q7
Q6
Q5
R25
R24
R23
R22
R21
R20
R19
R18
R16
R17
C10
R15
R14
R13
C9
R12
R11
R10
C8
R9
R8
R7
C7
R6
Q4
Q3
Q2
Q1
D11
D1
D2
C6
R5
C5
R4
C4
R26
R3
C3
R27
R2
C12
R28
R1
C11
R29
C1
E1
C2
E2

G223
Read/Write Driver

The G223 module contains two read/write drivers. Two of these modules are used in the PDP-15 for each 4K memory stack; one provides the drive for the X plane and the other provides the drive for the Y plane. (Refer to Engineering Drawings D-BS-MM15-0-6 and D-BS-MM15-0-7.) The G223 and G222 modules work together (see illustration) in that the current path selection through the core memory is established by the G222 modules, and



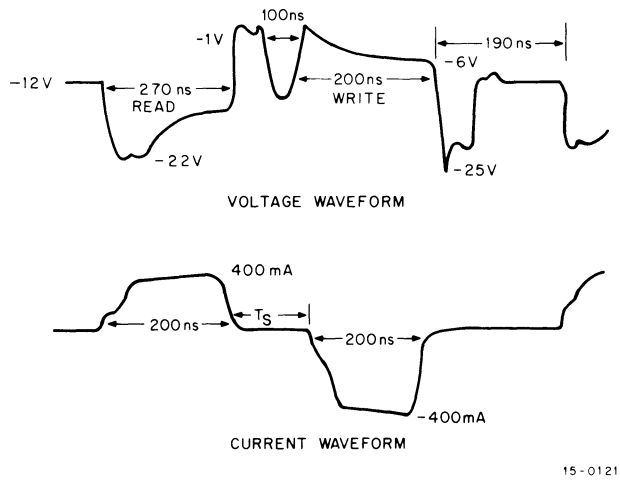
G223 Simplified Diagram

the drive current for reading and writing is supplied by the G223 module. Reading and writing currents travel in opposite directions. Each read/write driver consists of two input control NAND gates and two current switches connected in series with a common output. The read and write commands and the page select command are applied to the input control NAND gates, turning on the corresponding current switches and establishing a current path from ground to -24V. The balun network at the output of the driver ensures equality of input and output current through the stacks at all times.

The following are the input and output characteristics of the G223 module.

INPUTS: The READ and WRITE inputs (pins E1 and F1) each present 1.25 unit loads. The page-select input (pin D1) presents 2.5 unit loads.

OUTPUTS: The measured read/write voltage waveform and its current waveform for the worst case pattern take the form shown below for an 800 ns memory cycle time.



G223 Current and Voltage Waveforms

The current-rise time to get to 400 mA for both reading and writing is approximately 100 ns, while the fall time is 40 ns. The stagger time (Ts) between read and write currents is approximately 130 ns.

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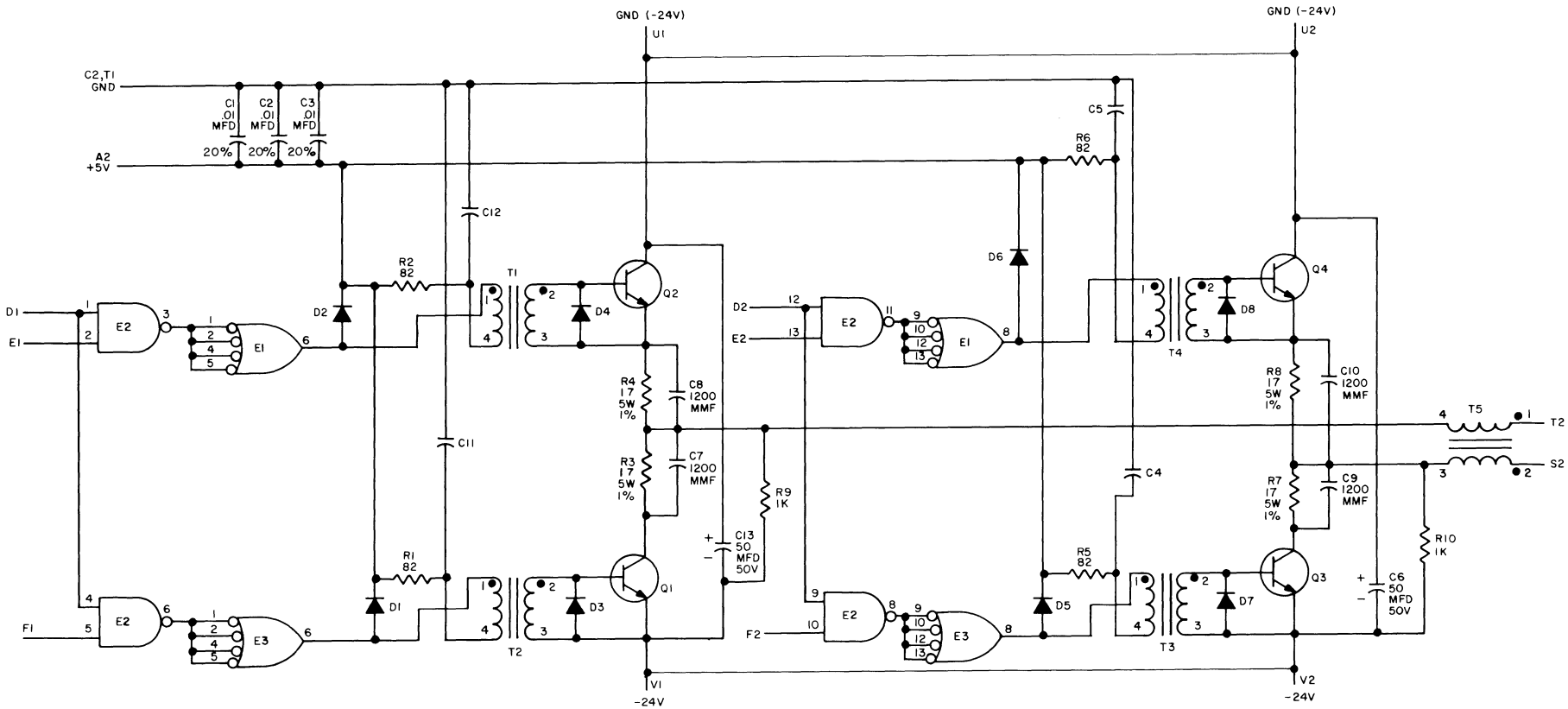


UNLESS OTHERWISE INDICATED:
- TRANSISTORS ARE DEC 1008
- T1-T4 ARE SPRAGUE 5574,17Z1 OR 5387 16-09479
- DIODES ARE D664
- CAPACITORS ARE 120MMF,100V,5%
- RESISTORS ARE 1/4W 5%
- T5 IS SPRAGUE 5386,OR 17Z5 16-09478
- PIN 14 ON EACH IC = +5V
- PIN 7 ON EACH IC = GND
- E2 IS SN74H00N
- E1,E3 ARE SN74H40N

REVISIONS				
CHK	CHG NO.	REV		
	00001	B		
	00002	C		
	000003	D		

DRN. R. BUTLER	DATE 4/11/69	
CHK'D G. Yanega	DATE 4-15-69	
ENG H. LaVoie	DATE 4/21/69	
PE	DATE	

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	IN3606		
DEC1008	MM1008		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: READ WRITE DRIVER G223

SIZE	CODE	NUMBER	REV.
C	CS	G223-0-1	D

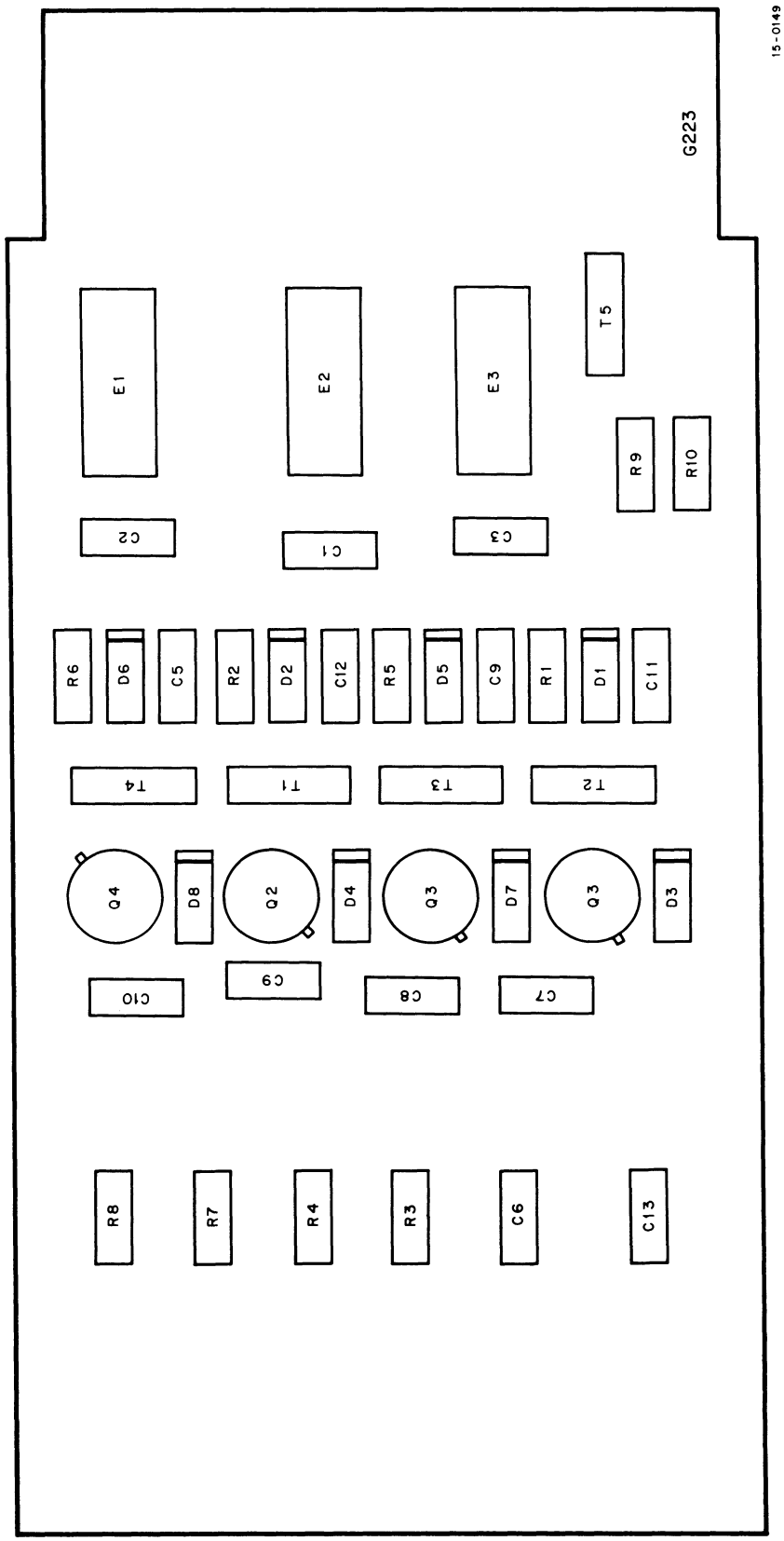
PRINTED CIRCUIT REV.

DEC FORM NO. DRC 102

DIST. 324,434,435

PINK

SIZE C | CODE CS | NUMBER G223-0-1 | REV. D


15-0149
G223
E1
E2
E3
T5
R9
R10
C2
C1
C3
R6
D6
C5
R2
D2
C12
R5
D5
C9
R1
D1
C11
T4
T1
T3
T2
Q4
D8
Q2
D4
Q3
D7
Q3
D3
C10
C9
C8
C7
R8
R7
R4
R3
C6
C13

G285
Series Switch

The G285 Series Switch is a single-height module consisting of two 4-inch AND gates, each driving the base of two driver transistors. This series switch is used together with the G290, the G286, and the G085 to form the Read/Write head matrix in the RS09 DECdisk. When a gate is enabled, it in turn switches its corresponding transistors that form part of the select and read/write matrix of the disk or memory.

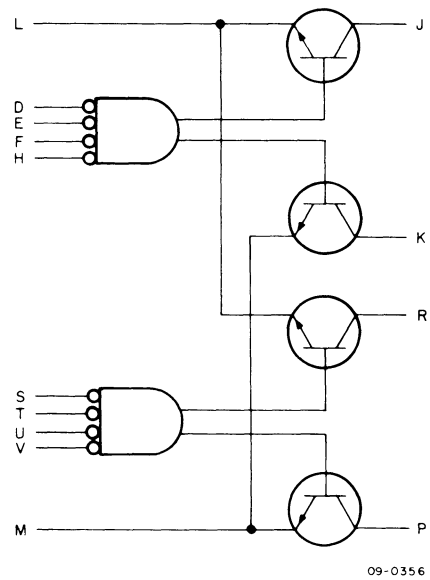
INPUTS: Voltage levels to the gates are 0 and -3V. In levels to the signal inputs L and M are 0 and -15V.

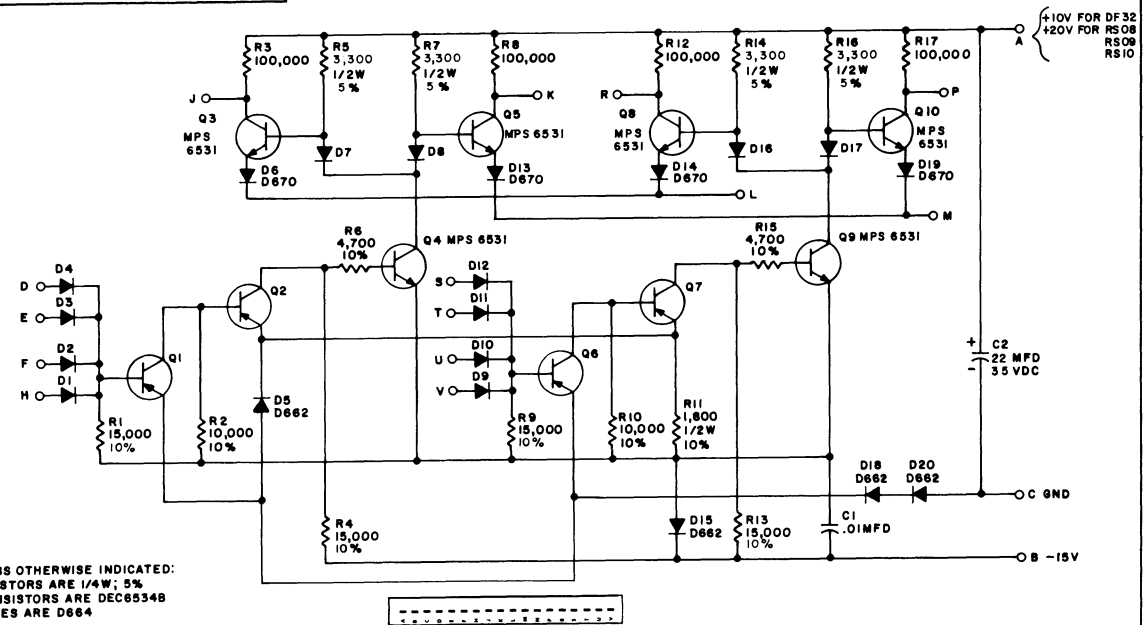
Pin	Function	Load
D,E,F,H,S T,V,M	Gate Enabling Inputs	1 mA shared among inputs at ground
L,M	Signal Inputs	

OUTPUTS: Voltage levels are 0 and -15V (i.e., the input signal gated through the transistor). Each switch pole can drive up to 150 mA. Reverse voltage transients up to 100V do not destroy the switch circuits. Output pins J, K, R, and P must be returned through the load to +10V. The common pins (L and M) to both sets of switches must be returned to -15V. The switches will pass 1 MHz current. The voltage drop for 100 mA is approximately 1V.

INPUT/OUTPUT DELAY: 1 μs

POWER DISSIPATION: 1.5W





UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
TRANSISTORS ARE DEC6534B
DIODES ARE D664

PARTS LIST IS A-PL-G285-0-0

REVISIONS	CHK	CHG NO	REV
		00001	A
		0000003	B

		DATE
DRN	M. Walter	1-30-67
CHK'D		1/31/67
ENG		2/11/67
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

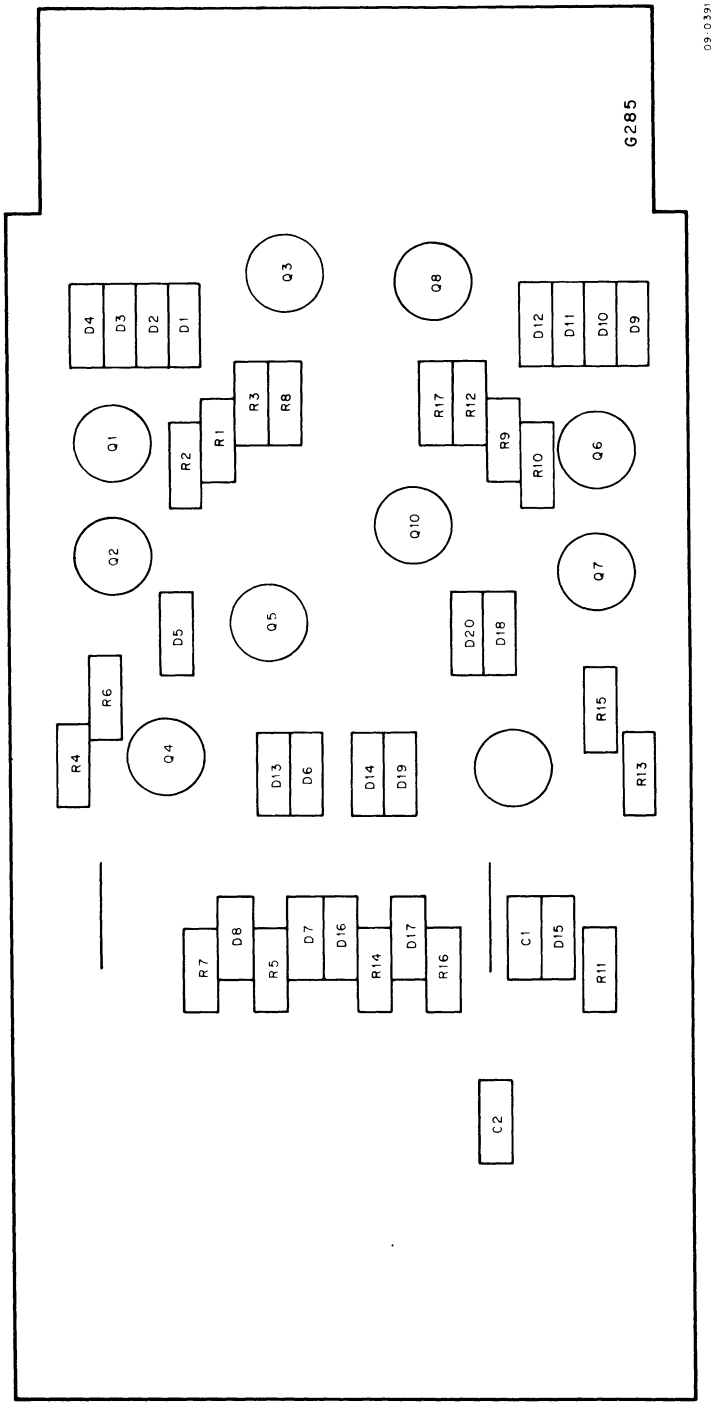
DEC	EIA	DEC	EIA
MPS6531	SAME		
DEC6534B	MPS6534		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: SERIES SWITCH G285

SIZE	CODE	NUMBER	REV
B	CS	G285-0-1	B

PRINTED CIRCUIT REV B


G285
09-0391
D4
D3
D2
D1
Q3
Q8
D12
D11
D10
D9
R3
R8
R17
R12
Q1
R2
R1
R9
R10
Q6
Q10
Q2
Q7
D5
Q5
D20
D18
R6
R15
R4
Q4
D13
D6
D14
D19
R13
R7
D8
R5
D7
D16
R14
D17
R16
C1
D15
R11
C2

G286
Center Tap Selector

The G286 Center Tap Selector is a single-height module consisting of four AND gates, each of which drives a power output stage that applies a +20V level to its output pin when enabled by the gate. This module supplies the +20V read/write level to the coil of each head it drives in the RS09 DECdisk Read/Write matrix.

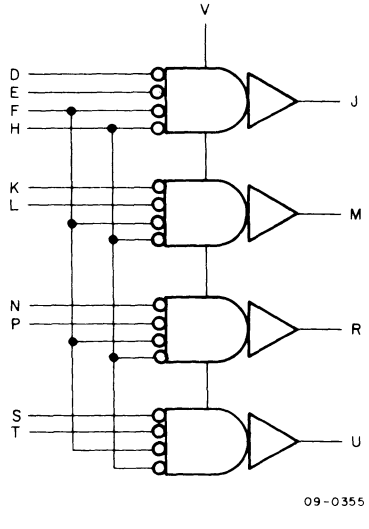
INPUTS: Voltage levels are 0 and -3V.

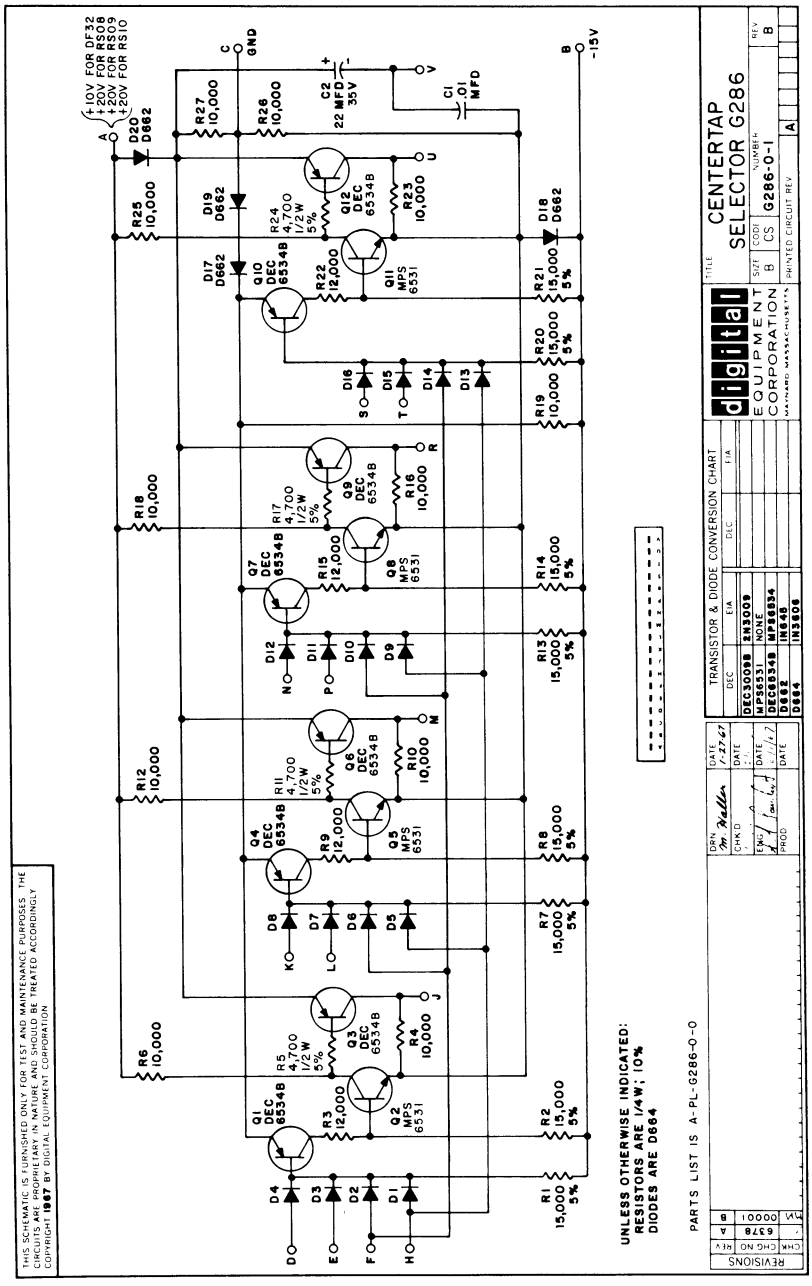
Pin	Function	Load
D,E,K,L,N,P,	Gate inputs	1 mA shared among
S,T,F,H	Gate inputs	inputs at ground in each circuit

OUTPUTS: Each output is +20V when the AND gate is enabled and 0V when the gate is not enabled. Each output drives 150 mA at +20V.

INPUT/OUTPUT DELAY: 500 ns

POWER DISSIPATION: 1.4W




CENTERTAP SELECTOR G286
digital
EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
G286-0-1
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
DEC30098 EN3009
MPS6531 NONE
DEC65349 MPS6534
D662 IN446
D664 IN3600
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D664
PARTS LIST IS A-PL-G286-0-0
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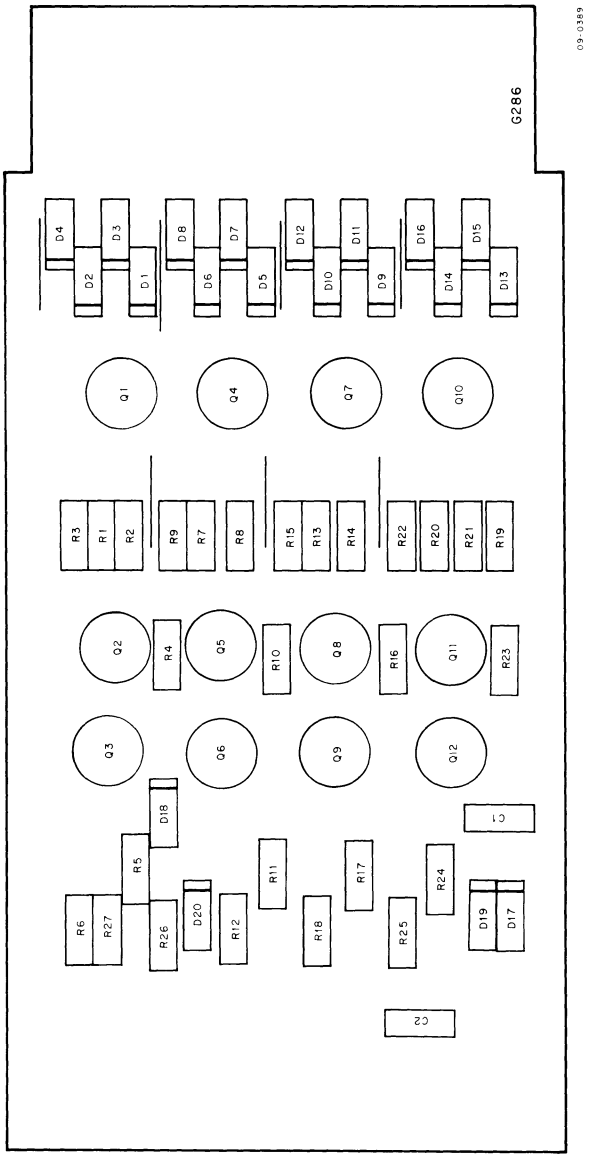
COPYRIGHT 1967 BY DIGITAL EQUIPMENT CORPORATION
REVISIONS
+10V FOR DF32
+20V FOR RS08
+20V FOR RS09
+20V FOR RS10
-15V
GND


G286
09-0389
D4
D3
D8
D7
D12
D11
D16
D15
D2
D1
D6
D5
D10
D9
D14
D13
Q1
Q4
Q7
Q10
R3
R1
R2
R9
R7
R8
R15
R13
R14
R22
R20
R21
R19
Q2
R4
Q5
R10
Q8
R16
Q11
R23
Q3
Q6
Q9
Q12
D18
C1
R5
R11
R17
R24
R6
R27
R26
D20
R12
R18
R25
D19
D17
C2

G290
Writer Flip-Flop

The G290 Writer Flip-Flop is a single-height board containing one JR flip-flop driving two AND gates and two power drivers. This module, used in the RS09 DECdisk supplies the -15V write voltage to the G285 Series Switch. There are several gates to the input of the flip-flop.

INPUTS: Voltage levels are 0 and -3V.

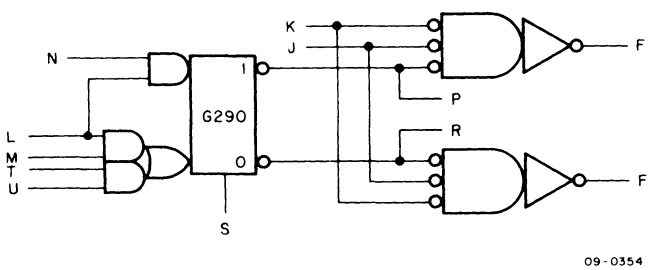
Pin	Function	Load
N,M,T,U,	Inputs to flip-flop	Each gate is a 1 mA
L	Input to flip-flop	load shared among
S	Direct Clear	its grounded inputs
K,J	Enable input to output driver gate	

OUTPUTS: The E and F outputs are -15V or an open collector. The P and R outputs are 0 and -3V.

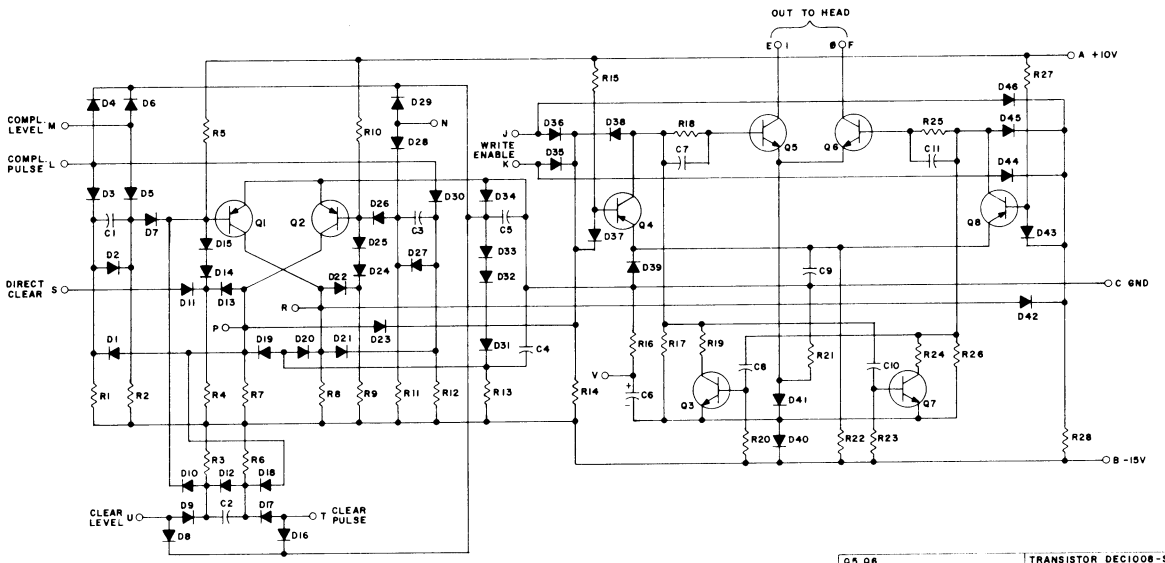
Pin	Function	Drive
E,F	Output to G285 Series Switch	150 mA
P,R	Test output of flip-flop	10 mA

INPUT/OUTPUT DELAY: 90 ns

POWER DISSIPATION: 1W



G290 Writer Flip-Flop, Block Schematic



REFERENCE DESIGNATION	PARTS LIST DESCRIPTION	PART NO.
Q5, Q6	TRANSISTOR DEC1006-S	1502155
Q4, Q8	TRANSISTOR DEC65348	1503409-01
Q3, Q7	TRANSISTOR DEC3009B-S	1503100
Q1, Q2	TRANSISTOR 2N4258	1505321
R19, R24	RES. 100 1/4W 5% CC	1300229
R16	RES. 10 1/4W 10% CC	1300170
R15, R27	RES. 10K 1/4W 10% CC	1300481
R14, R28	RES. 3.3K 1/4W 5% CC	1300439
R25, R26	RES. 1.5K 1/4W 5% CC	1300391
R7, R8, R13, R17, R18, R20-R23, R5, R10	RES. 100K 1/4W 5% CC	1302466
R1-R4, R6, R9, R11, R12	RES. 7.5K 1/4W 5% CC	1301422
D37, D39, D40, D41, D43 D14, D15, D24, D25, D31-D34, D35, D36, D38, D42, D44-D46	DIODE D662	1100113
D1-D13, D16-D23, D26-D30,	DIODE D664	1100114
C8, C10	CAP. 56MMF 100V 5% D.M.	1000012
C7, C11	CAP. 220MMF 100V 5% D.M.	1000021
C6	CAP. 47MFD 20V 20% S.TANT	1000079
C4, C5, C9	CAP. .01MFD 100V 20% DISC	1001610
C1, C2, C3	CAP. 82MMF 100V 5% D.M.	1000015

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D662	IN645	DEC1006	MM1006
D664	IN3606		
2N4258	SAME		
DEC3009B	2N3009		
DEC65348	MPS8534		

REVISIONS			
SYM	CHG NO	REV	

DRN M. Keller DATE 1-10-69
CHK'D W. W. DATE 1-15-69
ENG DATE
PROD DATE

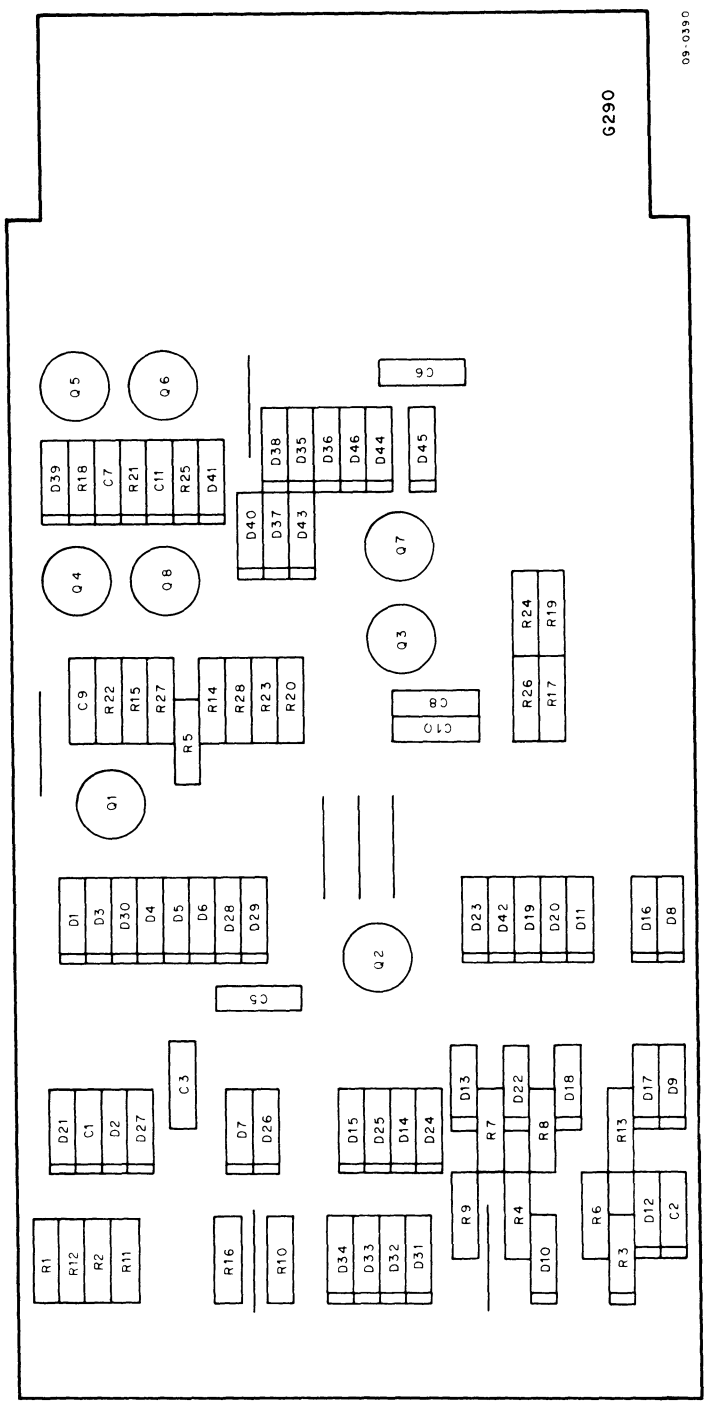
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE WRITER FLIP FLOP G290

SIZE	CODE	NUMBER	REV
C	CS	G290-0-1	

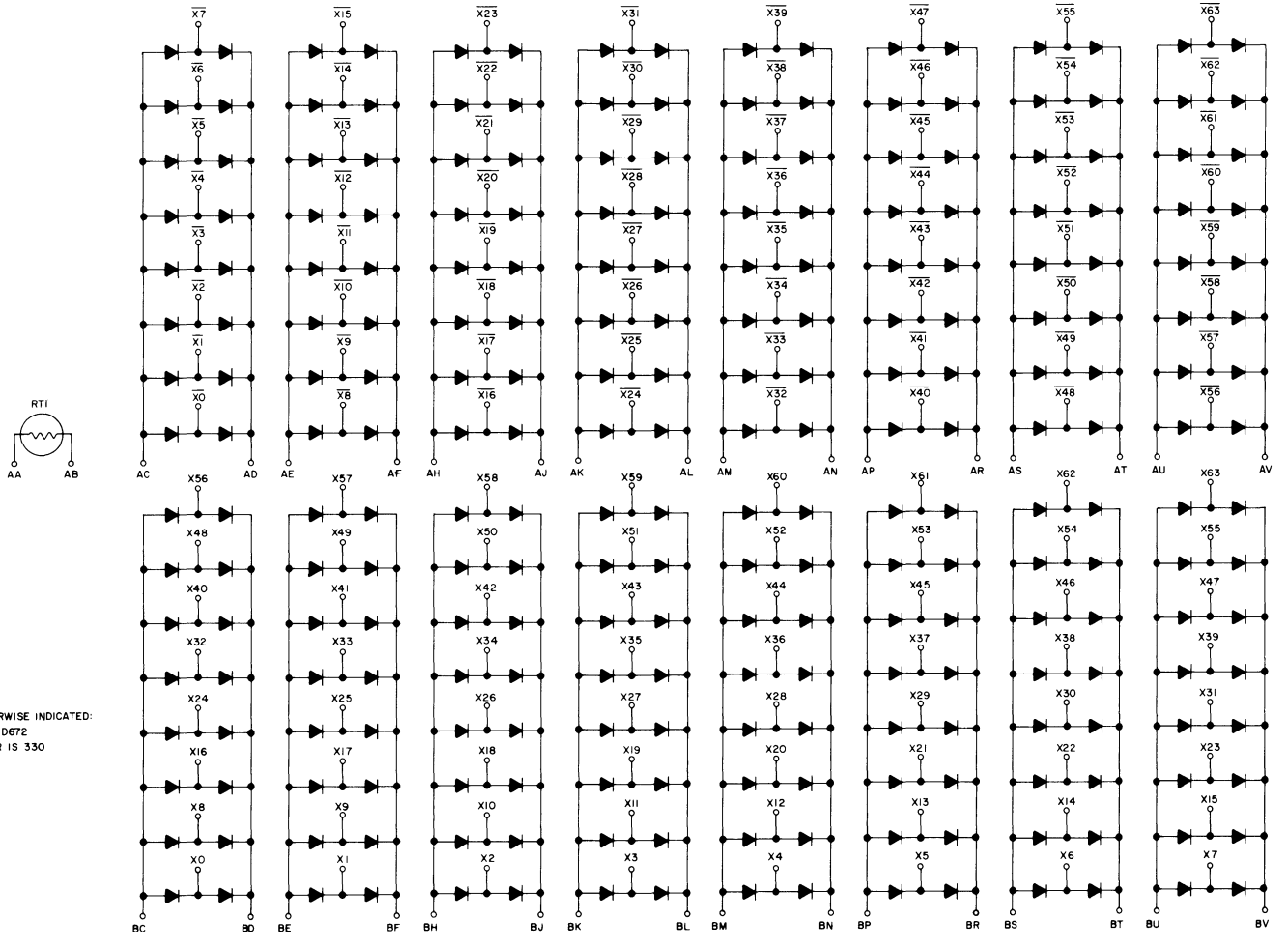
PRINTED CIRCUIT REV. A

G290-2


G290
09-0390
Q5
Q6
D39
R18
C7
R21
C11
R25
D41
D38
D35
D36
D46
D44
D45
D40
D37
D43
Q7
Q4
Q8
Q3
C9
R22
R15
R27
R14
R28
R23
R20
R5
C8
C10
R24
R19
R26
R17
Q1
D1
D3
D30
D4
D5
D6
D28
D29
Q2
D23
D42
D19
D20
D11
D16
D8
C5
C3
D21
C1
D2
D27
D7
D26
D15
D25
D14
D24
D13
R7
D22
R8
D18
R13
D17
D9
R9
R4
D10
R6
R3
D12
C2
R1
R12
R2
R11
R16
R10
D34
D33
D32
D31

G613
X Diode Matrix

The G613 module contains 256 diodes connected to form an 8 x 8 two-way crosspoint switching matrix that provides 64 pairs of interconnecting points. (Refer to Engineering Drawings D-BS-MM15-0-6 and D-BS-MM15-0-7.) Sixty-four cores from each of the 18 memory planes are connected between each pair of interconnecting points, thereby creating the current paths of the X-axis in the core memory stack. A thermistor is also included in the G613 module to control the read and write currents in response to temperature changes.



UNLESS OTHERWISE INDICATED:
DIODES ARE D672
THERMISTOR IS 330

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D672	IN3656		

REVISIONS

CHK	CHG NO.	REV.
[illegible]	00001	A
[illegible]	00002	

DRN. BUTLER 7/25/69
CHK'D. [illegible] 7/25/69
ENG. [illegible] 9/15/69
PROD. DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: X DIODE MATRIX G613

SIZE	CODE	NUMBER	REV.
C	CS	G613-0-1	A

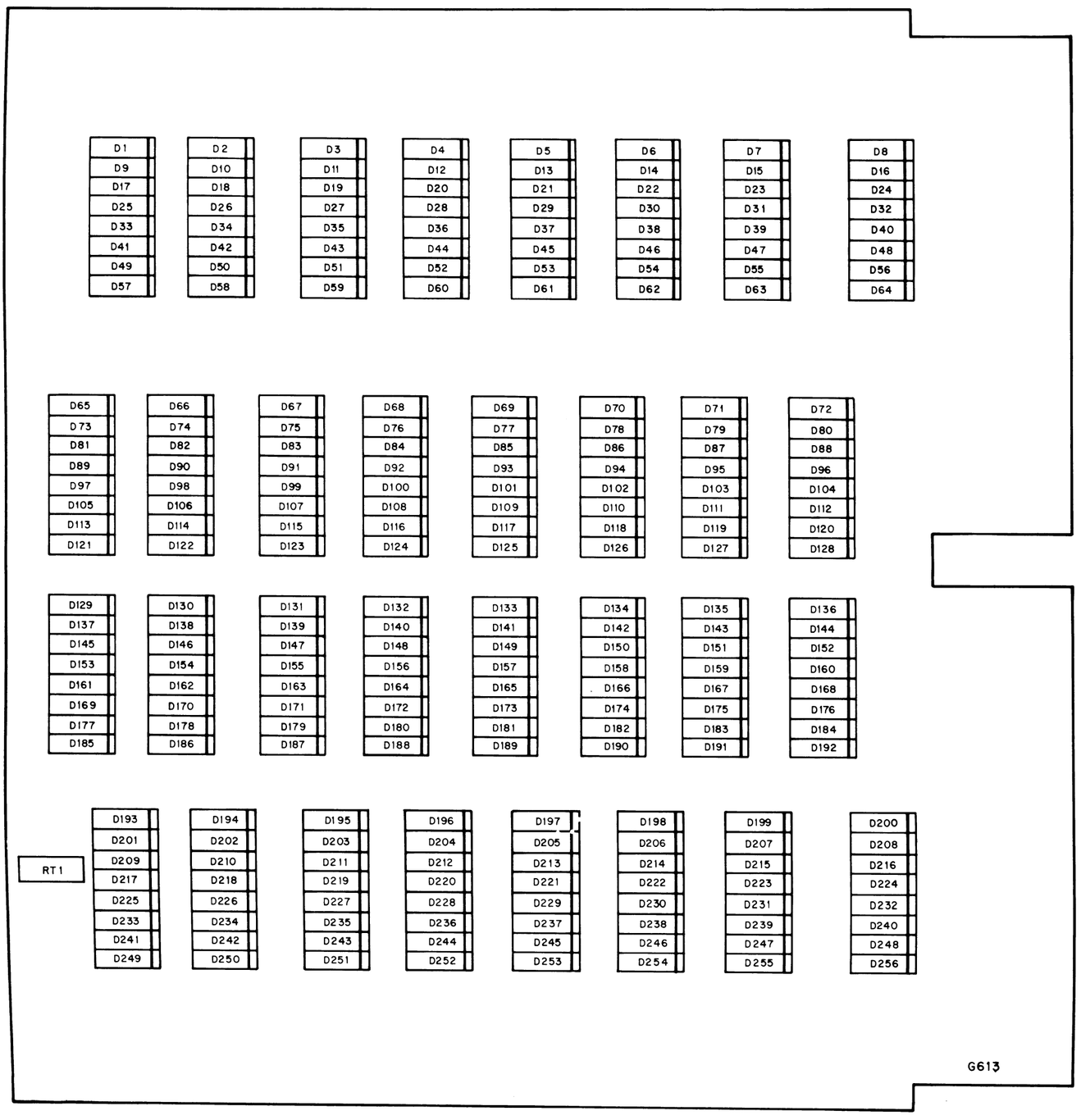
PRINTED CIRCUIT REV. A B C

DEC FORM NO. DRC 102

5 PINK DIST. 324,434,435

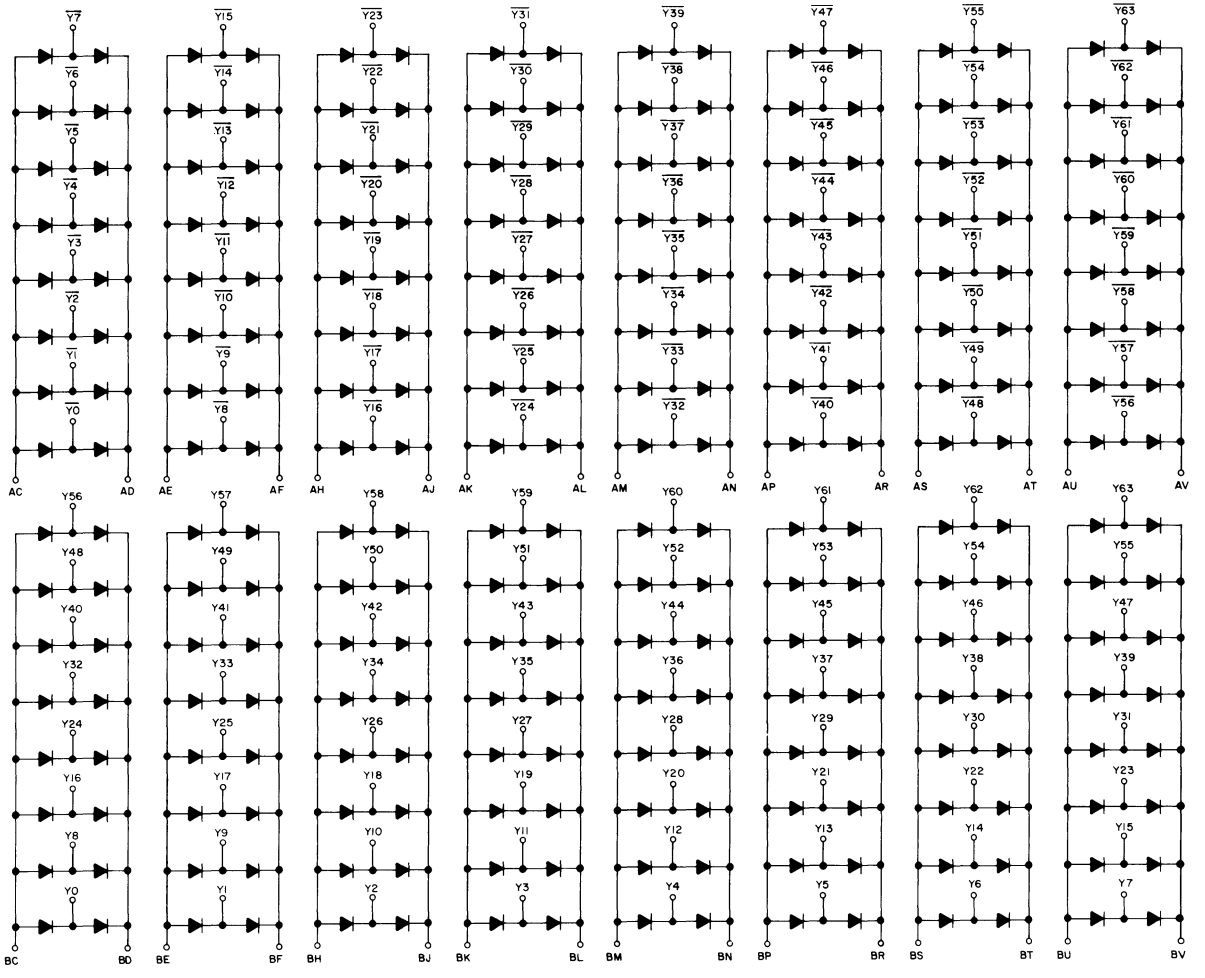
SIZE C CODE CS NUMBER G613-0-1 REV. A

G613-2


D1 D9 D17 D25 D33 D41 D49 D57
D2 D10 D18 D26 D34 D42 D50 D58
D3 D11 D19 D27 D35 D43 D51 D59
D4 D12 D20 D28 D36 D44 D52 D60
D5 D13 D21 D29 D37 D45 D53 D61
D6 D14 D22 D30 D38 D46 D54 D62
D7 D15 D23 D31 D39 D47 D55 D63
D8 D16 D24 D32 D40 D48 D56 D64
D65 D73 D81 D89 D97 D105 D113 D121
D66 D74 D82 D90 D98 D106 D114 D122
D67 D75 D83 D91 D99 D107 D115 D123
D68 D76 D84 D92 D100 D108 D116 D124
D69 D77 D85 D93 D101 D109 D117 D125
D70 D78 D86 D94 D102 D110 D118 D126
D71 D79 D87 D95 D103 D111 D119 D127
D72 D80 D88 D96 D104 D112 D120 D128
D129 D137 D145 D153 D161 D169 D177 D185
D130 D138 D146 D154 D162 D170 D178 D186
D131 D139 D147 D155 D163 D171 D179 D187
D132 D140 D148 D156 D164 D172 D180 D188
D133 D141 D149 D157 D165 D173 D181 D189
D134 D142 D150 D158 D166 D174 D182 D190
D135 D143 D151 D159 D167 D175 D183 D191
D136 D144 D152 D160 D168 D176 D184 D192
RT1
D193 D201 D209 D217 D225 D233 D241 D249
D194 D202 D210 D218 D226 D234 D242 D250
D195 D203 D211 D219 D227 D235 D243 D251
D196 D204 D212 D220 D228 D236 D244 D252
D197 D205 D213 D221 D229 D237 D245 D253
D198 D206 D214 D222 D230 D238 D246 D254
D199 D207 D215 D223 D231 D239 D247 D255
D200 D208 D216 D224 D232 D240 D248 D256
G613
15-0152

G614
Y Diode Matrix

The G614 module contains 256 diodes connected to form an 8 x 8 two-way crosspoint switching matrix providing 64 pairs of interconnecting points. (Refer to Engineering Drawings D-BS-MM15-0-6 and D-BS-MM15-0-7.) Sixty-four cores from each of the 18 memory planes are connected between each pair of interconnecting points, thereby creating the current paths of the Y axis in the core memory stack.



UNLESS OTHERWISE INDICATED:
DIODES ARE D672
COMPONENTS ARE MOUNTED ON SIDE TWO OF ETCH BOARD

REVISIONS			
CHK	CHG NO.	REV	
	00001	A	
	00002	B	
	00003	C	
	00004	D	

DRN BUTLER DATE 7/25/69
CHK'D DATE
ENG DATE
PROD. DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D672	IN3656		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

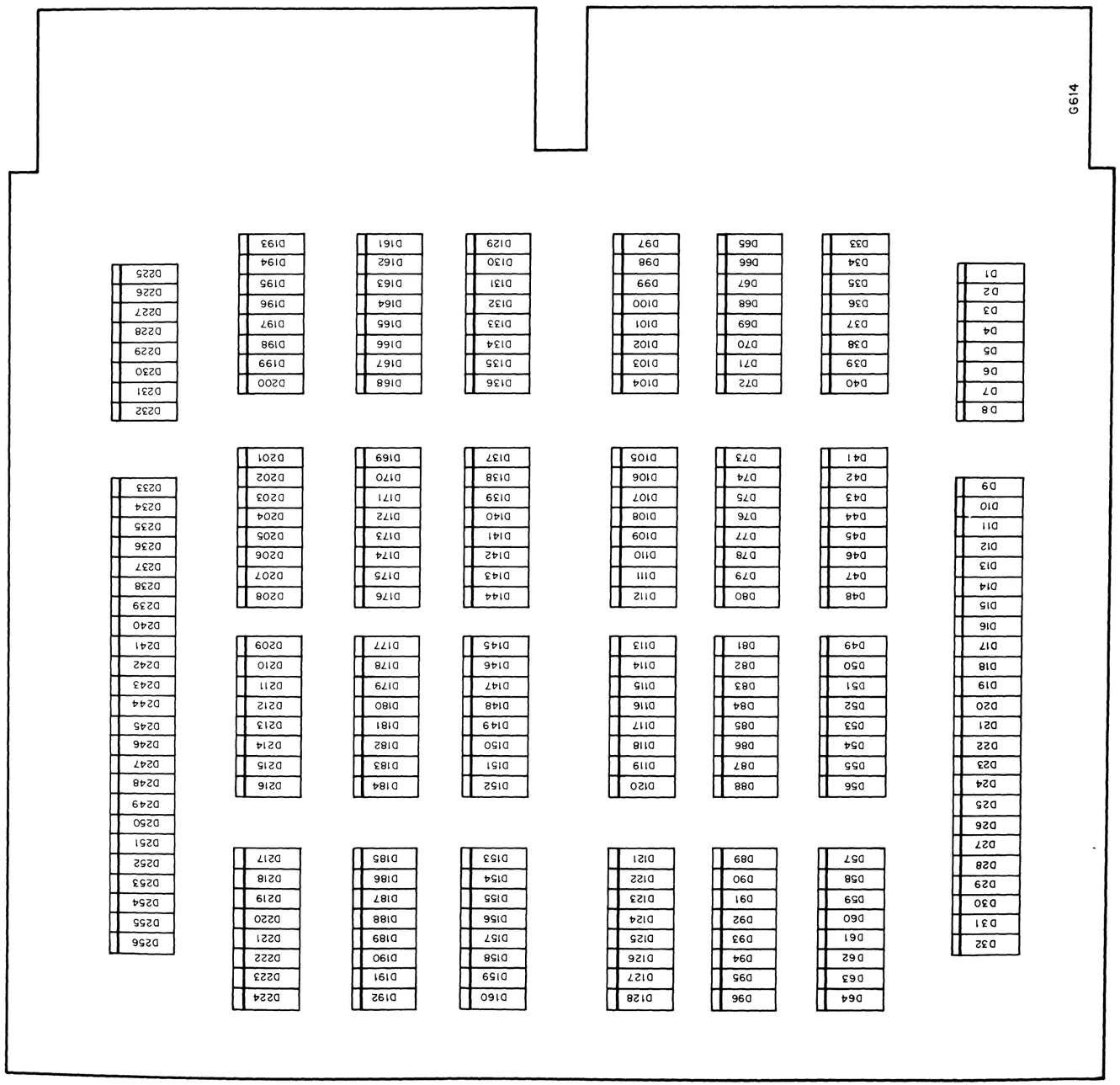
TITLE: Y DIODE MATRIX G614

SIZE C | CODE CS | NUMBER G614-0-1 | REV D

PRINTED CIRCUIT REV. A B C

DEC FORM NO. RC 102

SIZE C | CODE CS | NUMBER G614-0-1 | REV D


G614
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D242
D243
D244
D245
D246
D247
D248
D249
D250
D251
D252
D253
D254
D255
D256

G681,G711,G775
DECdisk Modules

1. G681 8 TRACK MATRIX

The G681 Track Matrix is a single-height board containing the resistors and diodes for eight DECdisk read/write heads.

2. G711 RF08 TERMINATOR BOARD

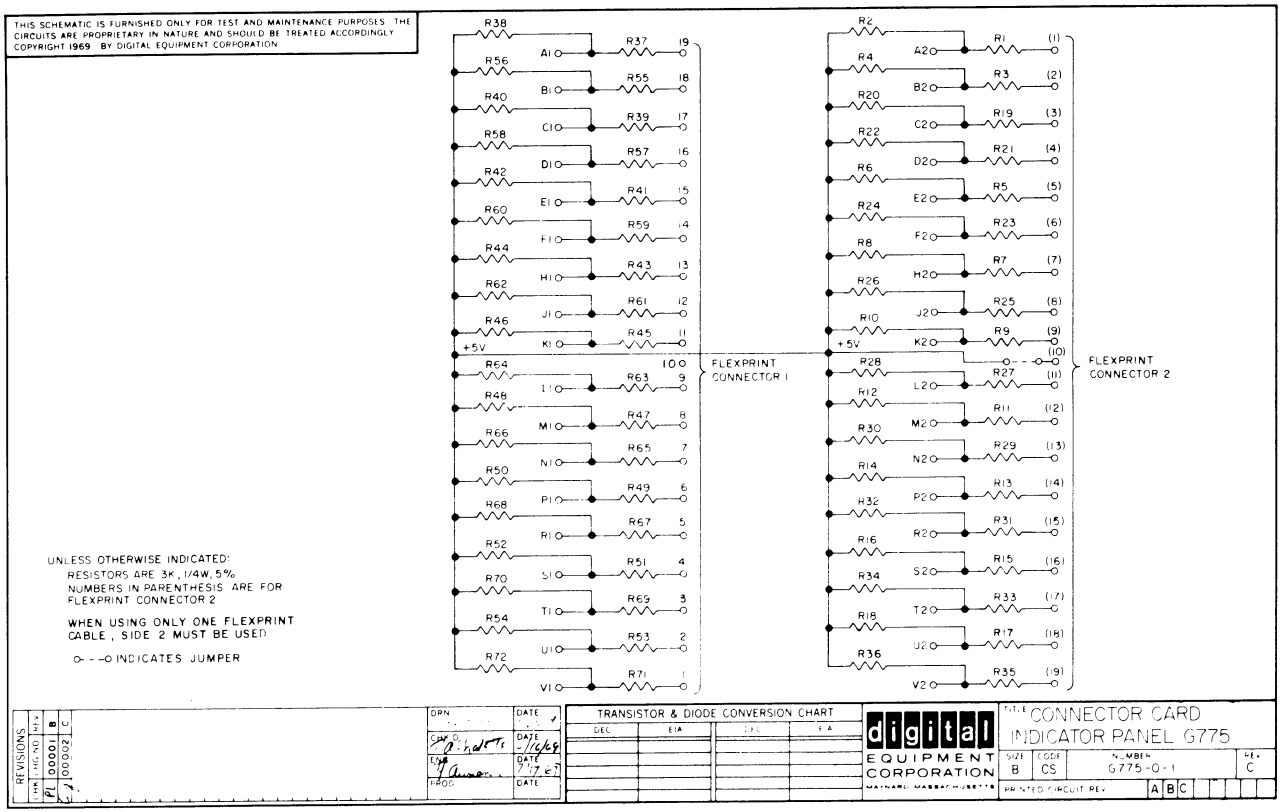
The G711 RF08 Terminator Board is a single-height board containing 15 terminating resistors that present 100Ω to ground at each input pin. This board must connect to the output cable slot of the last RS09 on each DECdisk cable bus.

INPUTS:	100Ω to ground
OUTPUTS:	None
POWER DISSIPATION:	Approximately 90 mW per terminator

3. G775 INDICATOR PANEL

The G775 Indicator Panel is a connector card that provides isolation for logic levels and allows these levels to directly drive indicator bulbs without using light drivers. The connector is designed to be used with the indicator panel, which supplies the necessary bias voltage.

INPUTS:	All inputs are 0 and -3V with 3 units of load each.
OUTPUTS:	The output connects a Flexprint cable to the indicator board.
POWER DISSIPATION:	150 mW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R38 R56 R40 R58 R42 R60 R44 R62 R46 +5V R64 R48 R66 R50 R68 R52 R70 R54 R72
A1 B1 C1 D1 E1 F1 H1 J1 K1 L1 M1 N1 P1 R1 S1 T1 U1 V1
R37 19 R55 18 R39 17 R57 16 R41 15 R59 14 R43 13 R61 12 R45 11 100 R63 9 R47 8 R65 7 R49 6 R67 5 R51 4 R69 3 R53 2 R71 1
FLEXPRINT CONNECTOR 1
R2 R4 R20 R22 R6 R24 R8 R26 R10 +5V R28 R12 R30 R14 R32 R16 R34 R18 R36
A2 B2 C2 D2 E2 F2 H2 J2 K2 L2 M2 N2 P2 R2 S2 T2 U2 V2
R1 (1) R3 (2) R19 (3) R21 (4) R5 (5) R23 (6) R7 (7) R25 (8) R9 (9) (10) R27 (11) R11 (12) R29 (13) R13 (14) R31 (15) R15 (16) R33 (17) R17 (18) R35 (19)
FLEXPRINT CONNECTOR 2
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 3K, 1/4W, 5%
NUMBERS IN PARENTHESIS ARE FOR FLEXPRINT CONNECTOR 2
WHEN USING ONLY ONE FLEXPRINT CABLE, SIDE 2 MUST BE USED
o- -o INDICATES JUMPER
REVISIONS
ECO 000001 B
ECO 000002 C
DRN
DATE
ENG
DATE 7/16/69
ENG
DATE 7/17/69
PROG
DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE CONNECTOR CARD INDICATOR PANEL G775
SIZE B
CODE CS
NUMBER G775-0-1
REV C
PRINTED CIRCUIT REV A B C

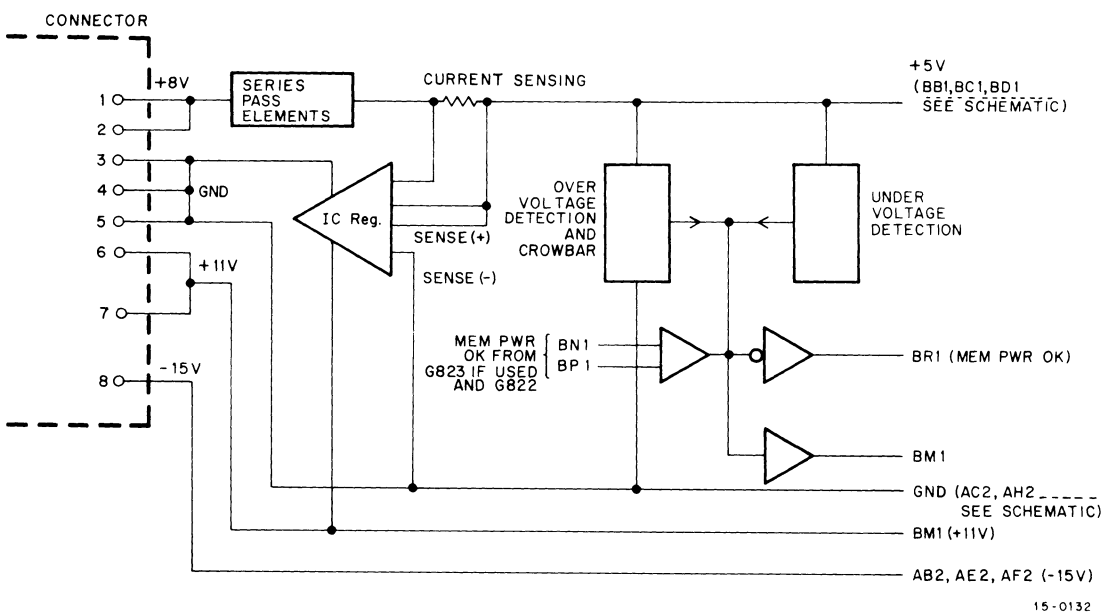
G821
+5V Regulator

The G821 module contains a voltage regulator with over-voltage, under-voltage, and over-current protection circuits. This module supplies the regulated +5V in the memory of the PDP-15. Combinational logic circuits are also included in the module to provide lamp driver and memory power OK signals when the memory voltages are within set levels. The input power connections to the module are made with an 8-pin mate-in-lock connector at the back of the module.

The following are the input and output characteristics of the G821 module.

INPUTS: The inputs to the G821 module are +8V, +11V, -15V, and ground. These voltages are supplied by the 715 power supply. The module also receives positive level power OK signals from the G822 and G823 modules.

OUTPUTS: The outputs of the G821 module are variable 4.5V to 5.5V at 7A (maximum)* (when set at 5V, regulation is ±2% with a ripple voltage of 25 mV peak-to-peak); +11V at 1.0 amp (maximum) with the same regulation as the input voltage; and -15V at 3.0 amps (maximum) with the same regulation as the input voltage.

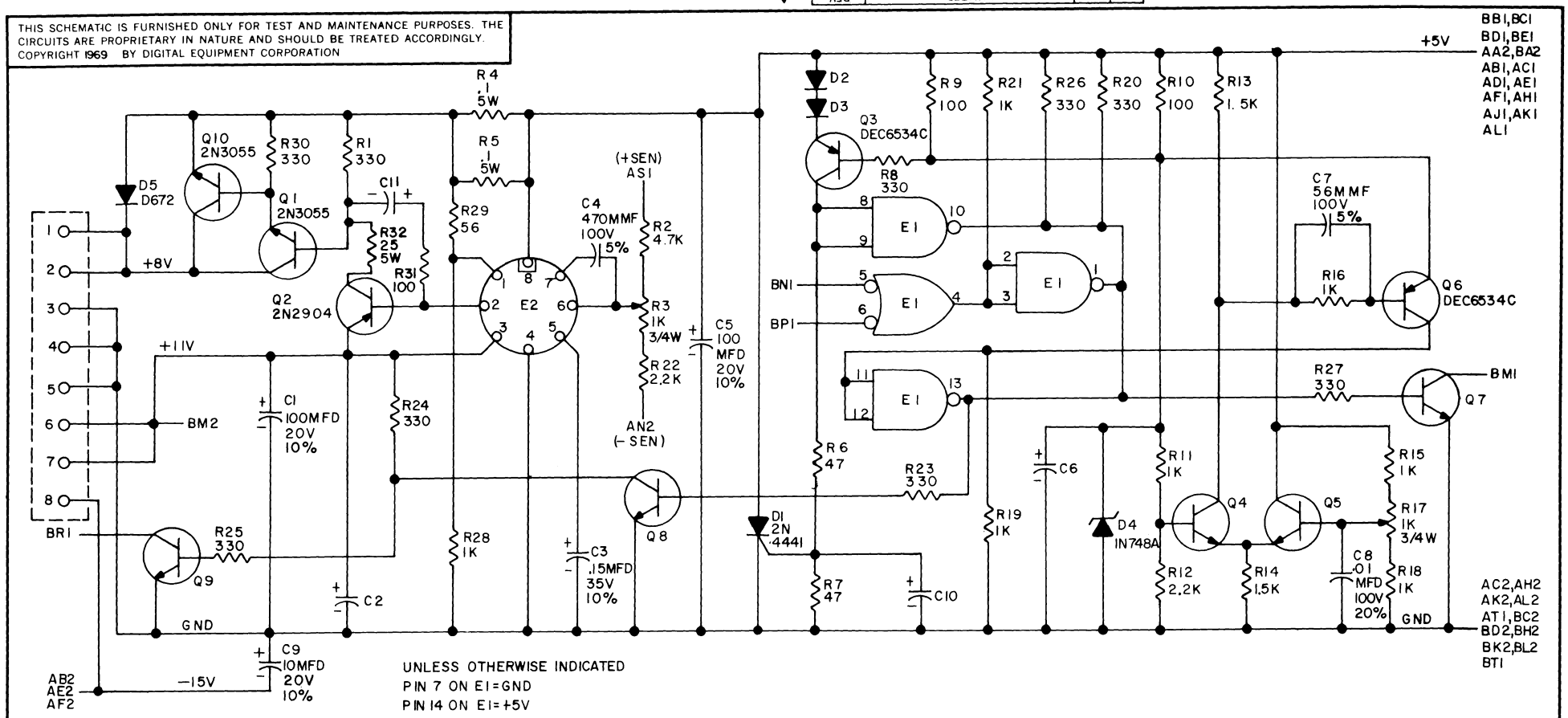


G821 Simplified Diagram

*The 7A rating is valid only when adequate fan cooling is used. Without additional coding, the output rating is 2A (maximum). The +5V potentiometer must be rotated clockwise to obtain a higher output voltage.

Additional outputs include an open collector lamp driver (output pin BM1) that is turned on when the 5V power is within set limits (by rotating the voltage detection potentiometer CCW, the low voltage limit decreases) and an open collector driver (output pin BR1) that is turned on only when the 5V power is not within set limits. Voltage limits are usually set at 4.75V by the voltage detection potentiometer, while the upper voltage detection level is set at 5.5V.

SIZE	CODE	NUMBER	REV.
B	CS	G821-0-1	B



UNLESS OTHERWISE INDICATED
PIN 7 ON E1=GND
PIN 14 ON E1=+5V
E1 IS DEC7401N
E2 IS LM300
CAPACITORS ARE 1MFD, 35V, 10%
DIODES ARE D664
RESISTORS ARE 1/4W 5%
R3, R17 ARE POTS #76PR
TRANSISTORS ARE DEC3009B

REVISIONS	REV	CHG NO	CHK
	A	00001	
	B	00002	

DRN.		DATE 1-29-69
CHK'D	R.A. Valette	DATE 2/5/69
ENG.	Wm Cramer	DATE 10/31/69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606	2N2904	SAME
D672	IN3653	2N3055	NONE
IN748A	SAME		
DEC3009B	2N3009B		
DEC6534B	MPS6534		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
+5V REGULATOR CONTROL G821

SIZE	CODE	NUMBER	REV.
B	CS	G821-0-1	B

PRINTED CIRCUIT REV. F

DEC FORM NO.
DRB 102

4 DISP. 324,434,435 PINK

G821-3

G822
−6V Regulator

The G822 module contains a voltage regulator with an over-voltage protection circuit. This module supplies the regulated -6V in the memory of the PDP-15. A sensing circuit is also included on the module to provide a memory power OK signal when the output is more negative than -6.5V.

The following are the input and output characteristics of the G822 module.

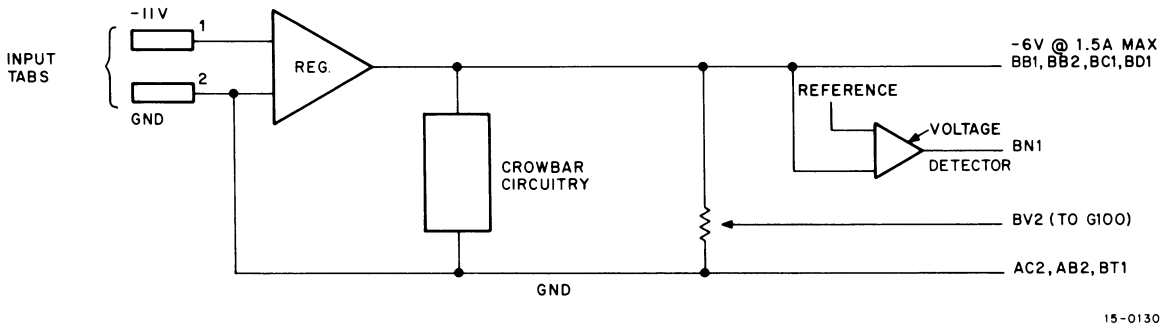
INPUTS: The G822 module operates on 11V input power from the 715 power supply.

OUTPUTS: The outputs of the G822 module are:

a. variable -5.0 to -7.0V at 1.5A. (When set at -6V, regulation is ±2% with a ripple voltage of 50 mV peak-to-peak. The potentiometer must be rotated clockwise to obtain a more negative voltage setting);

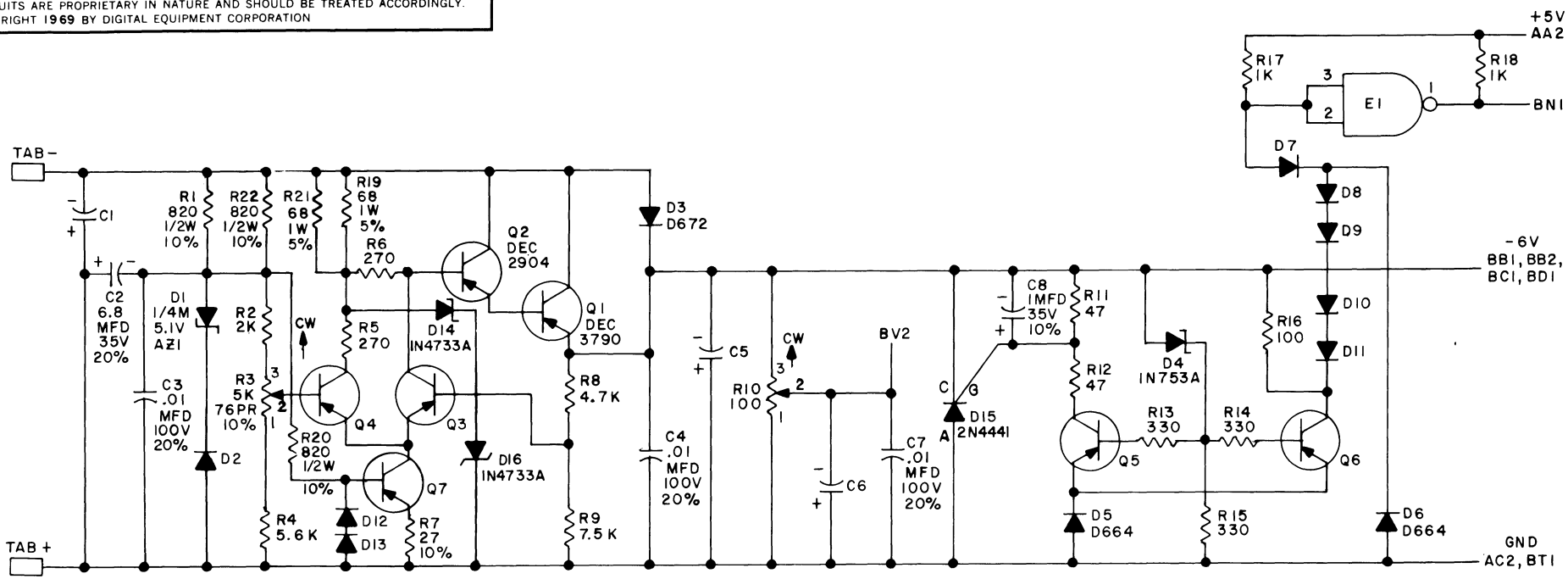
b. variable 0 to -6.0V used as the threshold voltage for the G100 module. (This voltage is nominally set at -3.8V. The potentiometer must be turned clockwise to obtain a more negative voltage setting);

c. BN1, which is a TTL output that drops to ground when the -6V output voltage is more negative than -6.5V.



G822 Simplified Diagram

REV.	NUMBER	CODE	SIZE
E	G822-0-1	CS	B



UNLESS OTHERWISE INDICATED:
DIODES ARE D662
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE 20MFD, 50V, -10 +75%
TRANSISTORS ARE DEC6534B
E1 IS DEC7401
PIN 7 ON E1 = GND
PIN 14 ON E1 = +5V

REVISIONS	REV	CHG NO	CHK
	C	00001	
	D	00002	
	E	00003	

DRN. M. Haller	DATE 12-15-69	
CHK'D	DATE	
ENG. E O Connor	DATE 12/30/69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	IN645	DEC6534B	MPS6534
D664	IN3606	DEC2904	2N2904
1/4M 5.1V AZ1	NONE	DEC3790	2N3790
IN753A	SAME	IN4733A	SAME
2N4441	NONE		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: −6V REGULATOR G822

SIZE	CODE	NUMBER	REV.
B	CS	G822-0-1	E

PRINTED CIRCUIT REV. F

DEC FORM NO. DRB 102

5

DIST. 324,434,1135 PMK

G822-2

15-0161
G822
D7
D6
D8
D9
D10
D11
R16
D4
R15
R14
R13
Q6
D5
Q5
D15
C5
E1
R17
R18
C4
R11
R12
C8
D1
R4
D2
R20
D13
D12
R7
R9
R8
D3
C6
C1
Q3
D14
Q7
Q2
Q1
R10
C7
Q4
C3
C2
R3
R2
R1
R19
R5
R6

G823
−24V Regulator Control

The G823 module contains a temperature-compensated voltage regulator control with an over-voltage protection circuit. This module is used in conjunction with the -24V pass element (G825) to supply a regulated -24V for the memory of the PDP-15 (see illustration). A thermistor mounted on the G613 module is connected to the -24V regulator control module to provide a negative temperature coefficient for controlling the regulated -24V. For a typical setting of -24V at 25°C and with an average output current of 4A, the output voltage changes to -22.4V at 50°C and to -25V at 0°C. The over-voltage protection circuit will disconnect the output above -26V.

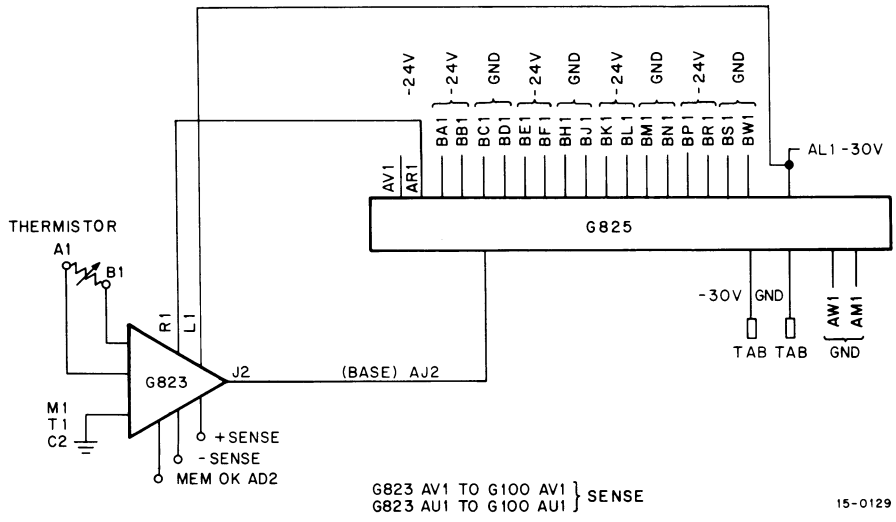
The following are the input and output characteristics of the G823 module.

INPUTS: The G823 module receives -30V from the 715 power supply.

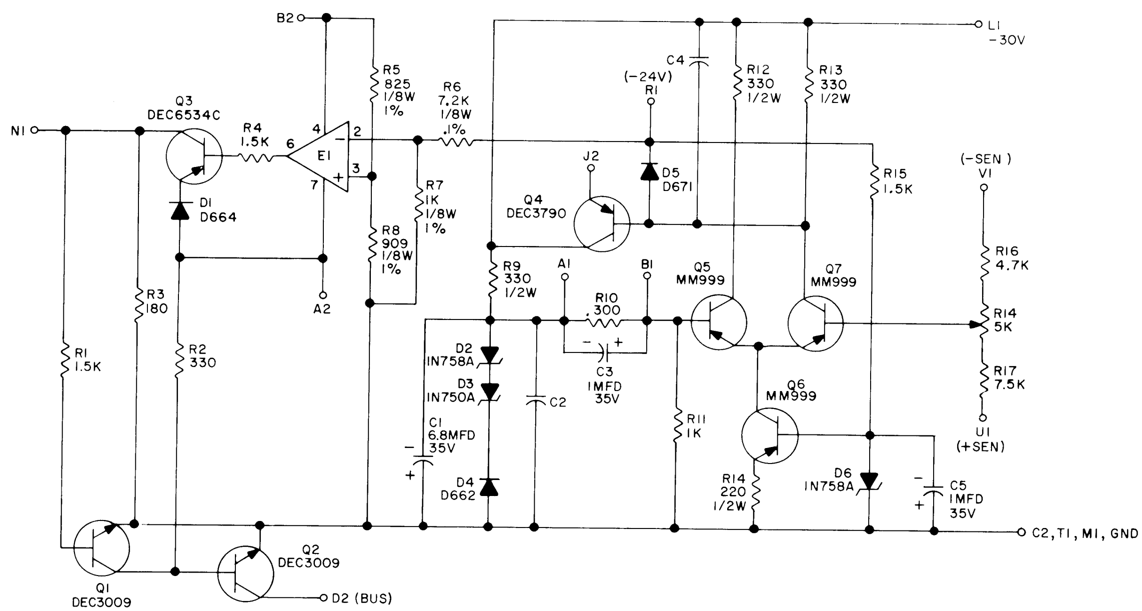
OUTPUTS: The outputs of the G823 module are:

a. A variable -18V to -28V at 5.5A. When the module is set for -24V regulation, the output is ±1% with a ripple voltage of less than 50 mV peak-to-peak at full load. Rotating the potentiometer CCW provides a more negative voltage setting.

b. An open collector driver (output pin N1) that supplies a memory power OK signal when the regulator control is operating properly.



G823 Simplified Diagram



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD
RESISTORS ARE 1/4W, 5%
E1 IS MC1709CG

REVISIONS

CHK	CHG NO	REV
Pd	10000	C

		DATE
DRN	[illegible]	7/23/69
CHK'D	[illegible]	7/30/69
ENG	[illegible]	7/31/69
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

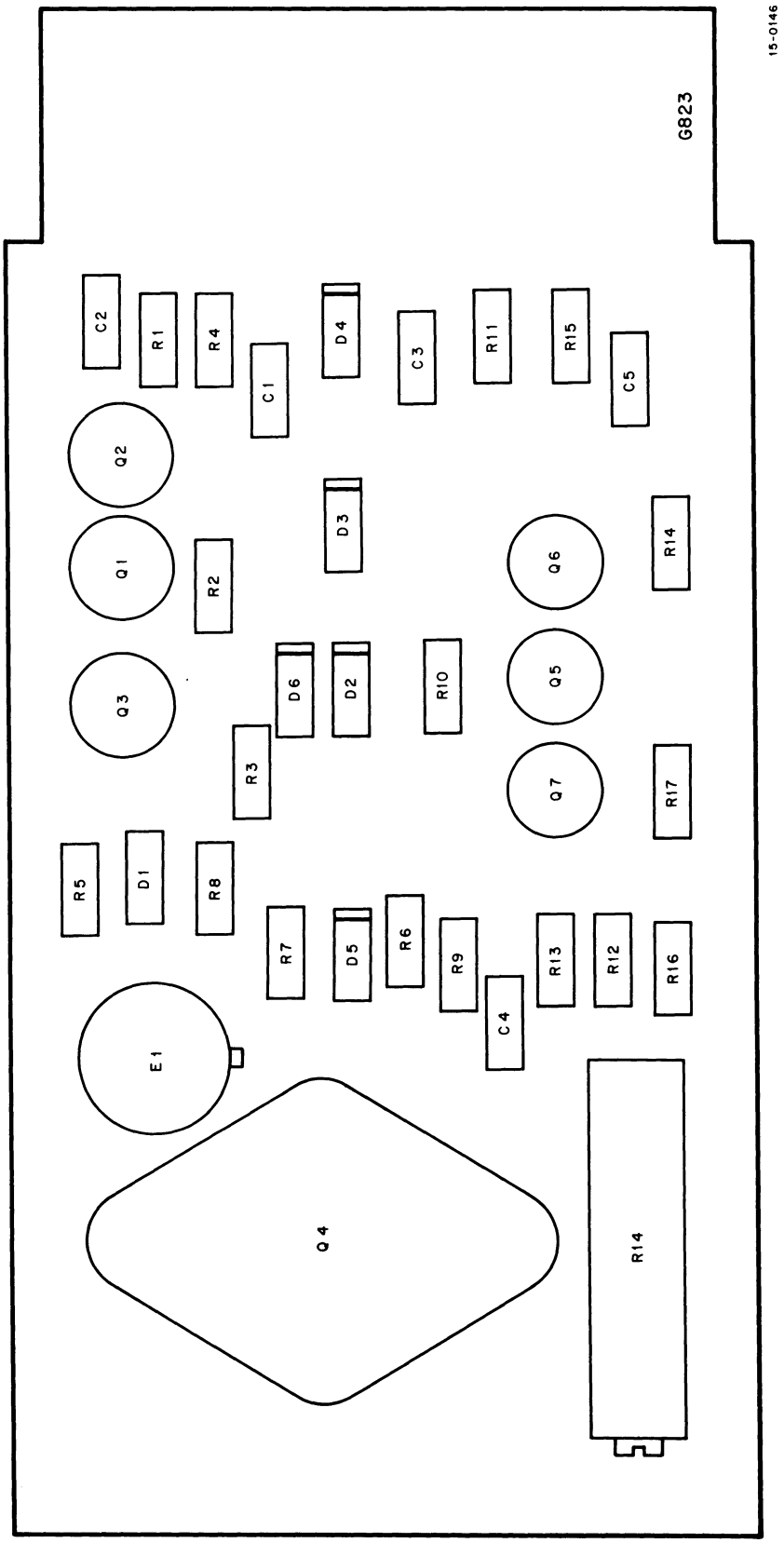
DEC	EIA	DEC	EIA
D662	1N645	MM999	SAME
D664	1N3606	DEC3790	2N3790
D671	1N3653	DEC6534C	MPS6534
1N758A	SAME	DEC3009	2N3009
1N750A	SAME		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE -24V REGULATOR CONTROL G823

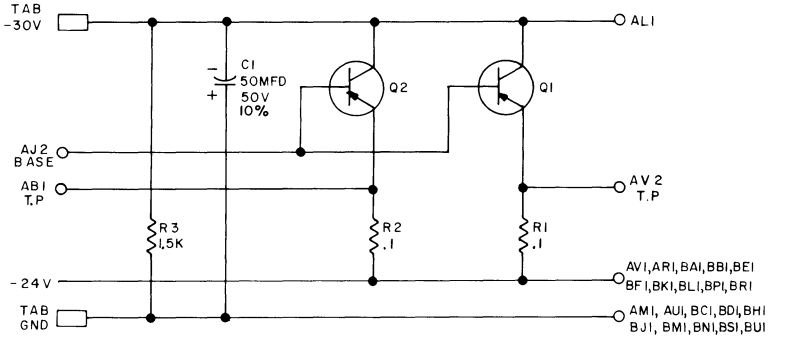
SIZE	CODE	NUMBER	REV
B	CS	G823-0-1	C

PRINTED CIRCUIT REV B C


G823
15-0146
C2
R1
R4
C1
D4
C3
R11
R15
C5
Q2
Q1
R2
D3
Q6
R14
Q3
D6
D2
R10
Q5
R3
Q7
R17
R5
D1
R8
R7
D5
R6
R9
R13
R12
R16
E1
C4
Q4
R14

G825
—24V Pass Element

The G825 module contains the power stage of the -24V regulator, which is controlled by the -24V regulator control module G823 to supply the regulated -24V for the memory of the PDP-15. Refer to the description of the G823 module.



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 5W, 5%
TRANSISTORS ARE DEC 3790-1

REVISIONS	REV	CHG NO	CHK

DRN		DATE	7-25-69
APVD		DATE	8-9-69
ENG		DATE	10/5/69
PROD		DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3790	2N3790		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
-24V PASS ELEMENT G825

SIZE	CODE	NUMBER	REV
B	CS	G825-0-1	

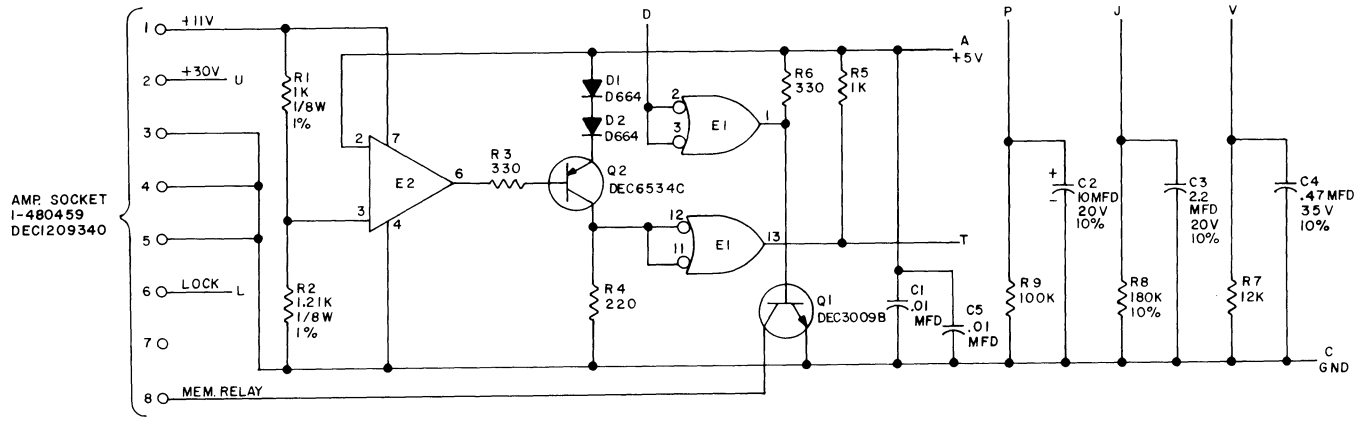
PRINTED CIRCUIT REV B

G825-2

G827
Power Sequence Detector and Delays

The G827 module contains a level detector, three RC networks, and an open-collector driver. This module is used in the I/O processor of the PDP-15. (Refer to Engineering Drawing D-BS-KP15-0-57.) The level detector is used to detect a power-low condition in the 11V supply and sequence the memory power off. The RC networks are connected to the K303 timers to establish the timer delays, and the open-collector driver is used to energize the memory power relay in response to the memory OK signal.

Power dissipation of the G827 module is 5V at 144 mA (maximum).



UNLESS OTHERWISE INDICATED
CAPACITORS ARE 100V, 20%
RESISTORS ARE 1/4 W, 5%
PIN 7 ON E1 = GND
PIN 14 ON E1 = +5V
E1 IS DEC 7401N
E2 IS MC1709CG

REVISIONS	CHK	CHG NO	REV
		00001	B

DRN		DATE 8-6-68
CHK'D		DATE 8/6/68
ENG		DATE 10/2/69
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

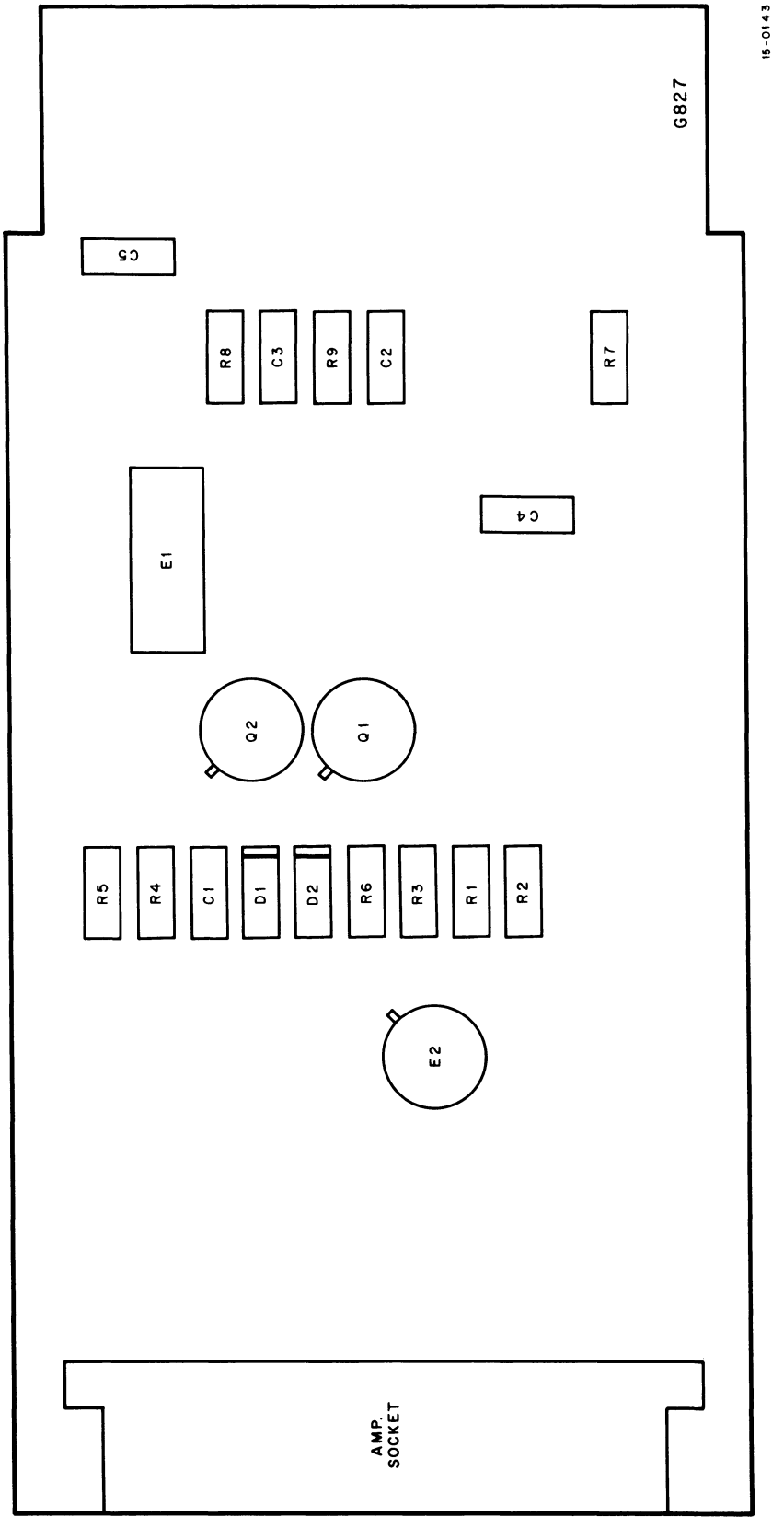
DEC	EIA	DEC	EIA
D664	1N3606		
DEC3009C	2N3009		
DEC6534	MPS6534		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE POWER SEQUENCE DELAYS AND DECODER G827

SIZE	CODE	NUMBER	REV
B	CS	G827-0-1	B

PRINTED CIRCUIT REV A


G827
15-0143
C5
R8
C3
R9
C2
R7
E1
C4
Q2
Q1
R5
R4
C1
D1
D2
R6
R3
R1
R2
E2
AMP.
SOCKET

G829
Power Connector

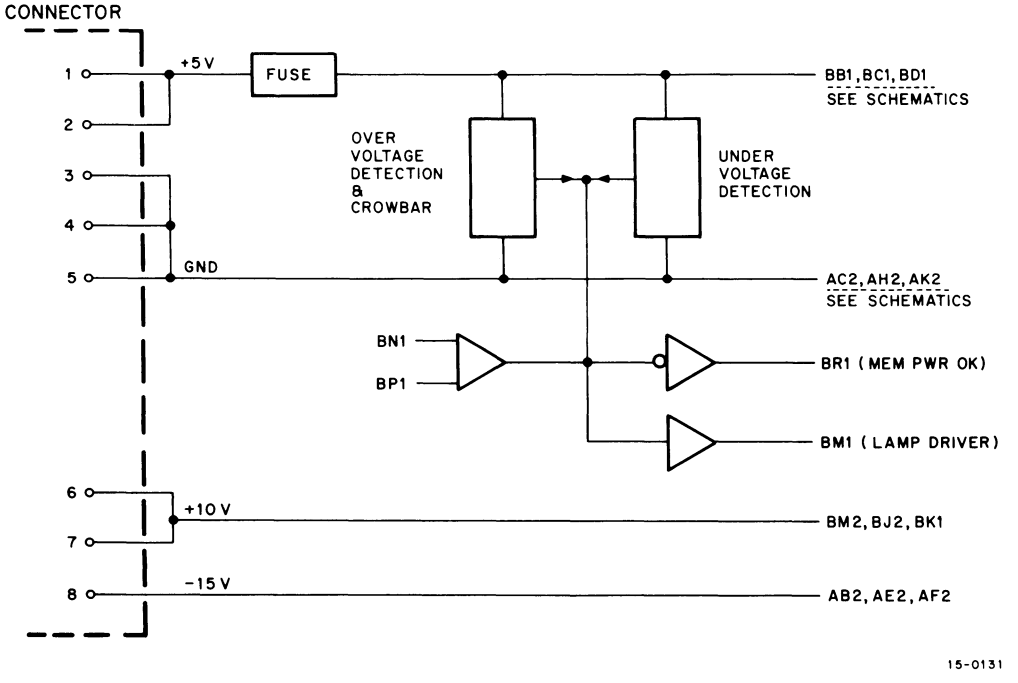
The G829 module is a power connector with over-voltage, under-voltage, and over-current protection circuits. This module connects the +5V to the peripherals of the PDP-15. Combinational logic circuits are also included in the module to provide lamp driver and power OK signals when the peripheral voltages are within set levels. Rotating the voltage detection potentiometer CCW lowers the low voltage limit. The potentiometer is normally set to detect voltage below 4.75V. The input power connections to the module are made with an 8-pin mate-in-lock connector at the back of the module.

The following are the input, output, and power characteristics of the G829 module.

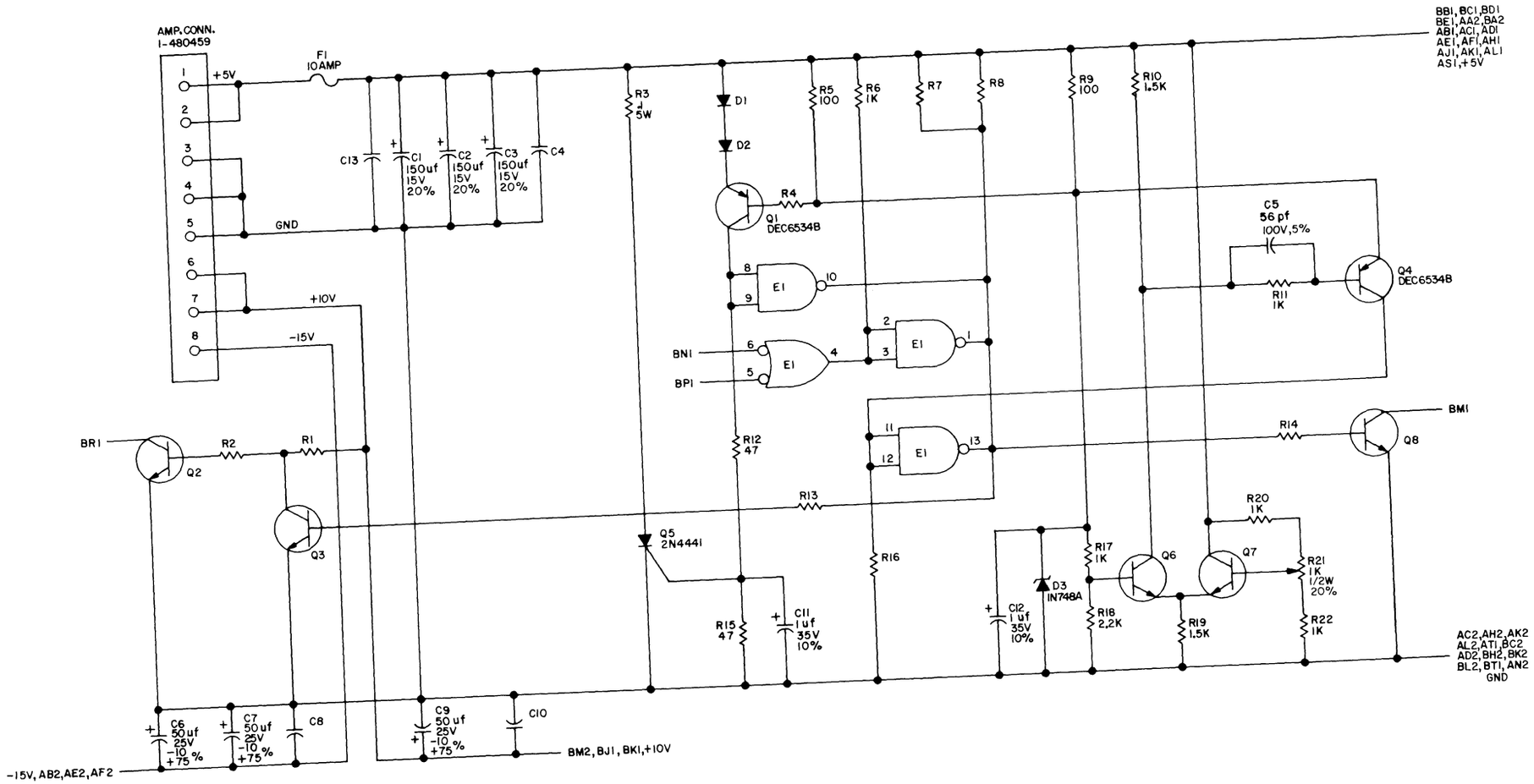
INPUTS: The inputs to the G829 module are +5V, +10V, -15V, and ground. These voltages are supplied by the 721 power supply. The module also receives positive power OK signals from associated power supplies.

OUTPUTS: The outputs of the G829 module are:

a. +5V at 10A (maximum) with the same regulation as the input, +10V at 2.5A (maximum) with the same regulation as the input, and -15V at 3.5A (maximum) with the same regulation as the input;



G829 Simplified Diagram



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 330, 1/4W, 5%
CAPACITORS ARE .01uf, 100V, 20%
DIODES ARE D664
TRANSISTORS ARE DEC3009B
E1 IS DEC7401
PIN 7 ON E1 = GND
PIN 14 ON E1 = +5V

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	IN3606		
IN748A	SAME		
DEC3009B	2N3009B		
DEC6534B	MPS6534		
SAME	2N4441		

REVISIONS			
CHK	CHG NO.	REV.	
SM	00001	A	

DRN. ALLAN RITCEY	DATE 1-16-70	
CHK.	DATE 1-18-70	
ENG.	DATE 2-23-70	
	DATE	

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: POWER CONNECTOR G829

SIZE	CODE	NUMBER	REV.
C	CS	G829-0-1	A

PRINTED CIRCUIT REV.

DIST. 324, 434, 435

DEC FORM NO. DRC 102

G829-F2

G829-2

4

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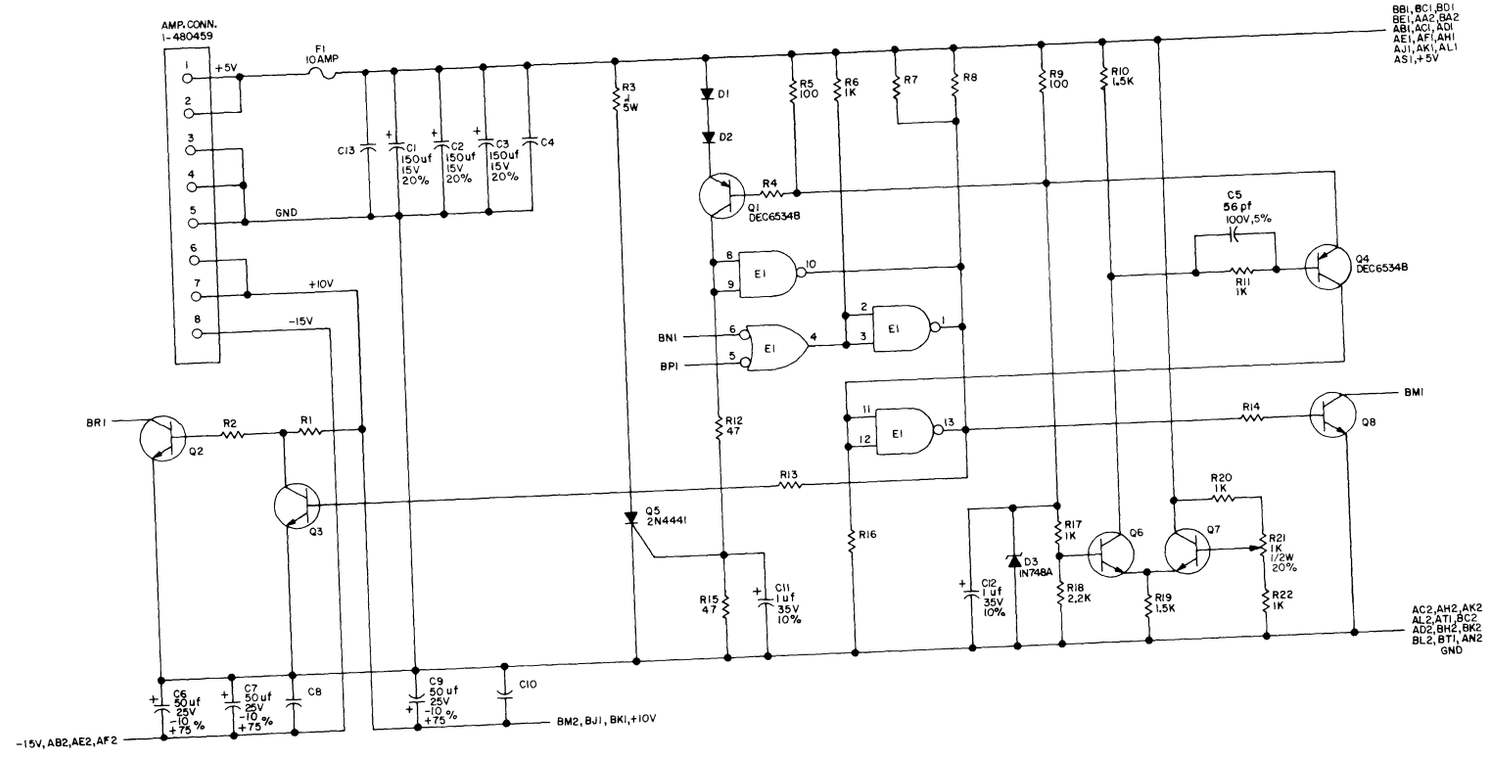


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 330, 1/4W, 5%
CAPACITORS ARE .01uf, 100V, 20%
DIODES ARE D664
TRANSISTORS ARE DEC3009B
E1 IS DEC7401
PIN 7 ON E1 = GND
PIN 14 ON E1 = +5V

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	IN3606		
IN748A	SAME		
DEC3009B	2N3009B		
DEC6534B	MPS6534		
SAME	2N4441		

DRN ALLAN RITCEY DATE 1-16-70
CHK'D DATE 1-16-70
ENG. DATE 2-3-70
PROD. DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: POWER CONNECTOR G829
SIZE C | CODE CS | NUMBER G829-0-1 | REV.
PRINTED CIRCUIT REV. A

REVISIONS | CHK | CHG NO. | REV.

DEC FORM NO. DRC 102

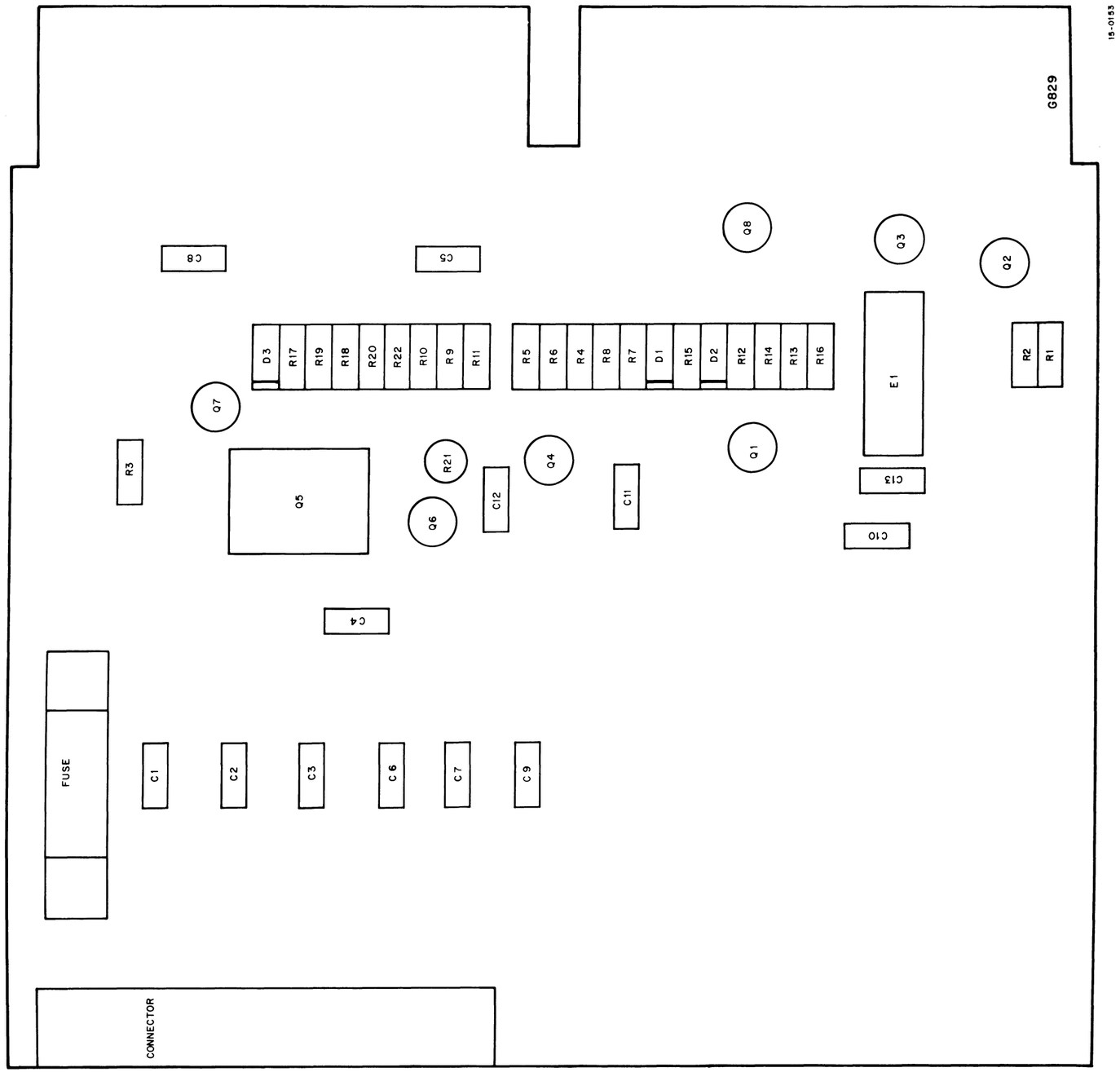
MS662-F2

5

DIST. 324, 434, 435

SIZE C | CODE CS | NUMBER G829-0-1 | REV.

G829-4


G829
15-0153
C8
C5
Q8
Q3
Q2
D3
R17
R19
R18
R20
R22
R10
R9
R11
R5
R6
R4
R8
R7
D1
R15
D2
R12
R14
R13
R16
E1
R2
R1
Q7
R3
Q5
R21
Q6
C12
Q4
C11
Q1
C13
C10
C4
FUSE
C1
C2
C3
C6
C7
C9
CONNECTOR

G858
Teletype Connector

The G858 module contains a level converter, an open-collector driver, and interconnecting wiring. The module is used as a Teletype connector for the PDP-15, serving as the interface between the Teletype receiver/transmitter (M706 and M707) and the Teletype. The converter changes the 0V and +30V levels received from the Teletype to 0V and +3V levels for the receiver/transmitter, and the driver provides the reader run drive current for the Teletype.

The following are the input, output, and power characteristics of the G858 module.

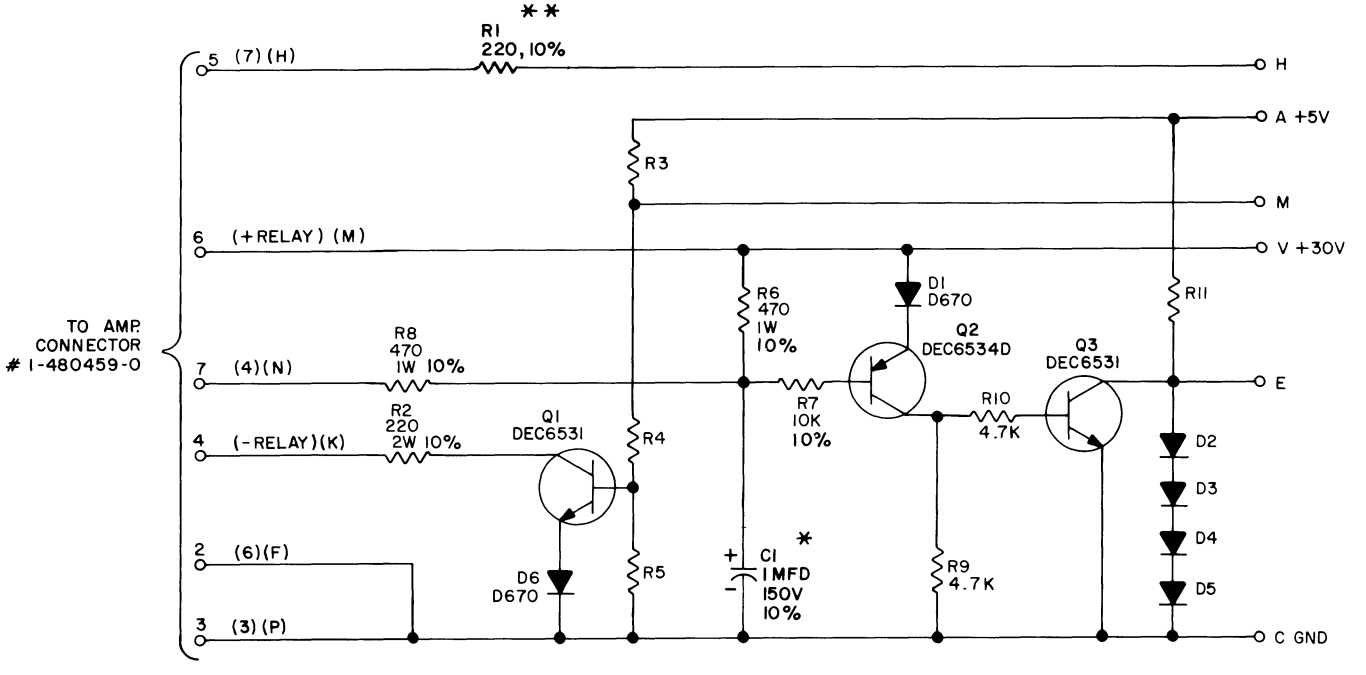
INPUT: Input pin M2 (the reader run in) presents 4 unit loads.

OUTPUT: Output pin E2 (the Teletype keyboard in) is capable of driving 30 unit loads.

POWER: Power dissipated in the G858 module is 5V at 12 mA and 30V at 30 mA.

SIZE	CODE	NUMBER	REV.
B	CS	6858-0-1	C

G858-2



UNLESS OTHERWISE INDICATED:
DIODES ARE D664
RESISTORS ARE 1K, 1/4W, 5%
AMP. CONN. PINS ARE #61320-1
* REMOVE AT 300 BAUD
** REMOVE & INSTALL JUMPER FOR LA30

REVISIONS	CHK	CHG NO	REV.
		00001	B
		2000002	C
		L.HALIO	

DRN. BUTLER	DATE 7/18/69	
CHK'D R.A. Galette	DATE 7/22/69	
ENG. C. Aumann	DATE 9/16/69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606		
D670	IN3653		
DEC6531	NONE		
DEC6534D	MPS6534		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE PDP-15 TELETYPE CONNECTOR G858

SIZE	CODE	NUMBER	REV.
B	CS	G858-0-1	C

PRINTED CIRCUIT REV. A

DEC FORM NO.
DRB 102

5 DIST. 324, 434, 4353 PINK

K303
Timer

The K303 module contains three timers that are triggered by a level change from HIGH to LOW.

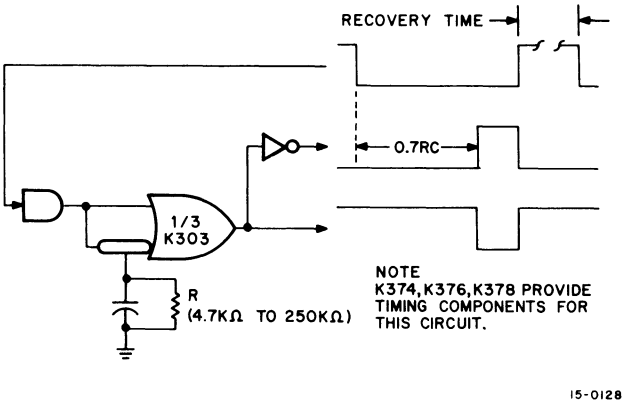
K303 timers provide time delays from 10 μs to 30 sec and can be interconnected to form clocks with periods covering the same intervals. Fixed or adjustable delays and frequencies are obtainable. Calibrated controls are available (K371 through K378) for mounting directly on the K303. Remote controls can also be added, if desired.

When a K303 input gate steps to zero, the uninverted output falls after a controlled interval, while the inverted output rises (see simplified illustration). The interval can be as little as 10 μs or as long as 30 sec, depending on the size of the R and C connected to pin J, P, or V. Recovery begins when the input gate rises to logic 1. A recovery time of at least 0.3 percent of the maximum delay obtainable from the capacitor is required in order to guarantee 95 percent repeat accuracy in the delay.

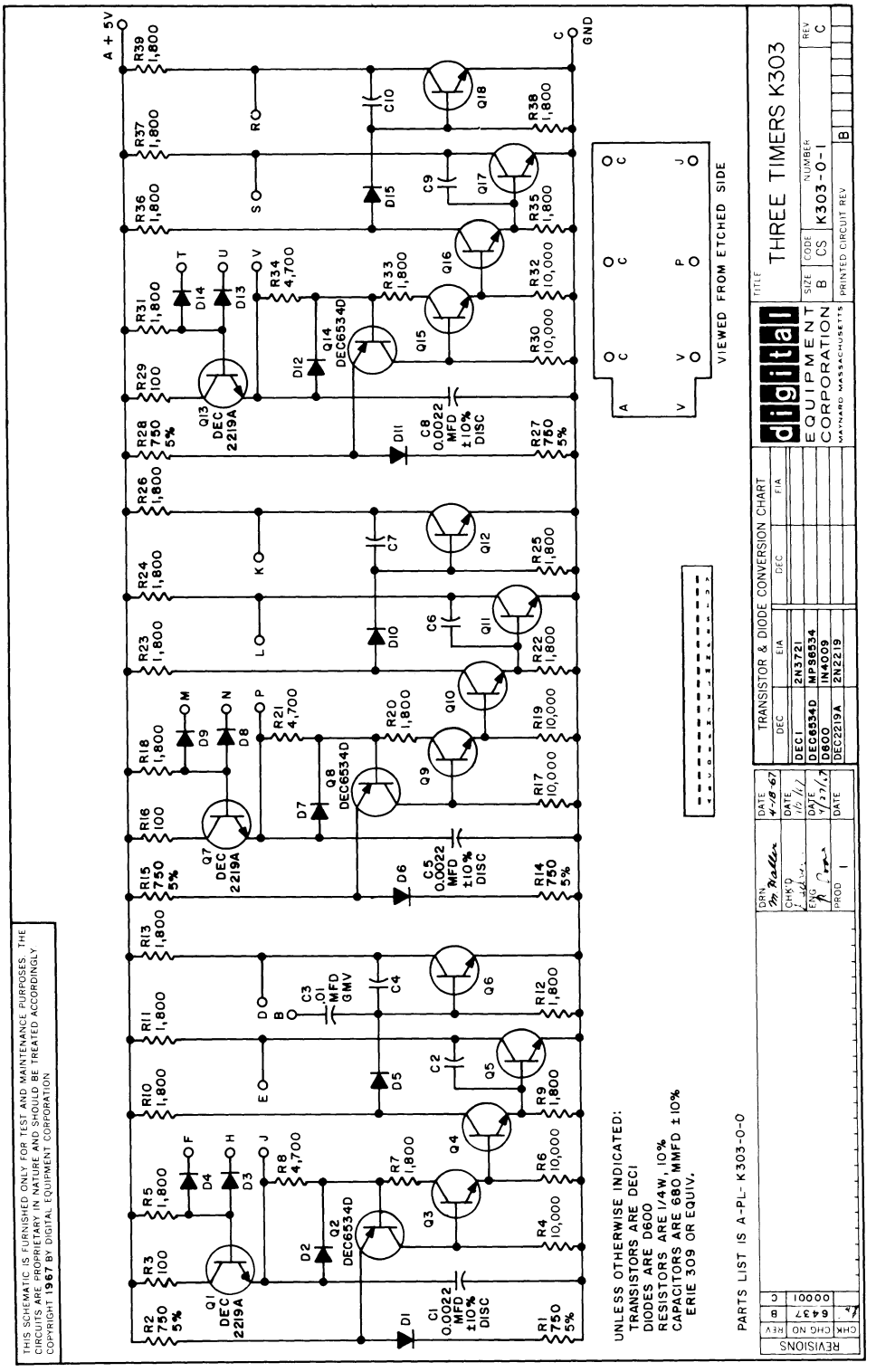
A positive step at the input gate resets the K303 timer outputs. If the step occurs before a timeout is complete, the timeout is terminated and no change appears at the outputs. This property is sometimes convenient for establishing a pulse repetition-rate threshold (frequency setpoint).

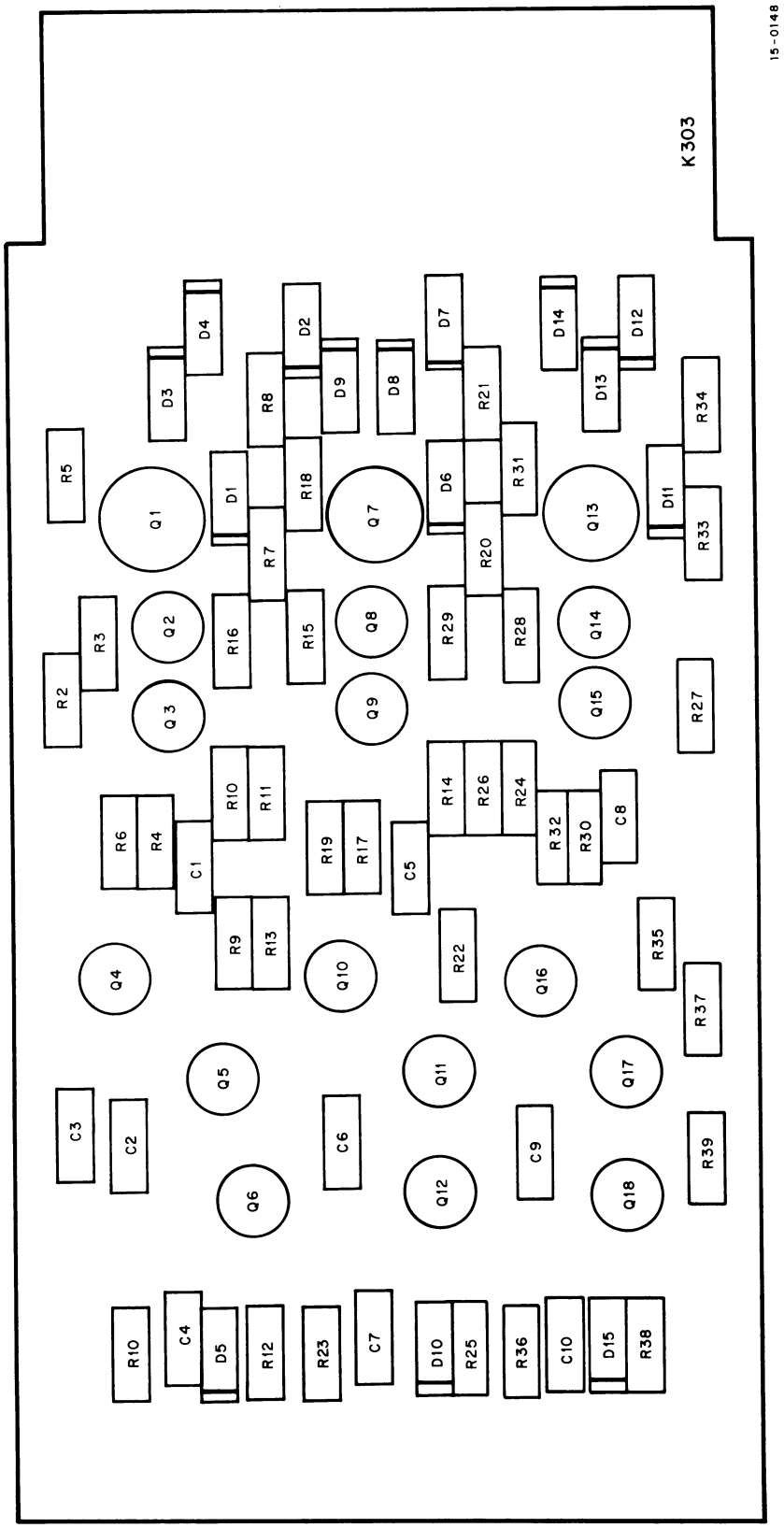
A built-in 2.2 nF timing capacitor assures adequate noise rejection when external capacitors are mounted several inches from the timer. Time threshold for resetting is always several percent of rated recovery time. Thus, noise rejection time increases in proportion to the size of the timing capacitor. If remote rheostats and timing capacitors are used, noise rejection is degraded. If several timing capacitors are to be switch selected, the smallest capacitor is wired near the module; and the other capacitors are switched in parallel with it.

For additional information, refer to DEC's **Digital Logic Handbook**, 1970 edition.



K303 Simplified Diagram

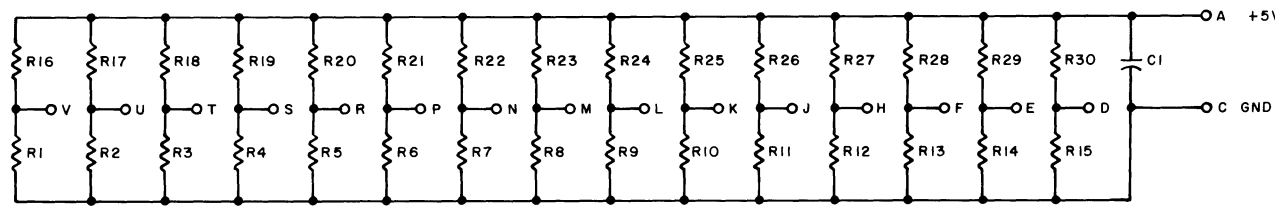

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY
COPYRIGHT 1967 BY DIGITAL EQUIPMENT CORPORATION
A + 5V
GND
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC1
DIODES ARE D600
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE 680 MMFD ±10%
ERIE 309 OR EQUIV.
PARTS LIST IS A-PL- K303-0-0
VIEWED FROM ETCHED SIDE
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
DEC1
2N3721
DEC6534D
NPN6534
D600
IN4009
DEC2219A
2N2219
digital
EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
THREE TIMERS K303
SIZE
B
CODE
CS
NUMBER
K303-0-1
REV
C
PRINTED CIRCUIT REV
B
REVISIONS
DRN
CHK'D
ENG
PROD
DATE


K303
15-0148
R10
C4
D5
R12
R23
C7
D10
R25
R36
C10
D15
R38
C3
C2
Q6
Q5
C6
Q11
Q12
C9
Q17
Q18
R39
Q4
R9
R13
Q10
R22
Q16
R35
R37
R6
R4
C1
R10
R11
R19
R17
C5
R14
R26
R24
R32
R30
C8
R2
R3
Q3
Q2
R16
R15
Q9
Q8
R29
R28
Q15
Q14
R27
R5
Q1
D1
R7
R18
Q7
D6
R20
R31
Q13
D11
R33
R34
D3
D4
R8
D2
D9
D8
D7
R21
D13
D14
D12

M002
Logic 1 Source

The M002 provides 15 outputs at +3V (logic 1) on pins D2 through V2 to hold unused M-series TTL gate inputs HIGH. Up to 10 unused M-series gate inputs can be connected to any one output. If a M002 circuit is driven by a gate, the M002 circuit appears as two TTL unit loads, or 3.2 mA at ground.

Power dissipation of the M002 module is +5V at 16 mA (maximum).



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
C1	CAP. .01MFD 100V 20% DISC	1001610
R1 - R15	RES. 3.3K 1/4W 5% CC	1300439
R16 - R30	RES. 1.8K 1/4W 10% CC	1301428

PARTS LIST

REVISIONS			
CHK	CHG NO.	REV.	

DRN.	M. Walker	DATE 6-21-68
CHK'D	[illegible]	DATE 6/26/68
ENG.	[illegible]	DATE 7/1/68
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: 15 LOADS M002

SIZE	CODE	NUMBER	REV.
B	CS	M002-0-1	

PRINTED CIRCUIT REV. A

M101
Bus Data Interface

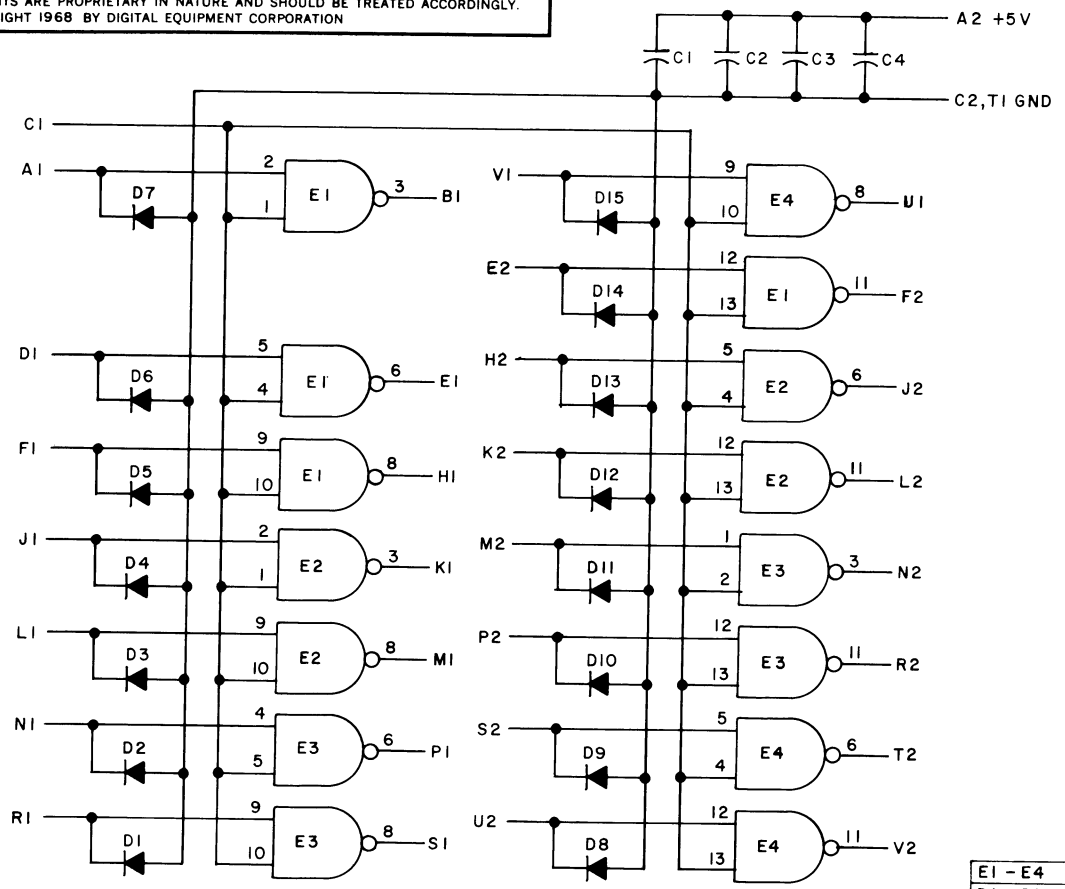
The M101 contains fifteen, two-input NAND gates. One input of each gate is tied to a common line so that all data signals on the second input of each gate can be enabled simultaneously. The M101 can also be used as inverters or a data multiplexer. All data inputs are protected from a negative or more than -0.8V.

INPUTS: Each data signal input presents one TTL unit load. The common line input presents fifteen unit loads.

OUTPUTS: Each output can drive ten unit loads.

POWER: +5V at 82 mA (max.)

SIZE	CODE	NUMBER	REV.
B	CS	M101-0-1	B



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
E1 - E4	INTEGRATED CKT. DEC7400N	1905575
D1 - D15	DIODE D664	1100114
C1 - C4	CAP. .01MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M101-0-0

PARTS LIST

REVISIONS			
CHK	CHG NO.	REV.	
	00001	B	

DRN. M. Waller	DATE 8-5-68	
CHK'D W. Fuller	DATE 8-6-68	
ENG.	DATE	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: BUS DATA INTERFACE M101

SIZE	CODE	NUMBER	REV.
B	CS	M101-0-1	B

PRINTED CIRCUIT REV. A

DEC FORM NO.
DRB 102

4 PINK

DIST. 324 4 5 6 7 8 2

M101-2

M103
Device Selector

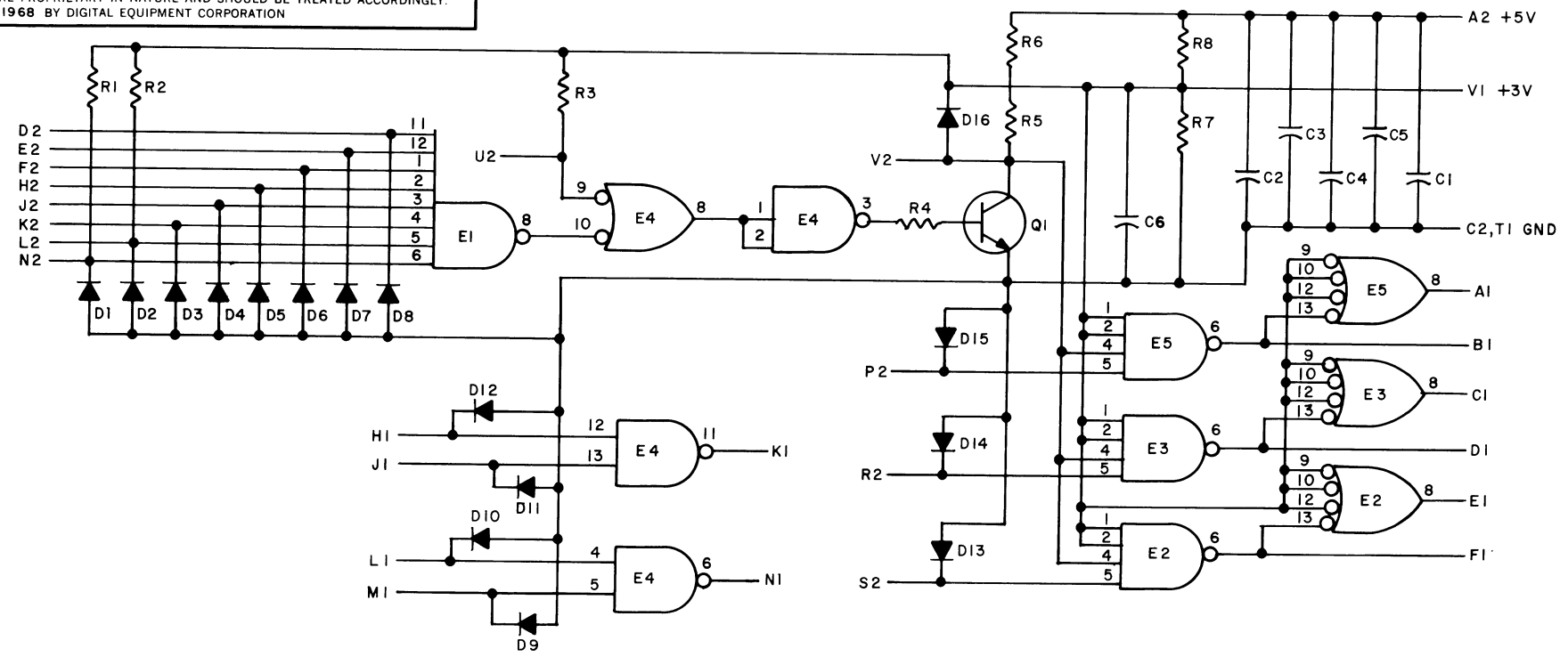
The M103 module is used to decode the six device bits transmitted in complement pairs on a positive bus in a digital system. Selection codes are obtained by selective wiring of the bus signals to the code select inputs; D2, E2, F2, H2, J2, and K2. The M103 module also includes pulse buffering gates for the IOP signals found on the positive bus in digital systems. Two 2-input NAND gates are also provided for any additional buffering that is required.

The following are the input, output, and power characteristics of the M103 module.

INPUTS: All inputs that receive positive bus signals are protected from negative voltage undershoot of more than -0.8V. The following inputs each present one TTL unit load: D2; E2; F2; H2; J2; K2; H1; J1; L1; and M1. Inputs P2, R2, and S2 present 2.5 TTL unit loads. Inputs U2, L2, and N2 each present 1.25 unit loads. These inputs do not need to be tied to a source of logic 1 when they are not in use.

OUTPUTS: Gate outputs K1 and N1 can each drive ten TTL unit loads. Pulse buffering outputs A1, B1, C1, D1, E1, and F1 can each drive 37 TTL unit loads. The Option Select output can drive 16 TTL unit loads.

POWER: The power dissipation of the M103 module is +5V at 110 mA (maximum).



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M103-0-0
Q1	TRANSISTOR DEC3009B-S	1503100
E4	INTEGRATED CKT. DEC7400N	1905575
E2, E3, E5	INTEGRATED CKT. DEC74H40N	1905586
E1	INTEGRATED CKT. DEC7430N	1905578
R8	RES. 330 1/4W 5% CC	1300295
R4-R7	RES. 750 1/4W 5% CC	1301401
R1, R2, R3	RES. 8.2K 1/4W 5% CC	1303179
D1-D16	DIODE D664	1100114
C1-C6	CAP. .01MFD 100V 20% DISC	1001610

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC3009B	2N3009		
D664	IN3606		

REVISIONS	REV.	CHG NO.	CHK
	A	00001	
	C	00002	

DRN. M. Keller	DATE	10-4-68
CHK'D G. Yaeger	DATE	3-12-69
ENG. [illegible]	DATE	11/27/68
PROD.	DATE	

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: DEVICE SELECTOR M103

SIZE	CODE	NUMBER	REV.
B	CS	M103-0-1	C

PRINTED CIRCUIT REV. B

DIST. 324 434 435 PINK

DEC FORM NO. DRB 102

M103-2

M104
I/O Bus Multiplexer

The M104 module has been designed specifically for controllers of PDP-15 peripherals. It is used in all controllers that make use of the API or data channel facilities in the I/O processor. It accepts a request from the controller logic at its FLAG (1) H input and synchronizes this request to the I/O SYNC H pulses issued from the I/O processor. These pulses are fed into SYNC of the M104 and immediately set the REQ flip-flop. The REQ flip-flop can be monitored through pins J2 and U2. The I/O processor responds to a request with a GRANT, and ENA is set. This flip-flop is generally used to gate any address information onto the bus; e.g., the API trap address or the word count address of the multicycle data break. The next SYNC pulse sets ENB.

The REQ flag can be reset through pin F2 (CLR RQ) by the controller logic. Pin N1 should be tied to power clear or its equivalent.

The Enabling level ENABLE IN holds REQ off if ENABLE IN arrives as a negative level. When REQ is set (if ENABLE IN is positive), ENABLE OUT goes negative; and the next peripheral on the bus receives this level as a negative ENABLE IN. In this way, the M104 establishes priorities among devices on the same API level or among devices that use the data channel. See the timing diagram for additional information.

The following are the input, output, and power characteristics of the M104 module.

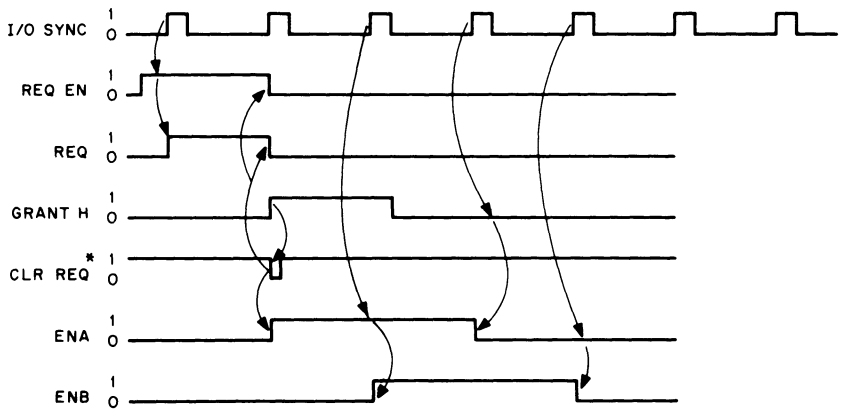
INPUTS: The inputs are standard TTL voltages and have the following input pins and loads:

Input Pin	Load (Units)
H2	2.5
S2	1
H1	6
E2	3
N1	1
F2	1-1/4
K2	68Ω Termination
S2	1

OUTPUTS: The output gates can drive as follows:

Output Pin	Number of Loads Pin Can Drive
U2	5
J2	8
P1	9
S1	10
E1	10
F1	10
M2	PDP-15 I/O Bus Compatible (30 units)
J1	7

POWER: The power dissipation of the M104 module is 1W at 5V.



M104 Timing Diagram

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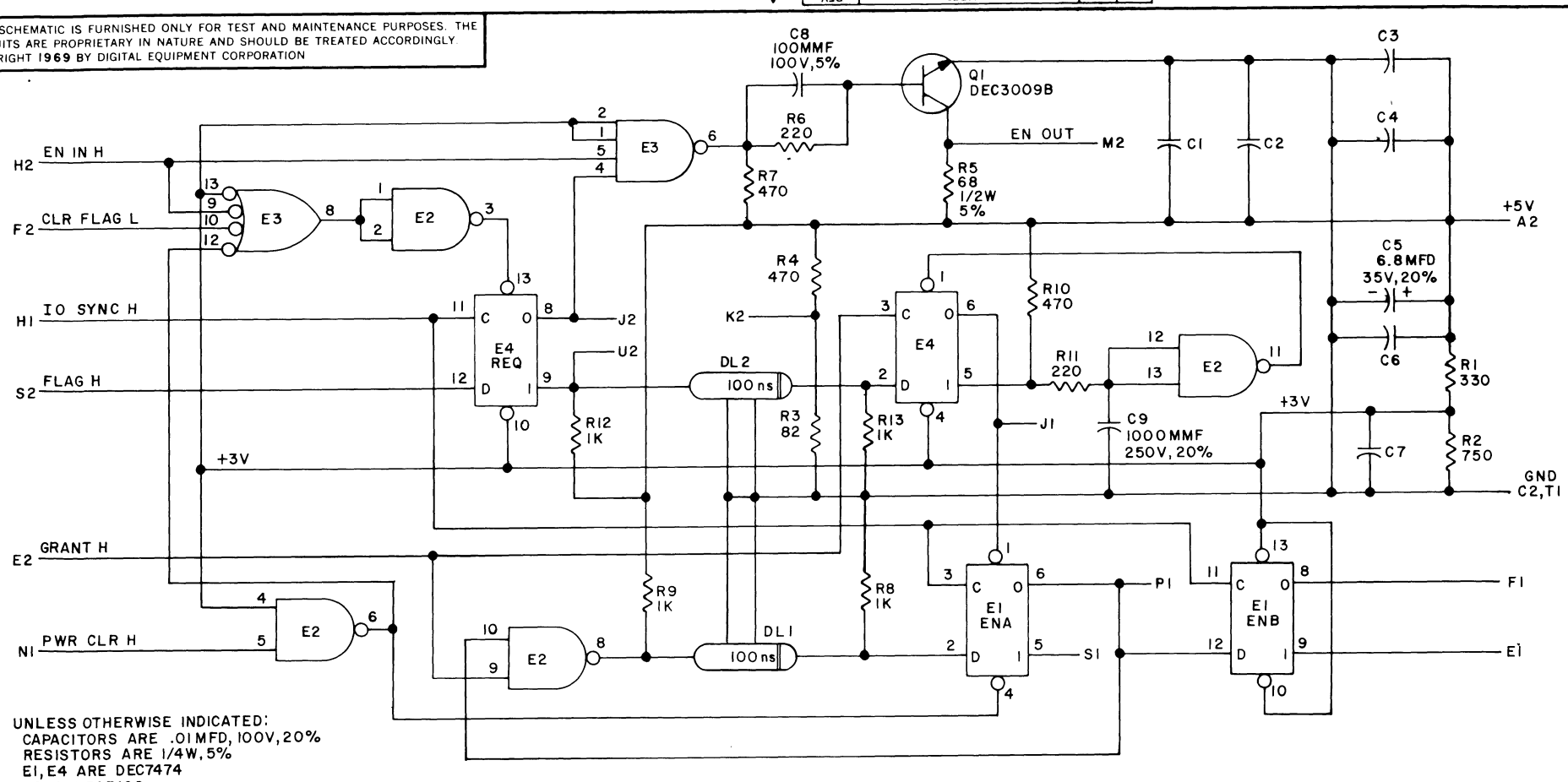


UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD, 100V, 20%
RESISTORS ARE 1/4W, 5%
E1, E4 ARE DEC7474
E2 IS DEC7400
E3 IS DEC74H40
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5 V

REVISIONS	REV.	CHG NO	CHK
	B	00002	REDR.
	C	00003	
	D	00004	
	E	00005	

DRN. R. GUTIERREZ	DATE 3-13-69
CHK'D A. YAUGA	DATE 3-17-69
ENG. J. GODBOUT	DATE 4-7-69
PROD.	DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3009B	2N3009		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE I/O BUS MULTIPLEXER M104

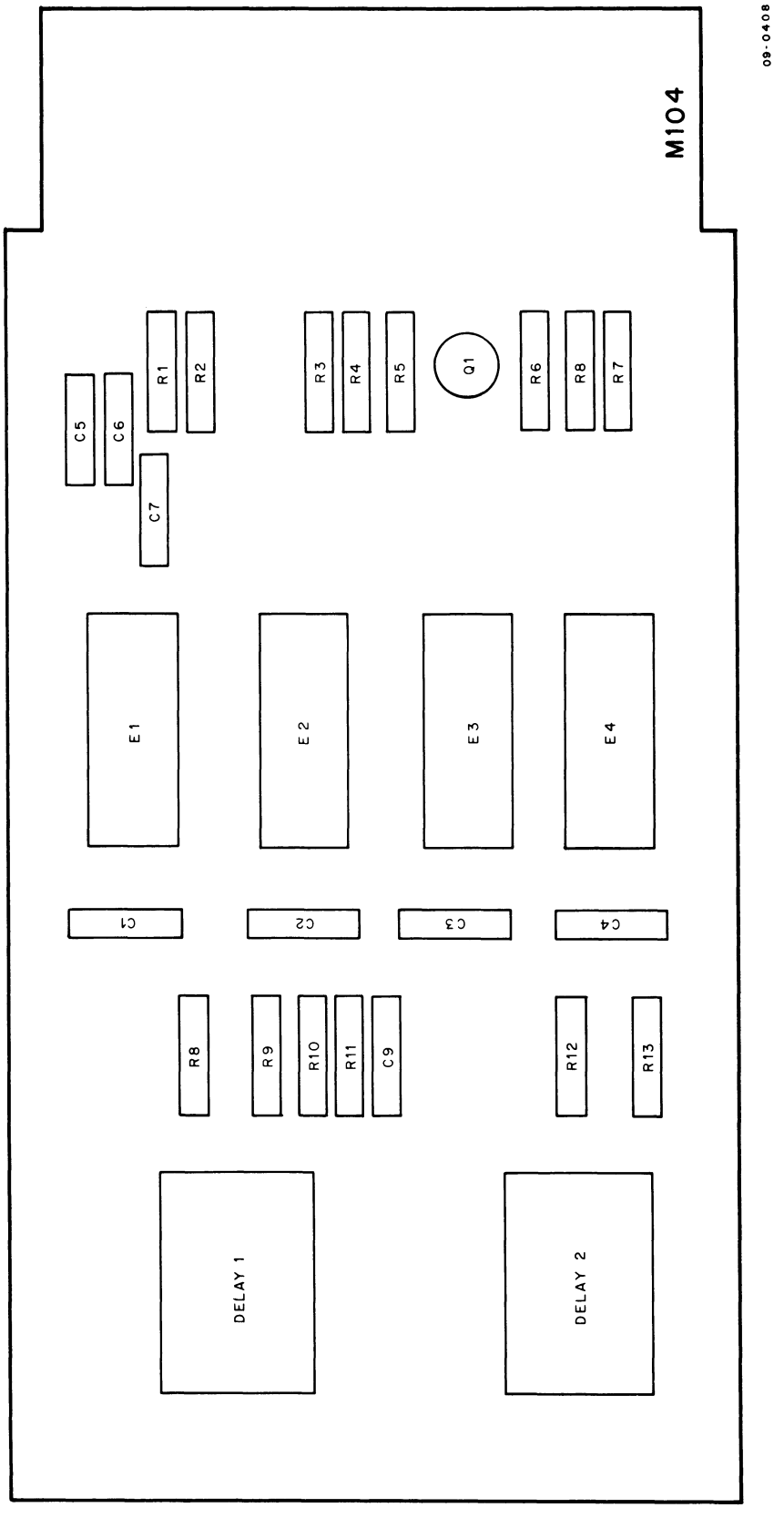
SIZE	CODE	NUMBER	REV.
B	CS	M104-0-1	E

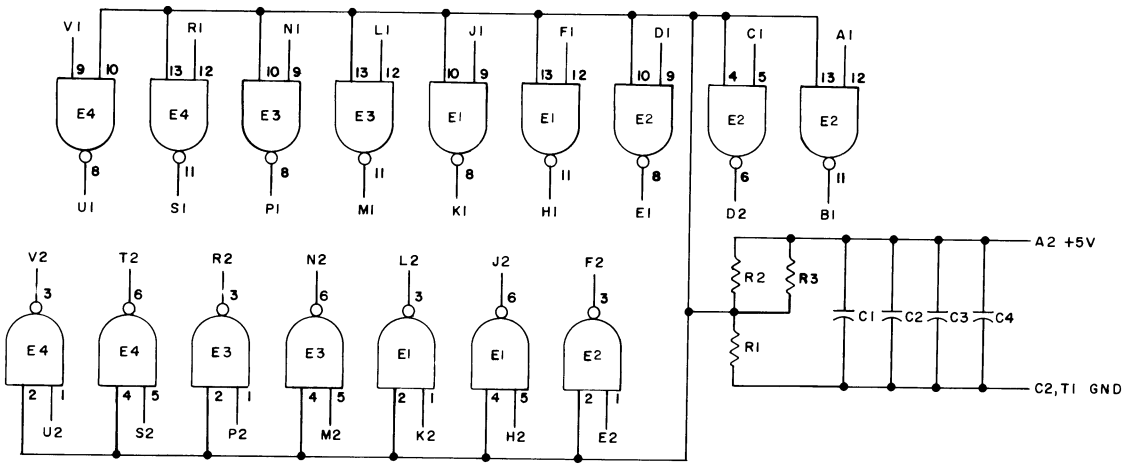
PRINTED CIRCUIT REV. D

DEC FORM NO. DRB 102

4 PINK DIST 1,435

M104-4


M104
09-0408
C5
C6
C7
R1
R2
R3
R4
R5
Q1
R6
R8
R7
E1
E2
E3
E4
C1
C2
C3
C4
R8
R9
R10
R11
C9
R12
R13
DELAY 1
DELAY 2



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
E1-E4	INTEGRATED CKT. DEC7400N	1905575
R1-R3	RES. 750 1/4W 5% CC	1301401
C1-C4	CAP. .01MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M111-0-0

PARTS LIST

REVISIONS			
REV	CHG NO.	CHK	
A	00001		

DRN. M. Keller	DATE 5-31-68	
CHK'D	DATE	
ENG.	DATE	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: INVERTER M111

SIZE	CODE	NUMBER	REV
B	CS	M111-0-1	A

PRINTED CIRCUIT REV C

M112
NOR Gates

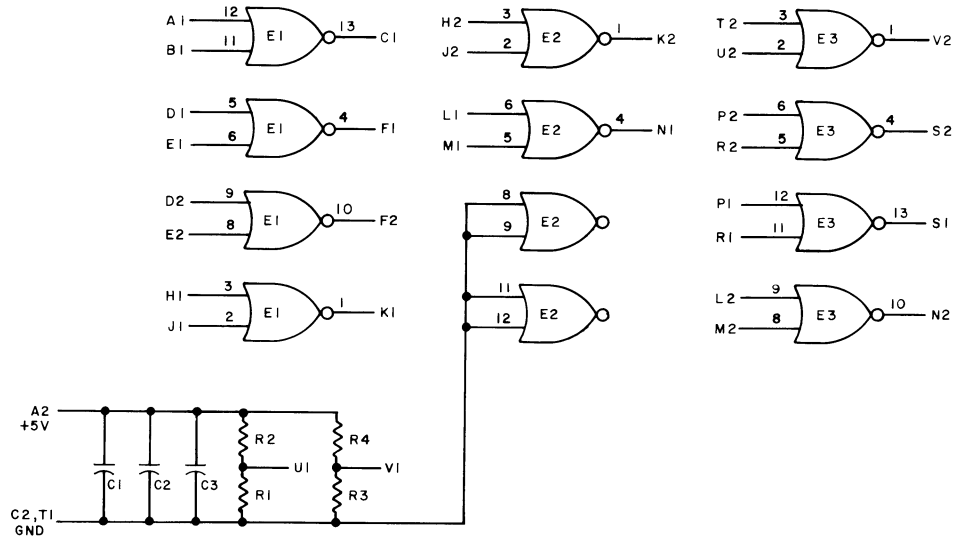
The M112 module contains ten 2-input NOR gates, each performing the function NOT (A + B). Pins U1 and V1 provide +3V, and each are capable of holding HIGH (logic 1) up to 40 unused M-series inputs. Propagation delay is 22 ns (maximum).

The following are the input, output, and power characteristics of the M112 module.

INPUT: Each input presents one unit load.

OUTPUT: Each output can drive up to ten unit loads.

POWER: The power dissipated in the M112 module is +5V at 50 mA (maximum).



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
C1,C2,C3	CAP. .01MFD 100V 20% DISC	1001610
E1,E2,E3	INTEGRATED CKT. DEC7402N	1909004
R2,R4	RES. 330 1/4W 5% CC	1300295
R1,R3	RES. 750 1/4W 5% CC	1301401
	PARTS LIST	A-PL-M112-0-0

PARTS LIST

REVISIONS	CHK	CHG NO	REV
	MM	00001	A
	[illegible]	00002	C
	MC	00003	D

DRN	M Waller	DATE 2-20-68
CHK'D	[illegible]	DATE 2/20
ENG	J Rovatti	DATE 3/7/68
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: NOR GATE M112

SIZE	CODE	NUMBER	REV.
B	CS	M112-0-1	D

PRINTED CIRCUIT REV. D

M112-2

M113, M115, M117, M119
NAND Gates

The M113, M115, M117, and M119 modules provide general purpose gating for the M-series. They are most commonly used for decoding, comparison, and control. Each module performs the NAND function NOT (A • B - - - - - - - - N), depending upon the number of inputs.

The modules and their descriptions are as follows:

M113 - Ten 2-input NAND gates that also can be used as inverters;

M115 - Eight 3-input NAND gates;

M117 - Six 4-input NAND gates;

M119 - Three 8-input NAND gates.

Unused inputs on any gate must be returned to a source of logic 1 for maximum noise immunity. In the M113, M117, M119, M121, M617, and M627 modules, two pins (U1 and V1) are provided as a source of +3V for noise immunity. Each pin can supply up to 40 unit loads. Modules M103, M111, and M002 provide additional sources of logic 1 level. Typical propagation delay of these gates is 15 ns, and maximum propagation delay is 22 ns.

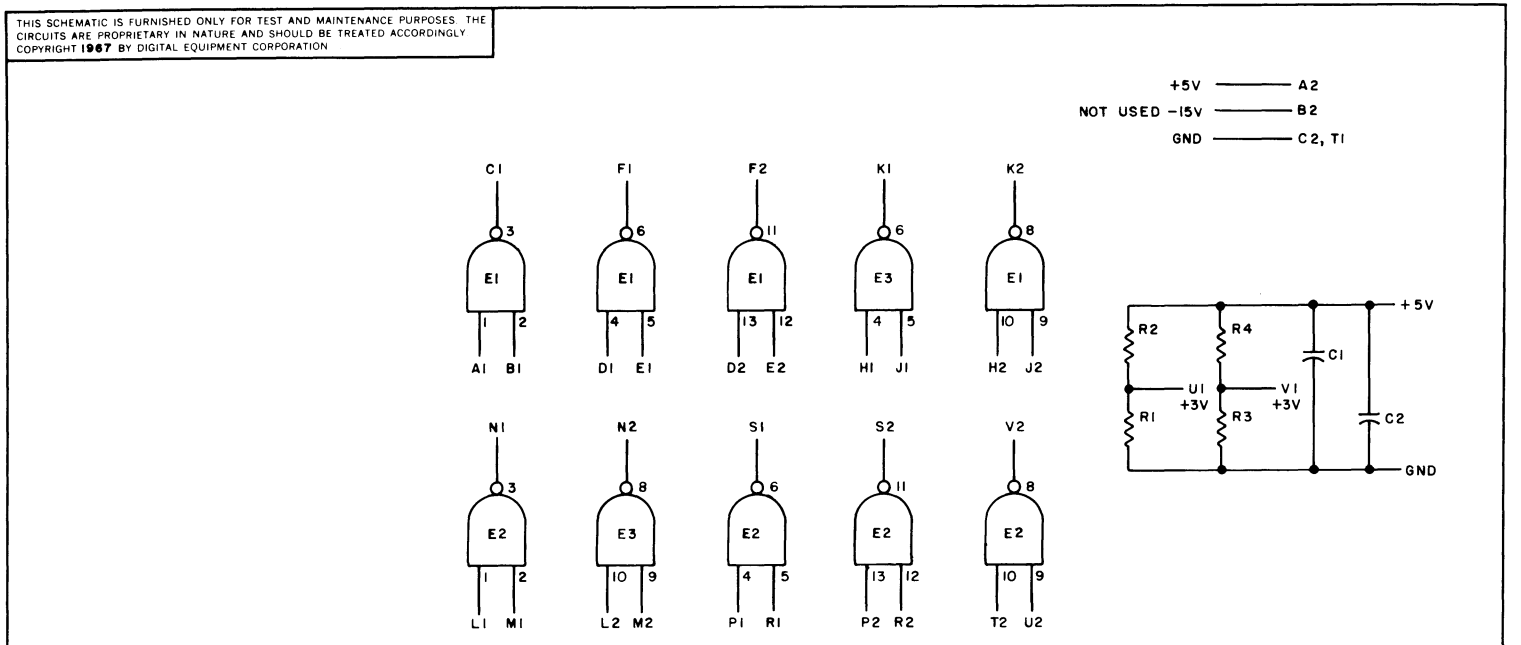
The following are the input, output, and power characteristics of these modules.

INPUTS: Each input presents one unit load.

OUTPUTS: Each output is capable of supplying 10 unit loads.

POWER: Power dissipation for the respective modules is:

M113: 71 mA
M115: 41 mA
M117: 41 mA
M119: 9 mA
} +maximum current at 5V



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M113-0-0
C1 AND C2	CAP. .01MFD 100V 20% DISC	1001610
R2 AND R4	RES. 330 1/4W 10% CC	1300293
R1 AND R3	RES. 750 1/4W 5% CC	1301401
E1 THRU E3	INTEGRATED CKT. DEC7400N	1905575

PARTS LIST

REVISIONS			
CHK	CHG NO	REV	
	8425	A	
	6801	B	
	10001	C	

DRN	M. Waller	DATE 3-15-67
CHK'D		DATE 4-21-67
ENG	J. White	DATE 4-21-67
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

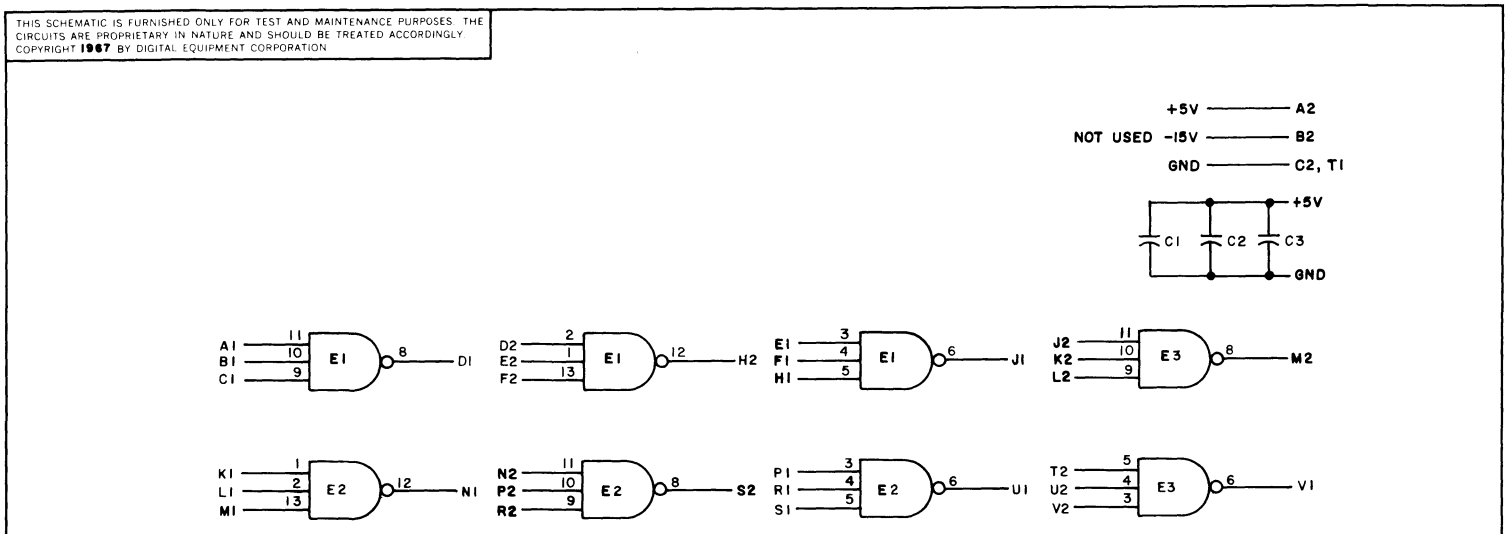
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE: 10-2 INPUT NAND GATES M113

SIZE	CODE	NUMBER	REV
B	CS	M113-0-1	C

PRINTED CIRCUIT REV: D



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
E1 THRU E3	INTEGRATED CKT. DEC7410N	1905576
C1 THRU C3	CAP. .01MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M115-0-0

PARTS LIST

REVISIONS	CHK	CHG NO	REV
		8423	A
		6800	B
	MM	00001	C

DRN	M. Waller	DATE 4-20-67
CHK'D		DATE
ENG	L. Mikuta	DATE 4/21/67
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

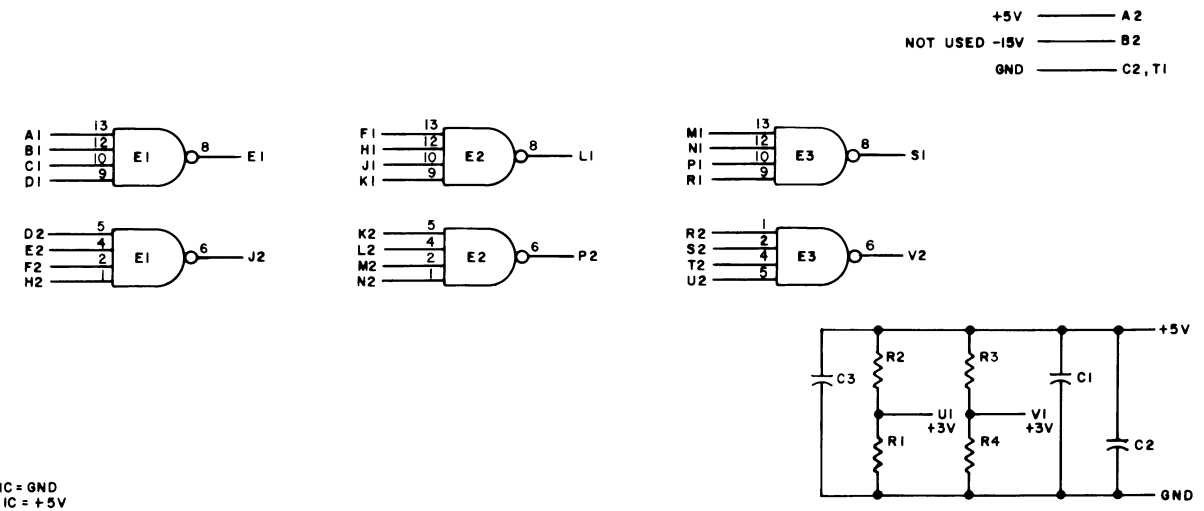
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: 8-3 INPUT NAND GATES M115

SIZE	CODE	NUMBER	REV
B	CS	M115-0-1	C

PRINTED CIRCUIT REV D



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
E1 THRU E3	INTEGRATED CKT. DEC7420N	1905577
R1 & R4	RES. 750 1/4W 5% CC	1301401
R2 & R3	RES. 330 1/4W 10% CC	1300293
C1 THRU C3	CAP. .01MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M117-0-0

PARTS LIST

REVISIONS	CHK	CHG NO	REV
		6424	A
		6799	B
	MH	00001	C
		00002	E

DRN	M. Waller	DATE 3-15-67
CHK'D		DATE 4-21-67
ENG	E. White	DATE 4-21-67
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

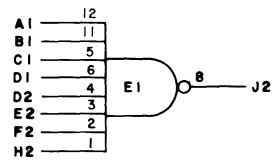
DEC	EIA	DEC	EIA

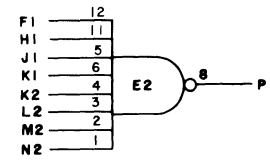
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

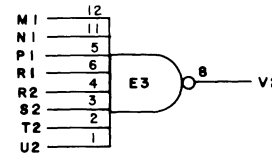
TITLE: 6-4 INPUT NAND GATES M117

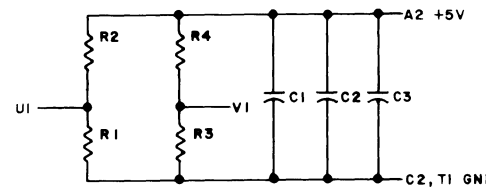
SIZE	CODE	NUMBER	REV
B	CS	M117-0-1	E

PRINTED CIRCUIT REV E









NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
C1 THRU C3	CAP. .01MFD 100V 20% DISC	1001610
R1 & R3	RES. 750 1/4W 5% CC	1301401
R2 & R4	RES. 330 1/4W 10% CC	1300293
E1 THRU E3	INTEGRATED CKT. DEC7430N	1905578

PARTS LIST A-PL-M119-0-0

REVISIONS			
REV.	CHG NO	CHK	
A	6804	[illegible]	M11
B	00001		

DRN. M. Walker	DATE 8-1-67	
CHK'D [signature]	DATE 8/4/67	
ENG [signature]	DATE 8/11/67	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 3-8 INPUT NAND-GATES M119

SIZE	CODE	NUMBER	REV.
B	CS	M119-0-1	B

PRINTED CIRCUIT REV. C

M121
AND/NOR Gates

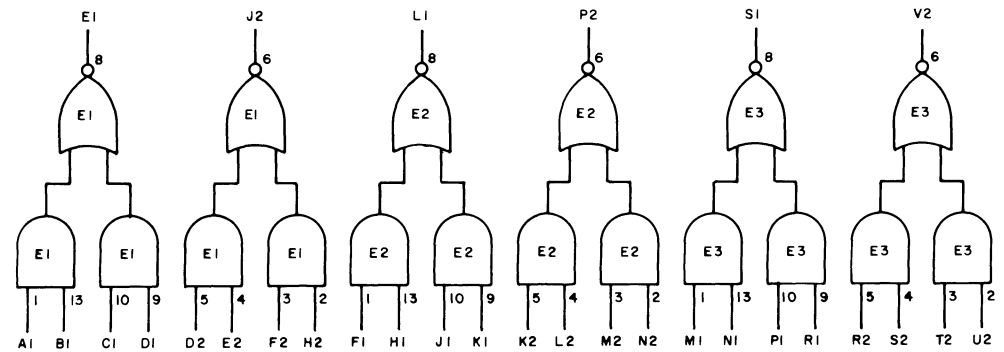
The M121 module contains six AND/NOR gates that perform the function NOT (AB + DC). The exclusive OR, coincidence, and NOR functions can be performed by proper connection of signals to the AND inputs. Maximum propagation delay of an M121 gate is 22 ns.

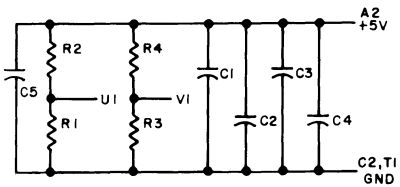
The following are the input, output, and power characteristics of the M121 module.

INPUTS: Each input presents one unit load to the driving module.

OUTPUTS: Each output is capable of driving up to 10 unit loads.

POWER: Power dissipation of the M121 module is +5V at 50 mA (maximum).





NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M121-0-0
C1 THRU C5	CAP, .01 MFD 100V 20% DISC	1001610
R2 & R4	RES, 330 1/4W 10% CC	1300293
R1 & R3	RES, 750 1/4W 5% CC	1301401
E1 THRU E3	INTEGRATED CKT. DEC7450N	1905580

PARTS LIST

REVISIONS			
CHK	CHG NO	REV	
	6802	A	
	100001	B	
	100002	C	

DRN	M. Waller	DATE 4-21-67
CHK'D		DATE 4-21-67
ENG	J. White	DATE 4-21-67
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: AND-NOR GATE M121

SIZE	CODE	NUMBER	REV
B	CS	M121-0-1	C

PRINTED CIRCUIT REV D

M127
AND/NOR Gates

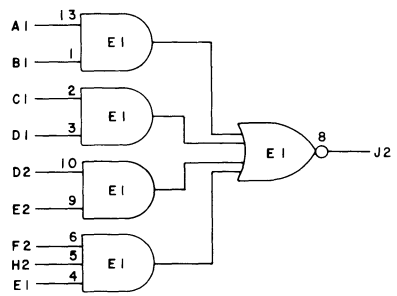
The M127 module contains three general purpose AND/NOR gates that perform functions similar to the M121 module. By connecting signals to the AND inputs, these gates can be used to select and to place on a single output any of several input signals. Propagation delay of an M127 gate is 11 ns (maximum).

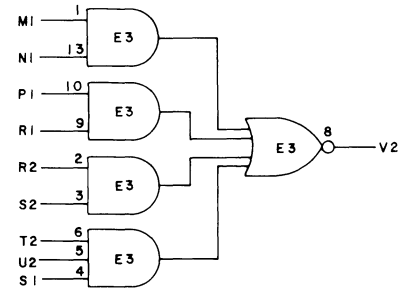
The following are the input, output, and power characteristics of the M127 module.

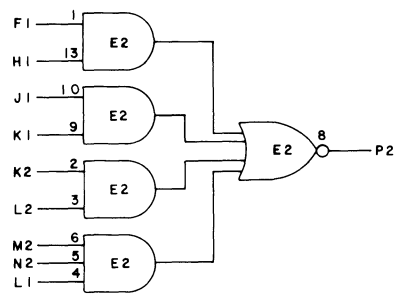
INPUTS: Each input presents 1.25 unit loads.

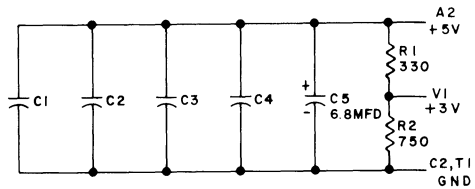
OUTPUTS: Each output is capable of driving 12.5 unit loads.

POWER: Power dissipation of the M127 module is 5V at 100 mA (maximum).









UNLESS OTHERWISE INDICATED
CAPACITORS ARE .01MFD
RESISTORS ARE 1/4W 5%
IC'S ARE DEC 74H53
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = GND

REVISIONS

CHK	CHG NO	REV

DRN.		DATE 3-14-69
CHK'D.		DATE 3-17-69
ENG.		DATE 4-9-69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 2-2-2-3 AND / NOR GATE M127

SIZE	CODE	NUMBER	REV.
B	CS	M127-0-1	

PRINTED CIRCUIT REV. A

M129
AND/NOR Gates

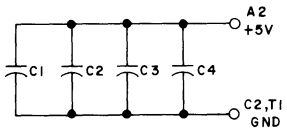
The M129 module contains four general purpose AND/NOR gates that perform functions similar to the M121 module. By connecting signals to the AND inputs, these gates can be used to select and to place on a single output any of several input signals. Propagation delay of an M129 gate is 11 ns (maximum).

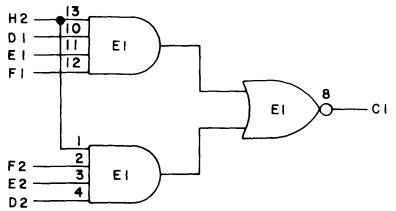
The following are the input, output, and power characteristics of the M129 module.

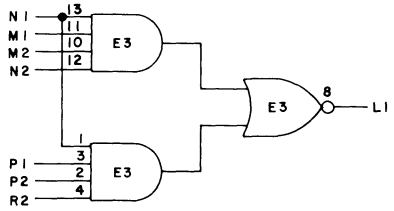
INPUTS: Inputs H2, L2, N1, and V2 present 2.5 unit loads, and the remaining inputs present 1.25 unit loads.

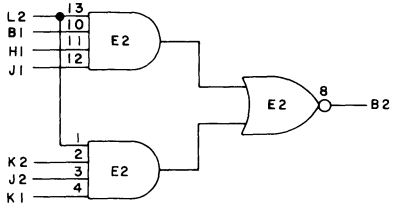
OUTPUTS: Each output is capable of driving 12.5 unit loads.

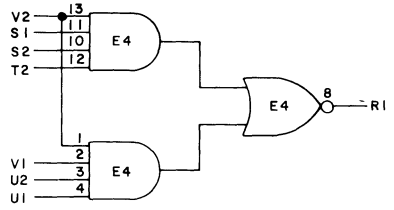
POWER: Power dissipation of the M129 module is 5V at 50 mA (maximum).











UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD
IC'S ARE DEC 74H55N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REVISIONS

CHK	CHG NO	REV

DRN		DATE 2-20-69
CHK'D		DATE 3.3.69
ENG		DATE 9.7.69
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: AND/OR INVERT GATE M129

SIZE	CODE	NUMBER	REV
B	CS	M129-0-1	

PRINTED CIRCUIT REV A

M129-2

M133
NAND Gates

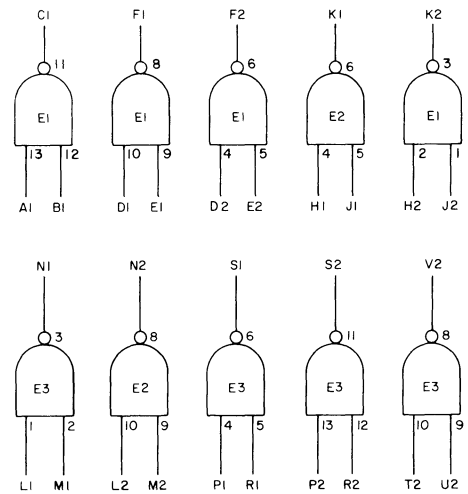
The M133 module contains ten 2-input NAND gates, each performing the function NOT (A·B). The module is used for general purpose high-speed gating. Maximum output propagation delay to a logic 1 or 0 is 10 ns. The high-speed characteristic of these gates frequently solves tight timing problems in complex systems. Unused inputs on any gate must be returned to a source of logic 1 for maximum speed and noise immunity.

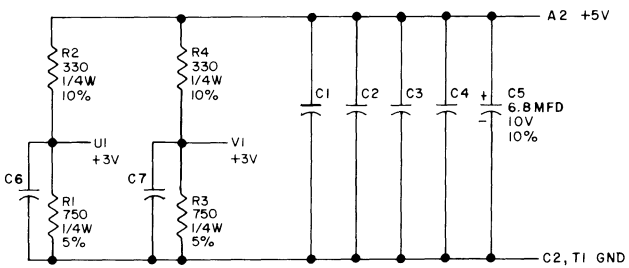
The following are the input, output, and power characteristics of the M133 module.

INPUTS: Each input presents 1.25 unit loads.

OUTPUTS: Each output is capable of driving 12.5 unit loads.

POWER: Power dissipated in the M133 module is +5V at 130 mA (maximum).





UNLESS OTHERWISE INDICATED:
E1 - E3 ARE DEC74H00N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
CAPACITORS ARE .01 MFD, 100V, 20%

REVISIONS			
CHK	CHG NO	REV	
J.J.	00001	A	

DRN. M. HALLER	DATE 8-8-68	
CHK'D W. MULLEN	DATE 8-9-68	
ENG. D. O'CONNOR	DATE 10-25-68	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: 10-2 INPUT NAND GATES M133

SIZE	CODE	NUMBER	REV
B	CS	M133-0-1	A

PRINTED CIRCUIT REV. B

M135
NAND Gates

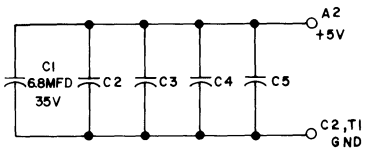
The M135 module contains eight high-speed 3-input NAND gates that perform the function NOT (A•B•C). These gates are most commonly used for decoding, comparison, and control. Unused inputs on any gate must be returned to a source of logic 1 for maximum speed and immunity. Propagation delay of an M135 gate is 10 ns (maximum).

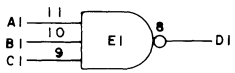
The following are the input, output, and power characteristics of the M135 module.

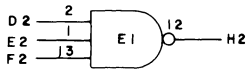
INPUTS: Each input presents 1.25 unit loads.

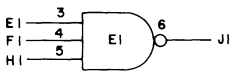
OUTPUTS: Each output is capable of driving 12.5 unit loads.

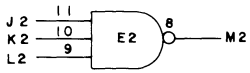
POWER: Power dissipated in the M135 module is 5V at 90 mA (maximum).

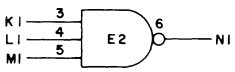


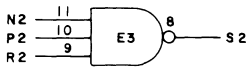




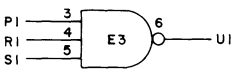


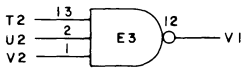






UNLESS OTHERWISE INDICATED
IC'S ARE DEC74H10
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
CAPACITORS ARE .01 MFD 50V





REVISIONS			
CHK	CHG NO	REV	

DRN		DATE 3-3-69
CHKD		DATE 3.3.69
ENG	DEO	DATE 3-7-69
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE 3 INPUT NAND GATE M135

SIZE	CODE	NUMBER	REV
B	CS	M135-0-1	

PRINTED CIRCUIT REV A

M135-2

M139
NAND Gates

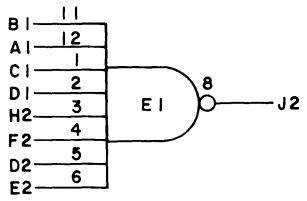
The M139 module contains three high-speed 8-input NAND gates that perform the NAND function NOT (A·B . . . N), depending on the number of inputs. These gates are most commonly used for decoding, comparison, and control. Unused inputs on any gate must be returned to a source of logic 1 for maximum speed and noise immunity. Propagation delay of an M139 gate is 10 ns (maximum).

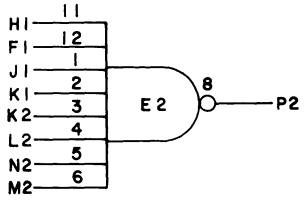
The following are the input, output, and power characteristics of the M139 module.

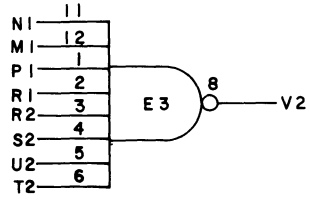
INPUTS: Each input presents 1.25 unit loads.

OUTPUTS: Each output is capable of driving 12.5 unit loads.

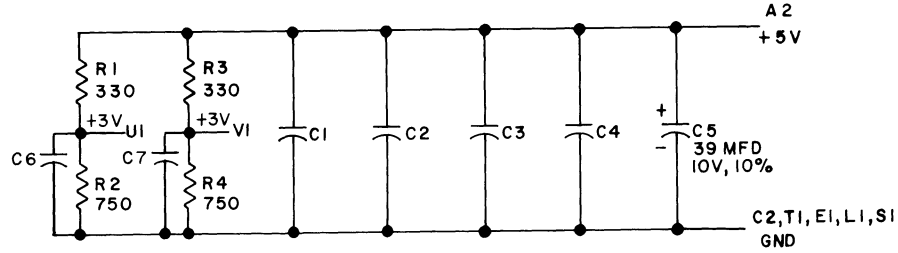
POWER: Power dissipated in the M139 module is 5V at 40 mA (maximum).







UNLESS OTHERWISE INDICATED:
IC'S ARE DEC1074H30
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
CAPACITORS ARE .01 MFD, 100V, 20%
RESISTORS ARE 1/4W, 5%



REVISIONS	REV.	CHG NO	CHK
	B	00001	PF
	C	00002	
	D	00003	

DRN.		DATE 3-8-69
CHK'D	A. Yanega	DATE 3-8-69
ENG.	NEO Cronin	DATE 4-7-69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: 3-8 INPUT NAND GATE M139

SIZE	CODE	NUMBER	REV.
B	CS	M139-0-1	D.

PRINTED CIRCUIT REV. B

DEC FORM NO. DRB 102

DIST. 324, 434, 435²

PINK

M149
NAND Wired OR Matrix

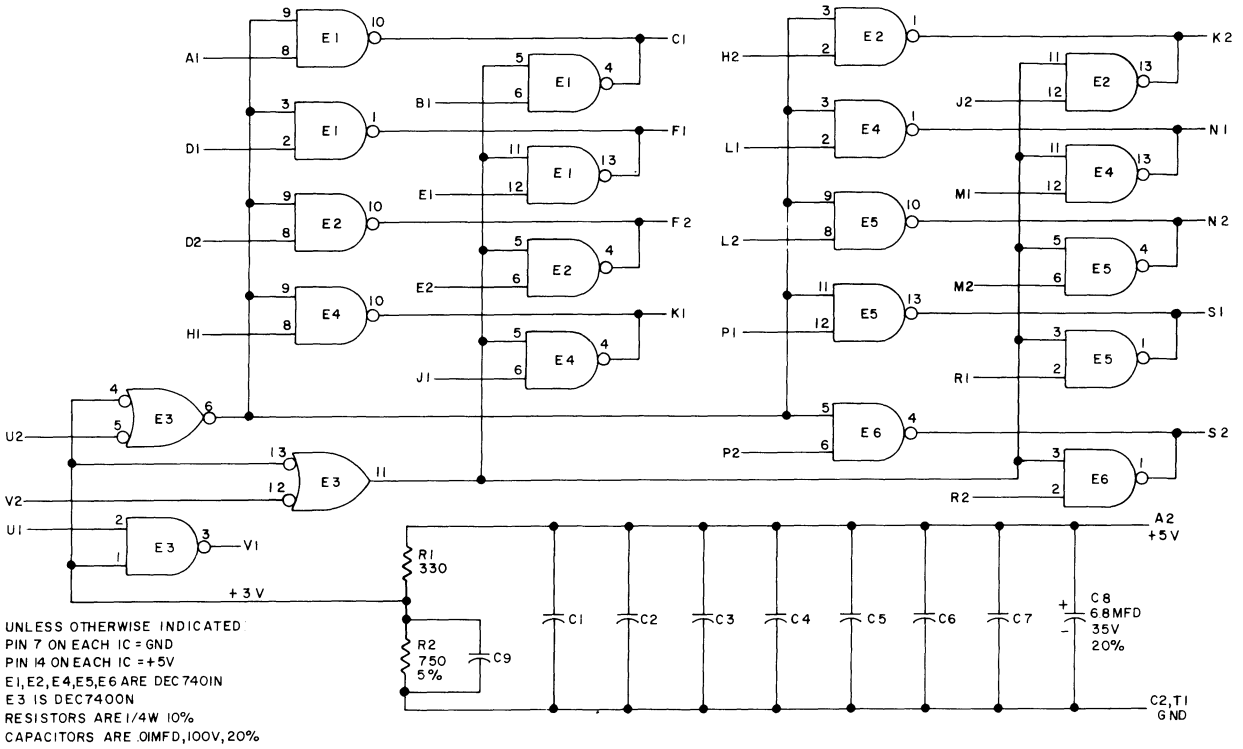
The M149 module contains two sets of nine open-collector NAND gates. The NAND gates are OR wired together onto nine output pins having the standard TTL output levels. Each set of NAND gates is connected to operate in conjunction with a separate enable gate. The M149 module is used to gate desired signals onto an open-collector bus. (Refer to Engineering Drawings D-BS-KP15-0-38 through D-BS-KP15-0-43, and D-BS-KP15-0-60 through D-BS-KP15-0-62).

The following are the input, output, and power characteristics of the M149 module.

INPUTS: Each input presents 1 unit load.

OUTPUTS: Gate outputs are all open-collector and can sink 16 mA (maximum). The pulse amplifier output is capable of driving 10 unit loads.

POWER: Power dissipation of the M149 module is 5V at 130 mA (maximum).



UNLESS OTHERWISE INDICATED
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E2, E4, E5, E6 ARE DEC 7401N
E3 IS DEC 7400N
RESISTORS ARE 1/4W 10%
CAPACITORS ARE .01MFD, 100V, 20%

REVISIONS			
CHK	CHG NO	REV	
	00001	B	

DRN		DATE 3-26-69
CHK'D	G Young	DATE 3-26-69
ENG		DATE 4/23/69
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE 9X2 NAND WIRED OR MATRIX M149

SIZE	CODE	NUMBER	REV
B	CS	M149-0-1	B

PRINTED CIRCUIT REV. C

M159
4-Bit Arithmetic Logic Unit

The M159 4-Bit Arithmetic Logic Unit (ALU) module contains a single DEC74181 integrated circuit. Nine of these ALU modules are used in the FP15 Floating-Point Processor to perform 36-bit arithmetic and logic operations, as shown on D-BS-FP15-0-19 through -28 of the FP15 drawings.

The integrated circuit is capable of performing 16 4-bit arithmetic operations when the MODE control and CN inputs are low and 16 logic functions when the MODE control input is high. The functions are selected by applying combinations of function select inputs S0 through S3. For FP15 applications, the function select and MODE control inputs are generated by the adder control logic shown on D-BS-FP15-0-33 of the FP15 drawings.

Only two arithmetic operations, A plus B and A minus B minus 1, are selected. Five logic functions, A, -A, B, -B, and logical 0, are performed. The combined ALU truth table for FP15 arithmetic operations and logic functions is listed as follows:

MODE Control	Function Select Inputs				Output Function
	S3	S2	S1	S0	
0	1	0	0	1	A plus B (arithmetic operation)
0	0	1	1	0	A minus B minus 1 (arithmetic operation)
0	0	0	0	0	A (logic function)
1	0	0	0	0	-A (logic function)
1	1	0	1	0	B (logic function)
1	0	1	0	1	-B (logic function)
1	0	0	1	1	Logical 0 (logic function)

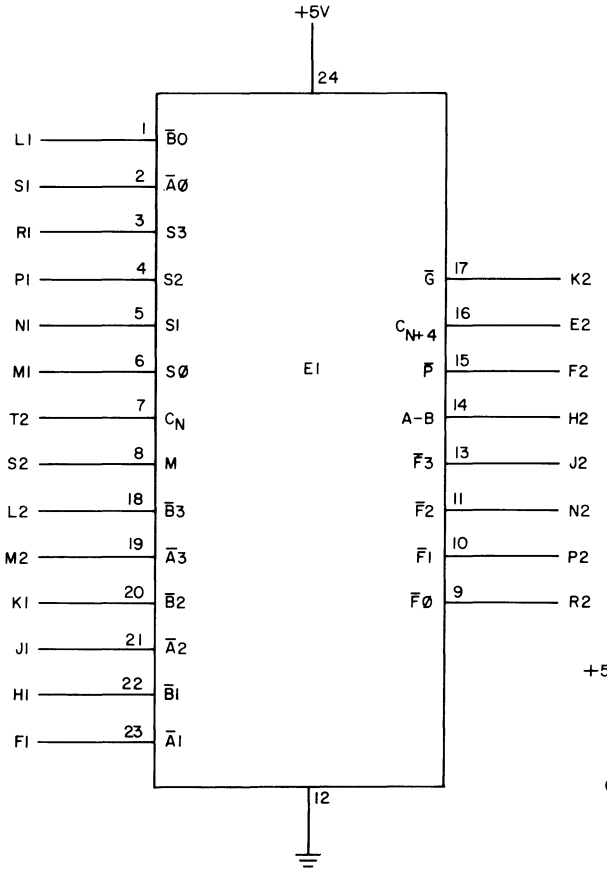
In addition, a comparator output, A=B, is provided when the four A inputs are equal to the four B inputs. A full carry look ahead capability is provided for fast, simultaneous carry generation.

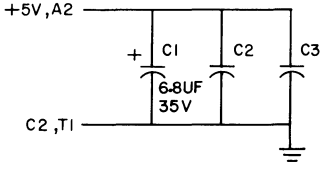
INPUTS: Each input presents 1 unit load.

OUTPUTS: All outputs are capable of driving 10 unit loads.

POWER:

SIZE	CODE	NUMBER	REV.
B	CS	M159-0-1	





UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01 UF, 100V, 20%
IC IS A DEC74181

REVISIONS	REV.	CHG NO	CHK

DRN	B. Wyatt	DATE	10-28-70
CHK	[illegible]	DATE	11-3-70
ENG	[illegible]	DATE	11/10/70
PROD.		DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: 4-BIT ARITHMETIC LOGIC UNIT M159

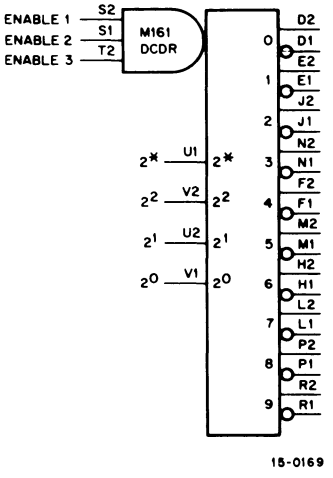
SIZE	CODE	NUMBER	REV.
B	CS	M159-0-1	
PRINTED CIRCUIT REV.		A	

DEC FORM NO.
DRB 102

5 DIST. 324, 434, 435 3 PINK

M161
Binary to Octal/Decimal Decoder

The M161 is a functional decoding module that can be used as a binary-to-octal or binary-coded decimal-(8421 or 2421 codes)-to-decimal decoder. In the binary-to-octal configuration, up to eight M161s can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2* input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4 modules) are shown in DEC's **Digital Logic Handbook**, 1970 edition. The figure assumes that the inputs to the decoder are the outputs of flip-flops such as FF2° (1), 1 output side; and FF2° (0), 0 output side.



M161 Simplified Diagram

The propagation delay through the decoder is typically 55 ns in the binary-to-octal mode and 75 ns in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 ns, thereby frequency-limiting this module to 8 MHz when used in this fashion. The ENABLE inputs can be used to strobe output data, if inputs 2° - 2* have settled at least 50 ns prior to the input pulse.

*The 2-bit input may be of decimal value 2, 4, 6, or 8 if illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.

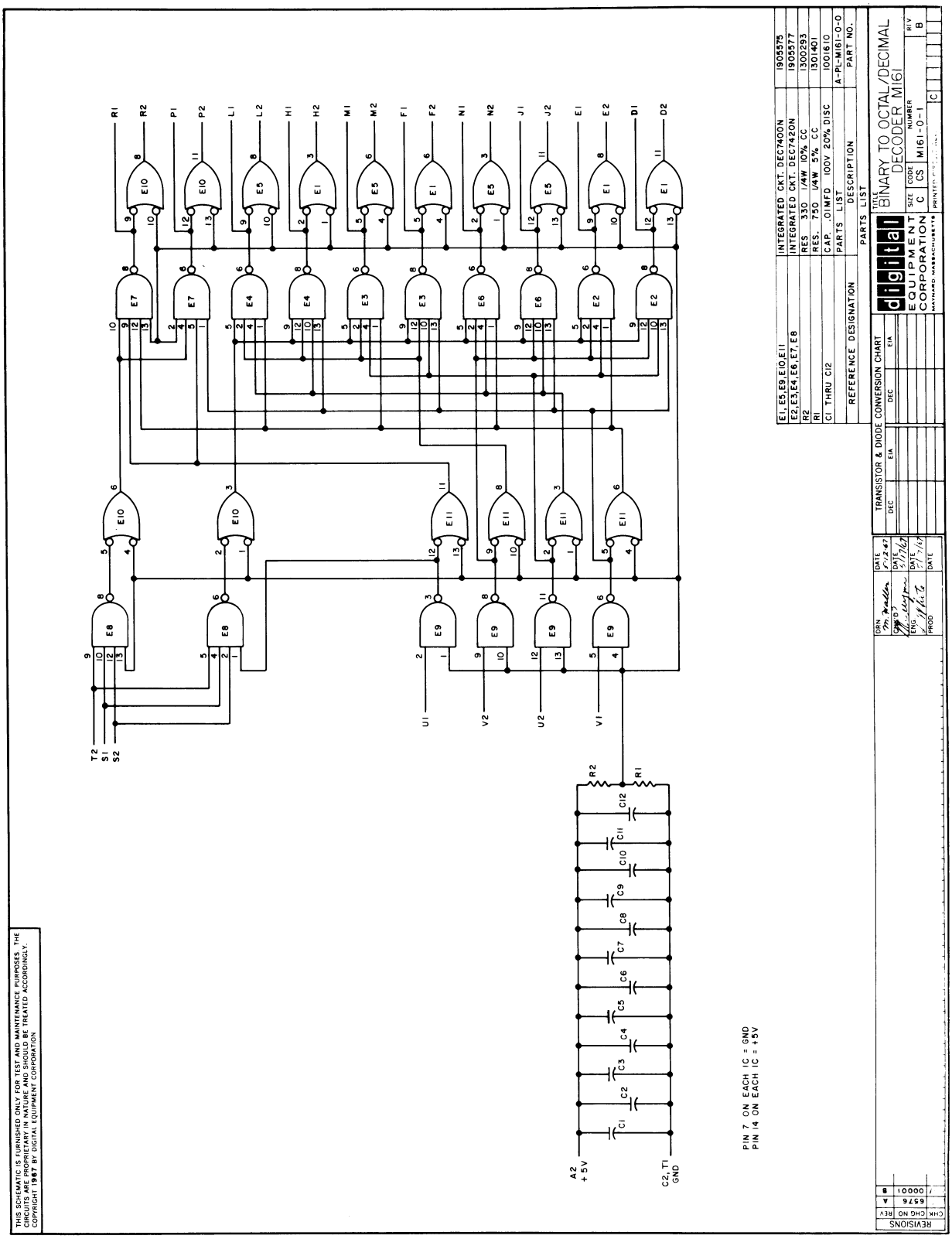
The following are the input, output, and power characteristics of the M161 module.

INPUTS: The inputs to the M161 are: 2° through 2*, 1 unit load each; ENABLE 1 through ENABLE 3, 2 unit loads each.

OUTPUTS: Each positive output is capable of driving 10 unit loads, and each negative output is capable of driving 9 unit loads.

POWER: Power dissipation of the M161 module is 5V at 120 mA (maximum).

*The 2-bit input may be of decimal value 2,4,6, or 8 if illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
COPYRIGHT 1967 BY DIGITAL EQUIPMENT CORPORATION
REVISIONS
CHK CHG NO REV
6576 A
10000 B
T2
S1
S2
U1
V2
U2
V1
A2 +5V
C2, T1 GND
R1
R2
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E5, E9, E10, E11 INTEGRATED CKT. DEC7400N 1905575
E2, E3, E4, E6, E7, E8 INTEGRATED CKT. DEC7420N 1905577
R2 RES. 330 1/4W 10% CC 1300293
R1 RES. 750 1/4W 5% CC 1301401
C1 THRU C12 CAP. .01MFD 100V 20% DISC 10016110
PARTS LIST A-PL-M161-0-0
REFERENCE DESIGNATION DESCRIPTION PART NO.
PARTS LIST
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
DEC EIA
DRN DATE
CHK DATE
ENG DATE
PROD DATE
digital
EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE BINARY TO OCTAL/DECIMAL DECODER M161
SIZE C CODE CS NUMBER M161-0-1 REV B
PRINTED
C

M162
Parity Circuit

The M162 module is a parity detector and contains two parity circuits. Each circuit indicates whether the binary data presented to it contains an odd or even number of 1s. The requirements of the data and its complement are shown in the illustration.

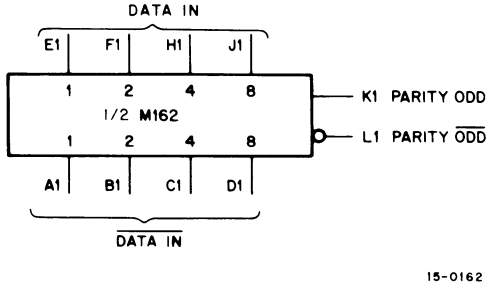
Indication of odd parity is given by a HIGH level at pins K1 and U2. Pins L1 and V2, when HIGH, indicate even parity or no input.

The following are the input, output, and power characteristics of the M162 module.

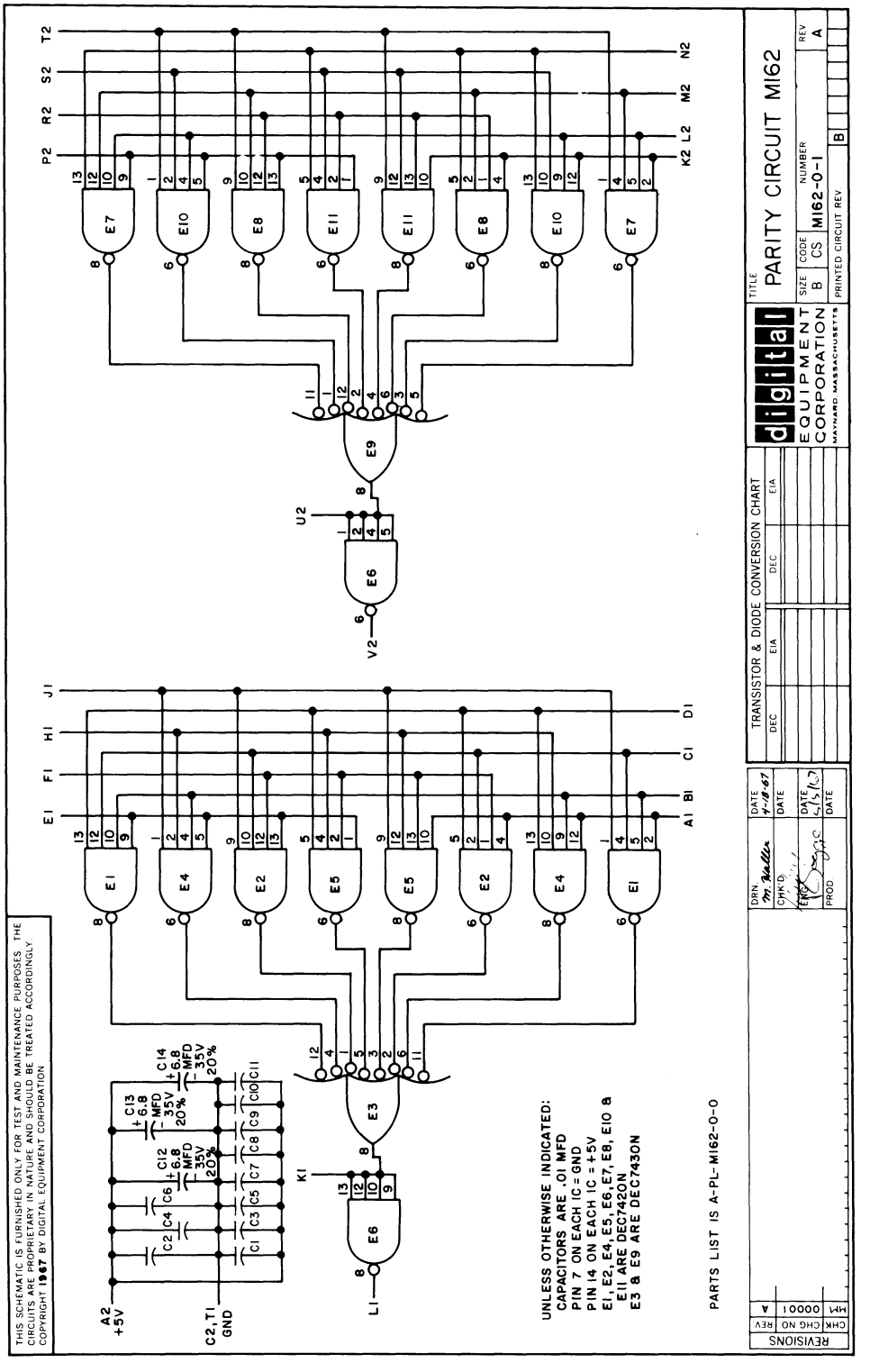
INPUTS: Each input presents four unit loads.

OUTPUTS: Pins L1 and V2 can each supply up to ten unit loads. Pin K1 and U2 can each supply up to six unit loads.

POWER: Power dissipation of the M162 module is +5V at 102 mA (maximum).

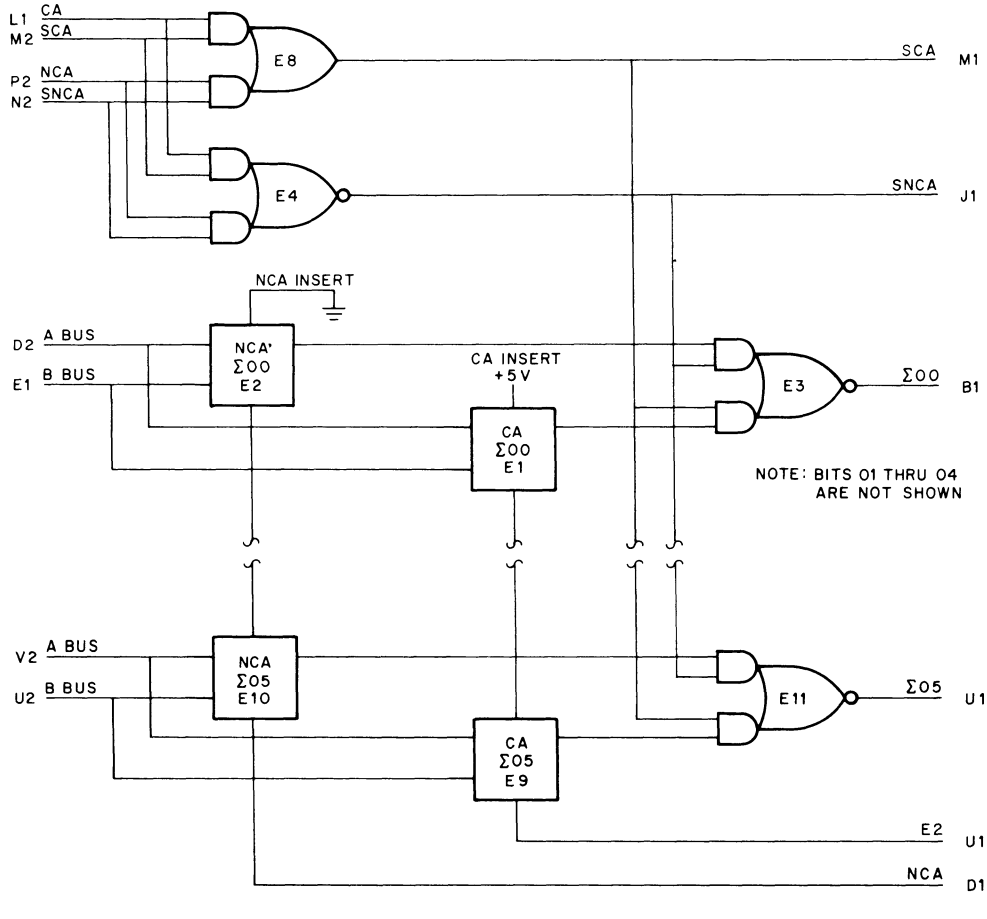


M162 Simplified Diagram


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY
COPYRIGHT 1967 BY DIGITAL EQUIPMENT CORPORATION
REVISIONS
CHK REV CHG NO DATE
A 10001
DRN M. Mullen DATE 4-8-67
CHK'D DATE
ENG DATE
PROD DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE PARITY CIRCUIT M162
SIZE B CODE CS NUMBER M162-0-1 REV A
PRINTED CIRCUIT REV B
A2 +5V
C2,T1 GND
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11
C12 6.8 MFD 35V 20%
C13 6.8 MFD 35V 20%
C14 6.8 MFD 35V 20%
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11
K1 L1 U2 V2
P2 R2 S2 T2 K2 L2 M2 N2
A1 B1 C1 D1 E1 F1 H1 J1
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01 MFD
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E2, E4, E5, E6, E7, E8, E10 & E11 ARE DEC7420N
E3 & E9 ARE DEC7430N
PARTS LIST IS A-PL-M162-0-0

M164
6-Bit Parallel Adder

The M164 module contains a 6-bit conditional sum adder. Three of these modules are connected in tandem to form the 18-bit adder used in the central processor of the PDP-15. (Refer to Engineering Drawings D-BS-KP15-0-1 through D-BS-KP15-0-18.) The adder can generate an 18-bit sum in 82 ns. This high speed is available because there is no carry propagated from one adder module to the next. Instead of having the carry propagated from module to module, which takes 48 ns per module, each 6-bit sum is performed twice simultaneously (see illustration). One sum, CA (carry anticipated), is formed without a carry inserted, while the other sum, NCA (no carry anticipated), is formed without a carry inserted. Combinational logic in each adder module



M164 Simplified Diagram

provides the control inputs SCA (select carry anticipated) or SNCA (select no carry anticipated) to the module handling the next six most significant bits. The sum from the first adder module during normal addition is always a sum without a carry inserted because the combinational logic is strapped to select the adder that has no carry inserted.

The following are the input, output, and power characteristics of the M164 module.

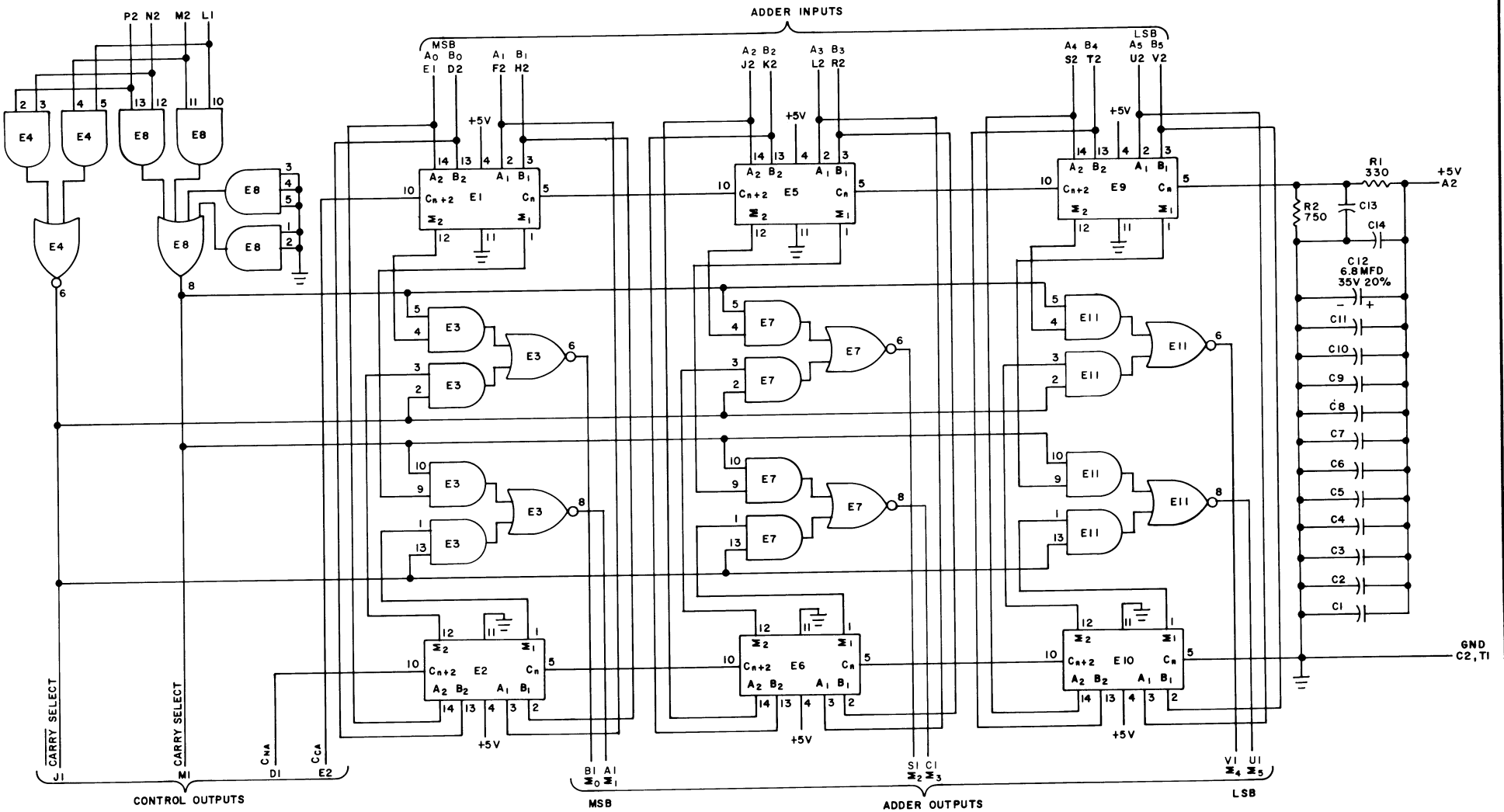
INPUTS: The M164 adder module is unbuffered; and all inputs must, therefore, remain stable for the entire add cycle. The following list shows all input connections and the TTL unit loading they present:

Name	Pin	Loading	True 1
A0	E1	2.0	+2.0
B0	D2	2.0	+2.0
A1	F2	8.0	+2.0
B1	H2	8.0	+2.0
A2	J2	2.0	+2.0
B2	K2	2.0	+2.0
A3	L2	8.0	+2.0
B3	R2	8.0	+2.0
A4	S2	2.0	+2.0
B4	T2	2.0	+2.0
A5	U2	8.0	+2.0
B5	V2	8.0	+2.0
CA	L1	2.5	+2.0
SCA	M2	2.5	+2.0
SNCA	N2	2.5	+2.0
NCA	P2	2.5	+2.0

OUTPUTS: The M164 adder module generates a 6-bit sum in 78 ns and a carry in 42 ns. All output connections and TTL driving capabilities are shown below.

Name	Pin	Drive	True 1
Σ 0	B1	12.5	0.4
Σ 1	A1	12.5	0.4
Σ 2	S1	12.5	0.4
Σ 3	C1	12.5	0.4
Σ 4	V1	12.5	0.4
Σ 5	U1	12.5	0.4
SNCA	J1	5.0	2.4
SCA	M1	5.0	2.4
CA	E2	5.0	0.4
NCA	D1	5.0	0.4

POWER: Power dissipated in the M164 module is 5V at 118 mA (maximum).



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD
RESISTORS ARE 1/4W; 5%
PIN 7 ON EACH IC (EXCEPT DEC7482N'S) = GND
PIN 14 ON EACH IC (EXCEPT DEC7482N'S) = +5V
E1, E2, E5, E6, E9, E10 ARE DEC7482N
E3, E4, E7, E11 ARE DEC74H50N
E8 IS DEC74H52N

OUTPUT DRIVE (UNIT LOADS)
$\Sigma_0, \Sigma_1 \cdots \Sigma_5$: 12.5
CARRY SELECT : 5.0
C_{NC}, C_{CA} : 5.0

INPUT LOADS (UNIT)
A_1, A_3, A_5 : 8
B_1, B_3, B_5 : 8
A_0, A_2, A_4 : 2
B_0, B_2, B_4 : 2
OUTPUT SELECT : 2.5

M164-3

REVISIONS			
CHK	CHG NO.	REV.	
	00001	C	

DRN. M. Keller	DATE 4-17-69	
CHK'D R. Yaeger	DATE 3-20-69	
ENG. J. Grabert	DATE 5/14/69	
PROD. [illegible]	DATE 9/14/[illegible]	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: 6 BIT ADDER M164

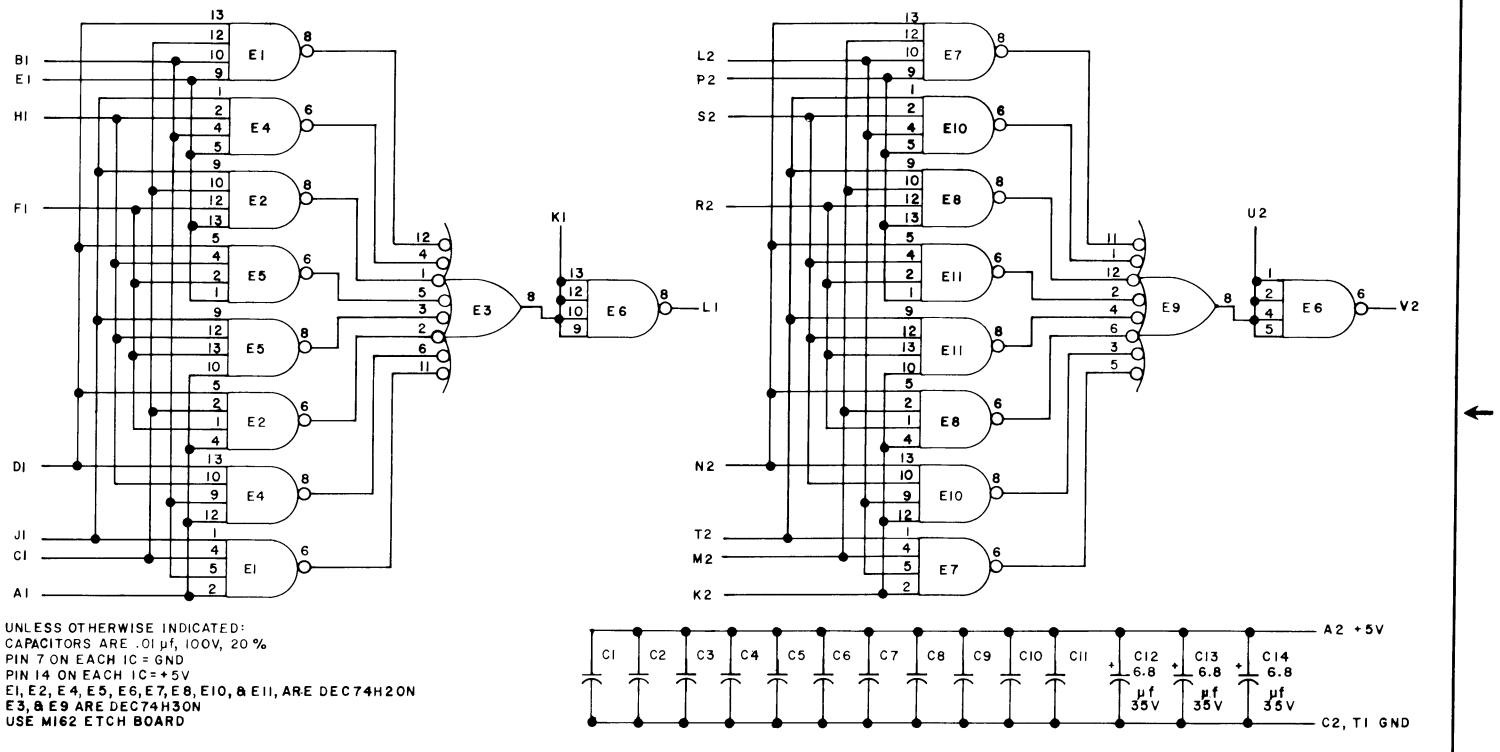
SIZE	CODE	NUMBER	REV.
C	CS	M164-0-1	C

PRINTED CIRCUIT REV. B

SIZE C | CODE CS | NUMBER M164-0-1 | REV. C

5 PINK DIST. 324, 434, 455

DEC FORM NO. DRC 102



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01 µf, 100V, 20 %
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E2, E4, E5, E6, E7, E8, E10, & E11, ARE DEC74H20N
E3, & E9 ARE DEC74H30N
USE M162 ETCH BOARD

REVISIONS	REV	CHK	CHG NO

DRN. Nancy Moore	DATE 2/13/70	
CHK'D D.G. Wall	DATE 3-9-70	
ENG. H. Lawson	DATE 5/19/70	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PARITY CIRCUIT M182

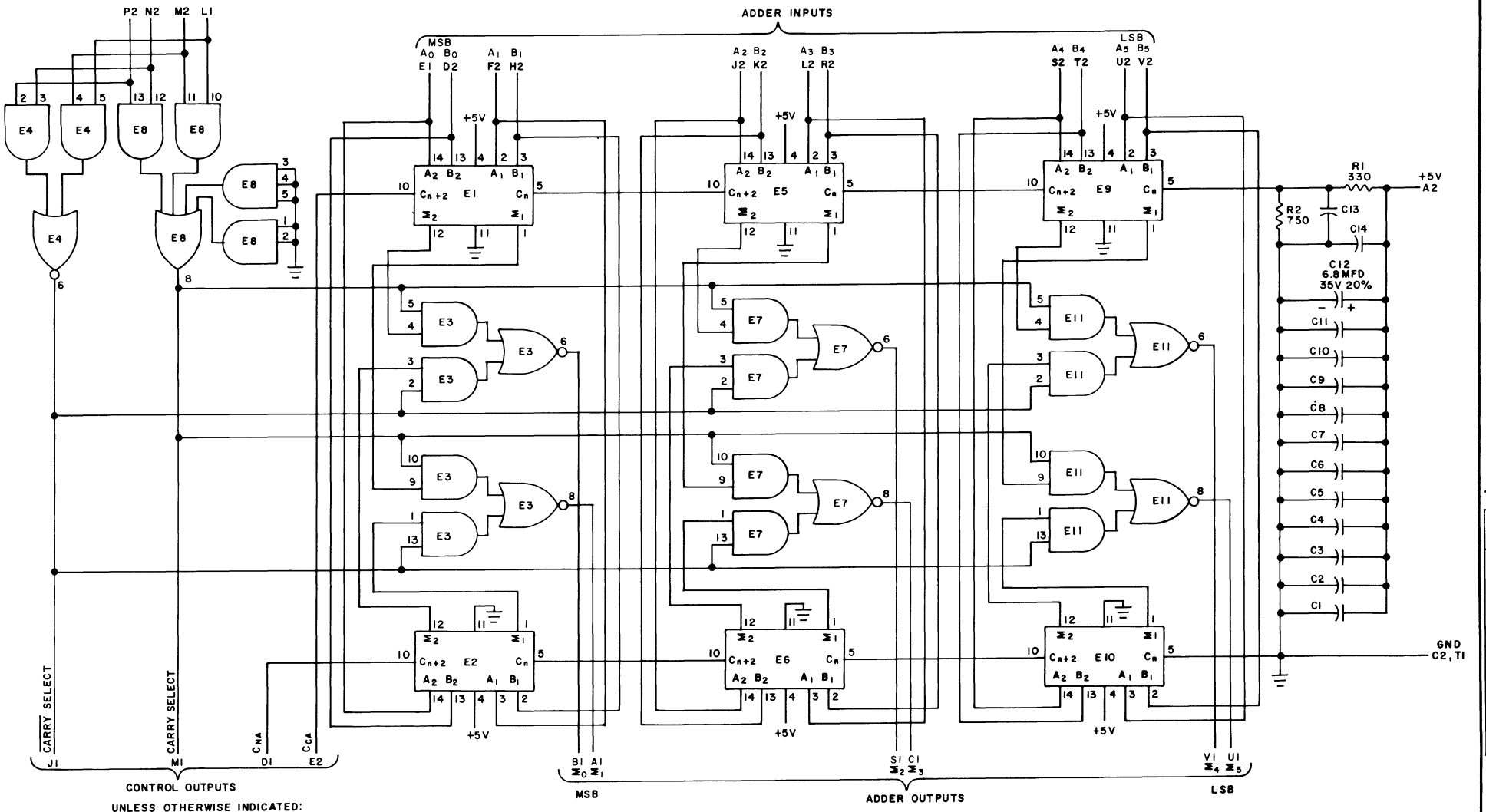
SIZE	CODE	NUMBER	REV.
B	CS	M182-0-1	

PRINTED CIRCUIT REV. B

DEC FORM NO. DRB 102

5 PINK DIST. 324,434,435 3

SIZE B | CODE CS | NUMBER M182-0-1 | REV.



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD
RESISTORS ARE 1/4W; 5%
PIN 7 ON EACH IC (EXCEPT DEC7482N'S) = GND
PIN 14 ON EACH IC (EXCEPT DEC7482N'S) = +5V
E1, E2, E5, E6, E9, E10 ARE DEC7482N
E3, E4, E7, E11 ARE DEC74H50N
E8 IS DEC74H52N

OUTPUT DRIVE (UNIT LOADS)	
$\Sigma_0, \Sigma_1 \cdots \Sigma_5$	12.5
$\overline{\text{CARRY SELECT}}$	5.0
C_{NC}, C_{CA}	5.0

INPUT LOADS (UNIT)	
A_1, A_3, A_5	8
B_1, B_3, B_5	8
A_0, A_2, A_4	2
B_0, B_2, B_4	2
OUTPUT SELECT	2.5

M164-3

REVISIONS			
CHK	CHG NO.	REV.	
	00001	C	

DRN. M. Keller	DATE 4-17-69	
CHK'D R. Granger	DATE 3-20-69	
ENG. J. Grabert	DATE 5/14/69	
PROD.	DATE 9/4/69	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: 6 BIT ADDER MI64

SIZE	CODE	NUMBER	REV.
C	CS	M164-0-1	C

PRINTED CIRCUIT REV. B

SIZE C | CODE CS | NUMBER M164-0-1 | REV. C

DEC FORM NO. DRC 102

5 PINK DIST: 324, 434, 455

M191
Carry Look-Ahead Generator

The M191 Carry Look-Ahead Generator, consisting of two DEC 74182 integrated circuits, is a high-speed generator capable of anticipating a carry through a group of ALUs. A 13-ns delay occurs for each look-ahead level.

Input Voltage:	5.5 volts (with respect to network grand terminal).
Supply Voltage:	4.75 – 5.25 (5 v. nominal)
Normalized Fan Out from Each Output:	High logic level 20 Low logic level 10

Each carry look-ahead circuit in the M191 is associated with four ALUs (16 bits). The M191, when used in conjunction with the M159 ALU, provides carry, generate-carry, and propagate-carry functions for 36-bit words. Each circuit generates the anticipated carry through its respective group of ALUs, as well as providing a Generate (G) and Propagate (P) input to a third carry look-ahead circuit associated with the last ALU; hence, the term full-carry look-ahead in three levels (36 bits).

Depending on the selected function of the ALUs, the carry look-ahead circuitry determines whether a carry will be propagated through the particular ALU, or whether the selected function will generate a carry. If a carry is produced, it is directed into the next ALU in line. This sequence is continued for each of the four ALUs in the section. The carry look-ahead circuitry then "looks" at the G and P signals of all four ALUs and determines whether a carry should be inserted into the next four ALUs and into the third level of carry look-ahead. This process is continued for the second section of ALUs (next 16 bits). Finally, the third level of carry look-ahead determines whether a carry should be inserted into the final ALU by examining the resulting G and P inputs of the other two look-ahead circuits.

The truth table for the first-stage carry is as follows:

True Carry Insert = L

P00	G00	C_{N00}	C_{N+X}
L	L	L	H
L	L	H	H
H	H	H	L
L	H	L	L

True Carry Insert = Low

P00	G00	C_{N00}	C_{N+X}
L	L	L	H
H	L	L	H
L	H	L	L
H	H	L	L
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	L

The following are the logic equations for a carry look-ahead stage:

$$C_{N01} = C_{N00} * G_0 + G_0 * P_0$$

$$C_{N02} = G_1*P_1 + P_0*G_0*G_1 + G_1*G_0*C_N$$

$$C_{N03} = P_2*G_2 + G_1*G_2*P_1 + G_0+G_1*G_2*P_0+G_0*G_1*G_2*C_N$$

$$GG00 = P_3*G_3 + P_2*G_3*G_2 + P_1*G_3*G_2*G_1+G_3*G_2*G_1*G_0$$

$$PP00 = P_3+P_2 + P_1+P_0$$

where

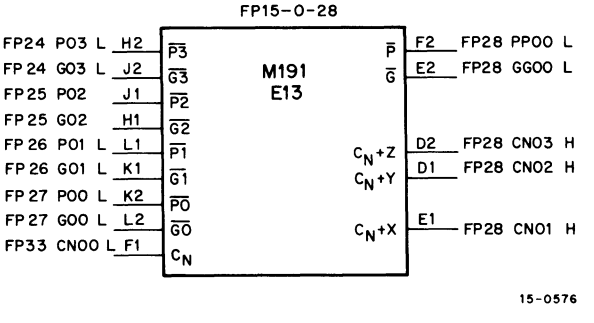
C_{NXX} = True L

GXX = True H

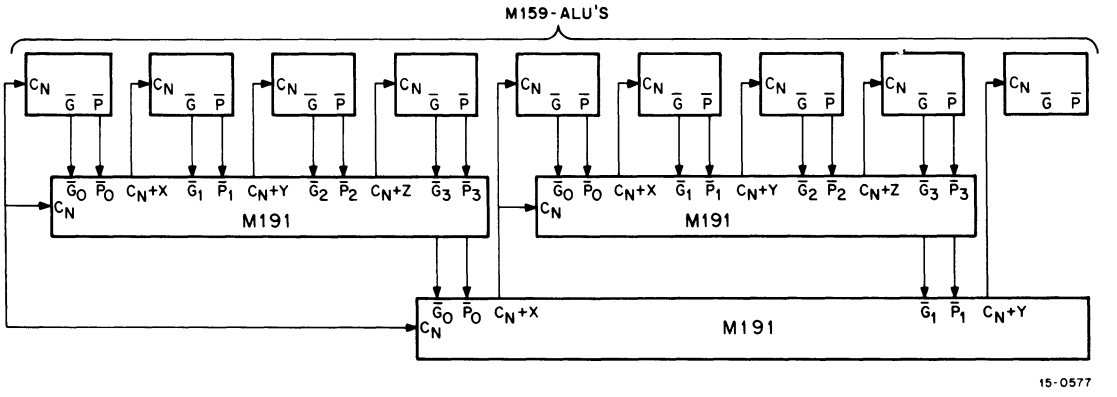
PXX = True H

GGXX = True H

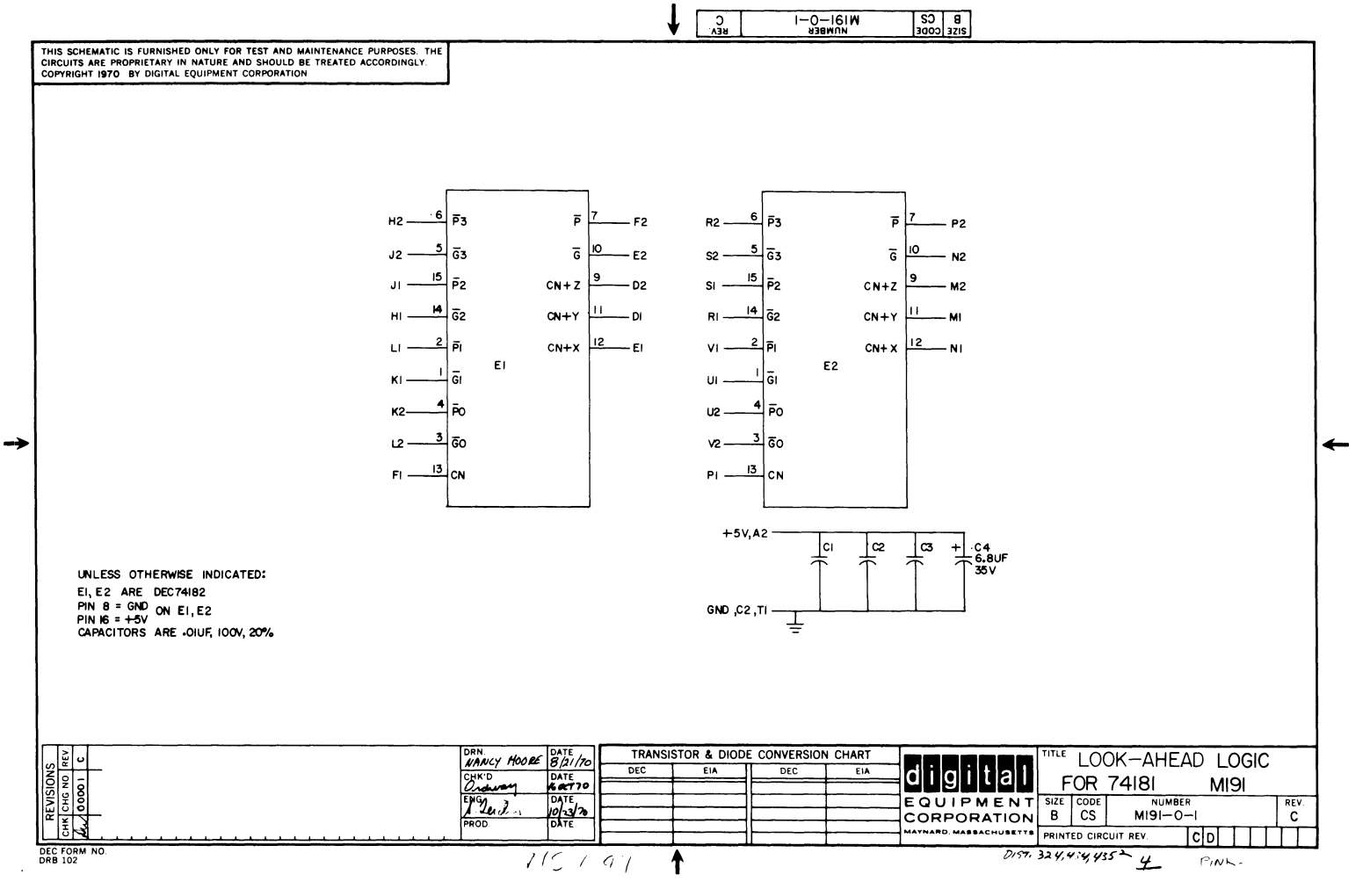
PPXX = True H



M191 Carry Look-Ahead Generator



36-Bit ALU, Full-Carry Look-Ahead in Three Levels



M205
D Flip-Flops

The M205 module contains five separate D-type flip-flops. Each flip-flop has independent DATA, CLOCK, SET, and CLEAR inputs. Information must be present on the DATA input 20 ns (maximum) before the CLOCK pulse, and the information should remain at the input at least 5 ns (maximum) after the CLOCK pulse has passed the threshold voltage. Data transferred into the flip-flop by the previous CLOCK pulse will be present on the 1 output of the flip-flop. Typical time duration of the CLOCK pulse preset and reset pulses is 30 ns each. Maximum delay through the flip-flop is 50 ns. Refer to the M206 description for additional details.

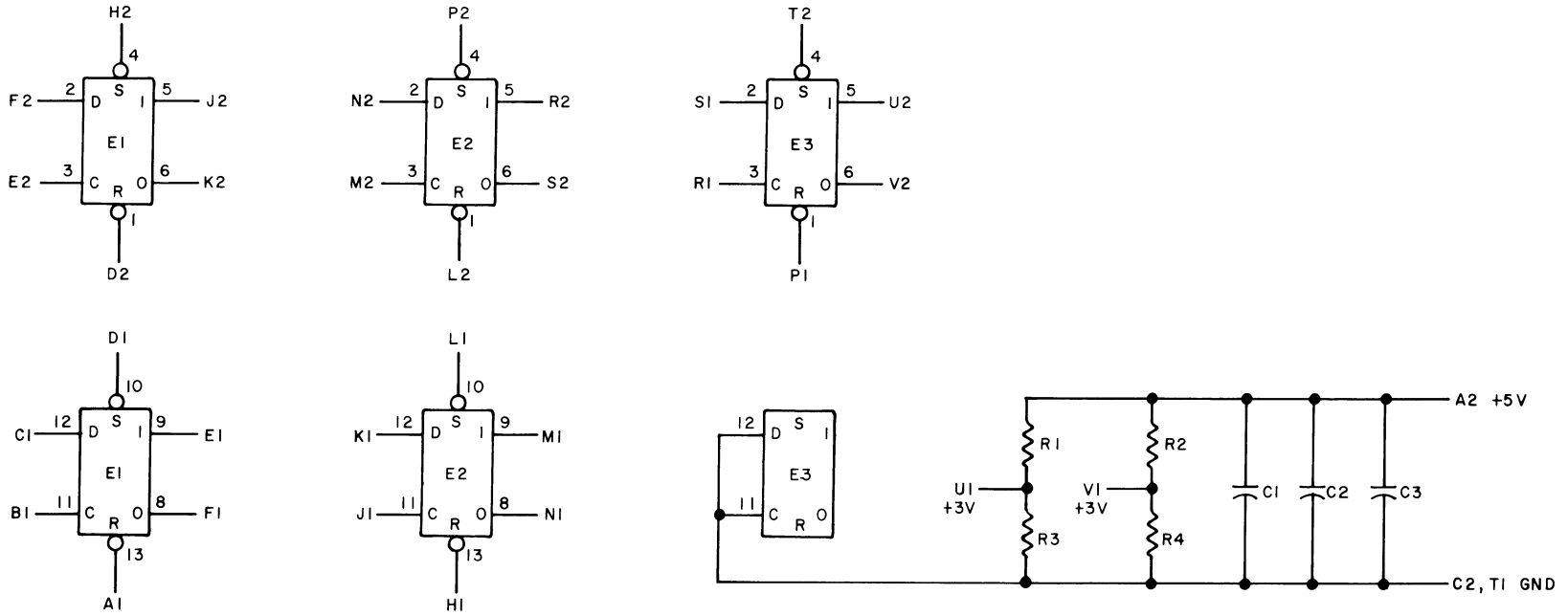
The following are the input, output, and power characteristics of the M205 module.

INPUTS: D inputs present 1 unit load each.
C inputs present 2 unit loads each.
SET inputs present 2 unit loads each.
CLEAR inputs present 3 unit loads each.

OUTPUTS: Each output (0 and 1) is capable of driving 10 unit loads. Two +3V supplies (U1 and V1), capable of 25 unit loads, are available.

POWER: Power dissipation of the M205 module is +5V at 55 mA (average), 100 mA (maximum).

SIZE	CODE	NUMBER	REV.
B	CS	M205-0-1	B



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M205-0-0
C1,C2,C3	CAP. .01MFD 100V 20% DISC	1001610
R1,R2	RES. 330 1/4W 5% CC	1300295
R3,R4	RES. 750 1/4W 5% CC	1301401
E1, E2, E3	INTEGRATED CKT. DEC7474N	1905547

PARTS LIST

REVISIONS	REV.	CHG NO	CHK
	B	100001	EJ

DRN. M. Keller	DATE 2-17-69	
CHK'D R. Schreiner	DATE 3/13/69	
ENG. F.C. Ausmann	DATE 4/7/69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: 5 "D" FLIP FLOPS M205

SIZE	CODE	NUMBER	REV.
B	CS	M205-0-1	B

PRINTED CIRCUIT REV. A

DEC FORM NO.
DRB 102

DIST 3 x 4,431,432

M206
D Flip-Flops

The M206 contains six separate D-Type flip-flops. Each flip-flop has independently gated DATA, CLOCK, and dc SET inputs.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

Configuration	CLEAR 1 (A1)	CLEAR 2 (K2)	Delete Jumper	Add Jumper
3-3	FFO, 1, & 2	FF3, 4, & 5		
4-2	FFO & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FFO	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

Information must be present on the D input 20 ns (maximum) prior to a standard CLOCK pulse and should remain at the input at least 5 ns (maximum) after the CLOCK pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop is stable at the output within 50 ns (maximum). Typical width requirement for the CLOCK, dc RESET, and dc SET pulses is 30 ns each.

Information present on the D input is transferred to the output when the threshold is reached on the leading (positive-going voltage) edge of the CLOCK pulse.

The following are the input, output, and power characteristics of the M206 module.

INPUTS: D inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 3 unit loads per connected flip-flop. S inputs present 2 unit loads each.

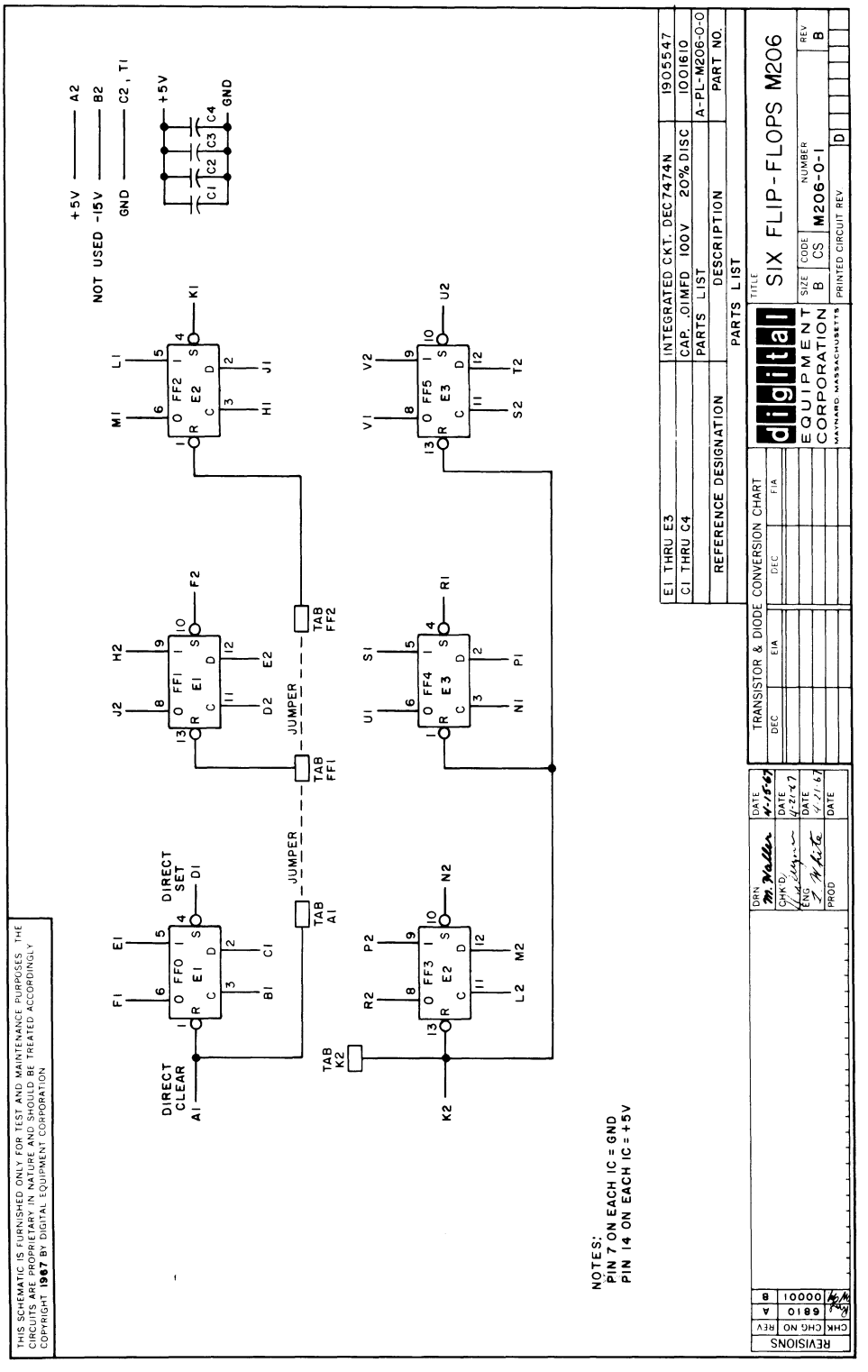
OUTPUTS: Each output is capable of driving 10 unit loads.

POWER: Power dissipation of the M206 module is +5V at 87 mA (maximum).

A common clear for all six flip-flops can be obtained by externally wiring pins A1 and K2 together.

CAUTION

The loading of each CLEAR line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY
COPYRIGHT 1967 BY DIGITAL EQUIPMENT CORPORATION
+5V A2
NOT USED -15V B2
GND C2, T1
+5V
C1 C2 C3 C4
GND
DIRECT CLEAR
A1
DIRECT SET
D1
JUMPER
TAB A1
TAB K2
K2
TAB FF1
TAB FF2
JUMPER
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1 THRU E3 INTEGRATED CKT. DEC7474N 19055547
C1 THRU C4 CAP. .01MFD 100V 20% DISC 100610
PARTS LIST A-PL-M206-0-0
REFERENCE DESIGNATION DESCRIPTION PART NO.
PARTS LIST
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
DEC EIA
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
SIX FLIP-FLOPS M206
SIZE B
CODE CS
NUMBER M206-0-1
REV B
PRINTED CIRCUIT REV D
REVISIONS
CHK CHG NO REV
10000 B
6810 A
DRN M. Miller DATE 4/1/67
CHK'D DATE
ENG DATE 4/11/67
PROD DATE

M207
Flip-Flop

The M207 Flip-Flop module contains six J-K type flip-flops that can be used as buffers, control flops, shift registers, and counters. A truth table for clocked set and reset conditions is shown below:

INPUT			OUTPUT			
			Initial State		Resultant State	
C	J	K	1	0	1	0
H→L	L	L	L	H	L	H
	L	H			L	H
	H	L			H	L
	H	H			H	L
	L	L	H	L	H	L
	L	H			L	H
	H	L			H	L
	H	H			L	H

Note that when both inputs are high, the flip-flop complements on each clock pulse.

Application of a low level to an R input for at least 30 ns unconditionally resets the flip-flop. Two CLEAR inputs are provided with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0.

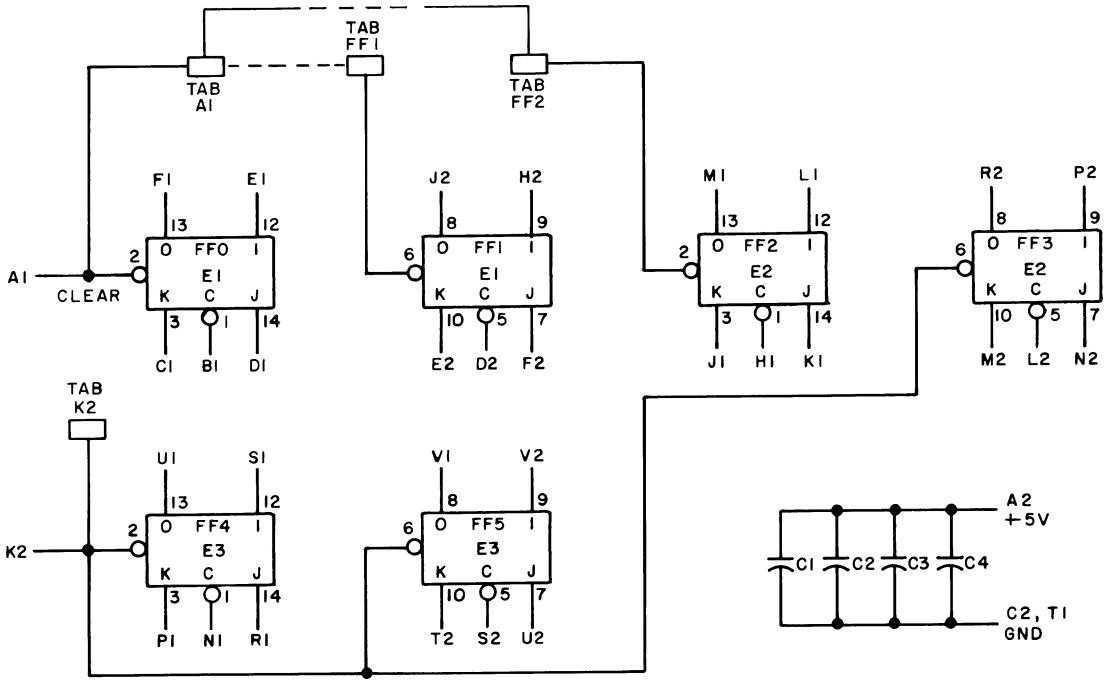
J and K inputs must be stable during the leading-edge threshold of the standard clock input, and must remain stable during the positive state of the clock. Data transferred into the flop will be stable at the output within 30 ns (typical) of the clock pulse trailing-edge threshold (negative-going voltage).

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M207 modules are supplied with the standard 3-3 configuration but the grouping can be changed as follows:

Clear Grouping	Clear 1 (A1)	Clear 2 (K2)	Delete Jumper	Add Jumper
3-3	FF0,FF1,FF2	FF3,FF4,FF5		
4-2	FF0,FF1	FF2,FF3,FF4, FF5	FF1-FF2	K2-FF2
5-1	FF0	FF1,FF2,FF3, FF4 and FF5	A1-FF1	K2-FF1

INPUTS:	Input characteristics are as follows: J and K inputs present one unit load C inputs present two unit loads. CLEAR inputs present two unit loads per connected flip-flop.
OUTPUTS:	Each output is capable of driving 10 unit loads.
POWER:	+5V, 96 mA (max.)

SIZE	CODE	NUMBER	REV
B	CS	M207-0-1	E



NOTES:
PIN 4 ON EACH IC = +5V
PIN 11 ON EACH IC = GND
---- INDICATES JUMPER
JUMPER CAN BE INSTALLED BY CUSTOMER BETWEEN FF2 & K2, AND BETWEEN FF1 & K2

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
E1 THRU E3	INTEGRATED CKT. DEC7473N	1905587
C1 THRU C4	CAP. .01 MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M207-0-0

REVISIONS	REV	CHG NO	CHK
	A	6809	
	B	00001	
	E	00002	

		DATE
DRN.	M. Waller	4-21-67
CHK'D		5-17-67
ENG.		5-22-67
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: FLIP-FLOP M207

SIZE	CODE	NUMBER	REV
B	CS	M207-0-1	E

PRINTED CIRCUIT REV. E

DIST. 324 434 43

PINK

DEC FORM NO. DRB 102

M211
Binary Up-Down Counter

The M211 is a 6-bit binary UP/DOWN counter. It can switch counting mode (UP or DOWN) without disturbing the contents of the counter. Maximum count rate is 10 MHz. SET/RESET inputs are available for each bit. Maximum carry propagation time is 80 ns per bit.

ENABLE LINE: The Enable input must be negated 100 nsec prior to an UP/DOWN level command.

The Enable input must not be negated earlier than 500 nsec after the leading edge (positive going voltage) of the clock pulse.

The Enable input must be asserted at least 60 nsec prior to the first count.

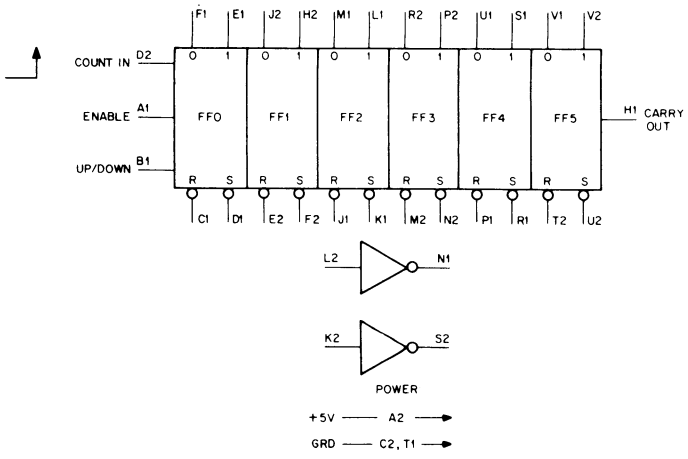
UP/DOWN Control Line: A logical 1 on this line will yield an up count. A logical 0 on this line will yield a down count.

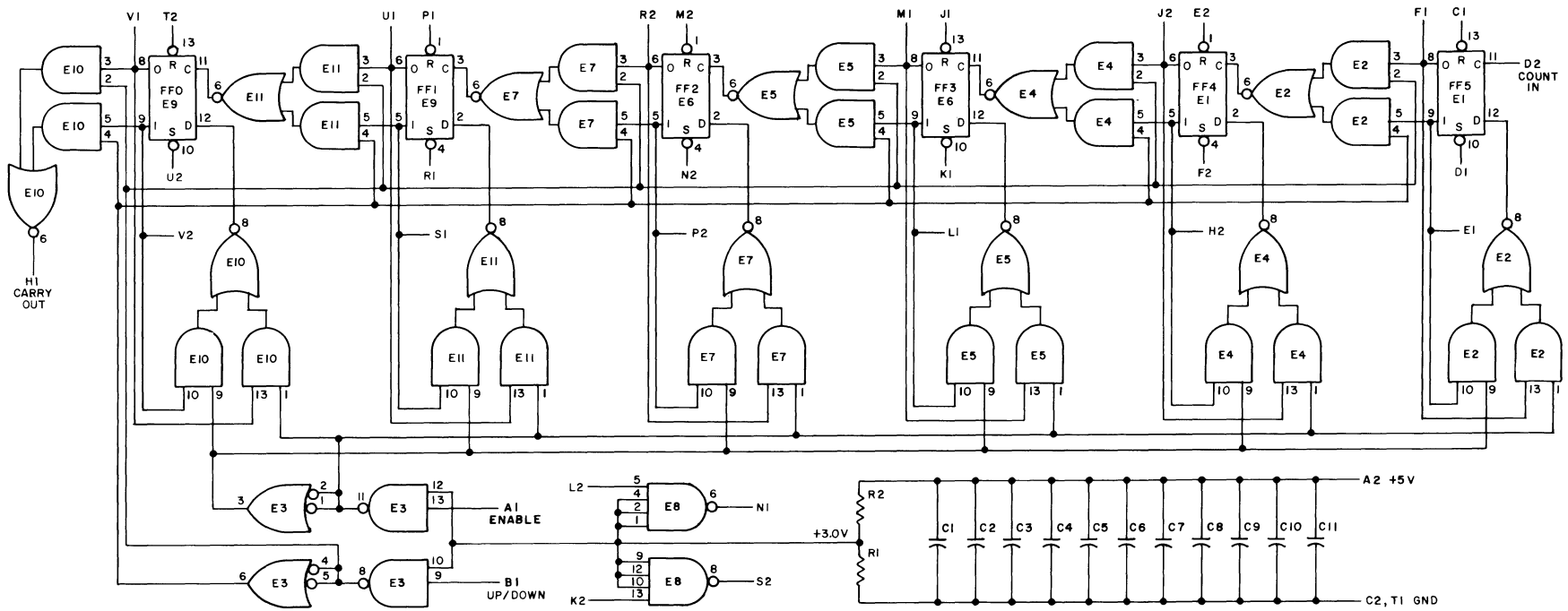
CARRY OUT: The Carry Out will yield a positive level change whenever a carry or borrow occurs.

INPUTS: Count In – positive transition or pulse with less than 400 nsec risetime. Count In presents 2 unit loads. Reset – Each reset input presents 3 unit loads. Set – Each set input presents 2 units loads. All other inputs present 1 unit load.

OUTPUTS: Each flip-flop output (1 or 0) can drive 8 unit loads. Carry Out can drive 10 unit loads. Each inverter output can drive 30 unit loads.

POWER: +5.0V, 217 mA (max.)





NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
DEC7451N MAY BE USED IN PLACE OF DEC7450N

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M211-0-0
C1 THRU C11	CAP. .01MFD 100V 20% DISC	1001610
R1	RES. 7.5K 1/4W 5% CC	1301422
R2	RES. 3.3K 1/4W 5% CC	1300439
E1, E6, E9	INTEGRATED CKT. DEC7474N	1905547
E2, E4, E5, E7, E10, E11	INTEGRATED CKT. DEC7450N	1905580
E3	INTEGRATED CKT. DEC7400N	1905575
E8	INTEGRATED CKT. DEC7440N	1905579

PARTS LIST

REVISIONS			
CHK	CHG NO.	REV	
	00001	A	
	00002	C	

DRN. M. Keller	DATE	10-12-67
CHK'D	DATE	
ENG.	DATE	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: BINARY UP/DOWN COUNTER M211

SIZE	CODE	NUMBER	REV.
C	CS	M211-0-1	C

PRINTED CIRCUIT REV. B

DIST. 324, 434, 435 PINK

DEC FORM NO. DRC 102

M211-2

SIZE C | CODE CS | NUMBER M211-0-1 | REV. C

M212
6-Bit Left/Right Shift Register

The M212 module is an internally-connected left/right shift register/buffer that consists of six edge-triggered D-type flip-flops. The M212 features parallel selection and loading of either of two independent 6-bit sources, or serial loading and shifting of data in either the left or right direction.

All operations of this register, with the exception of clear, are effected by the leading edge of a positive pulse applied at pin C1. Four function enable inputs define the module operation. The enable inputs are: ENABLE RIGHT SHIFT, ENABLE LEFT SHIFT, ENABLE INPUT A, and ENABLE INPUT B.

INPUTS: Input characteristics are as follows:

Data inputs present one unit load, logic 1 is +2.8V, or greater, logic 0 is +0.8V, or less.

Enable inputs present six unit loads, logic 1 is +2.8V, or greater, logic 0 is +0.8V or less.

Data and enable inputs must be stable at the gate inputs 50 ns before the clock threshold is attained.

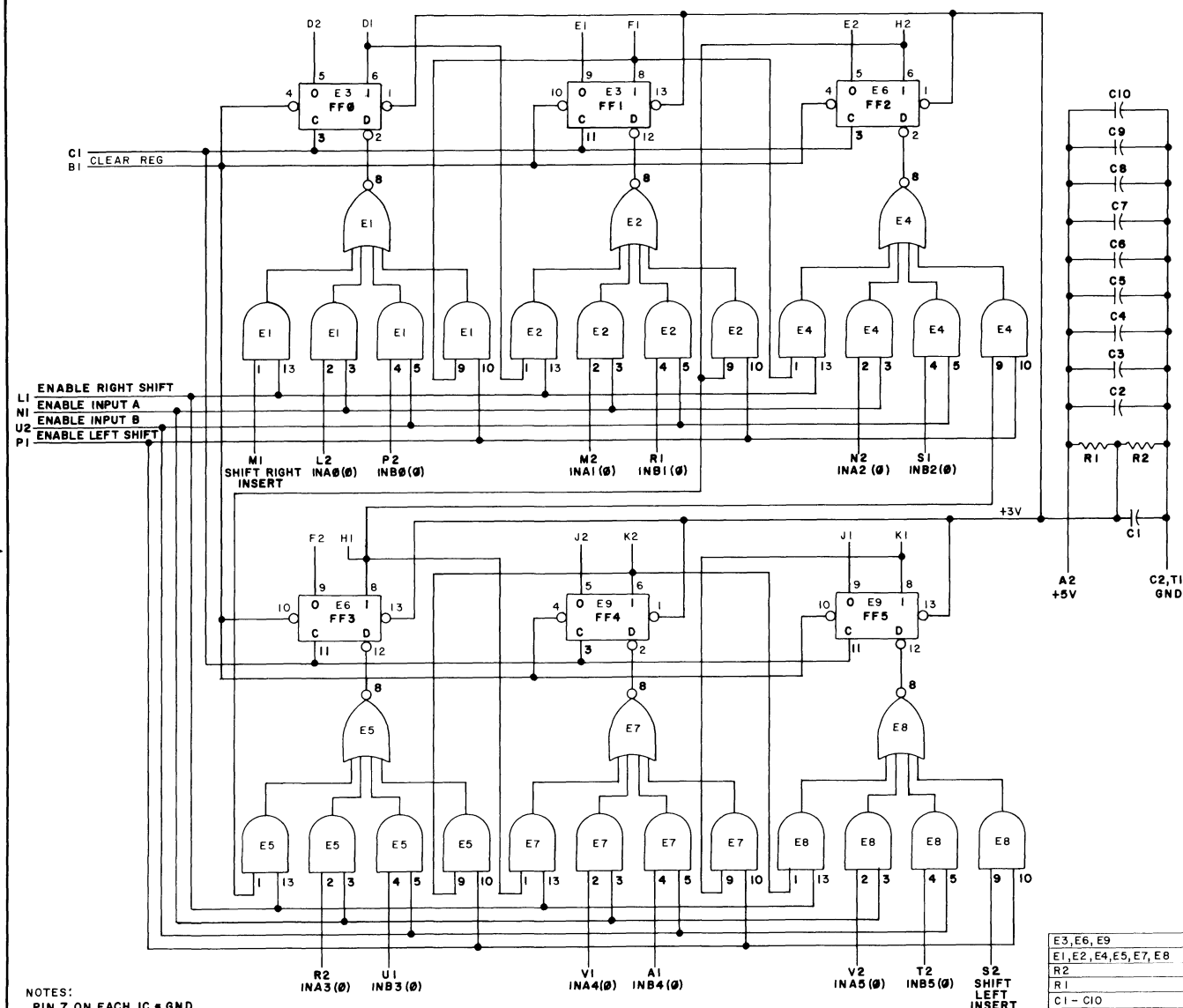
Assertion of the clock input is a transition from 0 to +3.0V. The clock input presents 12 unit loads.

A direct clear input at pin B1 resets all flip-flops. A +3.0 to 0V transition at least 30 ns duration is required. The direct clear input presents 12 unit loads.

OUTPUTS: Both the 0 and 1 output of each flip-flop are brought to output pins. Data transferred into each flip-flop will be stable at the output within 50 ns of the leading edge of the clock pulse.

Each 0 output will drive 10 unit loads. Each 1 output will drive 8 unit loads.

POWER: +5V, 145 mA (max.)



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
C1 - C10	CAP. .01 MFD 100V 20% DISC	1001610
R1	RES. 1.5K 1/4W 5% CC	1300391
R2	RES. 3K 1/4W 5% CC	1300432
E1,E2,E4,E5,E7,E8	INTEGRATED CKT. DEC7453N	1905582
E3,E6,E9	INTEGRATED CKT. DEC7474N	1905547

PARTS LIST A-PL-M212-0-0

REVISIONS			
CHK	CHG NO	REV	

DRN	Jo Waller	DATE 11-1-67
CHK'D		DATE
ENG.		DATE
PROD.	2	DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 6 BIT L-R SHIFT REGISTER M212

SIZE	CODE	NUMBER	REV
C	CS	M212-0-1	B

PRINTED CIRCUIT REV. B

M212-2

SIZE C | CODE CS | NUMBER M212-0-1 | REV B

DEC FORM NO. DRC 102

PINK

DIST. 324 ~ 54 ~ 352

M214
Data Storage Register

The M214 module contains a 6-bit adder and a 6-bit storage register with input gating logic. Three of these modules are connected in tandem to form the 18-bit data storage register (DSR) used in the I/O processor of the PDP-15. (Refer to Engineering Drawings D-BS-KD15-0-1 through D-BS-KD15-0-3.) The register is used for exchanging data between memory and I/O devices. Input gating logic is included in the module for strobing the memory data lines (MDL), I/O buffer (IOB), and the I/O address (IOA) into the register.

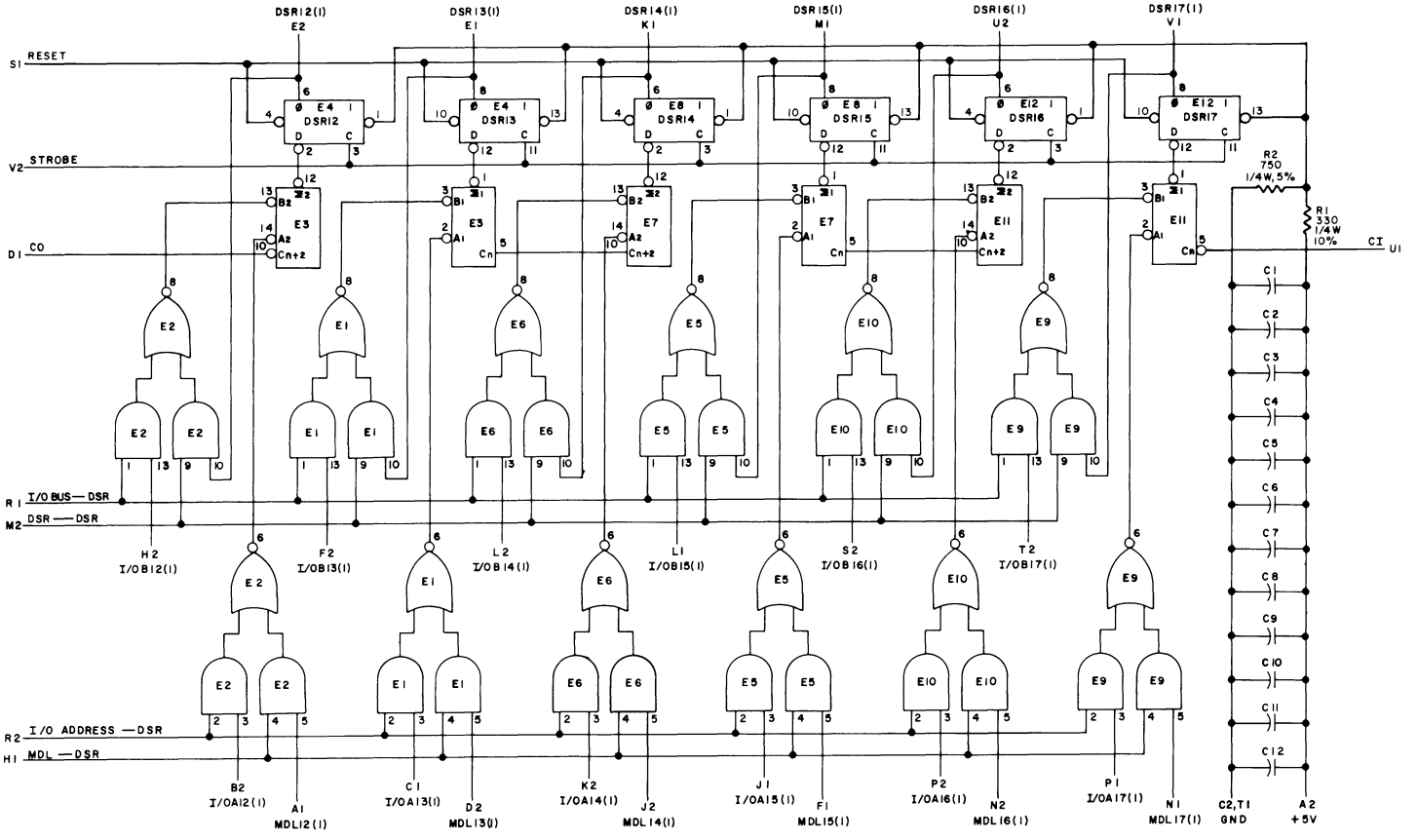
The following are the input, output, and power characteristics of the M214 module.

INPUTS: The following list shows all input connections and the TTL unit loading they present:

Name	Pin	Loading
CARRY-IN	U1	4
IOA to DSR	R2	6
IOB to DSR	R1	6
MDL to DSR	H1	6
DSR to DSR	M2	6
IOA	B2, C1, K2, J1, P2, P1	1 each
IOB	H2, F2, L2, L1, S2, T2	1 each
MDL	A1, D2, J2, F1, N2, N1	1 each
STROBE	V2	6

OUTPUTS: Each DSR output (pins E2, E1, K1, M1, U2, and V1) is capable of driving 9 unit loads, and the CARRY OUTPUT (pin D1) is capable of driving 5 unit loads. The STROBE pulse should occur at least 100 ns after the CARRY-IN and the input data have stabilized. DSR outputs should occur 50 ns (maximum) after the module is strobed.

POWER: Power dissipation of the M214 module is 5V at 280 mA (maximum).



UNLES OTHERWISE INDICATED:
PIN 7 ON EACH IC (EXCEPT E3, E7, E11) = GND
PIN 14 ON EACH IC (EXCEPT E3, E7, E11) = +5V
PIN 4 ON E3, E7, E11 = +5V
PIN 11 ON E3, E7, E11 = GND
E4, E8, E12 ARE DEC7474
E3, E7, E11 ARE DEC7482
E1, E2, E5, E6, E9, E10 ARE DEC 7450
CAPACITORS ARE .01μf, 100V, 20%

REVISIONS			
CHK	CHG NO.	REV.	
	00001	B	

DRN.		DATE 3-17-69
CHK'D		DATE 3-18-69
ENG.		DATE 5-5-69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DATA STORAGE REGISTER M214

SIZE	CODE	NUMBER	REV
C	CS	M214-0-1	B

PRINTED CIRCUIT REV. B

DEC FORM NO. DRC 102

DIST. 324,474,488 PINK

M214-2

SIZE C | CODE CS | M214-0-1 | REV. B

M216
D Flip-Flops

The M216 module contains six separate D-type flip-flops with independent DATA-SET and CLOCK inputs. The CLEAR inputs to these flip-flops are connected to two clear input lines (three flip-flops to each line).

Data must be present on the D input 20 ns (maximum) before the CLOCK pulse and should remain at the input at least 5 ns (maximum) after the CLOCK pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop is stable at the output within 50 ns (maximum). Typical width requirements for the CLOCK and dc RESET pulses are 30 ns each.

Data present on the D input is transferred to the output when the threshold is reached on the leading (positive-going voltage) edge of the CLOCK pulse.

The following are the input, output, and power characteristics of the M216 module.

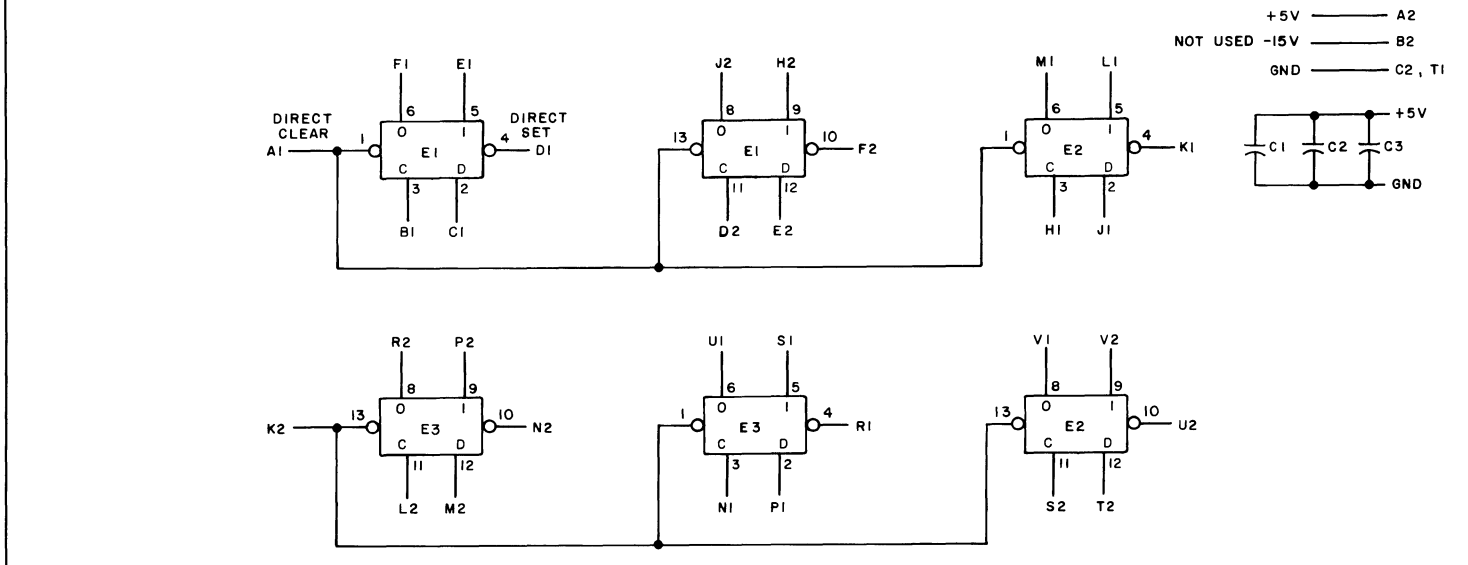
INPUTS: D inputs present 1 unit load each.
C inputs present 2 unit loads each.
CLEAR inputs present 3 unit loads per connected flip-flop.
SET inputs present 2 unit loads each.

OUTPUTS: Each output is capable of driving 10 unit loads.

POWER: Power dissipation of the M216 module is 5V at 87 mA (maximum).

A common clear line for all six flip-flops can be obtained by externally wiring pins A1 and K2 together.

CAUTION
The loading of each CLEAR line is calculated on the basis of 3 unit loads per flip-flop.



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
PARTS LIST		
	PARTS LIST	A-PL-M216-0-0
C1 THRU C3	CAP. .01 MFD 100V 20% DISC	1001610
E1 THRU E3	INTEGRATED CKT. DEC7474N	1905547

REVISIONS	CHK	CHG NO	REV
		6806	A
		00001	B

DRN	M. Waller	DATE 4-15-67
CHK'D		DATE
ENG		DATE
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE: SIX FLIP-FLOPS M216

SIZE	CODE	NUMBER	REV
B	CS	M216-0-1	B

PRINTED CIRCUIT REV C

M218
MQ Register

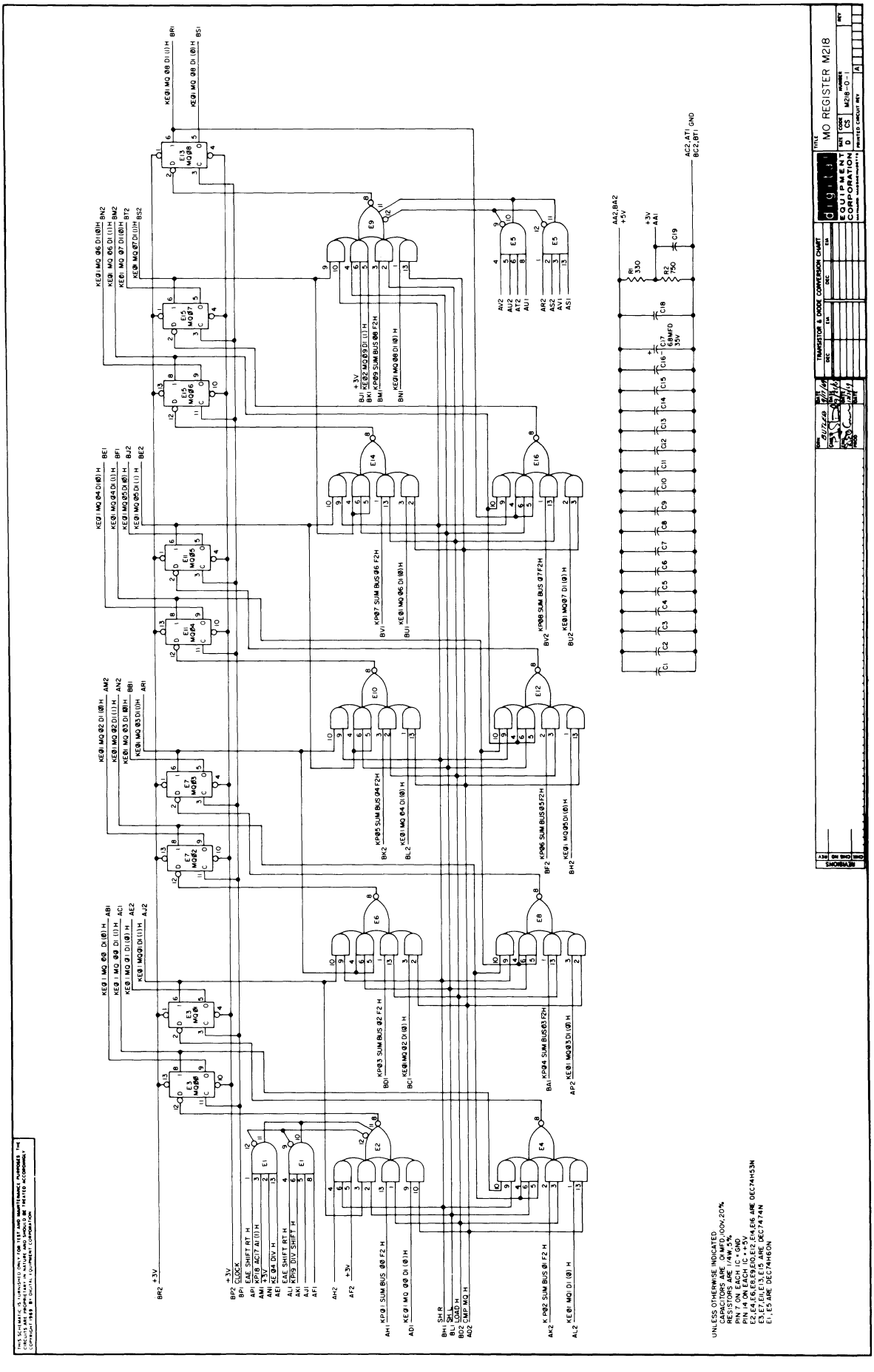
The M218 module contains a 9-bit storage register with input gating and shifting logic. Two M218 modules are used in the PDP-15 central processor equipped with the EAE option to form the 18-bit MQ register. (Refer to Engineering Drawings D-BS-KE15-0-1 and D-BS-KE15-0-2.) This register extends the AC shifter (M227), facilitating high-speed arithmetic operations (shifting, normalizing, division, and multiplication) and double-precision results.

The following are the input, output, and power characteristics of the M218 module.

INPUTS: All inputs but the CLOCK input present 1.25 TTL unit loads. The CLOCK input presents 18 unit loads.

OUTPUTS: Each output is capable of driving 10 TTL unit loads.

POWER: Power dissipation of the M218 module is 5V at 310 mA (maximum).


MQ REGISTER M218
DIGITAL EQUIPMENT CORPORATION
M218-0
TRANSITION & DIODE CONFORMATION CHART
UNLESS OTHERWISE INDICATED
CAPACITORS ARE .01 MFD 100V ±20%
RESISTORS ARE 1/4W ±5%
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E2, E4, E6, E8, E9, E10, E12, E14, E16 ARE DEC74H53N
E3, E7, E11, E13, E15 ARE DEC7474N
E1, E5 ARE DEC74H60N

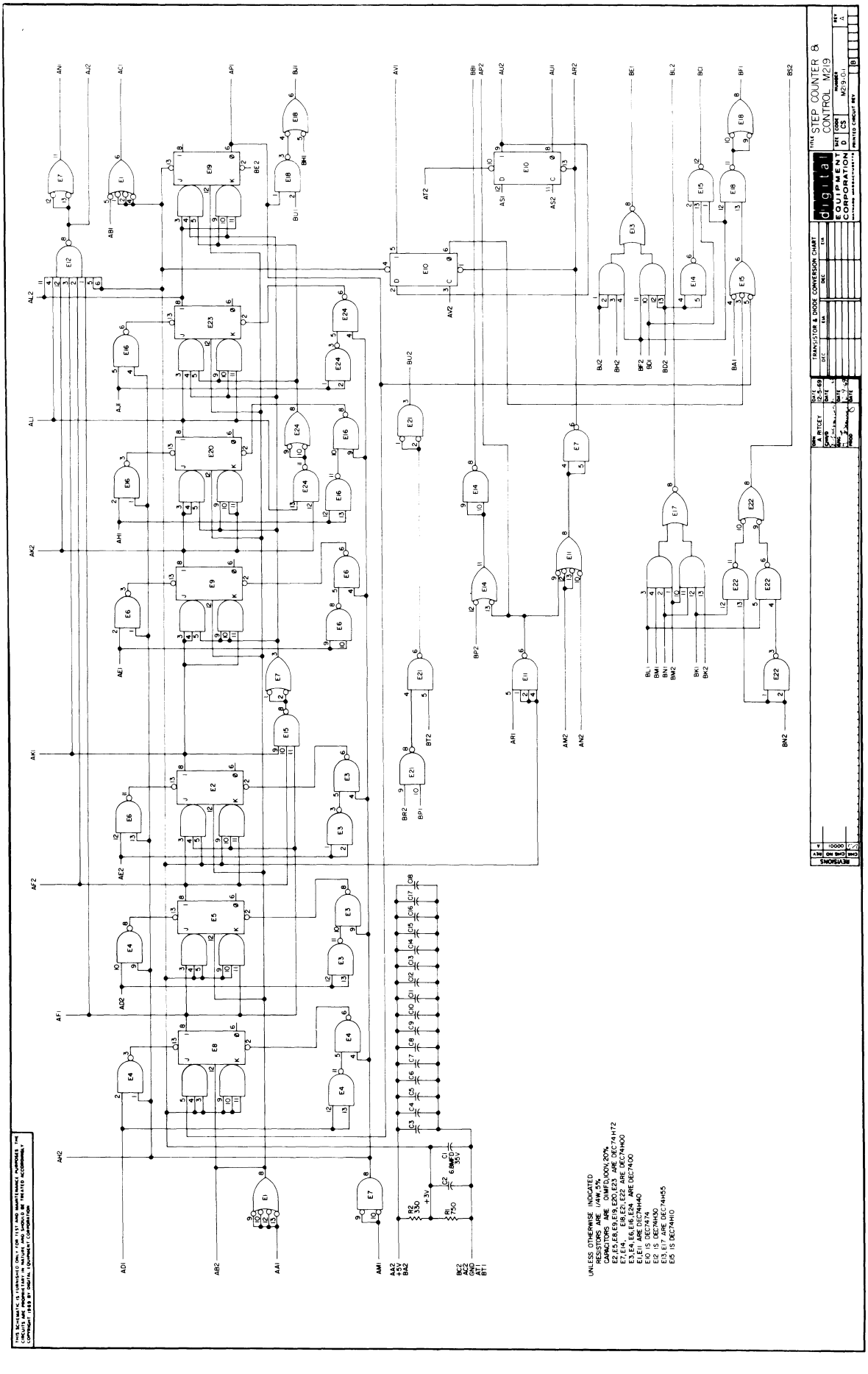
M219
Step Counter and Control

The M219 module contains a 7-bit synchronous step counter with input gating and EAE control logic. One of these modules is used in the PDP-15 central processor equipped with the EAE option. (Refer to Engineering Drawing D-BS-KE15-0-3.)

The following are the input, output, and power characteristics of the M219 module.

INPUTS AND OUTPUTS: Both inputs and outputs are standard TTL levels.

POWER: Power dissipated in the M219 module is 5V at 540 mA (maximum).


STEP COUNTER & CONTROL M219
digital
EQUIPMENT CORPORATION
M219-0-1
TRANSISTOR & DIODE CONVERSION CHART
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01MFD, 100V, 20%
E1 IS DEC74H00 E2, E3 ARE DEC74H72
E7, E8, E9, E18, E21, E22 ARE DEC74H00
E3, E4, E6, E16, E24 ARE DEC7400
E11, E11 ARE DEC74H40
E10 IS DEC7474
E13 IS DEC74H20
E14, E17 ARE DEC74H55
E15 IS DEC74H10

M223
MA and MB Registers

The M223 module contains two 4-bit registers with input gating logic. Five of these modules are used to form the 18-bit memory buffer (MB) register and the 13-bit memory address (MA) register that are used in each memory bank of the PDP-15. (Refer to Engineering Drawings D-BS-MM15-0-3 through D-BS-MM15-0-5.) The MA register receives the memory cell address from the central processor or the I/O processor and selects a specific core location. The data or instruction word to be read from or written into the specified core location travels through the MB register to or from the central processor and the I/O processor.

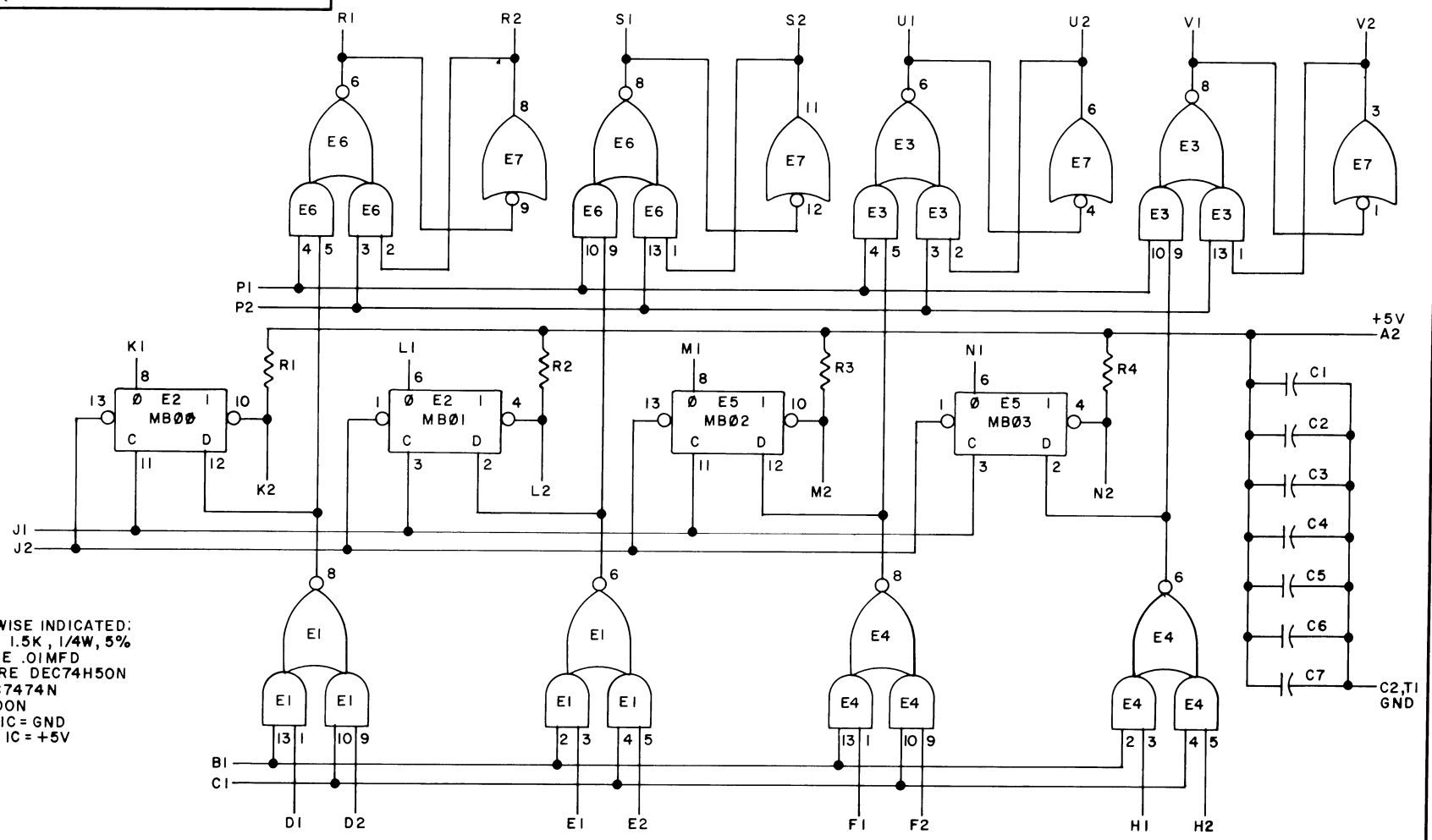
The following are the input, output, and power characteristics of the M223 module.

INPUTS: All input connections and the TTL unit loading they present are shown below.

Name	Pin	Loading
MDL	D2, E2, F2, H2	1 each
MB LOAD	J1	8
MB CLEAR	J2	12
MA LOAD	P1	4
MA HOLD	P2	4
SA (MB D SET)	K2, L2, M2, N2	2 each

OUTPUTS: Each MB output (pins K1, L1, M1, and N1) is capable of driving 9 unit loads. Each MA output (pins R1, R2, S1, S2, U1, U2, V1, and V2) is capable of driving 10 unit loads.

POWER: Power dissipation of the M223 module is 5V at 175 mA (maximum).



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1.5K, 1/4W, 5%
CAPACITORS ARE .01MFD
E1, E3, E4, E6 ARE DEC74H50N
E2, E5 ARE DEC7474N
E7 IS DEC74H00N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REVISIONS	REV.	CHG NO	CHK
	C	00001	

DRN. M Keller	DATE 5-7-69	
CHK'D G Gunyon	DATE 5-8-69	
ENG. DC Conner	DATE 7/17/69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MA MB REGISTER M223

SIZE	CODE	NUMBER	REV.
B	CS	M223-0-1	C

PRINTED CIRCUIT REV. B

DEC FORM NO. DRB 102

DIST 324, 439, 435² 4 PINK

M223-2

M226
Register

The M226 module contains seven storage flip-flops providing 1 bit of storage for each of the following registers:

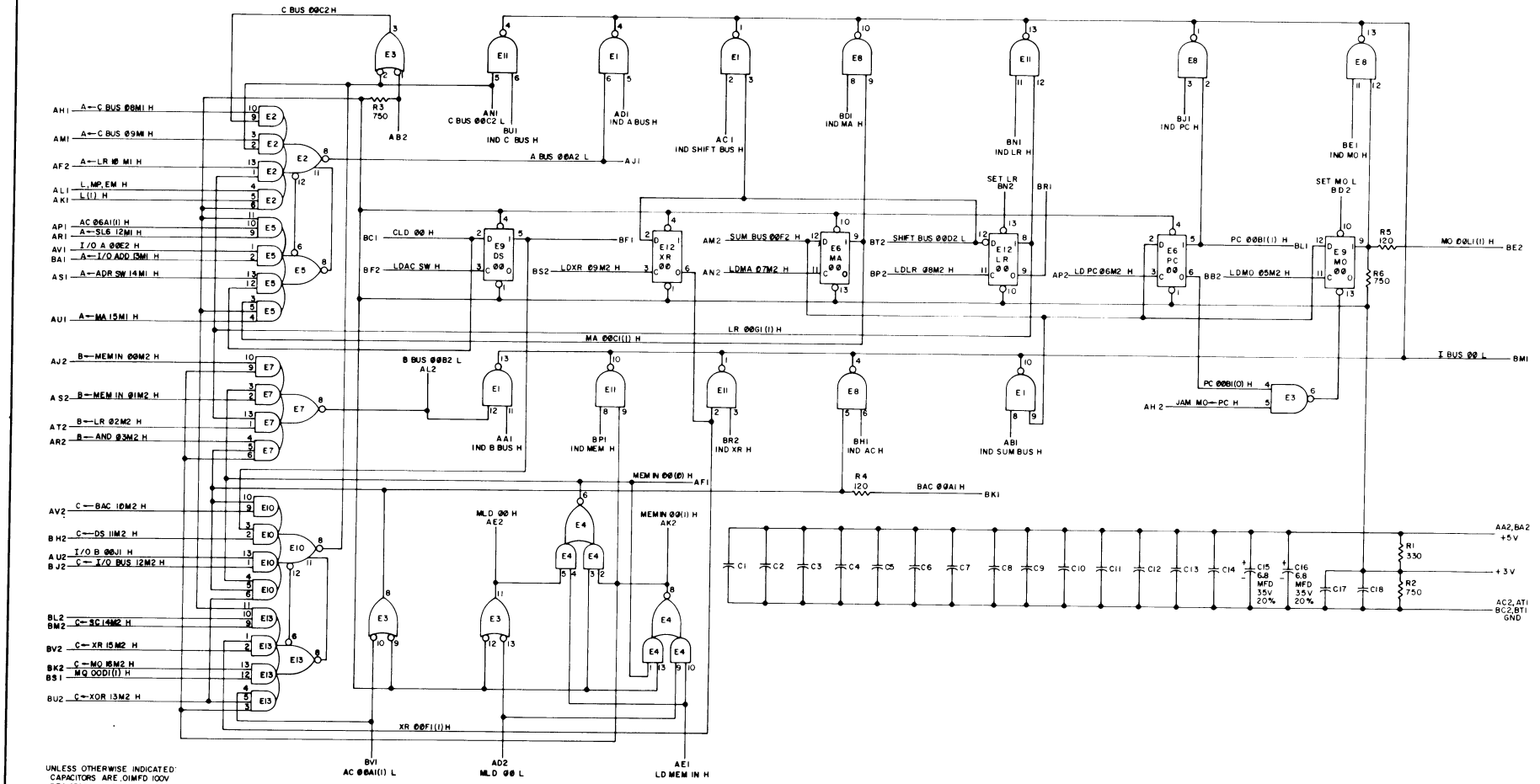
1. Data Switch (DS)
2. Index (XR)
3. Memory Address (MA)
4. Limit (LR)
5. Program Counter (PC)
6. Output Buffer to Memory (MO)
7. Memory Input (MI)

Eighteen M226 modules are used to form the registers in the central processor of the PDP-15. The registers require an 18-bit capacity. (Refer to Engineering Drawings D-BS-KP15-0-1 through D-BS-KP15-0-18.) Mixer-type logic for A bus, B bus, C bus, and I bus gating is also included on the M226 module.

The following are the input, output, and power characteristics of the M226 module.

INPUTS AND OUTPUTS: Inputs and outputs are standard TTL levels except for pin BM1, which is an open-collector output capable of sinking 16 mA (maximum).

POWER: Power dissipation of the M226 module is 5V at 260 mA (maximum).



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD 100V
RESISTORS ARE 1/4W 5%
PIN 7 ON EACH IC=GND
PIN 14 ON EACH IC=+5V
E1, E8, E11 ARE DEC7401N
E2, E7, E10 ARE DEC74H53N
E3 IS DEC74H00N
E4 IS DEC74H51ON
E5, E13 ARE DEC74H62N
E6, E9, E12 ARE DEC7474N

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: REGISTER MODULE M226

SIZE D | CODE CS | NUMBER M226-0-1 | REV A

PRINTED CIRCUIT REV

M226-2

M227
AC Shifter

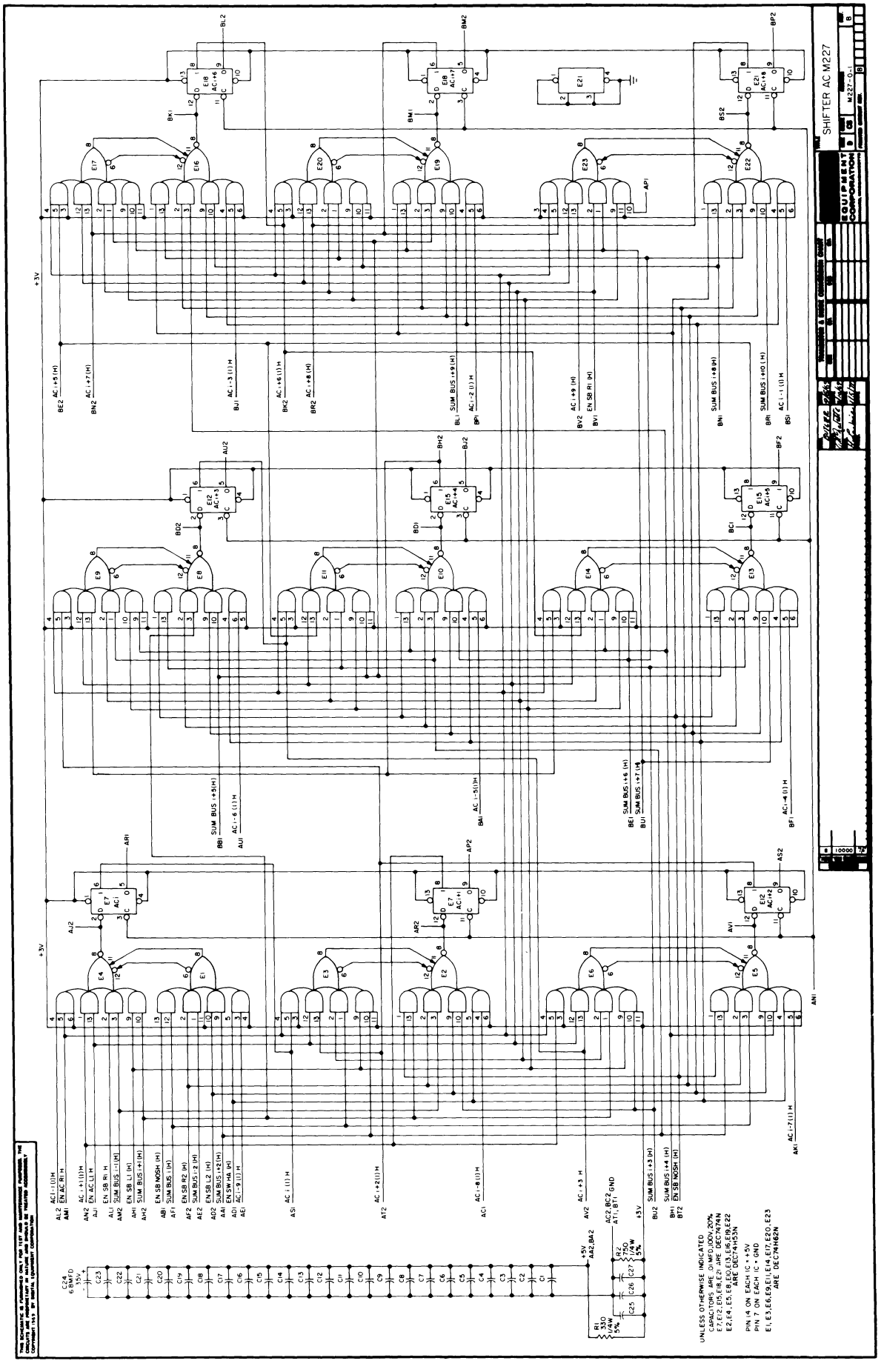
The M227 module contains 9 bits of the accumulator with input gating and shifting logic. Two of these modules are used in the central processor of the PDP-15 to form the 18-bit accumulator (AC) shift register. (Refer to Engineering Drawings D-BS-KP15-0-1 through D-BS-KP15-0-18.) The register is used for manipulating data and temporarily storing results of arithmetic/logical operations.

The following are the input, output, and power characteristics of the M227 module.

INPUTS: All inputs but the CLOCK input present 1.25 TTL unit loads. The CLOCK input presents 18 unit loads.

OUTPUTS: Each output is capable of driving 10 TTL unit loads.

POWER: Power dissipation of the M227 module is 5V at 420 mA (maximum).


SHIFTER AC M227
EQUIPMENT CORPORATION
M227-1(A)
UNLESS OTHERWISE INDICATED
CAPACITORS ARE .01 MFD, 100V, 20%
E7, E12, E15, E18, E21 ARE DEC 74174
E2, E4, E5, E8, E10, E13, E16, E19, E22
ARE DEC 74H52N
E1, E3, E6, E9, E11, E14, E17, E20, E23
ARE DEC 74H62N
PIN 14 ON EACH IC = +5V
PIN 7 ON EACH IC = GND
+3V
+5V
SUM BUS +1 (H)
SUM BUS +2 (H)
SUM BUS +3 (H)
SUM BUS +4 (H)
SUM BUS +5 (H)
SUM BUS +6 (H)
SUM BUS +7 (H)
SUM BUS +8 (H)
SUM BUS +9 (H)
SUM BUS +10 (H)
EN SB M2SH (H)
EN SB R1 (H)
EN SB R2 (H)
EN SB L (H)
EN AC R1 (H)
EN AC L (H)
EN SUM BUS -1 (H)
EN SUM BUS -2 (H)
EN SUM BUS +1 (H)
EN SUM BUS +2 (H)
AC(-1) H
AC(-2) H
AC(-3) H
AC(-4) H
AC(-5) H
AC(-6) H
AC(-7) H
AC(-8) H
AC(-9) H
AC(-10) H
AC(+1) H
AC(+2) H
AC(+3) H
AC(+4) H
AC(+5) H
AC(+6) H
AC(+7) H
AC(+8) H
AC(+9) H
AC(+10) H
AC2, BC2 GND
AT1, BT1 GND
R1 330 1/4W 5%
R2 750 1/4W 5%
C24 6.8MFD 15V
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23
C25 C26 C27

M238
Synchronous Up/Down Counter

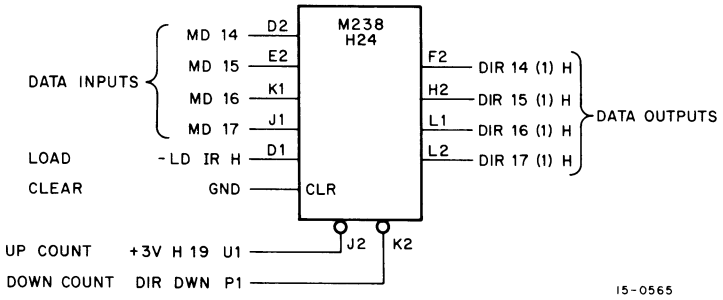
The M238 Synchronous Up/Down Counter consists of two DEC74193 4-bit synchronous up/down counter integrated circuits. The M238 is used in the EPA, DIR, and DAR registers of the FP15 Floating-Point Processor, where the counters are connected to provide eight bit counting capability.

Synchronous operations is provided by clocking all flip-flops in the counter simultaneously so that the outputs change in coincidence with each other. The flip-flops are master-slave flip-flops and the outputs are triggered by a positive-going transition of either of two clock inputs. One clock input is designated U (up count) and the other is designated D (down count). The direction of counting is determined by pulsing one clock input while the opposite clock input is kept high.

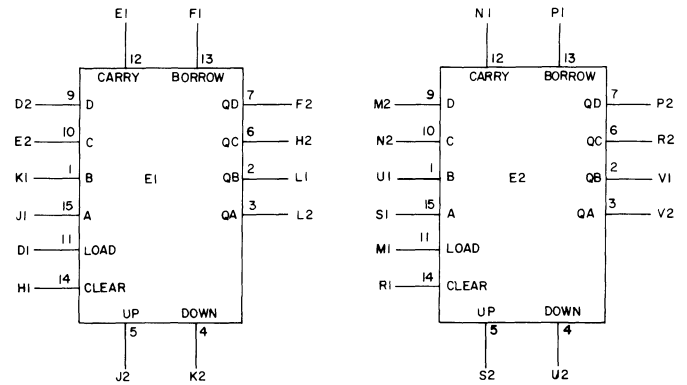
The outputs of the flip-flops may be preset to any state by entering the data at the data inputs while the load input (L) is low. The output will change to reflect the input, regardless of the clock pulses. The clear input is provided to clear all flip-flops, independent of the clock and load inputs.

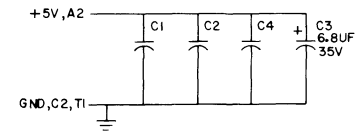
Both the borrow and carry outputs are available for cascading the up-counting and down-counting operations. When counter underflow occurs, the borrow output produces the same width pulse as the down-count input. When counter overflow occurs, the carry output produces the same width pulse as the up-count input. Cascading is accomplished by applying the borrow and carry inputs to the down-count and up-count inputs of the next counter.

In the example of the DIR register, the UPCOUNT input is inhibited by +3V, indicating that the DIR can only be decremented.



SIZE	CODE	NUMBER	REV
B	CS	M238-0-1	C





UNLESS OTHERWISE INDICATED:
E1, E2 ARE DEC74193
PIN 8 = GND ON E1, E2
PIN 16 = +5V
CAPACITORS ARE .01UF, 100V, 20%

REVISIONS	CHK	CHG NO	REV
		00001	C

DRN	NANCY MOORE	DATE 8/21/70
CHK'D		DATE 10/15/70
ENG		DATE 10/23/70
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE 2-SYNCHRONOUS 4 BIT UP/DOWN CONVERTERS M238

SIZE	CODE	NUMBER	REV
B	CS	M238-0-1	C

PRINTED CIRCUIT REV. D

DEC FORM NO.
DRB 102

DIST. 324, 434, 435 4.1 PINK

M240
R-S Flip-Flops

The M240 module contains six R-S-type flip-flops. Each flip-flop consists of two NAND gates with cross-coupled outputs. Two inputs are provided for setting the flip-flops, and one input is provided for resetting the flip-flops. The following truth table defines the operation of the flip-flops. When the SET output (F1) is HIGH, both of the SET inputs (C1 and B1) are HIGH. When the SET output is LOW, either one or both SET inputs are LOW.

Previous State		Input Condition		Result	
1	0	SET	RESET	1	0
L	H	L	H	H	L
H	L	H	L	L	H
L	H	H	H	No Change	
H	L	H	H	No Change	
H	L	L	H	No Change	
L	H	H	L	No Change	
L	H	L	L	H	H*
H	L	L	L	H	H*

*Ambiguous state: In practice, the input that stays low longest assumes control.

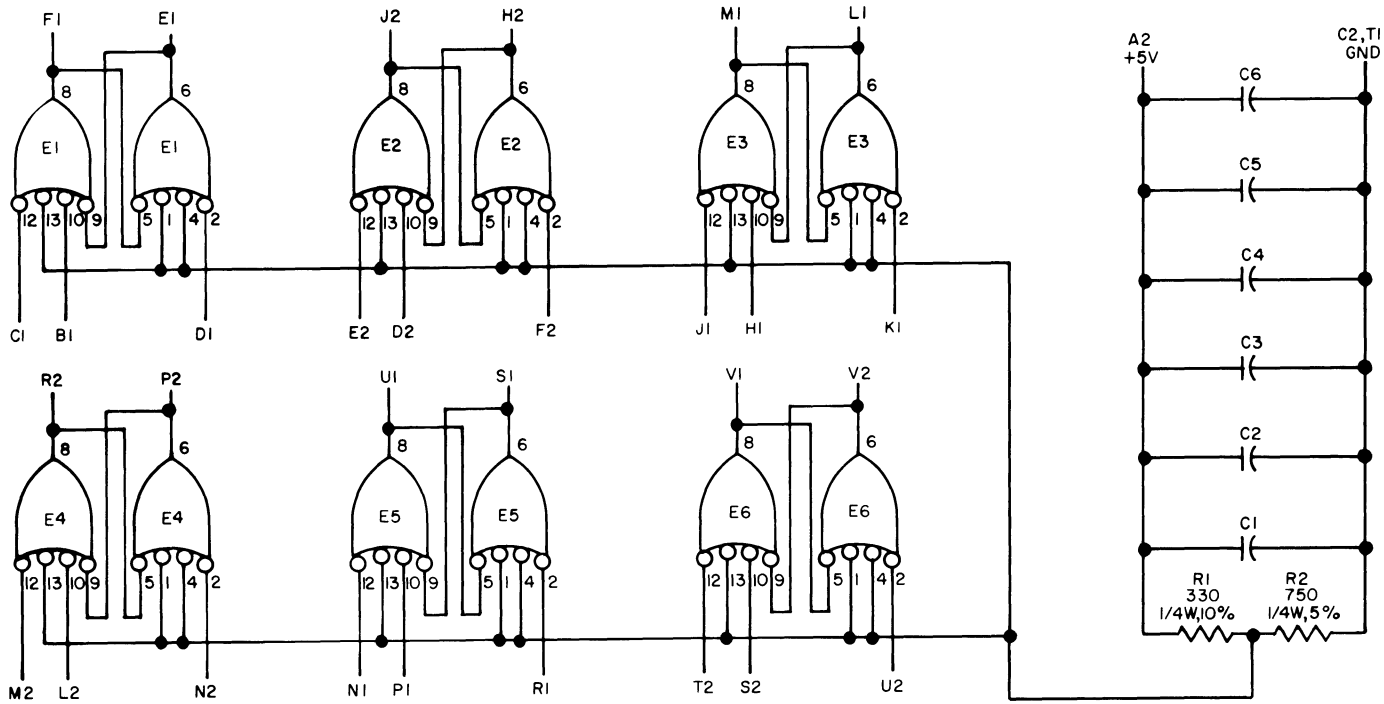
Propagation delay time from SET or RESET to logical 1 (HIGH) level output is 10 ns (maximum). Propagation delay time from SET or RESET to logical 0 (LOW) level output is 20 ns (maximum).

The following are the input, output, and power characteristics of the M240 module.

INPUTS: Each input presents 1.25 TTL unit loads.

OUTPUTS: Each output is capable of driving 34 TTL unit loads.

POWER: Power dissipated in the M240 module is 5V at 185 mA.



UNLESS OTHERWISE INDICATED:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
CAPACITORS ARE .01MFD 100V
E1,E2,E3,E4,E5,E6 ARE 74H40N

REVISIONS		
CHK	CHG NO	REV.
	00001	B

DRN.	R. BUTLER	DATE 4/11/69
CHK'D	M. Manchester	DATE 4/15/69
ENG.	[illegible]	DATE 4/15/69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: 6 R/S FLIPFLOPS M240

SIZE	CODE	NUMBER	REV.
B	CS	M240-0-1	B

PRINTED CIRCUIT REV. B

DEC FORM NO.
DRB 102

5 PINK DIST 32H, 43H, 43S 3

M240-2

SIZE B | CODE CS | NUMBER M240-0-1 | REV. B

M242
J-K Flip-Flops

The M242 module contains three J-K flip-flops augmented by multiple-input AND gates for general use as gated control flip-flops or buffers. A truth table for the clocked set and reset conditions appears below. The J or K inputs are HIGH when the three inputs to their corresponding AND gate are HIGH; otherwise, they are LOW. Note that when the J and K inputs are both HIGH, the flip-flop complements on each CLOCK pulse.

Starting Condition (Output)		Input Condition		Result at End of Standard CLOCK Pulse (Output)	
1	0	J	K	1	0
L	H	L	L	No Change	
		L	H	No Change	
		H	L	H	L
		H	H	H	L
H	L	L	L	No Change	
		L	H	L	H
		H	L	No Change	
		H	H	L	H

The J and K inputs must be stable during the leading edge threshold of a standard CLOCK input and must remain stable during the positive state of the CLOCK. The J and K inputs do not have to remain stable after the CLOCK pulse reaches its trailing edge threshold (negative-going voltage). The minimum width of the CLOCK pulse should be 12 ns.

Application of a LOW level to the R input for at least 16 ns resets the flip-flop unconditionally. Application of a LOW level to the 5 input for at least 16 ns sets the flip-flop unconditionally. Propagation delay time to logical 1 level (HIGH) from trailing edge of the CLOCK pulse to output is 21 ns (maximum). Propagation delay time to logical level (LOW) from trailing edge of the CLOCK pulse to output is 27 ns (maximum).

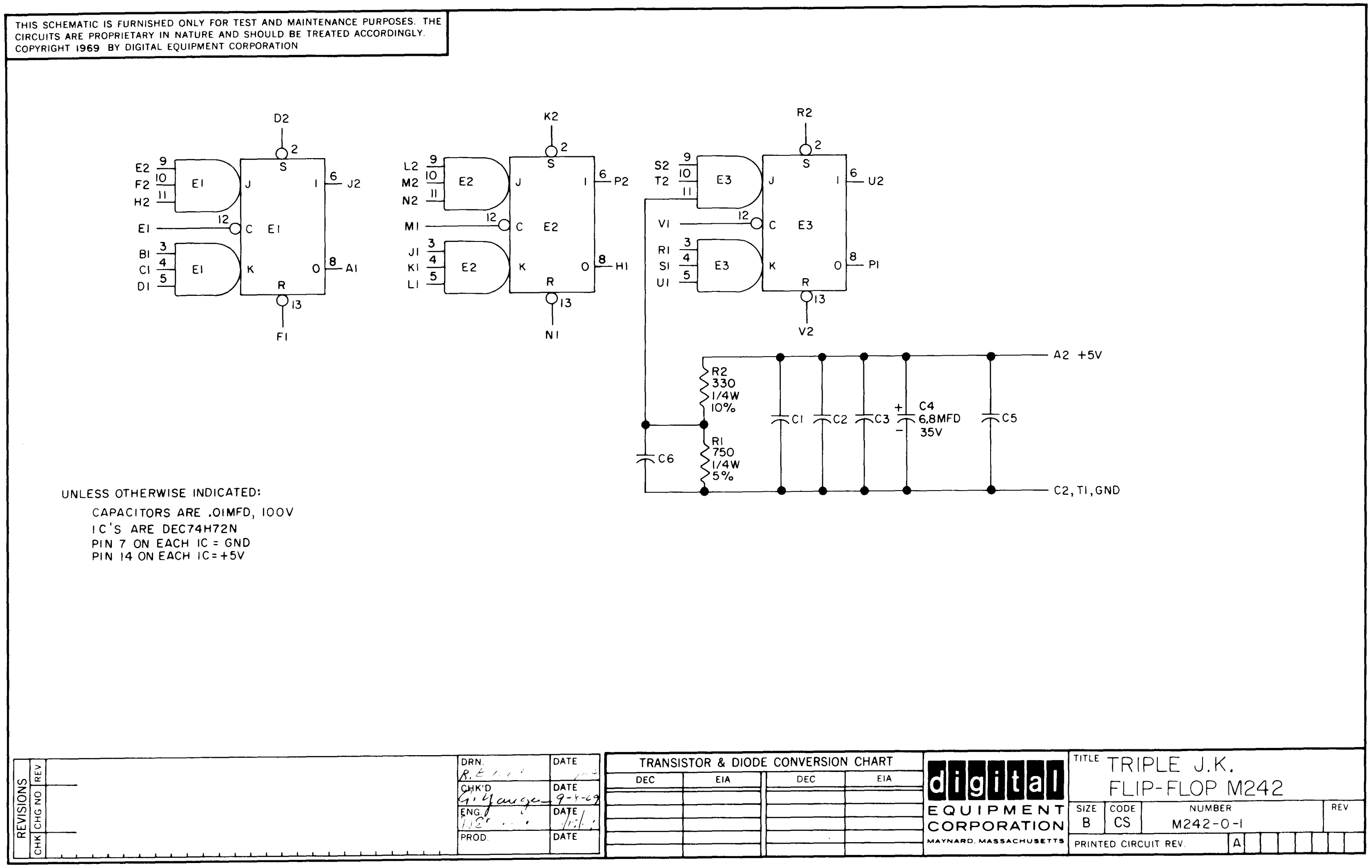
Propagation delay time to logical 1 level (HIGH) from S and R input to output is 12 ns (maximum). Propagation delay time to logical 0 level (LOW) from S and R input to output is 24 ns. Maximum clock frequency is 24 MHz.

The following are the input, output, and power characteristics of the M242 module.

INPUTS: All inputs but the S and R input present 1.25 TTL unit loads. The S and R input presents 2.5 unit loads.

OUTPUTS: Each output is capable of driving 12 unit loads.

POWER: Power dissipation of the M242 module is 5V at 90 mA (maximum).

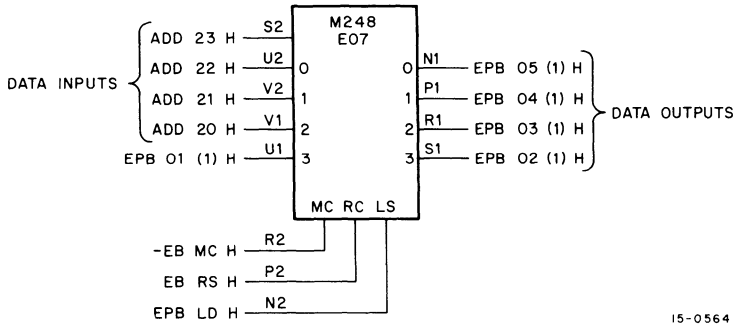

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY. COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION
D2
E2
F2
H2
E1
B1
C1
D1
J2
A1
F1
K2
L2
M2
N2
M1
J1
K1
L1
P2
H1
N1
R2
S2
T2
V1
R1
S1
U1
U2
P1
V2
A2 +5V
R2 330 1/4W 10%
R1 750 1/4W 5%
C1
C2
C3
C4 6.8MFD 35V
C5
C6
C2, T1, GND
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD, 100V
IC'S ARE DEC74H72N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
REVISIONS
CHK
CHG NO
REV
DRN.
CHK'D
ENG.
PROD.
DATE
9-4-69
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE TRIPLE J.K. FLIP-FLOP M242
SIZE B
CODE CS
NUMBER M242-0-1
REV
PRINTED CIRCUIT REV. A

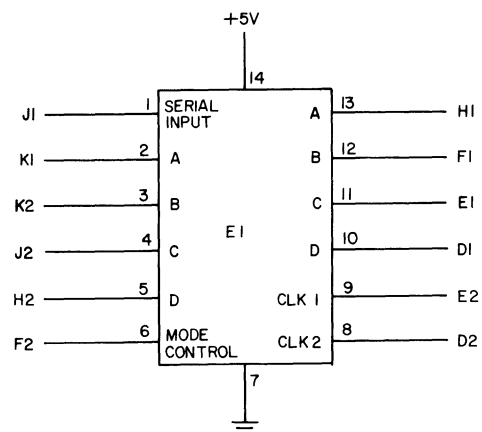
M248
Right Shift Parallel Load Register

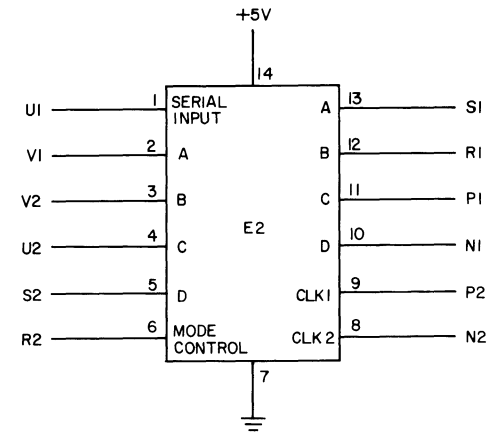
The M248 Right Shift Parallel Load Register consists of two DEC7495 Right Shift, Parallel Load Register integrated circuits. The M248 is used in the EPB, FMA, FMB, and FMQ registers in the FP15 Floating-Point Processor. The modules are connected to allow right-shifting between four-bit sections so that each module is capable of handling eight bits. A sample FP15 Floating-Point Processor application is shown in the illustration.

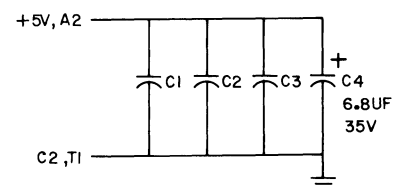
When a logic 0 input is applied to the mode control (MC) input, the output of each flip-flop is applied to the succeeding flip-flop. The right shift operation is performed by clocking at the RS input. During this time, the left-shift (LS) input is inhibited.

When a logic 1 input is applied to the mode control input, the flip-flops are decoupled to prevent right shift and parallel inputs are loaded when the LS input is clocked. The register can be configured for left-shift operations by connecting the output of each flip-flop to the parallel input of the preceding flip-flop.









UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01UF, 100V, 20%
IC'S ARE DEC7495

M248-2

REVISIONS	REV	CHG NO	CHK

DRN. C. Wyatt	DATE 10-28-70	
CHK'D	DATE 11-3-70	
ENG. J. Holmes	DATE 5/4/71	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 4-BIT RT SHIFT PARALLEL LD REG (DUAL) M248

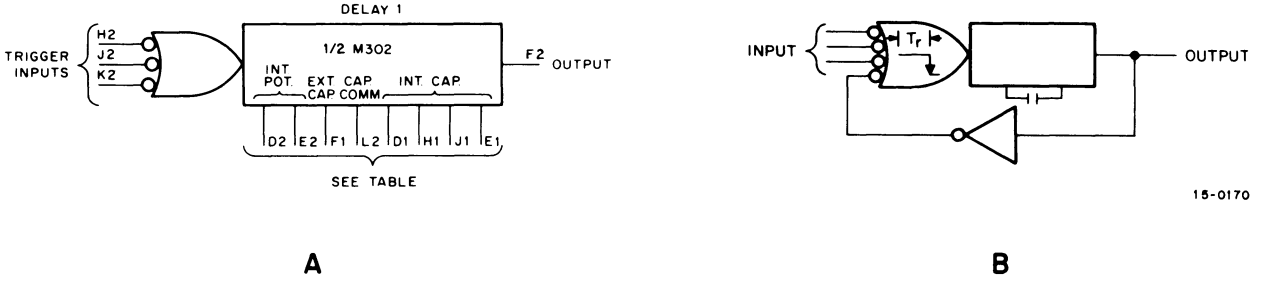
SIZE	CODE	NUMBER	REV
B	CS	M248-0-1	A

PRINTED CIRCUIT REV. B

DEC FORM NO
DRB 102

M302
Dual Delay Multivibrator

The M302 contains two delays (one-shot multivibrators, see Figure A) that are triggered by a level change from HIGH to LOW, or by a pulse to LOW whose duration is equal to or greater than 50 ns. When the input is triggered, the output changes from LOW to HIGH for a predetermined length of time and then returns to LOW. The basic delay range is determined by an internal capacitor. The delay range can be increased by selection of additional capacitance, which is available by connecting various module pins or by the addition of external capacitance. An internal potentiometer can be connected for fine delay adjustments within each range, or an external resistance can be used. If an external resistance is used, the combined resistance of the internal potentiometer and the external resistance should be limited to 10,000Ω.



M302 Simplified Diagram

The fall-time of the input trigger should be less than 400 ns.

The delay time is adjustable from 50 ns to 7.5 ms using the internal capacitors and can be extended by adding an external capacitor.

Care should be exercised in the selection of external capacitors to assure low leakage because leakage affects the time delay.

Recovery time is determined by the size of the capacitance used. The minimum recovery time of the M302 module is 30 ns when no additional capacitance is used. Recovery time with additional capacitance can be calculated by using the following formula:

$T_r = 300\ C$ Where T_r is in seconds and C is in farads

Recovery time is defined for this module as follows: Recovery time (T_r) is the minimum time interval that must exist before each trigger, with all inputs HIGH and the output LOW. The table below illustrates these conditions.

Delay Range	Capacitor Value	Interconnections Required	
		Delay 1	Delay 2
50 ns - 750 ns	100 pf (internal)	None	None
500 ns - 7.5 μs	1000 pf (internal)	D1 - L2	N1 - S2
5 μs - 75 μs	0.01 uf (internal)	H1 - L2	S1 - S2
50 μs - 750 μs	0.10 uf (internal)	J1 - L2	U1 - S2
500 μs - 7.5 ms	1.0 uf (internal)	E1 - L2	P1 - S2
Above 7.5 ms	Add external capacitors between specified pins		

For adjustable delays (D2 - E2 and V2 - R2), connect the pins to the internal adjustment potentiometer. Without a potentiometer, the delay will not recover. An external potentiometer of less than 10 KΩ can be used by connecting the potentiometer between E2 or R2 and ground pin C2. Use of an external adjustment resistor causes some increase in jitter. It is recommended that the leads to an external potentiometer be twisted pairs and be made as short as possible.

The following are the input, output, and power characteristics of the M302 module.

INPUTS: Each input presents 2.5 unit loads.

OUTPUTS: Each output is capable of driving 25 unit loads.

POWER: Power dissipation of the M302 module is +5V at 166 mA (maximum).

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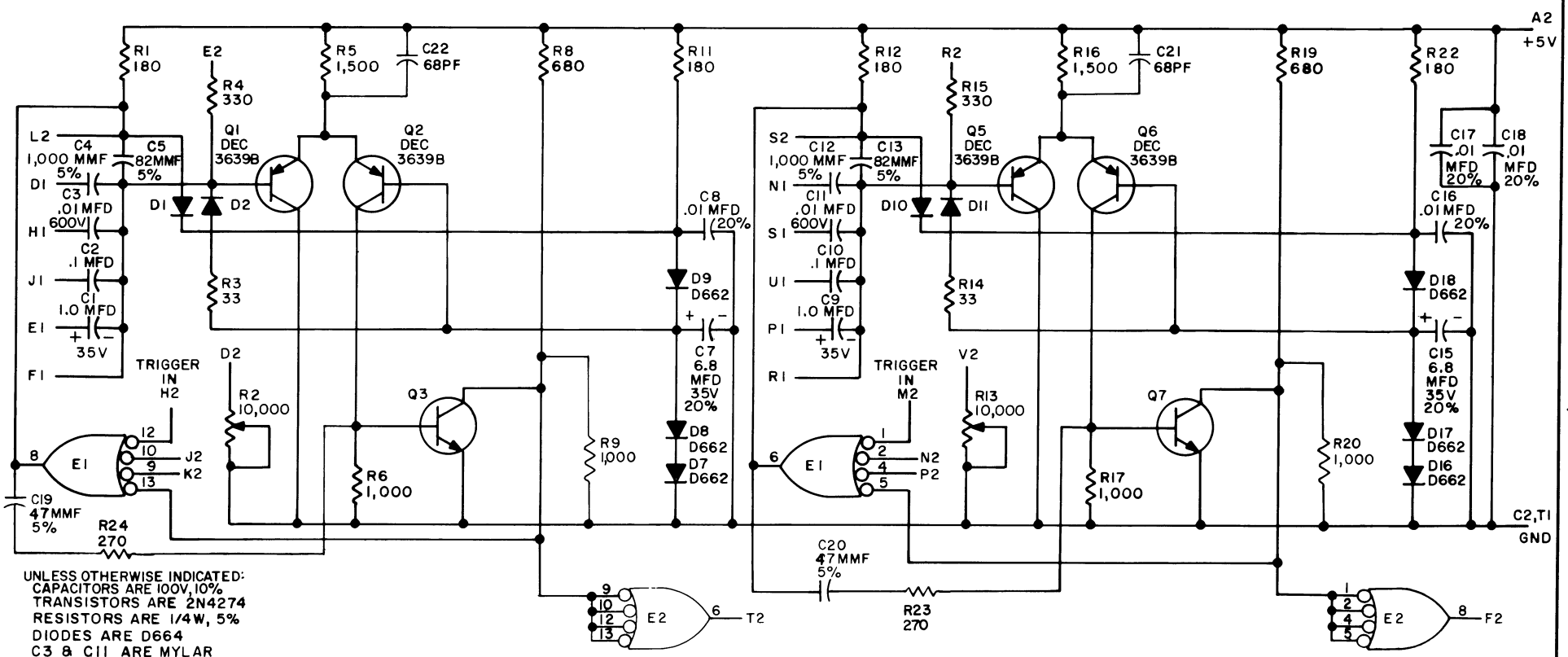


UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 100V, 10%
TRANSISTORS ARE 2N4274
RESISTORS ARE 1/4W, 5%
DIODES ARE D664
C3 & C11 ARE MYLAR
E1 IS DEC74H40N
PIN 7 ON IC'S = GND
PIN 14 ON IC'S = +5V
R2 & R13 ARE HELITRIM POT #78PR
1.0MFD CAPACITORS ARE TANTALUM
E2 IS DEC7413N

PARTS LIST A-PL-M302-0-0

REVISIONS	REV.	CHG NO	CHK
	B	6507	
	C	6719	
	D		
	E	6881	
	F	7077	
	H	00001	
	J	00002	
	K	00003	
	L	00004	

DRN. M. Haller	DATE	6-15-67
CHK'D	DATE	6/21/67
ENG. L. White	DATE	6/21/67
PROD. 1	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
2N4274	SAME		
DEC3639B	2N3639		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: ONE SHOT DELAY M302

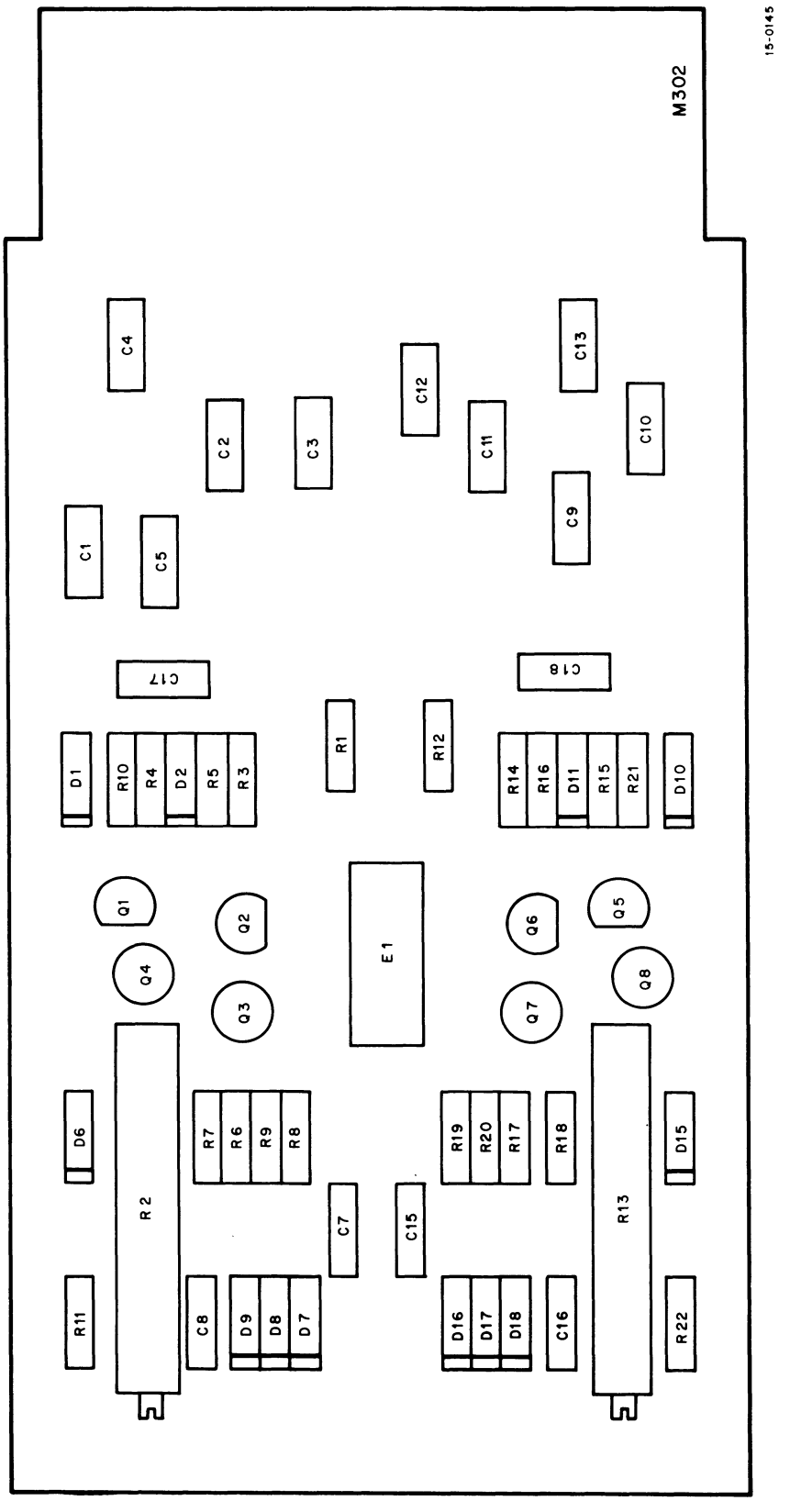
SIZE	CODE	NUMBER	REV.
B	CS	M302-0-1	L

PRINTED CIRCUIT REV. L

DIST. 324 434 435 4 PINK

DEC FORM NO. DRB 102

M302-4


M302
15-0145
C4
C2
C3
C12
C11
C13
C10
C1
C5
C9
C17
C18
R1
R12
D1
R10
R4
D2
R5
R3
R14
R16
D11
R15
R21
D10
Q1
Q2
E1
Q6
Q5
Q4
Q3
Q7
Q8
D6
R2
R7
R6
R9
R8
R19
R20
R17
R18
R13
D15
C7
C15
R11
C8
D9
D8
D7
D16
D17
D18
C16
R22

M311
Tapped Delay Lines

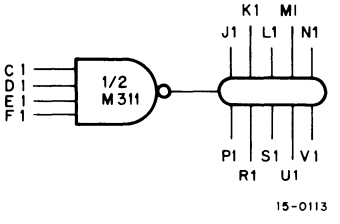
The M311 module contains two tapped delay lines. Each delay line has ten taps providing delays in 25 ns intervals from 25 ns through 250 ns (see simplified diagram). Pin J1 supplies the minimum delay of 25 ns and pin V1 supplies the maximum delay of 250 ns. The input NAND gate of the delay line provides an additional delay of 10 ns (maximum). Delay line tolerance is ±5%.

The following are the input, output, and power characteristics of the M311 module.

INPUTS: Each input presents 1.25 TTL unit loads.

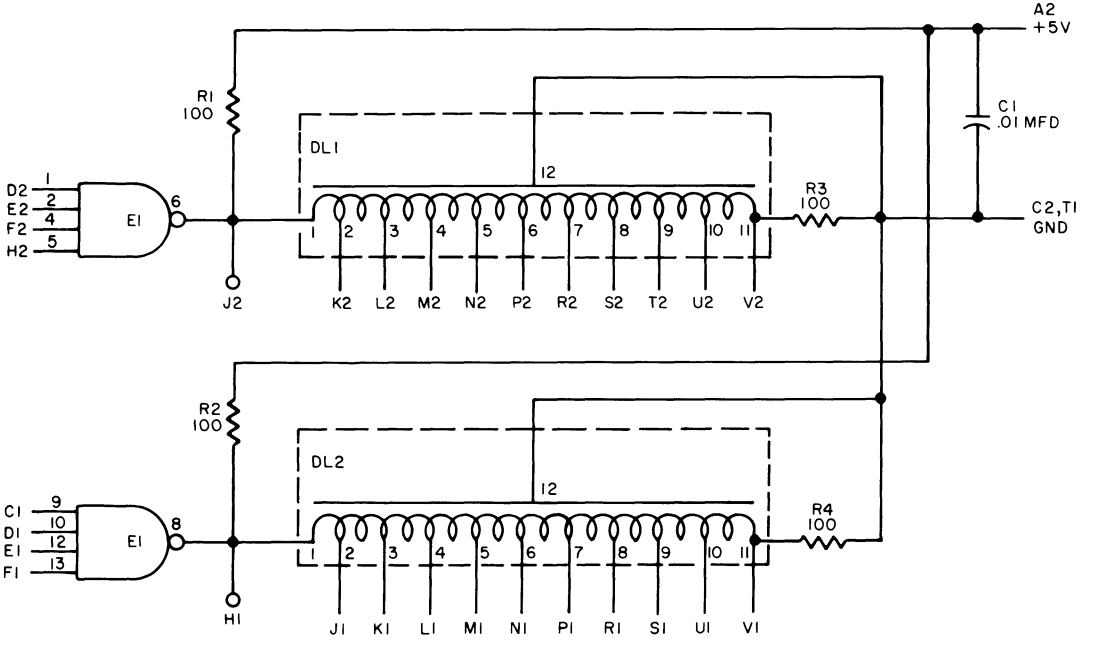
OUTPUTS: Each output is capable of driving 1.25 unit loads. Maximum driving capability of the delay line is 6 unit loads, with a maximum line length of 8 ns.

POWER: Power dissipation of the M311 module is 5V at 170 mA (maximum).



M311 Simplified Diagram

SIZE	CODE	NUMBER	REV.
B	CS	M311-0-1	B



UNLESS OTHERWISE INDICATED:

E1 IS DEC 74H40N
DELAYS ARE 0-250NS IN 25NS STEPS
RESISTORS ARE 1/4W 5%
PIN 14 ON IC = 5V
PIN 7 ON IC = GND

REVISIONS			
CHK	CHG NO.	REV.	
	00001	B	

DRN. R. BUTLER	DATE	4/2/69
CHK'D M. Mendoza	DATE	4/4/69
ENG. [illegible]	DATE	7/7/69
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: TAP DELAY M311

SIZE	CODE	NUMBER	REV.
B	CS	M311-0-1	B

PRINTED CIRCUIT REV. A

DEC FORM NO.
DRB 102

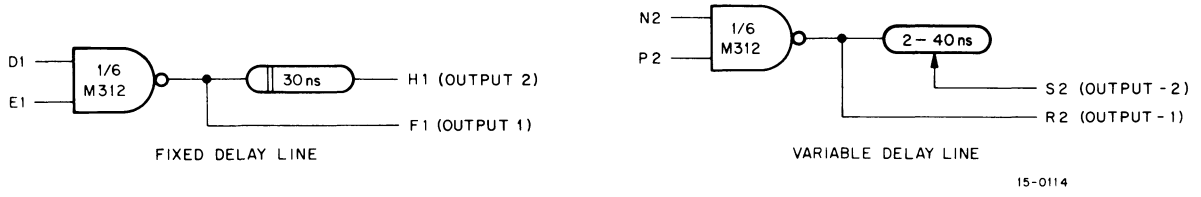
DIST 324, 434, 435 [illegible]

M312
Delay Lines

The M312 module contains six delay lines. Five of these delay lines have fixed delays with ±5% tolerance, and one is variable. Delays and output pins are as follows:

Delay (ns)	Output Pins	
	No. 1	No. 2
30	F1	H1
50	F2	H2
30	L1	M1
50	L2	M2
50	R1	S1
0-40	R2	S2

The input NAND gates of the delay lines provide an additional delay of 10 ns.



M312 Simplified Diagram

The following are the input, output, and power characteristics of the M312 module.

INPUTS: Each input presents 1.25 TTL unit loads.

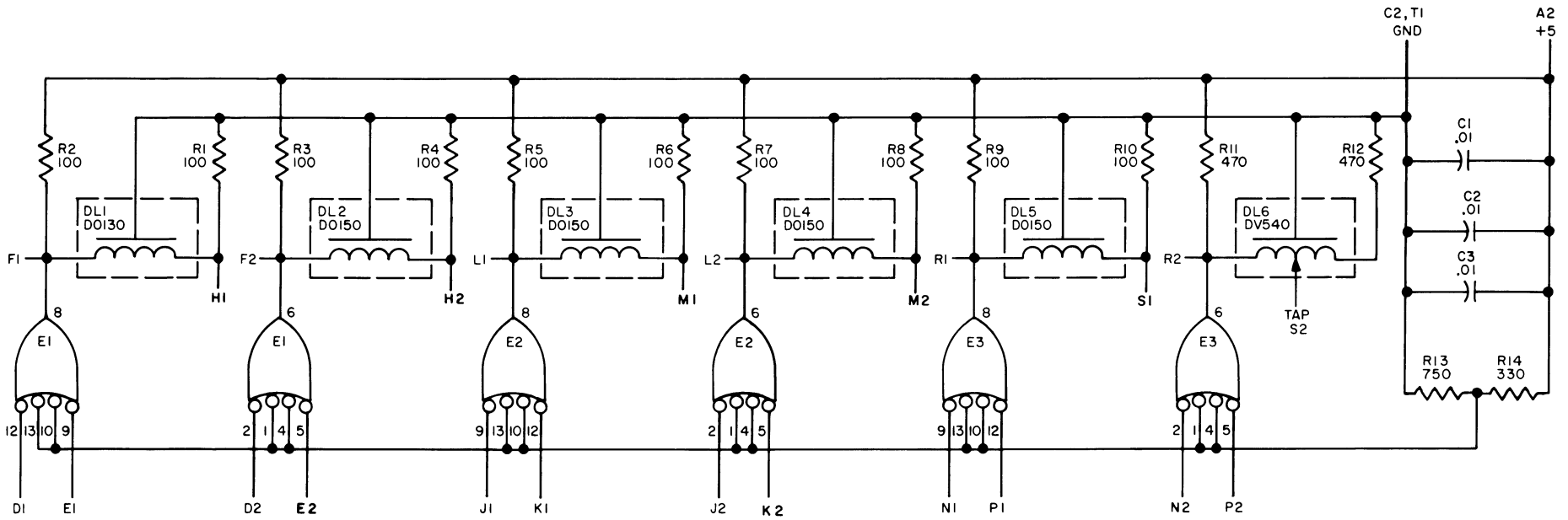
OUTPUTS: 30 ns delay lines - Each output of the 30 ns delay line is capable of driving 6 unit loads. However, the total number of unit loads on both outputs of the delay line should not exceed six.

50 ns lines - Output No. 1 of each 50 ns delay line is capable of driving 6 unit loads, and output No. 2 is limited to 4 unit loads. The total unit load capability of each delay line should not exceed 6 unit loads.

Variable delay line - Output No. 1 of the variable delay line is capable of driving 5 unit loads, and output No. 2 is limited to 1 unit load. The total unit load capability of this delay line should not exceed 5 unit loads.

POWER: Power dissipation of the M312 module is 5V at 275 mA (maximum).

SIZE	CODE	NUMBER	REV.
B	CS	M312-0-1	D



UNLESS OTHERWISE INDICATED:
IC'S ARE DEC 74H40N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
RESISTORS ARE 1/4W, 5%

M312-3

REVISIONS	CHK	CHG NO	REV.
		00001	B
		00002	C
		00003	D

DRN. B. BUTLER	DATE 4/2/69	
CHK'D M. Moorhead	DATE 4/3/69	
ENG DEO Cruz	DATE 4/5/69	
PROD	DATE 8/5/69	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE DELAY MODULE M312

SIZE	CODE	NUMBER	REV.
B	CS	M312-0-1	D

PRINTED CIRCUIT REV. C

DEC FORM NO.
DRB 102

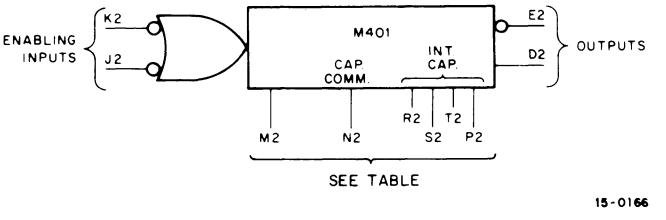
DIST. 324, 494, 435[3]

4 Pink

M401
Variable Clock

The M401 Variable Clock is a stable RC-coupled multivibrator that produces standard timing pulses at adjustable repetition rates.

The module is intended for use as the primary source of timing signals in a digital system. Repetition rate is adjustable from 175 Hz to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.



M401 Simplified Diagram

A 2-input OR gate input is provided for start-stop control of the pulse train. A level change from HIGH to LOW with fall time less than 400 ns is required to enable the clock.

Delay between enabling inputs and output pin E2 is 50 ns.

Frequency Range	Interconnections Required			
1.5 MHz to 10 MHz	(100 pF)		None	
175 kHz to 1.75 MHz	(1000 pF)	N2	-	R2
17.5 kHz to 175 kHz	(.01 μF)	N2	-	S2
1.75 kHz to 17.5 kHz	(0.1 μF)	N2	-	T2
175 Hz to 1.75 kHz	(1.0 μF)	N2	-	P2

Fine frequency adjustment is controlled by an internal potentiometer. No provision is made for any external connections.

External capacitance can be added by a connection between pin N2 and ground.

The M401 can also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision "E" or a later revision. The voltage applied to pin M should be limited to the range of 0V to +10V. This voltage swing allows the frequency to be shifted by approximately 30 percent in the frequency range, using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 μfd. If the voltage applied to pin M is dc or low frequency (below 1 KHz), pin M appears as a +1V source with a Thevenin resistance of 800Ω. Modulating the M401 with a 10V peak-to-peak signal about a center frequency, as derived by the application of a mean voltage of +5V to pin M, yields a typical frequency excursion of -0 in excess of ±15% about the center frequency. Typical frequency excursions that may be obtained are shown below.

Voltage (V) applied to Pin M	CAPACITOR			
	1.0 μfd	0.1 μfd	0.01 μfd	.001 μfd
0	1.000	10.00	100.0	1000
+1	1.054	10.49	104.6	1036
+2	1.101	10.94	109.2	1071
+3	1.147	11.39	113.6	1108
+4	1.193	11.83	118.0	1142
+5	1.238	12.26	122.2	1181
+6	1.282	12.69	126.4	1271
+7	1.325	13.10	130.4	1295
+8	1.368	13.50	134.2	1312
+9	1.408	13.87	137.7	1322
+10	1.443	14.20	140.9	1323
	Output frequency in kHz			

The following are the input, output, and power characteristics of the M401 module.

INPUTS: Each ENABLE input represents 1 unit load. For pin M, refer to above text.

OUTPUTS: The positive output can drive 10 unit loads; the negative output, 9 unit loads.

POWER: Power dissipation of the M401 module is +5V at 80 mA (maximum).

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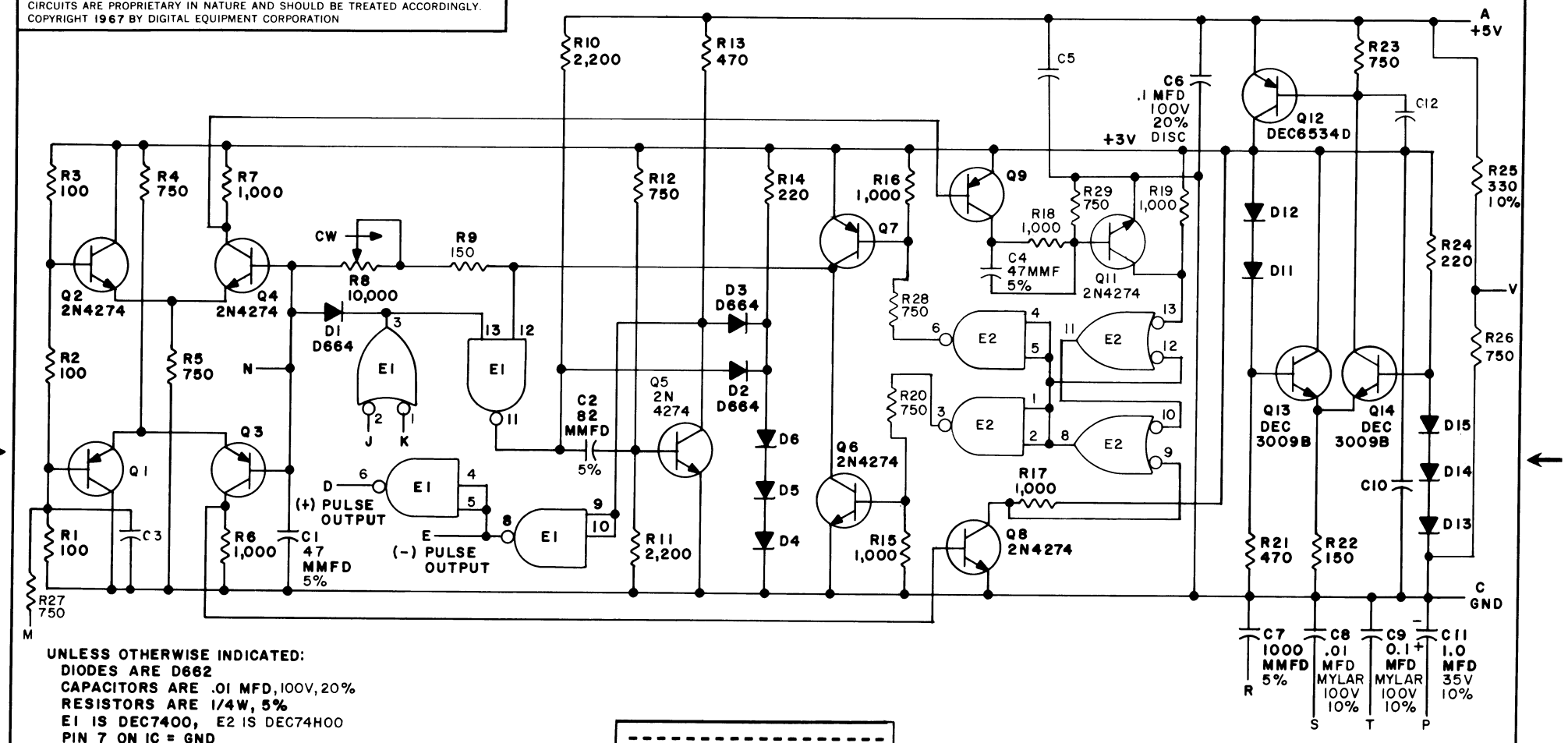


M4014

UNLESS OTHERWISE INDICATED:
DIODES ARE D662
CAPACITORS ARE .01 MFD, 100V, 20%
RESISTORS ARE 1/4W, 5%
E1 IS DEC7400, E2 IS DEC74H00
PIN 7 ON IC = GND
PIN 14 ON IC = +5V
TRANSISTORS ARE DEC4258
R8 IS A HELITRIM POT 10%-78PR

PARTS LIST A-PL-M401-0-0

REVISIONS	REV.	CHG NO.	CHK
	A	6769	
	B	6844	
	C	00001	
	D	00002 00003	
	F	00004	
	J	00005	
	K	00006	
	L	00007	
	M	00008	

DRN. M. Waller	DATE	9-11-67
CHK'D	DATE	9/13/67
ENG.	DATE	9/13/67
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3009B	2N3009	D662	IN645
DEC4258	2N4258	D664	IN3606
2N4274	SAME		
DEC6534D	MPS6534		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

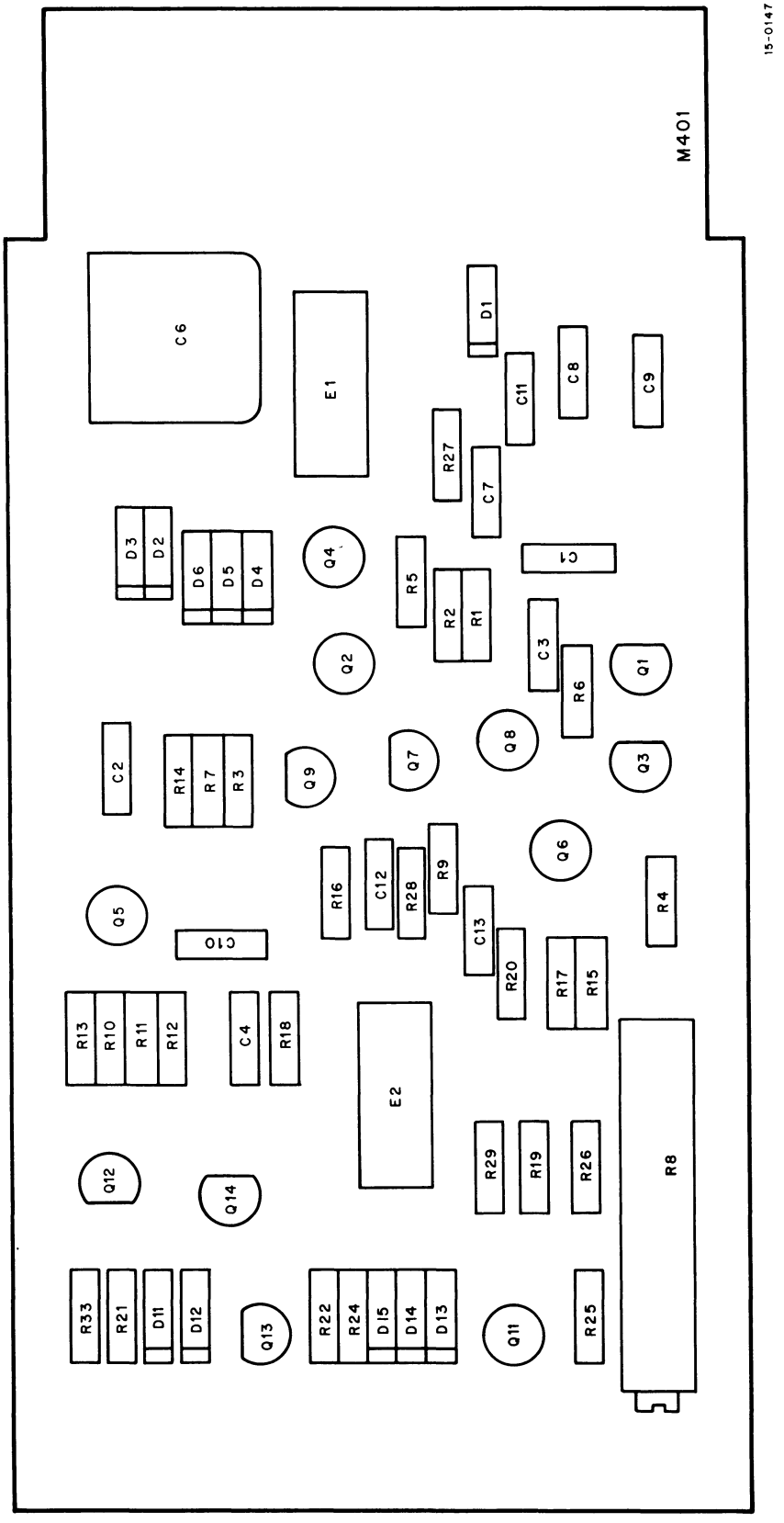
TITLE VARIABLE CLOCK M401

SIZE	CODE	NUMBER	REV
B	CS	M401-0-1	M

PRINTED CIRCUIT REV. M

DEC FORM NO. DRB 102

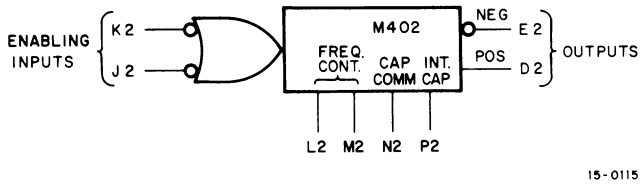
4 DIST. 324 434 432 PINK


M401
15-0147
C6
E1
D1
C11
C8
C9
R27
C7
D3
D2
D6
D5
D4
Q4
R5
C1
R2
R1
C3
Q2
R6
Q1
C2
R14
R7
R3
Q9
Q7
Q8
Q3
Q5
C10
R16
C12
R28
R9
Q6
R4
C13
R20
R17
R15
R13
R10
R11
R12
C4
R18
E2
R29
R19
R26
R8
Q12
Q14
R33
R21
D11
D12
Q13
R22
R24
D15
D14
D13
Q11
R25

M402
Photo Mod Clock

The 402 module contains a stable RC-coupled multivibrator that produces standard 100-ns timing pulses at adjustable repetition rates.

The module is intended for use as a source of timing signals in a digital system. Repetition rate is adjustable from 1 Hz to 500 kHz in two ranges. An internal capacitance, selected by a jumper wire, facilitates coarse frequency control; and an internal light source provides continuously variable adjustment within the selected range.



M402 Simplified Diagram

Coarse Frequency Range

Frequency Range	Cap	Interconnections Required
250 Hz to 500 kHz	0.01 μF	None
1 Hz to 6 kHz	2.00 μF	N2 - P2

A 2-input OR gate input is provided for start-stop control of the pulse train. A level change from HIGH to LOW with fall time less than 400 ns is required to enable the clock.

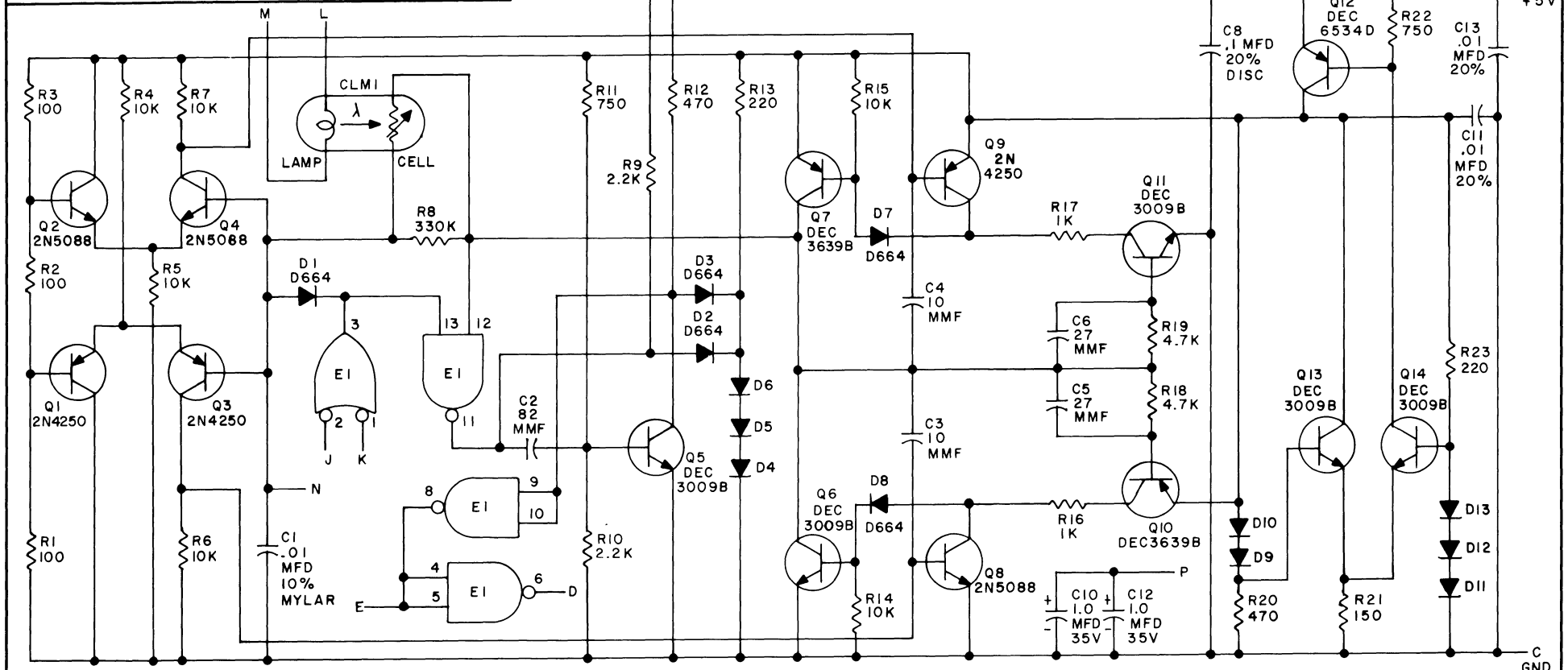
Fine frequency adjustment is obtained by applying a control voltage to pins L2 and M2. This voltage changes the intensity of a lamp inside the module, which in turn adjusts the recovery time of the multivibrator. The voltage applied between pins L and M should be limited to the range of 0V to 5V.

The following are the input, output, and power characteristics of the M402 module.

INPUTS: Each ENABLE input presents 1 unit load. For input characteristics of pins L and M, refer to text above.

OUTPUTS: Output pin D supplies positive 100 ns pulses capable of driving 10 unit loads. Output pin E supplies pulses that are the reverse of pin D. This output is capable of driving 9 unit loads.

POWER: Power dissipation of the M402 module is 5V at 100 mA (maximum).



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 100V, 5%
DIODES ARE D662
RESISTORS ARE 1/4W, 5%
E1 IS DEC7400N
PIN 7 ON IC = GND
PIN 14 ON IC = +5V
CLM1 IS 4006A

REVISIONS	REV.	CHG NO.	CHK

DRN. M. Waller	DATE	5-16-69
CHK'D G. Yaneza	DATE	5-20-69
ENG. R.E. Shagoul	DATE	9-12-69
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	IN645	DEC3639B	2N3639
D664	IN3606	DEC6534D	MPS6534
2N4250	NONE		
SE4020	NONE		
DEC3009B	2N3009		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PHOTO MOD CLOCK M402

SIZE	CODE	NUMBER	REV.
B	CS	M402-0-1	

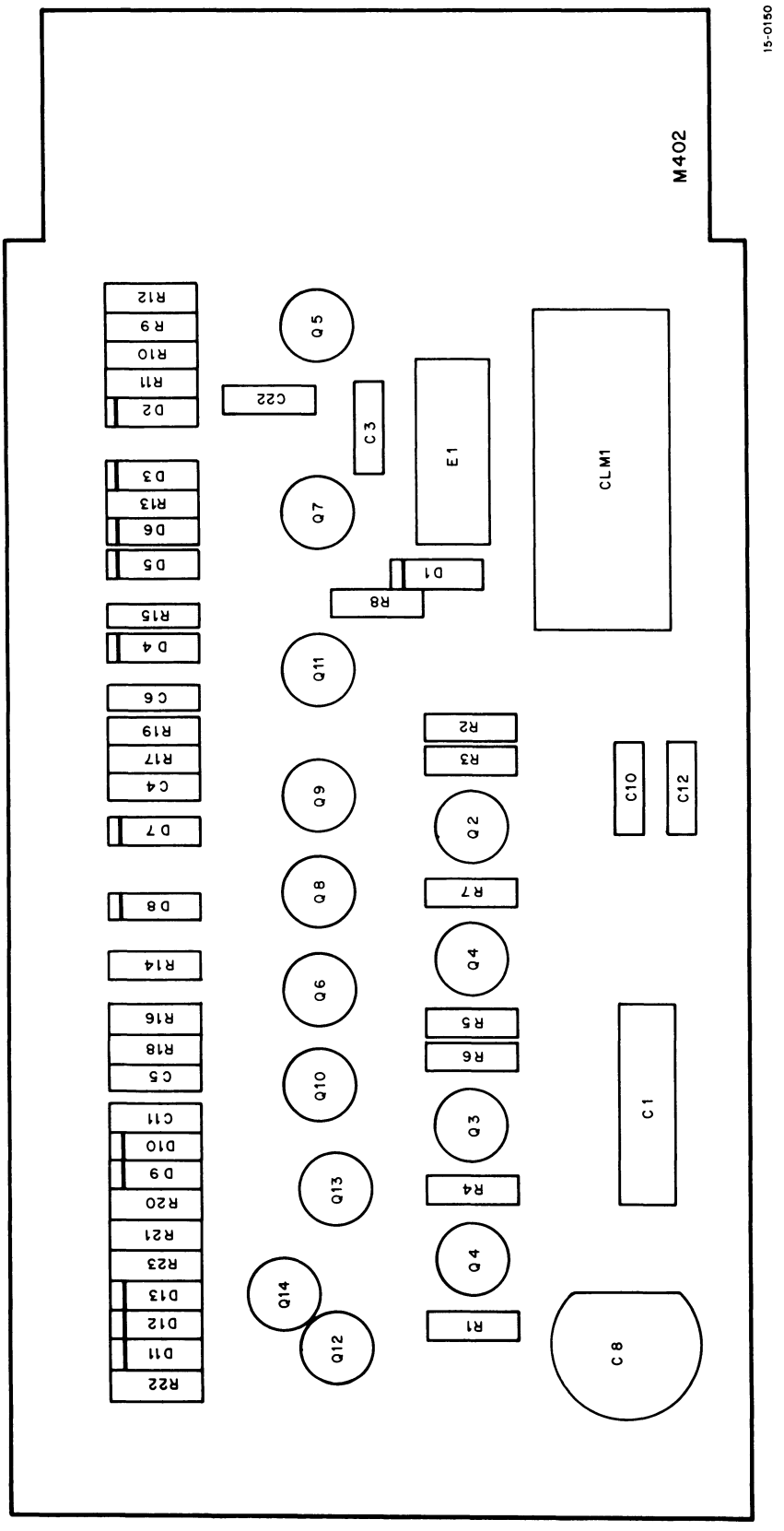
PRINTED CIRCUIT REV. B

DEC FORM NO. DRB 102

5

DIST. 324, 434, 435 3

PINK

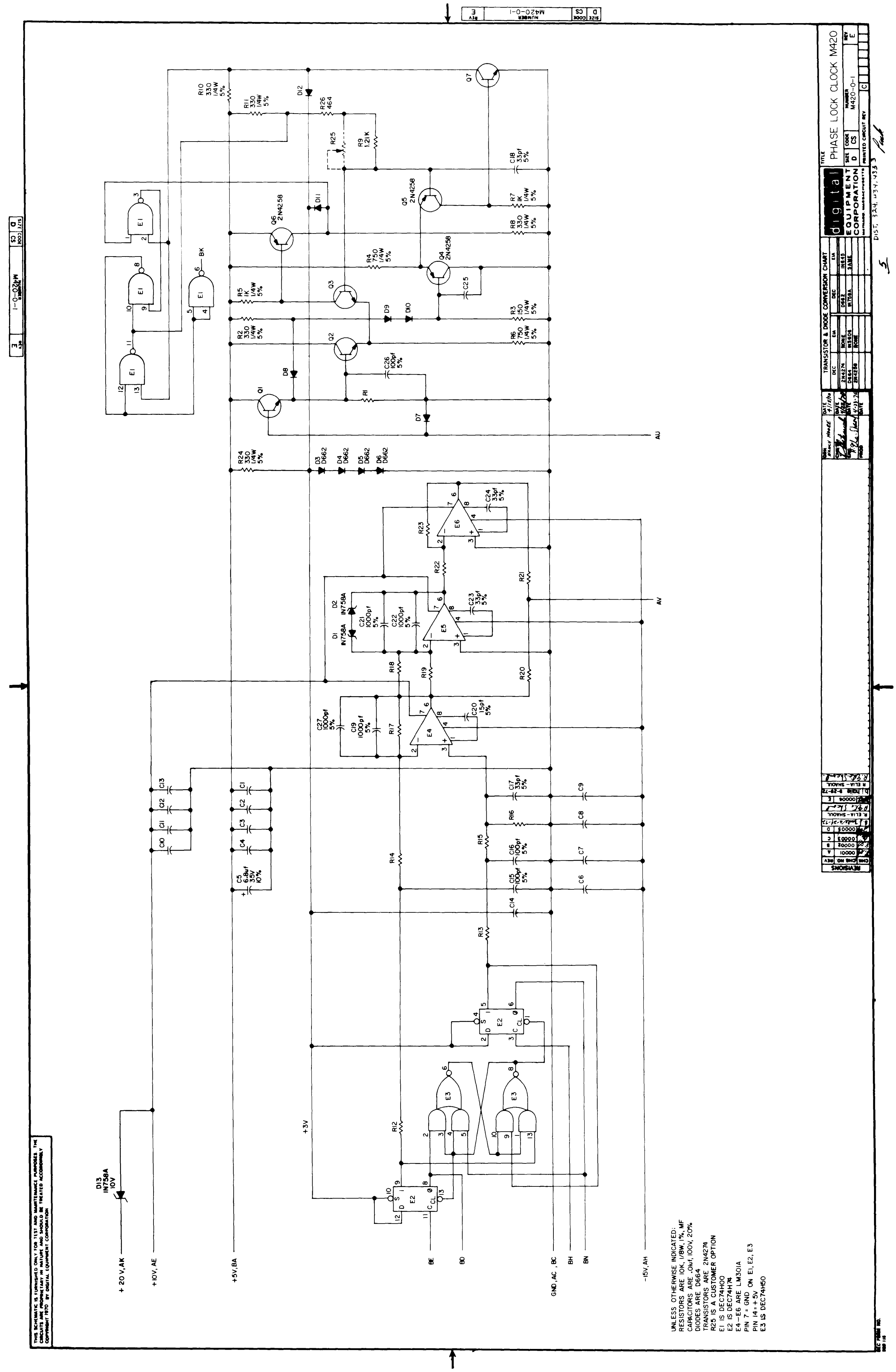

15-0150
M402
R12
R9
R10
R11
D2
D3
R13
D6
D5
R15
D4
C6
R19
R17
C4
D7
D8
R14
R16
C5
R18
C11
D10
D9
R20
R21
R23
D13
D12
D11
R22
Q14
Q12
Q13
Q10
Q6
Q8
Q9
Q11
Q7
C22
Q5
C3
E1
D1
R8
CLM1
R2
R3
Q2
R7
Q4
R5
R6
Q3
R4
Q4
R1
C8
C1
C10
C12

M420
Phase-Lock Clock

The M420 Phase-Lock Clock is used in the data separator control of the RP15 Disk Pack Control. Inputs include a reference signal at pin BE2 and a controlled input at pin BH2. The controlled input is the output frequency of the M420 at pin BK2 divided by 1, 2, or 4. This 5 MHz output has a 50 percent duty cycle.

The M420 contains a phase error detector and a voltage controlled oscillator (VCO). The phase error detector output is connected to the VCO input by a jumper between pins AV2 and AU2.

INPUTS:	Inputs at pins BE2 and BH2 present two unit loads.
OUTPUTS:	The output at pin BK2 can drive eight unit loads.
POWER:	13 mA at -15V (MAX) 10 mA at +10V (MAX) 108 mA at +5V (MAX)


PHASE LOCK CLOCK M420
digital EQUIPMENT CORPORATION
M420-0-1
TRANSISTOR & DIODE CONVERSION CHART
REVISIONS
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 10K, 1/8W, 1%, MF
CAPACITORS ARE .01uf, 100V, 20%
DIODES ARE D664
TRANSISTORS ARE 2N4274
R25 IS A CUSTOMER OPTION
E1 IS DEC74H00
E2 IS DEC74H74
E4–E6 ARE LM301A
PIN 7 = GND ON E1, E2, E3
PIN 14 = +5V
E3 IS DEC74H50
+20 V, AK
+10V, AE
+5V, BA
GND, AC, BC
-15V, AH
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY. COPYRIGHT 1970 BY DIGITAL EQUIPMENT CORPORATION

M452
Variable Clock

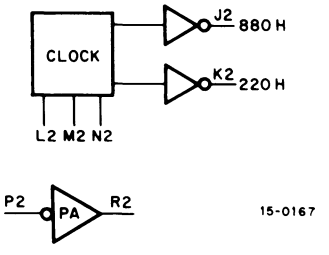
The M452 is a free-running clock that generates the necessary timing signals for the Teletype control in a digital system. Frequency adjustment of this module is limited to less than 5 percent, and the overall clock stability with respect to supply voltage and temperature variations is approximately 1 percent. The available output frequencies are 880 Hz and 220 Hz. A pulse amplifier is provided for the generation of nominal 150 ns pulses.

The following are the input, output, and power characteristics of the M452 module.

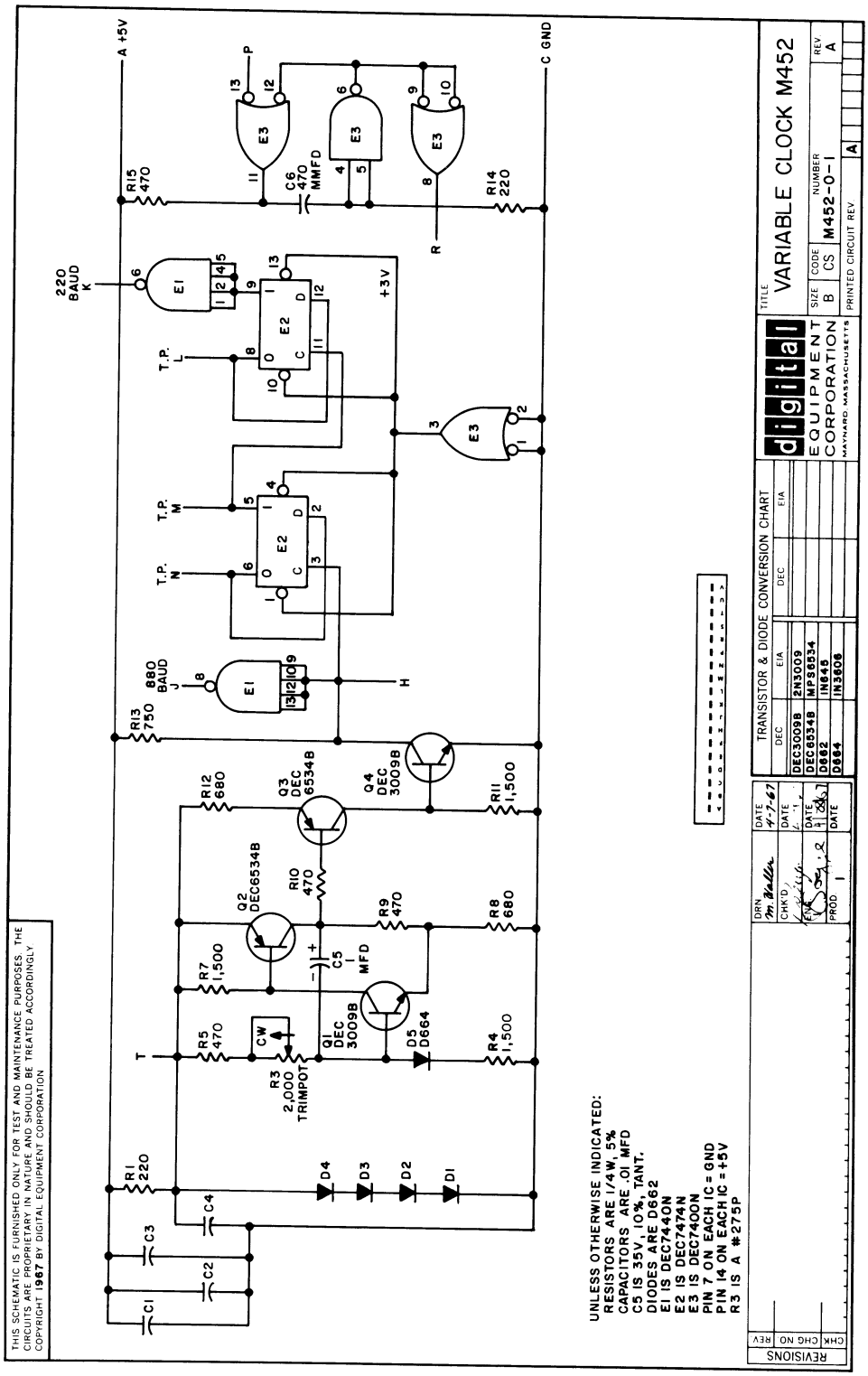
INPUTS: The pulse amplifier input presents 1 unit load.

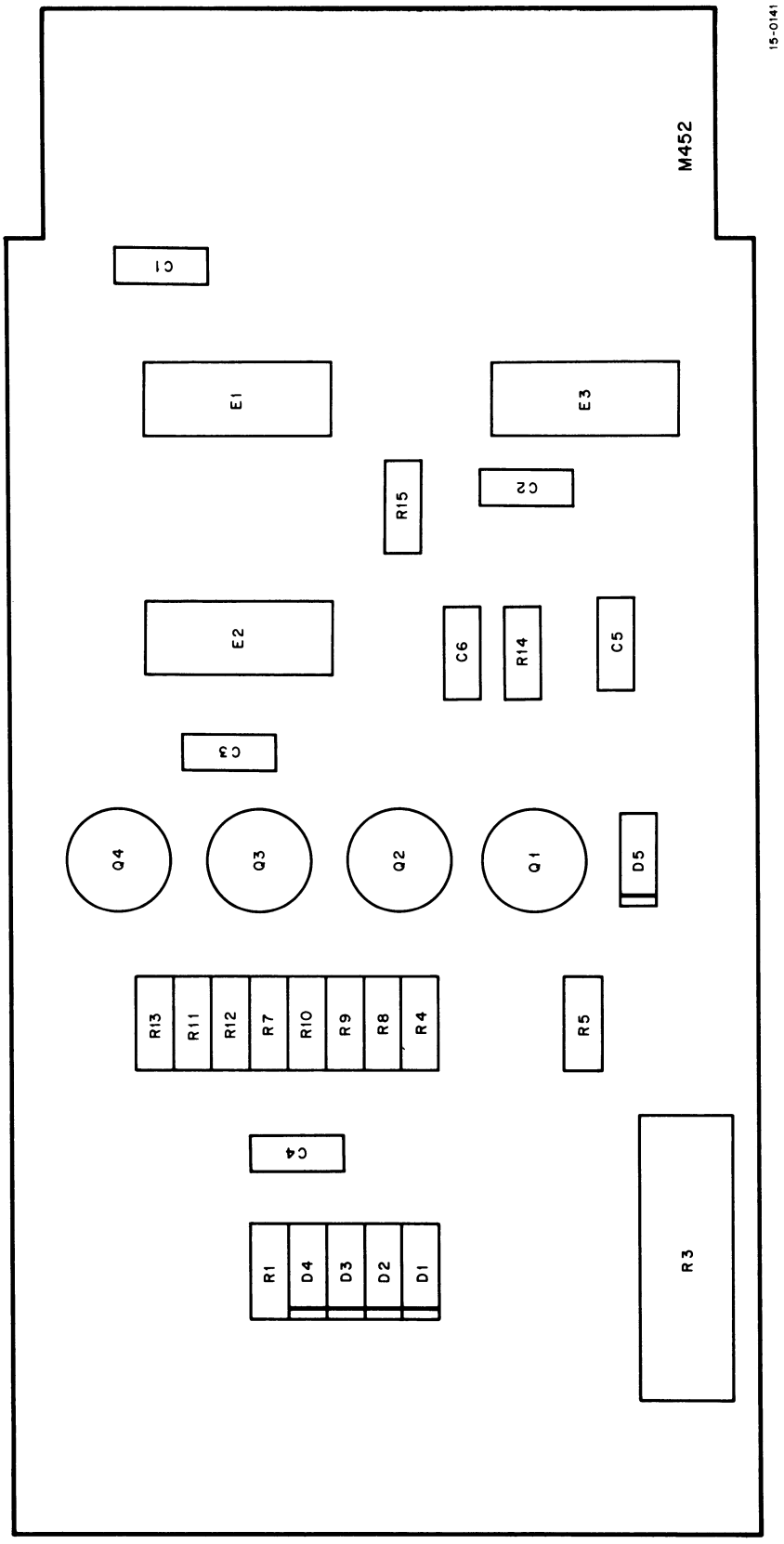
OUTPUTS: Pin J2 drives 30 unit loads at 880 Hz. Pins N2 and M2 drive 9 unit loads at 330 Hz. Pin L2 drives 9 unit loads at 220 Hz. Pin K2 drives 30 unit loads at 220 Hz. Pin R2 drives 10 unit loads with a nominal 150 ns positive output pulse. Under normal operating conditions, pins L2, M2, and N2 are used as test points.

POWER: Power dissipation of the M452 module is +5V at 77 mA (maximum).



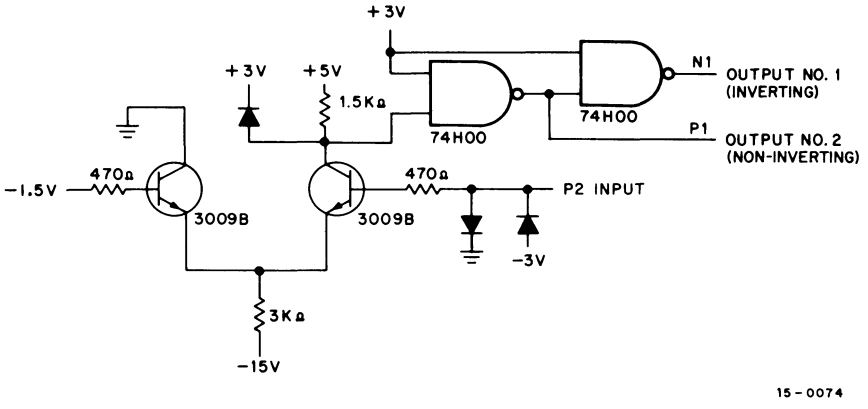
M452 Simplified Diagram


THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY
COPYRIGHT 1967 BY DIGITAL EQUIPMENT CORPORATION
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE .01 MFD
C5 IS 35V, 10%, TANT.
DIODES ARE D662
E1 IS DEC7440N
E2 IS DEC7474N
E3 IS DEC7400N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
R3 IS A #275P
A +5V
C GND
+3V
220 BAUD K
880 BAUD J
T.P. L
T.P. M
T.P. N
T.P. P
T.P. R
T
H
R1 220
R2 680
R3 2,000 TRIMPOT
R4 1,500
R5 470
R7 1,500
R8 680
R9 470
R10 470
R11 1,500
R12 680
R13 750
R14 220
R15 470
C1
C2
C3
C4
C5 1 MFD
C6 470 MMFD
D1
D2
D3
D4
D5 D664
Q1 DEC 3009B
Q2 DEC6534B
Q3 DEC 6534B
Q4 DEC 3009B
E1
E2
E3
CW
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
DEC30009B 2N3009
DEC6534B MPS6534
D662 IN645
D664 IN3606
REVISIONS
DRN
CHK'D
PROD
DATE 4-7-67
digital
EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
VARIABLE CLOCK M452
SIZE B
CODE CS
NUMBER M452-0-1
REV A
PRINTED CIRCUIT REV A


15-0141
M452
C1
E1
E3
R15
C2
E2
C6
R14
C5
C3
Q4
Q3
Q2
Q1
D5
R13
R11
R12
R7
R10
R9
R8
R4
R5
C4
R1
D4
D3
D2
D1
R3

M500
Converter-I/O Bus Receiver

The M500 Converter - I/O Bus Receiver module is an M-series single-height module containing eight converter - I/O bus receivers that can accept negative logic levels and convert them to positive levels. Each converter - bus receiver has a negative input clamped to 0V and -3V. The threshold switching level is -1.5V with an input current of 100 μA. Inverted and noninverted outputs are supplied by each receiver.



M500 Simplified Diagram

The following are the input, output, and power characteristics of the M500 module.

INPUTS: Input characteristics are as follows:

Minimum input impedance at 0V - 30 kΩ
Maximum current load to bus - 100 μA
Inputs are standard negative logic levels of 0V and -3V.

OUTPUTS: Outputs are standard TTL positive logic levels with the following driving capability:

Output No. 1 - 12 unit loads
Output No. 2 - 11 unit loads

DELAYS: Input/Output No. 1 delay - 50 ns
Input/Output No. 2 delay - 40 ns

POWER: Power dissipation in the M500 module is 750 mW (maximum) from -15V and 800 mW (maximum) from +5V.

The M500 module was designed to receive PDP-9 I/O bus signals for devices using positive logic. It provides a high input impedance. This module is pin compatible with the M510 module.

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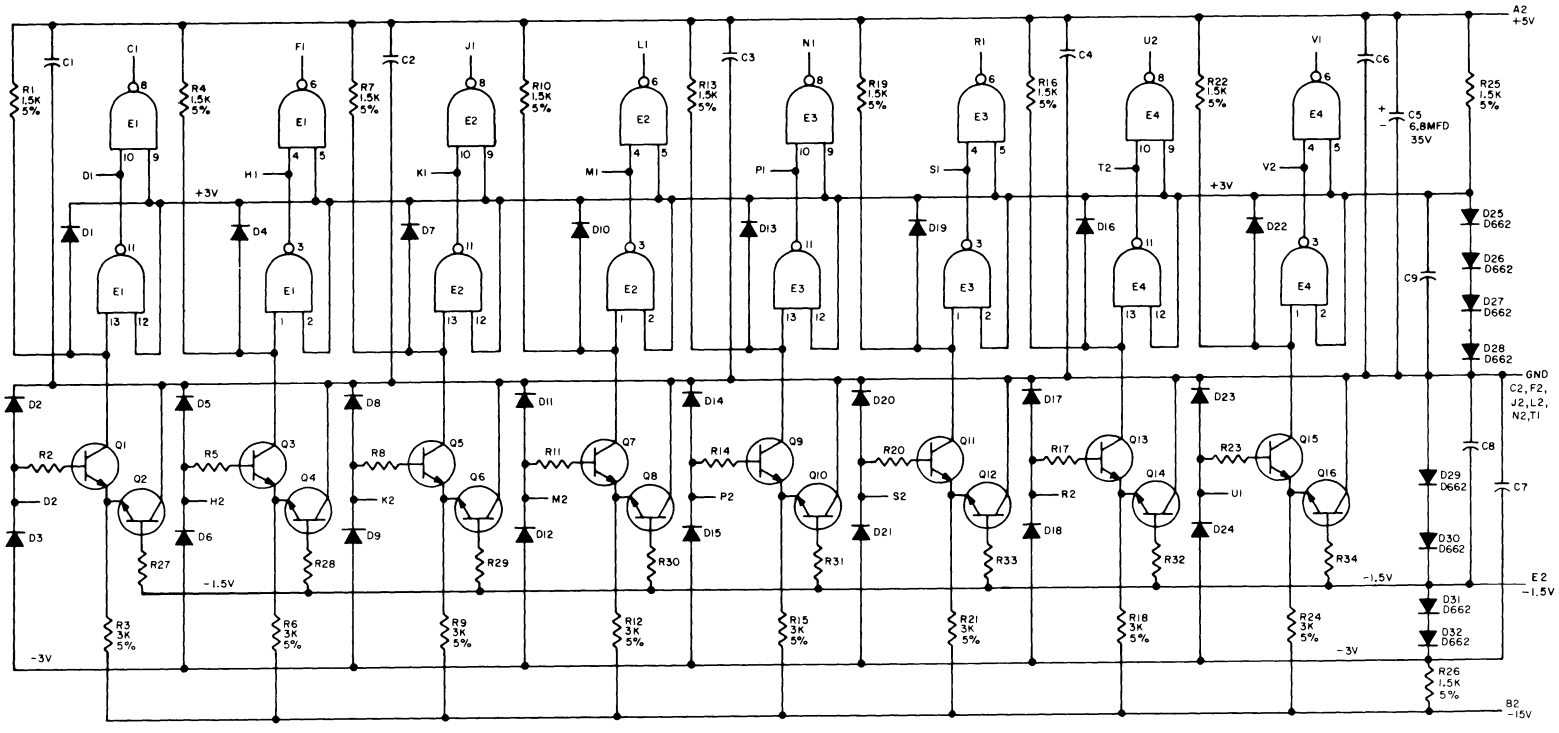


UNLESS OTHERWISE INDICATED:
- TRANSISTORS ARE DEC3009B
- DIODES ARE D664
- RESISTORS ARE 1/4W, 10%
- IC'S ARE DEC74H00N
- PIN 7 ON EACH IC = GND
- PIN 14 ON EACH IC = +5V
- CAPACITORS ARE .01 MFD
- RESISTORS ARE 470

REVISIONS	REV	CHG NO	CHK

DRN	BUTLER	5/5/69
CHK'D	M. Moreland	5-7-69
ENG		- 6-69
PROD		

TRANSISTOR & DIODE CONVERSION CHART

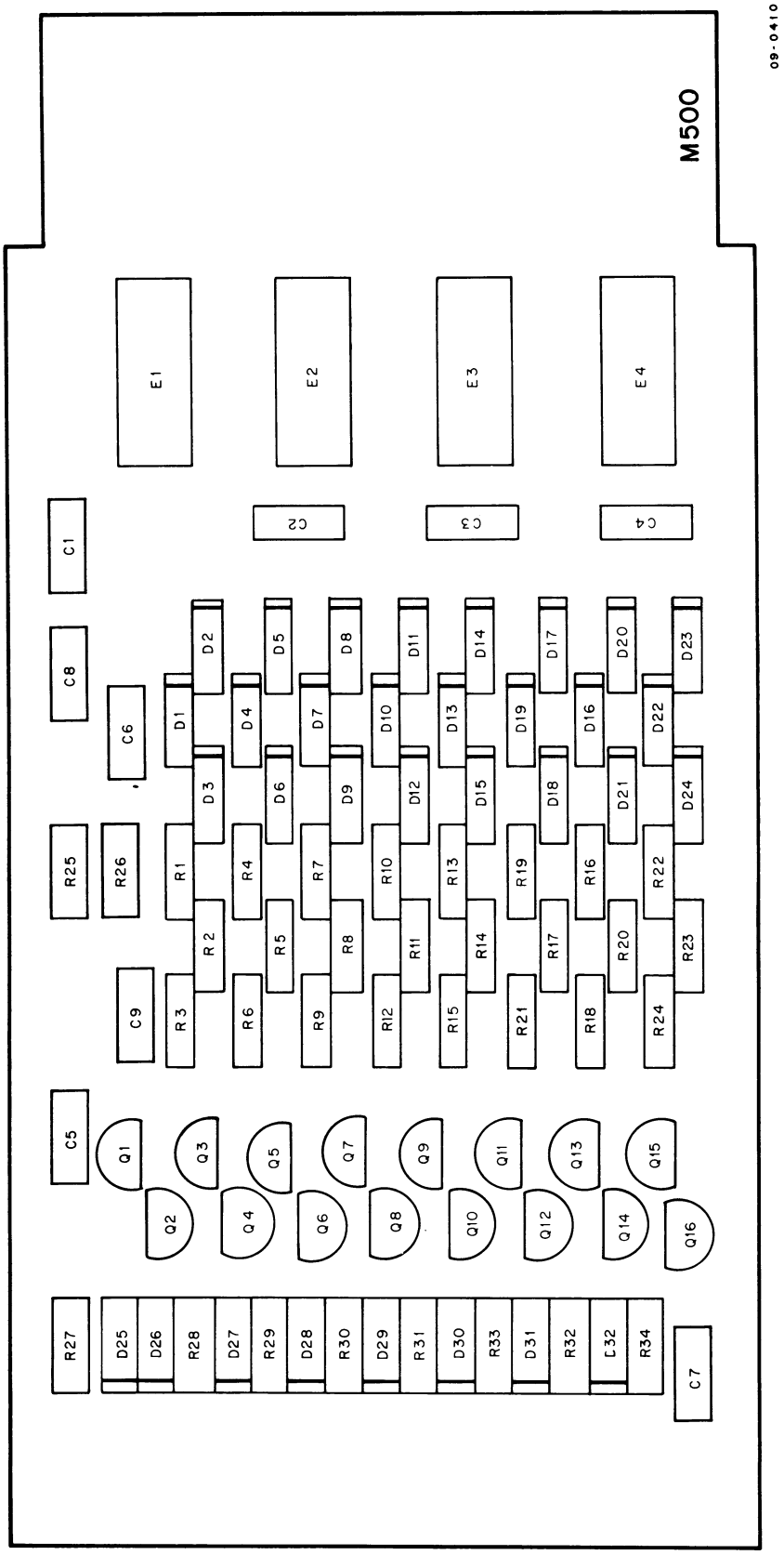
DEC	EIA	DEC	EIA
DEC3009B	2N3009B		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE NEGATIVE INPUT CONVERTER M500

SIZE	CODE	NUMBER	REV
C	CS	M500-0-1	

PRINTED CIRCUIT REV


M500
09-0410
E1
E2
E3
E4
C1
C2
C3
C4
C5
C6
C7
C8
C9
R25
R26
R27
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
R28
R29
R30
R31
R33
R32
R34
C32
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16

M510
I/O Bus Receiver

The M510 module is an M-series single-height module containing eight PDP-15 I/O bus receivers. The receiver circuit consists of a two-stage emitter follower with two TTL output buffer gates to supply both inverted and noninverted outputs.

The following are the input, output, and power characteristics of the M510 module.

INPUTS: Input characteristics are:

Minimum input impedance - 22.5 kΩ
Maximum current load to bus - 100 μA
Inputs are standard PDP-15 I/O Positive Bus levels.

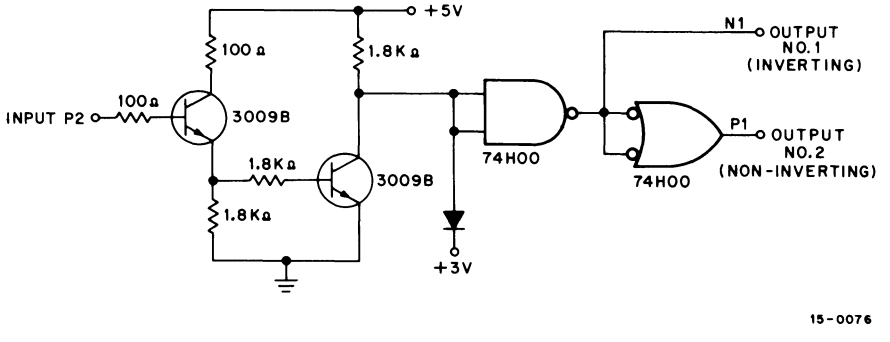
OUTPUTS: Outputs are standard TTL positive logic levels with the following driving capability:

Output No. 1 - 10 units
Output No. 2 - 12 units

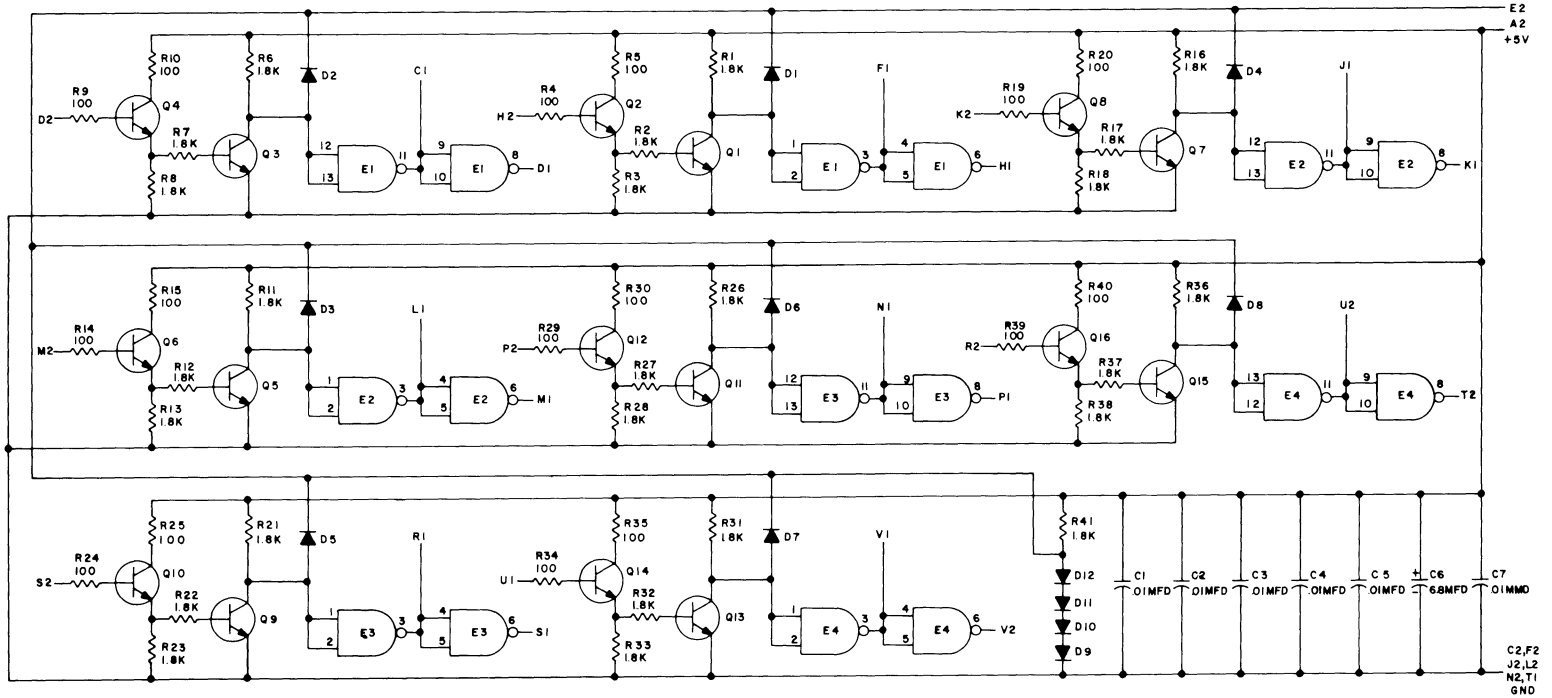
DELAYS: Input/Output No. 1 delay - 50 ns (maximum)
Input/Output No. 2 delay - 60 ns (maximum)

POWER: The power dissipation of the M510 module is 900 mW (maximum).

The M510 module was designed to receive PDP-15 I/O bus signals for devices using positive logic. It provides a high input impedance that yields a switching threshold between the HIGH and LOW levels of the propagated signals. This feature reduces loading and noise problems. The M510 module is pin compatible with the M500 module.



M510 Simplified Diagram



UNLESS OTHERWISE INDICATED
IC'S ARE DEC74H00
PIN 7 ON ECH IC = GND
PIN 14 ON EACH IC=+5V
DIODES ARE D 664
RESISTORS ARE 1/4W 10%
TRANSISTORS ARE DEC 3009B

REVISIONS

CHK	CHG NO.	REV

DRN		DATE 2-7-69
CHK		DATE 3/11/69
ENG		DATE 5-9-69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	1N3606		
DEC3009	2N3009		

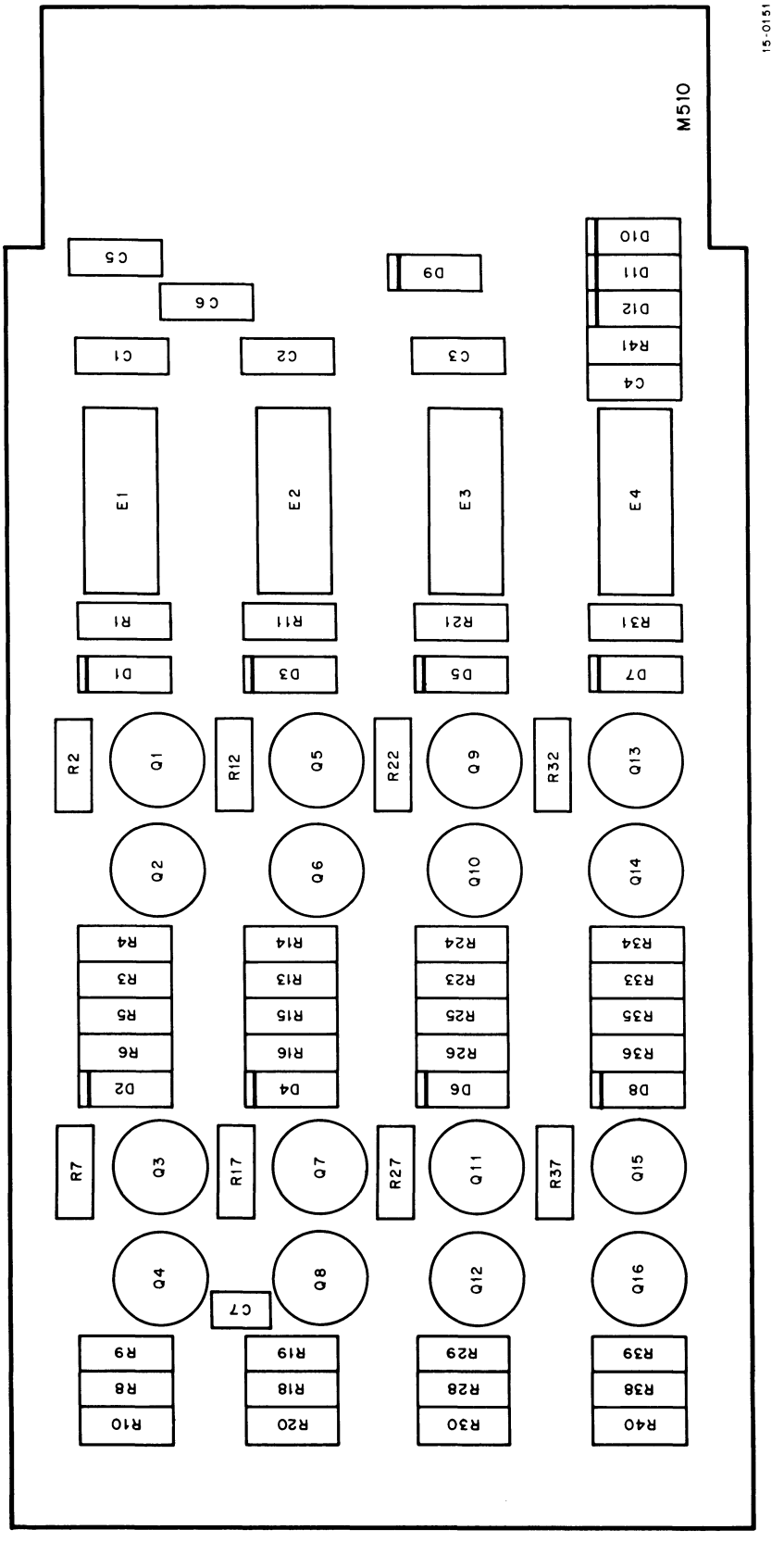
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 10 BUS RECEIVER M510

SIZE	CODE	NUMBER	REV
C	CS	M510-0-1	

PRINTED CIRCUIT REV. A

M510-2


M510
15-0151
C5
C6
C1
C2
C3
D9
D10
D11
D12
R41
C4
E1
E2
E3
E4
R1
R11
R21
R31
D1
D3
D5
D7
R2
Q1
R12
Q5
R22
Q9
R32
Q13
Q2
Q6
Q10
Q14
R4
R14
R24
R34
R3
R13
R23
R33
R5
R15
R25
R35
R6
R16
R26
R36
D2
D4
D6
D8
R7
Q3
R17
Q7
R27
Q11
R37
Q15
Q4
Q8
Q12
Q16
C7
R9
R19
R29
R39
R8
R18
R28
R38
R10
R20
R30
R40

M515
Real Time Clock

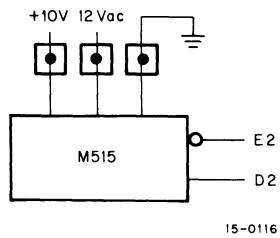
The M515 module contains a real time clock that converts conventional sinusoidal power waveforms into timing gates. Complementary timing gates are available at the output pins of the module (see illustration).

The following are the input, output, and power characteristics of the M515 module.

INPUTS: The input is 12 Vac.

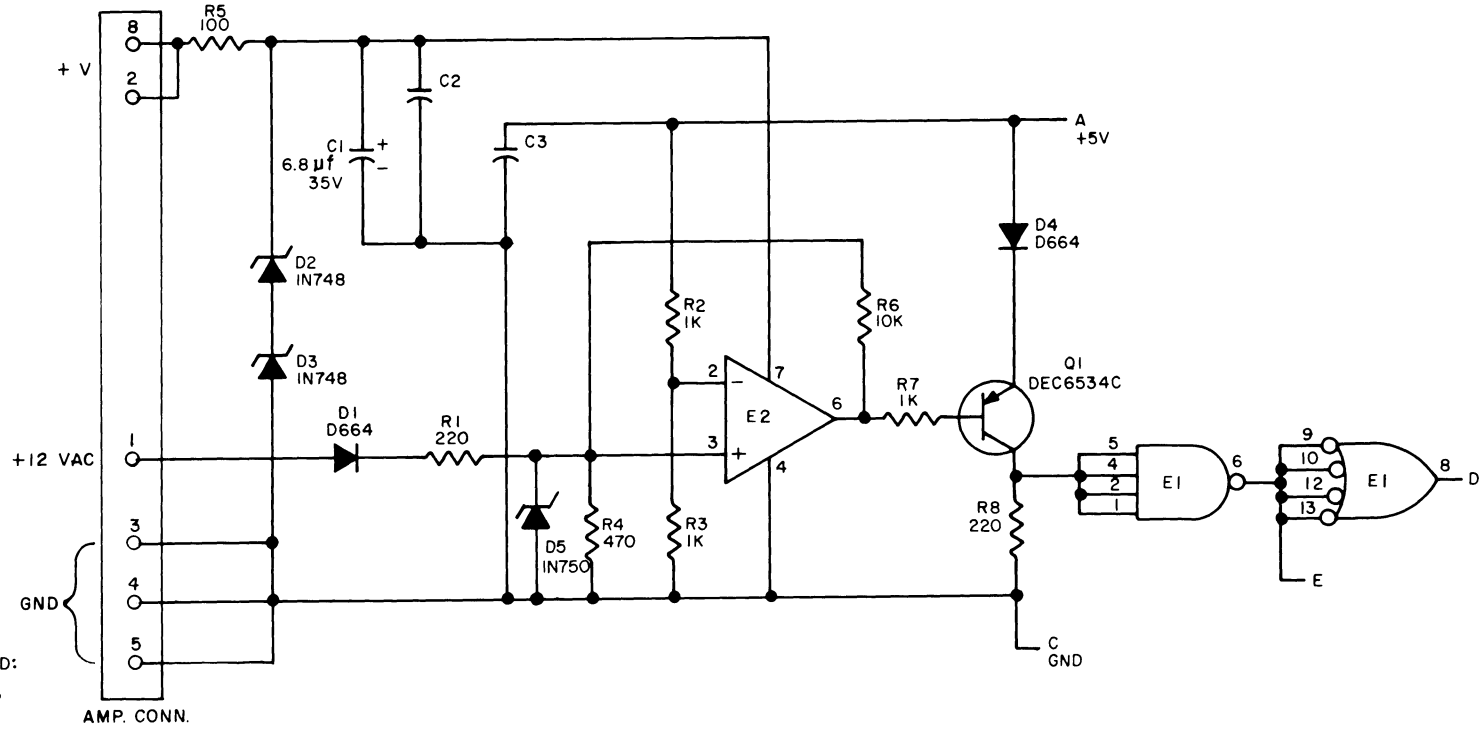
OUTPUTS: The output at pin D2 is capable of driving 36 unit loads, and the output at pin E2 is capable of driving 31 unit loads.

POWER: Power dissipation of the M515 module is 5V at 55 mA and 10V at 30 mA.



M515 Simplified Diagram

SIZE	CODE	NUMBER	REV.
B	CS	M515-0-1	D



UNLESS OTHERWISE INDICATED:

RESISTORS ARE 1/4W, 5%
E2 IS MC1709CG
E1 IS DEC74H40
CAPACITORS ARE .01µf, 100V, 20%
E1 PIN 7 = GND
E1 PIN 14 = +5V

CONNECTOR IS DEC#1209340
PINS ARE DEC #1209456

REVISIONS	REV.	CHG NO	CHK
	C	00001	
	D	00003	
SUPP	SUPP	00004	

DRN. BUTLER	DATE 5/1/69	
CHK'D M. Moorhead	DATE 5-8-69	
ENG. D.E. Conner	DATE 9/3/69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC6534C	MPS6534		
D664	IN3606		
IN748	SAME		
IN750	SAME		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: REAL TIME CLOCK M515

SIZE	CODE	NUMBER	REV.
B	CS	M515-0-1	D

PRINTED CIRCUIT REV. D

DEC FORM NO.
DRB 102

5 PINK 1951-324, 434, 433, 3

M602
Pulse Amplifiers

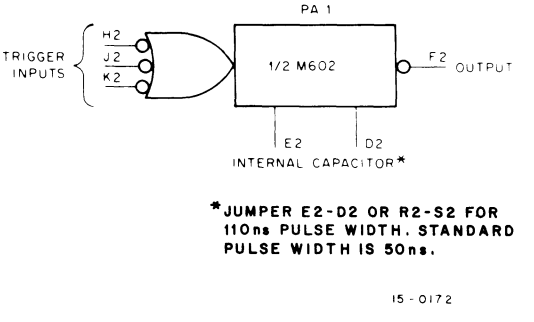
The M602 contains two pulse amplifiers that provide power amplification, standardize pulse amplitude and width, and transform level changes into a standard pulse. A negative pulse output is produced when the input is triggered by a transition from HIGH to LOW. Propagation time between input and output thresholds is 30 ns (maximum). An internal capacitor is brought out to pin connections to permit the standard 50 ns output pulse to be increased to 110 ns (nominal). Recovery time is equal to that of the output pulse width. The input must have a fall time (10 percent to 90 percent points) of less than 400 ns and must remain below 0.8V for at least 30 ns. Maximum PRF is 10 MHz.

The following are the input, output, and power characteristics of the M602 module.

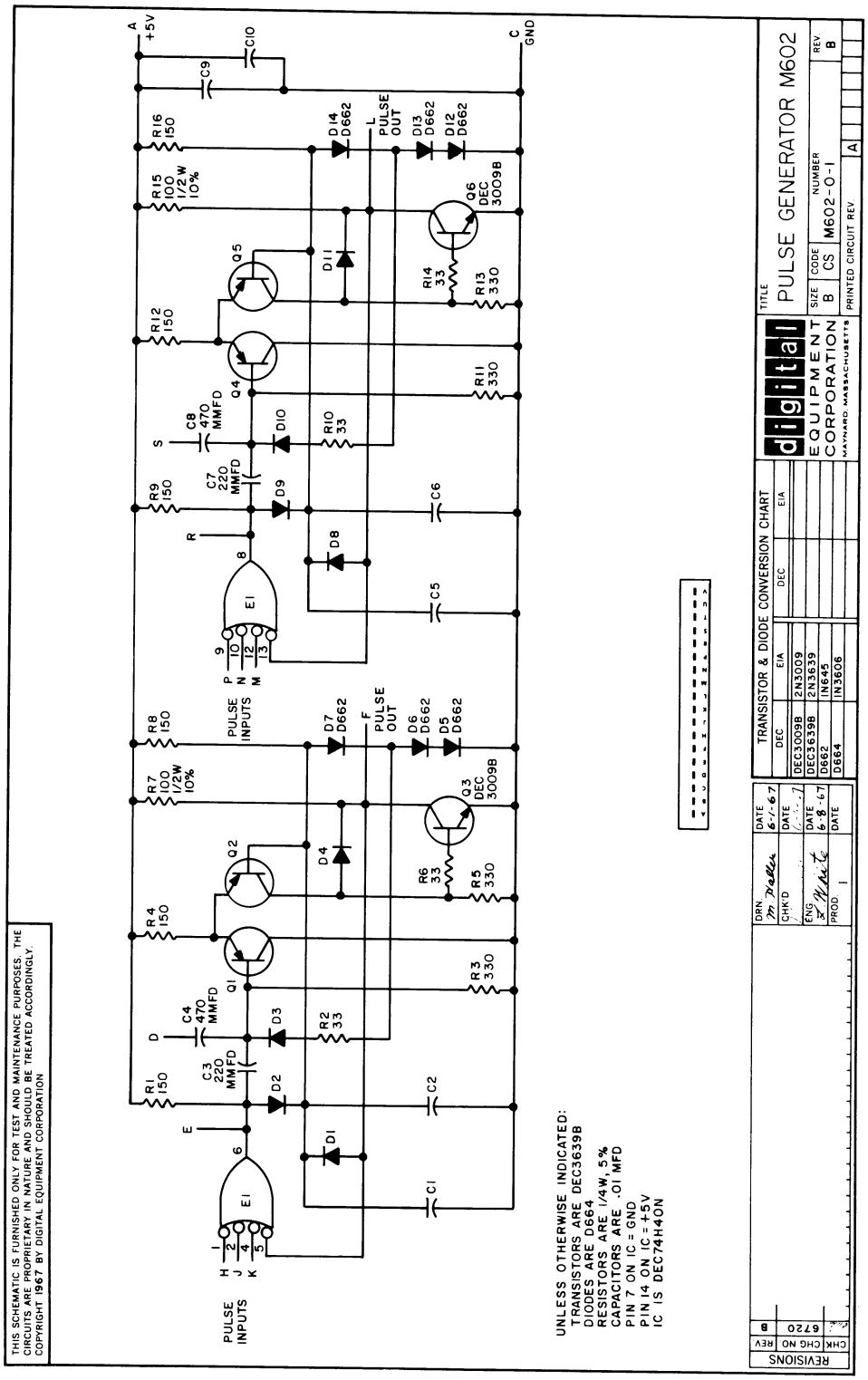
INPUTS: Each input presents 2.5 unit loads.

OUTPUTS: Each output is capable of driving 30 unit loads.

POWER: Power dissipation of the M602 module is 5V at 213 mA (maximum).



M602 Simplified Diagram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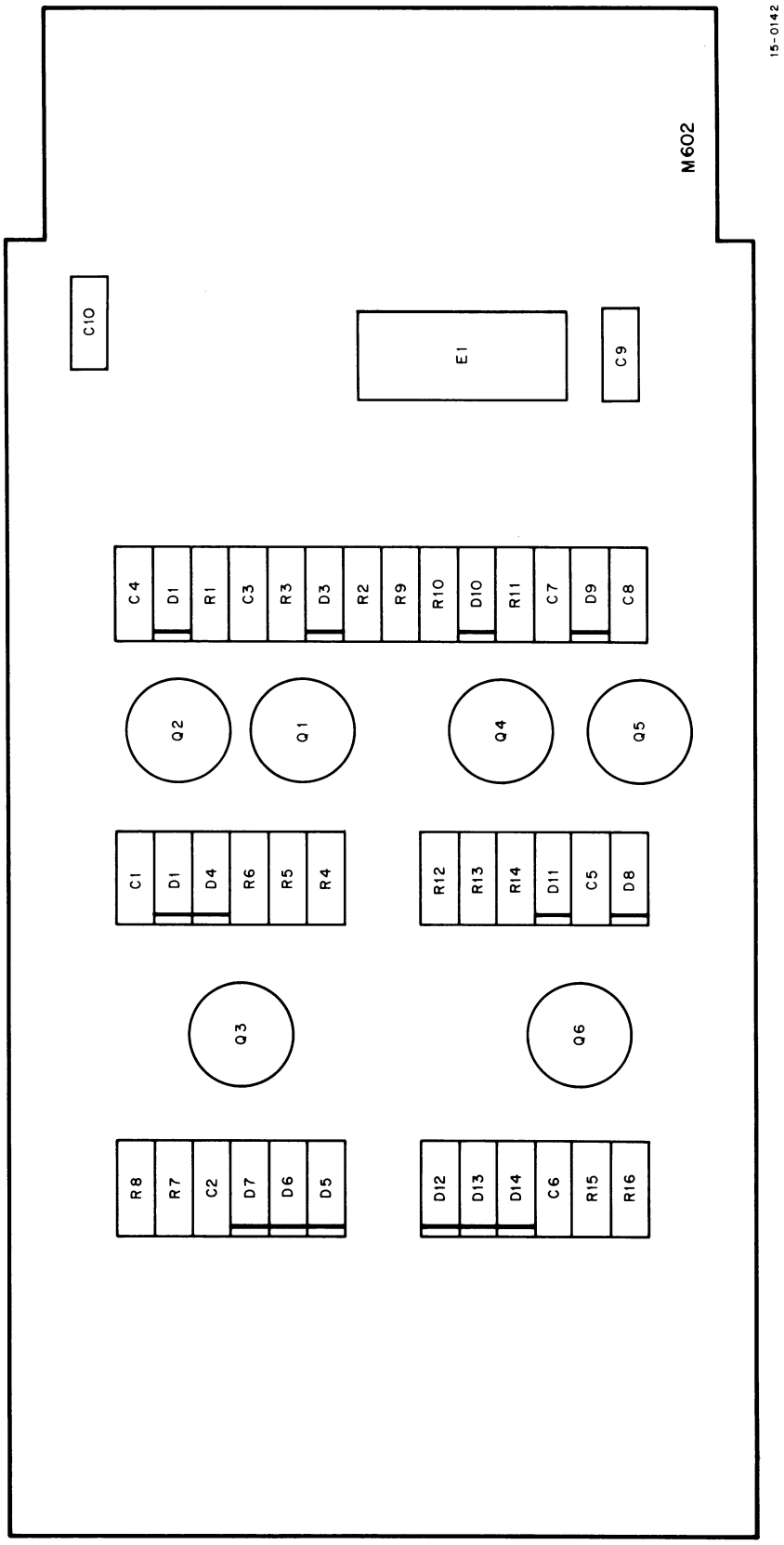
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC3639B
DIODES ARE D664
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01 MFD
PIN 7 ON IC = GND
PIN 14 ON IC = +5V
IC IS DEC74H40N
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
DEC3009B 2N3009
DEC3639B 2N3639
D662 IN645
D664 IN3606
DEC EIA
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
PULSE GENERATOR M602
SIZE B
CODE CS
NUMBER M602-0-1
REV B
PRINTED CIRCUIT REV A
REVISIONS
CHK CHG NO REV
6720 B
DRN M. Haller DATE 6-7-67
CHK'D DATE
ENG E. White DATE 6-8-67
PROD DATE


M602
15-0142
C10
E1
C9
C4
D1
R1
C3
R3
D3
R2
R9
R10
D10
R11
C7
D9
C8
Q2
Q1
Q4
Q5
C1
D1
D4
R6
R5
R4
R12
R13
R14
D11
C5
D8
Q3
Q6
R8
R7
C2
D7
D6
D5
D12
D13
D14
C6
R15
R16

M606
Pulse Generators

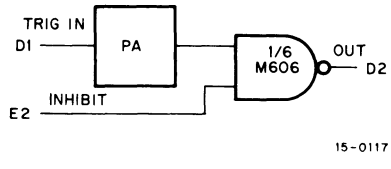
The M606 module contains six separate pulse generators. Each generator produces a pulse to ground in response to an input level shift from HIGH to LOW (see illustration). Duration of the pulse must be at least 30 ns, and the pulse can be no wider than 100 ns. Each pulse generator is also equipped with an inhibit gate that blocks the output if grounded. A logic 1 level should be applied to the inhibit gate if a continuous output is required. Each pulse generator can be used for setting or clearing flip-flops by connecting the output to the DIRECT CLEAR or SET inputs of up to 15 flip-flops.

The following are the input, output, and power characteristics of the M606 module.

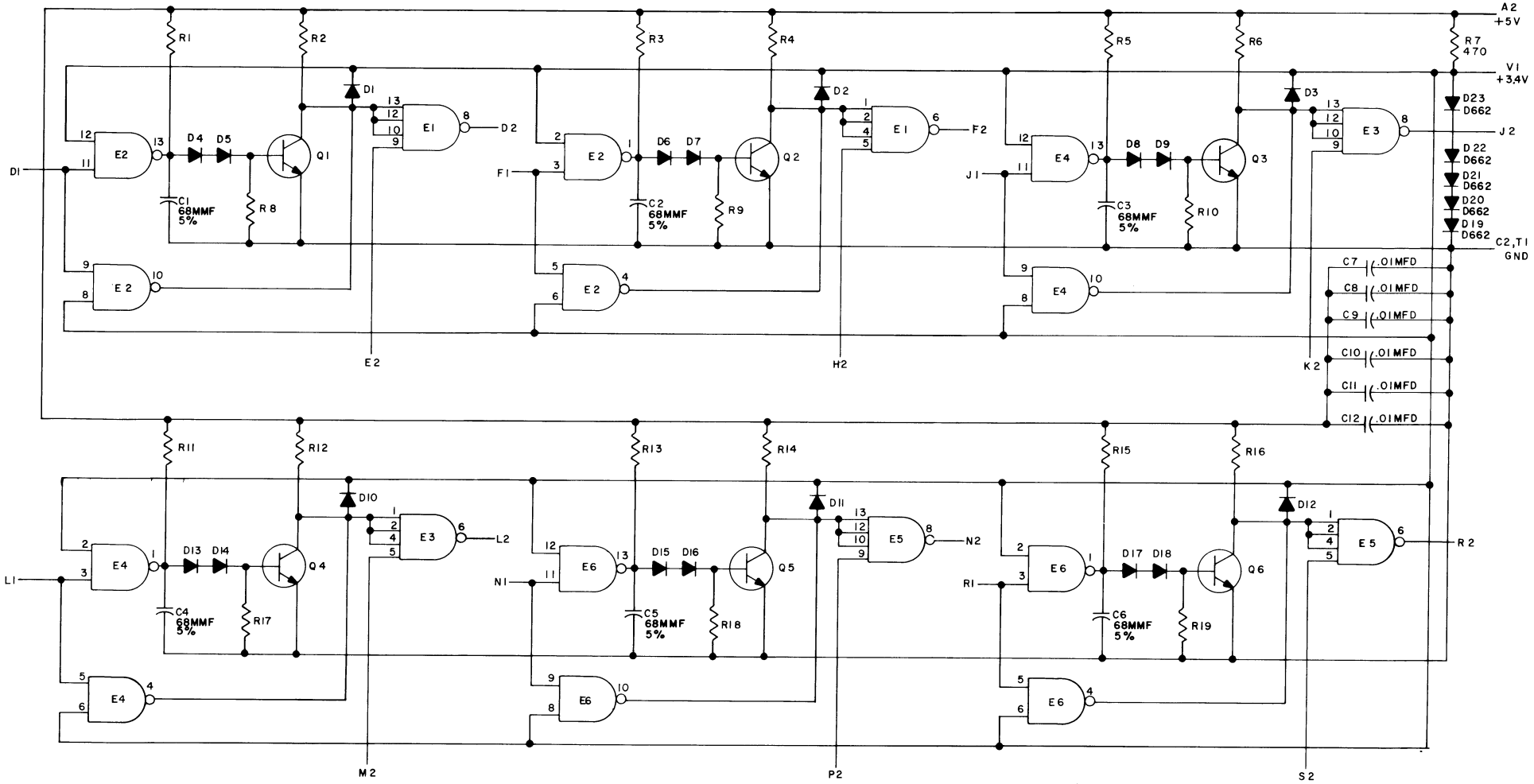
INPUTS: The TRIGGER input presents two TTL unit loads, and the INHIBIT input presents one unit load.

OUTPUTS: All pulse generator outputs present 30 unit loads. Output pin V1 is a source of a logic 1 level that is capable of driving 10 unit loads.

POWER: Power dissipation of the M606 module is 5V at 188 mA (maximum).



M606 Simplified Diagram



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 100V, 20%
DIODES ARE D 664
RESISTORS ARE 1.5 K, 1/4W, 5%
TRANSISTORS ARE DEC3009B
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E3, E5 ARE DEC 7440N
E2, E4, E6 ARE DEC 7401N

REVISIONS		
REV.	CHG NO.	CHK
B	00001	

DRN.		DATE 4-22-69
CHK'D		DATE 4/29/69
ENG.		DATE 6/3/69
PROD.		DATE 10/24/76

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	1N645		
D664	1N3606		
DEC3009B	2N3009		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: PULSE GENERATOR M606

SIZE	CODE	NUMBER	REV.
C	CS	M606-0-1	B

PRINTED CIRCUIT REV.

DEC FORM NO. DRC 102

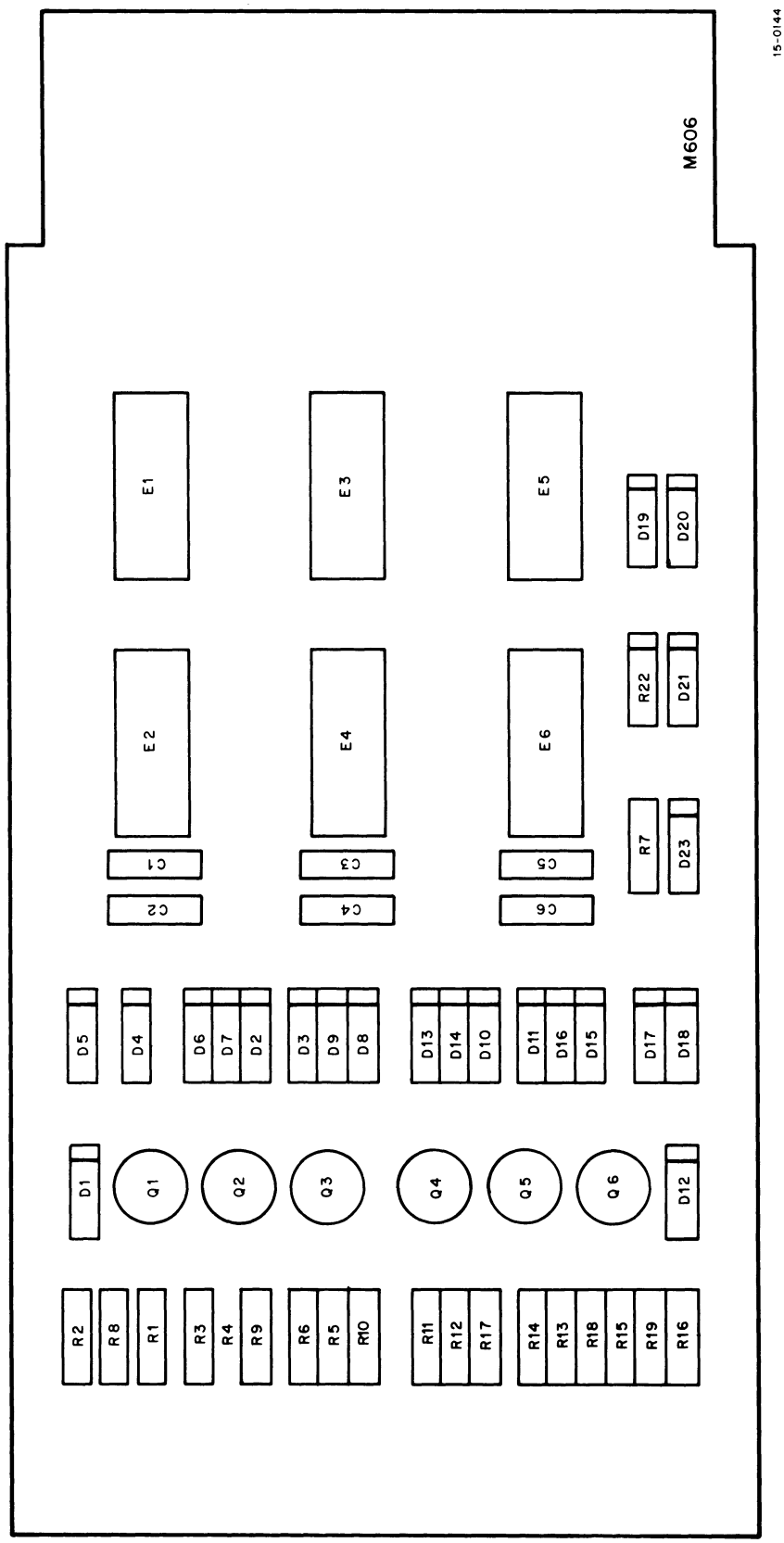
5

DIST. 224, 434, 4

PINK

M606-2

SIZE C | CODE CS | NUMBER M606-0-1 | REV. B


M606
15-0144
E1
E3
E5
D19
D20
E2
E4
E6
R22
D21
C1
C3
C5
R7
D23
C2
C4
C6
D5
D4
D6
D7
D2
D3
D9
D8
D13
D14
D10
D11
D16
D15
D17
D18
D1
Q1
Q2
Q3
Q4
Q5
Q6
D12
R2
R8
R1
R3
R4
R9
R6
R5
R10
R11
R12
R17
R14
R13
R18
R15
R19
R16

M611
High-Speed Power Inverters

The M611 module contains 14 high-speed power inverters. Each inverter has a maximum propagation delay of 12 ns.

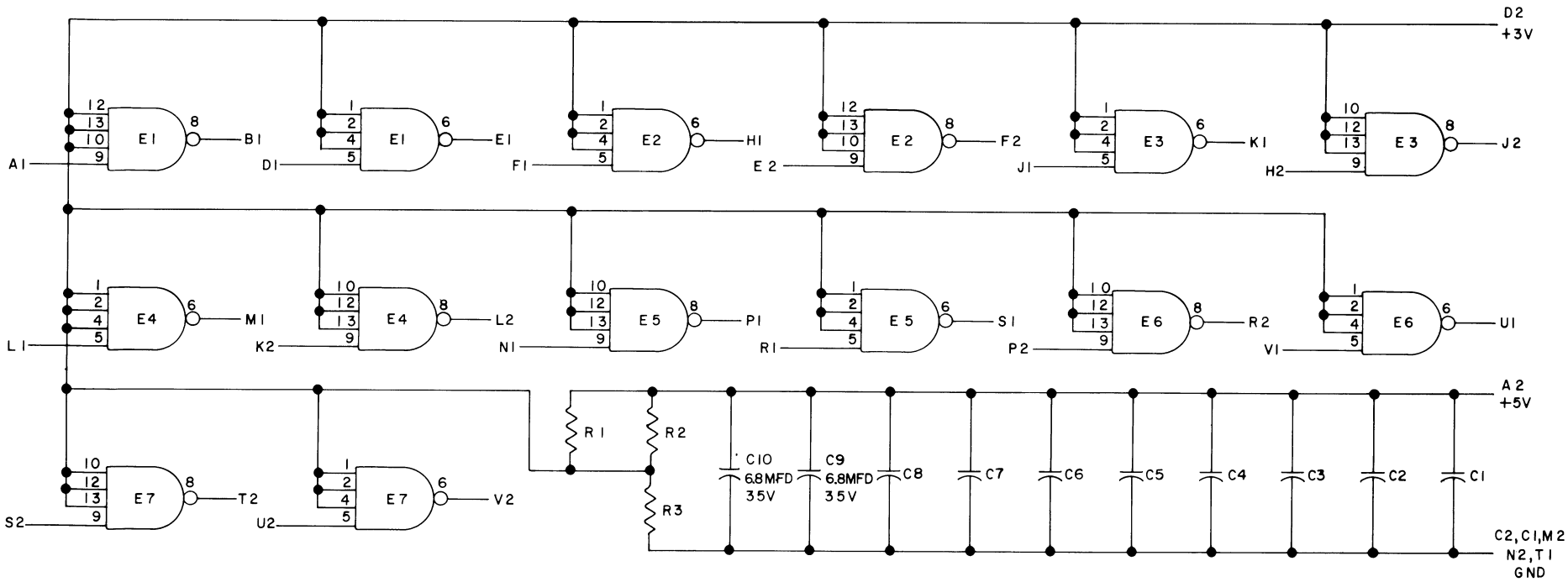
The following are the input, output, and power characteristics of the M611 module.

INPUTS: Each inverter input presents 1.25 TTL unit loads.

OUTPUTS: Each inverter output is capable of driving up to 36 unit loads.

POWER: Power dissipation of the M611 module is 5V at 240 mA (maximum).

SIZE	CODE	NUMBER	REV.
B	CS	M611-0-1	B



UNLESS OTHERWISE INDICATED
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
IC'S ARE DEC74H40
CAPACITORS ARE .01MFD 100V
RESISTORS ARE 220 1/4W 10%

REVISIONS	CHK	CHG NO	REV.
		00001	B

DRN.	Bellis	DATE 5-7-69
CHK'D	C. Yaeger	DATE 5-8-69
ENG	R. Eberhard	DATE 6-16-69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: HIGH SPEED POWER INVERTER M611

SIZE	CODE	NUMBER	REV.
B	CS	M611-0-1	B

PRINTED CIRCUIT REV. A

DEC FORM NO.
DRB 102

3 PINK DIST. 324, 434, 435

M611-2

M617
Power NAND Gates

The M617 contains six 4-input NAND gates, each capable of driving up to 30 unit loads. Gate propagation delay is 25 ns (maximum). Physical configuration and logical operation are identical to the M117.

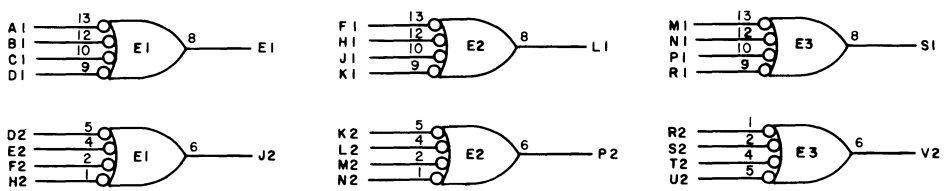
The following are the input, output, and power characteristics of the M617 module.

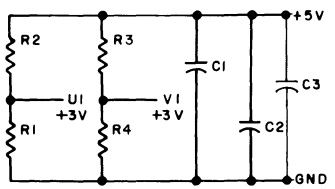
INPUTS: Each input presents 1 unit load.

OUTPUTS: Each output is capable of driving 30 unit loads.

POWER: Power dissipation of the M617 module is 5V at 97 mA (maximum).

+5V —— A 2
NOT USED -15V - —— B2
GND —— C2, T1





NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M617-0-0
R2 & R3	RES 330 1/4W 10% CC	1300293
R1 & R4	RES. 750 1/4W 5% CC	1301401
C1 & C2 & C3	CAP. .01MFD 100V 20% DISC	1001610
E1 THRU E3	INTEGRATED CKT, DEC744ON	1905579

PARTS LIST

REVISIONS	CHK	CHG NO	REV
		6422	A
		6824	B
		00001	C
		00002	C
		00003	E

DRN	W. Waller	DATE	3-15-67
CHK'D		DATE	4-21-67
ENG	L White	DATE	4-21-67
PROD		DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE: 6-4 INPUT NOR BUFFERS M617

SIZE	CODE	NUMBER	REV
B	CS	M617-0-1	E

PRINTED CIRCUIT REV A

M621
Data Bus Drivers

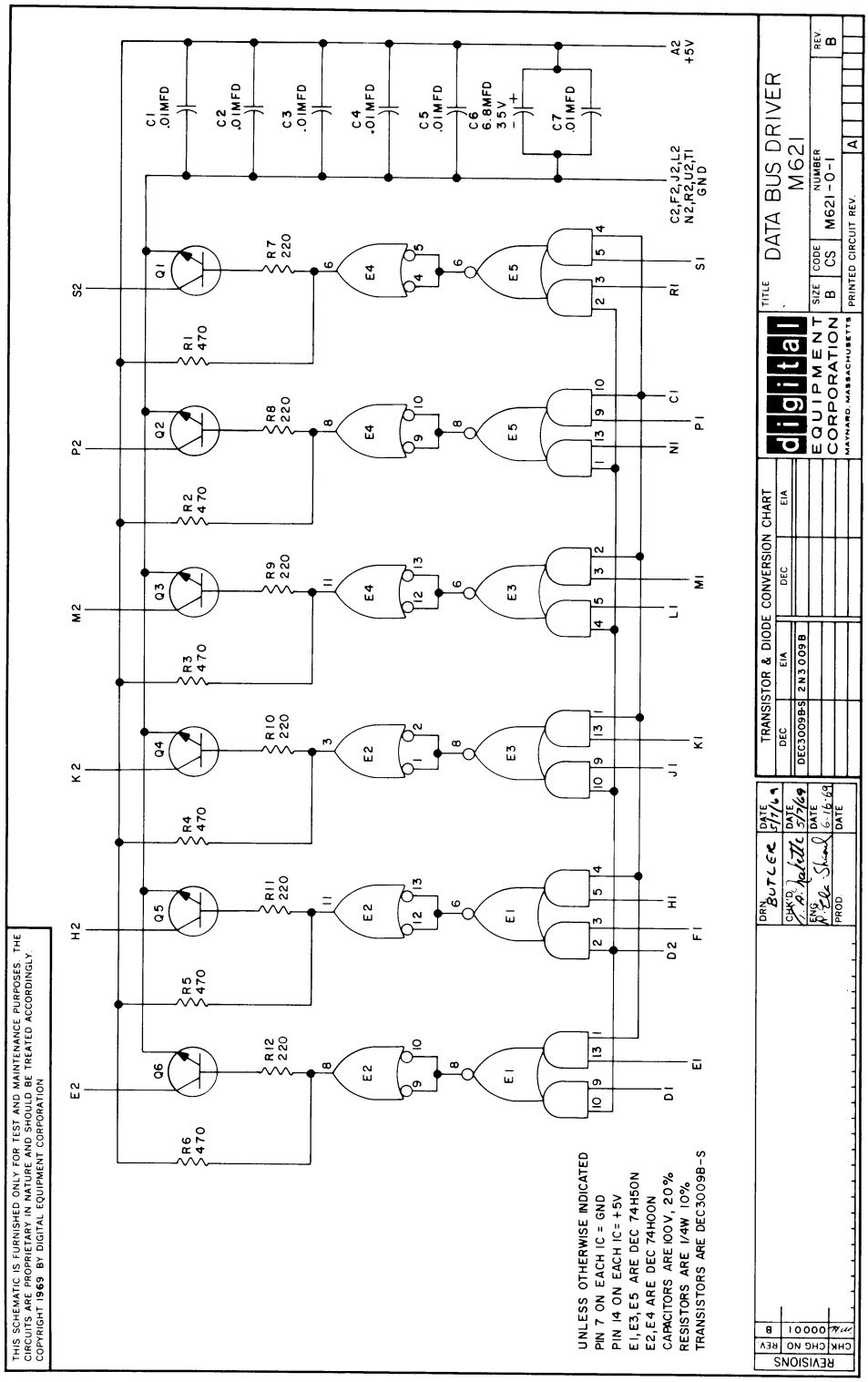
The M621 module contains six open-collector AND-NOR gate drivers. Two separate data inputs can be strobed through each driver. The strobe inputs are common to all six drivers. Propagation delay with a 68Ω resistive load is 55 ns (maximum) for outputs going HIGH and 35 ns (maximum) for outputs going LOW.

The following are the input, output, and power characteristics of the M621 module.

INPUTS: Data inputs present 1.25 unit loads. Strobe inputs present 8 unit loads.

OUTPUTS: Each driver output can sink 100 mA to ground.

POWER: Power dissipation of the M621 module is 5V at 200 mA.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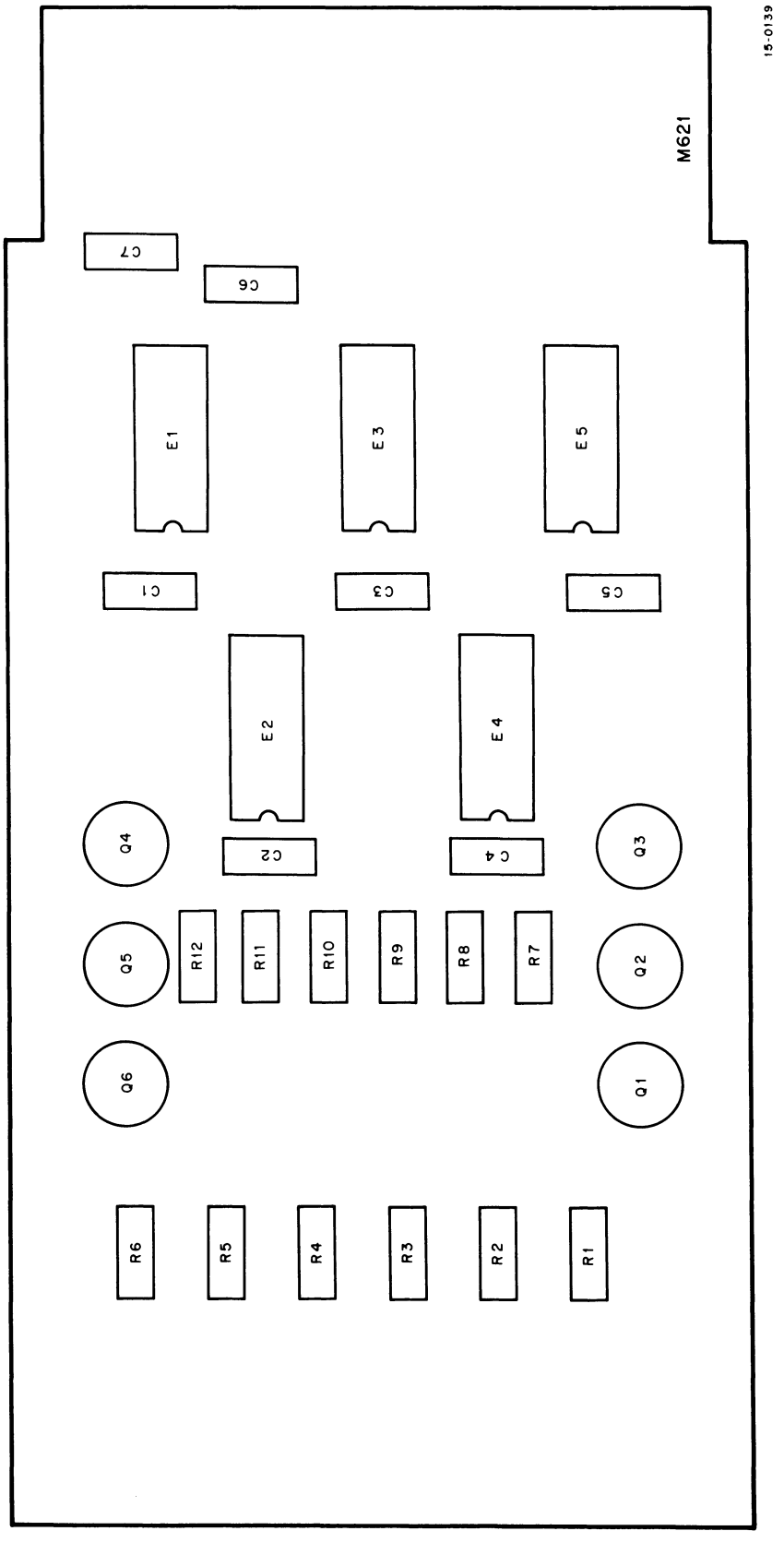
UNLESS OTHERWISE INDICATED
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E3, E5 ARE DEC 74H50N
E2, E4 ARE DEC 74H00N
CAPACITORS ARE 100V, 20%
RESISTORS ARE 1/4W 10%
TRANSISTORS ARE DEC3009B-S
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
DEC3009BS 2N3009B
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
DATA BUS DRIVER
M621
SIZE B
CODE CS
NUMBER M621-0-1
REV B
PRINTED CIRCUIT REV. A
DRN Butler 5/1/69
CHK'D 5/7/69
ENG 6-16-69
PROD
REVISIONS
CHK CHG NO REV
10000 B


15-0139
M621
C7
C6
E1
E3
E5
C1
C3
C5
E2
E4
Q4
C2
C4
Q3
Q5
R12
R11
R10
R9
R8
R7
Q2
Q6
Q1
R6
R5
R4
R3
R2
R1

M622
I/O Bus Drivers

The M622 I/O Bus Driver is an M-series single-height module containing eight I/O bus drivers. Each driver consists of an AND/OR integrated circuit gate and a discrete component open-collector driver.

The following are the input, output, and power characteristics of the M622 module.

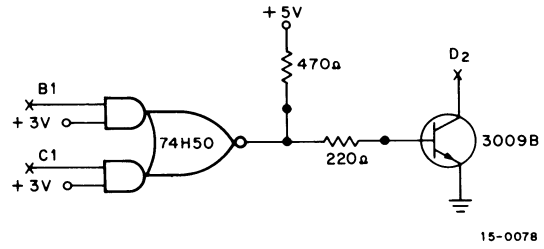
INPUTS: Inputs are standard TTL positive logic levels.
The input load is 1.25 units.

OUTPUTS: Outputs are standard PDP-15 positive I/O bus signals. Output characteristics are:

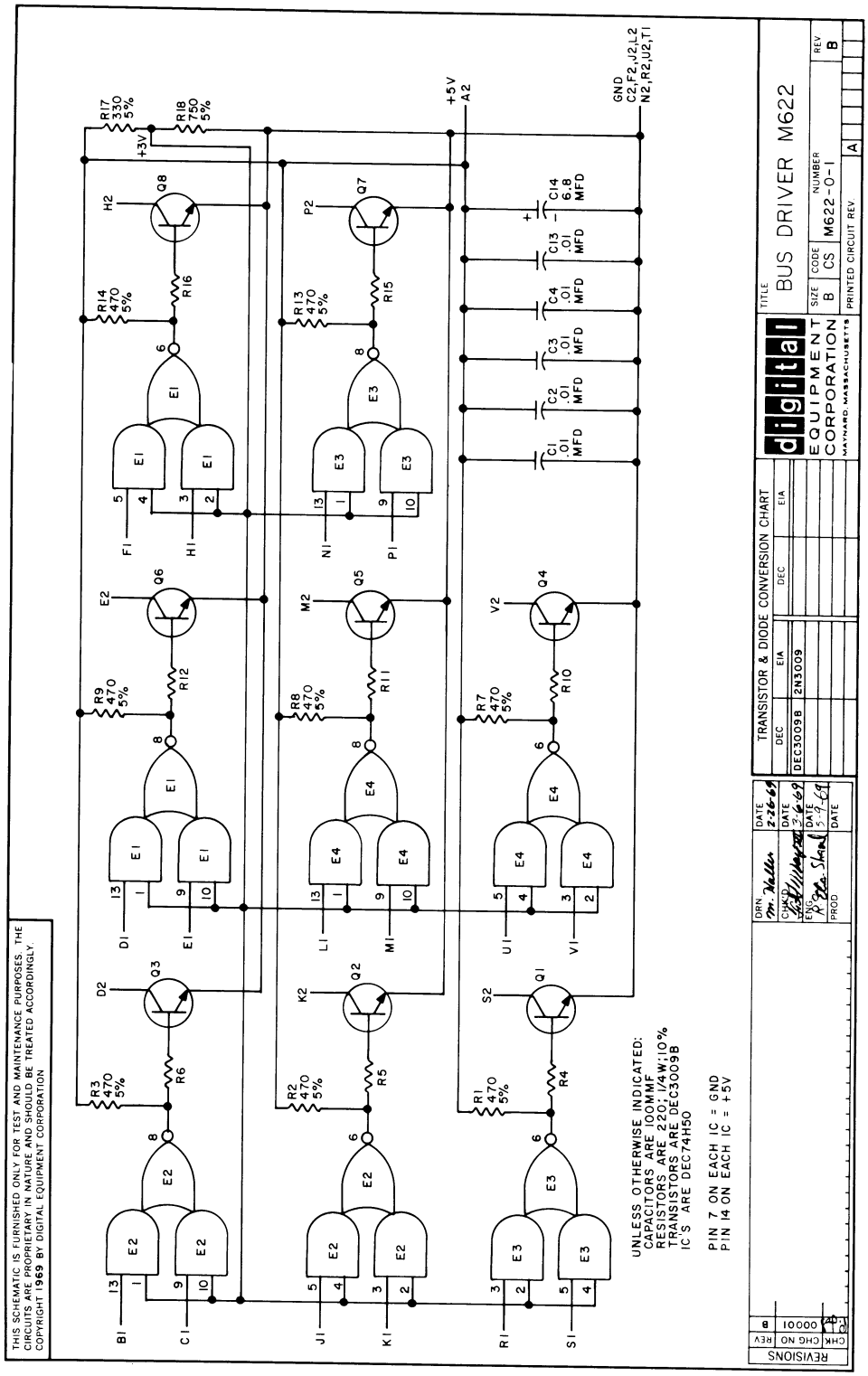
Risetime - 15 ns at the input to the cable
Current sink - 100 mA (maximum) at $V_{ce}sat$ = 0.4V (maximum)
Falltime - 10 ns at the input to the cable
Input-Output Delay - 45 ns (maximum)

POWER: The power dissipation of the M622 module is 1.05W (maximum) at +5V.

The M622 module was designed specifically to drive PDP-15 I/O bus signals for devices that use positive logic modules. The M622 module is pin compatible with the M632 module.



M622 Simplified Diagram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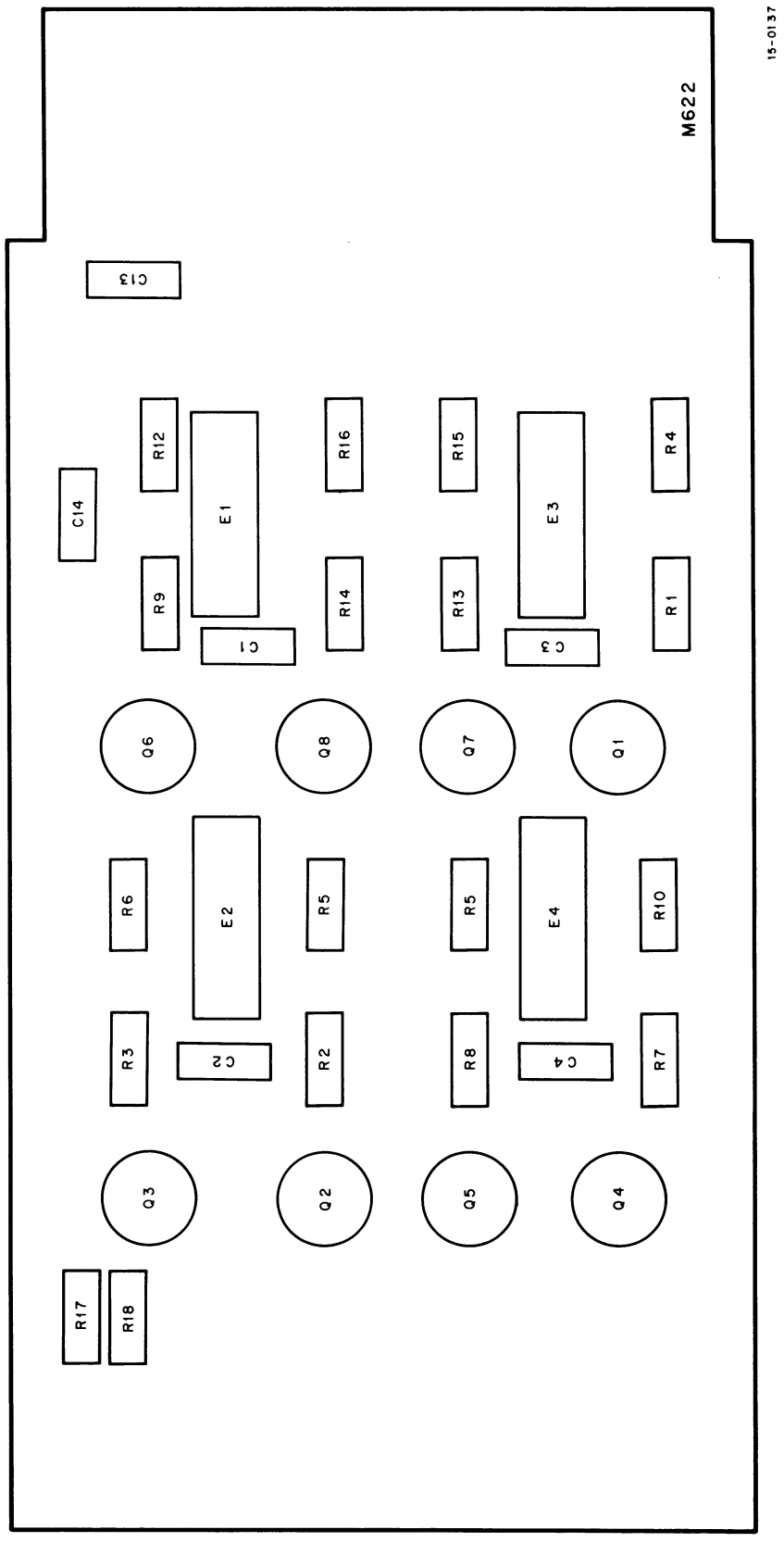
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 100MMF
RESISTORS ARE 220; 1/4W; 10%
TRANSISTORS ARE DEC3009B
IC'S ARE DEC74H50
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
+5V A2
+3V
GND C2,F2,J2,L2 N2,R2,U2,T1
R17 330 5%
R18 750 5%
R14 470 5%
R13 470 5%
R9 470 5%
R8 470 5%
R7 470 5%
R3 470 5%
R2 470 5%
R1 470 5%
C1 .01 MFD
C2 .01 MFD
C3 .01 MFD
C4 .01 MFD
C13 .01 MFD
C14 6.8 MFD
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
DEC3009B 2N3009
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE BUS DRIVER M622
SIZE B CODE CS NUMBER M622-0-1 REV B
PRINTED CIRCUIT REV A
REVISIONS
REV 8 CHG NO 10000 CHK
DRN DATE 2-26-69
CHK DATE
ENG DATE
PROD DATE


M622
15-0137
C13
C14
R12
E1
R16
R15
E3
R4
R9
R14
R13
R1
C1
C3
Q6
Q8
Q7
Q1
R6
E2
R5
R5
E4
R10
R3
C2
R2
R8
C4
R7
Q3
Q2
Q5
Q4
R17
R18

M627
NAND Power Amplifiers

The M627 combines power amplification with high-speed gating for high fan-out of clock or shift pulses that are to be expanded counters and shift registers. Propagation time between input and output transitions is 12 ns (maximum). To utilize the timing accuracy of this module, wire runs of minimum length are recommended.

The M627 module can also be used as a 4-input NAND gate. In the pulse amplifier application, unused inputs should be connected to the +3V pins provided.

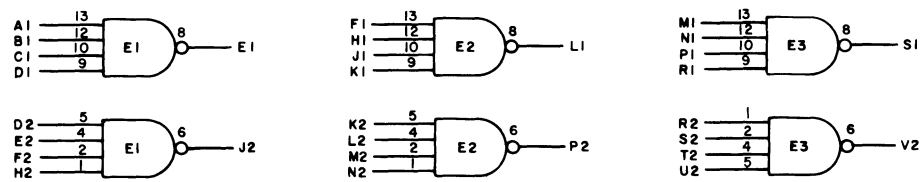
The following are the input, output and power characteristics of the M627 module.

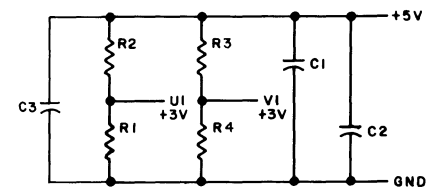
INPUTS: Each input presents 2.5 unit loads.

OUTPUTS: Each output is capable of driving 40 unit loads.

POWER: Power dissipation of the M627 module is +5V at 136 mA (maximum).

+5V ——— A2
NOT USED -15V ——— B2
GND ——— C2, T1





NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
	PARTS LIST	A-PL-M627-0-0
C1 THRU C3	CAP. .01 MFD 100V 20% DISC	1001610
R1 & R4	RES. 750 1/4W 5% CC	1301401
R2 & R3	RES. 330 1/4W 10% CC	1300293
E1 THRU E3	INTEGRATED CKT. DEC74H40	1905586

REVISIONS			
CHK	CHG NO	REV	
Rad	6825	A	
MM	00001	B	
Jm	00002	E	
RR	00003	F	

DRN	M. Waller	DATE 7-18-67
CHK'D	R. Silverman	DATE 7/19/67
ENG	M. Gordon	DATE 7/20
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: POWER AMPLIFIER MODULE M627

SIZE	CODE	NUMBER	REV
B	CS	M627-0-1	F

PRINTED CIRCUIT REV A

M627-2

M628
Block-Bank Address Card

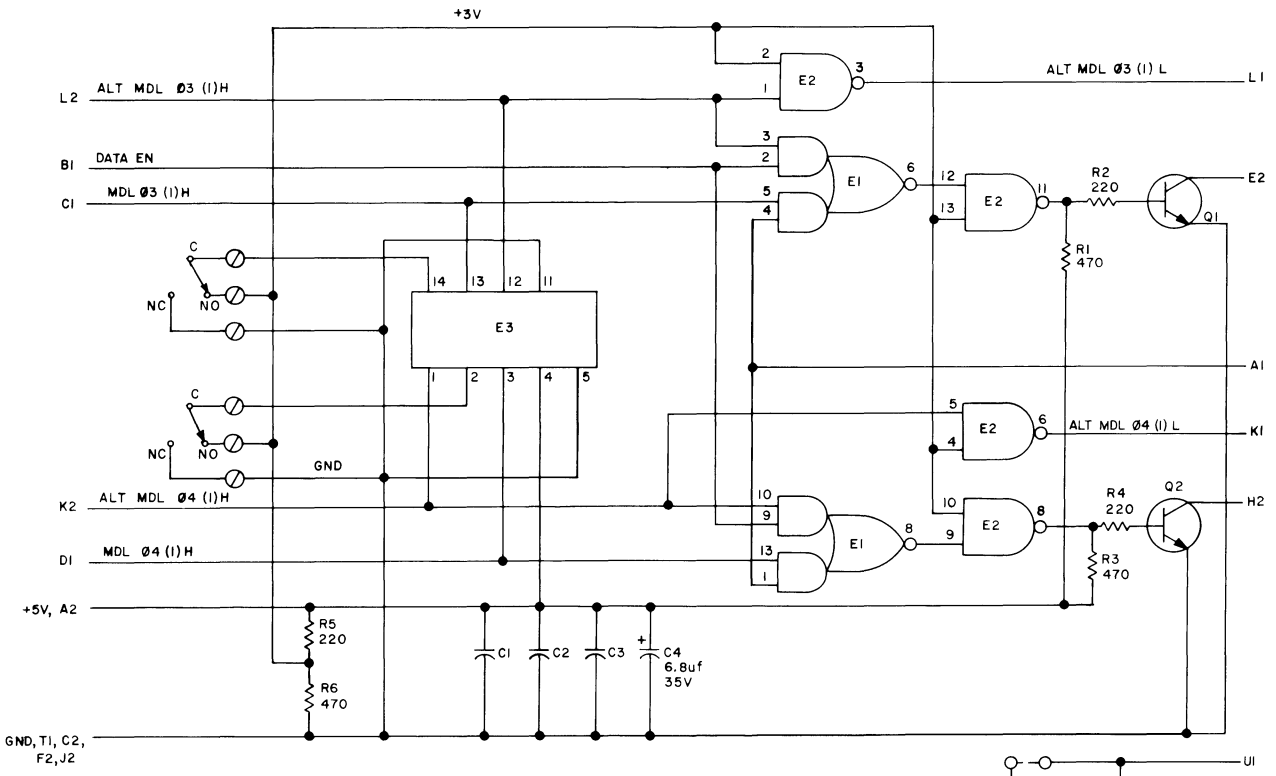
The M628 module contains two 2-position switches, a 2-bit adder, and output gating logic. A maximum of three M628 modules are used in one MX15A memory multiplexer. Address bits 03 and 04 are modified by the module to select the desired memory bank in the PDP-15 system. The module also contains a set of input-output connections that can be jumpered to select a specific memory block.

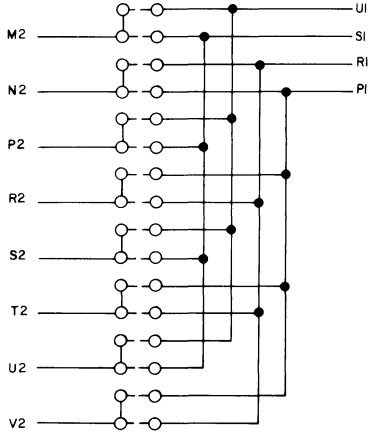
The following are the input, output, and power characteristics of the M628 module.

INPUTS: D1 presents 5.25 unit loads and C1 presents 2.25 unit loads.

OUTPUTS: L1 and K1 are capable of driving 12 unit loads each, while L2 and K2 can drive only 9 unit loads.
E2 and H2 are open-collector outputs capable of sinking up to 100 mA (maximum).
Total propagation delay through the adder and one driver is 100 ns (maximum).

POWER: Power dissipation of the M628 module is 5V at 150 mA (maximum).





UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC3009B
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01uf, 100V, 20%
⊘ INDICATES SPLIT LUGS
O-O INDICATES JUMPERS
E1 IS DEC74H50
E2 IS DEC74H00
E3 IS DEC7482
PIN 7 ON E1, E2=GND
PIN 14 ON E1, E2 =+5V
S1 & S2 ARE MICRO
SWITCH TYPE 6 AT 56-T2

M628-2

REVISIONS	CHK	CHG NO.	REV.
		0001	A
		00002	B

DRN. Nancy Moore	DATE	3/11/70
CHK'D	DATE	3-12-70
ENG.	DATE	4-21-70
	DATE	

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC3009B	2N3009B		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: FIELD BANK ADD CARD M628

SIZE	CODE	NUMBER	REV.
C	CS	M628-0-1	B

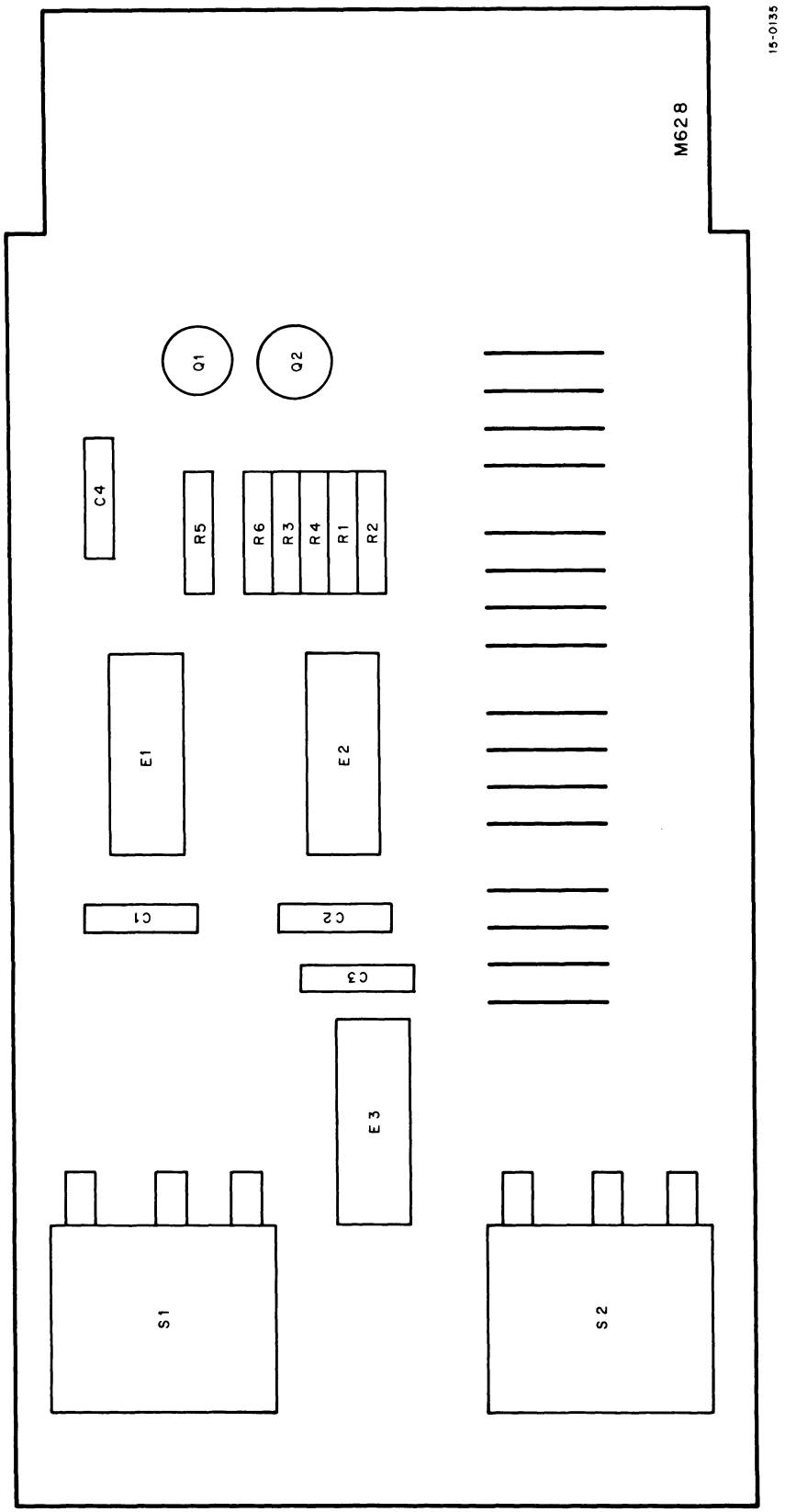
PRINTED CIRCUIT REV.

SIZE C | CODE CS | NUMBER M628-0-1 | REV. B

DEC FORM NO. DRC 102

DIST. 324,434,435

PINK


15-0135
M628
Q1
Q2
C4
R5
R6
R3
R4
R1
R2
E1
E2
C1
C2
C3
E3
S1
S2

M632
Converter-I/O Bus Driver

The M632 is an M-series single-height module containing eight converter-I/O bus driver circuits. It accepts positive logic signals and converts them to negative logic levels. Each driver consists of a TTL input gate and a negative open-collector output driver clamped to ground and -3V.

The following are the input, output, and power characteristics of the M632 module.

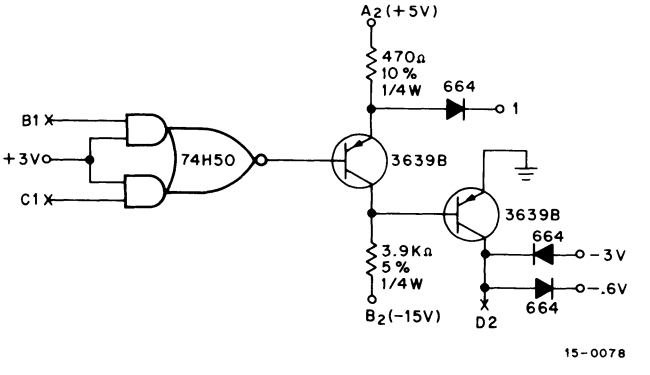
INPUTS: The inputs to the M632 are standard TTL positive logic levels. The input current load at 0V is 1.25 units.

OUTPUTS: Outputs are standard negative logic levels. Output characteristics are:

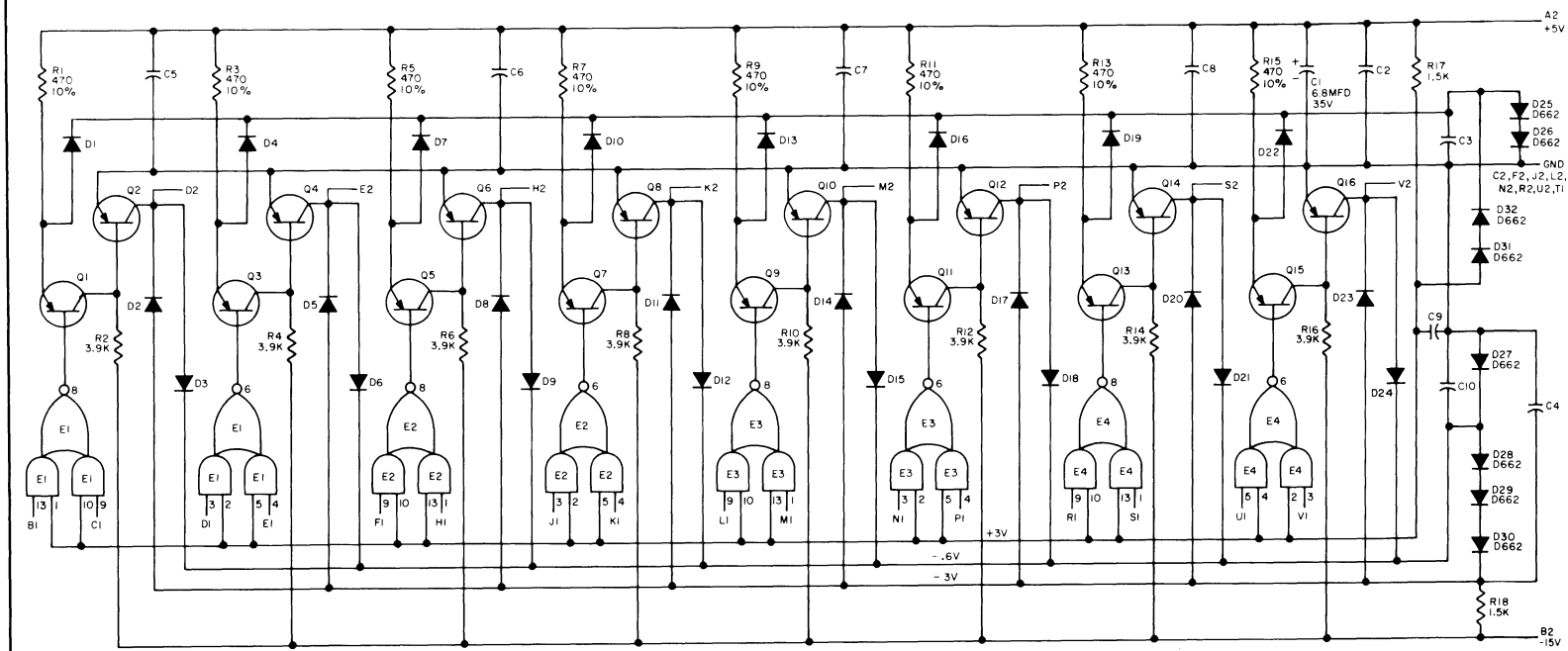
Risetime - 15 ns
Falltime - 15 ns with 1.5 kΩ to -15V at output
Input-Output Delay - 50 ns (maximum)

POWER: Power dissipation in the M632 module is 600 mW from -15V (maximum) and 900 mW from +5V (maximum).

This driver is used to convert positive logic signals to negative logic levels that drive the PDP-9 negative I/O bus. The M632 module is pin-compatible with the M622 module.



M632 Simplified Diagram



UNLESS OTHERWISE INDICATED:
- RESISTORS ARE 1/4W, 5%
- DIODES ARE D664
- TRANSISTORS ARE DEC3639B
- IC'S ARE DEC74H50
- PIN 7 ON EACH IC = GND
- PIN 14 ON EACH IC = +5V
- CAPACITORS ARE .01 MFD

REVISIONS

CHK	CHG NO	REV

DRN.	BUTLER	DATE 4.30.69
CHK'D	C.A. Talcitte	DATE 5/2/69
ENG.		DATE
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

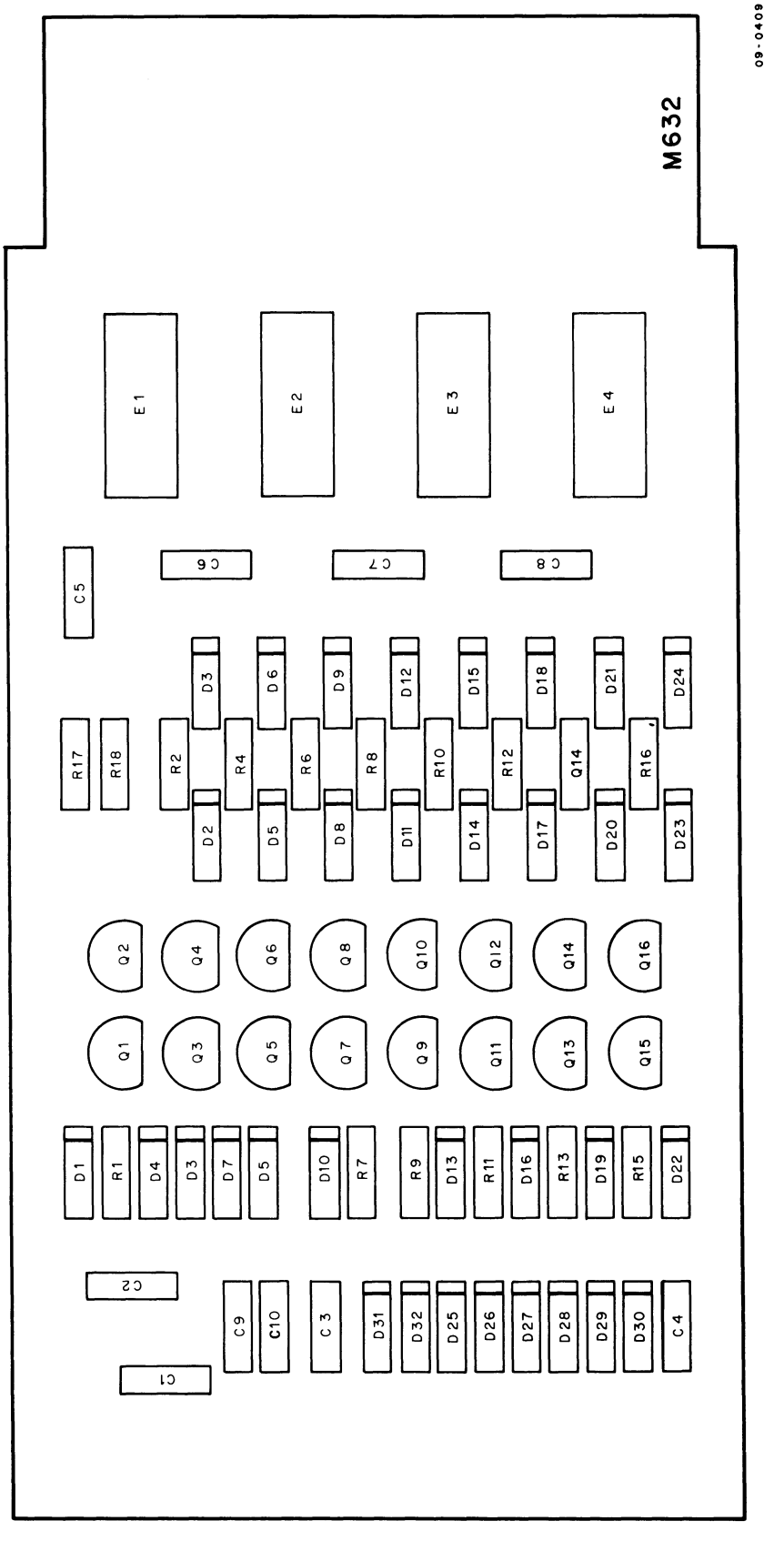
DEC	EIA	DEC	EIA
D664	IN3606		
D662	IN645		
DEC3639B	2N3639		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE POSITIVE INPUT CONVERTER DRIVER M632

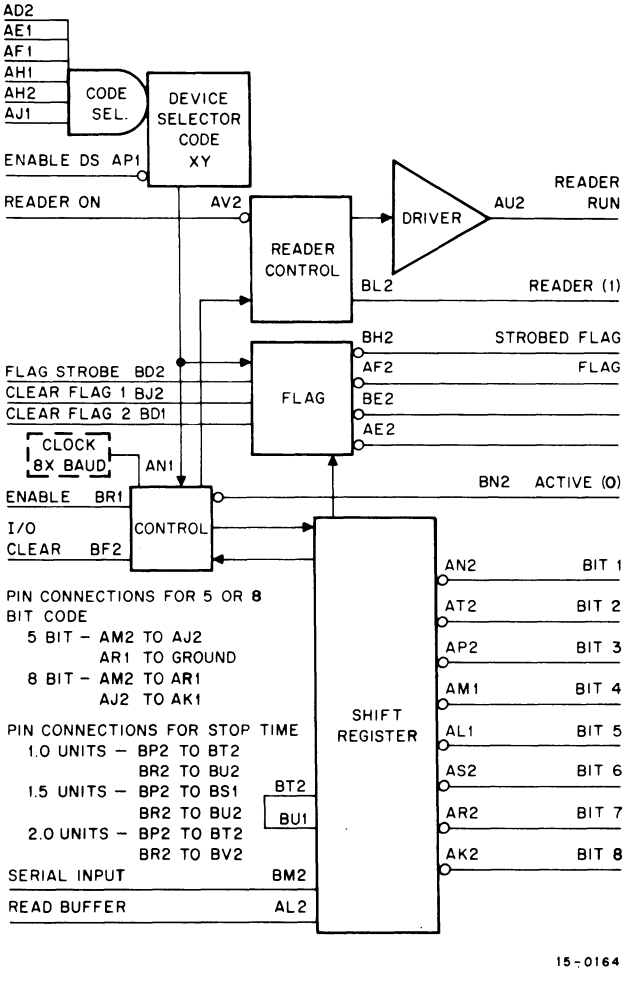
SIZE	CODE	NUMBER	REV
C	CS	M632-0-1	

PRINTED CIRCUIT REV. A


M632
09-0409
E1
E2
E3
E4
C5
C6
C7
C8
R17
R18
R2
R4
R6
R8
R10
R12
Q14
R16
D3
D6
D9
D12
D15
D18
D21
D24
D2
D5
D8
D11
D14
D17
D20
D23
Q2
Q4
Q6
Q8
Q10
Q12
Q14
Q16
Q1
Q3
Q5
Q7
Q9
Q11
Q13
Q15
D1
R1
D4
D3
D7
D5
D10
R7
R9
D13
R11
D16
R13
D19
R15
D22
C2
C1
C9
C10
C3
D31
D32
D25
D26
D27
D28
D29
D30
C4

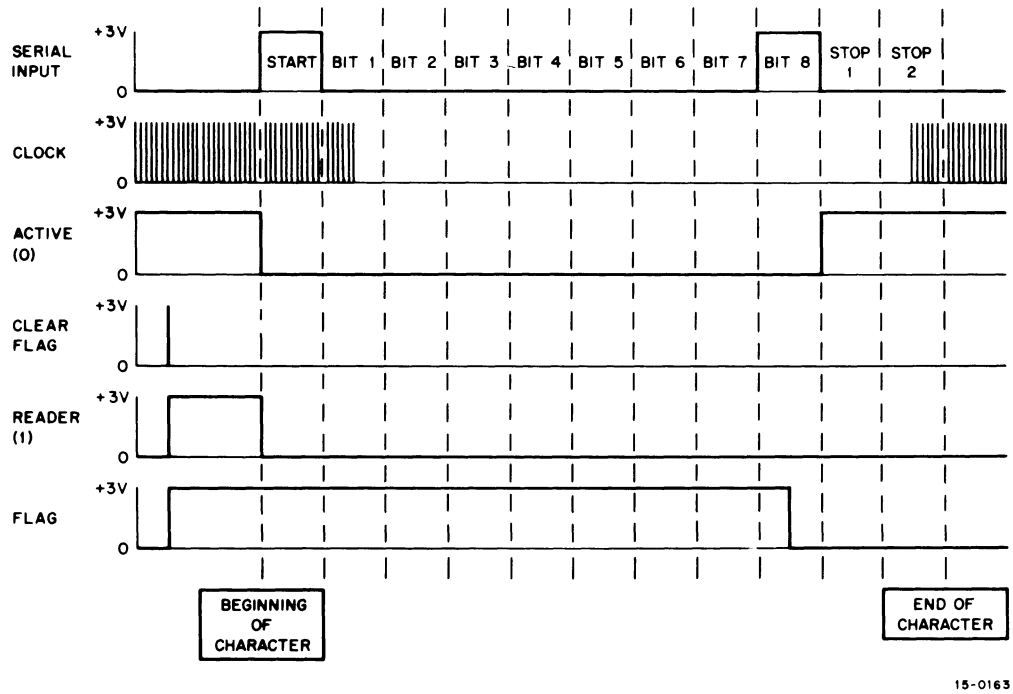
M706
Teletype Receiver

The M706 Teletype Receiver is a serial-to-parallel Teletype code converter self-contained on a double-height module. This module includes all of the serial-to-parallel conversion, buffering, gating, and timing (excluding only an external clock) necessary to transfer information in an asynchronous manner between a serial data line or Teletype device and a parallel binary device. Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units; or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the M706 through the use of different pin connections on the module. In the PDP-15, the Teletype receiver is connected to assemble 8-bit



M706 Simplified Diagram

characters consisting of 11 units. When conversion is complete, the start and stop bits accompanying the serial character are removed. The serial character is expected to be received with the start bit first, followed by bits 1 through 8 in order, and completed by the stop bits. Coincident with reception of the center of bit 8, the FLAG output goes LOW, indicating that a new character is ready for transmission into the parallel device. The parallel data is available at the BIT 1 through BIT 8 outputs until the beginning of the start bit of a new serial character is received on the SERIAL input (see the timing diagram for additional information).



M706 Timing Diagram

In addition to the above listed features, the M706 includes the necessary logic to provide rejection of spurious start bits less than 1/2-unit long, and to also provide half-duplex system operation in conjunction with the M707. Device selector gating is also provided; thus, this module can be used on the positive I/O bus of a digital system.

The following are the input, output, and power characteristics of the M706 Teletype Receiver.

INPUTS: All inputs present one TTL unit load (except where noted). When input pulses are required, they must have a width of 50 ns or greater.

CLOCK: The clock frequency must be eight times the serial input bit rate (baud rate). This input can be either pulses or a square wave. Input loading on the CLOCK line is three unit loads.

ENABLE: The ENABLE input, when brought to ground, inhibits reception of new characters. It can be grounded any time during character reception, but returned HIGH only between the time the FLAG output goes to ground and a new character start bit is received at the serial input. When not used, the ENABLE input should be tied to a source of +3V.

I/O CLEAR: A HIGH level or positive pulse at this input clears the flag and initializes the state of the control. When not used, or during reception, the I/O CLEAR input is grounded.

CODE SELECT Inputs: When a positive AND condition occurs at the CODE SELECT inputs, the following signals can assume their normal control functions: FLAG STROBE; READ BUFFER; and CLEAR FLAG 1. These inputs are frequently used to multiplex receiver modules when a signal such as READ BUFFER is common to many modules. The inputs are also used for device selector inputs when the M706 is used on the positive I/O bus of a digital system. The CODE SELECT inputs must be present at least 50 ns prior to any of the three signals that they enable. If it is desired to bypass the CODE SELECT inputs, they can be left open and the ENABLE D. S. line tied to ground.

CLEAR FLAG 1: A HIGH level or positive pulse at the CLEAR FLAG 1 input while the CODE SELECT inputs are all HIGH clears the flag. When not used, this line should be grounded. Propagation delay from input rise until the flag is cleared is a maximum of 100 ns. The flag cannot be set if this input is held HIGH.

CLEAR FLAG 2: A HIGH level or positive pulse at the CLEAR FLAG 2 input, independent of the state of the CODE SELECT inputs, clears the flag. All other characteristics are identical to those of CLEAR FLAG 1.

FLAG STROBE: If the flag is set and the CODE SELECT inputs are all HIGH, a positive pulse at the FLAG STROBE input generates a negative-going pulse at the STROBED FLAG output. Propagation delay from the strobe to output is a maximum of 30 ns.

READ BUFFER: A HIGH level or positive pulse at the READ BUFFER input while the CODE SELECT inputs are all HIGH transfers the state of the shift register to outputs BIT 1 through BIT 8. Final parallel character data can be read by this input as soon as the FLAG output goes to ground. Output data is available a maximum of 100 ns after the rising edge of this input. See the timing diagram for additional information.

READER ON: A LOW level or ground at the READER ON input turns on the internal reader flip-flop. This element is turned off at the beginning of a received character start bit. The READER ON input can also be pulsed by tying it to one of the signals derived at output pins AE2 or BE2.

SERIAL Input: Serial data received on the SERIAL input has a logical 0 (space) equal to +3V and a logical 1 (mark) of ground. The input receiver on the M706 is a Schmitt trigger with hysterisis thresholds of nominal 1.0V and 1.7V. This allows the SERIAL input data to be filtered up to 10 percent of bit width on each transition to remove noise. The SERIAL input is diode-protected from voltage overshoot above +5.9V and from voltage undershoot below -0.9V. Input loading is four unit loads.

OUTPUTS: All outputs can drive ten unit loads (unless otherwise specified).

BITS 1 through 8: A READ BUFFER input signal transfers the shift register contents to those outputs with a received logical 1 appearing as a ground output. If the READ BUFFER input is not present, all outputs are at logical 1. When the M706 is used for reception of 5-bit character codes, the output data appears on output lines BIT 1 through 5; and BITS 6, 7, 8 receive logical zeros.

ACTIVE (0): The ACTIVE (0) output goes LOW at the beginning of the start bit of each received character and returns HIGH at the completion of reception of bit 8 for an 8-bit character, or bit 5 for a 5-bit character. Because this signal uses from 0V to +3V (at 1/2-bit time after the FLAG output goes to ground) it can be used to clear the flag through the CLEAR FLAG 2 input while the FLAG output, after being inverted, can strobe parallel data out when connected to READ BUFFER.

If an M706 and M707 are to be used in half-duplex mode, this output should be tied to the WAIT input of the M707 to inhibit M707 transmission during M706 reception. Output drive is eight unit loads.

FLAG: The FLAG output falls from +3V to ground when the serial character data has been fully converted to parallel form. Relative to serial bit positions, this occurs during the center of either bit 8 or bit 5, depending on the respective character length. If the M706 is receiving at a maximum character rate (i.e., one character immediately following another), the parallel output data is available for transfer from the time the FLAG output falls to ground until the beginning of a new start bit. This is stop-bit time plus 1/2-bit time.

STROBED FLAG: The STROBED FLAG output is the NAND realization of the inverted FLAG output and FLAG STROBE.

READER (1): Whenever the internal reader flip-flop is set by the READER ON input, the READER output rises to +3V. The flip-flop is cleared whenever a start bit of a new character is received on the SERIAL input.

READER RUN: The READER RUN output is used with DEC modified 33 ASR and 35 ASR Teletypes that have relay-controlled paper tape readers. The READER RUN output can drive a load of 20 mA at +0.7V. The common end of the load can be returned to any negative voltage not exceeding -20V.

PIN AE2: The PIN AE2 output is the logical realization of NOT (CLEAR FLAG 1 or CLEAR FLAG 2 or I/O CLEAR) and is a +3V-to-ground output level or pulse, depending on the input. The signal is used to pulse READER ON for control of READER RUN in the system.

PIN BE2: The PIN BE2 output is brought from +3V to ground by an enabled CLEAR FLAG 1 input. It can be connected to READER ON for a different form of control of READER RUN.

+3 VOLTS Pin AD1 can drive ten unit loads at a +3V level.

POWER: Power dissipation of the M706 is 5V at 400 mA (maximum).

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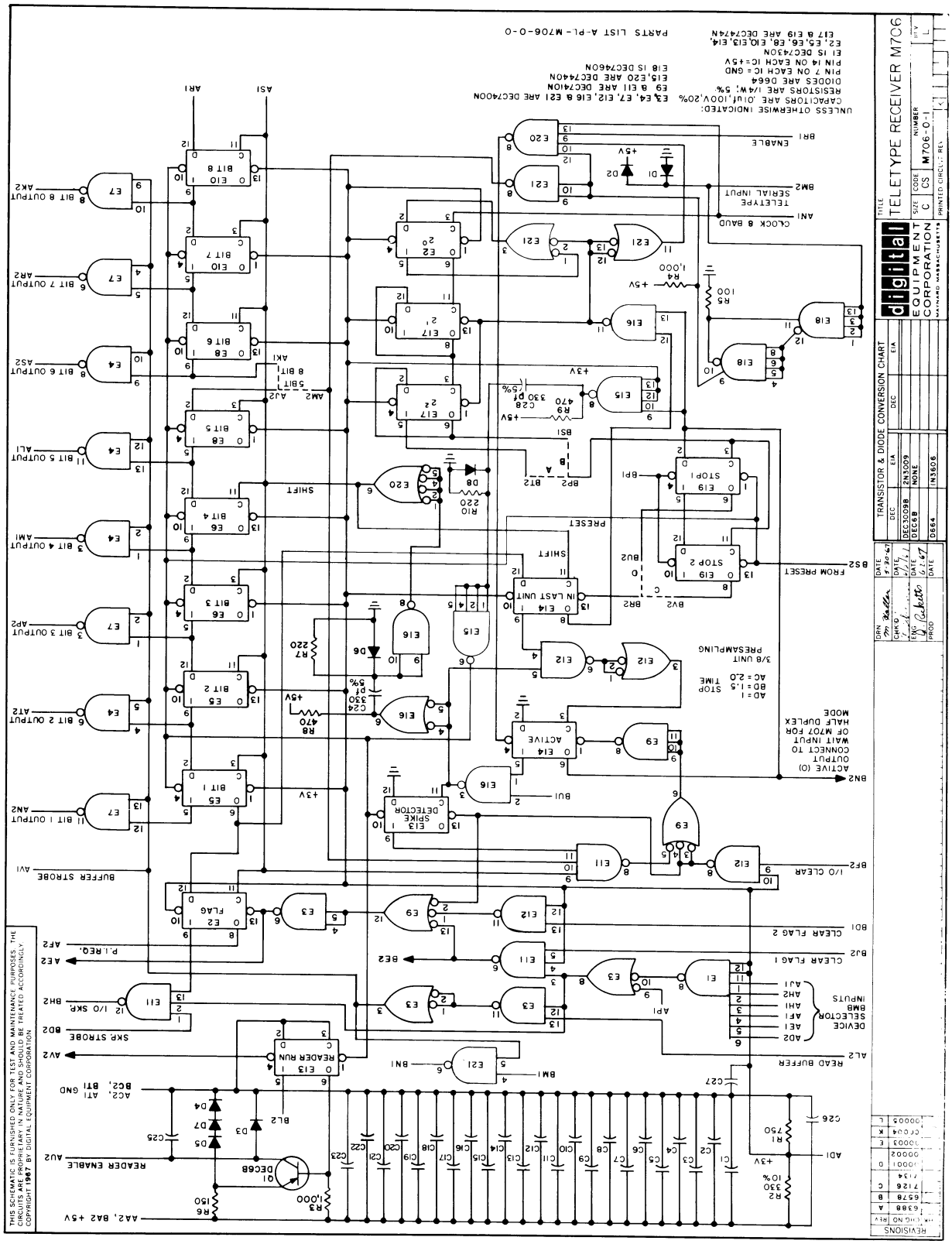
TELETYPE RECEIVER M706
digital EQUIPMENT CORPORATION
TRANSISTOR & DIODE CONVERSION CHART
PARTS LIST A-PL-M706-0-0
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01uf,100V,20%
RESISTORS ARE 1/4W, 5%
DIODES ARE D664
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1 IS DEC74ON
E17 & E19 ARE DEC74ON
E18 IS DEC74610N
E9 & E11 ARE DEC74ION
E15,E20 ARE DEC7440N
E3, E4, E7, E12, E16 & E21 ARE DEC7400N
E2, E5, E6, E8, E10, E13, E14, E17 & E19 ARE DEC7474N
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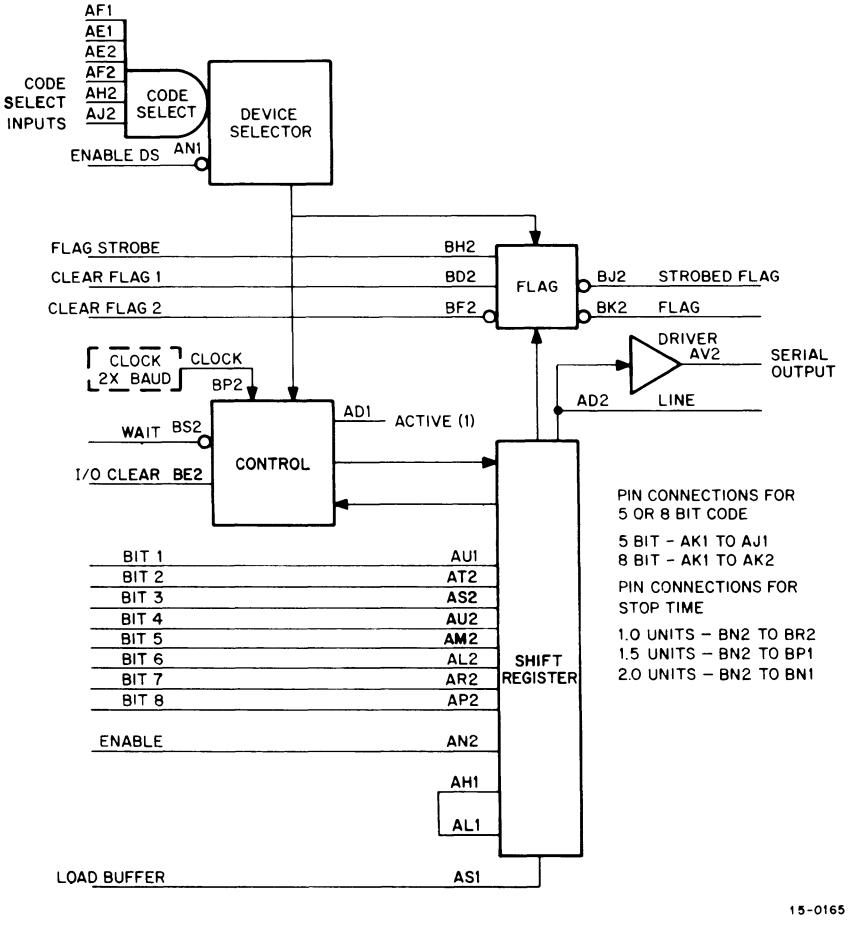
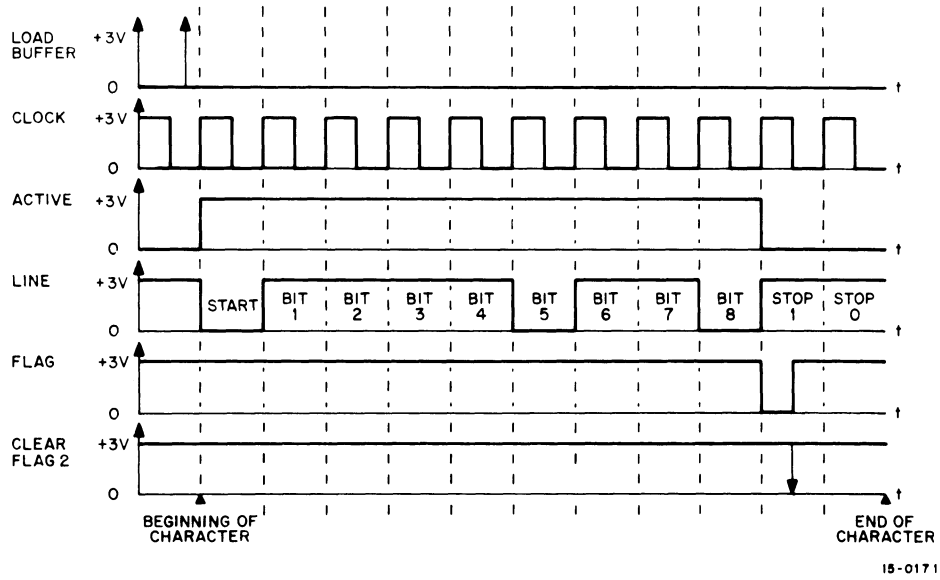
15-0155
M706
C23
C22
C26
D3
D5
D7
D4
Q1
R3
D6
R7
C24
R6
C25
E1
E4
E7
E10
E13
E16
E19
C27
C1
C4
C7
C10
C13
C16
C19
R2
R8
R1
E2
E5
E8
E11
E14
E17
E20
C2
C5
C8
C11
C14
C17
C20
C28
R9
R4
R10
D8
D2
D1
R1
E3
E6
E9
E12
C15
E15
E18
E21
C3
C6
C9
C12
C18
C21

M707
Teletype Transmitter

The M707 Teletype Transmitter is a parallel-to-serial Teletype code converter self-contained on a double-height module. This module includes all of the parallel-to-serial conversion, buffering, gating, and timing (excluding only an external clock) necessary to transfer information in an asynchronous manner between a parallel binary device and a serial data line or Teletype device. Either a 5-bit or an 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character (or a 10.0, 10.5, or 11.0 unit serial character) by the M707 through the use of different pin connections on the module. When conversion is complete, the necessary start bit and selected stop bits (1.0, 1.5, or 2.0 units) have been added to the original parallel character and transmitted over the serial line. In the PDP-15, the Teletype transmitter is connected to assemble 8-bit characters consisting of 11 units.



M707 Simplified Diagram



M707 Timing Diagram

The serial character is transmitted with the start bit first, followed by bits 1 through 8 in order, and completed by the stop bits. Coincident with the stop bit being put on the serial line, the FLAG output goes LOW indicating that the previous character has been transmitted and a new parallel character can be loaded into the M707. Transmission of this new character does not occur until the stop bits from the previous character are completed. See the timing diagram for additional information.

In addition to the above listed features, the M707 includes the necessary gating so that it can be used in a half-duplex system with the M706. Device selector gating is also provided to allow this module to be used on the positive bus of a digital system.

The following are the input, output, and power characteristics of the M707 Teletype Transmitter.

INPUTS: All inputs present one TTL unit load with the exception of the CLOCK input, which presents ten unit loads. Where the use of input pulses is required, the pulse width must be 50 ns or greater.

CLOCK: The clock frequency must be twice the serial output bit rate. The CLOCK input can be either pulses or a square wave.

BITS 1 through 8: A HIGH level at the BITS 1 through 8 inputs is reflected as a logic 1 or mark in the serial output. When a 5-bit code is used, BIT inputs 1 through 5 should contain the parallel data; BIT 6 should be considered as an enable; and BITS 7, 8, and ENABLE should be grounded.

ENABLE: The ENABLE input provides the control flexibility necessary for transmitter multiplexing. When grounded during a LOAD BUFFER pulse, the ENABLE input prevents transmission of a character. The ENABLE input can be driven from the output of an M161 for scanning purposes or, in the case of a single transmitter, tied to +3V.

WAIT: If the WAIT input is grounded prior to the stop bits of a transmitted character, the input then holds transmission of a succeeding character until the input is brought to a HIGH level. A ground on this line does not prevent a new character from being loaded into the shift register. This line is normally connected to ACTIVE (0) on a M706 in half-duplex two wire systems. When not used, the line should be tied to +3V.

CODE SELECT Inputs: When a positive AND condition occurs at the CODES SELECT inputs, the following signals assume their normal control functions: FLAG STROBE; LOAD BUFFER; and CLEAR FLAG 1. These inputs are frequently used to multiplex transmitter modules when signals such as LOAD BUFFER are common to numerous modules. The CODE SELECT inputs can also be used for device selector inputs when the M707 is used on the positive bus of a digital system. The CODE SELECT inputs must be present at least 50 ns prior to any of the three signals that they enable. If it is desired to bypass the CODE SELECT inputs, they can be left open and the ENABLE D.S. line tied to ground.

CLEAR FLAG 1: A HIGH level or positive pulse at the CLEAR FLAG 1 input while the CODE SELECT inputs are all HIGH clears the flag. When not used, this line should be grounded. Propagation delay from input rise until the flag is cleared at the FLAG output is a maximum of 100 ns. The flag cannot be set if the CLEAR FLAG 1 input is held at logic 1.

CLEAR FLAG 2: A LOW level or negative pulse at the CLEAR FLAG 2 input clears the flag. When not used, the CLEAR FLAG 2 input should be tied to +3V. The flag remains cleared if this input is grounded. Propagation from input fall to flag output rise is a maximum of 80 ns. If it is desired to clear the flag on a LOAD BUFFER pulse, CLEAR FLAG 2 can be tied to pin AR1 of the module.

FLAG STROBE: If the flag is set and the CODE SELECT inputs are all HIGH, a positive pulse at the FLAG STROBE generates a negative-going pulse at the STROBED FLAG output. Propagation delay from the strobe to output is a maximum of 30 ns.

I/O CLEAR: A HIGH level or positive pulse at the I/O CLEAR input clears the flag, clears the shift register, and initializes the state of the control. This signal is not necessary if the first serial character transmitted after power turn-on is not required to be correct. When not used, or during transmission, the I/O CLEAR input should be at ground.

LOAD BUFFER: A HIGH level or positive pulse at the LOAD BUFFER input while the CODE SELECT inputs are all HIGH loads the shift register buffer with the character to be transmitted. If the ENABLE input is HIGH when the LOAD BUFFER input occurs, transmission begins as soon as the stop bits from the previous character are counted out. If a level is used, it must be returned to ground within one bit time (twice the period of the clock).

OUTPUTS: All outputs present normal TTL logic levels except the serial output driver, which is an open collector PNP transistor with emitter returned to +5V.

SERIAL Output: This open collector PNP transistor output can drive 20 mA into any load returned to a voltage between +4V and -15V. A logical output or mark is +5V, and a logical 0 or space is an open circuit. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a high-speed silicon diode to the output and the diode anode to the coil supply voltage.

LINE: The LINE output can drive ten TTL unit loads and presents the SERIAL output signal with a logical 1 as +3V and a logical 0 as ground.

FLAG: The FLAG output falls from +3V to ground at the beginning of the stop bits driving a character transmission. The M707 can then be reloaded and the flag cleared (set to +3V). The FLAG output can drive ten TTL unit loads.

STROBED FLAG: The STROBED FLAG output is the NAND realization of the INVERTED FLAG output and FLAG STROBE. Output drive is ten TTL unit loads.

+3V: Pin BJ1 can drive ten TTL unit loads at a +3V level.

POWER: The power dissipation of the M707 is +5V at 375 mA (maximum).

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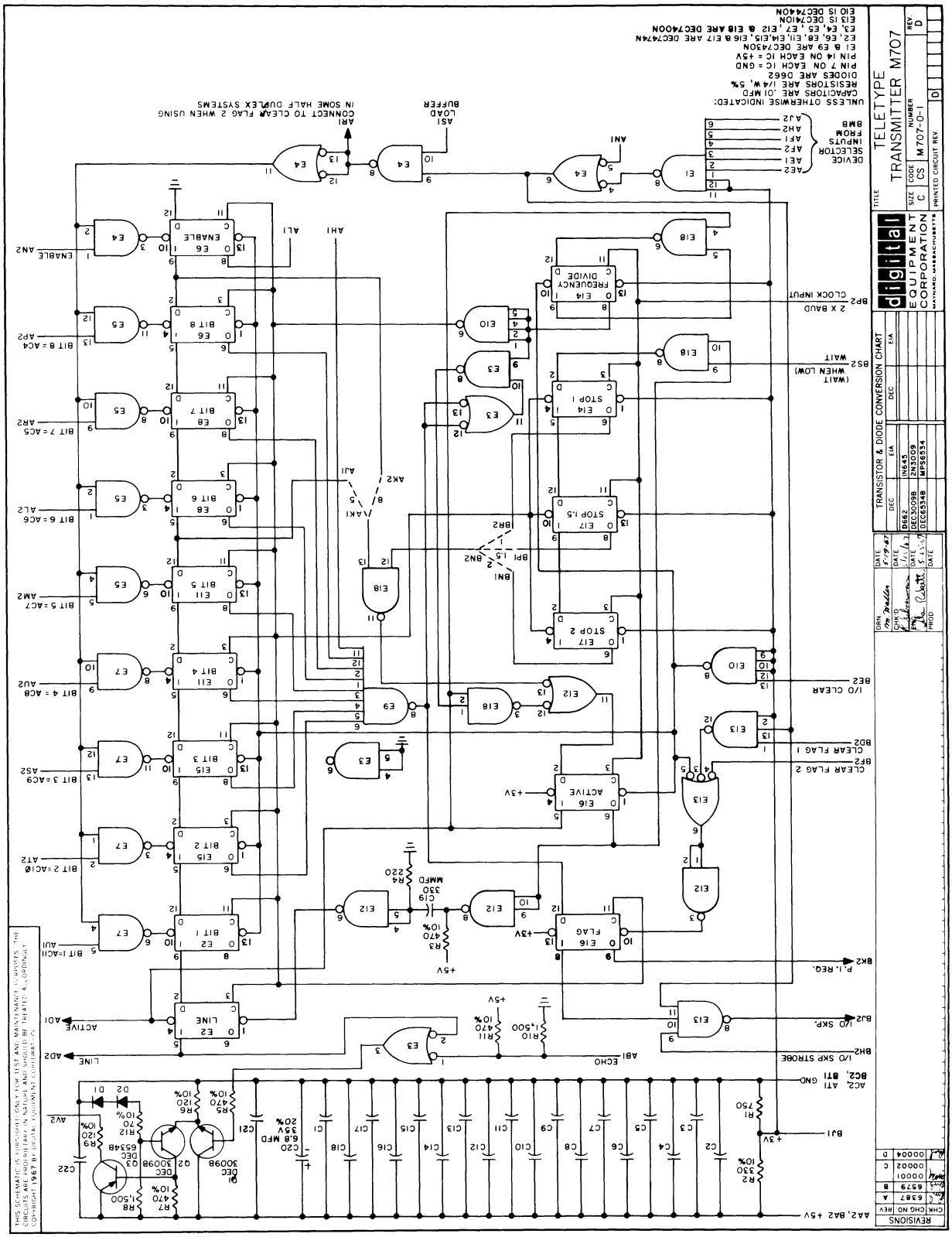
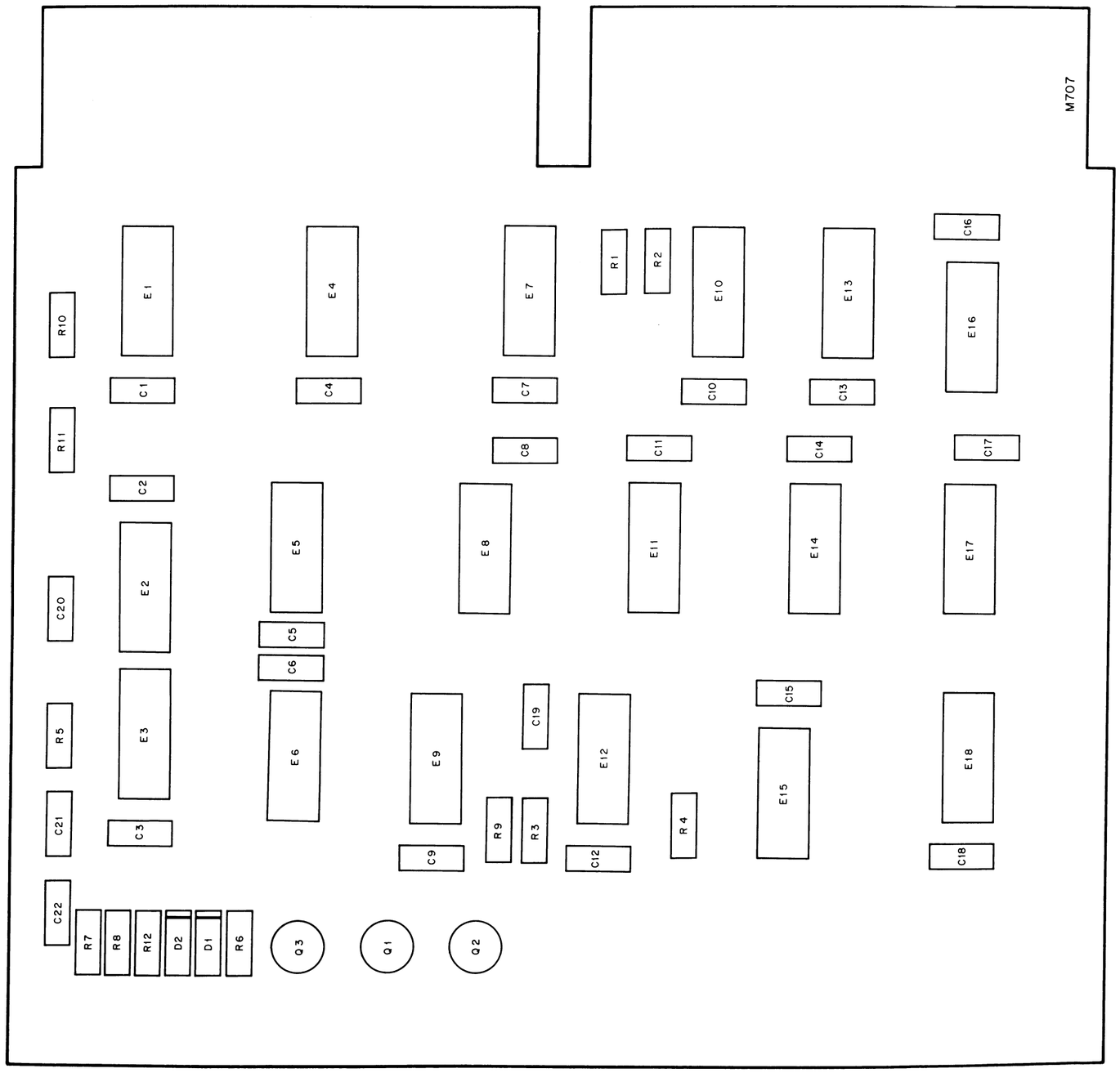

TELETYPE
TRANSMITTER M707
digital
EQUIPMENT
CORPORATION
MAYNARD, MASSACHUSETTS
M707-0-1
TRANSISTOR & DIODE CONVERSION CHART
REVISIONS
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01 MFD
RESISTORS ARE 1/4 W, 5%
DIODES ARE D662
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1 & E9 ARE DEC7430N
E2, E6, E8, E11, E14, E15, E16 & E17 ARE DEC7474N
E3, E4, E5, E7, E12 & E18 ARE DEC7400N
E13 IS DEC7410N
E10 IS DEC7440N
DEVICE SELECTOR INPUTS FROM BM8
2 X BAUD CLOCK INPUT
WAIT (WHEN LOW)
I/O CLEAR
CLEAR FLAG 1
CLEAR FLAG 2
P.I. REQ.
I/O SKP.
I/O SKP STROBE
ECHO
ACTIVE
LINE
BUFFER
LOAD
CONNECT TO CLEAR FLAG 2 WHEN USING IN SOME HALF DUPLEX SYSTEMS
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY
COPYRIGHT 1967 BY DIGITAL EQUIPMENT CORPORATION


M707
15-0158
R10
R11
C20
R5
C21
C22
R7
R8
R12
D2
D1
R6
Q3
Q1
Q2
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
R1
R2
R9
R3
R4
C16
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18

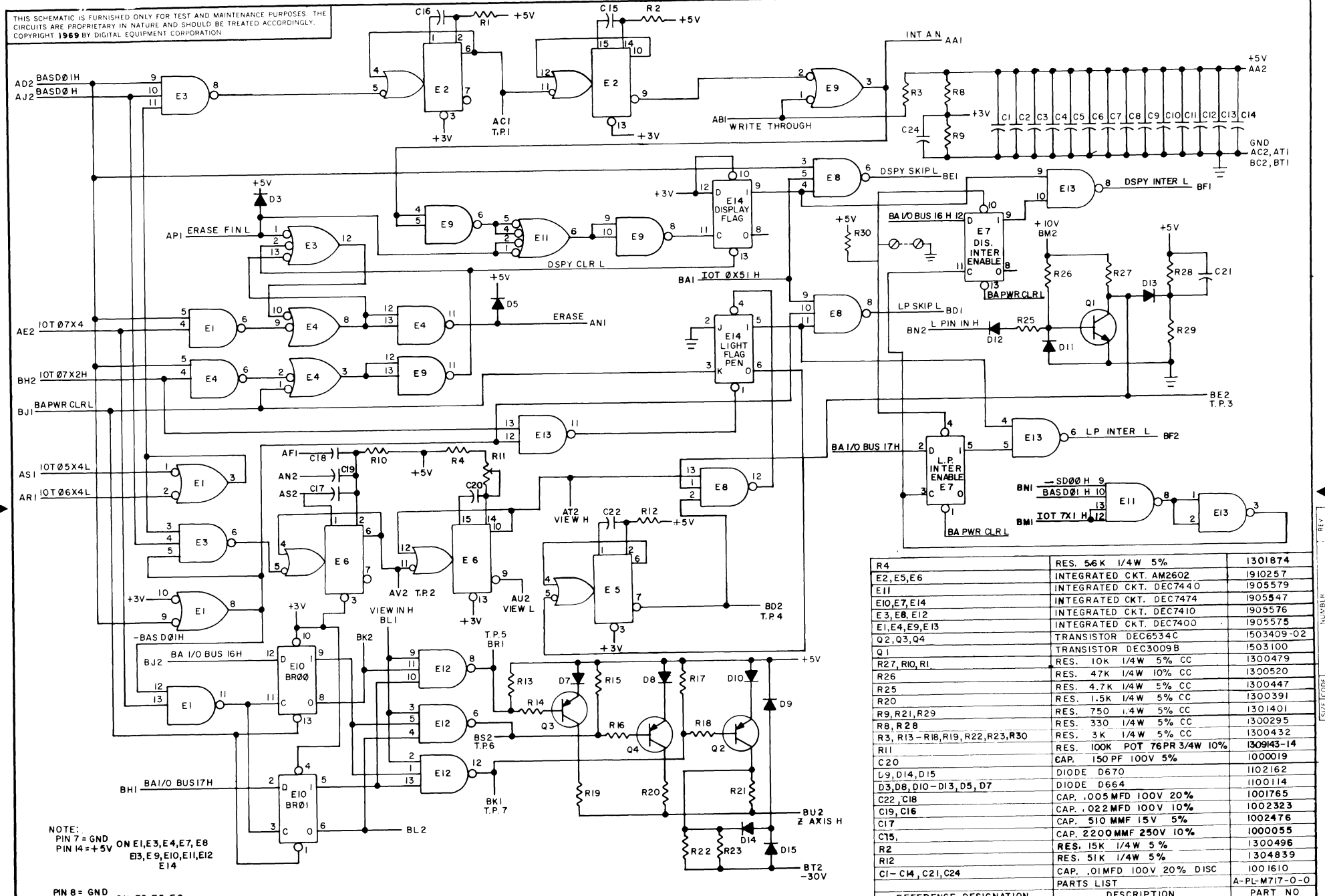
M717
Display Control VP15

The M717 module contains the timing and control circuits required by the VP15 point-plotting display. Since any one of three scopes can be used in the VP15 display, the M717 module incorporates the necessary control circuits for all three scopes. The scopes that can be used are the Tektronix RM503, the DEC VR12, and the Tektronix 611 storage tube in both the store and nonstore modes. A simple patching arrangement selects the required control circuits for a specific scope. The timing circuits on the module provide the necessary deflection settling time delays and intensification pulses for all scopes. Light pen circuitry is provided for use with the RM503 and the VR12. A display-done flag circuit and an erase control circuit are included for the 611. In addition, a two-bit brightness register is provided for controlling brightness on the RM503 and the VR12.

The power dissipation characteristics of the M717 module are:

10V at 10 mA
15V at 10 mA
5V at 130 mA
30V at 20 mA

M717-2



NOTE:
PIN 7 = GND
PIN 14 = +5V ON E1, E3, E4, E7, E8
E13, E9, E10, E11, E12
E14

PIN 8 = GND
PIN 16 = +5V ON E2, E5, E6
JUMPER NORMALLY OUT

REFERENCE DESIGNATION	DESCRIPTION	PART NO
	PARTS LIST	A-PL-M717-0-0
C1-C14, C21, C24	CAP. .01MFD 100V 20% DISC	1001610
R11	RES. 51K 1/4W 5%	1304839
R2	RES. 15K 1/4W 5%	1300496
C15,	CAP. 2200MMF 250V 10%	1000055
C17	CAP. 510 MMF 15V 5%	1002476
C19, C16	CAP. .022MFD 100V 10%	1002323
C22, C18	CAP. .005MFD 100V 20%	1001765
D3, D8, D10-D13, D5, D7	DIODE D664	1100114
D9, D14, D15	DIODE D670	1102162
C20	CAP. 150 PF 100V 5%	1000019
R11	RES. 100K POT 76PR 3/4W 10%	1309143-14
R3, R13-R18, R19, R22, R23, R30	RES. 3K 1/4W 5% CC	1300432
R8, R28	RES. 330 1/4W 5% CC	1300295
R9, R21, R29	RES. 750 1/4W 5% CC	1301401
R20	RES. 1.5K 1/4W 5% CC	1300391
R25	RES. 4.7K 1/4W 5% CC	1300447
R26	RES. 47K 1/4W 10% CC	1300520
R27, R10, R1	RES. 10K 1/4W 5% CC	1300479
Q1	TRANSISTOR DEC3009B	1503100
Q2, Q3, Q4	TRANSISTOR DEC6534C	1503409-02
E1, E4, E9, E13	INTEGRATED CKT. DEC7400	1905575
E3, E8, E12	INTEGRATED CKT. DEC7410	1905576
E10, E7, E14	INTEGRATED CKT. DEC7474	1905547
E11	INTEGRATED CKT. DEC7440	1905579
E2, E5, E6	INTEGRATED CKT. AM2602	1910257
R4	RES. 5.6K 1/4W 5%	1301874

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	IN3606		
D670	IN3653		
DEC3009B	2N3009		
DEC6534B	MPS6534		

REVISIONS	REV	CHG NO	CHK
	B	00001	
	C	00002	

		DATE
DRN	M. Waller	3-12-69
CHK'D	[illegible]	3/12/69
ENGR	[illegible]	6/3/69
PROD		DATE

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: DISPLAY CONTROL VP09
M717

SIZE	CODE	NUMBER	REV
C	CS	M717-0-1	C

PRINTED CIRCUIT REV.

DEC FORM NO. DRC 102

DIST, 324, 434, 43

4 PINK

15-0157
M717
E1
C18
E3
C19
D3
E5
E7
E9
E11
R13
R14
R15
R16
R17
R18
C1
C3
C5
C7
C9
C11
D2
R2
D4
R10
C17
D5
D1
R1
E2
E4
E6
D6
R11
C20
E8
R3
E10
E12
E13
C2
C4
C6
C8
C10
C12
C13
C14
C15
Q3
Q4
Q1
Q2
R8
R9
C24
D8
R19
D7
R20
D15
D14
R23
R22
R21
D9
D10
D11
D12
R25
R26
R27
D13
R29
C21
R28
C22
C23
R12
D16

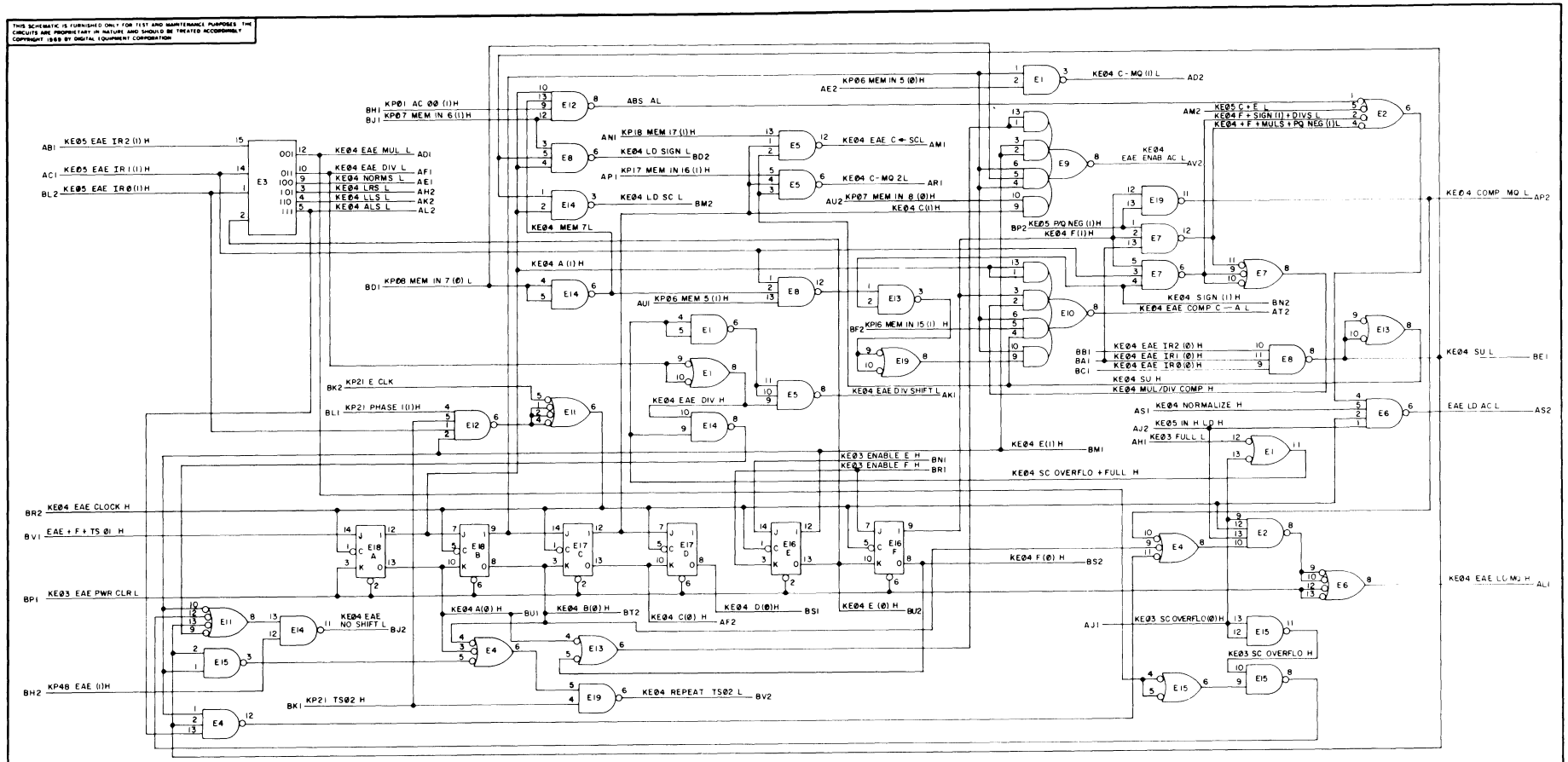
M770
EAE Control

The M770 module contains a 6-bit timing generator and EAE control logic. One of these modules is used in the PDP-15 central processor equipped with the EAE option (refer to Engineering Drawing D-BS-KE15-0-4).

The following are the input, output, and power characteristics of the M770.

INPUTS AND OUTPUTS: M770 EAE control module inputs and outputs are standard TTL levels.

POWER: The power dissipation of the M770 module is 5V at 500 mA (maximum).



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD, 100V, 20%
E1, E13, E14, E15, E19 ARE DEC74H00
E2, E12 ARE DEC74H20
E3 IS DEC9301
E4, E5, E7, E8 ARE DEC74H10
E9, E10 ARE DEC74H53
E6, E11 ARE DEC74H40
E16 THRU E18 ARE DEC7473

PIN 11 ON DEC7473 = GND
PIN 4 ON DEC7473 = +5V

PIN 14 ON EACH IC EXCEPT DEC7473 AND DEC9301 = +5V
PIN 7 ON EACH IC EXCEPT DEC7473 AND DEC9301 = GND

PIN 16 ON DEC9301 = +5V
PIN 8 ON DEC9301 = GND

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: EAE CONTROL M770

SIZE D | CODE CS | NUMBER M770-0-1 | REV A

PRINTED CIRCUIT REV | B

M770-2

M771
Internal IOT Decoder

The M771 module contains combinational logic circuits to decode bits 6 through 13 of the Input/Output Transfer (IOT) instructions of the PDP-15.

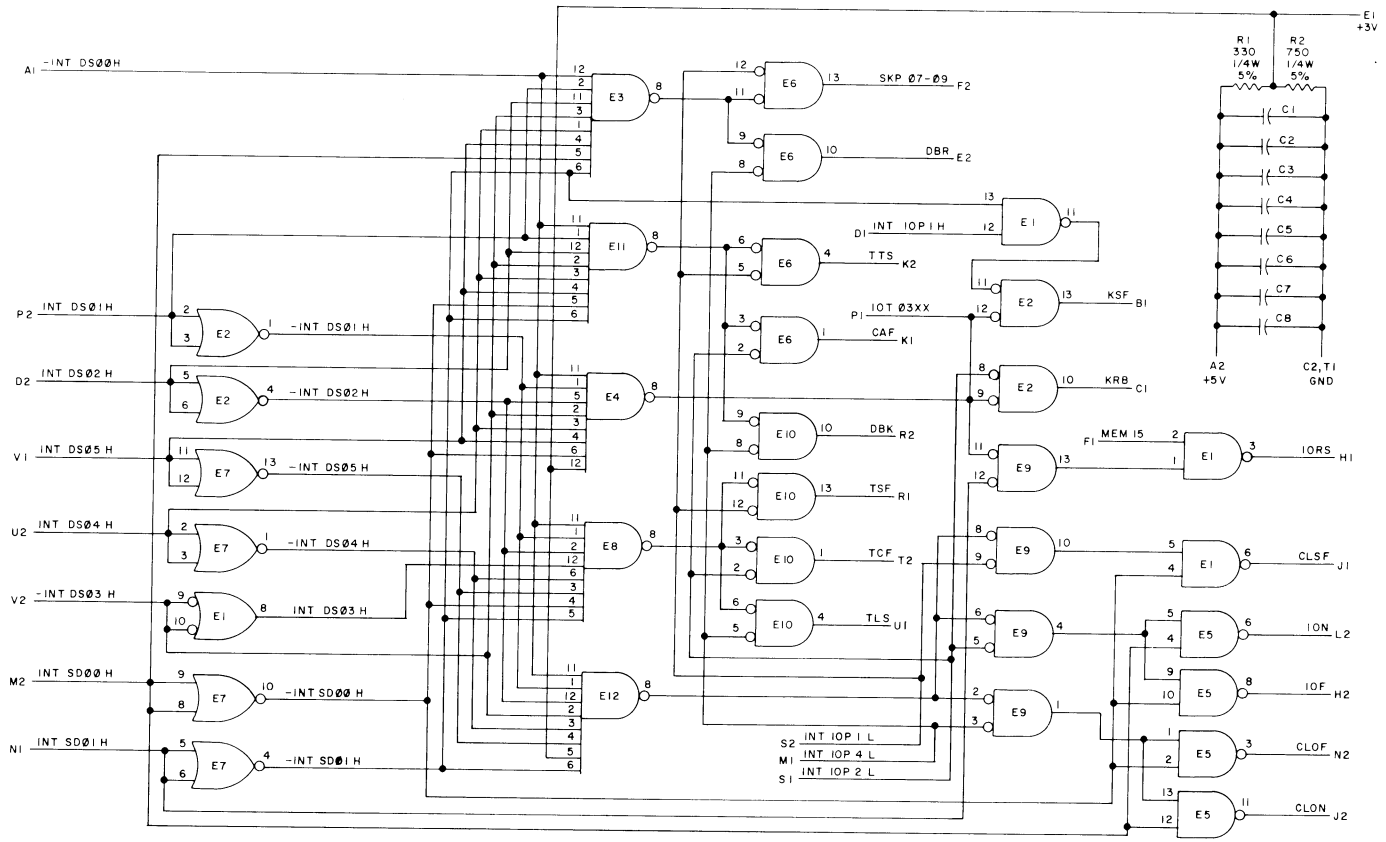
The following are the input, output, and power characteristics of the M771 module.

INPUTS: The table below lists all input connections and the TTL unit loading they present.

Name	Pin	Loading
NOT INT DS00	A1	5
INT DS01	P2	4
INT DS02	D2	4
INT DS03	V2	6
INT DS04	U2	5
INT DS05	V1	5
INT SD00	M2	5
INT SD01	N1	4
INT IOP1	S2	4
INT IOP2	S1	4
INT IOP4	M1	4
INT IOP1	D1	1
MEM	F1	1

OUTPUTS: Each decoder output (except IOT 03XX pin P1) is capable of driving 10 unit loads. Pin P1 is capable of driving 7 unit loads.

POWER: The power dissipation of the M771 module is 5V at 74 mA.



UNLESS OTHERWISE INDICATED:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E5 ARE DEC7400N
E2, E6, E7, E9, E10 ARE DEC7402N
E3, E4, E8, E11, E12 ARE DEC7430N
CAPACITORS ARE .01MFD, 100V, 20%

REVISIONS		
CHK	CHG NO.	REV.
	00001	A

DRN	Jo Keller	DATE 5-9-69
CHK'D	D Hastie	DATE 5/16/69
ENG	Y Gold	DATE
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: INTERNAL IOT DECODER M771

SIZE	CODE	NUMBER	REV
C	CS	M771-0-1	A

PRINTED CIRCUIT REV. A

M771-2

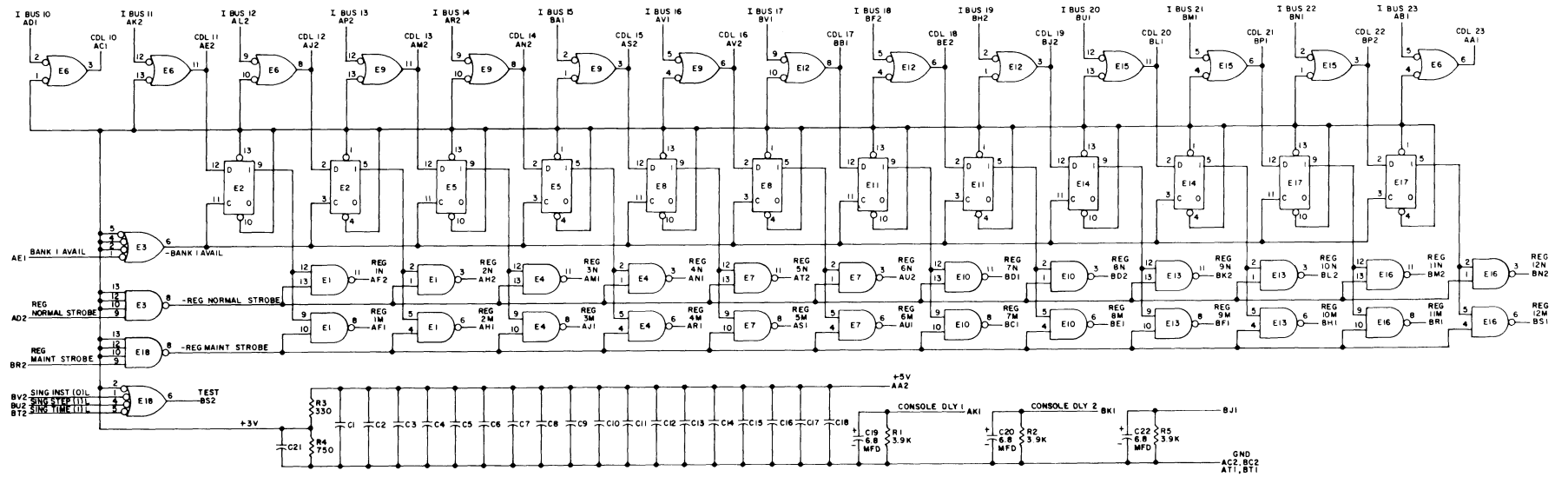
M772
Console Control No. 1

The M772 module contains 12 storage flip-flops and output gating circuits for generating 24 register strobes in response to a 12-position rotary switch and a slide switch. The module is used in the console of the PDP-15 to provide the strobes required for displaying selected data (refer to Engineering Drawing D-BS-KP15-0-44).

The following are the input, output, and power characteristics of the M772 module.

INPUTS AND OUTPUTS: M772 inputs and outputs are standard TTL levels.

POWER: Power dissipated in the M772 module is 5V at 440 mA (maximum).



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD
RESISTORS ARE 1/4W; 5%
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1,E4,E6,E7,E9,E10,E12,E13,E15,E16 ARE DEC7400N
E2,E5,E8,E11,E14,E17 ARE DEC7474N
E3,E18 ARE 7440N

REVISIONS					
CHK CHG NO	REV				
		DRN	DATE	TRANSISTOR & DIODE CONVERSION CHART	
		CHK'D	DATE	DEC / EIA	DEC / EIA
		ENGR	DATE		
		PROG	DATE		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: CONSOLE CONTROL M772

SIZE	CODE	NUMBER	REV
D	CS	M772-0-1	

PRINTED CIRCUIT REV: A

M772-2

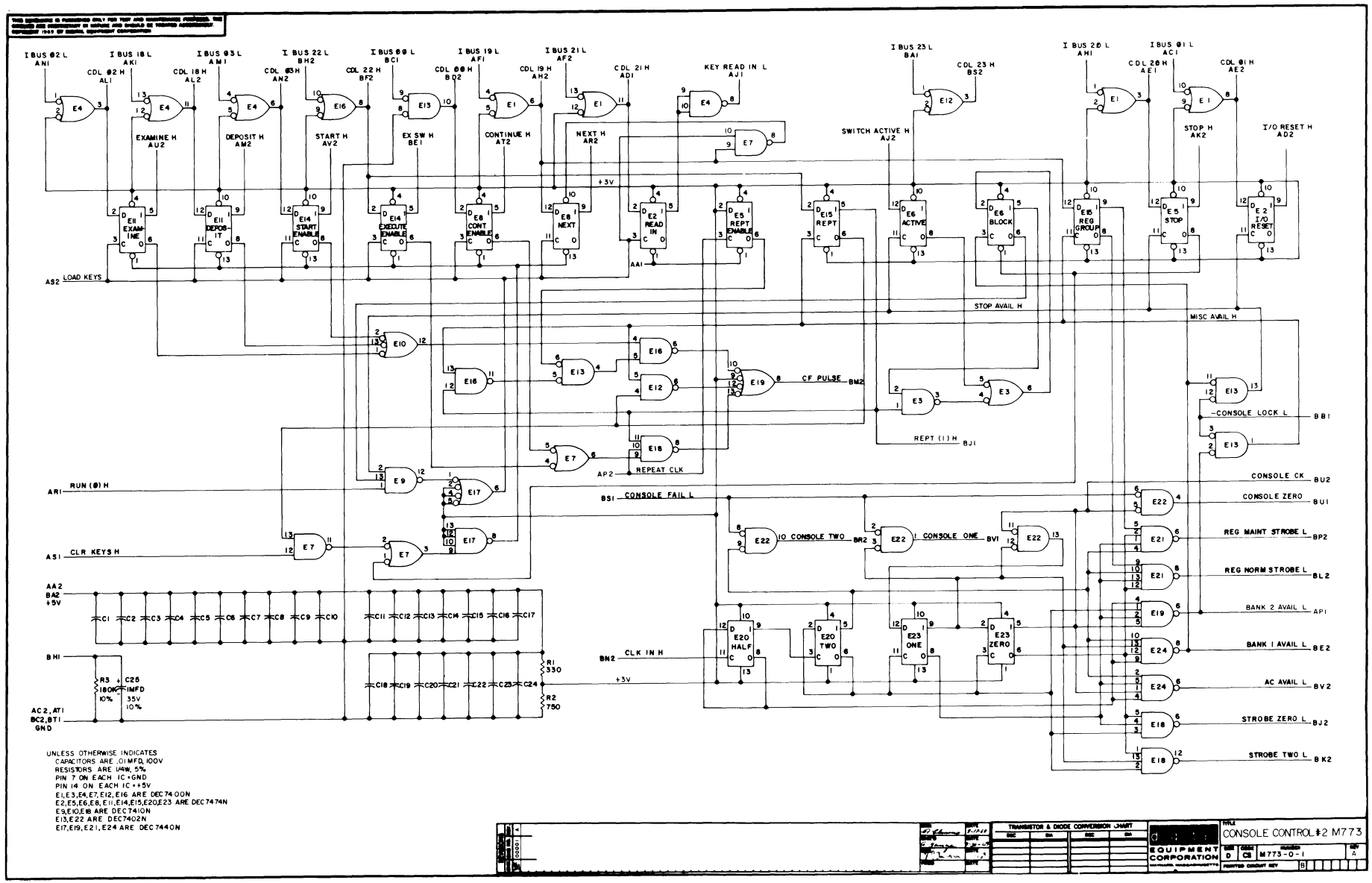
M773
Console Control No. 2

The M773 module decodes the console switch and key signals. A 6-count register generates timing pulses that strobe the address, data switches, and key functions such as STOP, START, CONTINUE, EXAMINE, and DEPOSIT) to the I/O processor. The M773 module also contains logic circuits for controlling the repeat speed functions (refer to Engineering Drawing D-BS-KP15-0-45).

The following are the input, output, and power characteristics of the M773 module.

INPUTS AND OUTPUTS: M773 inputs and outputs are standard TTL levels.

POWER: The power dissipated in the M773 module is 5V at 500 mA (maximum).


I BUS 02 L ANI
I BUS 18 L AKI
I BUS 03 L AMI
I BUS 22 L BH2
I BUS 00 L BCI
I BUS 19 L AFI
I BUS 21 L AF2
I BUS 23 L BAI
I BUS 20 L AHI
I BUS 01 L ACI
CDL 02 H ALI
CDL 18 H AL2
CDL 03 H AN2
CDL 22 H BF2
CDL 00 H BD2
CDL 19 H AH2
CDL 21 H AD1
CDL 23 H BS2
CDL 20 H AE1
CDL 01 H AE2
KEY READ IN L AJ1
EXAMINE H AU2
DEPOSIT H AM2
START H AV2
EX SW H BE1
CONTINUE H AT2
NEXT H AR2
SWITCH ACTIVE H AJ2
STOP H AK2
I/O RESET H AD2
+3V
AS2 LOAD KEYS
AA1
STOP AVAIL H
MISC AVAIL H
CF PULSE BM2
REPT (1) H BJ1
-CONSOLE LOCK L BB1
AP2 REPEAT CLK
CONSOLE CK BU2
BS1 CONSOLE FAIL L
CONSOLE ZERO BU1
BR2 10 CONSOLE TWO
BV1 1 CONSOLE ONE
REG MAINT STROBE L BP2
REG NORM STROBE L BL2
BANK 2 AVAIL L AP1
BANK 1 AVAIL L BE2
AC AVAIL L BV2
STROBE ZERO L BJ2
STROBE TWO L BK2
AR1 RUN (0) H
AS1 CLR KEYS H
AA2
BA2
+5V
BH1
AC2, AT1
BC2, BT1
GND
BN2 CLK IN H
R1 330
R2 750
R3 180K 10%
C26 FMFD 35V 10%
UNLESS OTHERWISE INDICATED
CAPACITORS ARE .01 MFD, 100V
RESISTORS ARE 1/4W, 5%
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E3, E4, E7, E12, E16 ARE DEC 7400N
E2, E5, E6, E8, E11, E14, E15, E20, E23 ARE DEC 7474N
E9, E10, E18 ARE DEC 7410N
E13, E22 ARE DEC 7402N
E17, E19, E21, E24 ARE DEC 7440N
TRANSISTOR & DIODE CONVERSION CHART
EQUIPMENT CORPORATION
TITLE CONSOLE CONTROL #2 M773
SIZE D CODE CS NUMBER M773-0-1 REV A
PRINTED CIRCUIT REV B

M775
Time State Generator

The M775 module contains a 5-18 MHz variable clock and a four-stage ring counter. This module is used in the central processor of the PDP-15 to divide each of the three time states of each cycle into four phases. The clock frequency is adjusted to obtain a period equivalent to one time phase.

The following are the input, output, and power characteristics of the M775 module.

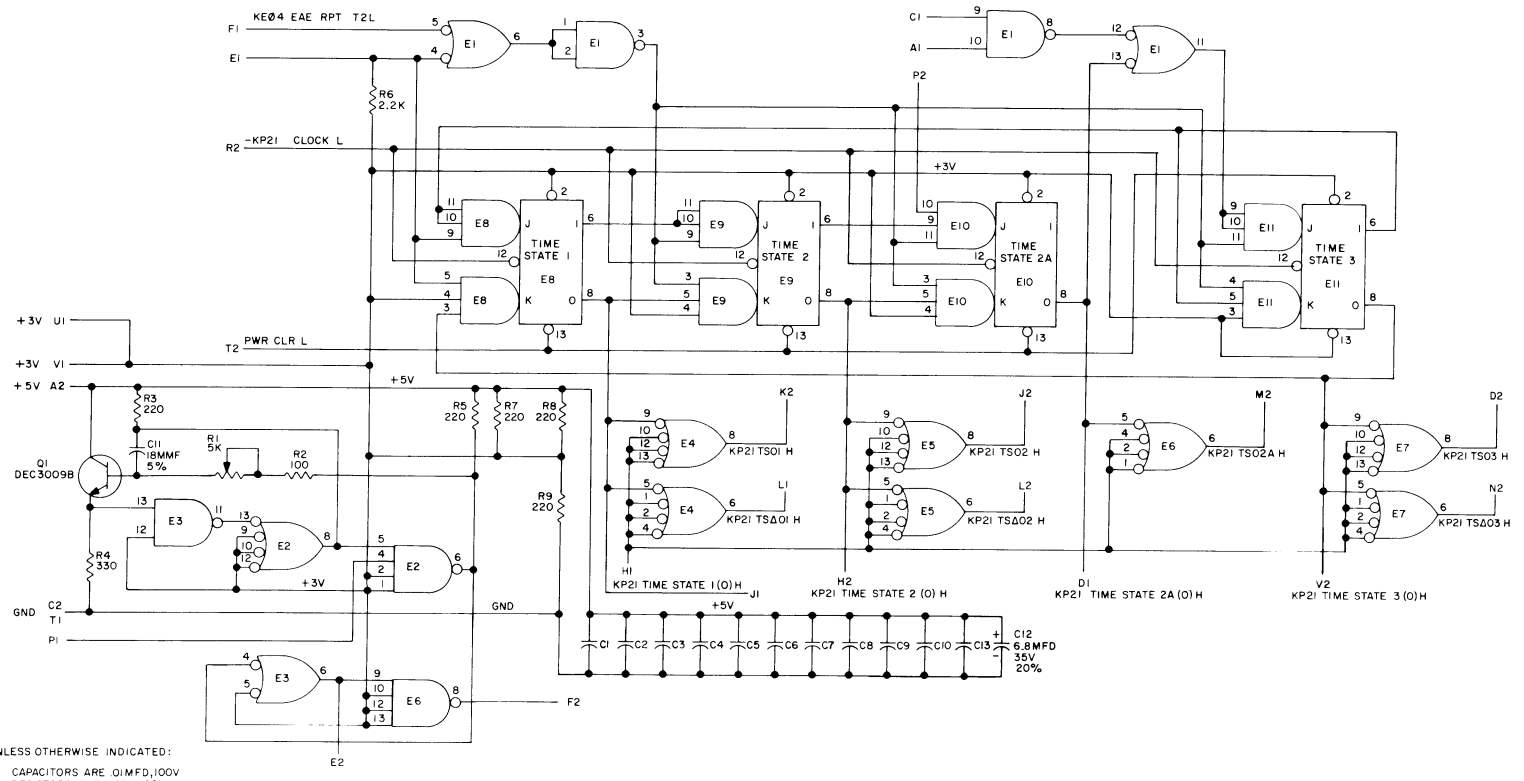
INPUTS: The table below lists all input connections and the TTL loading they present.

Name	Pin	Loading
REPEAT TS2	F1	1.25
SING TIME LOOP	E1	3.75
TS2	C1	1.25
ADD*TS2*E	A1	1.25
ADD*TS2*E	P2	1.25
CLOCK	R2	10
CLEAR	T2	10
STOP CLOCK	P1	1.25

OUTPUTS: The table below lists all output connections and their unit load-driving capabilities.

Name	Pin	Drive
TIME STATE 1	J1	9
TIME STATE 1	K2	36
TIME STATE 1	L1	36
TIME STATE 2	H2	9
TIME STATE 2	J2	36
TIME STATE 2	L2	36
TIME STATE 2A	D1	8
TIME STATE 2A	M2	36
TIME STATE 3	V2	9
TIME STATE 3	D2	36
TIME STATE 3	N2	36
HS CLOCK	E2	11
HS CLOCK	F2	36

POWER: Power dissipated in the M775 module is 5V at 325 mA (maximum).



UNLESS OTHERWISE INDICATED:

CAPACITORS ARE .01MFD,100V
RESISTORS ARE 1/4W, 5%
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

E1 IS DEC7400N
E3 IS DEC74H00N
E2,E4,E5-E7 ARE DEC74H40N
E8,E9,E10,E11, ARE DEC74H72N

DRN	BUTLER	DATE 8/4/69
CHK'D	[illegible]	DATE 8/8/69
ENG	[illegible]	DATE 11/4/69
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3009B	2N3009		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE TIME STATE GENERATOR M775

SIZE	CODE	NUMBER	REV
C	CS	M775-0-1	

PRINTED CIRCUIT REV

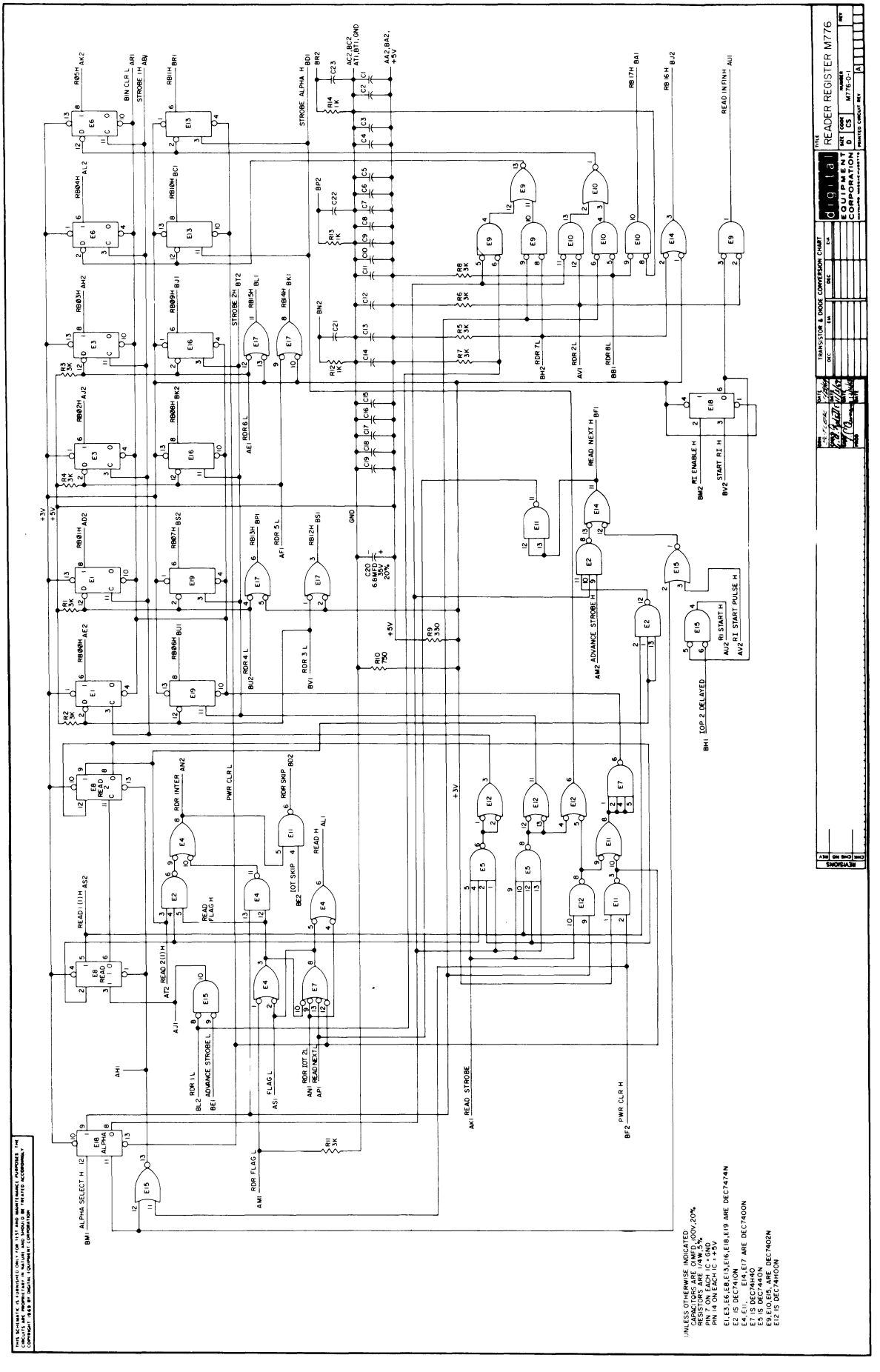
M776
Reader Register

The M776 module contains two 6-bit buffer registers, output gates, and control logic. The module is used in Reader Control PC15 to serve as the interface between Paper Tape Reader PC05 and the PDP-15, transferring 8-bit or 18-bit data words. For the 18-bit data transfers, three characters from the reader are automatically assembled by the module.

The following are the input, output, and power characteristics of the M776 module.

INPUTS AND OUTPUTS: M776 Reader Register inputs and outputs are standard TTL levels.

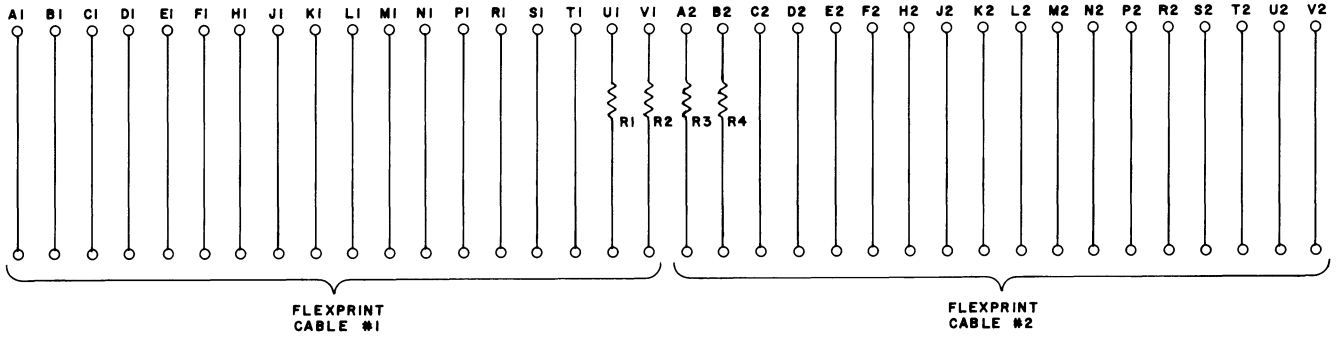
POWER: Power dissipated in the M776 module is 5V at 470 mA.


TITLE
READER REGISTER M776
digital
EQUIPMENT
CORPORATION
TRANSISTOR & DIODE CONVERSION CHART
DEC
SIZE
D
DWG
CS
NUMBER
M776-0-1
REV
PRINTED CIRCUIT REV
REVISIONS
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 0MFD, 100V, 20%
RESISTORS ARE 1/4W, 5%
PIN 14 ON EACH IC = +5V
PIN 7 ON EACH IC = GND
E1, E3, E6, E8, E13, E16, E18, E19 ARE DEC7474N
E2 IS DEC7410N
E4, E11, E14, E17 ARE DEC7400N
E7 IS DEC7440
E9, E10 ARE DEC7440N
E12, E15 ARE DEC7402N
E5 IS DEC7440
E20 IS DEC7450N
ALPHA SELECT H
STROBE ALPHA H
STROBE 1H
STROBE 2H
BIN CLR L
READ INFINH
READ NEXT H
ADVANCE STROBE H
RDR INTER
RDR SKIP
RDR IOT 2L
READ STROBE
PWR CLR H
PWR CLR L
IOP 2 DELAYED
RT ENABLE H
RT START PULSE H
RDR 1L
RDR 2L
RDR 3 L
RDR 4 L
RDR 5 L
RDR 6 L
RDR 7L
RDR 8L
READ FLAG H
FLAG L
RDR FLAG L
IOT SKIP
READ H
+5V
+3V
GND

M901
Flexprint Cable Connector

The M901 module allows 36 lines to be used as signals and/or grounds. The 100Ω resistors connected in series with the module pins A2, B2, U1, and V1 are provided to afford some measure of protection if these pins are inadvertently connected to a source of supply voltage.

The recommended current per line is 100 mA (maximum).



R1-R4	RES. 10 1/4W 10% CC	1300170
	PARTS LIST	A-PL-M901-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

REVISIONS	CHK	CHG NO	REV
		00001	C

DRN.	M. Waller	DATE 8-19-68
CHK'D	M. Fuller	DATE 8-19-68
ENG.	[illegible]	DATE 11/5/68
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: FLEXPRINT CABLE CONNECTOR M901

SIZE	CODE	NUMBER	REV.
B	CS	M901-0-1	C

PRINTED CIRCUIT REV. B C

M902
Terminator Card

The M902 module contains 18 terminating resistors connected to ground. Each resistor value is 100Ω, 1/4W at 5%. This single-height board replaces the output cable of the last memory used on the PDP-15 memory bus. Two of these boards are required for each PDP-15 system.

Ground pins are:

C2; F2; J2; L2; N2; R2; U2;
A1; C1; F1; K1; N1; R1; and T1.

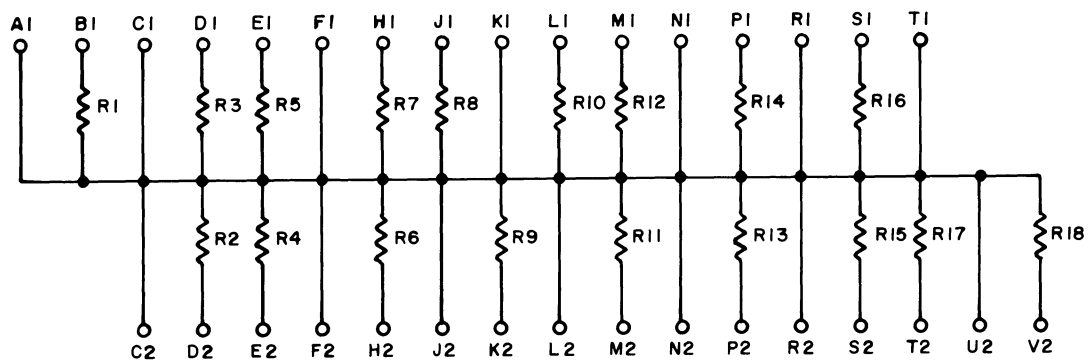
The following are the input, output, and power characteristics of the M902 module.

INPUTS: There are 18 inputs, one to each resistor.

OUTPUTS: There are no outputs.

POWER: The power dissipation of the M902 is 1.125W (maximum).

SIZE	CODE	NUMBER	REV.
B	CS	M902-0-1	B



M902-2

R1 – R18	RES. 100 1/4W 5% CC	1300229
	PARTS LIST	A-PL-M902-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

REVISIONS			
CHK	CHG NO.	00001	
REV.		B	

DRN.	M. Waller	DATE 6-18-68
CHK'D	W. F. Fisher	DATE 6/18/68
ENG.	[illegible]	DATE 7/10/68
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: RESISTOR TERMINATOR M902

SIZE	CODE	NUMBER	REV.
B	CS	M902-0-1	B

PRINTED CIRCUIT REV. A

DEC FORM NO.
DRB 102

P/NK | DIST. 1434 524 435 1 2 4

M904
Coaxial Cable Connector

The M904 connector is a single-size, double-sided board.

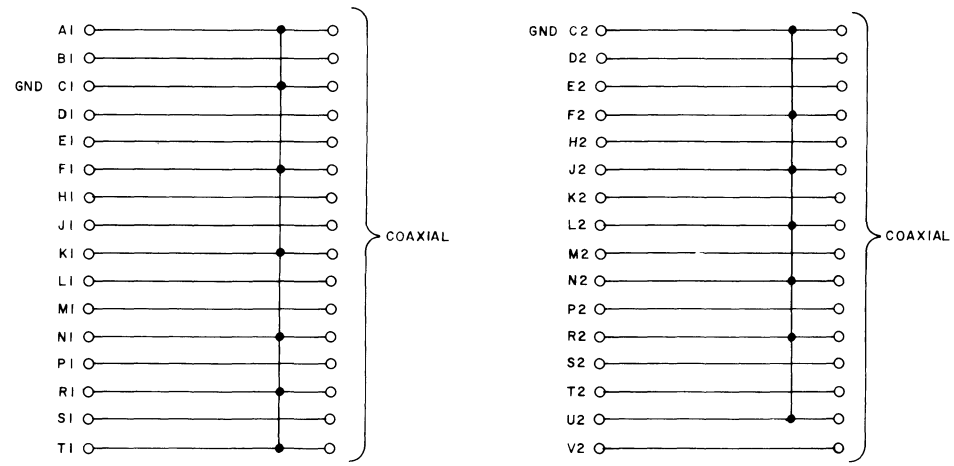
This connector provides high-density cable connections using coaxial cable. Provisions are made for connection of two 9-conductor coaxial cables to the M904 connector. Eighteen signal leads and grounds are used.

The signal leads are:

B1; D1; E1; H1; J1; L1; M1; P1; S1
D2; E2; H2; K2; M2; P2; S2; T2; and V2.

The common (ground) leads are:

A1; C1; F1; K1; N1; R1; T1;
C2; F2; J2; L2; N2; R2; and U2



PARTS LIST IS A-PL-M904-0-0

REVISIONS	CHK	CHG NO	REV
		00001	A
		00003	C

DRN. M. Keller	DATE 7-12-68	
CHK'D.	DATE 7-22-68	
ENG.	DATE 7/26/68	
MOD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE CONNECTOR (COAXIAL) M904

SIZE	CODE	NUMBER	REV.
B	CS	M904-0-1	C

PRINTED CIRCUIT REV. B

M909
Terminator Card

This is a standard single-height M-series board with 18 terminating resistors connected to ground. All the resistors are 68Ω, 1/4W at 5%.

GND Pins are: C2; F2; J2; L2; N2; R2; U2; A1; C1; F1; K1; N1; R1; and T1.

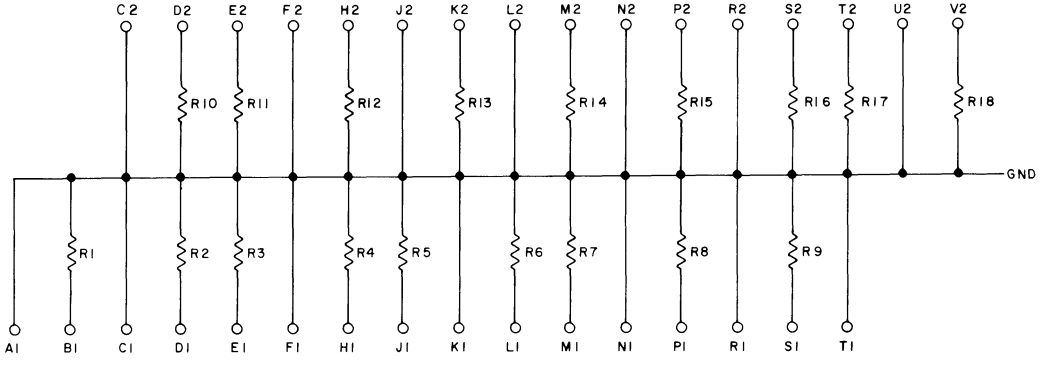
The following are the input, output, and power characteristics of the M909 module.

INPUTS: There are 18 inputs; one to each resistor.

OUTPUTS: There are no outputs.

POWER: The power dissipation of the M909 is 1.8W (maximum).

These boards replace the output cable of the last peripheral on the positive PDP-15 I/O bus.



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 68 1/4W 5%

REVISIONS			
CHK	CHG NO	REV	

DRN		DATE 4-7-69
CHK'D	G. Yanega	DATE 4-8-69
ENG.	R. Eka-Shand	DATE 5-5-69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: TERMINATOR CARD M909

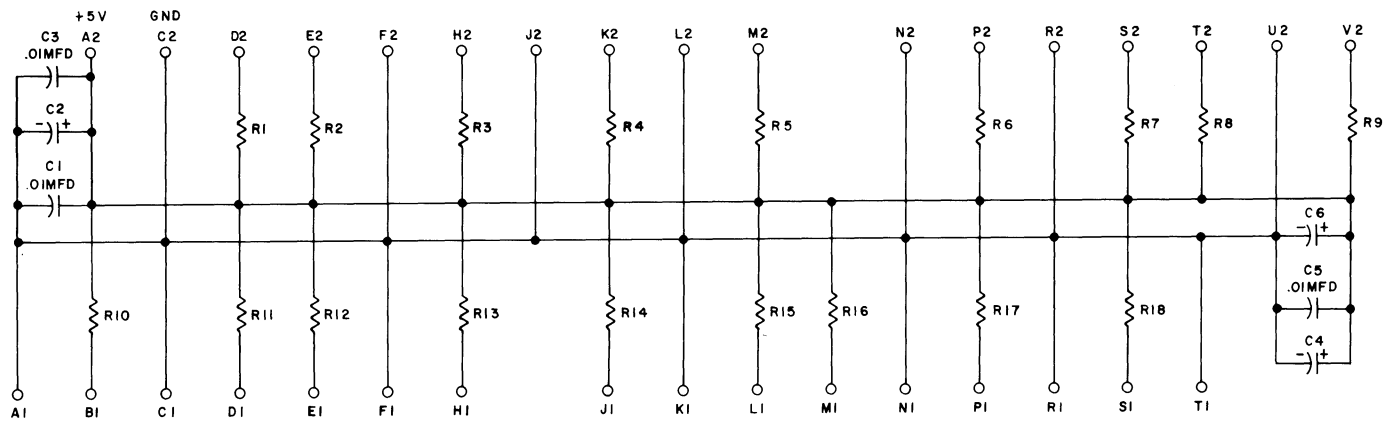
SIZE	CODE	NUMBER	REV.
B	CS	M909-0-1	

PRINTED CIRCUIT REV. A

M910
CP Terminator Card

The M910 module contains eighteen 68Ω terminating resistors. Each resistor is connected to a common +5V source. The resistors are used as load resistors to terminate the I/O bus lines in the PDP-15.

Power dissipation is 1.8W (minimum) and 7.2W (maximum).



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 6.8 MFD
RESISTORS ARE 68 1/2W, 5%

REVISIONS					
CHK	CHG NO.	REV.			
			DRN.		DATE 8-26-69
			CHK'D.		DATE 9-5-69
			ENG.	R. Elia-Shaw	DATE 9-10-69
			PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE CP TERMINATOR CARD M910

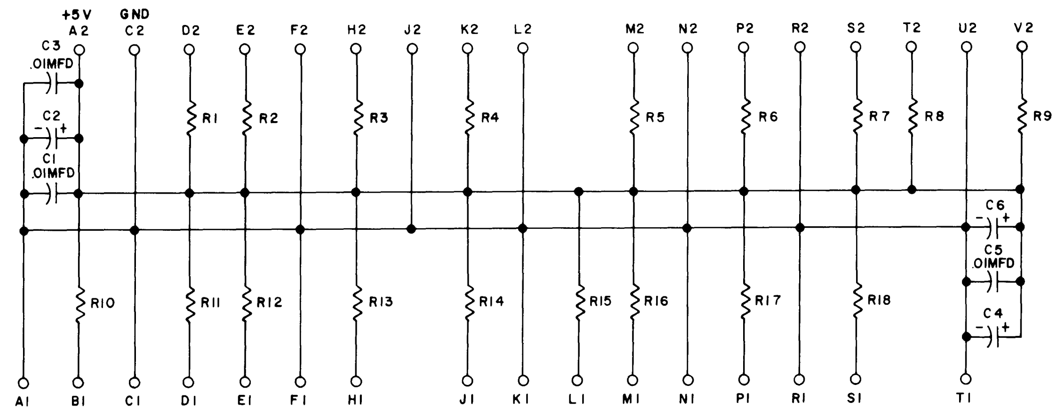
SIZE	CODE	NUMBER	REV.
B	CS	M910-0-1	

PRINTED CIRCUIT REV. A

M911
Memory Bus CP Terminator Card

The M911 module contains eighteen 100Ω terminating resistors. Each resistor is connected to a common +5V source. The resistors are used as load resistors to terminate all the memory bus lines at the CP end in the PDP-15.

Power dissipation is 1.25W (minimum) and 5.0W (maximum).



UNLESS OTHERWISE INDICATED
CAPACITORS ARE 6.8MFD
RESISTORS ARE 100 1/2W 5%

REVISIONS		
CHK	CHG NO	REV

DRN.	DATE 2-27-69
CHK'D	DATE
ENG.	DATE
PROD.	DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE MEMORY BUS CP TERMINATOR M911

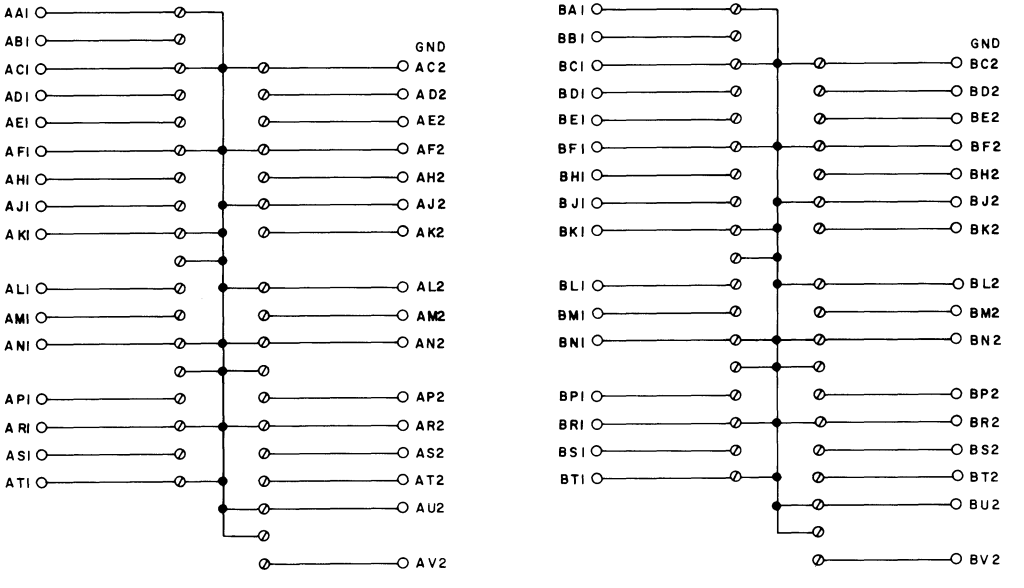
SIZE	CODE	NUMBER	REV
B	CS	M911-0-1	

PRINTED CIRCUIT REV. A

M912
I/O Bus Connector

The M912 module is a double-height and double-sided FLIP CHIP connector card used in fabricating I/O bus interconnect cables for peripheral devices.

Four of these cards are required to fabricate a BC09B cable, and two cards are needed to fabricate a BC09C cable.



Ø SPLIT LUGS

REVISIONS	REV	CHG NO	CHK

DRN		DATE 8-26-69
CHK'D		DATE 9-12-69
ENG	R. E. Shand	DATE 9-30-69
PROD		DATE 10/1/69

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: 10 BUS CONNECTOR CARD M912

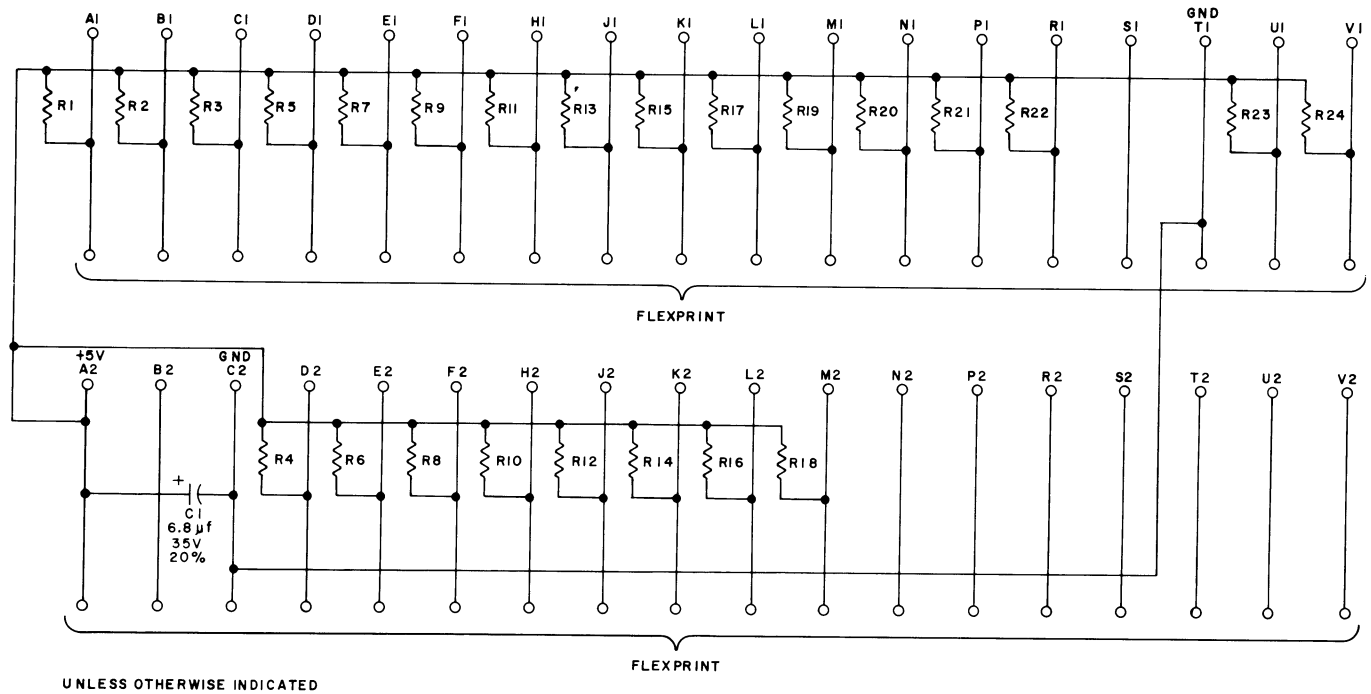
SIZE	CODE	NUMBER	REV.
B	CS	M912-0-1	

PRINTED CIRCUIT REV. A

M915
Console Cable Connector

The M915 module is used in conjunction with the M901 module and a Flexprint cable to fabricate the I bus interconnect cable. The M915 module contains twenty-four 750Ω terminating resistors and twenty-four 0.01 μF bypass capacitors. Each resistor is connected to a common +5V source. The resistors are used as load resistors to terminate the I bus lines in the PDP-15 console, and the capacitors bypass the I bus lines to ground.

Power dissipation of the M915 module is 5V at 330 mA.



UNLESS OTHERWISE INDICATED
RESISTORS ARE 390, 1/4W, 5%

REVISIONS	CHK	CHG NO	REV
		00001	B

DRN.		DATE 3-18-69
CHK'D		DATE 3/19/69
ENGR		DATE 4/23/69
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: CONSOLE CABLE CONNECTOR CARD M915

SIZE	CODE	NUMBER	REV.
B	CS	M915-0-1	B

PRINTED CIRCUIT REV. B

M1701
Data Selector

The M1701 Data Selector contains two DEC74153 Dual 4-Line-to-1-Line Data Selector/Multiplexer integrated circuits. These modules are used as input multiplexers in the ALU section of the FP15 Floating-Point Processor. Complete block schematics of these input multiplexers are shown on FP15 drawings D-BS-FP15-0-19 through -28.

For each section of each IC, one of four data inputs is selected by combinations of address input signals A and B. The selected data input is strobed to the output when the S (strobe) input goes low. Refer to the following truth table.

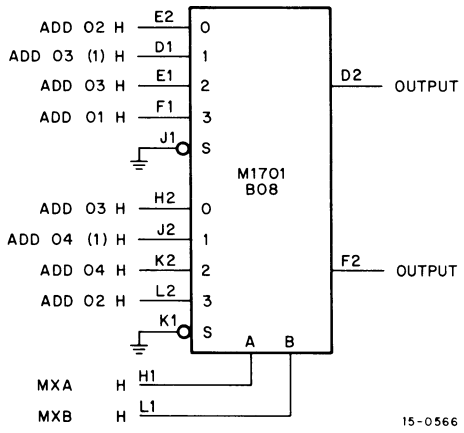
Address Inputs		Data Inputs				Strobe	Output
A	B	0	1	2	3	S	
x	x	x	x	x	x	1	0
0	0	0	x	x	x	0	0
0	0	1	x	x	x	0	1
1	0	x	0	x	x	0	0
1	0	x	1	x	x	0	1
0	1	x	x	0	x	0	0
0	1	x	x	1	x	0	1
1	1	x	x	x	0	0	0
1	1	x	x	x	1	0	1

x indicates irrevelancy. Address inputs A and B are common to both sections of each IC.

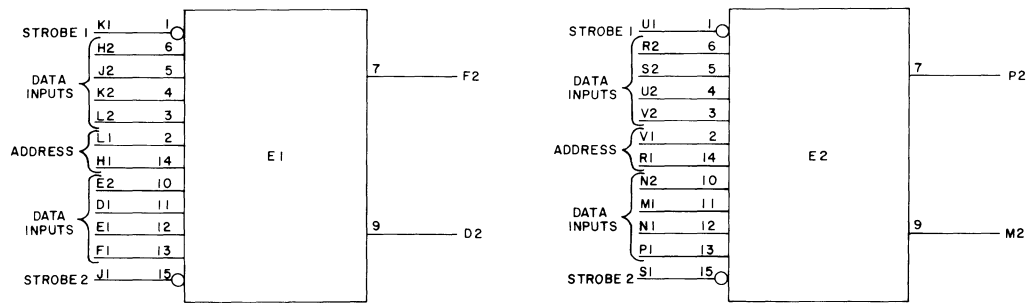
INPUTS: Each input represents 1 unit load.

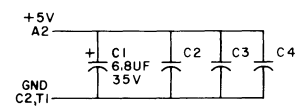
OUTPUTS: Each output is capable of driving 10 unit loads.

POWER: Typical power dissipation is 170 mW for each IC on the module.



SIZE	CODE	NUMBER	REV
B	CS	M1710-0-1	





UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01UF, 100V, 20%
IC'S ARE DEC74153

REVISIONS	REV	CHG NO	CHK

DRN	S. Cooper	DATE 1-15-71
CHK'D		DATE 1-19-71
ENG	Sam Holmes	DATE 1-19-71
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DATA SELECTOR M1701

SIZE	CODE	NUMBER	REV
B	CS	M1701-0-1	

PRINTED CIRCUIT REV D

DEC FORM NO. DRB 102

DIST 324,430,435 2

4 Pak

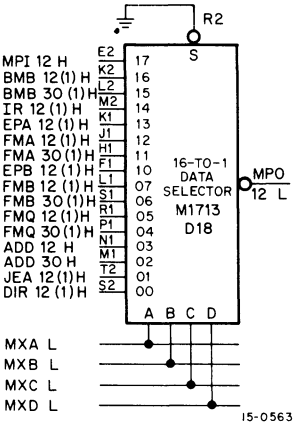
M1713
16-to-1 Data Selector

The M1713 16-To-1 Data Selector contains a single DEC74150 integrated circuit. It is used in the output multiplexer section of the FP15 Floating-Point Processor where up to 16 major register outputs are selected for transfer to the common MPO bus. The block schematic of the output multiplexer is shown on D-BS-FP15-0-03 of the FP15 drawings.

Data inputs are selected by combinations of data select signals MXA, MXB, MXC, and MXD, which are generated by the multiplexer control logic shown on D-BS-FP15-0-05. The strobe inputs are wired to ground so that each IC is always enabled. A typical truth table for the 16-To-1 Data Selector is shown in the following table.

Data Select Inputs				Data Input* Selected
MXD	MXC	MXB	MXA	
0	0	0	0	DIR12
0	0	0	1	JEA12
0	0	1	0	ADD30
0	0	1	1	ADD12
0	1	0	0	FMQ30
0	1	0	0	FMQ12
0	1	1	0	FMB30
0	1	1	1	FMB12
1	0	0	0	EPB12
1	0	0	1	FMA30
1	0	1	0	FMA12
1	0	1	1	EPA12
1	1	0	0	IR12
1	1	0	1	BMB30
1	1	1	0	BMB12
1	1	1	1	MPI12

*Signal mnemonics vary as shown on D-BS-FP15-0-03. Note that the output is the complement of the selected input.

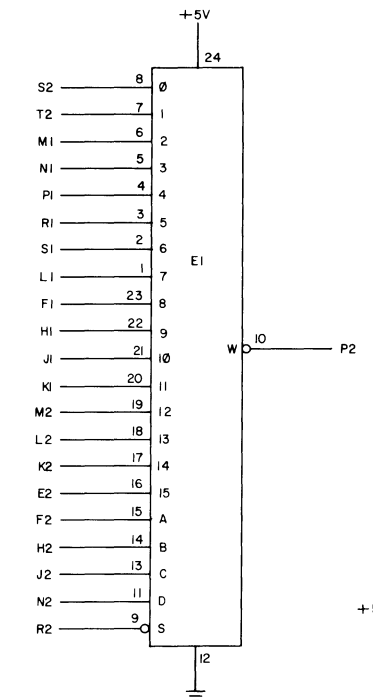


INPUTS: Each input represents 1 unit load.

OUTPUTS: The output is capable of driving up to 10 unit loads.

POWER: Typical power dissipation is 200 mw.

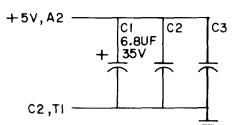
SIZE	CODE	NUMBER	REV
B	CS	M1713-0-1	



UNLESS OTHERWISE INDICATED:

CAPACITORS ARE .01 UF, 100V, 20%

IC IS A DEC74150



REVISIONS	REV	CHG NO	CHK

DRN	B. Wyatt	DATE 10-28-70
CHK'D	[illegible]	DATE [illegible]
ENG	Jim Holmes	DATE 11/23/70
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE: 16 LINE TO 1 LINE DATA SELECTOR M1713

SIZE	CODE	NUMBER	REV
B	CS	M1713-0-1	

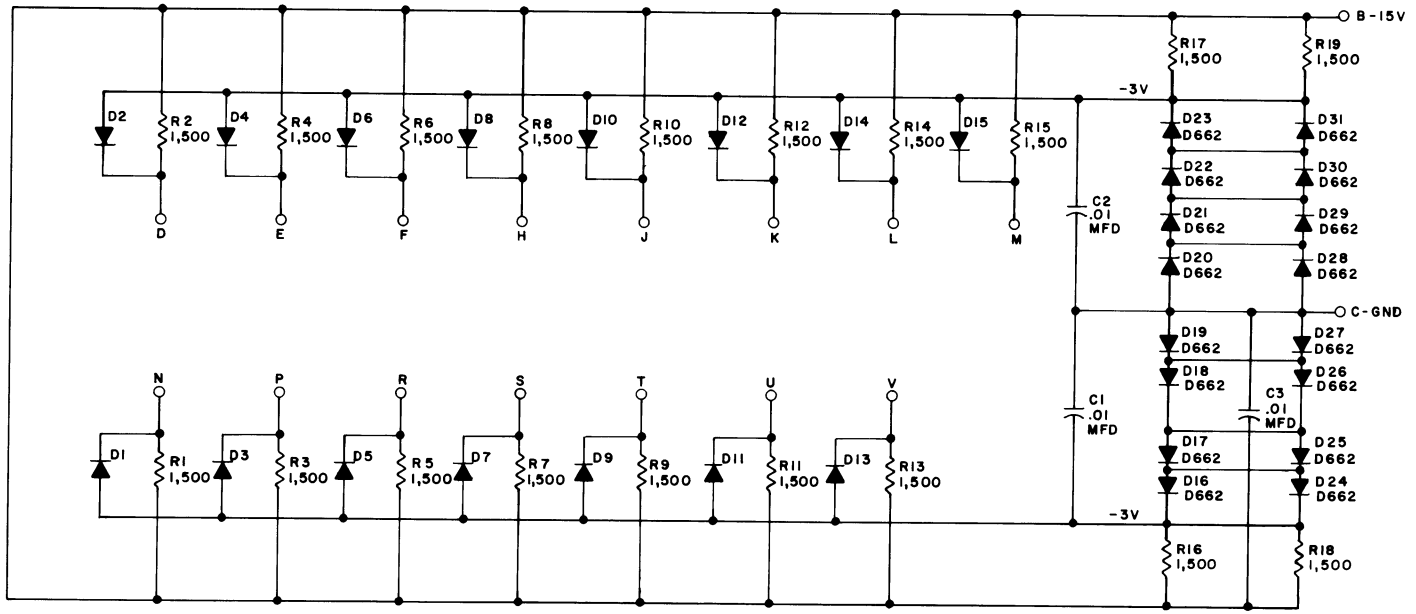
PRINTED CIRCUIT REV A

DEC FORM NO
DRB 102

W010
Clamped Loads

The W010 module contains fifteen identical 10 mA clamped loads, each consisting of a resistor and a diode. Each load resistor is connected to a common -15V source. The clamping diodes are connected to a -3V source, which is obtained by a resistor-diode voltage divider.

Power dissipation of the W010 module is 15V at 250 mA.



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4; 5%
DIODES ARE D664

REVISIONS

REV	CHG NO	CHK

DRN. M. Waller	DATE 11-15-66	
CHK'D. K. Lukermann	DATE 11/15/66	
ENG. G. Stutz	DATE 11/15/66	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

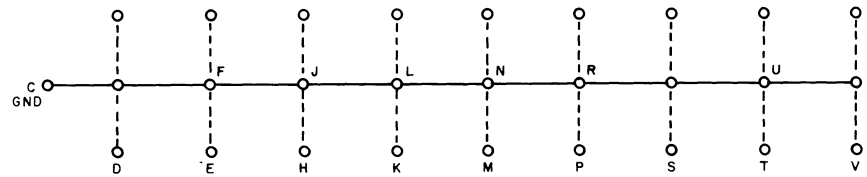
TITLE: CLAMPED LOADS W010

SIZE	CODE	NUMBER	REV.
B	CS	W010-0-1	

PRINTED CIRCUIT REV. A

W028
Cable Connector for Levels and Pulses

The W028 module provides cable connections to the FLIP CHIP mounting panel. The cable is a 19-conductor ribbon with 9 signal leads and 10 shields. The signal leads are connected to pins D, E, H, K, M, P, S, T, and V. The shields are internally connected together and to pins C, F, J, L, N, R, and U.



PARTS LIST A-PL-W028-0-0

REVISIONS			
CHK	CHG NO	REV	
	6534	A	

DRN.	M. Walker	DATE 2-14-68
CHK'D		DATE
ENG		DATE 3-20-68
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: TERMINATED BOARD W028

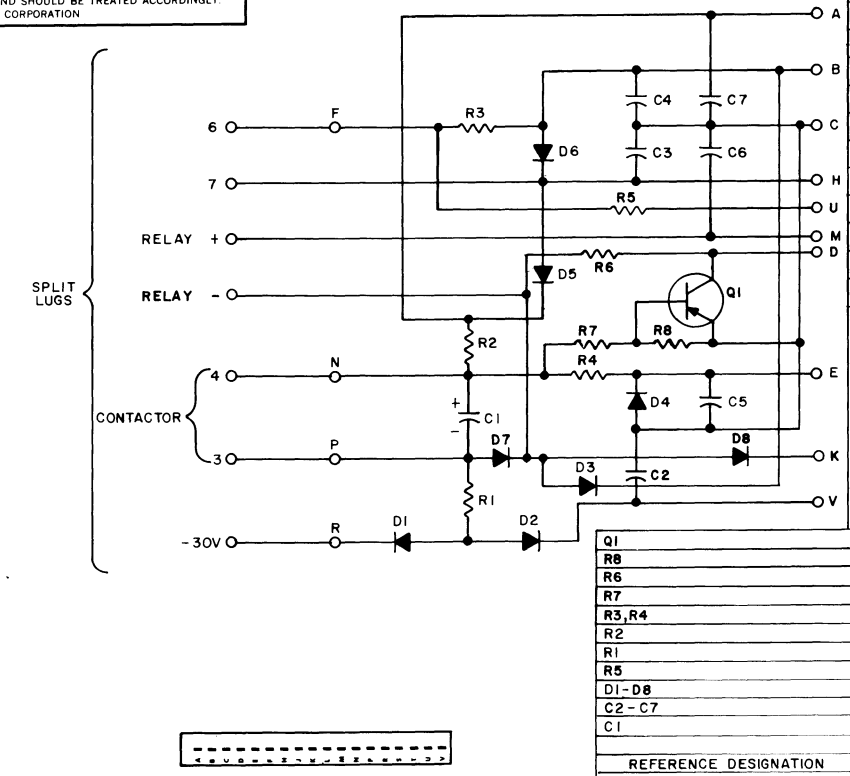
SIZE	CODE	NUMBER	REV.
B	CS	W028-0-1	A

PRINTED CIRCUIT REV. C

W076
Teletype Connector

The W076 module is a universal interface module used in controlling a Teletype from logic using positive voltages of +5V or +10V. The module is soldered to a cable that connects the Teletype to a computer. Networks contained on the module set the current through the keyboard contacts and selector drive magnet. Either -15V or -30V can be used across the commutator.

Power dissipation of the W076 is +5V at 25 mA or +10V at 25 mA; -15V at 4 mA or -30V at 51 mA.



TYPICAL PIN ASSIGNMENTS

PIN	8	8I, 8L	DC08
A	+10V	+5V	+5V
B	-15V	-15V	+5V
C	GND	GND	GND
H	LOGIC INPUT	LOGIC INPUT	—
U	—	—	LOGIC INPUT
M	READER ENABLE	READER ENABLE	READER ENABLE
D	LOGIC OUTPUT	—	—
E	—	LOGIC OUTPUT	LOGIC OUTPUT
K	—	—	-15V
V	-30V OPTIONAL	-30V OPTIONAL	-30V OPTIONAL

PARTS LIST

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
Q1	TRANSISTOR DEC6534D	1503409
R8	RES. 1.5K 1/4W 5% CC	1300391
R6	RES. 1.8K 1/2W 10% CC	1300400
R7	RES. 10K 1/4W 10% CC	1300481
R3,R4	RES. 750 1/2W 5% CC	1300354
R2	RES. 750 2W 5% CC	1301984
R1	RES. 1K 1W 10% CC	1301499
R5	RES. 120 1/2W 5% CC	1300243
D1-D8	DIODE D671	1103309
C2-C7	CAP. .01MFD 100V 20% DISC	1001610
C1	CAP. 1MFD 150V 10% FOIL	1000063
	PARTS LIST	A-PL-W076-0-0

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC6534D	MPS6534		
D671	IN3653		

REVISIONS	CHK	CHG NO.	REV.
REV. B REDR. 7010		00001	B
		00002	
		00003	C
		00004	
		00005	D

		DATE
DRN.	M. HALLER	5-18-67
CHK'D	N. PERRYMAN	5-23-67
ENG.	R. SOGGE	5-25-67
PROD.		DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: TELETYPE CONNECTOR W076

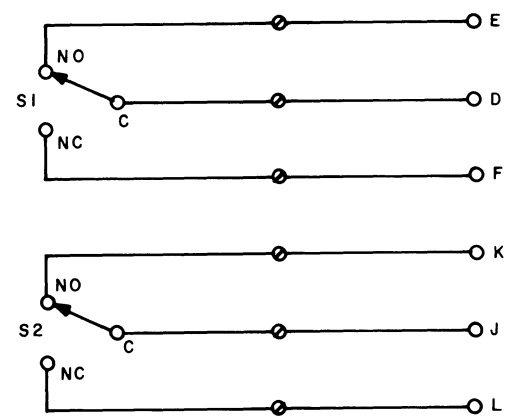
SIZE	CODE	NUMBER	REV.
B	CS	W076-0-1	D

PRINTED CIRCUIT REV. D

DEC FORM NO. DRB 102

W714
Switches

The W714 module contains two switches accessible at the back of the module. These switches are used as bank selection switches for the MM15 memory extension and the MX15A multiplexer.



UNLESS OTHERWISE INDICATED:
⊘ ARE SPLIT LUGS
SWITCHES ARE MICRO-SWITCH 6AT56-T2

REVISIONS	REV.	CHG NO.	CHK
	B	00001	
	C	00002	

DRN. M. Waller	DATE 3-27-69	
CHK'D M. Marshall	DATE 3/28/69	
ENG. R Cairns	DATE 3/27/69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: SWITCH MODULE W714

SIZE	CODE	NUMBER	REV.
B	CS	W714-0-1	C

PRINTED CIRCUIT REV. A

DEC FORM NO.
DRB 102

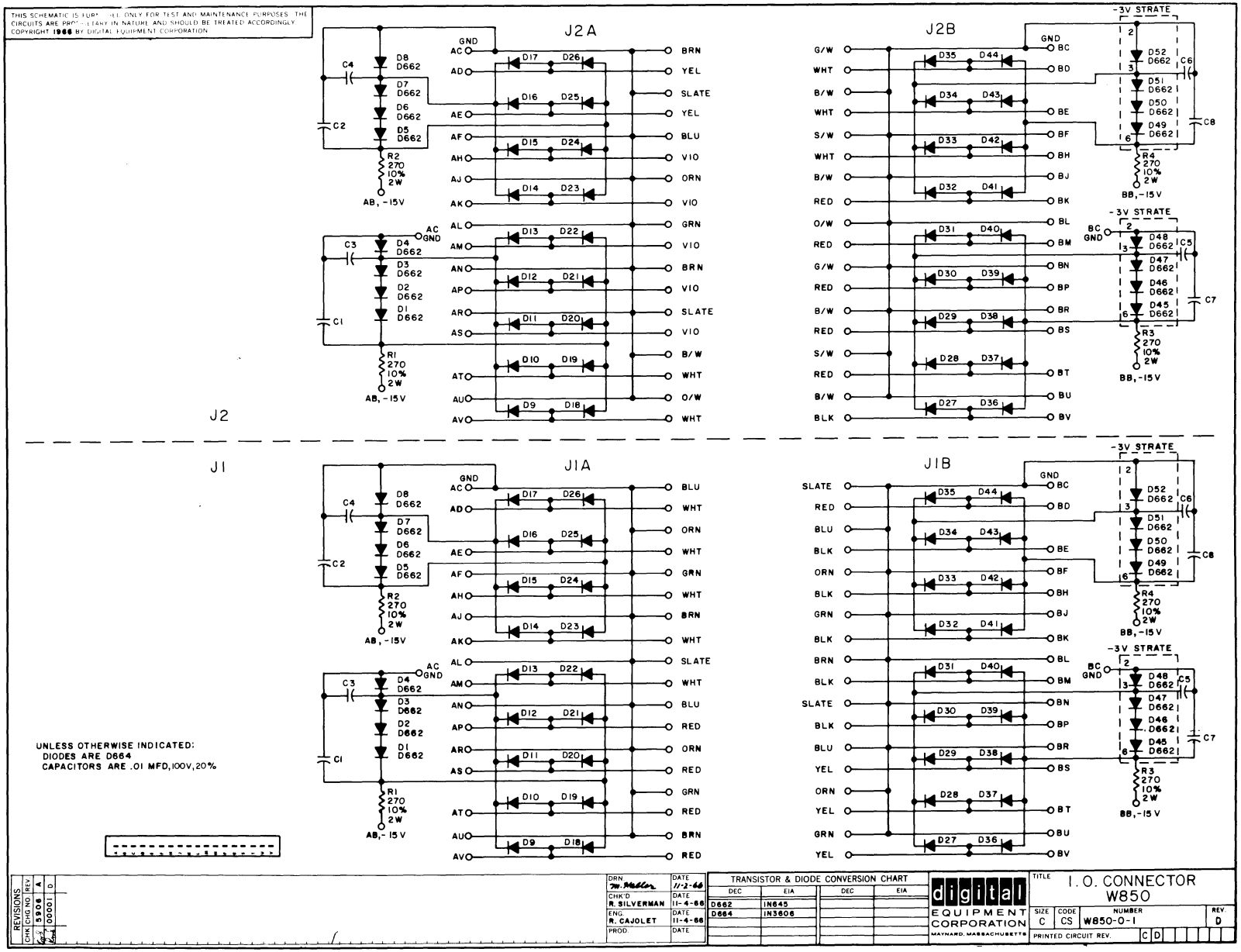
5 PINS

W850
I/O Connector

The W850 module is a double-height FLIP CHIP connector card used in fabricating I/O bus interconnect cables for peripheral devices.

Two of these modules are used to terminate each side of a cable having 36 twisted pairs, thus forming the BL09A cable assembly. One wire of every twisted pair is connected to ground, while the signals carried by each of the 36 signal wires are clamped to -0.6V and -3.0V by diodes.

Power dissipation of the W850 module is 15V at 250 mA (maximum).



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D662	1N645		
D664	1N3606		

REVISIONS			
CHK	CHG NO.	REV.	
	5906	A	
	00001	D	

DRN. M. Keller	DATE	11-2-66
CHK'D R. SILVERMAN	DATE	11-4-66
ENG. R. CAJOLET	DATE	11-4-66
PROD.	DATE	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE I.O. CONNECTOR W850

SIZE	CODE	NUMBER	REV.
C	CS	W850-0-1	D

PRINTED CIRCUIT REV. C D

W850-2

15-0154
W850
D26
D25
D24
D23
D22
D21
D20
D19
D18
D44
D43
D42
D41
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D34
D33
D32
D31
D30
D29
D28
D27
C2
D5
D6
D
D8
C4
C1
D1
D2
D3
D4
C3
R2
C8
C6
C7
C5
R4
R3
R1
D49
D50
D51
D52
D45
D46
D47
D48

Digital Equipment Corporation
Maynard, Massachusetts

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