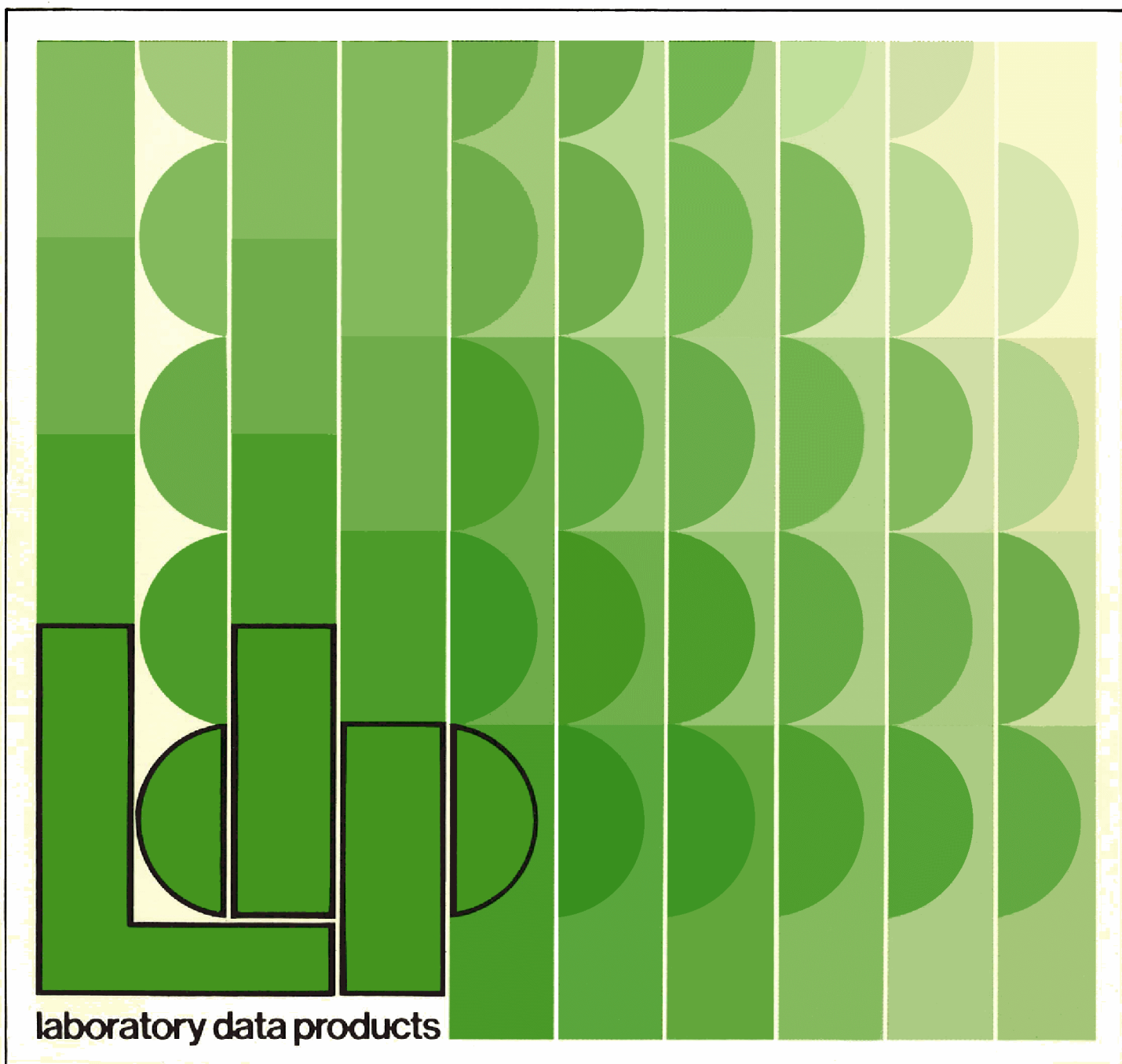


LPS11
laboratory peripheral
system
user's guide



laboratory data products

DEC-11-HLPGA-C-D

**LPS11
laboratory peripheral
system
user's guide**

1st Edition, March 1973
2nd Printing, September 1973
3rd Printing (Rev), January 1974
4th Printing, November 1974

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CHAPTER 1

LPS11 SYSTEM

1.1 INTRODUCTION

The Lab Peripheral System is a high performance, modular, real-time subsystem that interfaces with the PDP-11 family of computers via a single asynchronous bus, the Unibus. The flexibility of the system makes it well suited to a variety of applications, including biomedical research, analytical instrumentation, data collection and reduction, monitoring, data logging, industrial testing, engineering, and technical education.

1.2 SCOPE OF MANUAL

This manual offers the information that the Lab Peripheral System user needs to use the system effectively. Chapter 1 describes the overall system and the interrelationship of its parts from a functional standpoint. Chapters 2 through 5 cover options to the system, including the LPSAD-12 A/D Converter, the LPSKW Real-Time Clock, the LPSDR Digital I/O, and the LPSVC Display Control, respectively. Each chapter contains a detailed description of the option, as well as programming information. Instructions, register addresses, and vector addresses are listed in the appendices.

1.3 GENERAL DESCRIPTION

The Lab Peripheral System includes a 12-bit A/D converter, a programmable real-time clock with two Schmitt triggers, a display controller with two 12-bit D/A converters, and a 16-bit digital I/O option. Dual sample-and-hold preamplifiers and direct memory access capabilities for the A/D system are also available on an optional basis.

The front panel of the LPS11-S is designed to facilitate interfacing with outside instrumentation. The LPS11-S is 5-1/4 in. high, and mounts in a standard 19-in. cabinet. The power supply and all necessary cabling are included.

1.4 DETAILED DESCRIPTION

The Lab Peripheral System is available in six standard configurations, listed in Table 1-1. These are divided into rack mountable and table top configurations, and each is available for operation with 115V, 50/60 Hz, 230V, 50/60 Hz, or 100V, 50/60 Hz input power.

Up to nine different option types may be added to the basic Lab Peripheral System package. These options and their prerequisites are listed in Table 1-2, and are described in greater detail in succeeding chapters.

1.4.1 Standard LPS11-S

The standard LPS11-S is the basic unit of the Lab Peripheral System. It is housed in a 5-1/4 in. box, and includes power supply, bus control, prewired backplane, and front and back panels. The LPS11-S connects to any PDP-11 computer via a standard Unibus cable.

**Table 1-1
LPS11-S Configurations**

Designation	Description
LPS11-SA	Lab Peripheral System mounting unit, front panel, Unibus interface, and power supply. Rack mountable. 115V, 60 Hz.
LPS11-SB	Same as above except 230V, 50 Hz.
LPS11-SC	Same as above except 100V, 50 Hz.
LPS11-SD	Lab Peripheral System mounting unit, front panel, Unibus interface, and power supply. Table top. 115V, 60 Hz.
LPS11-SE	Same as above except 230V, 50 Hz.
LPS11-SF	Same as above except for 100V, 50 Hz.

**Table 1-2
LPS11-S Options**

Type No.	Description	Prerequisites
LPSAD-12	12-bit ADC, sample & hold, 8-channel multiplexer, and LED (light-emitting diodes) 6-digit programmable decimal readout display.	LPS11-S
LPSAD-NP	Direct memory access (DMA) option for the LPSAD-12 ADC.	LPSAD-12
LPSAM	Eight-channel expansion multiplexer.	LPSAD-12
LPSSH	Second sample & hold; implement if a dual sample & hold configuration is required.	LPSAD-12 and LPSAM
LPSAG	Four differential preamplifiers with $\pm 1V$ input. Maximum of 4 LPSAGs per LPS11-S system.	LPSAD-12 or LPSAM*
LPSAG-VG	Four independently selectable multigain differential preamplifiers. Ranges: $\pm 1V$, $\pm 5V$, 0 to $+2V$, 0 to $+10V$; all differential inputs.	LPSAD-12 or LPSAM*
LPSKW	Programmable real-time clock and two Schmitt triggers.	LPS11-S
LPSVC	Display control including two 12-bit DACs. This controller is capable of handling DEC VR14 and VR20 CRT displays. Also, Tektronix RM503, 602, 604, 611, and 613 oscilloscopes.	LPS11-S
LPSDR	Sixteen-bit buffered digital I/O with drive capabilities and two programmable N.O. relays.	LPS11-S

*If more than eight channels are implemented.

1.4.1.1 Bus Control – The bus control of the LPS11-S is an interface between the Unibus and the internal bus and LPS11-S options. The bus control forms its own internal bus (Figure 1-1), permitting the system to address up to six options, cause interrupts, and transfer data. It can decode up to 16 sequential addresses. These addresses are jumper selectable; changing the jumpers changes the total block of 16, but the respective ordering remains the same.

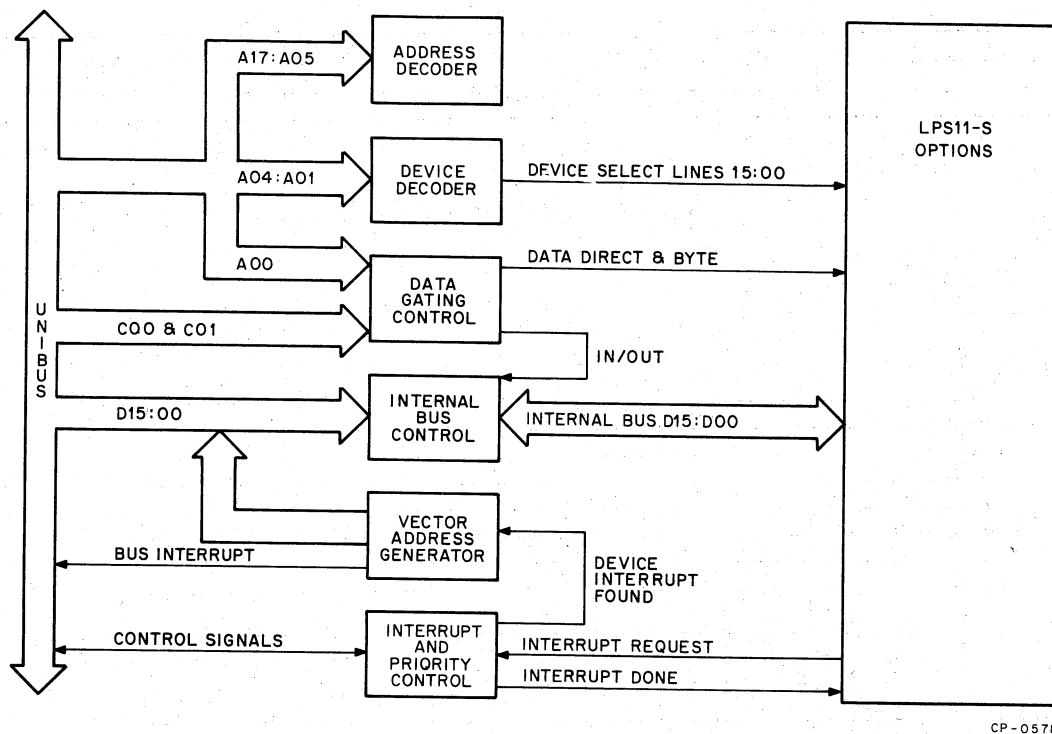


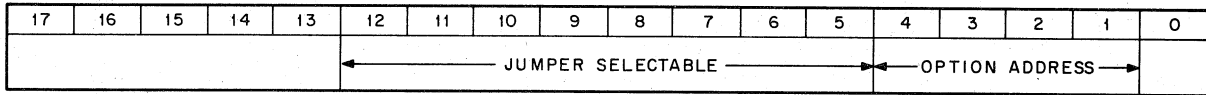
Figure 1-1 LPS11-S Bus Control Block Diagram

The bus control can handle six interrupts at individual bus priorities. Each option has its own interrupt and interrupt vector address (vector addresses are also selectable, and are defined as a floating vector field), its own interrupt priority chip (pluggable on the bus control), and its own enable/disable jumper for interrupts.

Bus control interfacing involves address lines, interrupts, and priorities.

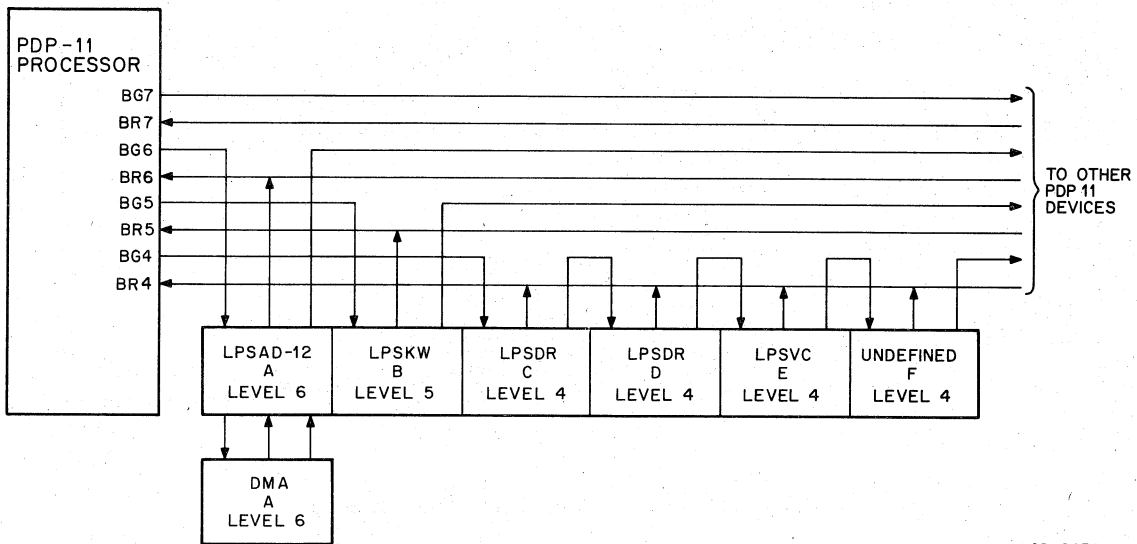
- a. **Address Lines** – Eighteen address lines are used to address the Lab Peripheral System and its options. The address register is shown in Figure 1-2. Bits 12–05 are jumper selectable (A12 through A05 jumpers), allowing the user to change the address block. The module is shipped with addresses as shown in Appendix A; these may be changed, but the respective ordering will remain the same.
- b. **Interrupts** – Interrupts may occur at any time from any Lab Peripheral System device. Upon issuance of an interrupt request from the device, the interrupt control of the bus control checks the BG and BR lines for priorities. When a BG is generated, the vector address generator sends an interrupt vector address to the Unibus. A bus interrupt is then generated, and the processor interrupts to the address specified by the vector address generator. Appendix A illustrates the vectors and their floating addresses. These addresses are sequential in nature, and exist between locations 000 and 777 (jumper assignable).

- c. Priorities – Priorities are necessary when two or more interrupts occur simultaneously. When this occurs, the bus grant priority control examines the interrupt requests and determines which device has the highest priority. That device is handled first, after which the next highest priority is established. This priority chaining (Figure 1-3) allows interrupts to be handled efficiently.



CP-0483

Figure 1-2 Address Register



CP-0476

Figure 1-3 Priority Chaining of LPS11 System

If Device A and Device C and Device E should all interrupt simultaneously, the bus grant priority control would allow Device A (Level 6 is high) to interrupt first (Devices C and E are Level 4, which is low). After the Device A interrupt is completed, Device C would be granted the next interrupt because it is electrically closer to the PDP-11 than is Device E, even though both are Level 4. Finally, Device E would be granted its interrupt.

The levels of operation indicated in Figure 1-3 are interchangeable. The bus control is shipped in this configuration, which is suggested for the user. If the levels are changed, however, the user must consider the following:

- Device importance
- Size of typical device transfer (number of words maximum)
- Duration of typical transfer (time maximum).

1.4.1.2 Power Supply – Power for the LPS11-S is supplied by a special supply, providing +5V at 13A and ±15V at 2A each.

1.4.1.3 Front Panel – The front panel of the LPS11-S is divided into three main areas (Figure 1-4). The largest of these areas, labeled ANALOG INPUT, includes phone jacks for inputs to analog channels 0–7, potentiometer knobs for channels 0–3, and a 6-digit light emitting diode (LED) display. This area is described in greater detail in Chapter 2 of this manual, covering the LPSAD-12 A/D Converter.

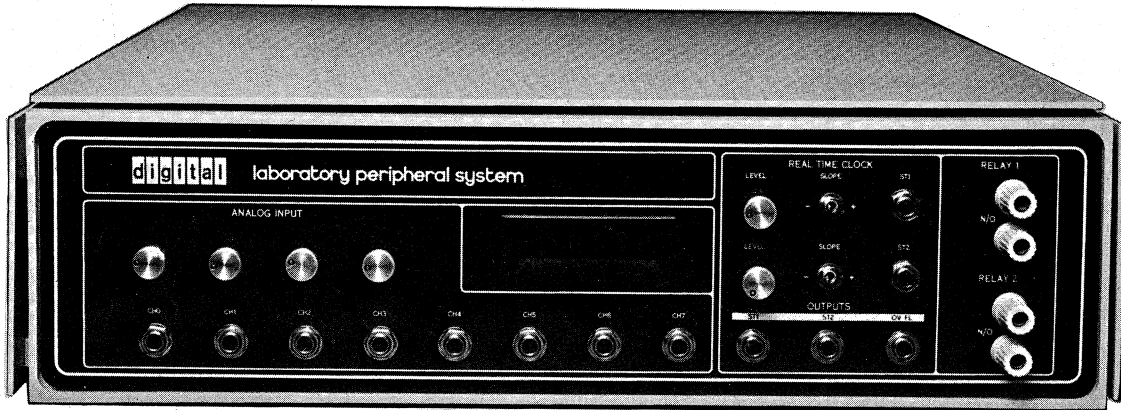


Figure 1-4 LPS11-S Front Panel

The second area of the LPS11-S front panel, labeled REAL TIME CLOCK, includes an output jack for the clock counter overflow and identical sets of controls and phone jacks for Schmitt triggers 1 and 2, each set consists of an input jack, an output jack, a slope polarity switch, and a firing level potentiometer. This area is described in greater detail in Chapter 3 of this manual, covering the LPSKW Real-Time Clock option to the Lab Peripheral System.

The third area of the front panel includes two pair of binding posts, labeled RELAY 1 and RELAY 2 after the two normally-open relays that they represent. These are controlled by the LPSDR Digital I/O option to the Lab Peripheral System, and are described more completely in Chapter 4 of this manual.

1.4.1.4 Back Panel – The back panel of the LPS11-S contains four 25-pin connectors which service three of the options to the Lab Peripheral System. Each connector is labeled to indicate which option it services, and is added to the box when the related option is added to the system. The connectors are routed through a connector shield board to the options (Figure 1-5). Pin assignments for the individual connectors are listed in tabular form in the chapters covering their related options.

CHAPTER 2

ANALOG-TO-DIGITAL CONVERTER SUBSYSTEM

2.1 GENERAL DESCRIPTION

The analog-to-digital subsystem enables the Lab Peripheral System user to sample analog data at specified rates and to store the equivalent digital value for subsequent processing. The basic subsystem consists of an 8-channel multiplexer (eight single-ended $\pm 5V$ inputs), sample-and-hold circuitry, a 12-bit A/D converter, and six programmable light emitting diode (LED) numerical readouts. Available options provide for:

- a. System Expansion – The LPSAM multiplexer makes it possible to expand the LPSAD-12 to 16 channels.
- b. Dual Sample-and-Hold – The LPSSH option permits the user to acquire data from two fixed and predetermined channels simultaneously.
- c. Direct Memory Access (DMA) – The LPSAD-NP option allows the transfer of data to memory at maximum rates without processor intervention, eliminating the software overhead of programmed I/O transfers.
- d. Preamplification – The LPSAG option implements four channels with preamplifiers and provides a $\pm 1V$ differential input to each of those channels. Ranges of 0 to 2V, $\pm 5V$, and 0 to 10V are additionally available via the LPSAG-VG option.

2.1.1 Block Diagram

Figure 1-5 shows an expanded A/D subsystem for the Lab Peripheral System in block diagram form. The basic subsystem may be expanded to a more elaborate configuration that includes 16 multi-range differential channels, dual sample-and-hold, a 12-bit analog-to-digital converter (ADC), and the direct memory access (DMA) interface, as well as a real-time clock. The clock is described more completely in Chapter 3; the other available options are described in the following paragraphs.

2.2 DETAILED DESCRIPTION

2.2.1 LPSAD-12

The LPSAD-12 is a 12-bit successive approximation A/D converter, consisting of four functional modules: an M7018 A/D Control module, an A804 A/D Converter module, an A406 Sample-and-Hold module, and an A407 8-Channel A/D Multiplexer module.

The M7018 A/D Control module controls all A/D operations. Its status register decodes multiplexer operation, sample-and-hold operation, A/D converter operation, and DMA operation. The A/D buffer register receives the converted analog signal in offset binary format.

A/D conversion may be initiated by a programmed instruction, or, if the Lab Peripheral System configuration includes the LPSKW Real-Time Clock, by either the overflow from the clock counter or the firing of a Schmitt trigger. During the conversion, the sample-and-hold mode is changed from sample to hold. The converted offset binary data is placed in the control module A/D buffer register, where it may be tested by the processor, cause an interrupt, or be transferred to memory.

The A804 A/D Converter module, although shipped as a 12-bit A/D converter, is capable of being used as an 8-, 9-, 10-, 11-, or 12-bit converter. The number of bits converted is determined by the position of rotary switch S1 on the A804 module. Conversion time is set using potentiometer R23, which is the center potentiometer on the module. Recommended conversion times are as follows:

8-Bit: 4.5 μ s
9-Bit: 6 μ s
10-Bit: 8 μ s
11-Bit: 15 μ s
12-Bit: 19 μ s

For improved differential linearity, the 12-bit conversion may be set for as high as 25 μ s.

2.2.2 LPSAM

The LPSAM option consists of a single A407 8-Channel A/D Multiplexer module, which operates in the same manner as the 8-channel multiplexer of the LPSAD-12. When not preceded by a preamplifier, it provides eight single-ended ± 5 V inputs.

2.2.3 LPSAG/LPSAG-VG

The LPSAG and LPSAG-VG options provide preamplification for the analog channels. The LPSAG provides a ± 1 V differential input to each of the four channels it serves. Two LPSAGs are needed to amplify all eight channels of the basic LPSAD-12. Two more are required if an LPSAM is implemented into the Lab Peripheral System.

The LPSAG-VG, which is also a 4-channel preamplifier, operates in a manner similar to the LPSAG in providing a ± 1 V input, but also offers additional gain and offset ranges of 0 to 2V, ± 5 V, and 0 to 10V. The input ranges for each of the four channels are individually selectable, as described in Paragraph 2.3.2.

2.2.4 LPSSH

The LPSSH option is contained on a single A406 Sample-and-Hold module, and provides dual sample-and-hold capability. The basic sample-and-hold circuitry ensures adequate conversions, even on rapidly changing signals, by holding the input voltage constant until the conversion process is complete. The LPSSH permits simultaneous sampling of two fixed and predetermined channels, and is controlled by the status register.

The system must contain both the basic LPSAD-12 and an LPSAM as prerequisites to the LPSSH.

2.2.5 LPSAD-NP

The LPSAD-NP Direct Memory Access (DMA) interface consists of a single M7020 DMA module. The primary function of this interface is to store data faster than normal I/O programming will allow. The throughput rate of A/D conversions can be increased from 40 kHz to the actual converter speed (50 kHz-12 bits/100 kHz-10 bits/150 kHz-8 bits). The LPSAD-NP is designed primarily for single-channel operation; however, dual-channel operation is also possible.

The only prerequisite for the LPSAD-NP is the LPSAD-12.

2.3 USER INTERFACING

The LPSAD-12 is the basic building block of the Lab Peripheral System A/D converter subsystem. Access is via the front panel, shown in Figure 2-1. Table 2-1 contains specifications for the LPSAD-12, LPSAM, and LPSAG/LPSAG-VG.

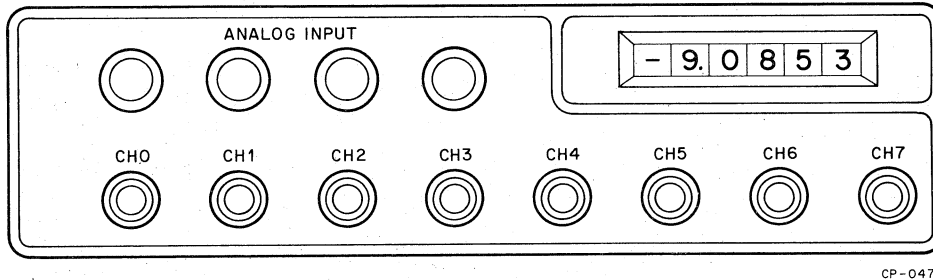


Figure 2-1 Analog Section of Front Panel

Table 2-1
LPSAD-12, LPSAM, and LPSAG/LPSAG-VG
Specifications Summary

Characteristic	Specification
LPSAD-12 A/D Converter Option	
Input voltage range	±5V, single-ended
Input channels	8
Input impedance	10 ⁹ Ω in parallel with 100 pF, measured at rear panel.
Input bias current	
Channel on (±10V input)	200 nA typ. For -10V < V in < +10V (Input clamps to ±10V) Switching transient = -5 mA maximum 0.5 μs maximum
Crosstalk	80 dB at 1 kHz, rolling off at 20 dB per decade.
Warmup time	3 minutes
Control	Controlled by programmed instructions, clock counter overflow, or Schmitt trigger from LPSKW
Maximum program throughput rate	PDP-11/20 with optimal coding:
Programmed start	40 kHz typical
Overflow or Schmitt trigger start	45 kHz typical

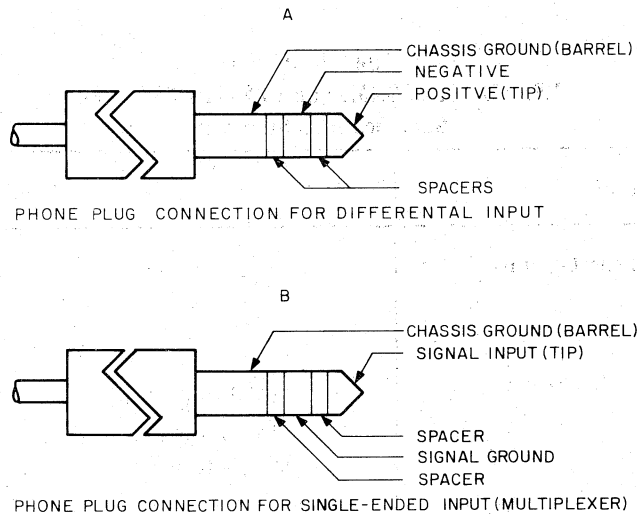
Table 2-1 (Cont)
LPSAD-12, LPSAM, and LPSAG/LPSAG-VG
Specifications Summary

Characteristic	Specification
LPSAD-12 A/D Converter Option (Cont)	
Resolution	12 bits (1 part in 4096) can be reduced to 8, 9, 10, or 11 bits for faster conversion time with switch on module
Output format	Parallel, 12 bits, right justified, offset binary, double buffered
Accuracy, at 25°C	±0.035% of full scale
Linearity	0.02% of full scale
Differential linearity	1 LSB
Temperature stability	30 ppm/°C (0.003%FS/°C)
Repeatability	$2\sigma \leq 1/2$ LSB
Conversion time	The time lapse from start command until a 12-bit result is acquired is 20 μ s.
LPSAM Multiplexer Option	
Input voltage range	±5V, single-end
Input channels	8
Input impedance	$10^9 \Omega$ in parallel with 100 pF, measured at rear panel
Input bias current	
Channel on (±10V input)	200 nA typ. For $-10V < V_{in} < +10V$ (Input clamps to ±10V) Switching transient = -5 mA maximum 0.5 μ s maximum
Channel off	200 nA typ.
Crosstalk	80 dB at 1 kHz, rolling off at 20 dB per decade
Analog output voltage range	±5V

Table 2-1 (Cont)
LPSAD-12, LPSAM, and LPSAG/LPSAG-VG
Specifications Summary

Characteristic	Specification
LPSAG/LPSAG-VG Preamplifier Options	
Input voltage range	
LPSAG	±1V differential
LPSAG-VG	±1V, 0 to +2V, ±5V, 0 to +10V
Input channels	4
Crosstalk	80 dB at 1 kHz, rolling off at 20 dB per decade
Input impedance	
+ to ground	128K in parallel with 100 pF
- to ground	64K in parallel with 100 pF
Differential	128K in parallel with 50 pF
Input bias current	40 nA maximum at + or - input
Common mode rejection	60 dB at 0 to 60 Hz
Accuracy	0.005% of full scale
Linearity	0.005% of full scale
Analog output voltage range	±5V
Bandwidth	
3 dB	60 kHz
1 dB	30 kHz
Full power	4 kHz, ±5V output
Slew rate	0.3V/μs, typical

All eight channels are connected to standard 1/4-in., 3-terminal phone jacks on the front panel, permitting direct interfacing with laboratory equipment. Figure 2-2 shows the correct phone plug connections for handling external signals. In addition, channels 0-3 are also connected to 10-turn potentiometer knobs that can be used as program parameter inputs. With the phone plugs removed, these potentiometers provide a full-scale analog input. When an external voltage is applied via insertion of one of the plugs, the output voltage of that potentiometer is disabled, allowing the user to apply external analog data to that analog channel for computer processing.

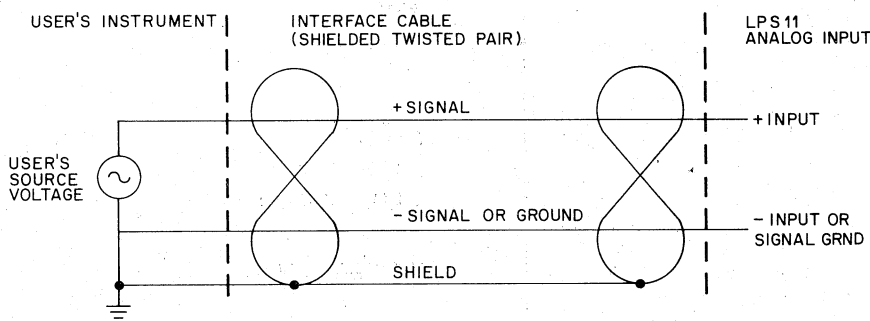


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Figure 2-2 Correct Phone Plug Connections for Handling External Signals

Figure 2-3 shows the recommended input wiring. The user should ensure a good ground between the LPS11-S and the units to be measured, all of which should be plugged into the same power lines, if possible, to minimize ground currents. A twisted, shielded pair is recommended for each channel input. The shield should be connected at the source end only, and should never be used as a ground strap between one chassis and another unless it is known absolutely that no extraneous current will flow between them, since such current could affect the input leads, causing extraneous noise in measurements.

The front panel also contains the 6-digit LED display, which can serve as a general purpose programmable device, permitting the display to be used as a time readout for the LPSKW Real-Time Clock, an LPSDR digital status indicator, an A/D channel display, or for similar visual indications.



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Figure 2-3 Recommended Input Wiring

2.3.1 A407 Eight-Channel A/D Multiplexer

The multiplexer makes it possible to incorporate up to 16 channels; eight in the multiplexer unit of the LPSAD-12, and another eight in an LPSAM. Interconnection is accomplished by one of two methods.

- a. If the LPSSH option is not installed, the expander node outputs of each multiplexer are joined and become the analog node for the multiplexers.
- b. If the LPSSH option is installed, multiplexer 10–17 connects directly to the second S&H as shown in Figure 1-5; channels 10–17 are accessed via the back panel. RC1 (analog 10–17) pin assignments are listed in Table 2-2.

Table 2-2
RC1 Analog Inputs

Pin	Signal Name	Pin	Signal Name
1	GND	14	GND
2	RC1 - CH17*	15	RC1 - CH16*
3	RC1 + CH17	16	RC1 + CH16
4	RC1 - CH15*	17	GND
5	RC1 + CH15	18	RC1 - CH12*
6	GND	19	RC1 + CH12
7	RC1 - CH14*	20	GND
8	RC1 + CH14	21	RC1 + CH11
9	GND	22	RC1 - CH11*
10	RC1 - CH13*	23	GND
11	RC1 + CH13	24	RC1 + CH10
12	GND	25	RC1 - CH10*
13	GND		

*When preamplifiers are not installed, this connection is signal ground.

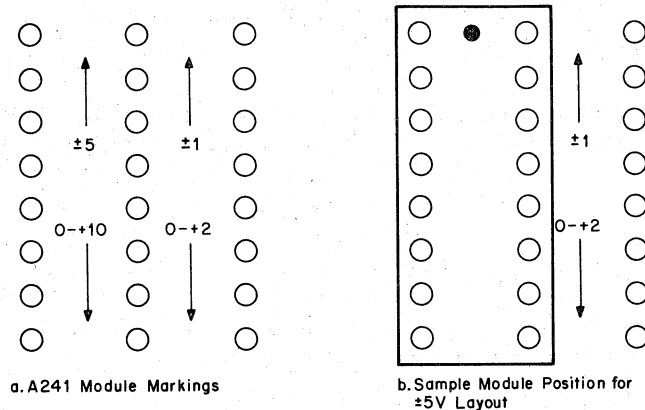
2.3.2 A/D Preamplifiers

The LPSAG is a 4-channel preamplifier intended as a front-end interface to the LPSAD-12. This unit plugs into the LPS11-S and provides a $\pm 1V$ differential input to the four channels that it serves. Two LPSAG preamplifiers are needed to amplify all eight channels of the LPSAD-12, and two more if an LPSAM requires preamplifiers. All rear panel controls and connectors operate in the same manner.

The LPSAG-VG is a 4-channel preamplifier, similar in operation to the LPSAG, but offering additional differential input gain and offset ranges. The range for each of the four channels may be selected or varied independently by the user via plug-in jumpers.

Each plug is marked with a dot, which is used to establish the direction of the plug. Thus, as Figure 2-4 indicates, in order to select a channel input of $\pm 5V$, the plug is mounted in the two leftmost rows with the dot at the top. An input of $\pm 1V$ may be obtained by moving the plug to the two rightmost rows, still with the dot at the top. Ranges of either 0 to 2V or 0 to 10V may be selected by inverting the plug so that the dot is at the bottom. Each of the four channels on the module is marked correspondingly. By switching input wires it is also possible to obtain the additional ranges of 0 to $-10V$ and 0 to $-2V$. Table 2-3 is a range chart for the LPSAG and LPSAG-VG.

If no preamplifiers are used, the preamplifier module slots in each LPSAD-12 or LPSAM are implemented with G728 Jumper modules to maintain continuity between the front panel and the multiplexers. If preamplifiers are subsequently added, they will replace the jumper modules on a one to one basis.



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Figure 2-4 LPSAG-VG Channel Range Selection via Jumper

Table 2-3
LPSAG, LPSAG-VG Range Chart

Octal Readout	Scale	Output/Range			
		±5V	±1V*	0 → 10V	0 → 2V
7777	+FS-1LSB	+4.9975	+0.9995	+9.9975	+1.9995
4000	Mid Scale	0.0000	0.0000	+5.0000	+1.0000
0000	-FS	-5.0000	-1.0000	0.0000	0.0000
Bit Size (MV)		2.44= 1 LSB	.488= 1 LSB	2.44= 1 LSB	.488= 1 LSB

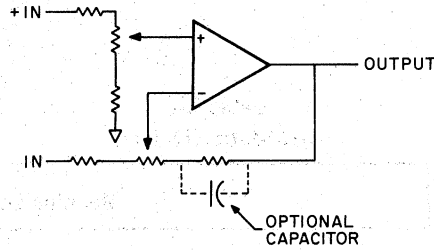
*Only ±1V range applies to LPSAG, all ranges apply to LPSAG-VG. The ±5V range also applies to multiplexer input.

The user benefits in several ways from the LPSAG/LPSAG-VG options:

- Converting from Single-Ended to Differential Inputs – The differential input makes it possible to measure differences between two sources, and to determine accurately a noisy source or a signal being measured with respect to a potential other than the ground of the Lab Peripheral System, because of the high common-mode rejection of the differential amplifier. Ground loop problems are significantly reduced, permitting more trouble-free interfacing to low-level signals.
- Providing Isolation – Installing the LPSAG or LPSAG-VG isolates the user's signal source from the switching and clamping currents of the analog multiplexer while maintaining a relatively high input impedance, thus eliminating the effect of source impedance on internal switching times and crosstalk.
- Low-Pass Filtering – The preamplifiers act as a natural filter to high frequency signals (e.g., noise) beyond the useful sampling rate of the A/D converter and yet detrimental to experimental results.

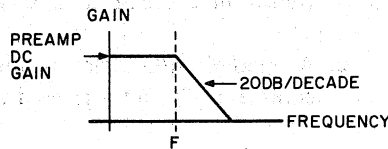
- d. **Additional Filtering** – In situations where the signal input to be measured is superimposed on high frequency noise, the bandwidth of the preamplifier may be reduced to attenuate the unwanted part of the information; however, the preamplifier must be operated single-ended (Figure 2-5) and inverting, i.e., the positive input must be grounded. This requires that no common mode signal or ground loop need be rejected by the preamplifier.

The bandwidth is reduced by the addition of a capacitor across printed circuit bands provided within the preamplifier feedback loop (Figure 2-5). The chart in Figure 2-6 gives 3 dB breakpoints for some values of capacitors.



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Figure 2-5 Low Pass Filtering



C (MFD)*	F (Hz)
1.00	2.5
0.10	25
0.01	250

3db BREAKPOINT FOR SELECTED CAPACITOR VALUES

*C must be a non-polarized capacitor

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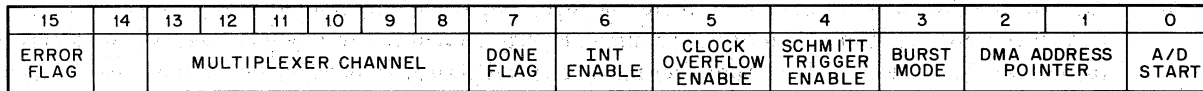
Figure 2-6 Bandwidth Reduction via Capacitor

2.4 PROGRAMMING

The Lab Peripheral System derives its addresses from the bus controller logic, with the first two addresses being assigned to the LPSAD-12. They are defined in Appendix B. The first interrupt vector address in the system is assigned to LPSAD-12 also (Appendix B). The bus request level for the LPSAD-12 is determined by a priority jumper in the LPS11-S control logic. This level is set to 6 prior to shipping.

2.4.1 A/D Status Register

The A/D status register is illustrated in Figure 2-7 and described in Table 2-4.



↑
RESERVED FOR
DUAL MODE
ENABLE

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Figure 2-7 A/D Status Register

Table 2-4
A/D Status Register

Bit	Name (Read/Write)	Meaning and Operation
15	Error Flag (R)	This bit is set when: <ul style="list-style-type: none"> a. A second A/D conversion ends before data from the previous A/D conversion is read. b. The multiplexer is changed during the first microsecond (HOLD transition of the S&H circuit) of a conversion. c. A second A/D start is initiated before the first conversion is complete. This bit is cleared when loaded or upon INIT.
14	Dual Mode Enable	1 = Dual S&H enable 0 = Single S&H
13-8	Mux Channel (R/W)	Defines which channel of the multiplexer is to be sampled.
7	Done Flag (R)	Set upon completion of A/D conversion. Cleared by hardware when an interrupt is completed or when the data register is read.
6	Interrupt Enable (R/W)	When a conversion is completed, the done flag will cause an interrupt if this bit is set to a 1.
5	Overflow Enable (R/W)	Permits overflow from LPSKW Real-Time Clock to cause an A/D start. This allows channel sampling at precisely timed intervals independent of software. Data may then be read by testing the done flag or by enabling the interrupt.
4	Schmitt Enable (R/W)	Permits an external event to fire a Schmitt trigger, which, in turn, initiates an A/D conversion.
3	Burst Mode	Permits continuous conversion at the maximum rate of the converter until DMA overflow, if DMA enable is set.

Table 2-4 (Cont)
A/D Status Register

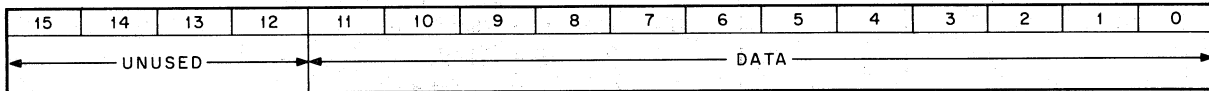
Bit	Name (Read/Write)	Meaning and Operation															
2-1	DMA Address Pointer	Decoded as follows: <table border="0"> <tr> <td>2</td> <td>1</td> <td>DMA Register</td> </tr> <tr> <td>0</td> <td>0</td> <td>No Register</td> </tr> <tr> <td>0</td> <td>1</td> <td>DMA Status Register</td> </tr> <tr> <td>1</td> <td>0</td> <td>Word Count Register</td> </tr> <tr> <td>1</td> <td>1</td> <td>Current Address Register</td> </tr> </table>	2	1	DMA Register	0	0	No Register	0	1	DMA Status Register	1	0	Word Count Register	1	1	Current Address Register
2	1	DMA Register															
0	0	No Register															
0	1	DMA Status Register															
1	0	Word Count Register															
1	1	Current Address Register															
0	A/D Start (R/W)	Starts an A/D conversion. Cleared at end of conversion.															

2.4.2 A/D Buffer

The A/D data buffer address serves two purposes. When read, it furnishes the 12-bit converted value after an A/D conversion is completed, formatted in 12-bit right-justified offset binary (Figure 2-8):

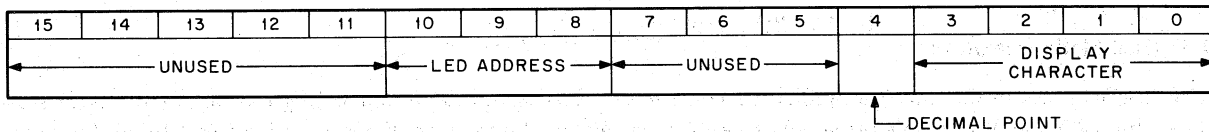
Input Volts	12-Bit Result (Octal)
+	007777
0	004000
-	000000

When loaded, the data buffer address programs the LED display on the front panel (Figure 2-9). These digits must be loaded one at a time, and will then remain displayed until changed. Table 2-5 contains the bit assignments for the A/D buffer (LED).



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
Figure 2-8 A/D Buffer Register (Read Only)



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Figure 2-9 LED Register (Write Only)

Table 2-5
A/D Buffer Bit Assignments

Bit	Assignments			
15-11	Not Used.			
10-8	Defines LED Address.			
	Bit 10	Bit 9	Bit 8	Digit
	0	0	0	LED 1 (Rightmost)
	0	0	1	LED 2
	0	1	0	LED 3
	0	1	1	LED 4
	1	0	0	LED 5
	1	0	1	LED 6 (Leftmost)
	1	1	0	Unused
	1	1	1	Unused
7-5	Not Used.			
4	When set, illuminates decimal point in addition to numeral.			
3-0	Selects numeral to be displayed:			
	3	2	1	0
	0	0	0	0 = 0
	0	0	0	1 = 1
	0	0	1	0 = 2
	0	0	1	1 = 3
	0	1	0	0 = 4
	0	1	0	1 = 5
	0	1	1	0 = 6
	0	1	1	1 = 7
	1	0	0	0 = 8
	1	0	0	1 = 9
	1	0	1	0 =  (test pattern)
	1	0	1	1 = Blank
	1	1	0	0 = Blank
	1	1	0	1 = - (Minus)
	1	1	1	0 = Blank
	1	1	1	1 = Blank

2.4.3 Dual Mode Operation

The LPSAD-12 controller has the ability to control the dual sample-and-hold configuration. In the A/D status register, bit 14 is the dual enable bit which, when set, permits dual operation. When bit 14 is disqualified, the second S&H is not used.

Channel selection in this mode requires the user to select the channel of his first sample, which must be one of channels 0 through 7; this channel automatically determines its dual partner, the corresponding channel in channels 10 through 17. By issuing an A/D START command, the user causes the respective analog inputs of the selected channel and its dual partner to be sampled, and the voltage of the former converted to its digital value. The second sample is held longer to allow the A/D converter to operate on the first sample. When the converter completes the conversion and flags the computer, another A/D START command, without changing the multiplexer, will cause the voltage of the dual partner to be converted to its digital value. Either prior to or during this time, the first sample should be read into the computer. After the second sample is acquired, the user can change the multiplexer channel, or continue to sample the same channels.

This operation can be performed on eight separate pairs of channels, but must be sequenced as follows:

First Sample	Second Sample
Channel 0	Channel 10
Channel 1	Channel 11
Channel 2	Channel 12
Channel 3	Channel 13
Channel 4	Channel 14
Channel 5	Channel 15
Channel 6	Channel 16
Channel 7	Channel 17

As noted above, the first channel selected in dual mode must be from 0 through 7. If, for example, channel 17 were to be the first channel selected, the first sample would be meaningless; the second sample would be the value of channel 17.

The user must always take two samples to acquire both channels of data. If only one sample is taken, the voltage on the second sample will be acquired first during the next A/D conversion. The second sample-and-hold can maintain 12-bit accuracy for 100 μ s; therefore, the user must initiate the second sample within 75 μ s.

The LPSKW Real-Time Clock can start A/D conversions directly, either by clock overflow or by firing Schmitt trigger 1 with an external signal. In dual mode, either method requires the program to acquire the second sample with an A/D START command, provided it is not in DMA mode. The LPSKW initiates the first conversion; when the A/D interface flags the computer that it is completed, the program starts the second conversion. After the second sample is accepted, the A/D converter waits for the next clock signal.

A conversion done in dual mode is tested in the same way as any other conversion.

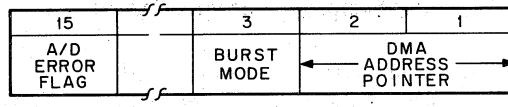
2.4.4 DMA Operation

In DMA operation, A/D conversions can be started in three ways: overflow from the clock, external input through Schmitt trigger 1, or by a program start. In all three cases, the samples are automatically taken and transferred directly to core. For dual mode DMA operation, two samples are automatically taken and transferred directly to core. Assuming that channel 0 is selected, the sequence of data in core would be as follows:

Channel 0	Data
Channel 10	Data
Channel 0	Data
Channel 10	Data

In dual mode DMA operation, the user must be careful to select the proper word count. Because two samples must be taken under dual-burst DMA, the number of dual points needed must be half of the word count. An odd value in the word count register will result in loss of the second sample of the last transfer; in addition, the next DMA transfer would begin with the lost sample.

To conserve Unibus addresses, only one address is defined as the DMA address. This 16-bit address will work with the A/D status register bits 2 and 1, which will define it as either the word count register, the current address register, or the DMA status register, as decoded in Table 2-4. Before loading or reading the DMA address, the user must first define these bits in the A/D status register. No byte operations are permitted with the DMA address. If the user should try a byte operation, the entire 16-bit word would be transferred. Figure 2-10 and Table 2-6 show A/D status register bit usage for the DMA.



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Figure 2-10 A/D Status Register Segment

Table 2-6
A/D Status Word and DMA Address

A/D Status Bit	Bit		DMA Function
	2	1	
Bits 2, 1	0	0	DMA Address Pointer (R/W). The DMA address will not load any register. When the DMA is not installed, these bits should be zeroed.
	0	1	When the A/D status bits are in this state, the DMA address will point to the DMA status register.
	1	1	This state defines the DMA address as the Current Address register.
	1	0	This state defines the DMA address as the Word Count register,
Bit 3	Burst Mode (R/W)		When bit 3 = 1 and the DMA enable bit (12) in the DMA status register has been enabled, the A/D will convert as fast as the system will allow it, until DMA overflow.

2.4.4.1 DMA Status Register – The DMA status register is a 4-bit register that defines the extended address bits, the DMA enable, and the time-out flag. Loading and reading of these bits occurs as shown in Figure 2-11 and Table 2-7.

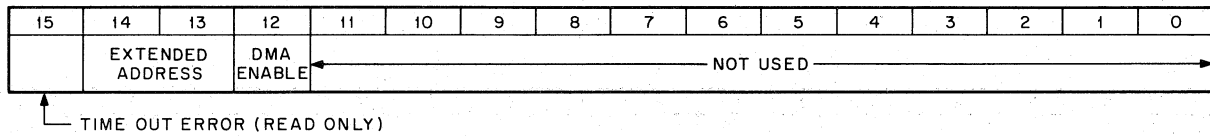
When set, the DMA enable bit (bit 12) will enable the DMA, and will remain set until the required number of transfers has been completed. Before each block of transfers can occur, the user must load the current address register and word count register, and set this bit.

The extended address bits (14, 13) allow the user to store data anywhere in 128K of core (32K core segments).

The time-out error bit is read-only, and occurs when the NPR device has not released the processor within 20 μ s. Each time the DMA status register is loaded, this bit clears automatically.

In addition to the three types of errors described in Table 2-4 for the A/D status register, another type, the time-out error, can occur when the DMA option is used. This error indicates that the DMA interface has held the processor for more than 20 μ s, or that A/D conversion data is being received more rapidly than the DMA is capable of transferring it to core. Bit 15 in the DMA status register is set when this error occurs, and should be tested after all DMA conversions are completed.

At the end of a block transfer, the A/D control interrupts the computer. This interrupt cannot be disabled, and occurs through the same interrupt circuitry as normal I/O transfers. The priority and vector address are the same as for the LPSAD-12.



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Figure 2-11 DMA Status Register

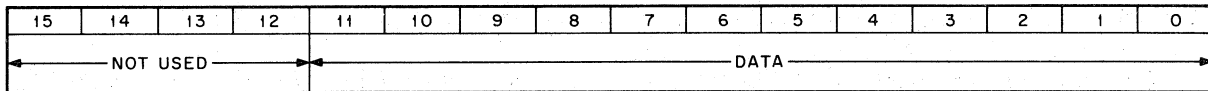
Table 2-7
DMA Status Register Bit Assignments

DMA Status Bits	Function	Description
12	DMA Enable	When set, qualifies DMA transfers.
14, 13	Extended Address	Qualify data transfer with the extended address.
15	Time-out	A read-only bit denoting that the DMA interface has held the processor for more than 20 μ s, or that data from the A/D conversion is coming faster than the DMA can transfer it to core.

2.4.4.2 DMA Word Count Register – The word count register is a 12-bit register that determines the number of transfers that will occur (Figure 2-12). After each DMA transfer, this register is incremented. When the word count register overflows, an interrupt occurs, signifying the correct amount of data has been transferred, after which the DMA enable bit is cleared and all transfers cease. The 2's complement of the word count must be loaded; thus, if one transfer is desired, the user would load 07777 in the DMA word count register. The maximum amount of data that may be accepted in one operation is 4096 words.

Bit 11–0 Word Count

The word count is a 12-bit number that defines the number of transfers to occur. The 2's complement of the number is loaded. A maximum of 4096 words may be transferred.

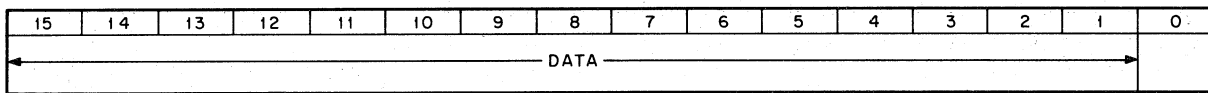


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Figure 2-12 DMA Word Count Register (Complement)

2.4.4.3 DMA Current Address Register – The current address register is a 16-bit register that defines the location in core where the data is to be stored (Figure 2-13). After each transfer, the current address register is incremented. This register can be loaded with any location in the first 32K of core, but if the user wishes to store data in locations above the first 32K of core, the extended address bits of the DMA status register must be used.

Bit 15–0 Current Address Bit 0 is undefined, since the user can only transfer to even addresses. This bit will always be forced to 0. This register defines the starting location of DMA transfers.



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Figure 2-13 Current Address Register

The only restriction on using the LPSAD-NP is in large system programming. When systems require other NPR devices (tape, disk, etc.) to work simultaneously, the average latency of the Unibus can be 4.0 μ s. If the A/D is run at rates faster than the computer can accept data, the result could be loss of data; therefore, care must be used in defining systems with the LPSAD-NP.

2.4.4.4 Programming Sequence to Operate the DMA Option –

1. Load A/D status register bits 2 and 1 with “11,” which will direct the DMA address to the current address register.
2. Load the current address register, using the DMA address with the location in core where the data is to be transferred.
3. Load A/D status register bits 2 and 1 with “10,” which will direct the DMA address to the word count register.
4. Load the word count register, using the DMA address with the 2’s complement number of transfers to occur.
5. Load A/D status register bits 2 and 1 with “01,” which will direct the DMA address to the DMA status register.
6. Load the DMA status register, using the DMA address. The extended address bits and the DMA enable should be loaded.

7. Load the A/D status register with the following information:
 - a. Channel – Select the multiplexer channel in which the conversions are to occur.
 - b. Modes – Select the method of starting the A/D conversion.
 - c. Dual – If the A/D is configured for dual sample-and-hold, the DMA will make two conversions for every point of data.
 - d. Interrupt Enable – The interrupt enable will have no effect in DMA operation. An interrupt will always occur at the end of a block transfer.
 - e. Burst Mode – Permits continuous conversion at maximum system rate until DMA overflow.
8. Initiate an A/D conversion in one of the three standard ways: clock overflow, external input via Schmitt trigger, or program start. At the end of the conversion, the DMA will transfer the data to core. When all of the data has been transferred, an interrupt will occur, and the DMA enable bit will be cleared. To initiate a second block transfer, the user must repeat the above steps. (See the programming examples below.)

2.4.5 Programming Examples

2.4.5.1 Programming Example 1 – Read 100 A/D conversions into locations 4000–4200 and halt.

Location	Instruction	Comment
START:	CLR A/D STATUS	; CLEAR STATUS
	MOV#4000, R0	; SET UP FIRST ADDRESS
	INC A/D STATUS	; START A/D CONVERSION ON CHANNEL 0
LOOP:	TSTB A/D STATUS	; CHECK DONE FLAG
	BPL LOOP	; WAIT UNTIL FLAG SET
	INC A/D STATUS	; START NEXT CONVERSION
	MOV A/D BUFFER, (R0) +	; PLACE CONVERTED VALUE IN A/D BUFFER INTO ; CORE LOCATION AND SET UP NEXT CORE ; LOCATION FOR TRANSFER
	TSTB R0	; CHECK IF 100 CONVERSIONS HAVE BEEN DONE
	BPL LOOP	; NO-GET NEXT CONVERSION
	HALT	; DONE

2.4.5.2 Programming Example 2 – Read 100 A/D conversions into locations 4000–4200 by sampling two channels simultaneously, and halt.

Location	Instruction	Comment
START:	CLR A/D STATUS	; CLEAR STATUS
	MOV#4000, R0	; SET UP FIRST ADDRESS
	MOV#42020, A/D STATUS	; READ CHANNELS 4 AND 14 WHEN ST1 FIRES
LOOP:	TSTB A/D STATUS	; CHECK DONE FLAG
	BPL LOOP	; WAIT UNTIL FLAG SET
	INC A/D STATUS	; START NEXT CONVERSION
	MOV A/D BUFFER, (R0) +	; PLACE CONVERTED VALUE IN A/D BUFFER INTO ; CORE LOCATION AND SET UP NEXT CORE LOCATION ; FOR TRANSFER
LOOP + 2:	TSTB A/D STATUS	; CHECK IF DONE
	BPL LOOP + 2	; NO-WAIT
	MOV A/D BUFFER, (R0) +	; PLACE CONVERTED VALUE IN A/D BUFFER INTO ; CORE LOCATION AND SET UP NEXT CORE LOCATION ; FOR TRANSFER
	TSTB R0	; CHECK IF 100 CONVERSIONS HAVE BEEN DONE
	BPL LOOP	; NO-GET NEXT ST1 SAMPLE
	HALT	; DONE

2.4.5.3 Programming Example 3 – Using Burst Mode and DMA:

Location	Instruction	Comment
LOOP:	MOV#6, ADSR	; LOAD THE A/D STATUS REGISTER WITH A VALUE THAT PERMITS ; THE DMA ADDRESS TO OPERATE ON THE CURRENT ADDRESS ; REGISTER.
	MOV#2000, DMA	; THE STARTING LOCATION OF THE DMA TRANSFER IS LOADED ; INTO THE CURRENT ADDRESS REGISTER.
	MOV#4, ADSR	; LOAD THE A/D STATUS REGISTER WITH A VALUE THAT PERMITS ; THE DMA ADDRESS TO OPERATE ON THE WORD COUNT ; REGISTER.
	MOV#7000, DMA	; (1000) ₈ TRANSFERS ARE LOADED INTO THE WORD COUNT ; REGISTER.
	MOV#00002, ADSR	; LOAD THE A/D STATUS REGISTER WITH A VALUE THAT ; PERMITS THE DMA ADDRESS TO OPERATE ON THE DMA ; STATUS REGISTER.
	MOV#10000, DMA	; LOAD THE DMA ENABLE BIT IN THE DMA STATUS REGISTER.
	MOV#00013, ADSR	; LOAD THE A/D STATUS REGISTER WITH BURST MODE, ; CHANNEL 0, AND START THE A/D CONVERSIONS.
	WAIT	; WAIT FOR AN INTERRUPT.
	HALT	; STOP, TRANSFERS ARE COMPLETE.
	BR LOOP	; START AGAIN (BY PRESSING CONTINUE).

Interrupt Subroutine for DMA

Location	Instruction	Comment
ROUT:	TST ADSR	; CHECK FOR LOST DATA.
	BPL CONT	; NO, GO TO CONT
	HALT	; ERROR
CONT:	TST DMA	; CHECK FOR TIME-OUT.
	BPL GO	; NO, BRANCH TO GO
	HLT	; ERROR.
GO:	RTI	; RETURN FROM INTERRUPT.

2.4.5.4 Programming Example 4 – Load the contents of A/D buffer into front panel LED readouts:

Location	Instruction	Comment
START:	MOV#6, CNTLED	; LOAD COUNTER
	CLR, LEDSV3	; CLEAR LED POINTER
	MOV A/D BUFFER, LEDSV1	; STORE A/D BUFFER
LEDSA:	MOV LEDSV1, LEDSV2	; MOVE LEDSV1 to LEDSV2
	BIC#177770, LEDSV2	; CLEAR ALL BITS EXCEPT BITS 2, 1, 0
	MOVB LEDSV3, LEDSV2+1	; MOV LOW BYTE OF LEDSV3 TO HIGH ; BYTE OF LEDSV2
	MOV LEDSV2, A/D BUFFER	; LOAD LED READ OUTS
	ASR LEDSV1	; ARITH SHIFT RIGHT
	ASR LEDSV1	; ARITH SHIFT RIGHT
	ASR LEDSV1	; ARITH SHIFT RIGHT
	INC LEDSV3	; INCREMENT LEDSV3
	DEC CNTLED	; DECREMENT COUNTER
	BNE LEDSA	; NOT DONE, GO BACK TO LEDSA
	HALT	; DONE
	CNT LED:6	; COUNTER
	LEDSV1:0	; STORAGE REGISTER
	LEDSV2:0	; WORKING REGISTER
	LEDSV3:0	; LED POINTER

2.5 LPSAM-SG AND BA408 SWITCHED GAIN OPTIONS

2.5.1 Description

The LPSAM-SG and BA408 are switched gain multiplexer options with program-selectable gains of 1, 4, 16 and 64, allowing for expansion of the dynamic range of the LPS from 12 bits (4095:1) to 18 bits (262,080:1). The BA408 option consists of a single A408 module, which is directly pin-for-pin compatible with the LPSAD-12 multiplexer (A407 module). The BA408 replaces either the A407 supplied with the LPSAD-12 for channels 0–7, or the A407

supplied with the LPSAM for channels 10–17. The LPSAM-SG is an A408, with additional hardware required for input of channels 10–17. The two types of multiplexers (A407 and A408) must not be mixed. Gain programming is accomplished by means of the two MUX expansion bits originally reserved for MUX expansion to 64₁₀ channels. Thus, it is not possible to have both switched gain and LPS11-E expansion beyond 16 channels. Worst case settling time (including both gain and channel change settling) is 15 μ s, allowing 25 KHz program throughput to core. Constant bandwidth (typically 150 KHz) is maintained, independent of gain level. Throughput rates under external start, clock overflow start, or DMA control are the same as with the A407 module; there are no channel changes in these conditions.

2.5.2 Performance Specifications

Input Channels	8 (single-ended)								
Switching	Break-before-make								
Input Range	<table border="0"> <tr> <td>± 5 V</td> <td>G=1</td> </tr> <tr> <td>± 1.25 V</td> <td>G=4</td> </tr> <tr> <td>± 312.5 mV</td> <td>G=16</td> </tr> <tr> <td>± 78.125 mV</td> <td>G=64</td> </tr> </table>	± 5 V	G=1	± 1.25 V	G=4	± 312.5 mV	G=16	± 78.125 mV	G=64
± 5 V	G=1								
± 1.25 V	G=4								
± 312.5 mV	G=16								
± 78.125 mV	G=64								
Gain Accuracy	0.02%								
Linearity	0.01%								
Input Impedance	$>10^9 \Omega$ in parallel with 0.01 μ f								
Input Bias Current	± 400 nA max., -15 V $<V_{in}$ $<+10$ V								
Input Offset Voltage	Adjustable to zero								
Offset Drift	5 μ V/ $^{\circ}$ C max. RTI* + 120 μ V/ $^{\circ}$ C max. RTO*								
Bandwidth	100 KHz min., 150 KHz typ.								
Settling Time (to $\pm 1/2$ LSB)	15 μ s max.								
Crosstalk	80 db min. at 1 KHz, 20 db/decade rolloff								
Noise (rms)	70 μ V max. RTI* + 550 μ V max. RTO* <table border="0" style="margin-left: 100px;"> <tr> <td>G=1</td> <td>0.25 LSB max.</td> </tr> <tr> <td>G=4</td> <td>0.33 LSB max.</td> </tr> <tr> <td>G=16</td> <td>0.66 LSB max.</td> </tr> <tr> <td>G=64</td> <td>2 LSB max.</td> </tr> </table>	G=1	0.25 LSB max.	G=4	0.33 LSB max.	G=16	0.66 LSB max.	G=64	2 LSB max.
G=1	0.25 LSB max.								
G=4	0.33 LSB max.								
G=16	0.66 LSB max.								
G=64	2 LSB max.								
Warmup Time	3 minutes								

*RTI – referred to input

*RTO – referred to output

2.5.3 Packaging

The LPSAM-SG option consists of an A408 single-height module, which plugs into the slot reserved for the channel 10–17 multiplexer module in the LPS11 basic mounting box, plus the cable and jumper cards required for input of the 10–17 analog inputs from the backpanel. The BA408 consists of an A408 module to replace the multiplexer module used for analog inputs 0–7.

2.5.4 Programming

Gain is programmed using the two highest order address bits of the LPSAD status register (bits 12 and 13) which were previously reserved for expansion beyond the original 16 channels, as shown in Table 2-8.

Table 2-8
Gain Programming

Bit 13	Bit 12	Gain	Input Range
0	0	1	±5 V
0	1	4	±1.25 V
1	0	16	±312.5 mV
1	1	64	±78.125 mV

Thus, two gain bits and a 4-bit channel address can be programmed, or a 6-bit channel address can be used as shown in Table 2-9.

Table 2-9
6-Bit Channel Addresses

Address	Result
Channels 0–17	Channels 0–17 at G=1
Channels 20–37	Channels 0–17 at G=4
Channels 40–57	Channels 0–17 at G=16
Channels 60–77	Channels 0–17 at G=64

Note that for channels 0–17 the switched gain multiplexer is both hardware and software compatible with the fixed gain multiplexer.

In addition, any software written to support the full 64-channel address capacity of the LPSAD-12 status register also supports the switched gain option automatically.

2.5.5 Switched Gain with LPSSH

If the LPSSH option is not installed, the node outputs of the two switched gain multiplexer modules are tied together, as is the case with fixed gain multiplexer modules.

If the LPSSH option is installed, each multiplexer module feeds its own sample-and-hold module. In simultaneous sample-and-hold operation, the LPSAD-12 controller adds 10_8 to the selected channel to obtain the address of the second channel. As with the fixed gain multiplexer, if channel 0 is selected, channels 0 and 10 are simultaneously

sampled and converted in turn. With switched gain multiplexers installed, if channel 40 is sampled (channel 0 at a gain of 16), then channels 40 and 50 are simultaneously sampled, i.e., the two simultaneous samples are always at the same gain level.

2.5.6 Switched Gain with Pre-Amps

2.5.6.1 Input Ranges – Input ranges of an LPSAD-12 system with switched gain multiplexer and LPSAG or LPSAG-VG pre-amps are shown in Table 2-10, at the four gain levels of 1, 4, 16, and 64.

Table 2-10
Input Ranges

Gain	LPSAM-SG/BA408	LPSAG	LPSAG-VG			
			±1 V	0 to 2 V	±5 V	0 to 10 V
1	±5 V	±1 V	±1 V	0 to 2 V	±5 V	0 to 10 V
4	±1.25 V	±250 mV	±250 mV	0 to 500 mV	±1.25 V	0 to 2.5 V
16	±312.5 mV	±62.5 mV	±62.5 mV	0 to 125 mV	±312.5 mV	0 to 62.5 mV
64	±78.125 mV	±15.625 mV	±15.625 mV	0 to 31.25 mV	±78.125 mV	0 to 156.25 mV

2.5.6.2 Resolution – The least significant bit (LSB) value, or resolution, of an LPSAD-12 system with switched gain multiplexer and LPSAG or LPSAG-VG pre-amps is shown in Table 2-11, at the four gain levels of 1, 4, 16, and 64.

Table 2-11
Least Significant Bit (LSB) Value, Resolution

Gain	LPSAM-SG/BA408	LPSAG	LPSAG-VG	
			±1 V, 0–2 V	±5 V, 0–10 V
1	2.44 mV	488 μV	488 μV	2.44 mV
4	610 μV	122 μV	122 μV	610 μV
16	152.5 μV	30.5 μV	30.5 μV	152.5 μV
64	38.125 μV	7.625 μV	7.625 μV	38.125 μV

2.5.6.3 Zero Drift with Pre-Amps – Worst case zero drift of the LPSAG and LPSAG-VG pre-amps is 30 μV/° C, referred to the input. When running with LPSAG pre-amps or LPSAG-VG pre-amps set for ±1 V or 0 to 2 V inputs, with the A408 multiplexer at G=64, the LSB value is approximately 8 μV. Consequently, when running under these conditions, software baseline correction should be considered, as required by the application.

2.5.6.4 Noise Levels with Pre-Amps – The LPSAM-SG/BA408 noise specs in Paragraph 2.5.2 do not include pre-amp noise. When using LPSAG pre-amps or LPSAG-VG pre-amps with ±1 V or 0 to 2 V input ranges, referred-to-input (RTI) noise levels are a factor of five higher. This translates to the following maximum rms noise levels, expressed in number of LSB “counts”.

Gain	rms Noise (LSB)
1	0.36
4	0.78
16	2.46
64	9

These figures represent the noise present in the broad bandwidth, which supports full 25-KHz throughput under any conditions of gain and channel switching. Significant noise reductions can be achieved by using the filtering method discussed below.

2.5.7 Filtering the Switched Gain Input

2.5.7.1 Reasons for Input Filtering – Generally, there are two cases in which it is desirable to filter an analog input to remove its high frequency components.

Anti-Aliasing – It is necessary to sample any analog signal at a rate which is at least twice the frequency of the highest frequency components present in the signal, whether these high-frequency components are signals of interest or noise. For example, if a signal is sampled once per millisecond (1 KHz), there should be no frequency components present above 500 Hz. Any frequency components present above one-half the sampling frequency cause “aliasing” – the generation of spurious beat frequencies between dc and one-half the sampling frequency. In many cases, it is known that the input signal is already bandwidth limited, so no further filtering is required. However, in some applications, high-frequency components are present and filtering is then desirable.

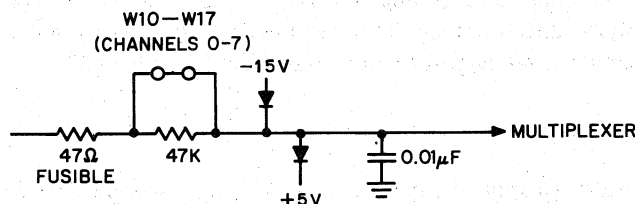
Noise Filtering – The level of “white” noise can be reduced by filtering, with the rms value decreasing with the square root of the bandwidth. Thus, significant noise reduction (and corresponding improvement in signal-to-noise ratio) can be achieved by inserting a low-pass filter to remove high-frequency noise components without affecting the low-frequency signals of interest.

2.5.7.2 Filtering Capability of the Switched Gain Multiplexer – Input circuitry of a single switched gain multiplexer channel is shown in Figure 2-14.

The switched gain multiplexer option is shipped with jumpers W10–W17 connected, so that the input impedance consists of a 0.01 μ F capacitor to ground. This permits a user to implement a low-pass input filter, with the external source resistance controlling the break frequency, according to the following equation:

$$F_b = \frac{1}{2\pi R_s C}$$

R_s = Source resistance
 $C = 0.01 \mu\text{F}$



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Figure 2-14 Switched Gain Multiplexer Input

Values of the break frequency for typical source resistance values are shown in Table 2-12.

Table 2-12
Break Frequencies and Source Resistance Values

R_s	F_b
1K	16 kHz
3.3K	5 kHz
10K	1.6 kHz
33K	500 Hz
47K	340 Hz
100K	160 Hz

When using the switched gain multiplexer with pre-amps, it is inconvenient to provide a source resistance to work in conjunction with the 0.01 μF input capacitor as a low-pass filter. Consequently, the multiplexer is equipped with jumpers W10–W17, which, when removed, provide a 47K source resistance, thereby reducing the bandwidth to 340 Hz on channels 0–7, respectively.

This bandwidth reduction is recommended when the switched gain multiplexer is used at a gain of 64 with LPSAG pre-amps or LPSAG-VG pre-amps with $\pm 1\text{ V}$ or 0–2 V input ranges. Under these conditions, with no bandwidth reduction, the equivalent rms input noise is 9 LSB maximum, corresponding to about 70 μV . With the bandwidth reduced, (jumper cut), the rms input noise drops to a maximum of 2 LSB, corresponding to about 15 μV . Typical rms noise is 1–1.5 LSB, and this can be further reduced to 0.5–1 LSB (4–8 μV) by means of line-synchronous sampling, under control of the LPSKW, KW11-L or KW11-P Real-Time Clock options, or the LTC feature of the 11/05–11/10 processor.

2.5.7.3 Zero Shift Due to Filter — Introduction of a source resistance, either externally or by cutting the bandwidth jumper, results in an input offset voltage shift equal to the source resistance times the A408 module's bias current (400 nA maximum, 40 nA typical). In systems with pre-amps installed, this offset can be nulled out for each channel with the pre-amp balance potentiometer, using the procedure in Paragraph 4.2.5.4 of the *LPS Maintenance Manual*.

2.5.7.4 Throughput Limitations Due to Filter — The switched gain multiplexer settling time of 15 μs is for conditions of zero source impedance and bandwidth jumper uncut, i.e., no input low-pass filter implemented. Under these conditions, the programmer need not be concerned with settling effects, since the LPSAD-12 controller allows 15 μs after a programmed start before initiating the A/D conversion. This allows a full 25 kHz throughput capability.

With the input filter implemented on a given channel, it is necessary to provide a program delay to allow for slower settling between channels. When switching between two channels at the same gain level, the output settles within 3% of the inter-channel voltage difference in the initial 15 μs and then approaches the final value with a time constant of $R_s C$. When switching from one channel to another channel operating at higher gain, the effect is larger than 3% because the inter-channel voltage difference can be larger than the full scale input range at the higher gain. When switching from a high-gain channel to a low-gain channel, the effect is less than 3%.

Example 1,

Channel 0 input +5 V, Channel 1 input -5 V, $R_s = 3.3\text{K}$, corresponding to a time constant of 33 μs and $F_b = 5\text{ kHz}$. The inter-channel voltage difference is 10 V, so the initial settling error is 3% of 10 V, or 300 mV. At a gain of 1, the LSB value is 2.5 mV, and it takes five time constants, or 165 μs for the error to be less than 1 LSB.

Example 2

Channel 0 input +5 V, Channel 1 input -78 mV, $R_s = 3.3K$; now switch from channel 0 to channel 61, increasing the gain by a factor of 64 as channels are changed. The inter-channel voltage difference is 5.078 V, giving an initial input error of 3% of 5.078 V, or 152 mV. Thus, the input after the first 15 μ s is at +74 mV instead of -78 mV, and at a gain of 64, this error amounts to 97% of the input range. To settle within 1 LSB from this error takes about 8.5 time constants, or 280 μ s.

Example 3

Channel 0 input +5 V, Channel 1 input -78 mV, bandwidth jumper cut, corresponding to $R_s = 47K$, for a time constant of 0.47 ms and $F_b = 340$ Hz. Here, if channel 0 is switched to channel 61, the same voltage conditions as in Example 2 are present, necessitating a delay of 8.5 time constants. With the larger source resistance, the required delay is 4 ms.

Note that these throughput limitations only apply when switching into a channel with external source resistance or whose bandwidth jumper has been cut. All remaining (unfiltered) channels may still be scanned at 25 kHz, and a single channel with reduced bandwidth may be sampled at rates up to 25 kHz, as long as no channel switching occurs.

Allowable throughput rates under various filter configurations are summarized in Table 2-13.

Table 2-13
Throughput Rates

R_s	F_b	Single-Channel		Multi-Channel Single Gain		Multi-Channel Multi-Gain	
		Software Delay Req'd	Throughput	Software Delay Req'd	Throughput	Software Delay Req'd	Throughput
0	(Unfiltered)	0	25 kHz	0	25 kHz	0	25 kHz
1K	16 kHz	0	25 kHz	50 μ s	15 kHz	85 μ s	11 kHz
3.3K	5 kHz	0	25 kHz	165 μ s	5.5 kHz	280 μ s	3.5 kHz
10K	1.6 kHz	0	25 kHz	500 μ s	2 kHz	850 μ s	1.15 kHz
33K	500 Hz	0	25 kHz	1.65 ms	600 Hz	2.8 ms	350 Hz
47K*	340 Hz	0	25 kHz	2.35 ms	425 Hz	4 ms	250 Hz
100K	160 Hz	0	25 kHz	5 ms	200 Hz	8.5 ms	115 Hz

*Bandwidth jumper cut

CHAPTER 3

LPSKW PROGRAMMABLE REAL-TIME CLOCK

3.1 GENERAL DESCRIPTION

The LPSKW Real-Time Clock option offers the Lab Peripheral System user several methods for accurately measuring and counting intervals or events. The clock can be used to synchronize the central processor to external events, count external events, measure intervals of time between events, or provide interrupts at programmable intervals. It can also be used to start the analog-to-digital converter by means of the overflow from the clock counter or by the firing of a Schmitt trigger. Many of these operations can be performed concurrently.

The clock will operate in any one of four programmable modes: single interval, repeated interval, external event timing, and event counting from zero base. The user can select from five crystal-controlled frequencies: 1 MHz, 100 kHz, 10 kHz, 1 kHz, or 100 Hz. The LPSKW may also use an external (Schmitt trigger) input or a line frequency input as a time base.

Two Schmitt triggers with front panel slope and level adjusting knobs are included with the real-time clock. The Schmitt triggers can start and read the clock, start the A/D converter, and cause program interrupts.

3.2 BLOCK DIAGRAM DESCRIPTION

The LPSKW is a prewired option for the Lab Peripheral System. It is contained on a single quad-size M7016 module, which includes a status register, a rate control, a mode control, a counter register, a buffer/preset register, and an interrupt control. Figure 3-1 is a block diagram of the LPSKW option.

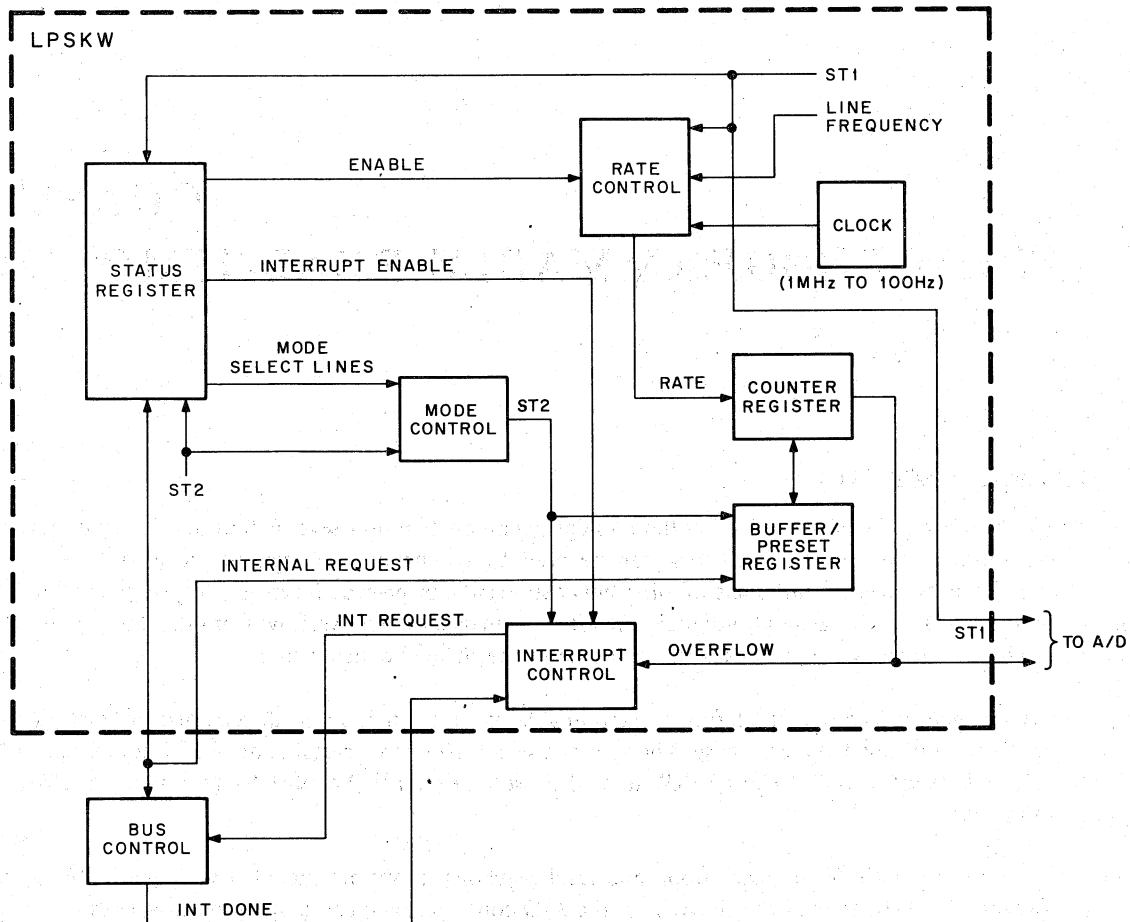
The real-time clock works with the M7015 Unibus Control module, transferring all data, addresses, and interrupts via the internal bus. All clock operation is controlled by the clock status register, which controls the rate, mode, and counter registers.

3.2.1 Status Register

When the status register enables the rate control, a selected rate (1 MHz to 100 Hz, line frequency, or Schmitt trigger 1) clocks the 16-bit counter register, which may be loaded from or read into the buffer/preset register at any time via the mode control or Schmitt trigger 2. By selecting one of four modes, the user can decide what data the multiplexer will pass when loading the buffer/preset register and the counter.

Overflow of the counter may cause an interrupt if the interrupt enable bit of the status register is set. (The vector address of that interrupt is defined in Appendix B.) Flags and interrupts are controlled via the status register and mode control, and the user can determine by status register flags whether an interrupt has been caused by the firing of a Schmitt trigger or by an overflow. Either method (Schmitt trigger firing or overflow) may be used to initiate an analog-to-digital conversion.

The status register also controls the mode of operation of the clock, defining the modes of operation in which the clock can be used.



CP-0439

Figure 3-1 LPSKW Block Diagram

3.2.2 Mode Control

The LPSKW Real-Time Clock may be used in any one of four different modes.

3.2.2.1 Single Interval Mode – In this mode, the counter counts from a preset value until it overflows, completes its last count, and returns to all 0s. An overflow turns off the counter, sets the mode flag, and, if the interrupt enable bit is qualified, causes an interrupt. Interrupts can occur only when the proper jumper on the M7015 Bus Control has been removed. By disabling the interrupt enable and sampling the mode flag, it is possible to determine when the operation is complete without causing an interrupt; this is useful in timing single experiments. To re-initialize the counter for a second operation, the buffer/preset is loaded with a value and the clock enable counter bit of the status register is set.

3.2.2.2 Repeated Interval Mode – The user need only load the buffer/preset and enable the counter. After each overflow, the contents of the buffer/preset are transferred to the counter, which continues without losing a single count. If an interrupt occurs, it must be processed before a second interrupt can occur, unless the program permits stacking of interrupts (see *PDP-11 Peripherals and Interfacing Handbook*). This mode permits the user to determine not only the rate of counting, but also the number of counts before overflow, giving him two dimensions in selecting intervals between overflows. The repeated interval mode can be used to start A/D conversions or experiments, to keep time, or even as a variable frequency pulse generator.

Using the full 16-bit counter allows intervals as large as 10.92 minutes or as small as 6.0 μ s. Intervals as small as 1.0 μ s are theoretically possible; however, the programming time necessary to acknowledge the flags and interrupts exceeds the minimum interval of the clock.

3.2.2.3 External Events Timing Mode – In this mode, the counter is free-running. An external pulse from Schmitt trigger 2 (ST2) causes data to transfer from the counter to the buffer/preset while the counter continues to run, causing an interrupt or flag to occur. The program can then sample the value in the buffer/preset register.

3.2.2.4 Event Timing from Zero Base Mode – This mode operates in much the same manner as the external events timing mode, except that the counter is cleared (zeroed) after each transfer to the buffer/preset.

3.2.3 Rate Control and Clock

The rate control, in conjunction with the clock, provides the time base for the LPSKW. Of the seven distinct rates, six are internally generated; the seventh, Schmitt trigger 1 (ST1) is external to the system. The internal programmable rates include 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz crystal-controlled frequencies and a line frequency (50 Hz or 60 Hz). Accuracy of the line frequency depends on the power source; thus, unless an experiment depends on synchronization with the line frequency, it is preferable to use either the crystal oscillator or an external oscillator as a base frequency to program an accurate 50 Hz or 60 Hz signal. The output of the external oscillator would be applied to ST1; however, the maximum rate the external oscillator can run is 250 kHz (square wave). The same method can be used to count external pulses or peaks, provided that the pulse width is 2 μ s or greater. Using the clock as an external counter will provide a maximum number of counts of 65,536.

3.2.4 Buffer/Preset and Counter Registers

The buffer/preset register is a non-byte-oriented 16-bit read/write register which reads, via a multiplexer, the external bus data or the counter data. Internal bus data is normally selected, but the firing of ST2 causes the register to read the contents of the counter in modes 2 and 3. The buffer/preset can be loaded either under program control or upon an ST2 firing. This register should always be loaded before the status register.

The counter register is a 16-bit read/write register which is read by transferring its contents into the buffer/preset register and reading the latter. The counter register is loaded by loading the buffer/preset register and not enabling the counter via the status register.

3.2.5 Interrupt Control

Interrupts are caused by data transfers, overflows, and the firing of Schmitt triggers. Because the clock has only one interrupt and one interrupt vector, two interrupt enables and two flags are provided. When an interrupt occurs, it is necessary to test these flags to determine the source of the interrupt.

The mode flag sets when a counter overflow occurs, when ST2 fires, or when a maintenance bit is used manually to simulate a Schmitt trigger firing for the purpose of transferring the clock counter register to the buffer/preset register. Setting the mode flag when the mode interrupt enable is set will cause an interrupt.

The ST1 flag may also cause interrupts, if a firing occurs while the interrupt enable bit is set; it may be set via a maintenance bit if a programmed Schmitt trigger firing is desired.

3.2.6 Schmitt Triggers

The functions of the two Schmitt triggers on the LPSKW option include the following:

1. Schmitt Trigger 1 (ST1)
 - a. External A/D starts
 - b. External clock inputs
 - c. Starting clock
 - d. Causing interrupts
 - e. Setting flag
2. Schmitt Trigger 2 (ST2)
 - a. Operating during modes 2 and 3
 - b. Causing interrupts during modes 2 and 3
 - c. Transferring counter to buffer/preset
 - d. Setting flag during modes 2 and 3

A more detailed description of the operation of the Schmitt triggers in the LPSKW option to the Lab Peripheral System is provided in Paragraph 3.3.

3.3 USER INTERFACING

The real-time clock section of the Lab Peripheral System front panel (Figure 3-2) contains identical sets of controls and jacks for ST1 and ST2, each set consisting of an input plug, an output plug, a switch to control slope polarity, and a potentiometer for the firing level, as well as an output plug for the clock counter overflow (OVFL).

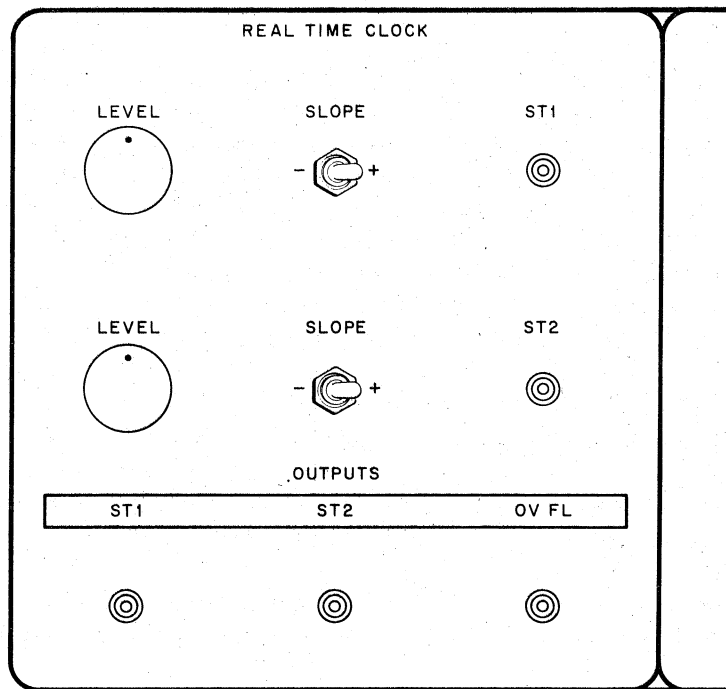


Figure 3-2 Real-Time Clock Front Panel Section

All of the outputs are capable of driving 25 ft of cable at 50 pF/ft, and all may be used to start or stop external events and adjust the Schmitt triggers. Figure 3-3 shows signal connections for the phone jack associated with the front panel plugs mentioned above.

- a. **Overflow** – Overflow is a negative-going pulse which goes from +5V to +0V, and is capable of sinking 30 mA of current and sourcing 10 mA of current. The pulse width may vary from 300 to 450 ns, depending on the clock rate.
- b. **Schmitt Triggers** – The Schmitt triggers are an integral part of the LPSKW, and may be used to initiate A/D conversions or clock operations, cause interrupts, and drive pulse-operated systems from analog sources. Table 3-1 lists Schmitt trigger specifications for the LPSKW.

Input and output plugs for the two Schmitt triggers are labeled ST1 and ST2. Their firing is governed by slope and threshold controls. The potentiometer knobs may be set to the extreme right for +5V, to the extreme left for -5V, or somewhere in between for intermediate voltages. The slope switch may be set to + or -.

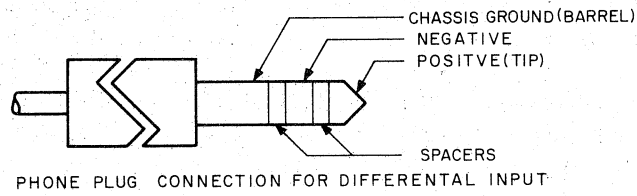


Figure 3-3 Input or Output Phone Jack Connections

Table 3-1
Schmitt Trigger Specifications for the LPSKW

Function	Specification
Input Threshold	Variable between $\pm 5V$
AC Source	Voltages between $\pm 25 V_{ac}$
Input Type	Differential
Input Impedance	$50 K\Omega$
Input Pulse	$2 \mu s$
DC Source	Maximum voltage of $\pm 50 V_{dc}$
Common Mode	35 dB
Propagation Delay	Slew rate dependent
Output Voltage	0 to +5V (falling edge denotes firing and resets on recrossing threshold voltage minus hysteresis)
Hysteresis	.3V typical 1.0V typical (remove W1 and W2 jumpers from M7016)

After a voltage threshold has been selected and either a positive-going or a negative-going slope has been chosen, the Schmitt trigger is ready to begin operation. Each time the external signal crosses the preset voltage in the direction indicated by the slope switch, the Schmitt trigger fires and the output signal drops to zero. When the signal crosses the preset voltage plus the hysteresis voltage in the opposite direction, the output voltage rises from 0 to +5V.

Figure 3-4a illustrates an example of an input signal applied to a Schmitt trigger, with points A and C representing the firing points (assuming positive threshold and positive slope settings), and points B and D representing the points where the Schmitt trigger resets [(+ threshold) - (- hysteresis) = + reset point].

Figure 3-4b illustrates the output of the Schmitt trigger, with a minimum output pulse width of 2 μ s. The falling edge of the output pulse denotes the firing of the Schmitt trigger; the rising edge denotes its reset point. The time between points A and B and points C and D is determined by examining the input wave; the lower the threshold voltage (to a minimum of 0.3V), the longer the output pulse. This function may be seen by observing the input and output signals simultaneously and varying the threshold for that Schmitt trigger.

Figure 3-4c illustrates an internal signal to the real-time clock that is used to pulse the digital logic used by the Schmitt trigger. Because the trigger need not be enabled to make use of its signal-conditioning properties, an analog signal can be used to drive a pulse-operated system by selecting the proper thresholds. (In the case of TTL logic, 2.4V or greater is considered a logic 1, while 0.8V or less is considered a logic 0.)

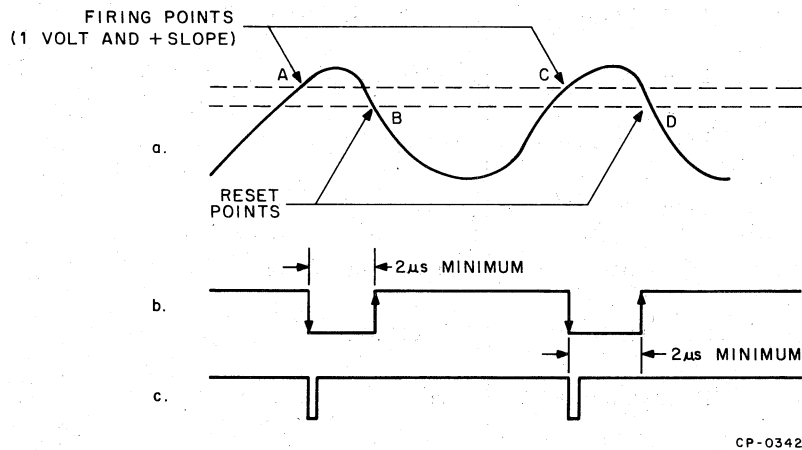


Figure 3-4 Schmitt Trigger Firing

Figure 3-5 further illustrates the reset point formula noted above. It can be seen that only one firing of the Schmitt trigger has occurred between points I and J in the figure, because the input did not extend 0.3V in the opposite direction of the slope. The formula then says:

For + Slope	Threshold Voltage - Hysteresis = Reset
For - Slope	Threshold Voltage + Hysteresis = Reset

Hence, for a +1V peak-to-peak sine wave input, a firing on -1V using a positive slope is not possible. This would require the input wave to go below -1.3V to reset the Schmitt trigger. However, the user could fire at -1V with a negative slope, because the trigger would then reset at -0.7V [(-1V) + (+0.3V) = -0.7V].

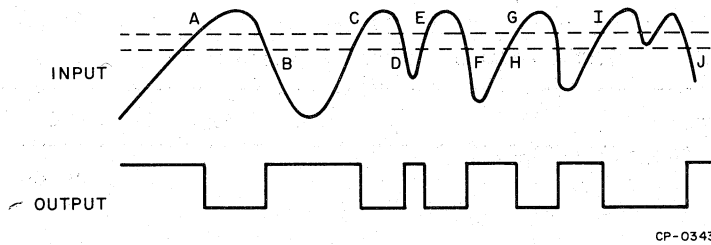


Figure 3-5 Schmitt Trigger Firing – Hysteresis

3.4 PROGRAMMING

3.4.1 Status Register

The status register controls all clock operations by defining the manner in which the clock is to be used. It must be loaded after the buffer/preset register. All normal program instructions, including byte operations, can be performed on this register. It should be noted that a TST or TSTB instruction does not clear the bit which is being tested.

Maintenance bits 10, 11, and 12 of the status register are write-only bits, and will always read back as zeros, as will bits 04 and 05, which are unused (Figure 3-6). All of the other bits are read/write bits. Table 3-2 defines the bit assignments for the LPSKW status register.

Table 3-2
LPSKW Status Register Bit Assignments

Bit	Name	Meaning & Operation
15 (Read/Write)	ST1 FLAG	Sets when ST1 has fired or MAINT ST1 has been loaded.
14 (Read/Write)	ST1 INTERRUPT ENABLE	When set, a firing of ST1 will cause an interrupt.
13 (Read/Write)	ST1 ENABLE	When set, will allow ST1 firing to set the clock enable counter.
12 (Write Only)	MAINT ST1	Used to check operation (digital only) of Schmitt trigger 1 circuitry. Loading this bit simulates the firing of ST1 with regard to all functions.
11 (Write Only)	MAINT COUNT	When loaded with the clock counter enable turned off, this bit simulates a 1 MHz pulse to the counter, providing 1 MHz is selected. By enabling the proper rates, the user can select the base frequency at which the counter will operate, e.g., at a rate of 100 kHz, loading this bit ten times will increment the 16-bit counter by one.
10 (Write Only)	MAINT ST2	Used to check operation (digital only) of Schmitt trigger 2 circuitry. Loading this bit simulates the firing of ST2. Bit 10 can be used to transfer the contents of the counter to the buffer/preset when in mode 10 or 11.

Table 3-2 (Cont)
LPSKW Status Register Bit Assignments

Bit	Name	Meaning & Operation																																								
09-08 (Read/Write)	MODE	<table border="0"> <thead> <tr> <th colspan="2" data-bbox="727 363 824 384">Bits</th> <th data-bbox="1092 363 1190 384">Function</th> </tr> <tr> <th data-bbox="727 394 776 415">09</th> <th data-bbox="792 394 824 415">08</th> <th></th> </tr> </thead> <tbody> <tr> <td data-bbox="727 457 743 478">0</td> <td data-bbox="792 457 808 478">0</td> <td data-bbox="857 457 1385 510">Single interval mode. Counter counts from preset value to overflow, sets mode flag, and stops.</td> </tr> <tr> <td data-bbox="727 552 743 573">0</td> <td data-bbox="792 552 808 573">1</td> <td data-bbox="857 552 1417 636">Repeated interval mode. Counter counts from preset value to overflow, sets mode flag, transfers buffer/preset to counter, and begins again.</td> </tr> <tr> <td data-bbox="727 678 743 699">1</td> <td data-bbox="792 678 808 699">0</td> <td data-bbox="857 678 1417 804">External event timing mode. The counter is free running, and a pulse from ST2 will transfer contents of counter to buffer/preset, set mode flag, then continue counting.</td> </tr> <tr> <td data-bbox="727 867 743 888">1</td> <td data-bbox="792 867 808 888">1</td> <td data-bbox="857 867 1417 993">Event timing from zero base mode is the same except that, upon transfer of the counter to the buffer/preset and setting of the mode flag, the counter is cleared and the count begins from zero.</td> </tr> </tbody> </table>	Bits		Function	09	08		0	0	Single interval mode. Counter counts from preset value to overflow, sets mode flag, and stops.	0	1	Repeated interval mode. Counter counts from preset value to overflow, sets mode flag, transfers buffer/preset to counter, and begins again.	1	0	External event timing mode. The counter is free running, and a pulse from ST2 will transfer contents of counter to buffer/preset, set mode flag, then continue counting.	1	1	Event timing from zero base mode is the same except that, upon transfer of the counter to the buffer/preset and setting of the mode flag, the counter is cleared and the count begins from zero.																						
Bits		Function																																								
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07 (Read/Write)	MODE FLAG	Sets by mode operation as defined below.																																								
06 (Read/Write)	MODE INTERRUPT ENABLE	When set, the setting of the mode flag will cause an interrupt.																																								
04-05		Unused.																																								
03-01 (Read/Write)	RATE	<p>Controls the rate of the base frequency. The user may select the following rates:</p> <table border="0"> <thead> <tr> <th colspan="3" data-bbox="873 1371 971 1392">Bits</th> <th data-bbox="1011 1371 1247 1392">Function (Frequency)</th> </tr> <tr> <th data-bbox="824 1402 873 1423">03</th> <th data-bbox="889 1402 938 1423">02</th> <th data-bbox="954 1402 1003 1423">01</th> <th></th> </tr> </thead> <tbody> <tr> <td data-bbox="824 1465 841 1486">0</td> <td data-bbox="889 1465 906 1486">0</td> <td data-bbox="954 1465 971 1486">0</td> <td data-bbox="1011 1465 1190 1486">No rate selected</td> </tr> <tr> <td data-bbox="824 1497 841 1518">0</td> <td data-bbox="889 1497 906 1518">0</td> <td data-bbox="954 1497 971 1518">1</td> <td data-bbox="1011 1497 1092 1518">1 MHz</td> </tr> <tr> <td data-bbox="824 1528 841 1549">0</td> <td data-bbox="889 1528 906 1549">1</td> <td data-bbox="954 1528 971 1549">0</td> <td data-bbox="1011 1528 1109 1549">100 kHz</td> </tr> <tr> <td data-bbox="824 1560 841 1581">0</td> <td data-bbox="889 1560 906 1581">1</td> <td data-bbox="954 1560 971 1581">1</td> <td data-bbox="1011 1560 1092 1581">10 kHz</td> </tr> <tr> <td data-bbox="824 1591 841 1612">1</td> <td data-bbox="889 1591 906 1612">0</td> <td data-bbox="954 1591 971 1612">0</td> <td data-bbox="1011 1591 1076 1612">1 kHz</td> </tr> <tr> <td data-bbox="824 1623 841 1644">1</td> <td data-bbox="889 1623 906 1644">0</td> <td data-bbox="954 1623 971 1644">1</td> <td data-bbox="1011 1623 1092 1644">100 Hz</td> </tr> <tr> <td data-bbox="824 1654 841 1675">1</td> <td data-bbox="889 1654 906 1675">1</td> <td data-bbox="954 1654 971 1675">0</td> <td data-bbox="1011 1654 1190 1675">Schmitt trigger 1</td> </tr> <tr> <td data-bbox="824 1686 841 1707">1</td> <td data-bbox="889 1686 906 1707">1</td> <td data-bbox="954 1686 971 1707">1</td> <td data-bbox="1011 1686 1255 1707">Line (50 Hz or 60 Hz)</td> </tr> </tbody> </table>	Bits			Function (Frequency)	03	02	01		0	0	0	No rate selected	0	0	1	1 MHz	0	1	0	100 kHz	0	1	1	10 kHz	1	0	0	1 kHz	1	0	1	100 Hz	1	1	0	Schmitt trigger 1	1	1	1	Line (50 Hz or 60 Hz)
Bits			Function (Frequency)																																							
03	02	01																																								
0	0	0	No rate selected																																							
0	0	1	1 MHz																																							
0	1	0	100 kHz																																							
0	1	1	10 kHz																																							
1	0	0	1 kHz																																							
1	0	1	100 Hz																																							
1	1	0	Schmitt trigger 1																																							
1	1	1	Line (50 Hz or 60 Hz)																																							
00 (Read/Write)	CLOCK ENABLE COUNTER	Enables counter to count at the specified rate. If no rate specified, clock will not count. Can be set by ST1 and is cleared by overflow in mode 1. When bit 00 is disqualified, loading of the buffer/preset also transfers data to clock counter.																																								

15	14	13	12	11	10	09-08	07	06	05-04	03-01	00
ST1 FLAG	ST1 INTERRUPT ENABLE	ST1 ENABLE	MAINT ST1	MAINT COUNT	MAINT ST2	MODE	MODE FLAG	MODE INT ENABLE	UNUSED	RATE	CLOCK ENABLE COUNTER

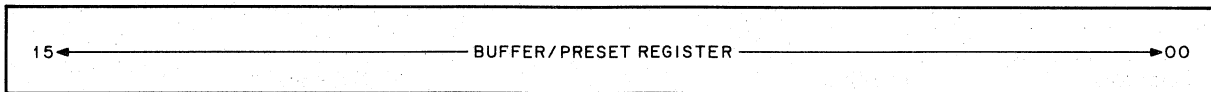
CP-0442

Figure 3-6 LPSKW Status Register

A more detailed discussion of the operations controlled by the status register is contained in Paragraph 3.2.1.

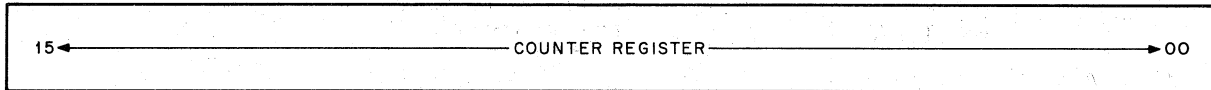
3.4.2 Buffer/Preset and Counter Registers

The buffer/preset register (Figure 3-7) is a 16-bit word-oriented register. Byte operations cannot be performed on it. The counter register (Figure 3-8) cannot be loaded directly from the processor, but must be loaded from the buffer/preset register. When the clock enable counter bit of the status register is cleared, loading the buffer/preset register also loads the counter register; when this bit is set, i.e., the clock is running, a transfer to the buffer/preset register loads only the buffer/preset register. Also, when the clock is running, the counter may be loaded from the buffer/preset or vice versa, depending upon the mode of operation.



CP-0440

Figure 3-7 LPSKW Buffer/Preset Register



CP-0441

Figure 3-8 LPSKW Counter Register

3.4.3 Register Addressing, Vector Addressing, and Priority

The clock has two register addresses (status and buffer/preset), one vector address, and one accompanying priority level. All of these are controlled by jumpers or jumper plugs on the LPS11-S M7015 Bus Control module. A further explanation of these functions is contained in Appendix A.

3.4.4 Program Examples

3.4.4.1 Program Example 1 – This program rings the TTY bell and performs A/D conversions on overflow; overflow occurs every two seconds.

Location	Instruction	Comment
INITIALIZE:	MOV 177470, @ BUFFER/PRESET MOV 000040, @ A/D STATUS REG MOV 000413, @ CLK STATUS REG	; SET TO DECIMAL - 200 ; ENABLE OVERFLOW TO START A/D CONVERSION ; START COUNT AT 100 Hz WITH MODE 1
LOOP:	TSTB @ CLK STATUS REG BPL LOOP	; CHECK FOR MODE FLAG ; NO, TRY AGAIN
PUNCH:	TSTB TPS BPL PUNCH MOV 207, TPB	; TEST FOR READY ON TTY PUNCH ; NO, TRY AGAIN ; RING THE BELL
CONV:	TSTB @ A/D STATUS REG BPL CONV BR LOOP	; CHECK FOR DONE FLAG ; NO, TRY AGAIN ; DO IT AGAIN

3.4.4.2 Program Example 2 – This program determines if an external pulse to Schmitt trigger 1 is drifting, occurring randomly, or is at a constant rate. An external oscillator is required.

Location	Instruction	Comment
START:	MOV 000000, BUF MOV 001505, CLK STAT	; CLEAR BUFFER/PRESET ; MODE 3, INTERRUPT ENABLE, 100K RATE, CLOCK ; START
FINISH:	WAIT BR START	; WAIT FOR ST PULSE ; TRY AGAIN
INTERRUPT:	MOV BUF, R0 RESET	; SET UP DATA DISPLAY ; CLEAR ALL AND DISPLAY CONTENTS OF R0. IF R0 ; CHANGES, THE INPUT IS DOING ONE OF THE ; FOLLOWING: A. DRIFTING B. OCCURRING RANDOMLY
	RTI	; RETURN FROM INTERRUPT TO FINISH INSTRUCTION

NOTE

This program does not apply to the PDP-11/05, which does not display R0. To use this program with the PDP-11/05, load the front panel LED as described in A/D converter programming example 4, Paragraph 2.4.5.4.

4.1 GENERAL DESCRIPTION

The LPSDR-A Digital I/O is a prewired option for the Lab Peripheral System that provides a means of transferring 16 parallel bits of data to and from an external device. Through this option, laboratory equipment such as recorders, oscillators, lamps, and general instrumentation can be conveniently controlled.

For output operations, data is loaded into the Output Register of the LPSDR-A under program control. Once data is in the Output Register, a signal (INTL NEW DATA READY) is sent to the external device indicating that data is on the lines. When the external device accepts (reads) the data, it will send a signal (EXT DATA ACCEPT) to the LPSDR-A which tells the Digital I/O that the device has the data. Now the LPSDR-A is ready for new data. The EXT DATA ACCEPT signal sets an output flag (located in the Status Register) and may cause an interrupt if the Output Interrupt Enable bit in the Status Register is set.

For input operations when data is available on the input lines, the flag is latched and, depending on the mode selected by a jumper and a switch, one of the following occurs:

1. The data bit may cause an interrupt,
2. A data word is transferred,
3. A combination of both an interrupt and a data transfer.

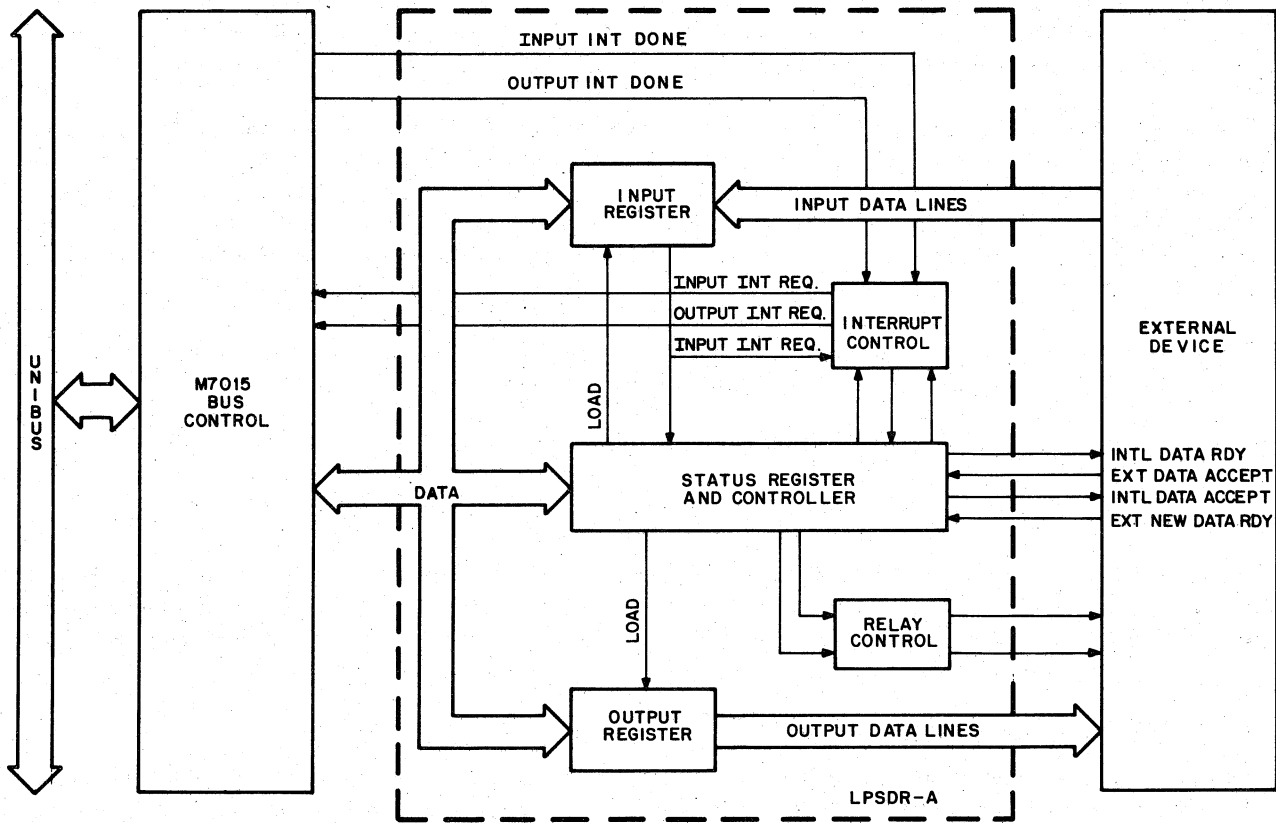
The LPSDR-A option is contained on a HEX board. Because this module derives its control and data signals from the internal bus of the LPS11-S System Bus Control module (M7015), it can only be used with the Lab Peripheral System. Input and Output connections for the LPSDR-A option are located on the rear connector panel, as separate 25-pin connectors. Relay connections are located on the front panel.

4.2 BLOCK DIAGRAM DESCRIPTION

Figure 4-1 is a block diagram of the LPSDR-A showing its relationship to the system. The main functional units of the LPSDR-A are a 16-bit buffered Output Register, a 16-bit Input Register, a Status Register, and the Interrupt Control logic.

4.2.1 Output Register

The Output Register may be loaded from or read into the bus control. When data is placed on the output register, the signal INTL NEW DATA READY (a negative going pulse of 1.0 μ s duration) is placed on the output lines and the 16 data lines. The external device receives the data and issues an EXT DATA ACCEPT pulse indicating that the output register may now be loaded with new data. Receipt of this signal sets the output flag of the Status Register and causes an interrupt if the output interrupt enable bit is set.



CP-0775

Figure 4-1 Digital I/O Block Diagram

4.2.2 Input Register

The Input Register is a Read-All/Write Zero register which may be manually or unconditionally cleared. A manual clear occurs whenever the user moves data to the Input Register from the processor. The bits loaded into the Input Register by the processor will clear the bits in that register. An unconditional clear occurs whenever the user writes the Input Register into itself or performs a RESET instruction.

NOTE

Bit Clear (BIC) and Clear (CLR) instructions will not work on the input register.

The Input Register is factory wired in the STIMULUS MODE of operation. (There are, however, two other modes – WORD TRANSFER and MIX – which will be discussed later.) Table 4-1 illustrates the jumper configurations for the three modes.

STIMULUS MODE – This mode is factory set with machine-insertable jumpers and switches SW15 through SW00 in ON position (Figure 4-2). If any of the machine-insertable jumpers have been removed, refer to Table 4-1 for correct jumper configuration – they must be reinstalled. In this mode of operation, the Falling Edge (+3 V to 0 V) of any or all bits entering the Input Register from an external device may do two things: 1) set a flip-flop, 2) the latched bits will cause an input interrupt if the input Interrupt Enable bit (06) in the Status Register is set. Thus the user may sample 16 different stimuli and interrupt on any combination of bits. Under this mode the most effective method of handling the data received would be to store the Input Register, then write the Input Register into itself. Any stimuli occurring after this function will be latched and the user need only set the input Interrupt Enable in the Status Register to repeat the process.

If interrupts are not used, the flag may be sampled periodically and when set, a stimulus has occurred. The flags must be cleared under Program Control.

WORD TRANSFER MODE – The jumper configuration for this mode is defined in Table 4-1. Under this mode, any 16-bit word can be transferred from an external device to the LPSDR-A input register. The external device sends a signal EXT NEW DATA READY (NEGATIVE GOING PULSE – 100 ns MINIMUM 1 μ s MAX) to the LPSDR-A controller to set an input flag and possibly cause an interrupt. (Interrupts will occur if the Input Interrupt Enable bit (06) in the Status Register is set.) The data must be held on the input lines until the LPSDR-A has read it or it will be lost. The time required to hold the data is dependent on the user program, but can be as short as 7.5 μ s. When the data is read by the PDP-11, an INTERNAL DATA ACCEPT PULSE is generated to notify the external device that the transfer is complete.

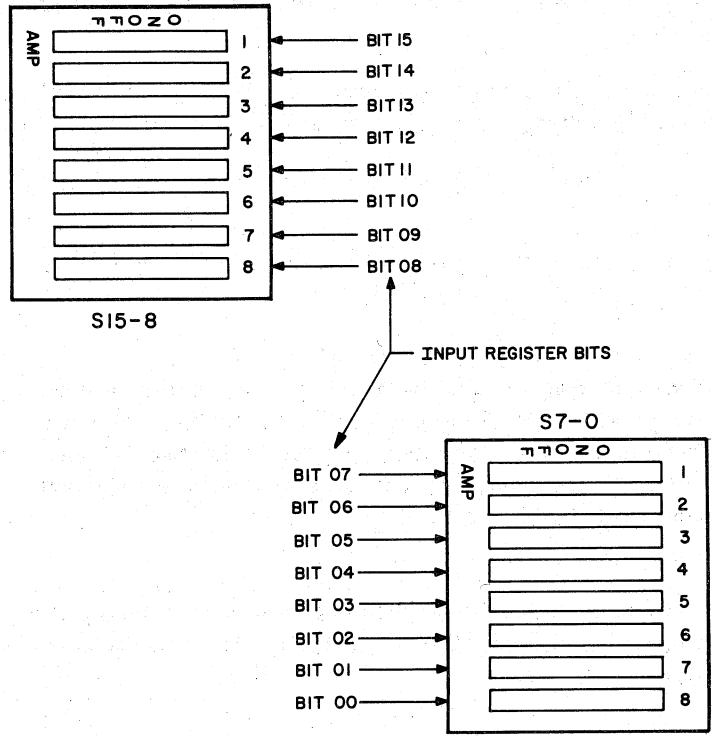
In this function the Input Interrupt Enable bit in the Status Register is cleared after the interrupt has occurred.

MIX MODE – The jumper configuration for this mode is a mixture of STIMULUS and WORD TRANSFER modes and is shown in Table 4-1. Any 16-bit data word may be transferred to the input register from an external device and depending on the jumper configuration, it can be treated as a combination of data words and interrupt bits.

Bits 15 and 14 of the Input Register may have inverted inputs (+3 V when true and 0 V when false) as defined by jumpers W16A and W16, and jumpers W17A and W17 respectively. Any mode may be used when these jumpers are installed. Production modules, however, are not normally configured for this operation.

**Table 4-1
Mode Select Jumper Configuration**

Input Bit	Installed Jumper	Removed Jumper	Stimulus	Mode Word Transfer	Mix
15	W15	W15A	X		Either but not both
	W15A	W15		X	
14	W14	W14A	X		
	W14A	W14		X	
13	W13	W13A	X		
	W13A	W13		X	
12	W12	W12A	X		
	W12A	W12		X	
11	W11	W11A	X		
	W11A	W11		X	
10	W10	W10A	X		
	W10A	W10		X	
09	W09	W09A	X		
	W09A	W09		X	
08	W08	W08A	X		
	W08A	W08		X	
07	W07	W07A	X		
	W07A	W07		X	
06	W06	W06A	X		
	W06A	W06		X	
05	W05	W05A	X		
	W05A	W05		X	
04	W04	W04A	X		
	W04A	W04		X	
03	W03	W03A	X		
	W03A	W03		X	
02	W02	W02A	X		
	W02A	W02		X	
01	W01	W01A	X		
	W01A	W01		X	
00	W00	W00A	X		Either but not both
	W00A	W00		X	



11-2409

Figure 4-2 Input Register Interrupt Switches

4.2.3 Interrupt Control

There are two interrupts associated with the LPSDR-A which, when enabled, indicate that the data has been accepted (output) or is being sent (input) by the external device. The priority of both interrupts is determined by two priority jumper plugs (PRIORITY 4) supplied with the M7015 Bus Control module (normally PRIORITY 4).

The Interrupt Enable bits are cleared by INITIALIZE and set under program control. The input Interrupt Enable in the Status Register is also cleared by the completion of the interrupt. When set, the output Interrupt Enable in the Status Register permits the associated request signal INTL NEW DATA READY to generate an interrupt. When set, the input Interrupt Enable bit in the Status Register allows the associated request signal EXT NEW DATA READY or data bits (when the associated switch is in the ON position) to generate an interrupt. Both Interrupt Enable Bits inhibit interrupts when cleared. Qualifying interrupts allows any stimulus to cause an interrupt and vector to the proper address (see Appendix B).

Two maintenance bits are associated with the interrupts. Bit 13 sets the Output Interrupt while bit 05 sets the Input Interrupt. These bits can be used by software to test the interrupts. INTERRUPT enable need not be set to generate interrupts with these bits.

4.2.4 Relays

The relay option consists of two normally-open relays, each capable of switching a 5 A resistive load at 115 Vac or a 2.5 A resistive load at 230 Vac.

CAUTION

When the relay is used with other than resistive loading, voltage spikes resulting from inductive loading can cause deterioration of the relay contacts, increase contact resistance, and reduce current carrying capabilities. Contact bounce may last as long as 20 ms

The two relays are controlled by bits (00 and 08) in the Status Register. Each relay tracks its respective register bit, thus, when the bit is set the contact is closed, and when the bit is clear the contacts are open. Binding posts on the front panel are used for the relays.

4.3 USER INTERFACING

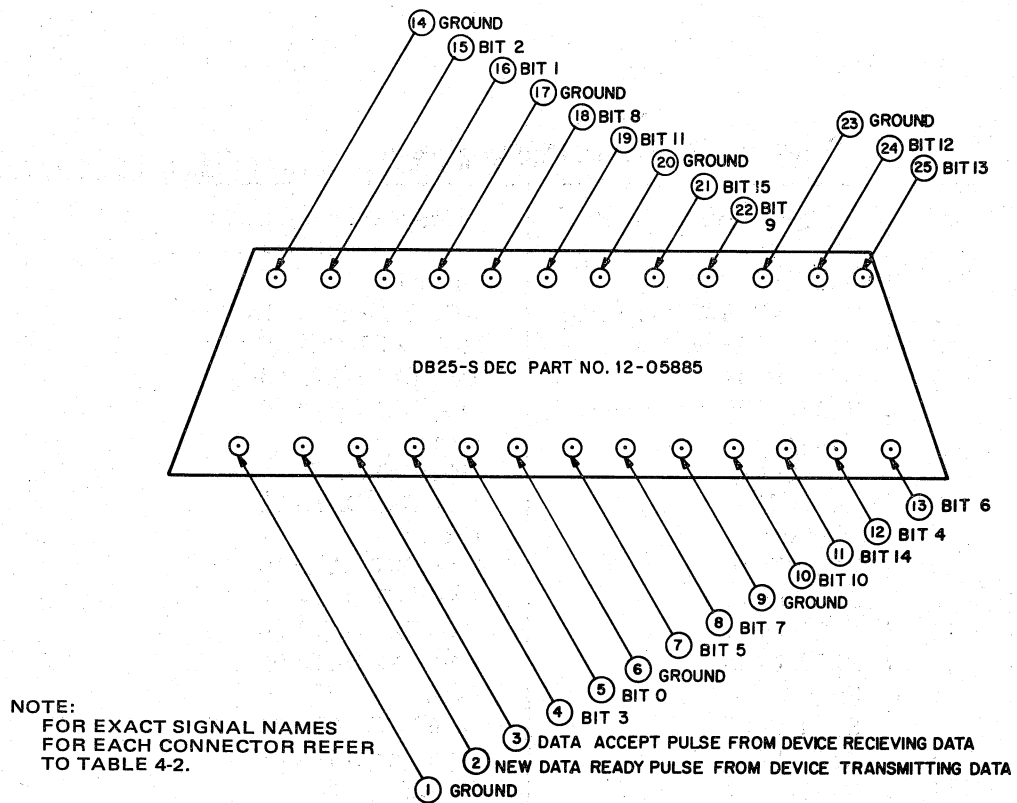
The LPSDR-A is interfaced to external equipment through two 25-pin connectors on the rear connector panel. Use mating connector CINCH DB-25P, DEC Part No. 12-05886, supplied with the option for interfacing. One connector contains input lines, the second is for output lines. Pin assignments for these connectors are listed in Table 4-2 and Figure 4-3.

All output signals from the LPSDR-A are ground (0.4 V max), for a logical one, and +3 V (+5 V max) for a logical zero. Each output is driven from an open collector gate (Figure 4-4) with a 470 Ω pull-up to +5 V and a 47 Ω fusible resistor (DEC Part No. 13-10881-2) in series. Thus each line can sink¹ 30 mA (in the one state) and source² 10 mA (in the zero state). The 47 Ω fusible resistor provides protection against an over-voltage of ± 20 Vdc. The resistor will open and protect the circuitry above 20 Vdc.

1. SINK is defined as current into the LPSDR-A.
2. SOURCE is defined as current supplied by the LPSDR-A.

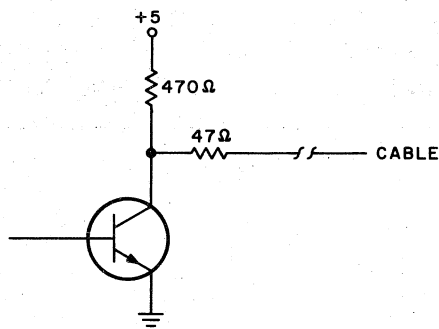
Table 4-2
LPSDR-A Input/Output Pin Assignments

Pin	Digital Input – RC2B	Digital Output – RC2A
1	Ground	Ground
2	D4-4 EXT NEW DATA RDY	RC2 INT NEW DATA RDY
3	D4-4 INT DATA ACC	RC2 EXT DATA ACC
4	RC2 E IN 03	D4-6 EXT DATA 03
5	RC2 E IN 00	D4-6 EXT DATA 00
6	Ground	Ground
7	RC2 E IN 05	D4-6 EXT DATA 05
8	RC2 E IN 07	D4-6 EXT DATA 07
9	Ground	Ground
10	RC2 E IN 10	D4-6 EXT DATA 10
11	RC2 E IN 14	D4-6 EXT DATA 14
12	RC2 E IN 04	D4-6 EXT DATA 04
13	RC2 E IN 06	D4-6 EXT DATA 06
14	Ground	Ground
15	RC2 E IN 02	D4-6 EXT DATA 02
16	RC2 E IN 01	D4-6 EXT DATA 01
17	Ground	Ground
18	RC2 E IN 08	D4-6 EXT DATA 08
19	RC2 E IN 11	D4-6 EXT DATA 11
20	Ground	Ground
21	RC2 E IN 15	D4-6 EXT DATA 15
22	RC2 E IN 09	D4-6 EXT DATA 09
23	Ground	Ground
24	RC2 E IN 12	D4-6 EXT DATA 12
25	RC2 E IN 13	D4-6 EXT DATA 13



11-2413

Figure 4-3 LPSDR-A Signal Labels for Input/Output Connectors



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Figure 4-4 Cable Driving Circuit

Timing for the output signal is shown in Figure 4-5. Cable driving capabilities are dependent on the characteristics of the particular cable being used and are of particular importance for the INTL NEW DATA READY and INTL NEW DATA ACCEPT signals which are factory set at 1 μ s. A method for calculating the maximum cable lengths for these signals is shown in Figure 4-6. Using this method and assuming that the external device can tolerate a maximum fall time of 200 ns, the maximum cable capacitance would be $(200 \times 10^{-9}) / (\frac{30 \text{ mA}}{5 \text{ V}})$ 1200 pF. If the cable has 50 pF/ft, this would result in a maximum length of 24 ft. The rise time of this signal would be $500 \times (122 \times 10^{-11})$ or approximately 600 ns. This and the 200 ns (TD) time would also have to be considered.

NOTE

Accuracy of calculations is $\pm 15\%$.

All input circuitry is TTL compatible. Ground (0.0–0.4 V max) represents a logical one and +3 V (+5 V max) represents a logical zero (exception to bits 15 and 14 of Input Register). The input circuit consists of a TTL gate preceded by a 3.3 K Ω resistor to +5 V, an 820 pF cap to ground, and a 47 Ω fusible resistor in series. The external device must be able to sink 3.5 mA. The 47 Ω fusible resistor provides protection against an overvoltage of ± 20 Vdc. Above 20 Vdc, the fusible resistor will open and protect the circuit. Timing for the input signal is illustrated in Figure 4-7.

Signals INTL NEW DATA READY and INTL NEW DATA ACCEPT may be polarity inverted by removing jumpers W18 and W19 respectively and installing jumpers W18A and W19A respectively. Figure 4-5 does not apply in this instance as the rise time becomes T2 and the fall time becomes T1.

These signals may also have the pulse width (TD) changed. Removal of associated resistors and installation of other resistors across split lugs H and J and E and F respectively will change the pulse width.

Table 4-3 lists possible pulse widths. Other pulse widths may be obtained using the following formulae:

$$T_w = (92.4) (R_t) + 0.6$$

$$T_w = \text{TIME IN ns}$$

$$R_t = \text{RESISTANCE IN K ohms}$$

NOTE

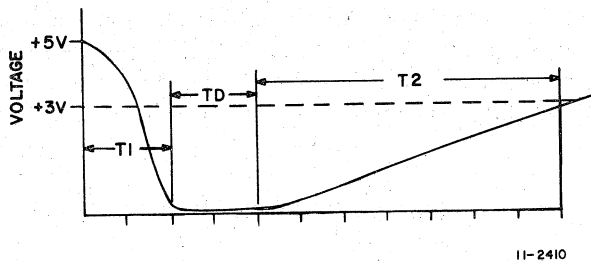
This formula only accurate to $\pm 15\%$

4.4 PROGRAMMING

4.4.1 Status Register (See Table 4-4)

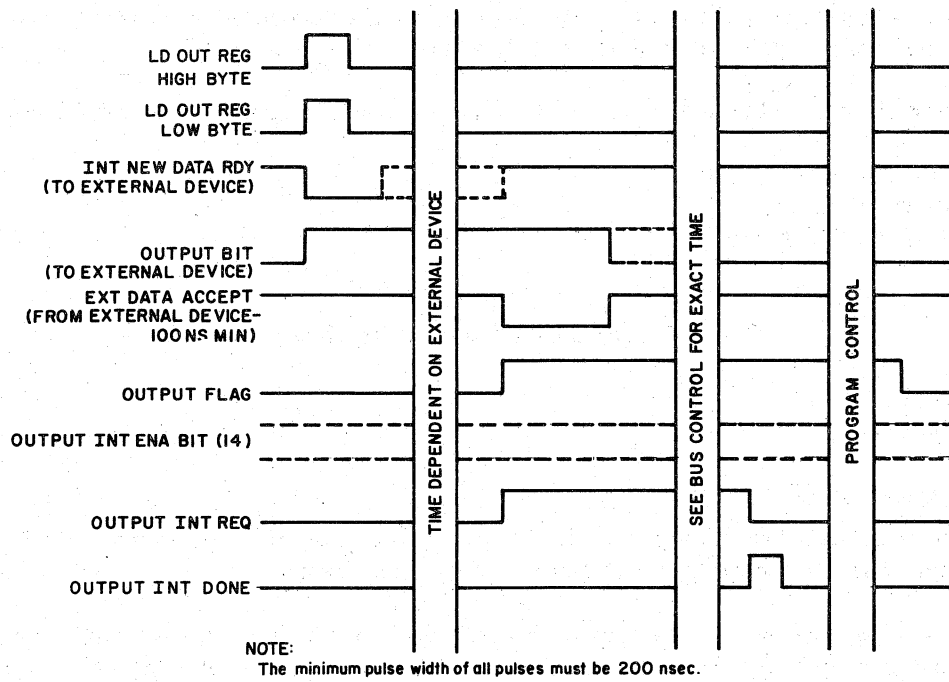
The Status Register contains two Interrupt Enable bits, two maintenance bits, two relay control bits, and two flags (output and input). Figure 4-8 shows the bit assignments of the status register.

The Status Register may have word or byte operations performed upon it. TST and TSTB instructions may be used to test the output and input flags. These flags must be cleared by the user when not in the interrupt mode (bit 06 is set in interrupt mode). Byte operations and increments may be used to control the relay bits. The maintenance bits are write-only bits and, like the unused bits, will read back as zeros.



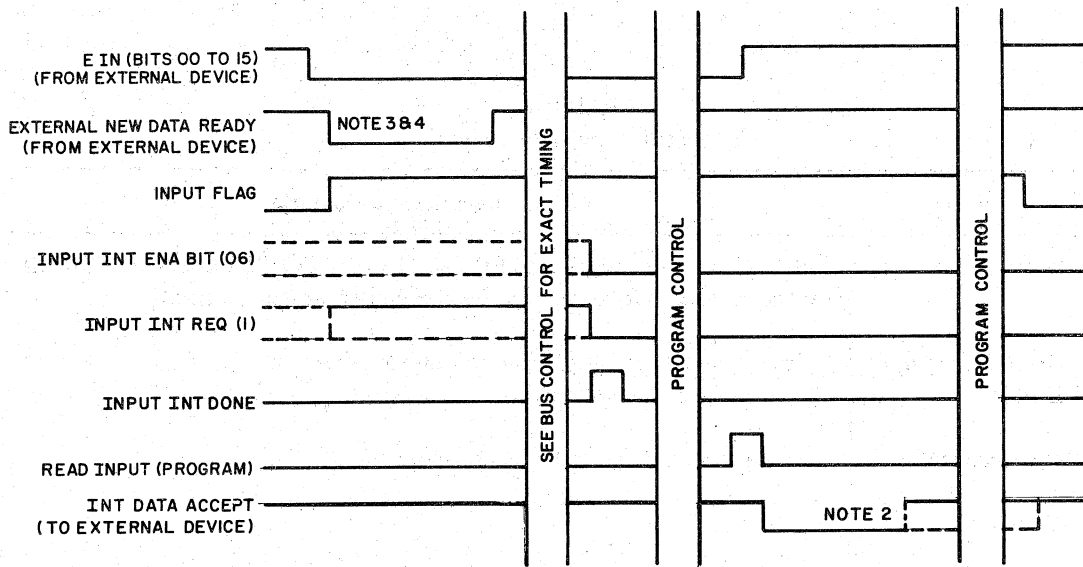
11-2410

Figure 4-5 LPSDR-A Output Timing Diagram



11-2411

Figure 4-6 Time Voltage vs Time Chart for Computing Signal Rise Time



- NOTES:
1. Dependent on user program.
 2. Time dependent on user selection of resistance, factory setting is approximately 1 micro sec.
 3. Maximum is 1 μ sec and minimum is 100ns.
 4. Data must available for a minimum of 75 ns before the new data ready pulse is generated.

11-2412

Figure 4-7 Input Timing Diagram

Table 4-3
Pulse Width Computations

Resistance (K Ω)	Pulse Width (ns)
5	500
10	1000
20	1900
50	4700

The minimum pulse width of all pulses must be 200 ns.

**Table 4-4
Status Register Operation**

Bit	Name	Meaning and Operation
15	Output Flag	Sets when device sends EXTERNAL DATA ACCEPT pulse, signifying that data is taken from output register. Cleared under program control.
14	Output Interrupt Enable	Permits setting of output flag to cause an interrupt.
13	Maintenance Bit 2	Sets output flag for maintenance purposes.
12-9	Unused	
8	Relay 2	Setting or clearing causes Relay 2 to close or open, respectively.
7	Input Flag	Sets when device sends EXTERNAL NEW DATA READY signal, signifying that data has been placed in input register. Cleared under program control.
6	Input Interrupt Enable	Permits setting of input flag to cause interrupt. Cleared automatically after each interrupt or under program control.
5	Maintenance Bit 1	Sets input flag for maintenance purposes.
4-1	Unused	
0	Relay 1	Setting or clearing causes Relay 1 to close or open, respectively.

15	14	13	12-09	08	07	06	05	04-01	00
OUTPUT FLAG	OUTPUT INTERRUPT ENABLE	MAINT BIT 2	UNUSED	RELAY #2	INPUT FLAG	INPUT INTERRUPT ENABLE	MAINT BIT 1	UNUSED	RELAY #1

CP-0443

Figure 4-8 Status Register

4.4.2 Data Registers

The Output Register is a byte operable Read/Write register 16 bits long. It is loaded under Program Control. Loading the output may be byte oriented.

The Input Register may be cleared by byte operations. It may also be bit cleared by loading the bit to be cleared into the Input Register. A RESET instruction clears the entire register. In Stimulus Mode, any bit entering the Input Register will cause an interrupt when the Interrupt Enable bit is set and will set the INPUT FLAG. In this mode the best method of clearing a stimulus is to MOV the DATA READ into the Input Register, thereby ensuring that any bits entering after this function will not be lost. In Word Transfer mode the Input Register transfers words from an external device to the PDP-11.

4.4.3 Programming Examples

Program Example 1 – Output Data

Location	Instruction	Comment
GO:	CLR STATUS REG MOV#A, OUTPUT REG	;Clear the status Reg. ;Load data (data is on the lines, and a pulse has been generated).
LOOP:	TST STATUS REG BPL LOOP HALT BR GO	;Check to see if the external device received data ;No try again ;Transfer complete ;Do again

Program Example 2 – Turn on Both Relays

Location	Instruction	Comment
GO:	MOV#0401, STATUS REG CLR R0	;Turn relays on
LOOP 1:	INC R0 BNE LOOP 1 CLR STATUS REG	;Do 64,000 times (300 MS) ;Turn relays off
LOOP 2:	INC R0 BNE LOOP 2 BR GO	;Do 64,000 times ;Start all over again

The relays should turn on and off approximately 10 times/6 seconds.

Program Example 3 – Input Data: STIMULUS MODE

Location	Instruction	Comment
INTERRUPT:	MOV INPUT,R0 MOV R0,INPUT MOV #100,STATUS RTI	;Save stimulus bits ;Clear stimulus bits from input ;Set interrupt enable ;Return to main program until another stimulus occurs

Program Example 4 – Input Data: WORD TRANSFER MODE

Location	Instruction	Comment
LOOP:	TSTB STATUS REG BPL LOOP MOV INPUT, R0 CLR STATUS REG HALT BR LOOP	;Check to see if device has sent data ready pulse ;Not yet ;Read data ;Clear done flag ;Transfer complete ;Do it again

CHAPTER 5

DISPLAY CONTROL

5.1 GENERAL DESCRIPTION

The LPSVC Display Control is a prewired option for the Lab Peripheral System that permits the user to display data in the form of a $4096_{10} \times 4096_{10}$ dot array. Under program control, a bright dot may be produced at any point in this array, or a series of these dots may be programmed to produce graphical output.

The LPSVC may output to either an X/Y recorder or a display unit. Normal configuration calls for its use with either a VR14 display unit or a VR20 color display unit; however, the LPSVC is capable of operating with other equipment, such as the Tektronix RM503, 602, and 604 scopes and the 611 and 613 storage scopes.

Output operations are accomplished by loading the status register and the X or Y register. Through use of status register bits, the user can intensify the contents of X or Y registers, provide delays necessary for some scope applications, change scope color or channel, indicate when a scope is ready for intensification, provide erase, write-thru, and non-store control functions for storage scope applications, and enable interrupts.

The LPSVC offers four program-controlled modes in which the scope can intensify a point; it also has the capability of changing X or Y register values by a small increment without a long scope settling time, which is a useful feature in developing a software character generator. Jumpers give the LPSVC additional flexibility by enabling the user to select the desired outputs, output polarities, output clamping, delays, and intensification pulses.

The LPSVC option for the Lab Peripheral System consists of an M7019 Scope Control module and an A625 Digital-to-Analog Converter module. These modules must be used with the M7015 Bus Control.

5.2 BLOCK DIAGRAM DESCRIPTION

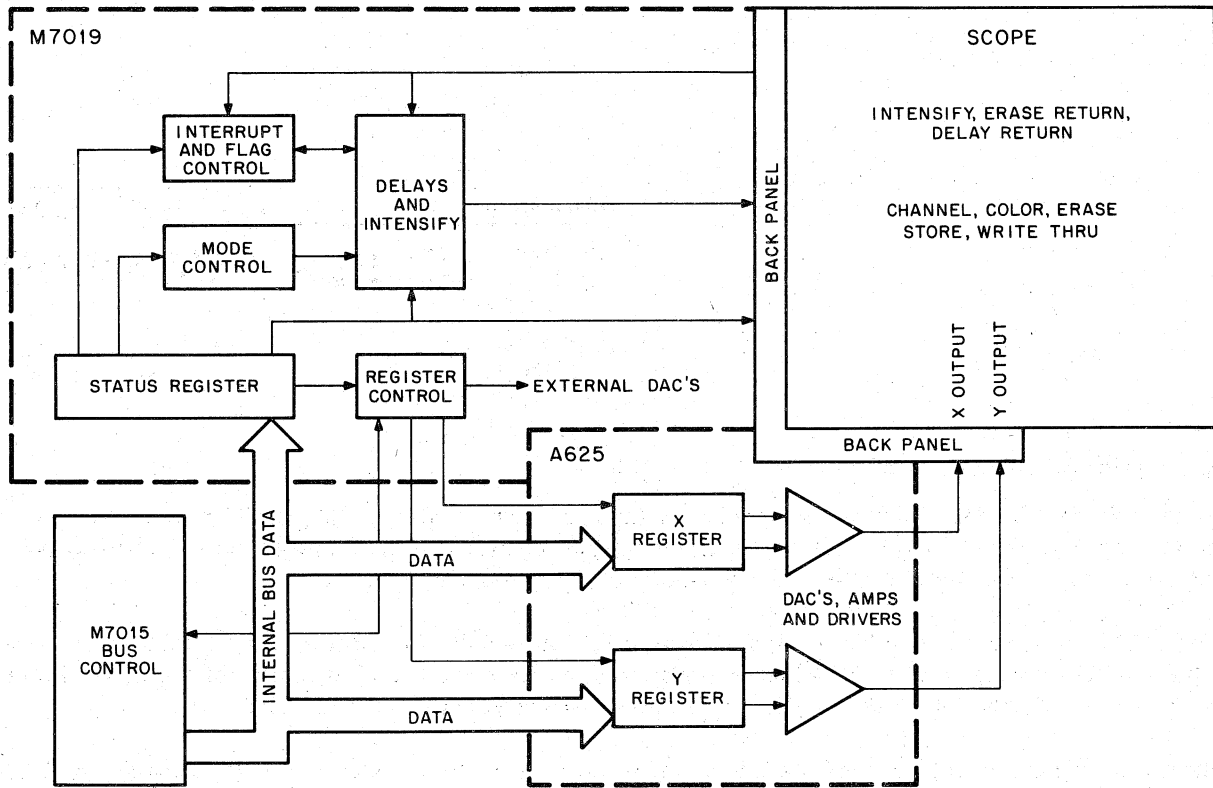
Figure 5-1 is a block diagram of the LPSVC option, indicating its relationship to the Lab Peripheral System. The principal functional units of the LPSVC are the status register, the register control, the intensify control, and the D/A control.

5.2.1 Status Register

The status register is a read/write byte-operable register. It controls all operations of the LPSVC, and permits the user to select or change modes, color, intensification, delays, and interrupts. The bits governing channel and color are principally intended for use with the VR14 and VR20 scopes, but may also be used to provide a "pen up/pen down" capability with an X/Y recorder.

The status register mode control offers the user four distinct modes of operation, making it possible to intensify upon command or to intensify upon loading X and Y registers. Flags and enables let the user interrupt or terminate operations. (This interrupt has a vector address as defined in Appendix B.)

For storage scope applications, the status register can control the write-thru, erase, and storage modes of operation.



CP-0340

Figure 5-1 LPSVC Block Diagram

5.2.2 Digital-to-Analog Control

The digital-to-analog control decodes status register information and provides the necessary delayed pulses to the intensification control, which, via jumpers, emits an intensify pulse of proper duration and size.

The D/A converter contains the X and Y registers which, when loaded, are converted to analog voltages (jumper selectable gain and polarity). D/A converter outputs are capable of driving up to 100 ft of cable.

5.3 USER INTERFACING

The LPSVC is interfaced through a back panel connector labeled DISPLAY. Pin assignments for this 25-pin connector are listed in Table 5-1. By adding or deleting jumpers, the user can control the delay and/or intensification of the output. Table 5-2 lists jumper configurations for some available scopes. Table 5-3 lists scope specifications.

Table 5-1
Pin Assignments for Back Panel Display Connector (RC3)

Pin	Signal Name
1	Ground
2	Ground
3	Ground
4	D10-2 WRITE THRU
5	RC3 ERASE RETURN

Table 5-1 (Cont)
Pin Assignments for Back Panel Display Connector (RC3)

Pin	Signal Name
6	Ground
7	D10-2 ERASE L
8	D10-2 NON-STORE L
9	Ground
10	D10-2 RED Δ L
11	D10-2 CHANNEL 2 L
12	D10-2 INTENSE
13	Ground
14	Ground
15	Ground
16	RC3 DELAY RETURN L
17	Ground
18	Ground
19	Ground
20	Ground
21	D11-2 Y OUTPUT
22	VC Δ AN GND
23	Ground
24	D11-2 X OUTPUT
25	VC Δ AN GND

D/A converter output may also be adjusted for gain, as shown in Table 5-4, or for polarity, as shown in Table 5-5. Specifications for the D/A converter are shown in Table 5-6.

Manufacturer's manuals for the scope or plotter being used should be checked to obtain accurate input specification. Any modifications involving pre-existing circuits should be discussed thoroughly with a DEC Field Service Representative before they are implemented.

Table 5-2
Jumper Arrangements for LPSVC Option

		Digital			Tektronix						
		Standard Module	VR14	VR20	601	602	603	604	611	613	503
*Recommended		NA	NA	NA	5	5	5	5	5	5	
Attenuation	D-W1	X	X	X							X
Factor	W2				X		X		X	X	
	A-W3	X	X	X							
M7019	B				X	X	X	X	X	X	
Jumper	C										X
Arrangement	E				X	X	X	X	X	X	X
	F-W4	X	X	X							
	G-W5	X	X	X		X		X			
	H				X		X		X	X	X

Table 5-2 (Cont)
Jumper Arrangements for LPSVC Option

		Digital			Tektronix						
		Standard Module	VR14	VR20	601	602	603	604	611	613	503
A625 Jumper Arrangement	W1										
	W2	X	X	X	X	X	X	X	X	X	X
	W3	X	X	X	X	X	X	X	X	X	X
	W4	X	X	X					X	X	X
	W5				X	X	X	X			
	W6	X	X	X						X	X
	W7										
	W8	X	X	X	X	X	X	X	X	X	X
	W9	X	X	X	X	X	X	X	X	X	X
	W10	X	X	X					X	X	X
	W11				X	X	X	X			
	W12	X	X	X					X	X	X

X denotes a jumper placement on the M7019 and A625 modules.

*To set up the attenuation factor, refer to associated Tektronix manual.

Table 5-3
Scope Specifications

Scope Type	Installed Jumpers (M7019)	Settling Times (M7019)	M7019 Intensification Time	Intensity Pulse Voltage
RM503	H, W1, C, E	21 μ s	5 μ s	+4V \rightarrow -12V
601, 602 603, 604	E, B, G	6 μ s	1 μ s	+1V \rightarrow -1/2V
611, 613	E, B, H, W2	80 μ s	1 or 5 μ s	+1V \rightarrow -1/2V
VR14	W1, W2, G, F	21 μ s	1 μ s	+4V \rightarrow -2V
VR20	W1, W2, G, F	21/15 μ s	1 or 5 μ s	+4V \rightarrow -2V

*All times can be \pm 10% of the nominal values.

Table 5-4
Gain Selection

Gain	Jumpers		Bipolar Output	Unipolar Output
	X	Y		
20	W8	W2	\pm 10V	DO NOT USE
10	W8, W9	W2, W3	\pm 5V	0 \rightarrow 10V
1	W7	W1	\pm 1/2V	0 \rightarrow 1V

Table 5-5
Polarity Selection
 (Used with gains listed in Table 5-4)

Polarity of Output (X or Y)	Jumpers	
	X	Y
Unipolar	W11	W5
Bipolar	W10	W4

Table 5-6
D/A Converter Specifications
 (Assuming Setup for VR14 or VR20)

Specification	Description
Output voltage	±5V
Resolution	1 part in 4096 (0.025% full scale)
Accuracy absolute	0.1%
Slewing speed	10V/0.5 μs
Settling time to 0.03%	4 μs
Drive capability	300 ft at 50 pF/ft cable
Offset adjustment range	200 mV
Gain adjustment range	20 mV
Output specifications: Z axis	The Z axis polarity is controlled by a jumper on the M7019 module. The pulse will be either positive or negative.
Pulse Width	1 μs (green) or 6 μs (red)
Pulse Size	+4V to -2V
Rise Time	100 ns
Fall Time	200 ns

NOTE

If the gain of the D/A converter is changed to any value other than 10, the above specifications do not apply.

5.3.1 Intensification

Pulse width, polarity, and voltage are prime considerations in intensification. The LPS11 can supply a 1 μ s or 6 μ s pulse width, as indicated by Table 5-7. Pulse widths other than those specified should have a 200 ns rise time to avoid reflection on long cables. Signal polarity may be changed via jumpers E and F on the M7019 module.

NOTE

Improper value of the intensity polarity will result in signal blanking at the wrong time and retraces will be seen.

Intensity pulse voltage is variable as shown in Table 5-7.

NOTE

Changing the voltage may result in an increase in rise and fall times.

Table 5-7
Intensity Pulse Voltage

Scope	Output Swing	Pulse Polarity	Polarity Jumper	Settling Time	Output Pulse Width	Driver Jumpers
VR14 VR20 Green Red	4 1/2V → -1 1/4V	Neg	F	21 μ s 21 μ s 15 μ s	1 μ s 1 μ s 6 μ s	W1-D & W3-A
TEK 601-604 TEK 611, 613	-1/2V → 1 1/4V	Pos	E	21 μ s	1 μ s 6 μ s	B
RM503	-11V → 4V					W1-D & C

5.3.2 X and Y Inputs

The voltages generated by the X and Y outputs are listed in Table 5-7, and should not be modified. The user must have external attenuators or an internal scope gain adjustment, and should be aware that many scopes call for only positive voltage swings. However, an offset position can usually be adjusted to correct input polarity problems.

Scope settling time may vary from 1 μ s to 100 μ s. The LPSVC is designed for use with the VR14, VR20, 503, 602, 604, 611, and 613 scopes. If any other scope is used, the user must determine whether the LPSVC delays are adequate for that scope. Longer delays may be achieved by using the switching time of the color circuitry. Switching from green to red causes a 300 μ s delay; switching from red to green causes a 1600 μ s delay. For slow scopes, software delays may be used.

5.3.3 Drive

Careful selection of cabling is essential. The X and Y outputs, color, and channel are capable of driving loads greater than 1K in parallel with no greater than 5000 pF of capacitance, i.e., 100 ft of cable at 50 pF/ft.

5.3.4 Ground Logic

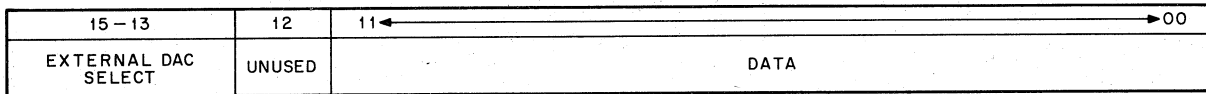
The analog signals that are present at the output of the X and Y axes are analog voltages, analog grounds, and logic grounds (shield). When differential inputs are used, the analog voltage and analog ground are required. When single-ended inputs are used, only the analog voltage and logic ground are required. At no time should the analog ground be connected to the system ground.

5.4 PROGRAMMING

Programming is accomplished through the status register and the X and Y registers. One hardware interrupt vector is associated with the LPSVC, as defined in Appendix B.

5.4.1 X and Y Registers

The X and Y registers are read/write registers, but are not byte operable. Bits 12–15 of those registers govern the selection of external D/A converters (Figure 5-2); the method of decoding is shown in Table 5-8.



CP-0460

Figure 5-2 External D/A Register

Table 5-8
External DAC Register

15	14	13	DAC Pointer
0	0	0	DAC 0
0	0	1	DAC 1
0	1	0	DAC 2
0	1	1	DAC 3
1	0	0	DAC 4
1	0	1	DAC 5
1	1	0	DAC 6
1	1	1	DAC 7

5.4.2 Status Register

The status register is a read/write register, and is also byte operable. It is shown in Figure 5-3 and described in Table 5-9.

15—13	12	11	10	09	08	07	06	05	04	03—02	01	00
UNUSED	ERASE	WRITE THRU	STORE	CHANNEL	COLOR	READY FLAG	INT ENABLE	UNUSED	EXT DELAY	MODE	FAST INTENSIFY	INTENSIFY

CP-0349

Figure 5-3 Status Register

**Table 5-9
Status Register**

Bit	Name	Meaning & Operation
Bit 15–13	Unused	Always reads 0.
Bit 12	Erase (write only)	Bit 12 = 1, erase data in the Store scope (Write only).
Bit 11	Write thru (read/write)	Bit 11 = 1, an intensified point will not be stored even though the user is in the store operation.
Bit 10	Store (read/write)	Bit 10 = 1, all intensified points will be stored.
Bit 9	Channel (read/write)	Bit 9 = 0, channel 1 Bit 9 = 1, channel 2
Bit 8	Color (read/write)	Bit 8 = 0, Green Mode Bit 8 = 1, Red Mode
Bit 7	Ready Flag (read only)	Bit 7 = 0, the scope is not ready, do not load or intensify points. Bit 7 = 1, the scope is ready.
Bit 6	Interrupt Enable (read/write)	Bit 6 = 1 and bit 7 in transition from a 0 to a 1 will cause an interrupt.
Bit 5	Unused	Always reads 0.
Bit 4	EXT DELAY (read/write)	When bit 4 = 1, all internal timing stops. When the external device (scope or XY recorder) returns a Done signal, an intensify pulse will be generated and the ready flag will be set.
Bit 3, 2	Mode (read/write) 00 Normal 01 X Mode 10 Y Mode 11 XY Mode	Intensification with bit 0 only. Intensification on loading X register. Intensification on loading Y register. Intensification on loading X or Y.
Bit 01	Fast Intensify Enable (read/write)	Bit 1 = 0, all scope settling delays are as defined for each scope. Bit 1 = 1, all scope settling delays are 3 μ s.
Bit 00	Intensify (write only)	Bit 0 = 1, any coordinate in X and Y register will be intensified (Write only).

When the LPSVC is used with a scope, a scope grid coordinate scheme similar to that shown in Figure 5-4 is used. The control display takes the form of a $4096_{10} \times 4096_{10}$ dot array. Under program control, a bright spot can be momentarily produced at any point in this array.

Any point in the array can be intensified by status register bit 00 (INTENSIFY), bits 02 and 03 when loading X or Y values (MODES 0–3), or with bit 01 (FAST INTENSIFY) enabled.

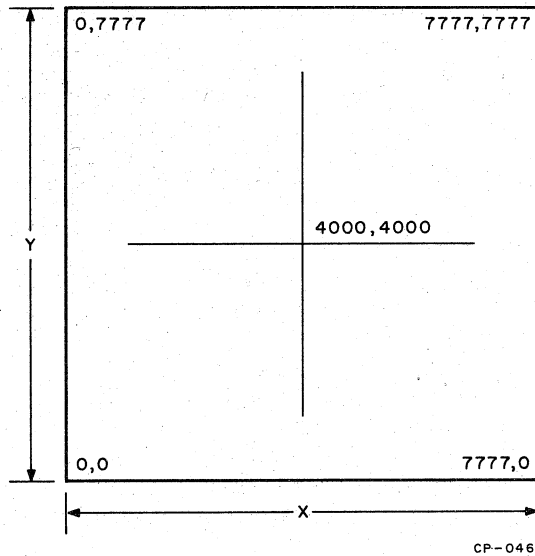


Figure 5-4 Scope Grid Coordinate (X, Y)

Bit 00 allows a point to be intensified under normal program operation and jumper configuration (Tables 5-3 and 5-4). Bit 01 should only be used when an incremental type display (e.g., character generator, graphic display, etc.) is used. Under no circumstances should the user attempt to set both INTENSIFY and FAST INTENSIFY bits simultaneously, or retrace will result.

Modes 0–3 may be used with either bit 00 or bit 01. Mode 0 allows the user to control when an intensification will occur. Mode 1 intensifies a point upon loading the X register; mode 2 intensifies a point upon loading the Y register. Mode 3 intensifies upon loading either the X or Y register.

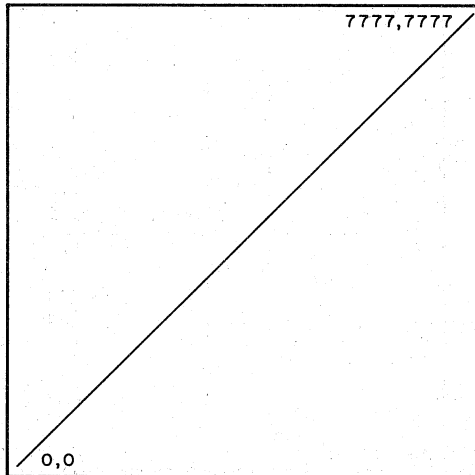
Interrupts occur when bit 06 (interrupt enable) is set and bit 7 (ready flag) sets. Bit 07 sets when an intensify pulse occurs, when an erase operation is complete, or when either red or green delays have been completed.

5.4.3 Programming Examples

Programs 1 and 2 illustrate correct usage of the modes, intensify, color, and channel functions. Program 3 uses INTENSIFY or FAST INTENSIFY to display two dots at opposite ends of the screen. The user can select INTENSIFY (when bit 07 = 0) or FAST INTENSIFY (when bit 07 = 1). Note that when FAST INTENSIFY is used, a blur occurs instead of a dot. FAST INTENSIFY should not be used when more than 10 points exists between two succeeding dots in a display.

5.4.3.1 Program Example 1 (Figure 5-5)

Location	Instruction	Comment
GO:	MOV 000004, STATUS REG	; MODE 1, COLOR GREEN ; CHANNEL 1, NO ; INTERRUPT.
	INC Y REG	; LOAD Y REGISTER.
	INC X REG	; LOAD X REGISTER.
LOOP:	TSTB STATUS REG	; CHECK IF DONE.
	BPL LOOP	; NO, TRY AGAIN.
	BR GO	; LOAD THE SECOND ; COORDINATE.

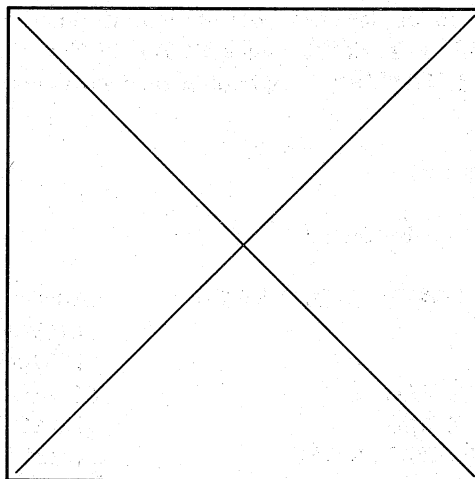


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Figure 5-5 Program 1 Display

5.4.3.2 Program Example 2 (Figure 5-6)

Location	Instruction	Comment
ST:	MOV 00416, STATUS REG	; MODE 3, COLOR RED, ; CHANNEL 1, NO ; INTERRUPT, FAST ; INTENSIFY.
	INC X REG	; LOAD X.
	INC Y REG	; LOAD Y.
LOOP 1:	TSTB STATUS REG	; CHECK IF DONE.
	BPL LOOP 1	; NO, TRY AGAIN.
	MOV 00015, STATUS REG	; SAME AS ABOVE.
	DEC X	; LOAD X.
	INC Y	; LOAD Y.
LOOP 2:	TSTB STATUS REG	; CHECK IF DONE.
	BPL LOOP 2	; NO, TRY AGAIN.
	BR ST	; DO IT ALL AGAIN.

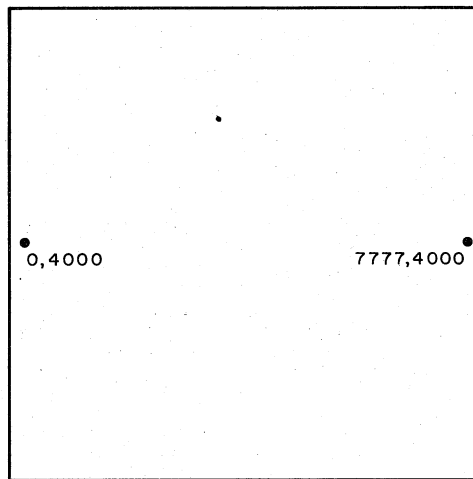


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Figure 5-6 Program 2 Display

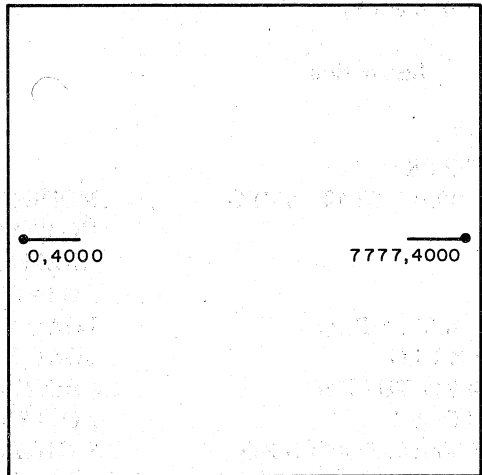
5.4.3.3 Program Example 3 (Figures 5-7 and 5-8)

Location	Instruction	Comment
ST:	RESET	
	BR CHECK	
ST1:	MOV 00015, STATUS REG	; MODE 3, NORMAL ; INTENSIFY, COLOR ; GREEN, CHANNEL 1, ; NO INTERRUPT.
	MOV 4000, Y REG	; LOAD Y REG.
	COM X REG	; LOAD X REG.
LOOP 1:	TSTB STATUS REG	; CHECK FOR DONE.
	BPL LOOP 1	; NO, TRY AGAIN.
	MOV 00015, STATUS REG	; SAME AS ABOVE.
	COM X REGISTER	; LOAD X REG.
LOOP 2:	TSTB STATUS REG	; CHECK FOR DONE.
	BPL LOOP 2	; NO, TRY AGAIN.
	BR CHECK	; CHECK SWITCHES.
ST2:	MOV 00016, STATUS REG	; MODE 3, FAST INTENSIFY, ; GREEN COLOR, CHANNEL ; 1, NO INTERRUPT
	COM X REG	; LOAD X.
	MOV 00016, STATUS REG	; SAME AS ABOVE.
	COM X REG	; LOAD X
	BR CHECK	; CHECK SWITCHES.
CHECK:	MOV@SWITCH REGISTER, R0	; READ SWITCHES.
	TSTB R0	; CHECK FOR BIT 07 SET ; OR CLEAR.
	BPL ST	; NORMAL INTENSIFY ; (CLEAR).
	BM1 ST2	; FAST INTENSIFY (SET).



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Figure 5-7 Normal Intensify – Wait for Done Flag



CP-0465

Figure 5-8 Fast Intensify – Disregard Done Flag

APPENDIX A

FLOATING VECTORS FOR THE PDP-11

Interrupt vectors for the Lab Peripheral System must be assigned according to the floating vector convention used for all communications devices interfacing with the PDP-11. These vector addresses are assigned in order from 300 to 777, according to a priority system that ranks the devices in a particular PDP-11 system.

Table A-1 shows the assigned sequences. Note that the first vector address (300) is assigned to the first DC11 in the system. If another DC11 is used, it is assigned vector address 310, etc. When vector addresses have been assigned for all the DC11s (up to a maximum of 32), they are then assigned consecutively to each unit of the next highest-ranked device (KL11 or DP11 or DM11A, etc.), then to the third-ranked device, and so on in accordance with the priority rating in Table A-1.

The vector assignment sequence will normally be the same sequence as that in which the devices enter production. A new option's vector will never be inserted before a device that is in production.

Table A-1
Priority Ranking for Floating Vectors
(Starting at 300 and proceeding upward)

Rank	Device	Vector Size	Max No.	BR
1	DC11	10	32	5
2	KL11	10	16	4
3	DP11	10	32	5
4	DM11A	10	16	5
5	DN11	4	16	4
6	DM11BB	4	16	4
7	DR11A	10*	32	5
8	DR11C (Start after DR11A)	10*	32	5
9	PA611 Readers	4*	16	4
10	PA611 Punches	4*	16	4
11	DT11	10*	8	7
12	DX11	10*	4	4
13	LPS11	30*	1	4, 5, 6

*The first vector for the first device of this type must always be on a 10_8 boundary.

APPENDIX B PROGRAMMER'S REFERENCE

STANDARD* REGISTER ADDRESSES

Option	Register	Address
LPSAD-12	Status	770400
LPSAD-12	Buffer/Led	770402
LPSKW	Status	770404
LPSKW	Buffer/Preset	770406
LPSDR	Status	770410
LPSDR	Input	770412
LPSDR	Output	770414
LPSVC	Status	770416
LPSVC	X – D/A	770420
LPSVC	Y – D/A	770422
LPSVC	EXT D/A	770424
Unused	–	770426
Unused	–	770430
Unused	–	770432
Unused	–	770434
LPSAD-NP	DMA	770436

*The register address is jumper selectable in increments of 40 locations, however the relative location of the various registers will remain the same.

VECTOR ADDRESSES** And PRIORITY LEVELS

Option	Address	BR Level
LPSAD-12	300	6
LPSKW	304	5
LPSDR (IN)	310	4
LPSDR (OUT)	314	4
LPSVC	320	4
UNDEFINED	324	4
LPSAD-NP	300	6

**The vector address field is jumper selectable and will be assigned in conjunction with existing option. However, the relative positions of the option will remain constant once the initial location is determined.

LPSAD-12 STATUS REGISTER

15															0
----	--	--	--	--	--	--	--	--	--	--	--	--	--	--	---

Bit	Function
15	Error Flag
14	Dual Mode Enable (LPSSH)
13-8	Multiplexer Channel
7	A/D Done Flag
6	Interrupt Enable
5	Clock Overflow Enable
4	Schmitt Trigger Enable
3	Burst Mode (LPSAD-NP)
2,1	DMA Address Pointer (LPSAD-NP) *
0	A/D Start

*DMA Address Pointer

Bit 2	Bit 1	Function
0	0	Unused
0	1	DMA Status Register
1	0	DMA Word Count Register
1	1	DMA Current Address Register

LPSAD-12 BUFFER/LED REGISTER

A/D Buffer (Read only)

15			12	11										0
Unused				A/D Data										

Led Register – Numeric Display (Write only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unused			Digit Address			Unused			Decimal point	Display					

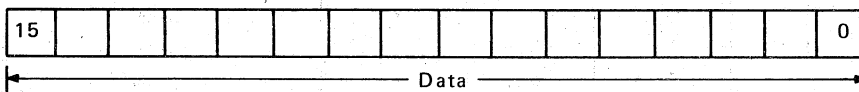
Digit Address

Bit 10	Bit 9	Bit 8	Digit
0	0	0	LED 1 (Right most)
0	0	1	LED 2
0	1	0	LED 3
0	1	1	LED 4
1	0	0	LED 5
1	0	1	LED 6 (Left most)
1	1	0	Unused
1	1	1	Unused

Rate

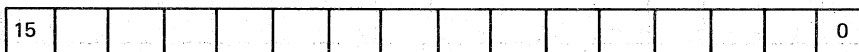
Bit 3	Bit 2	Bit 1	Base Frequency
0	0	0	Stop
0	0	1	1 MHz
0	1	0	100 kHz
0	1	1	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
1	1	0	External (Schmitt Trigger #1)
1	1	1	Line

LPSKW BUFFER/PRESET REGISTER



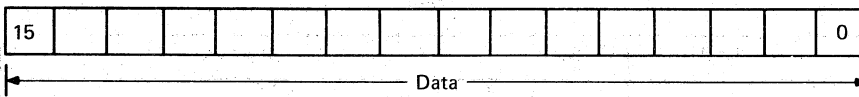
No byte operation is permitted. Data will simultaneously be loaded to the clock counter when Bit 0 of the status register is disqualified.

LPSDR STATUS REGISTER



Bit	Function
15	Output Flag
14	Output Interrupt Enable
13	Maintenance Output Interrupt
12-9	Unused
8	Relay #2
7	Input Flag
6	Input Interrupt Enable
5	Maintenance Input Interrupt
4-2	Unused
1	Internal Load
0	Relay #1

LPSDR INPUT and OUTPUT REGISTERS



Input – Read only
 Output – Read/Write

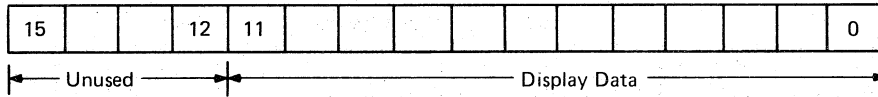
LPSVC STATUS REGISTER

15																	0
Bit		Function															
15-13		Unused															
12		Erase	(Storage Scope)														
11		Write thru	(Storage Scope)														
10		Store	(Storage Scope)														
9		Channel	(VR14–VR20)														
8		Color	(VR20)														
7		Ready Flag															
6		Interrupt Enable															
5		Unused															
4		Ext Delay	(Special Scopes)														
2,3		Mode															
1		Fast Intensify															
0		Intensify															

Mode

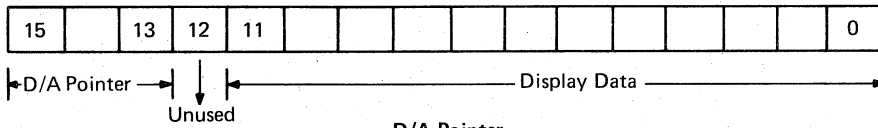
Bit 3	Bit 2	Function
0	0	Intensification with Bit 0 only
0	1	Intensification on Loading X Register
1	0	Intensification on Loading Y Register
1	1	Intensification on X or Y

LPSVC X and Y REGISTERS



Data is in offset binary format.

LPSVC EXT D/A REGISTER



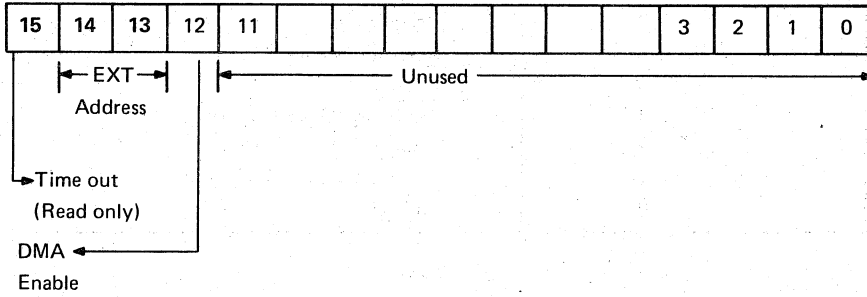
D/A Pointer

Bit 15	Bit 14	Bit 13	Expansion D/A Converter
0	0	0	DAC 0 (LPS DA # 1)
0	0	1	DAC 1 (LPS DA # 1)
0	1	0	DAC 2 (LPS DA # 2)
0	1	1	DAC 3 (LPS DA # 2)
1	0	0	DAC 4 (LPS DA # 3)
1	0	1	DAC 5 (LPS DA # 3)
1	1	0	DAC 6 (LPS DA # 4)
1	1	1	DAC 7 (LPS DA # 4)

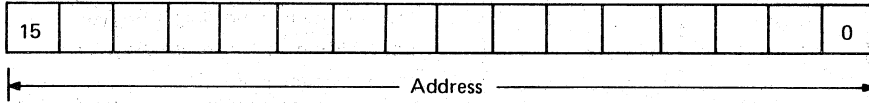
LPSAD-NP DMA REGISTER

The DMA Register will function as defined by the DMA Pointer in the LPS AD-12 Status Register

DMA Status Register

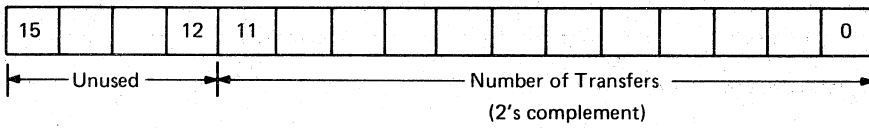


DMA Current Address Register



Bit 0 will always be loaded as a zero.

DMA Word Count Register



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SYSTEM USER'S GUIDE
DEC-11-HLPGA-C-D**

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