Digital Equipment Corporation
Maynard, Massachusetts

digital

DECkit11-D assembly and installation manual

LOGIC PRODUCTS

DEC-11-HKITD-A-D

DECkit11-D assembly and installation manual

digital equipment corporation • marlborough, massachusetts

1st Edition, January 1975

CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

TABLES

CHAPTER 1
INTRODUCTION

1.1 GENERAL

DECkit11-D, designed and manufactured by Digital Equipment Corporation, is a high-speed I/O interface utilizing Direct Memory Access (DMA) to transfer 16-bit data words directly between the PDP-11 memory and a user's I/O device. Data Transfer Out (DATO) or Data Transfer In (DATI) takes place via the PDP-11 Unibus after a Non-Processor Request (NPR) cycle, where the kit becomes bus master. DECkit11-D is intended for the PDP-11 system user who requires high I/O data transfer rates and who also has the capability to assemble and install the kit into an existing system. The kit is designed to be compatible with TTL logic levels; it uses simple I/O interfacing techniques and has unidirectional I/O signals. The kit consists of a pre-wired system unit mounting panel and nine M-Series modules and mounts in the PDP-11 processor or in an expansion mounting box, or other suitable enclosure. Figure 1-1 is a simplified system block diagram of a PDP-11 utilizing the DECkit11-D DMA Interface.

1.2 BASIC DATA TRANSFER

DECkit11-D receives or transfers 16-bit words to or from the user's I/O device and utilizes DATO and DATI cycles to DMA transfer the 16-bit words to or from the PDP-11 memory. The basic sequences for transferring words are as follows:

a. I/O device to DECkit11-D to memory – DMA transfers from the user's I/O device to PDP-11 memory take place when the I/O device places a 16-bit data word on the input lines to the kit and asserts a DATA AVAILABLE IN signal. A non-processor request (NPR) is now made by the kit. The kit becomes bus master and uses a DATO cycle to transfer the 16-bit data word to the PDP-11 memory. The kit now asserts a DATA ACCEPTED OUT signal to the user's I/O device to indicate that the word has been transferred.

b. Memory to kit to I/O device – DMA transfers from the PDP-11 memory to the user's I/O device take place when the kit makes a non-processor request (NPR) and becomes bus master. A DATI cycle is now used to make a DMA transfer of a 16-bit data word to the kit. At the end of the transfer, the kit places the 16-bit data word on the lines to the I/O device and asserts a DATA AVAILABLE OUT signal to the device. The I/O device responds by asserting a DATA ACCEPTED IN signal when the data is read.

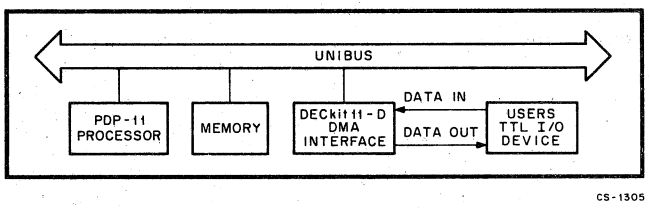

Figure 1-1 Simplified System Block Diagram

1.3 SPECIFICATIONS

The following specifications and particulars are for information purposes only and are subject to change without notice.

Mechanical

Logic Panels
One, type H933-CA (system unit)

Dimensions
10 in. h, 16-1/2 in. w, 2-1/4 in. d
(25.4 cm h, 41.9 cm w, 5.72 cm d)

Weight
4-1/2 lb
(2.0 kg)

Interconnections

Unibus: M920 required when DECkit11-D mounts in a cabinet with other system units; BC11A-XX* (of correct length) required when DECkit11-D is first unit in expansion box.

Input/Output: One input and one output cable are required.

Mounting Requirement

Space in existing PDP-11 processor or in an expansion mounting box.

Electrical

Logic Power Requirements

+5 V ± 5% @ 3 A nominal

Loading

Presents 1 Unibus load

Logic

TTL

Module Type

M-Series

Environmental

Temperature

Storage: -40° to 66° C

Operating: 5° to 50° C (ambient at module surface)

Relative Humidity

10% to 95% non-condensing

Operational

Transfer Mode

DMA utilizing Non-Processor Request (NPR)

Data Transfer

Bit parallel, word serial, unidirectional input and output

Data Signal Levels

TTL

Operating Speed

Data input to PDP-11 memory

Up to 1/2 million words per second depending on memory and other options.

Data output from PDP-11 memory

Up to 2/5 million words per second depending on memory and other options.

1.4 RELATED LITERATURE

In addition to the documents associated with the PDP-11 processor and KIT11-D Engineering Drawings, the *PDP-11 Peripherals Handbook* and the *Logic Handbook* contain information useful for installing operating, and maintaining DECkit11-D. Handbooks may be obtained from the nearest Digital Equipment Corporation sales office.

*Not furnished with DECkit11-D.

CHAPTER 2
ASSEMBLY

2.1 GENERAL

Assembly consists of unpacking the DECkit11-D from the shipping carton, verifying that the kit is complete, selecting the appropriate kit device address and kit interrupt vector address, configuring the M796 module for use with long I/O device cables (if required), and installing the modules into the pre-wired mounting panel.

2.2 UNPACKING DECkit11-D

Remove the kit components from the shipping carton and place on a suitable work surface. Verify that the M-Series modules are the same as those in the DECkit11-D Parts List in Appendix A. In addition, the kit should contain one pre-wired BB11-D system mounting unit (with two knurled mounting screws), five H850 handle extenders, two H852 (rib type) and two H853 (non-rib type) module holders. Parts missing from the kit should be reported to the nearest Digital Equipment Corporation sales office for replacement.

2.3 VISUAL INSPECTION

After verifying the shipped DECkit11-D components against the parts list, visually inspect for signs of physical damage, i.e., modules (excluding address selection jumpers removed from modules during factory test), broken casting or cracked mounting blocks on the pre-wired mounting panel. Inspect the mounting panel for bent or touching wire-wrap pins. Carefully straighten any bent pins. Contact the nearest Digital Equipment Corporation sales office for repair or replacement of damaged components.

2.4 TOOLS REQUIRED

The only tools required to carry out the assembly of the DECkit11-D is a pair of diagonal cutters and possibly, a low-wattage soldering iron. Installation requires only a screwdriver.

2.5 DECkit11-D DEVICE ADDRESS SELECTION (M7219)

There are four registers employed by DECkit11-D. The absolute bus address of these registers are determined by the configuration of jumpers on the address selection portion of the M7219 module. The four kit registers and the associated addresses are:

Register	Address
Word Count Register (WCR)	$7XXXX0_8$
Bus Address Register (BAR)	$7XXXX2_8$
Control/Status Register (CSR)	$7XXXX4_8$
Data Buffer Register (DBR)	$7XXXX6_8$

Normal user addresses start at 764000_8 and progress upward. At the time of manufacture, address 760000_8 is wired on the M7219 module. Using a pair of diagonal cutters, cut out the address selection jumpers on the M7219 module for bits to be decoded as "ONE" bits in the kit address. Figure 2-1 shows the kit address select format.

2.6 DECkit11-D INTERRUPT VECTOR ADDRESS SELECTION (M7821)

Vector addresses 170_8, 174_8, 270_8, and 274_8 are reserved for users. Address selection jumpers on the M7821 Interrupt Control Module are to be cut out for address bits which are "ZERO" bits in the vector address. Figure 2-2 shows the interrupt vector address select format.

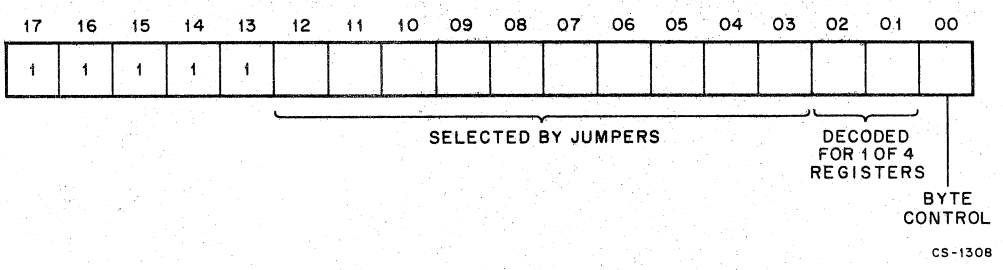

Figure 2-1 DECkit11-D Device Address Select Format

2.7 I/O CABLE LENGTH CONSIDERATIONS

During data output transfers, the M796 module asserts (low) DATA AVAILABLE OUT 150 ns (minimum) after the DECkit11-D Data Buffer Register is loaded. A period longer than 150 ns may be required to allow data levels to settle when cables over ten feet in length are used and no provisions for deskewing at the receiving end exist. The delay period can be lengthened by adding a capacitor to the split lugs provided on the M796 module. Each 50 pF of added capacitance increases the delay period by 100 ns. As a general rule, add 15 pF (per foot) for cable lengths greater than ten feet. In any event, capacitance greater than 1500 pF and cable lengths longer than 100 feet should be avoided.

2.8 MODULE INSTALLATION

Module installation involves the insertion of the DECkit11-D modules into the proper slots on the mounting panel.

CAUTION

To ensure proper module installation, insert the modules so that the deep notch on each module seats against the connector block rib.

Figure 2-3 shows the DECkit11-D slot assignments from the module side. After installation, secure the modules with the H852 and H853 module holders. Fasten one H852 module holder between module locations E and F, fasten the other H852 between locations C and D. The H853 module holders are fastened between module locations D and E, and B and C. Slots AB01 and AB04 are the Unibus I/O slots. The use of these slots varies with the type of installation (Paragraph 3.3.1).

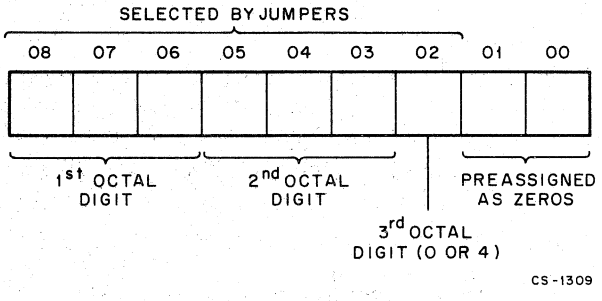

Figure 2-2 DECkit11-D Interrupt Vector Address Select Format

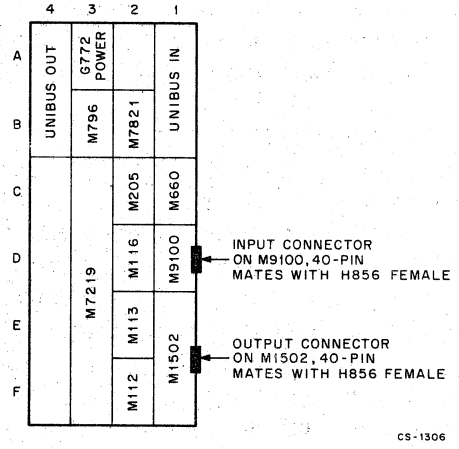

Figure 2-3 DECkit11-D Slot Assignments – Module Side

CHAPTER 3
INSTALLATION

3.1 GENERAL

Installation of DECkit11-D consists of securing the mounting panel (with the previously installed modules) into either an existing PDP-11 processor or expansion mounting box, or an added expansion mounting box; then connecting the Unibus, power, and I/O cables to the kit.

3.2 SYSTEM CONSIDERATIONS

Before installing DECkit11-D, consideration must be given to Unibus loading, priority requirements, space requirements, and power requirements.

3.2.1 Unibus Loading

DECkit11-D presents one bus load to the Unibus. Twenty bus loads can be handled by the standard PDP-11 Unibus before a bus repeater is required. Therefore, the user must determine the Unibus load when installing the kit and the possible need for a DB11-A bus repeater to handle additional bus loads. The bus repeater is not supplied with the kit but can be ordered from Digital Equipment Corporation.

3.2.2 Priority Requirements

DECkit11-D makes bus requests on priority level five (BR5) for interrupts and utilizes non-processor requests (NPRs) for DMA transfers. Since the user may connect the kit to the bus along with other devices which use the BR5 level and/or the NPR level, the user must bear in mind that when more than one device is connected to the same request line (either BR or NPR), the device electrically nearest the PDP-11 processor has the highest priority.

3.2.3 Space Requirements

DECkit11-D consists of one BB11 system unit mounting panel. The kit may be mounted either in an existing PDP-11 processor, an existing expansion mounting box, or by the addition of an expansion mounting box, or in any other suitable enclosure which provides proper cooling and protection.

3.2.4 Power Requirements

DECkit11-D requires +5 Vdc at 3 amperes. When the kit is mounted in a PDP-11 processor, or in an expansion mounting box, power is provided by the existing +5 Vdc power supply. Any power supply capable of meeting the voltage, current, regulation, and ripple requirements of a Digital Equipment Corporation H720 power supply may be used to power the kit (if the kit is not installed in a PDP-11 or a mounting box).

3.3 CABLING

DECkit11-D requires connections to the PDP-11 Unibus, to the user's I/O device, and to the logic +5 Vdc power source. Unibus, I/O, and power cables for use with the kit may be ordered from Digital Equipment Corporation.

3.3.1 Unibus Cables

Installation of DECkit11-D into a cabinet containing other system units requires an M920 Unibus connector module. The M920 module plugs into slot AB04 of the existing system unit and into slot AB01 of the kit (Figure 2-3). When the kit is installed as the first system unit in an expansion box, a BC11A-XX* cable (of correct length) is required to connect between slot AB04 of the last system unit in the cabinet or previous expansion box and slot AB01 of the kit.

Neither the M920 module nor the BC11A-XX* cable is supplied with the kit. An M930 terminator module must be installed in slot AB04 of the kit (Figure 2-3) when the kit is the last device on the Unibus. The M930 module becomes available when the Unibus is extended from the previous system unit.

3.3.2 Power Cables

There are three wire harnesses available for use in connecting the DECkit11-D to PDP-11 systems. Each expansion mounting box is equipped with a wire harness, terminated with a G772 connector, to mate with power connector slot A03 (Figure 2-3) of the kit. Early PDP-11

*XX = cable length in feet.

processors (PDP-11/15, PDP-11/20) have wire harnesses with G772 connectors for all system unit mounting locations. Later PDP-11 processors (PDP-11/30, PDP-11/40, and PDP-11/45) have wire harnesses with a Mate-N-Lok power connector for all system unit mounting locations. Wire harnesses are furnished only as needed. When installing the kit into one of the later systems, one of the following harness assemblies is required:

a. For PDP-11/45 systems having serial numbers below 2000 and using 8-pin Mate-N-Lok to G772 connectors:

Cable No.	Length
7008855-1J	20 in.
7008855-2B	26 in.

b. For PDP-11/40 systems having serial numbers below 6000; in PDP-11/35 systems (21 in. high processor cabinet) having serial numbers below 6000; in H960-D and H960-E cabinet configurations having serial numbers below 7000; and in all PDP-11/E05, PDP-11/E10, PDP-11/35 (10-1/2 in. high processor cabinet); all using 9-pin Mate-N-Lok to G772 connectors:

Cable No.	Length
7008909-11	11 in.
7008909-24	24 in.

c. For PDP-11/45 systems having serial numbers 2000 and above; in PDP-11/40 systems with serial numbers 6000 and above; in PDP-11/35 (21 in. high processor cabinet) systems with serial numbers 6000 and above; and in H960 and H960-E cabinet configurations having serial numbers 7000 and above; all using 15-pin and 6-pin Mate-N-Lok to G772 connectors:

Cable No.	Length
7009562	18 in.

Alternatively, a G772 connector can be installed on a suitable cable for use with any +5 Vdc power supply, meeting the current and regulation requirements of DECkit11-D, or +5 Vdc power can be directly connected to wire-wrap pins for +5 V and ground on slot A03 (shown on BB11D-4 in the KIT11-D Engineering Drawings).

3.3.3 User I/O Cables

Two cable assemblies are required for transferring the user's I/O device 16-bit data words to and from the DECkit11-D. Input signals to the kit are applied through a 40-pin male connector, mounted on the M9100 module in slot D01 (Figure 2-3), while output signals from the kit are brought to a 40-pin male connector on the M1502 module in slot EF01 (Figure 2-3). It is recommended that cable assemblies from the following list be used to interface the kit with the user's I/O device. Cable selection is determined by the type of connections used on the I/O device. The desired cable length (XX) must be specified when ordering.

Cable No.	Connectors	Type	Standard Lengths (Ft.)
BC07A-XX	H856 to open end	20-twisted pair	10, 15, 25
BC07D-XX	H856 to open end	2, 20-conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25 50, 75, 100
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

3.4 INSTALLATION

The installation procedure presented below details the installation of the DECkit11-D into a PDP-11 processor or an expansion mounting box. The installation procedure is as follows:

1. Mount the kit (with modules previously installed) into the vacant system unit location; secure with the two special knurled screws supplied with the kit (Figure 3-1).

2. Plug Unibus cable or an M920 Unibus connector module (whichever applies) into slot AB01 (Figure 2-3) of the kit.

3. Plug an M930 terminator in kit slot AB04 if the kit is the last device on the Unibus, if not the last device, install an M920 connector module or BC11A cable in slot AB04.

4. Plug the G772 power connector into kit slot A03.

5. Examine the interconnecting cables for pinched wires or loose connections.

6. The user's I/O device input and output cables are plugged into the kit after performing the initial turn-on procedure.

3.5 INITIAL TURN-ON

After completing the installation procedure, turn on the PDP-11 system power and perform the following:

1. Check for the presence of +5 Vdc and -15 Vdc at the kit mounting panel (refer to KIT11-D Engineering Drawings and Figure 3-2).

2. Load address of the WCR, BAR, CSR, and DBR through the PDP-11 console switches and examine the locations. The console indicators will display the following:

   WCR and BAR contents will be all 0s.

   CSR contents will be 610_8.

   DBR contents will be all 1s.

3. The WCR and BAR can be loaded with data from the PDP-11 console switches and the corresponding data (with the exception of BAR bit 0) read back on the console indicators. BAR bit 0 will always remain 0.

The user's I/O device cables can now be connected to the kit at the M9100 module (slot D01) and the M1502 module (slot EF01), (Figure 2-3).

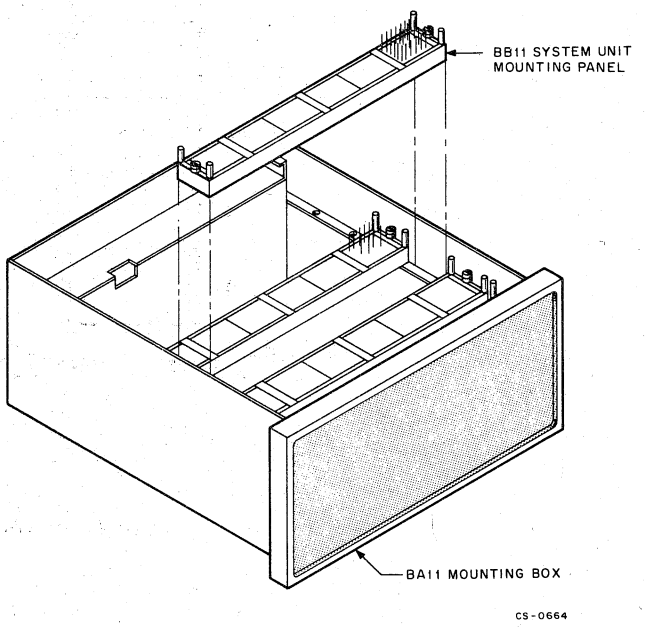

Figure 3-1 Installation of DECkit11-D System Unit Mounting Panel

3.6 OPTIONAL DIAGNOSTIC TEST KIT (KIT11-DT)

The check procedure performed in Paragraph 3.5 does not completely verify the operation of DECkit11-D. Complete kit operation can be verified through the use of the optional *Diagnostic Test Kit* which is available from Digital Equipment Corporation. The diagnostic test kit consists of a BC08R-01 one foot cable, used to loop the DBR output to the DBR input, and a software diagnostic program which tests DECkit11-D. This test kit is a prerequisite for Field Service installation and for Field Service contracts.

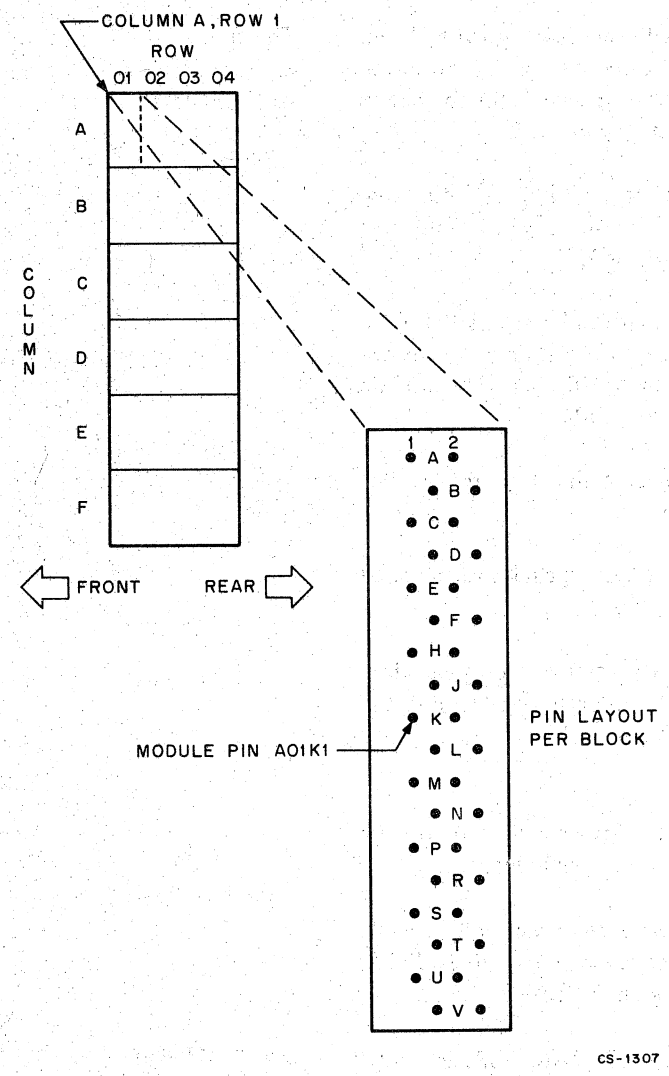

Figure 3-2 Mounting Panel Pin Designation

CHAPTER 4
BASIC OPERATION

4.1 GENERAL

This chapter contains a general functional description of DECkit11-D operations. Figure 4-1 is a block diagram of DECkit11-D. Operation consists of transferring 16-bit data words from the user's I/O device to the Unibus through the kit, and transferring 16-bit data words from the Unibus to the user's I/O device through the kit. Finally, brief descriptions of the kit timing associated with the word transfers are presented.

4.2 FUNCTIONAL DESCRIPTION

4.2.1 User's I/O Device to Unibus Word Transfer

Word transfers from the user's I/O device to the Unibus are DMA transfers. The kit Word Count Register (WCR) is loaded with a count equal to the number of words to be transferred, the Bus Address Register (BAR) is loaded with the starting memory address for word storage, and the Control and Status Register (CSR) is set for input transfers. The user's I/O device places 16 bits of data on the lines to the kit and sets DATA AVAILABLE IN. DATA AVAILABLE IN is now applied to the DMA control. This causes the DMA control to produce a DMA REQUEST which is applied to the interrupt control; the interrupt control in turn places an NPR on the Unibus. In response to the NPR, the PDP-11 processor returns a bus grant (NPG). The kit now becomes bus master and places the starting memory address [A(17:00)] from the BAR onto the Unibus and sets the C0 and C1 control lines for a DATO cycle and issues MSYN. Sixteen bits of user I/O data are now gated (by the READ command) through the DMA input to the Unibus. Memory now stores the data and responds with SSYN, terminating the DATO cycle. As words are transferred, the WCR and BAR are incremented. For each transfer, DATA ACCEPTED OUT is applied to the user's I/O device to indicate that the word has been read. The process of transferring words and incrementing the WCR and BAR continues until the WCR increments to zero (indicating that all words are transferred), then an interrupt is generated by the kit to signify the "done" state.

Interrupts from DECkit11-D to the PDP-11 processor occur on BR5 for four possible causes:

a. When the Word Count Register increments to zero (WC0) – This is a normal interrupt at the end of a designated number of word transfers.

b. When the user's I/O device presents data to the kit for transfer and the kit is not prepared to perform a DMA transfer.

c. When the user's I/O device transfers a number of words which is less than the number stored in the WCR.

d. When a non-existent memory location is addressed by the program.

(Interrupts are presented in greater detail in Chapter 5 of this manual.)

Each interrupt causes the DMA control to generate and apply an INT REQUEST to the interrupt control. The interrupt control requests service through BR5. After receiving the bus grant (BG5), the kit becomes bus master (after completing the Unibus handshake routine) and applies INT and the vector address [D(08:02)] on the Unibus lines. The PDP-11 processor may now read the kit CSR word [D(15:00)].

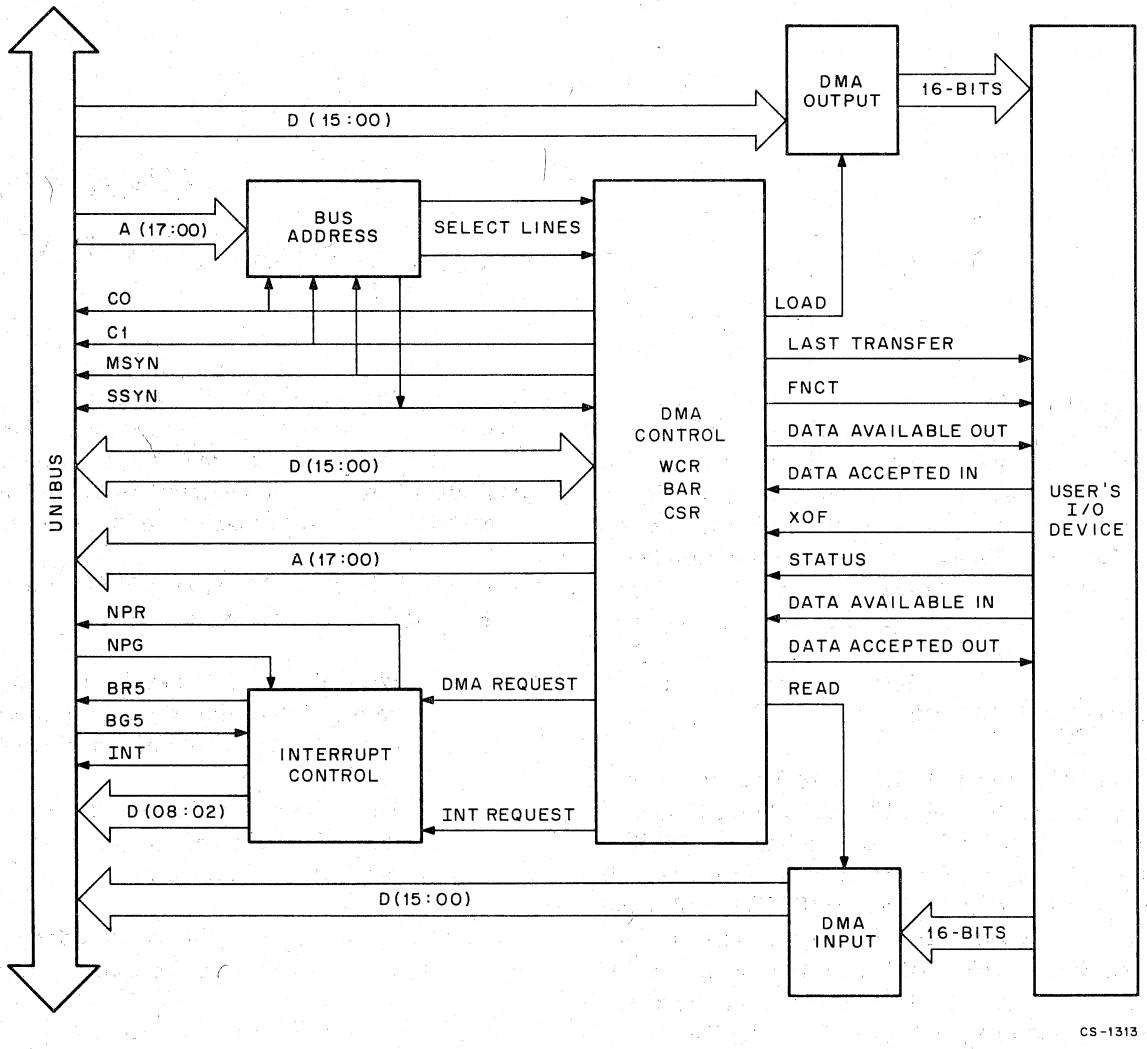

Figure 4-1 DECkit11-D Block Diagram

4.2.2 Unibus to User's I/O Device Word Transfer

Word transfers from the Unibus to the user's I/O device may be either a DMA transfer or a program-controlled transfer. For DMA transfers, the PDP-11 processor loads the WCR with a count equal to the number of words to be transferred, loads the BAR with the address of the first word to be transferred, and sets the CSR for an output transfer. The kit now makes an NPR request and after receiving a bus grant (NPG), becomes bus master and sets the C0 and C1 lines for a DATI cycle. MSYN is now issued by the kit. Memory then places the data on the bus followed by SSYN. The kit DMA control loads the data into the DMA output and applies DATA AVAILABLE OUT to the user's I/O device. When the user's I/O device accepts the data, DATA ACCEPTED IN is applied to the DMA control to indicate that the data has been read. The BAR and WCR are incremented for each DATI cycle until the WCR is incremented to zero. When WCR equals zero, an interrupt is generated by the kit to signify the "done" state.

Program-controlled transfers are accomplished through the use of the MOV instruction. The PDP-11 processor "moves" the contents of a particular location to the DBR* address specified in the destination field of the instruction word. This destination address [A(17:00)] is decoded by the kit and generates SELECT LINES to the DMA control. The DMA control then produces LOAD and DATA AVAILABLE OUT. LOAD strobes the data [D(15:00)] from the Unibus into the DBR while DATA AVAILABLE OUT notifies the user's I/O device that data is ready. Each word transfer to the user's I/O device is acknowledged with DATA ACCEPTED IN.

*Data Buffer Register (DMA output).

4.3 TIMING

4.3.1 Output Timing

Figure 4-2 shows the DECkit11-D output timing sequence. The timing sequence starts when a 16-bit data word is loaded into the DBR. This occurs at the completion of an output DMA cycle on the Unibus.

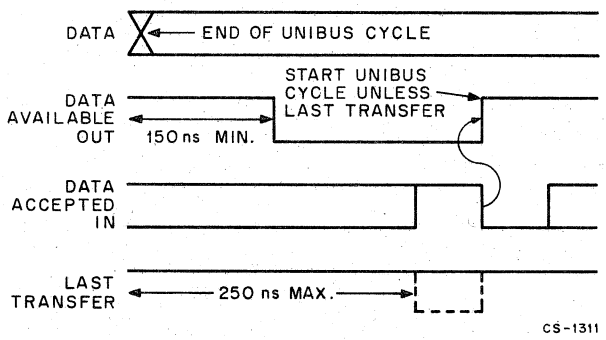

Figure 4-2 Output Timing

DATA AVAILABLE OUT is asserted (low) 150 ns (minimum) after the DBR is loaded. This 150 ns period can be lengthened by adding a capacitor to split lugs provided on the M796 module. The longer period may be required to allow data settling. (See Paragraph 2.7 for I/O cable length considerations.) The DATA AVAILABLE OUT signal specifies to the receiving device that the data in the Data Buffer Register can be read. When the receiving device has accepted the data, it causes DATA ACCEPTED IN to become low. This transition negates DATA AVAILABLE OUT and terminates the output cycle.

LAST TRANSFER is set by WCOF to specify the end of a block of DMA transfers. Assertion is at the low level. LAST TRANSFER can occur up to 250 ns following loading of the DBR. When DATA AVAILABLE OUT is negated, LAST TRANSFER is cleared.

4.3.2 Input Timing

Figure 4-3 shows the input timing sequence. The input timing sequence starts when a data word is presented to the input logic. Sufficient time must be provided to allow the data to settle to its final state. This is a function of the driver circuit at the source of the data word in the user device. Once the data has settled, the user's device asserts DATA AVAILABLE IN low, signalling the processor that the data can be read. DATA AVAILABLE IN must remain low until DATA ACCEPTED OUT becomes low, specifying that the processor has accepted the data. If DATA AVAILABLE IN is not held low, the processor accepts the data word but DATA ACCEPTED OUT is not generated. DATA AVAILABLE IN must not transition from high to low for at least 100 ns after DATA ACCEPTED OUT goes low. In instances where the number of words to be received by the processor is unknown, XOF is generated by the sending device when the last word is transferred. XOF is sampled at the completion of the input cycle when DATA ACCEPTED OUT is issued.

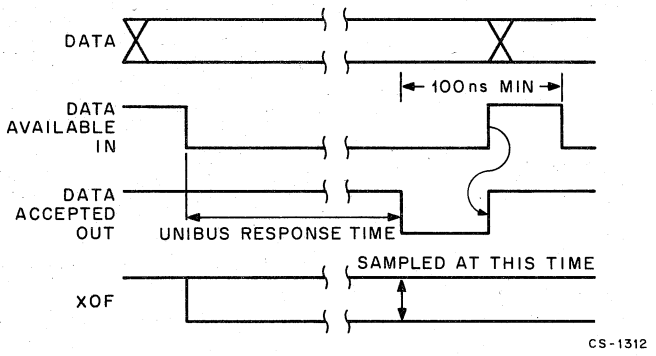

Figure 4-3 Input Timing

CHAPTER 5
PROGRAMMING

5.1 GENERAL

This chapter presents basic programming information for the DECkit11-D. The use of the four kit registers, the program interrupts, and input/output transfers are discussed. Finally, a short sample program is provided.

5.2 DECkit11-D REGISTERS

Four registers are utilized by DECkit11-D: Word Count Register (WCR), Bus Address Register (BAR), Control/Status Register (CSR), and the Data Buffer Register (DBR). The addresses of these registers are determined by the jumper configuration on the M7219 module (refer to Paragraph 2.5, Address Selection).

5.2.1 WCR

The 16-bit WCR holds the 2's complement (negative number) of 16-bit data words to be transferred into or out of the PDP-11 memory during DMA transfers. Following each word transfer, the WCR is incremented by one to indicate the number of words transferred. When the last word is transferred, the WCR is incremented to zero and an interrupt is requested.

NOTE

The WCR is not byte-addressable. DECkit11-D is capable of addressing up to 32K words. Bit 15 of the WCR should always be loaded with a one to keep the total number of transfers to 32K or less.

5.2.2 BAR

The 15-bit BAR initially holds the address that specifies the memory location into which the first word is written, or from which the first word is read. Following the transfer of each word, the BAR is incremented by two, to point to the next higher sequential memory word location, up to 32K.

NOTE

The BAR is not byte-addressable. If the BAR is incremented to the 32K limit and the WCR has not incremented to zero, and there has been no word count overflow, the address will "wrap around" to location zero on the next transfer.

5.2.3 CSR

The 16-bit CSR provides the means by which the PDP-11 processor commands and monitors DECkit11-D operations; it is the only register that is byte-addressable. Figure 5-1 shows the CSR bit assignments. The function of each bit is described in Table 5-1.

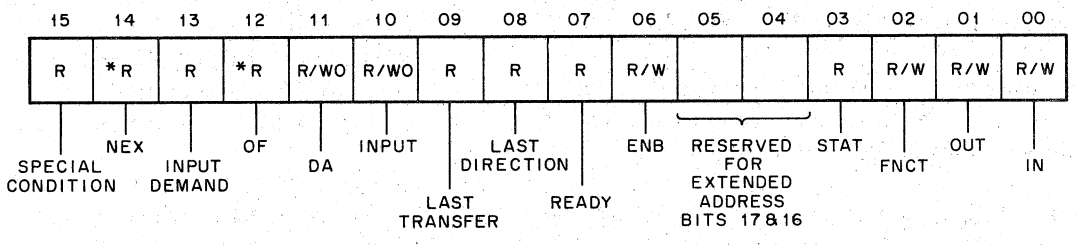

Figure 5-1 CSR Format

Table 5-1
CSR Bit Functions

Bit	Function
00	*IN:* Read/write bit controls all data input transfers. When set to a 1, this bit allows data to be transferred to PDP-11 memory by means of an NPR request and a DATO bus cycle. The NPR occurs when bit 10 (INPUT) is set to a 1 by the DATA AVAILABLE IN signal. When IN is a 0, and INPUT is set to a 1 by DATA AVAILABLE IN, an interrupt request occurs on BR level 5. Incoming data can be ignored only by clearing IN and bit 06 (ENB). IN is cleared by INIT, bit 14 (NEX) setting to a 1, by word count overflow, or by external overflow.
01	*OUT:* Read/write bit controls all data output transfers. When this bit is set to a 1, the interface performs a DATI cycle, loads data into the output buffer and asserts DATA AVAILABLE OUT. When DATA ACCEPTED goes low, DATA AVAILABLE OUT is negated and another DATI cycle occurs. The output operation is normally terminated by word count overflow; however, it can be terminated under program control. OUT is cleared by INIT, bit 14 (NEX) setting to a 1, by word count overflow, or by external overflow.
02	*FNCT:* Read/write bit available at Pin V of the output cable for use as a function bit. When set, a low is present at Pin V. FNCT is cleared by INIT.
03	*STAT:* Read-only bit associated with Pin V of the input cable and is used to indicate status. When set, a high is present at Pin V.
04	Reserved for Extended Bus Address Bit 16.
05	Reserved for Extended Bus Address Bit 17.
06	*ENB:* Read/write bit enables DECkit11-D priority interrupts when set to a 1 and disables the interrupt feature when on a 0. ENB is cleared by INIT.
07	*READY:* Read-only bit, when set to a 1, specifies that the DECkit11-D is conditioned to accept a command. READY (1) is the result of the AND of IN (0), OUT (0) and DA (0). When word count overflow occurs and READY is a 1, an interrupt request is posted.
08	*LAST DIRECTION:* Read-only bit specifies the direction of the last transfer: 0 = input, 1 = output. INIT sets LAST DIRECTION to a 1 if the output module is installed, if not, LAST DIRECTION always reads as 0.
09	*LAST TRANSFER:* Read-only bit is set to a 1 when the final data word is transmitted; LAST TRANSFER is cleared to 0 when the final data word is accepted.
10	*INPUT:* Can be read but can be written to 0 only. It is set to a 1 by DATA AVAILABLE IN when data is presented to the input. INPUT causes an NPR request when bit 00 (IN) is set and causes an interrupt request when IN is on a 0. INPUT is cleared at the completion of an input DMA cycle.
11	*DA:* Can be read but can be written to 0 only. DA is set to a 1 when DATA AVAILABLE OUT is asserted and is cleared to 0 when DATA ACCEPTED IN is asserted, signifying acceptance of the data.
12	*OF:* Set to a 1 on completion of an input DMA cycle when XOF is held low until DATA ACCEPTED OUT goes low. OF, when set to a 1, terminates transfers, sets bit 15 (SPECIAL CONDITION) and causes an interrupt request. OF is cleared automatically when the low byte of the CSR is written.
13	*INPUT DEMAND:* Read-only bit is set to a 1 by the AND of INPUT (1) and IN (0) and is cleared when either condition becomes false. INPUT DEMAND, when set to a 1, sets bit 15 (SPECIAL CONDITION) and causes an interrupt request.
14	*NEX:* Read-only bit is set when an addressed memory location fails to respond with SLAVE SYNC within 20 μs. NEX, when set to a 1, sets bit 15 (SPECIAL CONDITION) and causes an interrupt request. NEX is cleared to 0 automatically when the low byte of the CSR is written.
15	*SPECIAL CONDITION:* Read-only bit is set to a 1 by the OR of NEX, INPUT DEMAND or OF, or by word count overflow when interrupt enable (bit 06) is zero. Bit 15 (0) is used to test for the normal interrupt condition, word count overflow.

5.2.4 DBR

The DBR holds 16-bit data words for transfer to memory from the user's I/O device or from memory to the I/O device. This register is not byte-addressable.

5.3 PROGRAM INTERRUPTS

DECkit11-D interrupts the processor on BR priority level five. Interrupts are conditioned on the state of bit 06 of the CSR (Figure 5-1 and Table 5-1) and occur for four reasons:

a. Word count overflow (normal interrupt)

b. Input demand (special condition indicated by CSR bit 13)

c. External overflow (special condition indicated by CSR bit 12)

d. Non-existent memory (special condition indicated by CSR bit 14)

5.3.1 Word Count Overflow Interrupt

Word count overflow (WCO) is the condition of the WCR incrementing to zero. The following conditions occur during word count overflow:

a. CSR IN (bit 00) and OUT (bit 01) are cleared, DA (bit 11) and LAST TRANSFER (bit 09) are set.

b. If CSR ENB (bit 06) is a one and DA (bit 11) is reset to zero by data accepted in, DECkit11-D interrupts on BR5. Special condition (bit 15) will be a zero.

c. If CSR ENB (bit 06) and DA (bit 11) are zeros, special condition (bit 15) will be a one.

5.3.2 Input Demand Interrupt

An input demand interrupt occurs when data is presented to the kit and the kit is not prepared to perform a DMA transfer. CSR bits 15, 13, 10, and 06 are set; bit 00 is zero for this interrupt.

5.3.3 External Overflow Interrupt

An external overflow interrupt occurs when the user's I/O device transfers a quantity of data words less than that designated by the WCR count selected by the processor. This overflow essentially simulates a word count overflow. CSR bits 15, 12, and 06 are set.

5.3.4 Non-Existent Memory Interrupt

A non-existent memory interrupt occurs when an addressed memory location fails to respond with SLAVE SYNC within 20 μs. CSR bits set for this interrupt are 15, 14 and 06.

5.4 PROGRAMMING CONSIDERATIONS

5.4.1 Output Transfers (Memory to User's I/O Device)

Output transfers are initiated by loading the WCR with the 2's complement of the number of data words to be transferred, loading the BAR with the address of the first word to be transferred, and then setting the out bit (bit 01) in the CSR. If an interrupt is desired to signal the processor when all transfers have been made, the interrupt enable bit (bit 06) in the CSR must be set.

If for some reason, such as an interrupt from the input, the output function must be terminated before all transfers have been made, the out bit (bit 01 of CSR) may simply be written to a zero by the processor. In this case, be sure to byte address the low byte to avoid disturbing DA (bit 11) or input (bit 10) in the high byte of the CSR. The WCR and BAR can then be read and stored away for use in completing the transfer at a later time.

5.4.2 Input Transfers (User's I/O Device to Memory)

Input transfers may be initiated for two reasons: if the processor is expecting input transfers, or if there has been an interrupt from input demand. In either case, the WCR and BAR must be set up as in output transfers (Paragraph 5.4.1). The in bit (bit 00) and the enable bit (bit 06) in the CSR must be set by writing into the low byte.

If the processor knows how many words are to be transferred, it sets the WCR to count the quantity of words. After the prescribed number of transfers, the WCR overflows and interrupts the processor.

In the case where the user's I/O device controls the number of words to be transferred, the processor sets the WCR to its maximum buffer size and the transfer is terminated by external overflow (XOF) from the user's I/O device. External overflow causes an interrupt which signals the processor to read the WCR to determine how many words were transferred.

5.5 EXAMPLE PROGRAM

The program below performs two NPRs and one interrupt per cycle. A wrap-around cable such as a BC08R-01 must be used to connect the output back to the input of the kit.

Enter the following octal equivalents by means of the PDP-11 console switches:

NOTE

PDP-11 register contents will be altered when power is turned off.

PDP-11 Processor Registers

Register	Location	Data	Comments
R1	177701	000000	
R2	177702	160000*	Device base address (jumper-selectable)
R3	177703	177776 (-2)	2's complement of number of transfers
R4	177704	1224	Location of first transfer
R5	177705	103	Control bits
SP	177706	1200	Stack pointer
PSW	177776	200	Processor status word (priority level 4)

*This is the device base address if no jumpers are cut on the M7219.

Program

Location	Instruction	Mnemonic Symbol	Comment
001200	010201	Start: Mov R2, R1	Place device address into R1
001202	010321	Mov R3, (R1)+	Set word count (-2)
001204	010421	Mov R4, (R1)+	Set Bus Address Register
001206	010511	Mov R5, (R1)	Set Control Status Register
001210	000001	Wait	Wait for kit interrupt
001212	000772	BR Start	Loop back to "Start"
001214	005711	Service: Test	Test the CSR
001216	100401	BMI	Is there a special condition?
001220	000002	RTI	No, return from interrupt
001222	000000	HLT	Yes, there shouldn't be
001224	Buffer, Data Word Out		Data to be transferred
001226	Buffer, Data Word In		Data received
Vector Address*	1214	Service DECkit	Start of service routine
Vector Address +2	240	Establish priority	Kit will interrupt on priority level 5

Start program at location 1200. Program will run.
*Vector Address is jumper-selectable on M7821 module, slot B02 of the DECkit11-D.

APPENDIX A
DECkit11-D PARTS LIST

A.1 PARTS LIST

Table A-1 lists the parts supplied with DECkit11-D by part number, description, and quantity used.

Table A-1
DECkit11-D Parts List

Part No.	Description	Quantity
BB11-D	Mounting Panel	1
H852	Module Holder (rib type)	2
H853	Module Holder (non-rib type)	2
H850	Handle Extender	5
M112	NOR Gates	1
M113	NAND Gates	1
M116	4-Input NOR Gates	1
M205	General Purpose Flip-Flops	1
M660	Positive Level Cable Driver	1
M796	Unibus Master Control	1
M1502	Bus Output Interface	1
M7219	Bus Interface	1
M7821	Interrupt Control	1
M9100	H854 to H854 to Flip Chip Adapter	1

APPENDIX B
MODULE M1502 OUTPUT CONNECTOR PIN ASSIGNMENTS

B.1 M1502 CONNECTOR PIN ASSIGNMENTS

Table B-1 lists the signals on the M1502 output connector by pin designation, signal name, signal description, and the drive capability.

Table B-1
M1502 Output Connector Pin Assignments

Pin	Signal	Description	Drive Capability (TTL Unit Loads)
A	GROUND	Logic Ground	
B	BD15	Buffered Data Bit 15 1 = High	20
C	GROUND	Logic Ground	
D	BD14	Buffered Data Bit 14 1 = High	20
E	GROUND	Logic Ground	
F	BD13	Buffered Data Bit 13 1 = High	20
H	GROUND	Logic Ground	
J	BD12	Buffered Data Bit 12 1 = High	20
K	GROUND	Logic Ground	
L	BD11	Buffered Data Bit 11 1 = High	20
M	GROUND	Logic Ground	
N	BD10	Buffered Data Bit 10 1 = High	20

Table B-1 (Cont)
M1502 Output Connector Pin Assignments

Pin	Signal	Description	Drive Capability (TTL Unit Loads)
P	GROUND	Logic Ground	
R	BD09	Buffered Data Bit 09 1 = High	20
S	GROUND	Logic Ground	
T	BD08	Buffered Data Bit 08 1 = High	20
U	GROUND	Logic Ground	
V	FNCT	Function Bit 1 = Low	20
W	GROUND	Logic Ground	
X	DA OUT	Data Available Out Low	30
Y	GROUND	Logic Ground	
Z	DATA ACCEPTED IN*	Data Accepted In Low	10*
AA	GROUND	Logic Ground	
BB	LAST TRANSFER	Last Transfer 1 = Low	20
CC	GROUND	Logic Ground	
DD	BD07	Buffered Data Bit 07 1 = High	20
EE	GROUND	Logic Ground	
FF	BD06	Buffered Data Bit 06 1 = High	20
HH	GROUND	Logic Ground	
JJ	BD05	Buffered Data Bit 05 1 = High	20

*This is an input signal on the output connector. It presents a load and has no drive capability.

Table B-1 (Cont)
M1502 Output Connector Pin Assignments

Pin	Signal	Description	Drive Capability (TTL Unit Loads)
KK	GROUND	Logic Ground	
LL	BD04	Buffered Data Bit 04 1 = High	20
MM	GROUND	Logic Ground	
NN	BD03	Buffered Data Bit 03 1 = High	20
PP	GROUND	Logic Ground	
RR	BD02	Buffered Data Bit 02 1 = High	20
SS	GROUND	Logic Ground	
TT	BD01	Buffered Data Bit 01 1 = High	20
UU	GROUND	Logic Ground	
VV	BD00	Buffered Data Bit 00 1 = High	20

APPENDIX C
MODULE M9100 INPUT CONNECTOR PIN ASSIGNMENTS

C.1 M9100 CONNECTOR PIN ASSIGNMENTS

Table C-1 lists the signals for the M9100 input connector, by pin designation, signal name, signal description, and the unit loading.

Table C-1
M9100 Input Connector Pin Assignments

Pin		Signal	Description	Loading (TTL Unit Loads)
J2	J1			
A	VV	GROUND	Logic Ground	
B	UU	DAT 15 IN	Data Bit 15 1 = High	1
C	TT	GROUND		
D	SS	DAT 14 IN	Data Bit 14 1 = High	1
E	RR	GROUND		
F	PP	DAT 13 IN	Data Bit 13 1 = High	1
H	NN	GROUND	Logic Ground	
J	MM	DAT 12 IN	Data Bit 12 1 = High	1
K	LL	GROUND	Logic Ground	
L	KK	DAT 11 IN	Data Bit 11 1 = High	1
M	JJ	GROUND	Logic Ground	

Table C-1 (Cont)
M9100 Input Connector Pin Assignments

Pin J2	Pin J1	Signal	Description	Loading (TTL Unit Loads)
N	HH	DAT 10 IN	Data Bit 10 1 = High	1
P	FF	GROUND	Logic Ground	
R	EE	DAT 09 IN	Data Bit 09 1 = High	1
S	DD	GROUND	Logic Ground	
T	CC	DAT 08 IN	Data Bit 08 1 = High	1
U	BB	GROUND	Logic Ground	
V	AA	STAT	Status Bit 1 = High	1
W	Z	GROUND	Logic Ground	
X	Y	DA IN	Data Available In Low	10
Z	W	DATA ACCEPTED OUT*	Data Accepted Out Low	30*
AA	V	GROUND	Logic Ground	
BB	U	XOF	External Overflow Low	10
CC	T	GROUND	Logic Ground	
DD	S	DAT 07 IN	Data Bit 07 1 = High	1
EE	R	GROUND	Logic Ground	
FF	P	DAT 06 IN	Data Bit 06 1 = High	1
HH	N	GROUND	Logic Ground	
JJ	M	DAT 05 IN	Data Bit 05 1 = High	1
KK	L	GROUND	Logic Ground	

*This is an output signal on the input connector. It has a drive capability and is not a load.

Table C-1 (Cont)
M9100 Input Connector Pin Assignments

Pin J2	Pin J1	Signal	Description	Loading (TTL Unit Loads)
LL	K	DAT 04 IN	Data Bit 04 1 = High	1
MM	J	GROUND	Logic Ground	
NN	H	DAT 03 IN	Data Bit 03 1 = High	1
PP	F	GROUND	Logic Ground	
RR	E	DAT 02 IN	Data Bit 02 1 = High	1
SS	D	GROUND	Logic Ground	
TT	C	DAT 01 IN	Data Bit 01 1 = High	1
UU	B	GROUND	Logic Ground	
VV	A	DAT 00 IN	Data Bit 00 1 = High	1

DECKIT 11-D ASSEMBLY AND INSTALLATION MANUAL
DEC-11-HKITD-A-D

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

CUT OUT ON DOTTED LINE

— — — — — — — — — — — — Fold Here — — — — — — — — — — — —

— — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — — —

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

Digital Equipment Corporation
Technical Documentation Department
146 Main Street
Maynard, Massachusetts 01754

Digital Equipment Corporation
Maynard, Massachusetts

digital

printed in U.S.A.