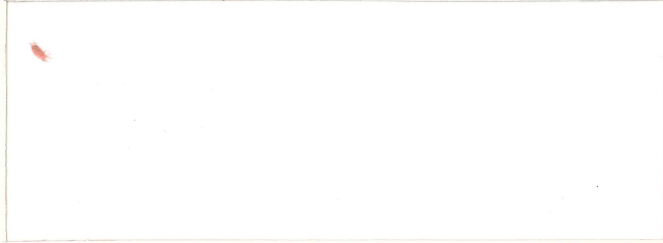


BM792  
read-only-memory  
and MR11-DB  
bootstrap loader

pdp11

digital



**BM792  
read-only-memory  
and MR11-DB  
bootstrap loader**

1st Edition, July 1971  
2 ns Printing, December 1971  
3rd Printing (Rev), October 1972  
4th Printing, December 1972  
5th Printing, May 1973  
6th Printing (Rev), January 1974

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# CHAPTER 1

## INTRODUCTION

### 1.1 SCOPE

This manual provides the user with theory of operation, programming information, and schematics necessary to understand and program the BM792 Read-Only-Memory (ROM). The level of discussion assumes that the reader is familiar with basic digital computer theory.

Although the input and output signals of the ROM are carried by the Unibus <sup>TM</sup>, it is beyond the scope of this manual to describe the Unibus itself. A detailed description of the Unibus is presented in the *PDP-11 Peripherals Handbook*.

### 1.2 GENERAL DESCRIPTION

The BM792 is a 32-word read-only-memory (ROM). The diode matrix and address selection circuits that constitute the ROM are mounted on an extra-width quad-board module. This module is inserted in either one of the two small peripheral controller slots in the PDP-11 processor or in one of the four slots in the DD-11 peripheral mounting panel.

The ROM is available either unprogrammed (designated BM792) or preprogrammed (designated BM792-Y X, where the letter in the X position identifies the program). The unprogrammed module can be programmed to form code conversion tables or contain frequently-used mathematical values and subroutines. These applications of the ROM provide an access time of 100 ns, which can increase the program speed.

Preprogrammed ROMs are used for implementing small standard programs required in PDP-11 System operation, such as bootstrap loaders for paper tape or DECTape. The preprogrammed ROMs that are available at publication of this manual are described in the Appendices and listed in Table 1-1. As additional preprogrammed ROMs become available, additional appendices will be published to describe them.

---

<sup>TM</sup> Unibus is a registered trademark of Digital Equipment Corporation.

Table 1-1  
Preprogrammed ROMs

Module	Option	No. of Words	Address Range	Power-Up Vector	Devices	No. of Words Read-In	Loading Area
M792-YA	BM792-YA	32	773000-773077	No	KL, DL-A, DL-B, PC, PR	162 max.	Highest Memory
M792-YB	BM792-YB	32	773100-773177	No	TC, RC, RF, RK, RP	256	0 and up
M792-YC	BM792-YC	32	773200-773277	No	CR, CM	Variable	Variable
M792-YD M792-YE	MR11-DB	64	773100-773277	Yes (Ex- cept TM)	TC, TM, RC, RF, RK, RP	TM:256 Others:512	0 and up
M792-YF	BM792-YF	32	773200-773277	No	TC, RK, RF	256	0 and up
M792-YH	BM792-YH	32	773300-773377	Yes	TA	64	0 and up



## CHAPTER 2

### DETAILED DESCRIPTION

#### 2.1 BASIC OPERATION

The ROM diode matrix contains 32 16-bit words, each of which can be applied to the bus under program control. The ROM responds only to a DATI from the Unibus, DATO, DATOB, and DATIP are ignored. A block diagram of the ROM is shown in Figure 2-1.

When both a DATI and a ROM address are sent to the ROM, the word in the addressed location of the diode matrix is applied to the Unibus. When the ROM address is received, the 5-bit code on address lines A01 through A05 is decoded to apply a signal to the cathodes of the diodes in the addressed word location. The word in the addressed location is transferred through the output buffer to data lines D00 through D15 of the Unibus.

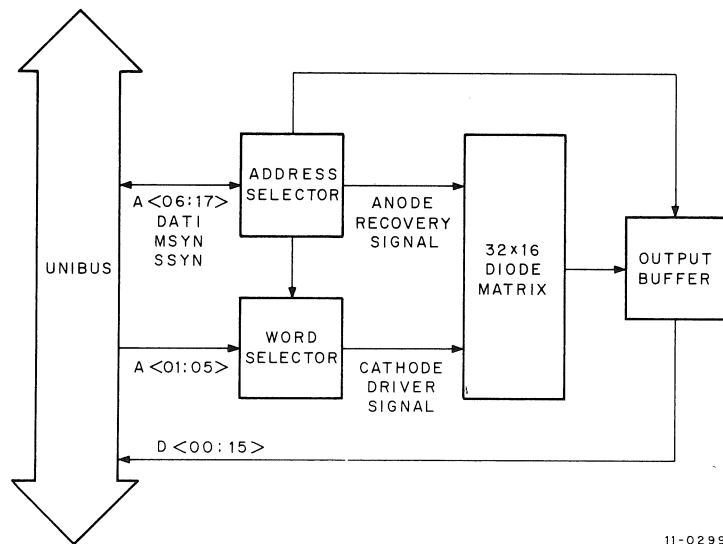


Figure 2-1 ROM Block Diagram

#### 2.2 ADDRESS SELECTION

The address word format for the ROM is shown in Figure 2-2. Octal addresses for the ROM must be of the 773XXX format. The ROM reads-out only full 16-bit words and does not issue byte data; thus, address bit A00 is not used.

The addresses are further divided into eight groups, which are determined by address bits A08, A07, and A06 and listed in Table 2-1.

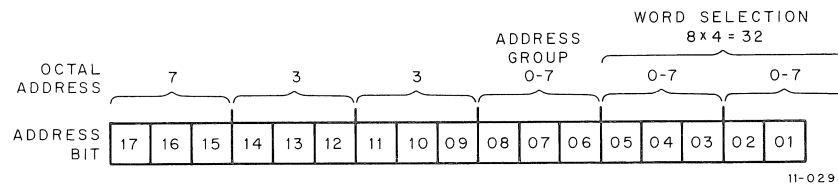


Figure 2-2 ROM Address Word Format

Table 2-1  
ROM Addresses

Address Word Bit			Address Ranges	Preprogrammed ROMs
A08	A07	A06		
0	0	0	773000 - 773076	BM792-YA
0	0	1	773100 - 773176	BM792-YB, YD
0	1	0	773200 - 773276	BM792-YC, YE, YF
0	1	1	773300 - 773376	BM792-YH
1	0	0	773400 - 773476	
1	0	1	773500 - 773576	
1	1	0	773600 - 773676	
1	1	1	773700 - 773776	

In a PDP-11 System, only one ROM module can be used for each of the eight address groups. Jumpers on the module are connected in a configuration that causes the module to respond to its designated address group.

For example, when a ROM module is to be addressed in the group 773400 - 773476, bits A08, A07, and A06 of the address word contain binary 100 as shown in Table 2-1. The bus lines for these bits are shown connected to the circuits of the ROM in Figure 2-3, a simplified logic diagram of the address selection circuits. Figure 2-3 also shows the address selection circuit jumpers connected to respond to address group 773400 - 773476. Asserted bus lines are low and unasserted bus lines are high, so that the output of gate E12 at pin 14 is high and the outputs of pins 2 and 3 are low when a valid address is received. Each of the three outputs from the E12 gates is exclusive NORed with a low or a high level, depending on the jumper configuration. The outputs of the three E13 gates must be high to accomplish address selection; therefore, the jumper configuration shown responds to addresses in the 773400 - 773476 group.

The signal, which results from the decoding of bits A08, A07, and A06, is gated with a signal generated by the decoding of an address in the format 773XXX and receiving MSYN (Drawing D-CS-M792-0-1). The resulting signal (pin 10 of gate E17) is gated with a signal generated by the decoding of a DATI on the control lines. Therefore, pin 8 of gate E17 provides a low output signal when the ROM address, MSYN, and DATI are asserted on the bus. This signal at pin 8 is used to accomplish the following in the ROM circuits (see Drawing D-CS-M792-0-1):

1. Assert SSYN on the bus.
2. Activate the word selection circuits.
3. Provide a gating signal to the output buffer.

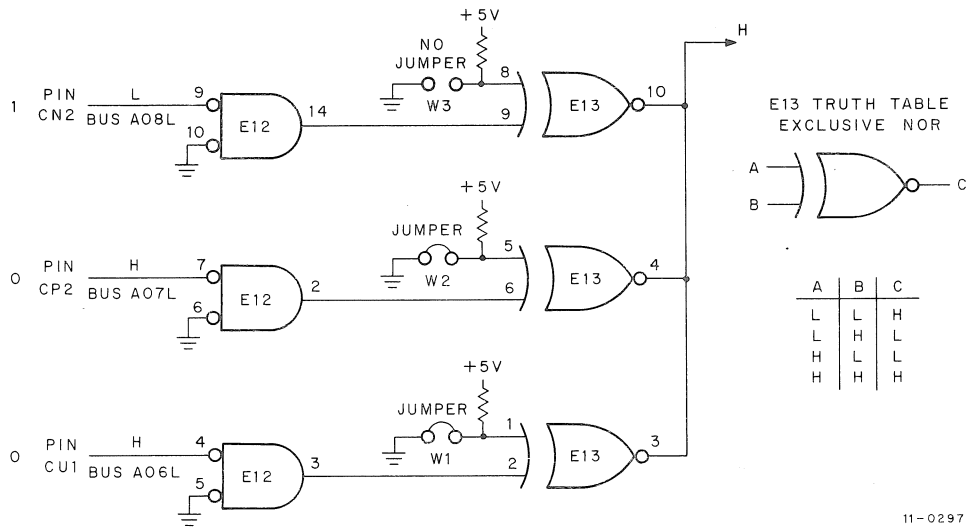


Figure 2-3 Simplified Logic Diagram of ROM Address Selection Circuits for Addresses 773400 – 773476

### 2.3 WORD SELECTION

Bits A05 – A01 of the address word are decoded by the word selection circuits to select one of the 32 word locations in the diode matrix. A low-level signal is then applied to the diodes in the addressed word location, resulting in 16 bits of data being read out on the data bus lines.

Because address bit A00 is not connected to the ROM, byte addressing is ignored and a 16-bit word is read onto the bus regardless of the state of A00. In the octal coding of the address, A00 is considered in designating the last octal digit. Therefore, the addresses of the words in the ROM use the following sequence:

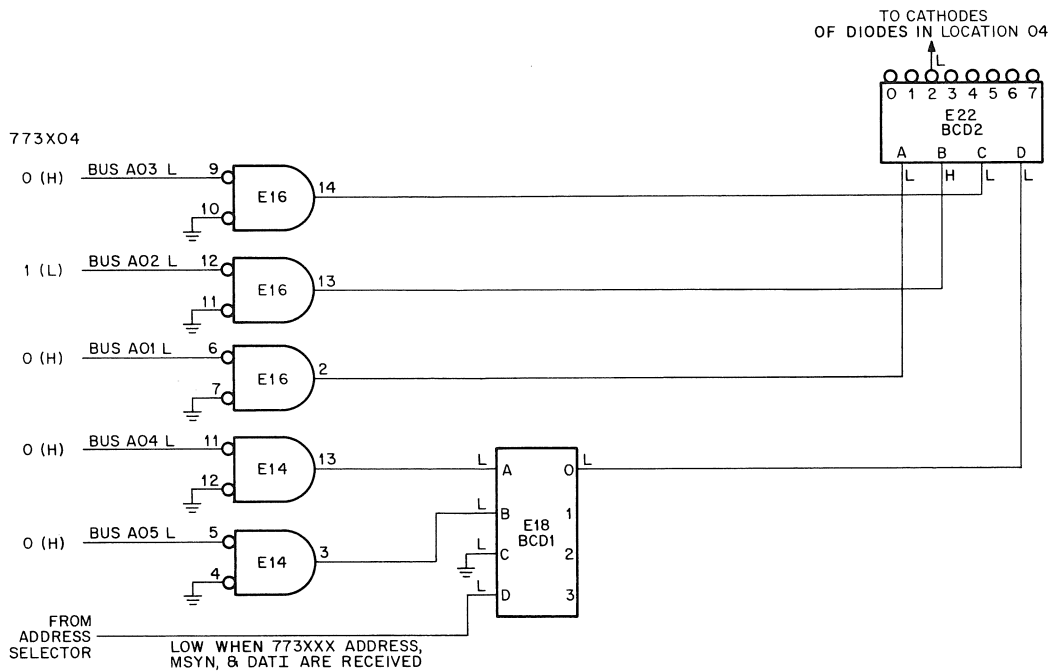
773X00  
 773X02  
 773X04  
 773X06  
 773X10  
 773X12  
 etc.

An address of 773X01 would address the same location as 773X00, and 773X03 would be the same as location 773X02.

A simplified logic diagram for the word selection circuits is shown in Figure 2-4. This diagram illustrates how the circuits operate for a 773X04 address. Table 2-2 is a truth table for the Binary-Coded Decimal (BCD) decoders that are shown in the diagram and on Drawing D-CS-M792-0-1.

For address 773X04, binary code 000 10 is applied to the word selection circuits on address lines A05 – A01 as shown in Figure 2-4. The D input of BCD 1 receives a low signal from the address selector circuits when addressing and bus signal conditions are satisfied. All inputs to BCD 1 are low with the result that output 0 is low (refer to Table 2-2). Output 0 of BCD 1 is connected to input D of BCD 2. The other inputs of BCD 2 are as shown in Figure 2-4 when address 773X04 is received. Table 2-2 shows that output 2 of BCD 2 is low with the input signal configuration shown. Output 2 of BCD 2 is connected to the cathodes of the 16-bit positions of location 04 in

the ROM. The signal levels on the cathodes of the other 31 word locations are high. Thus, only the diodes in location 04 are forward-biased, allowing the word in this location to be read by the output buffers and applied to the Unibus.



11-0296

Figure 2-4 Word Selection Circuit for 773X04 Address

## 2.4 DIODE MATRIX AND OUTPUT BUFFER

The BM792 ROM is supplied with a complete diode matrix. A diode is wired into each of the 16-bit locations of all 32 words. The binary content of each word is determined by the presence or absence of the diodes; thus, the user can program the module by cutting out selected diodes. Presence of a diode in a bit location produces a binary 1 and absence produces a binary 0. The preprogrammed ROMs are manufactured with the diode configuration required for their programs.

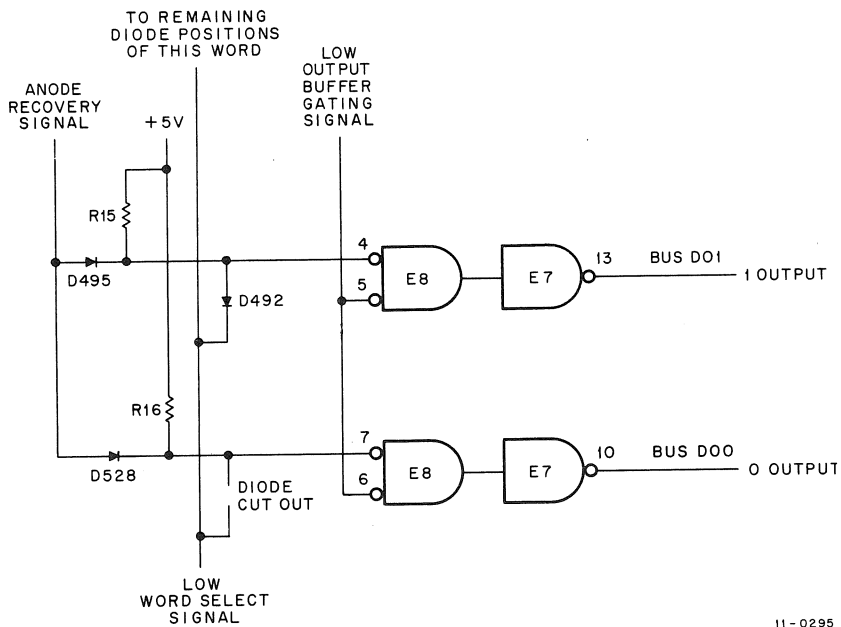
A simplified logic diagram of the diode matrix and the output buffer is illustrated in Figure 2-5. The low output buffer gating signal is present when the ROM address, MSYN, and DATI are asserted on the bus (refer to Paragraph 2.2). The word select signal is low when the particular word location is selected by the decoding of bits A05 – A01 (refer to Paragraph 2.3).

Diode D492 for the D01 bit is in the circuit and is forward-biased. Therefore, a low level is gated with the output buffer gating signal, which results in the assertion of a low level on bus line D01 to signify a binary 1. The diode for the D00 bit is cut out of the circuit. Therefore, a high-level signal is gated with the output buffer gating signal, which results in the assertion of a high level on bus line D00 to signify a binary 0. The remaining bit positions in the word are read out on bus lines D02 through D015 at the same time. The configuration of diodes for the bit positions of the word determines the binary content of the word read out on the bus lines.

Table 2-2  
BCD Decoder Truth Table

Input				Output							
A	B	C	D	0	1	2	3	4	5	6	7
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L
L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	H	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H

L = Low  
H = High



11-0295

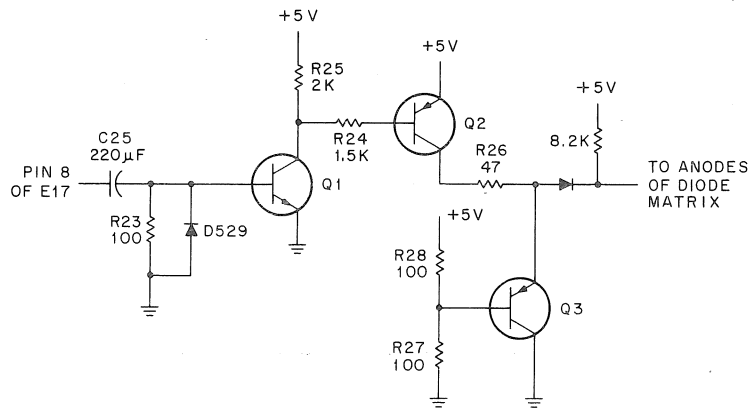
Figure 2-5 Diode Matrix and Output Buffer, Simplified Logic Diagram

## 2.5 ANODE RECOVERY CIRCUIT

The anode recovery circuit (see Figure 2-6) provides a voltage surge to the anodes of the diodes in the matrix immediately after a word is read out. This voltage surge charges the capacitance of the diode in the matrix and ensures that the anode lines in the matrix are at a high level for the next read out.

Transistors Q1, Q2, and Q3 (see Figure 2-6) are turned off when the ROM is not being addressed. Pin 8 of E17 goes from low to high when the bus addressing signals are concluded. The high signal turns on Q1 and subsequently Q2, which provides the positive voltage surge to the anodes of the diodes in the matrix.

Transistor Q3 of the anode recovery circuit is used as a clamp. When the voltage surge from the collector of Q2 reaches a high enough value, Q3 turns on and grounds out the surge.



11-0367

Figure 2-6 Anode Recovery Circuit

# CHAPTER 3

## PROGRAMMING AND OPERATION

### 3.1 GENERAL

The ROM operates in a manner similar to other memory devices that can be included in a PDP-11 system. When the ROM is used for storage of constants, the processor may be programmed to address the appropriate ROM location for the required constant. When the ROM is used for storage of a subroutine, a jump instruction is used to get into the subroutine and place the first address in the program counter. Then the program counter is changed to address the other sequential steps in the subroutine. The last step of a subroutine stored on the ROM should be either a jump instruction to a location out of the ROM or a return from subroutine instruction.

### 3.2 PROGRAMMING THE ROM

Programming the ROM is accomplished by cutting diodes out of the diode matrix in the configuration required for the binary data words to be used. The diode must be removed for each bit position that is to read out as a binary 0.

The physical orientation of the diode matrix with respect to the addresses and the bit positions is shown in Figure 3-1. Address 773X00 is shown with diodes removed in a configuration that reads out the binary word 1 010 010 011 101 011. With Figure 3-1 and a binary listing of up to 32 16-bit words, the user can program his ROM module.

The ROM module must also be programmed to respond to one of the address groups determined by address bits A08, A07, and A06 (refer to Table 2-1). Figure 3-1 shows the locations of the three sets of address-bit jumper terminals which are labeled W1, W2, and W3 on the ROM printed circuit board. The relationship between the jumper terminals and the address bit is as follows:

W1	A06
W2	A07
W3	A08

Jumper wires are connected across each of the three sets of jumper terminals on an unprogrammed ROM when it is shipped from the factory. The jumper wire must be cut out from between the two terminals for each address bit (A08, A07, or A06), that is a binary 1 in the ROM address used.





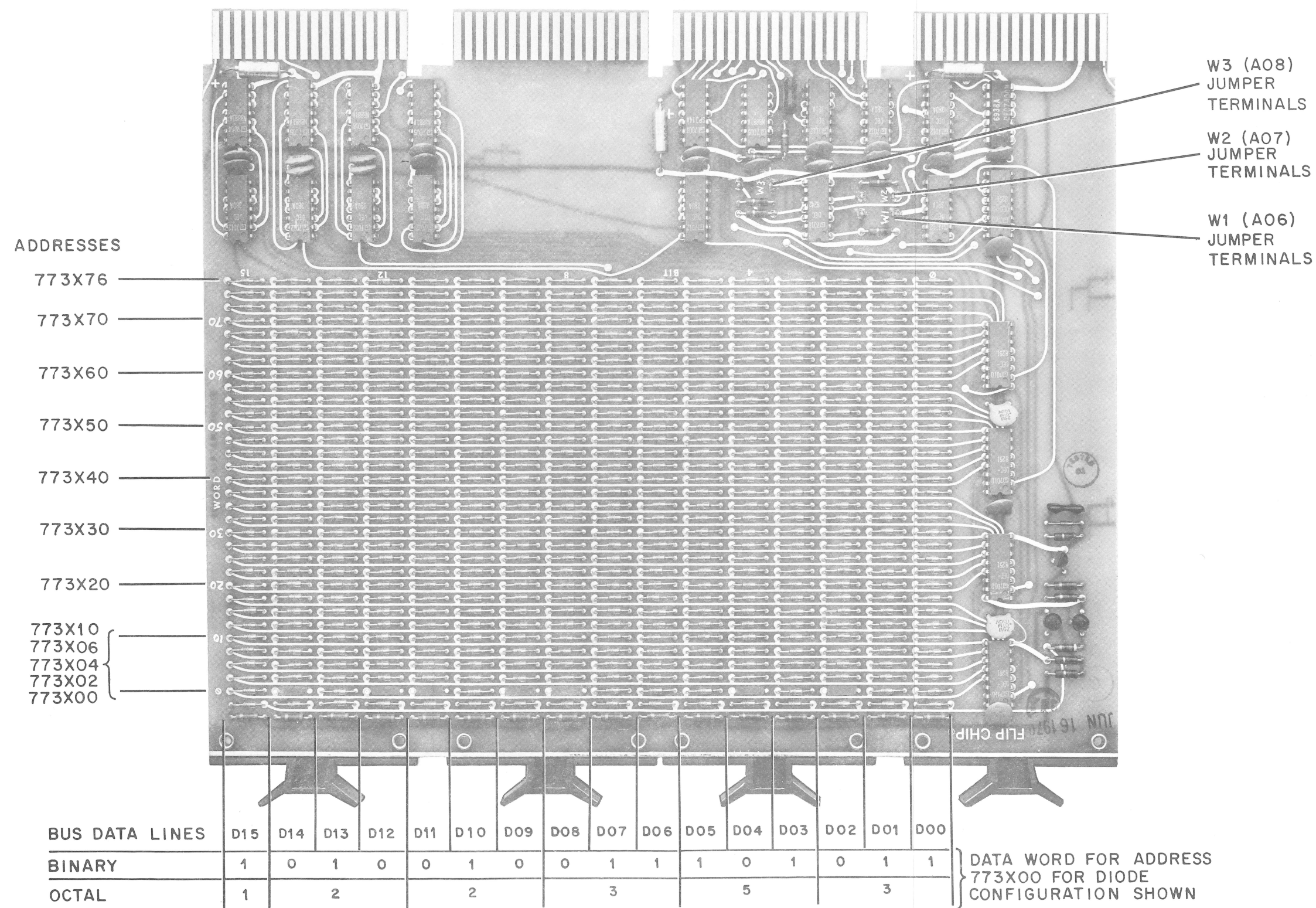


Figure 3-1 Physical Locations of Addresses and Bits in the ROM Diode Matrix



## CHAPTER 4

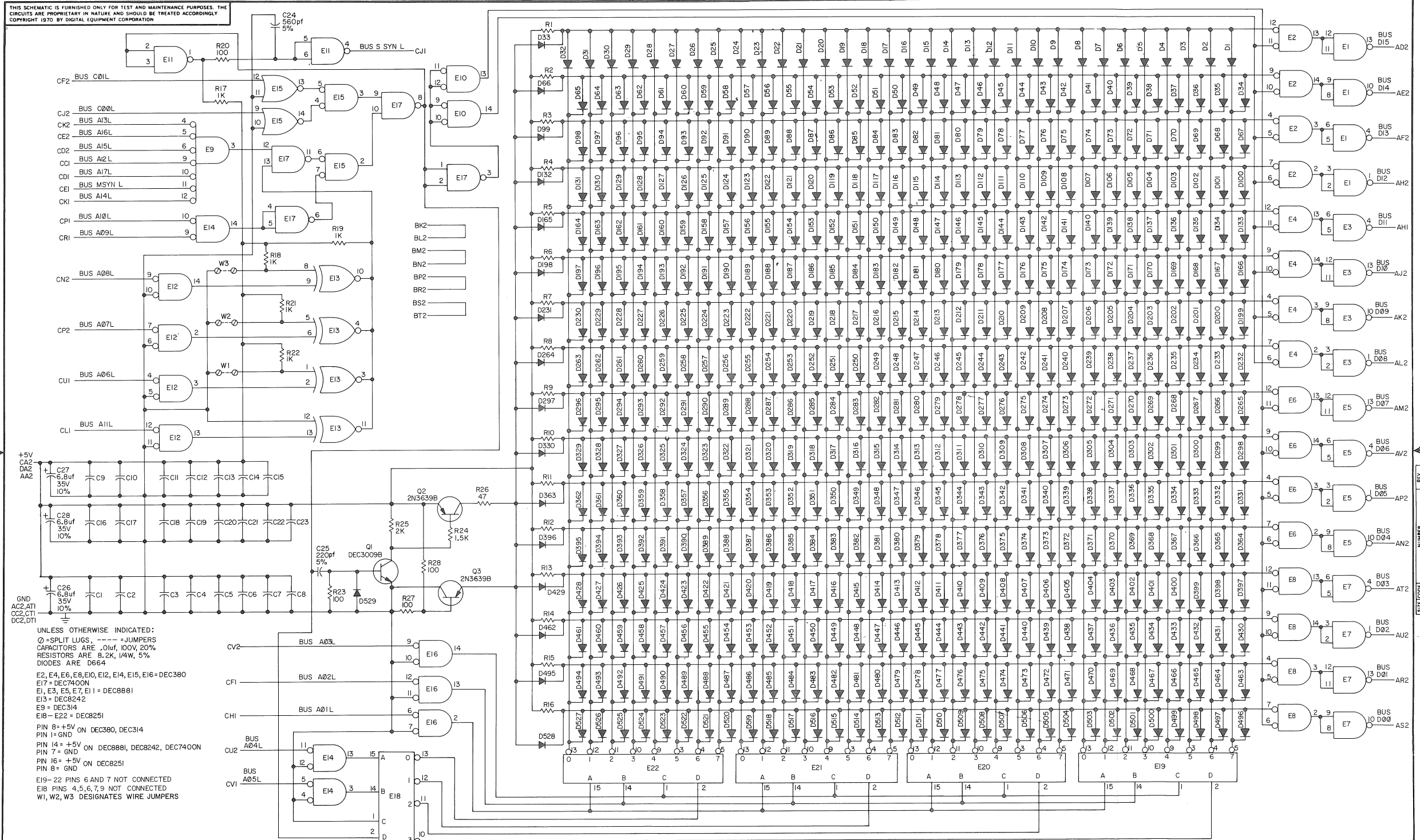
### ROM ENGINEERING DRAWINGS

The following engineering drawings are applicable to the BM792 ROM:

Title	Drawing No.	Rev.	Page
ROM Diode Matrix M792	D-CS-M792-0-1	D	4-3
ROM Diode Matrix M792-YA	D-CS-M792-YA-1	H	4-5
ROM Diode Matrix	D-CS-M792-YB-1		4-7
ROM Card Reader Bootstrap	D-CS-M792-YC-1		4-9
ROM Diode Matrix	D-CS-M792-YD-1	A	4-11
ROM Diode Matrix	D-CS-M792-YE-1	A	4-15
ROM Diode Matrix	D-CS-M792-YF-1		4-19
Cassette Bootstrap ROM	D-CS-M792-YH-1		4-23



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O = SPLIT LUGS, --- = JUMPERS  
CAPACITORS ARE .01uf, 100V, 20%  
RESISTORS ARE .2K, 1/4W, 5%  
DIODES ARE D664  
E2, E4, E6, E8, E10, E12, E14, E15, E16 = DEC380  
E17 = DEC7400N  
E1, E3, E5, E7, E11 = DEC8881  
E13 = DEC8242  
E9 = DEC314  
E18 - E22 = DEC8251  
PIN 8 = +5V ON DEC380, DEC314  
PIN 1 = GND  
PIN 14 = +5V ON DEC8881, DEC8242, DEC7400N  
PIN 7 = GND ON DEC8881, DEC8242, DEC7400N  
PIN 16 = +5V ON DEC8251  
PIN 8 = GND  
E15 - 22 PINS 6 AND 7 NOT CONNECTED  
E18 PINS 4, 5, 6, 7, 9 NOT CONNECTED  
W1, W2, W3 DESIGNATES WIRE JUMPERS

REVISIONS

CHK	CHR	NO	REV
Z	7	00001	B
W	4	00002	C
U	3	00003	D
T	2	00003	D

TRANSISTOR & DIODE CONVERSION CHART

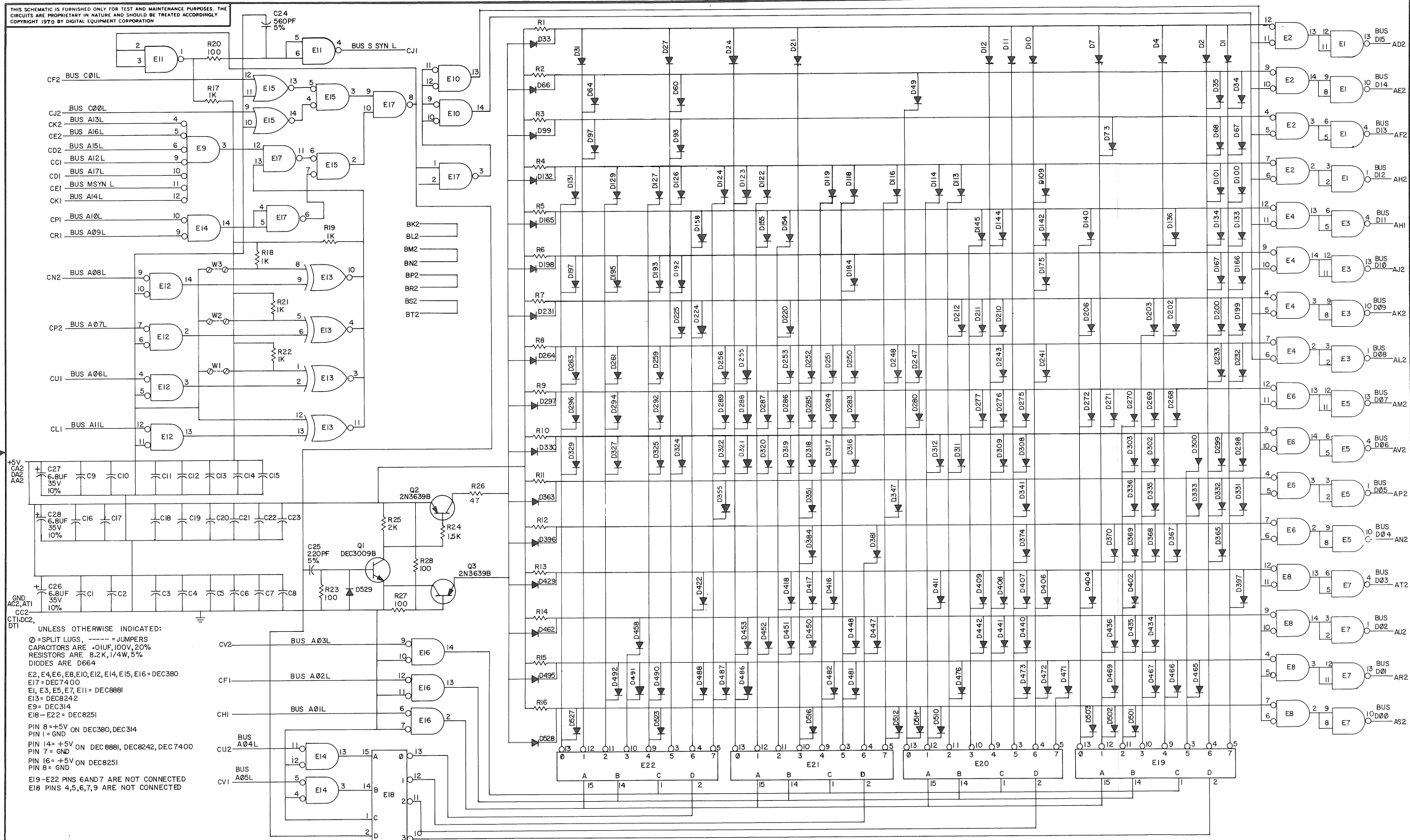
DATE	DESIGNED BY	DATE	DESIGNED BY
DEC 68	IN 3606		
DEC 30	DEC3009B	2N3009	
DEC 30	2N3639B	NGNE	

**digital** EQUIPMENT CORPORATION  
MAYNARD, MASSACHUSETTS

TITLE: ROM DIODE MATRIX M792  
SIZE: D CS NUMBER: M792-0-1 REV: D  
PRINTED CIRCUIT REV: [ ] [ ] [ ] [ ]



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 CAPACITORS ARE .01UF, 100V, 20%  
 RESISTORS ARE .2K, 1/4W, 5%  
 DIODES ARE D664  
 E2, E4, E6, E8, E10, E12, E14, E15, E16 = DEC380  
 E17 = DEC7400  
 E1, E3, E5, E7, E11 = DEC8881  
 E13 = DEC8242  
 E9 = DEC314  
 E18 - E22 = DEC8251  
 PIN 8 = +5V ON DEC380, DEC314  
 PIN 1 = GND  
 PIN 14 = +5V ON DEC8881, DEC8242, DEC7400  
 PIN 7 = GND  
 PIN 16 = +5V ON DEC8251  
 PIN 8 = GND  
 E19 - E22 PINS 6 AND 7 ARE NOT CONNECTED  
 E18 PINS 4, 5, 6, 7, 9 ARE NOT CONNECTED

REV	NO	DATE	BY	CHKD
1	1	10/28/70	B. Dyall	
2	1	11/2/70		

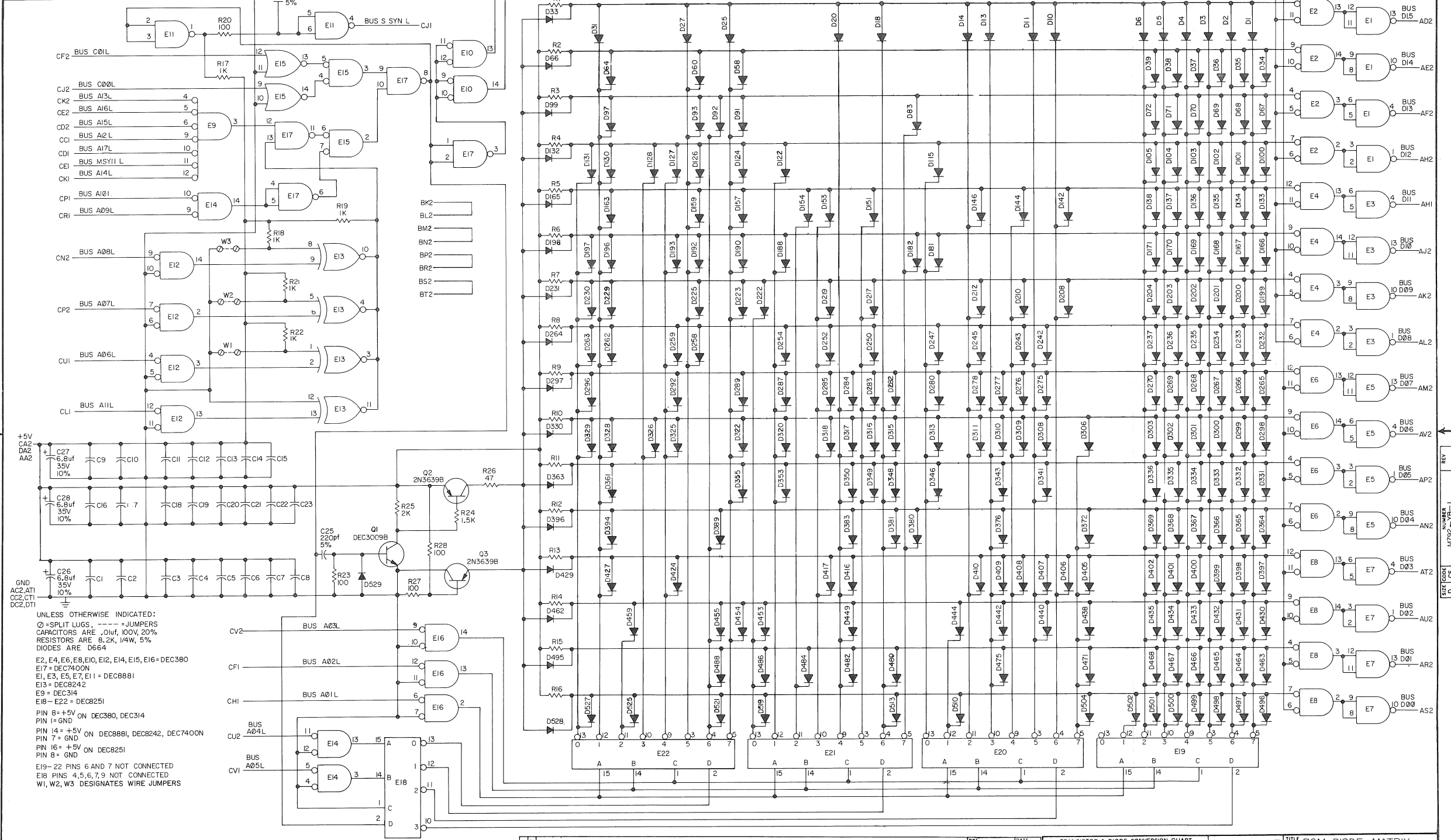
TRANSISTOR & DIODE CONVERSION CHART			
MANUFACTURER	TYPE	DIGITAL	MANUFACTURER
DEC	D664	IN3606	
DEC	DEC3009B	2N3009B	
DEC	2N3639B	SAME	

**digital** EQUIPMENT CORPORATION  
 TITLE: ROM DIODE MATRIX  
 NUMBER: M792YA  
 SIZE: D CS  
 CODE: M792-YA-1  
 NUMBER: H  
 PRINTED CIRCUIT REV: E





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 Q = SPLIT LUGS --- = JUMPERS  
 CAPACITORS ARE .01uf, 100V, 20%  
 RESISTORS ARE .8.2K, 1/4W, 5%  
 DIODES ARE D664

E2, E4, E6, E8, E10, E12, E14, E15, E16 = DEC380  
 E17 = DEC7400N  
 E1, E3, E5, E7, E11 = DEC8881  
 E13 = DEC8242  
 E9 = DEC314  
 E18 = E22 = DEC8251

PIN 8 = +5V ON DEC380, DEC314  
 PIN 1 = GND ON DEC380, DEC314  
 PIN 14 = +5V ON DEC8881, DEC8242, DEC7400N  
 PIN 7 = GND ON DEC8881, DEC8242, DEC7400N  
 PIN 16 = +5V ON DEC8251  
 PIN 8 = GND ON DEC8251

E19 - 22 PINS 6 AND 7 NOT CONNECTED  
 E18 PINS 4, 5, 6, 7, 9 NOT CONNECTED  
 W1, W2, W3 DESIGNATES WIRE JUMPERS

REV	DATE	BY	CHKD
1	8-25-70	W. MOORE	
2	11-17-71	M. MOORE	
3	1-10-76	D. MOORE	

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC380	IN3606	DEC380	IN3606
DEC309B	2N3019	DEC309B	2N3019
2N3639B	NONE	2N3639B	NONE

DATE	8-25-70	BY	W. MOORE
CHKD		DATE	11-17-71
DATE	1-10-76	BY	D. MOORE
DATE		DATE	

**digital**  
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 MAYNARD, MASSACHUSETTS

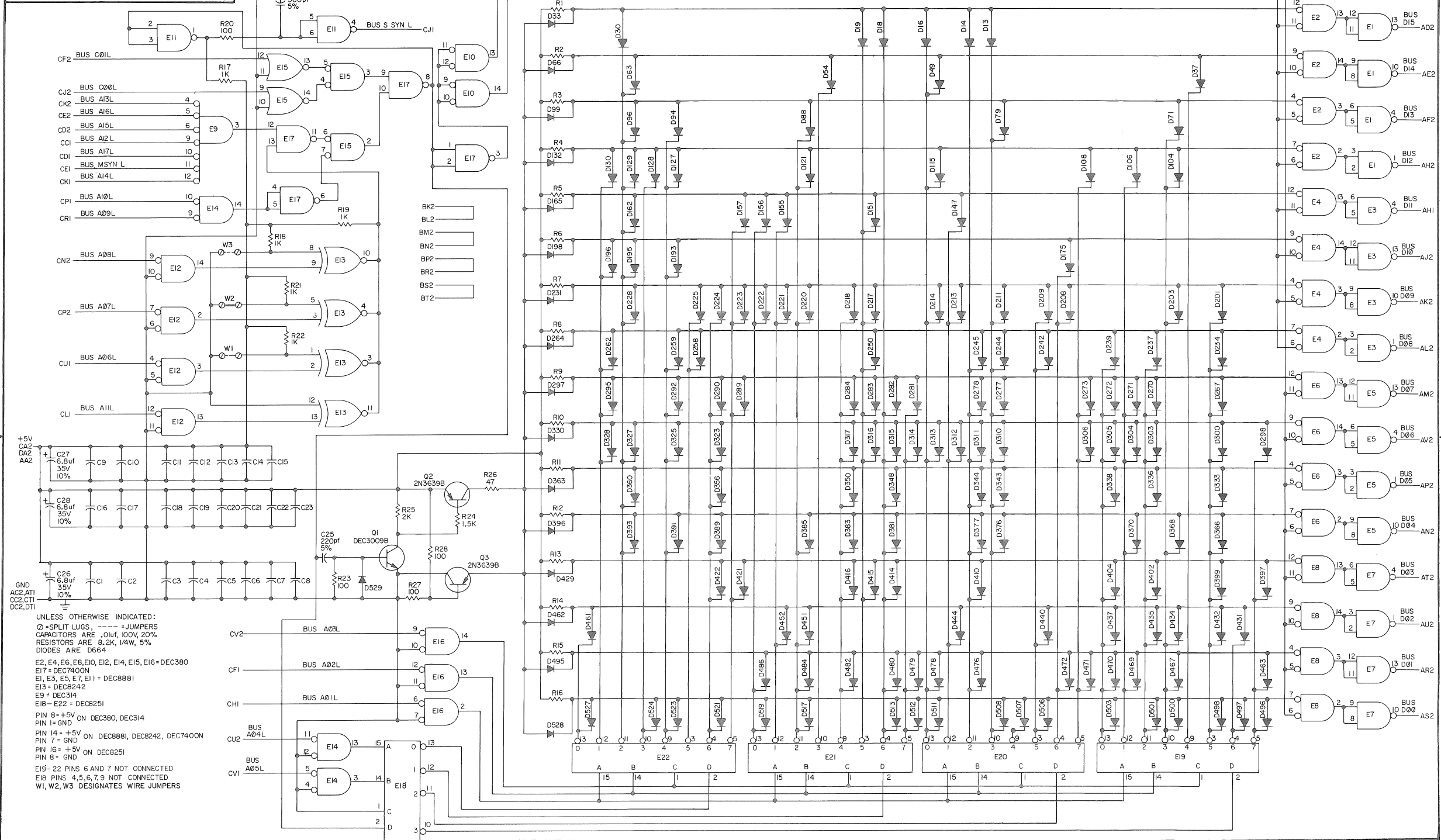
TITLE: ROM DIODE MATRIX

SIZE	CODE	NUMBER	REV
D	CS	M792-YB-1	

PRINTED CIRCUIT REV. [ ] [ ] [ ] [ ]



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CAPACITORS ARE .01uf, 100V, 20%  
RESISTORS ARE 0.2K, 1/4W, 5%  
DIODES ARE D664

E2, E4, E6, E8, E10, E12, E14, E15, E16 = DEC380  
E17 = DEC7400N  
E1, E3, E5, E7, E11 = DEC8881  
E13 = DEC8242  
E9 = DEC314  
E18 = E22 = DEC8251

PIN 8 = +5V ON DEC380, DEC314  
PIN 1 = GND  
PIN 14 = +5V ON DEC8881, DEC8242, DEC7400N  
PIN 7 = GND  
PIN 16 = +5V ON DEC8251  
PIN 8 = GND

E19 - 22 PINS 6 AND 7 NOT CONNECTED  
E18 PINS 4, 5, 6, 7, 9 NOT CONNECTED  
W1, W2, W3 DESIGNATES WIRE JUMPERS

REVISIONS  
DATE  
BY

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	IN3806		
DEC3009B	2N3009		
2N3639B	NONE		

**digital**  
EQUIPMENT CORPORATION  
MAYFORD, MASSACHUSETTS

TITLE: CARD READER BOOTSTRAP ROM  
SIZE: D CS  
NUMBER: M792-YC-1  
REV: E







## APPENDIX A

# BM792-YA PAPER-TAPE BOOTSTRAP LOADER

The BM792-YA ROM is shipped with jumper wires connected for address group 773000 - 773076, and its diode matrix is preprogrammed for a paper-tape bootstrap read-in-loader program. The BM792-YA can only be used in a PDP-11 System that has at least 4K of read-write memory and either a Teletype<sup>®</sup> (KL11) or a high-speed paper-tape reader (PR11 or PC11), or both. If neither the high-speed reader nor the low-speed reader (Teletype) is available, the paper-tape bootstrap loader program will not function properly.

An absolute loader or dump program contained on a bootstrap format paper tape (described in Chapter 5 of the *Paper-Tape Software Programming Handbook*, DEC-11-GGPA-D) is loaded into read-write memory by the paper-tape bootstrap loader. The sequence of operations used by the paper-tape bootstrap loader is:

1. Determines which paper-tape reader is available. Checks the high-speed reader first and then the low-speed reader. The high-speed reader is considered unavailable if no tape is in it.
2. Determines the size of the read-write memory of the system.
3. Stores the device address (determined in Step 1 above) in the last location of read-write memory. This action is required by the absolute loader program.
4. Loads the absolute loader program from the bootstrap format tape into the read-write memory.
5. Jumps to program loaded, as specified on the bootstrap format tape.

The paper-tape bootstrap loader program and the absolute loader program require the use of 96 locations at the high end of the read-write memory. Memory locations 4, 14, 16, 20, and 22 are modified during the operation of the paper-tape bootstrap loader program. Also, the illegal memory reference (bus time-out) trap at location 4 is used extensively by this loader.

A program listing for the paper-tape bootstrap loader is provided in Table A-1. Hardware addresses in the PDP-11 use 18 bits with the result that bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler program uses 16-bit addresses so that only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table A-1 are listed as 173XXX instead of 773XXX.

The operating procedure for loading a bootstrap format paper tape with the paper-tape bootstrap loader is:

Step	Procedure
1	Set the HALT/ENABLE switch to HALT, then to ENABLE.
2	Place the bootstrap format paper tape in the reader to be used, with the special tape leader placed over the read head.
3	If the high-speed reader is to be used, set the switch to ON.

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<sup>®</sup> Teletype is a registered trademark of Teletype Corporation.

Step	Procedure
4	If the low-speed reader is to be used, set the high-speed reader switch to OFF and set the low-speed reader switch to START.
5	Set the starting address, 773000, into the SWITCH REGISTER.
6	Depress the LOAD ADDR switch.
7	Depress the START switch. After a short pause, the paper tape should read in.



Table A-1  
BM792-YA Paper-Tape Bootstrap Loader Program

		IREG, STEPS USED		R1, R2, R3, R4, SP	
000001				R1=X1	; ADDRESS POINTER
000002				R2=X2	; TEMPORARY STORAGE
000003				R3=X3	; TEMPORARY STORAGE
000004				R4=X4	; DEVICE POINTER
000006				SP=X6	; STACK POINTER
000007				PC=X7	; PROGRAM COUNTER
177550				HSR=177550	; HIGH SPEED READER ADDRESS
177560				LSR=177560	; LOW SPEED READER ADDRESS
173000	012701	160000		START: MOV #160000, R1	; SET MEMORY CHECK LIMITS
173004	012702	000006		MOV #0, R2	; TRAP VECTOR IS LOCATION 4/6
173010	012703	173100		MOV #DEV+4, R3	; POINTER TO DEVICE ADDRESSES
173014	005012			CLR @R2	; CLEAR TRAP STATUS AT LOCATION 6
173016	010742			MOV PC, @(R2)	; SET TRAP ADDRESS IN LOCATION 4
173020	110706			MOV B PC, SP	; SET UP STACK OUT OF THE WAY
173022	014304			DEV1: MOV @(R3), R4	; GET DEVICE ADDRESS
173024	205714			TST @R4	; CHECK AVAILABILITY OF DEVICE
173026	100775			BMI DEV1	; BRANCH IF HSR IS OUT OF TAPE (BIT 15)
173030	010712			MOV PC, @R2	; RESET TRAP ADDRESS AT LOCATION 4
173032	012706	000024		MOV #24, SP	; SPECIAL ADDRESS USED AS MASK LATER
173036	010441			MOV R4, @(R1)	; DO MEM CHKI READER STATUS ADDRESS IS MOVED
173040	040601			BIC SP, R1	; SET R1=X7752, MASK IN SP=24
173042	010111			MOV R1, @R1	; STORE OWN ADDRESS IN POINTER
173044	011102			LOOP1: MOV @R1, R2	; GET BYTE POINTER
173046	005214			INC @R4	; ENABLE READER
173050	105714			TSTB ,=2	; TEST DONE BIT (BIT 07)
173052	100376			BPL ,=2	; WAIT UNTIL READY
173054	116412	000002		MOV B 2(R4), @R2	; THEN PICK IT UP AND STORE IT
173060	005211			INC @R1	; BUMP POINTER
173062	120227	000375		CMPB R2, #375	; STORED JUMP OFFSET?
173066	001366			BNE LOOP	; NOT YET
173070	105222			INCB (R2)+	; YES, ALL DONE
173072	000142			JMP =(R2)	; GO EXECUTE AS BRANCH
; DEVICE ADDRESSES FOLLOW = DO NOT CHANGE THE ORDER					
173074	177560		DEV1:	LSR	; LOW SPEED READER
173076	177550			HSR	; HIGH SPEED READER



## APPENDIX B

# BM792-YB BULK STORAGE BOOTSTRAP LOADER

The BM792-YB ROM is shipped with jumper wires connected for address group 773100-773176, and its diode matrix is preprogrammed for a bulk storage (disk or DECTape) bootstrap loader program. The BM792-YB is used in a PDP-11 System that has at least 4K of read-write memory and one or more mass storage devices, such as disk or DECTape.

The actual bootstrap loader program, stored in the first 256 words of a disk or DECTape, is transferred from the device into read-write memory by the BM792-YB program. The transfer is started from location 0 of the device, and the loaded routine is assumed to be operative at read-write memory location 0. The BM792-YB program jumps to location 0 after a satisfactory completion of the transfer, so that there is automatic starting of the actual bootstrap loader program. If error conditions occur during the running of the BM792-YB program, the program starts over again.

The sequence of operations used by the bulk storage bootstrap loader is as follows:

1. It determines whether the device is a disk or DECTape from the address set in the SWITCH REGISTER.
2. If the device is a DECTape transport, it moves the tape until the front endzone is sensed.
3. It reads 256 words stored in the device, starting with address 0 of the device.
4. The loader then stores the 256 words in read-write memory sequential locations, starting with location 0.
5. The loader checks for errors and starts the program over if any errors occur.
6. The loader then jumps to read-write memory location 0 for automatic starting of the actual bootstrap loader program.

A program listing for the bulk storage bootstrap loader is provided in Table B-1. Hardware addresses in the PDP-11 use 18 bits; thus, bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler uses 16-bit addresses; consequently, only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table B-1 are listed as 173XXX instead of 773XXX.

The operating procedure for use of the BM792-YB bulk storage bootstrap loader is as follows:

Step	Procedure
1	Set the HALT/ENABLE switch to HALT, then to ENABLE.
2	Set the ROM address, 773100, into the SWITCH REGISTER.
3	Depress the LOAD ADDR switch.

(continued on next page)

## Step

## Procedure

- 4 Set the address of the word count register of the disk or DECTape to be used into the SWITCH REGISTER. The standard addresses for the word count registers of the DEC devices are as follows:

RC11 Disk	777450
RF11 Disk	777462
RK11 Disk	777406
RP11 Disk	776716
TC11 DECTape	777344

- 5 Depress the START switch. The disk or DECTape data should then read into the read-write memory.

Table B-1  
BM792-YB Bulk Storage Bootstrap Loader Program

```

; REGISTER ASSIGNMENTS:
000000 R0=%0
000001 R1=%1
;
173100 013701      MOV      @#177570,R1      ;READ SWITCH REG FOR ....
          177570
173104 000005-    BEGIN:  RESET          ;FORCE CLEAR IF RETRY
173106 010100      MOV      R1,R0          ;...DEVICE WC ADDRESS
173110 012710      MOV      #-256.,@R0     ;SET TO READ 256 WORDS
          177400
173114 020027      CMP      R0,#177344     ;IS IT DECTAPE?
          177344
173120 001007      BNE      START.        ;NO. GO TO START
173122 012740      MOV      #4002,-(R0)    ;YES. MOVE TAPE TO FRONT
          004002
173126 005710      TST      @R0          ;WAIT FOR ERROR!
173130 100376      BPL      .-2
173132 005740      TST      -(R0)        ;IS IT ENDZONE?
173134 100363      BPL      BEGIN        ;NO. TRY AGAIN
173136 022020      CMP      (R0)+,(R0)+   ;ADJUST POINTER
173140 012740      START:  MOV      #5,-(R0) ;NOW START ACTUAL READ
          000005
173144 105710      TSTB     @R0          ;WAIT FOR DONE
173146 100376      BPL      .-2
173150 005710      TST      @R0          ;ERROR ENCOUNTERED?
173152 100754      BMI      BEGIN        ;IF SO START OVER
173154 105010      CLRB     @R0          ;FOR DECTAPE,STOP TRANSPORT
173156 000137      JMP      @#0          ;GO TO ROUTINE LOADED
          000000
          000001      .END

BEGIN      000004R      R0      =%000000      R1      =%000001
START      000040R      .        = 000062R

```

## APPENDIX C

### BM792-YC CARD READER BOOTSTRAP LOADER

The BM792-YC ROM is shipped with jumper wires connected for address group 773200-773276. Its diode matrix is preprogrammed for loading binary data into the PDP-11 memory from cards using the CR11 or CM11 Card Reader. If the data represents a PDP-11 program, the program can be automatically started upon completion of loading. The BM792-YC is used in PDP-11 Systems that have at least 4K of read-write memory and a card reader.

On the card that is read, each pair of columns (column 1 and column 2; 3 and 4; etc.) beginning with column 1 contains two 8-bit bytes which represent one 16-bit word. Also a control bit can be contained in the second column of a pair. The eight bits that represent each byte are punched or marked in rows 2 through 9 of each column.

The first column of a pair contains the high-order byte (PDP-11 bits 15-8) of the word and the second column of the pair contains the low-order byte (PDP-11 bits 7-0) of the word. A control bit punched or marked in row 0 of the second column of a pair designates that the word in those two columns is a new Loading Address. Each Loading Address must be equal to zero modulo two because loading must begin at a word boundary in memory rather than a byte boundary. Loading is accomplished one word at a time, thus a new Loading Address can appear anywhere on the card. However, a Loading Address must be in the first two columns of the first card read.

The absence of control bits in rows 12, 11, 1, and 0 of the second column of a pair designates the word as a Data Word to be loaded into the PDP-11 memory. The Data Word can represent a machine instruction or data. After each Data Word is loaded into memory the current loading address is incremented by two.

A control bit in row 1 of the second column of a pair designates the word as a Transfer Address. When a Transfer Address is read, the bootstrap program issues a RESET and branches to the Transfer Address. The card which contains the Transfer Address passes through the card reader, but no other Loading Addresses or Data Words are read from it.

A program listing for the card reader bootstrap loader is provided in Table C-1. Hardware addresses in the PDP-11 use 18 bits; thus, bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler uses 16-bit addresses; consequently, only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table C-1 are listed as 173XXX instead of 773XXX.

The operating procedure for use of the BM792-YC card reader bootstrap loader is as follows:

Step	Procedure
1	Set the HALT/ENABLE switch to HALT, then to ENABLE.
2	Load the input hopper of the card reader with the cards to be read.
3	On the card reader set the MODE switch to REMOTE.
4	On the card reader depress the RESET switch and observe that the associated green indicator lights. The card reader is now on-line.
5	Set the starting address, 773200, into the switch register.
6	Depress the LOAD ADDR switch.
7	Depress the START switch. After a short pause, the card reader should read the data on the cards into the computer memory.

Table C-1  
 BM792-YC Card Reader Bootstrap Loader Program

1					
2					
3					
4	173200				
5	000400				
6	001000				
7	040000				
8	000000				
9	000001				
10	000002				
11	000003				
12	000004				
13	000007				
14	177160				
15					
16	173200	000005			
17	173202	012700	177160		
18	173206	010001			
19	173210	032701	001400		
20	173214	001371			
21	173216	005210			
22	173220	005003			
23	173222	005004			
24	173224	031027	040000		
25	173230	001372			
26	173232	105710			
27	173234	100373			
28	173236	000303			
29	173240	151103			
30	173242	005104			
31	173244	100772			
32	173246	121751	000001		
33	173252	001425			
34	173254	003002			
35	173256	010302			
36	173260	000757			
37	173262	010322			
38	173264	000755			
39	173266	031027	040000		
40	173272	001775			
41	173274	000005			
42	173276	000113			
43		000001			

BIT06	000400
BIT09	001000
BIT14	040000
CRS	177160
DATA	173262
NEXTC	173216
NEXTV	173220
PC	000007R
R0	000000R
R1	000001R
R2	000002R
R3	000003R
R4	000004R
START	173200
TESTCD	173224
TRANSF	173246
WAITC	173232





## APPENDIX D

### MR11-DB BULK STORAGE BOOTSTRAP LOADER

The MR11-DB is a 64-word bootstrap loader for the following bulk storage control devices: RF11, RK11, TC11, TM11, RP11, and RC11. This option can be used in any PDP-11 system. It includes a feature of special value to PDP-11/45 systems that are equipped with MS11 Semiconductor Memory (MOS or bi-polar) Systems. On those PDP-11/45 systems, the KB11-A start vector for power up can be selected for bootstrap load from any of the above-listed devices, except the TM11, which loses vacuum on power fail.

The MR11-DB option consists of two programmed ROM diode matrix modules. The M792-YD ROM Diode Matrix stores the first 32 words of the bootstrap loader program at addresses 773100-773176. The M792-YE ROM Diode Matrix stores the second 32 words of the bootstrap loader program at addresses 773200-773276.

Table D-1 is a program listing of the MR11-DB Bootstrap Loader program that is encoded on the two ROM diode matrix modules. PDP-11 hardware addresses use 18 bits. The software assembler uses 16-bit addresses. Therefore, the addresses listed in Table D-1 are listed as 173XXX, instead of 773XXX.

#### KEY START LOADING

Operate the MR11-DB Bulk Storage Bootstrap Loader as follows:

1. Set the HALT/ENABL switch to HALT, then to ENABL.
2. Set the console switches to the starting address assigned to the selected bulk storage device control, as listed in Table D-2.
3. Press LOAD ADRS.
4. Press START.

The processor will start executing the bulk storage bootstrap loader program at the selected address. The program loads the first 512 words from unit 0 into memory, starting at memory location 0. After the bootstrap is loaded from the bulk storage device, the loader program causes the processor to start executing the bootstrap at location 0.

#### NOTE

**When magnetic tape is the bulk storage medium, magnetic drive unit 0 must be selected and positioned at the load point.**

**Loading from Disks** — The program starts at the selected address, then branches to a common routine that resets all Unibus devices. Thus, disk address registers and current memory address registers are initialized to 0. The pointer to the device's word count register is located in R1. Then, the word count register is loaded with the 2s

complement of 512. The device command to read and go is issued to the device command register. As the 512-word record is read into memory from the disk, the loader program checks for errors. If an error is detected, the entire routine is repeated, starting at the selected address. When no errors are detected and the last word has been transferred, the PC is cleared, and the bootstrap is executed, starting at memory location 0.

**Loading from Tapes** – The program starts at the selected address for DECtape or magtape; then branches to a common tape routine which first resets all the device registers. Then, the device's word count register (or byte count) is decremented by one. If the routine is entered from the TC11 address, a first command is issued to rewind the DECtape to the forward end zone. If the routine is entered from the TM11 address, a first command is issued to advance the magnetic tape one record. After the specified operation is done and checked for errors, the program branches to the common disk loading routine that reads a 512-word record into memory from the selected tape storage device.

### POWER UP LOADING

The MR11-DB provides for automatically loading a bootstrap program from a pre-selected bulk storage device during the power up sequence. This feature is provided for PDP-11/45 systems with MOS or bipolar memory and no power backup. The KB11-A Central Processor Unit in those systems has a start vector jumper field located on DAP module M8100. Table D-3 lists the start vector jumper connections required to select the specific MR11-DB starting address for each type of bulk storage device.

### START VECTOR PROGRAM OPERATION

The start vector jumpers on the DAP module select bits SV(07:00) of the start vector. Bits SV(01:00) are always 0. High-order bits of the starting address are generated by CPU sign-extension logic, blocking bits 11 and 8. A hard-wired address 773XXX with the SV(07:00) offset is generated. The power up sequence uses the resultant address to load the PC and PS from the address pointed to by the start vector.

For example, jumper selection of the RK11 provides start vector 260. The resultant address, 173260, accesses a location provided by the MR11-DB, to load the PC with starting address 173110 and the PS with 000340. The bulk storage program loader proceeds to load a bootstrap from the RK11, with the CPU operating at priority level 7, which prevents external devices from interrupting the program.

### INSTALLATION

**PDP-11/45 Systems** – Install the M792-YD and M792-YE modules that comprise the MR11-DB option in two of the three spaces reserved on the CPU backplane for small peripheral controllers. The quad-height slots are designated 26, 27, and 28. Refer to Table D-3 and remove jumpers W1 through W6, as required, from the DAP module to select the bulk storage device that is to provide the bootstrap program during power up.

#### NOTE

**The TM11 must be restarted manually, with the tape drive positioned at the load point. Therefore, power up start vector selection is not provided.**

**Other PDP-11 Systems** – Install the MR11-DB modules on a DD11-A Peripheral Mounting Panel that is connected to the Unibus by an M920 Unibus Connector module.

Table D-1  
MR11-DB Bulk Storage Program Loader Listing

173100	010702	RF11:	MOV	%7,%2	;FIXED HEAD DISK (256KW)
173102	000451		RR	OTHER	
173104	177462			177462	
173106	000005			5	
173110	010702	RK11:	MOV	%7,%2	;MOVING HEAD DISK (CARTRIDGE)
173112	000445		BR	OTHER	
173114	177406			177406	
173116	000005			5	
					;COMMAND WORD
173120	010702	TC11:	MOV	%7,%2	;ADRS OF WORD COUNT ;LAST COMMAND ;FIRST COMMAND ;DONE MASK ;ERROR MASK
173122	000417		BR	TAPES	
173124	177344			177344	
173126	000005			5	
173130	004003			4003	
173132	100000			100000	
173134	024000			24000	
173138	010702	TM11:	MOV	%7,%2	
173140	000410		BR	TAPES	
173142	172524			172524	
173144	060003			60003	
173146	060011			60011	
173150	000200			200	
173152	100000			100000	
173154	010702	RP11:	MOV	%7,%2	;MOVING HEAD DISK (PACK)
173156	000423		BR	OTHER	
173160	176716			176716	
					;COMMAND WORD (5) IS THE RESET
173162	000005	TAPES:	RESET		
173164	010200		MOV	%2,%0	;GET THE ADDRESS OF THE BRANCH
173166	005720		TST	(0)+	;%0 TO POINT AT LAST COMMAND
173170	012001		MOV	(0)+,%1	;GET THE WORD COUNT ADDRESS
173172	005311		DEC	(1)	;SET UP FOR ADVANCE 1 RECORD
173174	005720		TST	(0)+	;MOVE %0 TO FIRST COMMAND
173176	012041		MOV	(0)+,-(1)	;COMMAND WORD TO COMMAND REG.
173200	031011		BIT	(0),(1)	;LOOK FOR DONE INDICATORS
173202	001776		SEQ	,-2	;NONE SET, TRY AGAIN
173204	005720		TST	(0)+	;DONE FIRST COMMAND, CHECK FOR ERROR
173206	031041		RIT	(0),-(1)	;LOOK FOR SET ERROR BITS
173210	001406		BEQ	OTHER	;NO ERRORS = TRY THE READ
173212	000112	AGAIN:	JMP	(2)	;RERUN FOR ERRORS
173214	173100	RFVEC:	RF11		;RF11 POWER UP VECTOR
173216	000340			340	
173220	010702	RC11:	MOV	%7,%2	;FIXED HEAD DISK (64KW)
173222	000401		BR	OTHER	
173224	177450			177450	
					;ADRS OF WORD COUNT (COMMAND*2) ;COMMAND WORD (5) IS THE RESET
173228	000005	OTHER:	RESET		
173230	010200		MOV	%2,%0	;%0 TO POINT AT WORD COUNT ADRS
173232	005720		TST	(0)+	;POINT TO ADDRESS
173234	012001		MOV	(0)+,%1	;WORD COUNT ADRS TO %1
173236	012711	177000	MOV	#-1000,(1)	;LOAD WORD COUNT
173240	011041		MOV	(0),-(1)	;COMMAND TO COMMAND REGISTER
173244	032711	100200	BIT	#100200,(1)	;CHECK FOR ERROR OR DONE
173250	001775		BEQ	,-4	;IF NEITHER, KEEP LOOKING
173252	100757		BMI	AGAIN	;ERROR, TRY AGAIN
173254	005007		CLR	%7	
173258	000000			0	;FILLER
173260	173110	RKVEC:	RK11		;RK11 POWER UP VECTOR
173262	000340			340	
173264	173220	RCVEC:	RC11		;RC11 POWER UP VECTOR
173266	000340			340	
173270	173154	RPVEC:	RP11		;RP11 POWER UP VECTOR
173272	000340			340	
173274	173120	TCVEC:	TC11		;TC11 POWER UP VECTOR
173276	000340			340	
	000001				.END

**Table D-2**  
**Starting Address**

Bulk Storage Device Control	Starting Address (octal)
RF11 (for RS11 DECdisk)	773100
RK11 (for RK02 DECpack)	773110
TC11 (for TU56 DECtape)	773120
TM11 (for TU10 Magtape)	773136
RP11 (for RP02 Disk Pack)	773154
RC11 (for RS64 DECdisk)	773220

**Table D-3**  
**Power Up Start Vector Jumper Connections**

Bulk Storage Control Device	Power Up Vector Address	Jumpers on DAP Module					
		W1	W2	W3	W4	W5	W6
RF11	773214	In	In	Out	Out	Out	In
RK11	773260	Out	Out	In	In	Out	In
TC11	773274	In	In	In	In	Out	In
TM11	None	—	—	—	—	—	—
RP11	773270	Out	In	In	In	Out	In
RC11	773220	Out	Out	In	Out	Out	In

## MAINTENANCE

Diagnostic program MAINDEC-11-DZMRA-D is provided with the MR11-DB Bulk Storage Bootstrap Loader option. The diagnostic program can be used to troubleshoot and maintain the MR11-DB hardware. The available tests are:

- PRG0: Logic Tests
- PRG1: ROM data dump
- PRG2: Single ROM address read data loop

These tests can also be used to check data reliability and as a post-installation checkout procedure. Complete operating procedure is described in the MAINDEC description supplied as part of the diagnostic program package.

Module schematics, parts lists, and component location drawings for the M792-YD and M792-YE ROM Diode Matrix modules are located in the MR11-DB engineering drawing set. Module Schematics of the two modules are also provided in Chapter 4 of this manual.

# APPENDIX E

## BM792-YF BULK STORAGE BOOTSTRAP LOADER

The BM792-YF ROM is shipped with jumper wires connected for address group 773200-773276, and its diode matrix is preprogrammed for a bulk storage (disk or DECTape) bootstrap loader program. The BM792-YF can only be used on a PDP-11 System that has at least 4K of read-write memory and one or more mass storage devices, such as a disk or DECTape.

The actual bootstrap loader program, stored in the first 256 words of a disk or DECTape, is transferred from the device into read-write memory by the BM792-YF program. The transfer is started from location 0 of the device, and the loaded routine is assumed to be operative at read-write memory location 0. The BM792-YF program jumps to location 0 after a satisfactory completion of the transfer, so that there is automatic starting of the actual bootstrap loader program. If error conditions occur during the running of the BM792-YF program, the program starts over again.

The sequence of operations used by the bulk storage bootstrap loader is as follows:

1. It determines whether the device is a disk or DECTape from the address set in the Switch register.
2. If the device is a DECTape transport, it moves the tape until the front endzone is sensed.
3. It reads 256 words stored in the device, starting with address 0 of the device.
4. The loader then stores the 256 words in read-write memory sequential locations, starting with location 0.
5. The loader checks for errors and starts the program over if any errors occur.
6. The loader then jumps to read-write memory location 0 for automatic starting of the actual bootstrap loader program.

A program listing for the bulk storage bootstrap loader is provided in Table E-1. Hardware addresses in the PDP-11 use 18 bits; thus, bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler uses 16-bit addresses; consequently, only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table E-1 are listed as 173XXX instead of 773XXX.

The operating procedure for use of the BM792-YF bulk storage bootstrap loader is as follows:

Step	Procedure
1	Set the HALT/ENABLE switch to HALT, then to ENABLE.
2	Set the ROM address, 7732XX, into the Switch register.
	XX      Equipment
	00      RK11 Disk
	06      RF11 Disk
	14      TC11 DECTape

(continued on next page)

## Step

## Procedure

- 3 Depress the LOAD ADDR switch.
- 4 Depress the START switch. The disk or DECTape data should then read into the read-write memory.

Table E-1  
BM792-YF Bulk Storage Bootstrap Loader Program

			REGISTERS USED		
	000000		R0=%0		
	000001		R1=%1		
173200	012701	177406	RKBOOT:	MOV #177406,R1	;SET UP RK11 ADDRESS
173204	000405			BR BEGIN	
173206	012701	177402	RFBOOT:	MOV #177402,R1	;SET UP RF11 ADDRESS
173212	000402			BR BEGIN	
173214	012701	177344	DTBOOT:	MOV #177344,R1	;SET UP DECTAPE ADDRESS
173220	000005		BEGIN:	RESET	
173222	010100			MOV R1,R0	;SET WORD COUNT
173224	012710	177400		MOV #-256,,R0	;TO READ 256 WORDS
173230	020027	177344		CMP R0,#177344	;IS THIS DECTAPE BOOT?
173234	001007			HNE START	;IF NOT, SKIP SEARCH CODE
173236	012740	004002		MOV #4002,=(R0)	;SEARCH BACKWARD
173242	005710			TST R0	;LOOP UNTIL
173244	100376			BPL ,=2	;ERROR FLAG
173246	005740			TST =(R0)	;IF NOT 'END ZONE',
173250	100363			BPL BEGIN	;TRY AGAIN
173252	022020			CMP (R0)+,(R0)+	;RESET R0
173254	012740	000005	START:	MOV #5,=(R0)	;ISSUE READ COMMAND
173260	105710			TSTB R0	;LOOP UNTIL
173262	100376			BPL ,=2	;READY
173264	005710			TST R0	;IF ERROR,
173266	100754			BMI BEGIN	;TRY AGAIN
173270	000005			RESET	;STOP ANY TAPE MOTION
173272	000137	000000		JMP R0	;GO TO THE BOOT

## APPENDIX F

# BM792-YH CASSETTE BOOTSTRAP LOADER

The BM792-YH ROM is shipped with jumper wires connected for address group 773300-773376, and its diode matrix is preprogrammed for a tape cassette (TA11/TU60 Cassette System) bootstrap loader program. This quad-sized module is one of the Small Peripheral Controllers (SPC) and can be mounted in any SPC slot in a DD11-A, DD11-B, or most PDP-11 family processors. Any PDP-11 System that has 4K of read-write memory and a cassette can use the BM792-YH.

The actual bootstrap loader program, stored in the first 128 bytes of a cassette tape, is transferred from the cassette into read-write memory by the BM792-YH program. The bytes are consecutively read from the cassette and loaded into memory locations 0 through 177 (octal). When the loading is complete, program control is transferred to location 0 so that the loaded program can be executed. At the point when the program control is transferred, the cassette is positioned at the end of the second block of the first file so that the loaded program can continue to read in additional data.

The sequence of operations used by the cassette bootstrap loader is as follows:

1. The cassette is rewound and then spaced forward one block. This action skips the header block (normally 32 bytes) associated with the first file and positions the tape at the second block of the first file.
2. The BM792-YH program consecutively reads 128 bytes from the cassette tape into read-write memory locations 0 through 177 (octal).
3. The first byte read is compared to octal 240 (NOP) and if it does not equal octal 240, the program comes to a halt at location 173350. To restart the program from this halt, the CONT switch is depressed.
4. After the 128 bytes are read, the loader program checks the TA11 error bit (block check error, off-line error, etc.) and if an error is detected, the program comes to a halt at location 173350 and can be restarted by depressing the CONT switch.
5. If no error is detected, program control is transferred to location 0 to execute the loaded program.

A program listing for the cassette bootstrap loader is provided in Table F-1. Hardware addresses in the PDP-11 use 18 bits; thus, bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler uses 16-bit addresses; consequently, only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table F-1 are listed as 173XXX instead of 773XXX.

The BM792-YH program has no provisions for initializing the system since it does not issue a RESET instruction. Initialization is necessary because other devices may issue interrupts or an internal processor option may be enabled. When the BM792-YH program is started from the console, initialization is performed because the START





switch initializes the system prior to starting. However, if the BM792-YH program is started by a program transferring control to location 173300, then that program must issue a RESET instruction prior to the JMP 173300.

Normally, the PDP-11 processor's power-up vector is address 24/26; however, processors such as the PDP-11/40 and PDP-11/45 have jumper selectable power-up vectors that allow the vector address to be set to an address within a restricted range in the highest 4K-words of Unibus address. The power-down vector remains at 24/26.

The BM792-YH provides a power-up vector at address 173374/6. When the power-up trap sequence executes with a vector address set to 173374/6, program execution begins at 173300 with a priority level of 7.

The operating procedure for use of the BM792-YH cassette bootstrap loader when the cassette is operating from cassette unit number 0 at the standard octal address of 777500 is as follows:

Step	Procedure
1	Write-lock the cassette for security.
2	Mount the cassette in cassette unit number 0 (left-hand drive unit on the TU60).
3	Set the HALT/ENABLE switch to HALT, then to ENABLE.
4	Set the ROM address, 773300, into the Switch register.
5	Depress the LOAD ADDR switch.
6	Depress the START switch. The cassette data should then read into the read-write memory.

The operating procedure to bootstrap load from cassette unit number 1 or from a cassette unit other than one at the standard octal address of 777500 is as follows:

Step	Procedure
1	Write-lock the cassette for security.
2	Mount the cassette in the selected unit.
3	Set the HALT/ENABLE switch to HALT, then to ENABLE.
4	Set the R0 address, 777700, into the Switch register.
5	Depress the LOAD ADDR switch.
6	Set the address of the cassette unit into the Switch register.
7	Depress the DEP switch. This loads R0 with the address of the cassette unit.
8	With the Switch register still set at the address of the cassette unit, depress LOAD ADDR switch.
9	Set the octal designation for the cassette unit number into Switch register (000 for unit number 0 or 400 for unit number 1).
10	Depress the DEP switch. This establishes bit 08, the Unit Select bit, of the TA11 Command and Status register.
11	Set the R7 address, 777707 into the Switch register.
12	Depress the LOAD ADDR switch.

(continued on next page)

**Step****Procedure**

- 13 Set 773306 into the Switch register.
- 14 Depress the DEP switch. This sets the PC to the BM792-YH restart address.
- 15 Depress the CONT switch. This starts the processor without system initialization. When started at address 773306, the BM792-YH program uses R0 to reference the cassette registers but does not modify R0 or the Unit Select bit.
- When the 128-byte program is loaded from the cassette into the read-write memory, this 128-byte program determines whether read-in will continue from this same cassette. R0 and the Unit Select bit can be modified by the loaded program so that a different cassette can be accessed for loading.

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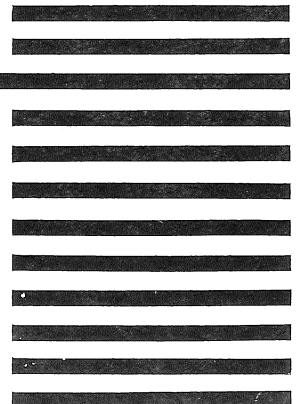
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