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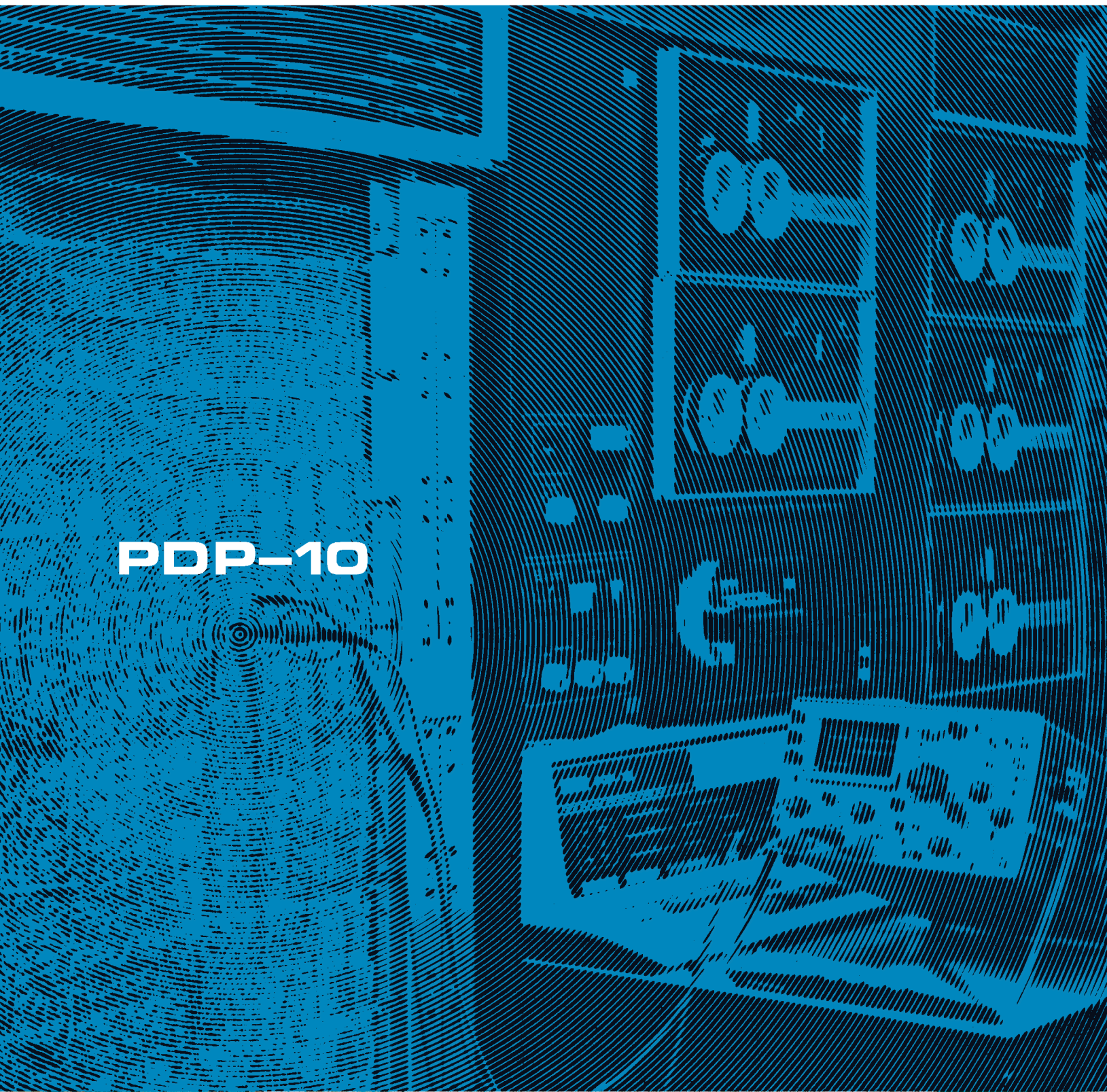
RC10 DISK SYNCHRONIZER-ADAPTER



DEC-10-I5AA-D

RC10 DISK SYNCHRONIZER-ADAPTER

INSTRUCTION MANUAL

April 1968

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 INTRODUCTION

The RC-10 Disk Synchronizer-Adapter controls the operation of a maximum of four RD-10 Disk Files (Figure 1-1). The RC-10 Synchronizer uses the facilities of the DF-10 Data Channel to transfer data between the RD-10 Disk File and the PDP-10 central processor memory. Standard PDP-10 I/O instructions initiate and monitor the operation of the synchronizer.

The RD-10 Disk File has a storage capacity of 512,000, 36-bit words. The transfer rate is approximately 76,000 words-per-second (13 μs per word). The disk file contains 200 tracks of data. Each track contains 80 addressable segments with each segment containing 32 36-bit words. When recording, the 36-bit word is disassembled into 6-bit characters which are then written onto the addressed track and segment. Each segment is approximately 400 μs long. The disk makes one revolution in approximately 34 ms; therefore, the average access time to any segment is approximately 17 ms. Since each segment contains 32 words, the smallest record that can be written is 32 words.

This manual provides a complete description of operation, programming, theory, and maintenance of the RC-10 Synchronizer. The level of discussion assumes familiarity with the PDP-10 Programmed Data Processor and a working knowledge of DEC logic symbology. The RD-10 Disk File and the DF-10 Data Channel are described in separate manuals and will only be discussed to the extent necessary to understand the operation of the RC-10 Synchronizer.

1.2 PHYSICAL SPECIFICATIONS

Line Current	4 amps (nominal)
Power Dissipation	500W
Heat Dissipation	1700 Btu
Dimensions	69 in. high 19-3/4 in. wide 27 in. deep
Service Clearance	36 in. front and rear
Weight	350 lbs
Operating Temperature	60°F min. 100°F max.
Storage Temperature	40°F min. 100°F max.
Relative Humidity	20% min. 80% max.

Maximum Wet Bulb	78°F
Signal Cable Length	100 ft Channel Bus 150 ft I/O Bus

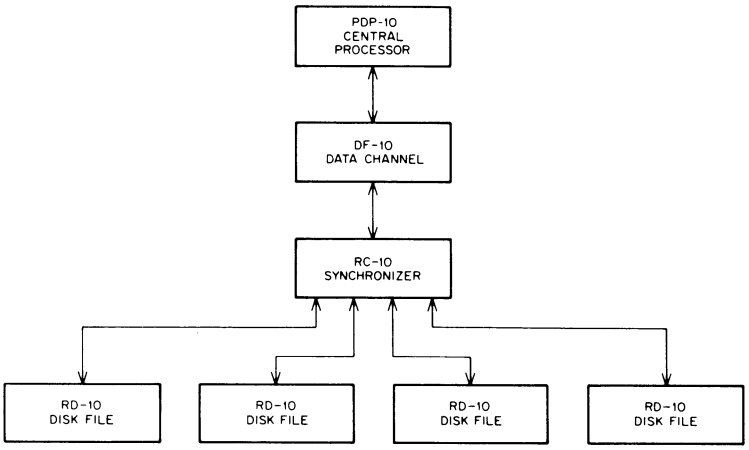

Figure 1-1 Typical RC-10 System

CHAPTER 2
OPERATION AND PROGRAMMING

2.1 INTRODUCTION

The RC-10 Synchronizer operates under the control of the DF-10 Data Channel to transfer data between the RD-10 Disk File and core memory. The RC-10 controls the operation of as many as four RD-10 Disk Files; however, only one disk file is controlled at any one time. Each disk file has a storage capacity of 512,000 36-bit words. The transfer rate is approximately 76,000 words-per-second (13 μs per word).

The disk file contains 200 tracks of data. Each track contains 80 addressable segments with each segment containing 32 36-bit words. When recording, the 36-bit word is disassembled into 6-bit characters which are then written in parallel onto the addressed track and segment. Each segment is approximately 400 μs long. The disk makes one revolution in approximately 34 ms; therefore, the average access time to any segment is approximately 17 ms. Since each segment contains 32 words, the smallest record that can be written is 32 words.

The computer initializes the synchronizer operation when it issues the DATAO 170 instruction. Thereafter, the synchronizer operates under the control of the DF-10 Data Channel to transfer data to or from memory. For the following discussion, it is assumed that the reader is familiar with the programmed operation of the DF-10.

2.2 CONTROLS AND INDICATORS

Figure 2-1 shows the indicator panel, Table 2-1 lists the front panel controls and defines their function.

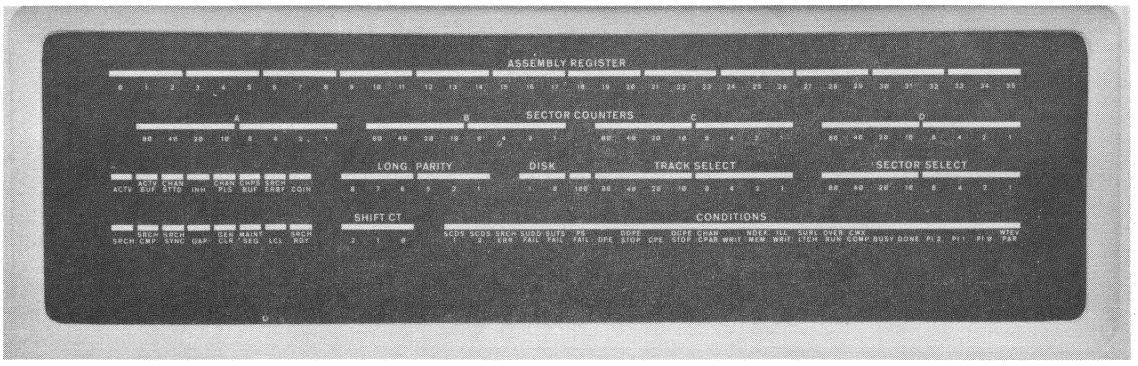

Figure 2-1 RC10 Indicator Panel

Table 2-1
Operating Controls

Switch	Function
DATA SWITCHES	In local control, contains the data to be written onto the maintenance segment of the selected disk and track.
PARITY SWITCHES	In local control, specifies the initial parity character.
START	In local, starts the read or write operation.
STOP	In local control stops read or write, and if held depressed, permits only one cycle of the read or write operation when start is operated.
CLEAR	In local control, clears the synchronizer and stops the operation.
LOCAL/REMOTE	In LOCAL, permits operation from the maintenance panel. In REMOTE, permits operation by computer. In REMOTE, DATA SWITCHES, PARITY SWITCHES, TRACK SELECT, CHANGE TRACK, WRITE, CLEAR, STOP and START are disabled.
MAINT SEG/NORMAL	In local controls, has no effect. In remote control and MAINT SEG selected, the processor reads and writes only the maintenance segment.
WRITE	In local control, when ON, defines the write mode. If OFF, read mode is enforced.
CHANGE TRACK	In local control, permits the operator to increment the track select register after each read or write of the maintenance segment.
TRACK SELECT	Selects the disk and track number for local control operation.
PROTECT LEVEL	Defines a boundary consisting of a disk and track number for the area of write protection defined by the PROTECT AREA switch.
PROTECT AREA	Defines an area in relation to the boundary established by PROTECT LEVEL in which the protected area is excluded from the write operation. Switch positions are as follows: X UNDER - Exclusively under the track number. UNDER - Protect the selected track and below. OVER - Protect the selected track and above. X OVER - Protect exclusively over the track number.
DISK A, DISK B, DISK C and DISK D	Assigns a unit number to physical disk (disk A, B, C, or D). The processor selects the unit number for operation. Two disks must not be assigned the same unit number. In the off position, puts that disk exclusively off-line.

Table 2-2
Operating Indicators

Indicator	Function Indicated
ASSEMBLY REGISTER	Current value of the assembly register. Fluctuates during read or write. Thereafter, shows the value of the last word written on or from disk.
SECTOR COUNTERS	Current value of segment address of disk A, B, C, and D.
ACTV	ACTIVE. Synchronizer has generated CHANNEL START and waiting for data channel access. If ACTV BUF off when ACTV is on, synchronizer has data channel access.
ACTV BUF	Synchronizer has requested data channel access and is waiting for the channel to go inactive.
CHAN STTD	CHANNEL STARTED. Self explanatory.
INH	Inhibit flip-flop in channel control circuits is set. Inhibits CHANNEL START OUT.
CHAN PLS	Channel pulse flip-flop. The channel pulse has been received from the channel.
CHPS BUF	Channel pulse buffer. At least one channel pulse has been sent by the channel.
SRCH ER BUF	One revolution of disk without finding the addressed segment.
COIN	Coincidence between the LSD of segment select register and LSD of segment address from disk.
LONG PARITY	Current value of longitudinal parity register.
DISK	Disk unit selected for a data transfer (0-3).
TRACK SELECT	Current value of track selected for a data transfer (0-199 BCD).
SECTOR SELECTOR	Initial segment address of a data transfer (0-79 BCD).
SRCH	SEARCH. The synchronizer is in the search mode.
SRCH CMP	Search complete. The synchronizer is in a read or write operation.
SRCH SYNC	Search Sync flip-flop.
GAP	Disk is reading gap between segments.
MAINT SEG	Maintenance segment is being written or read.
LCL	The synchronizer is in local control.
SRCH RDY	Synchronizer is ready to start search.
SHIFT CT	Contents of DTC shift counter, that sequences the assembly or disassembly of AR.
SCDS	Unit number of disk selected for sector counter surveillance.

Table 2-2 (cont)
Operating Indicators

Indicator	Function Indicated
SRCH ERR	Search error flag.*
SUDD FAIL	Supress disk designation failure.
SUTS FAIL	Suppress track select failure.
PS FAIL	Power supply failure.*
DPE	Disk parity error.*
DDPE STOP	Disable disk parity error stop.*
CPE	Channel data parity error.*
DCPE STOP	Disable channel data parity error stop.
CHAN C PAR	Control word parity error from channel.*
WRITE	Data transfer is toward the disk.
NOEX MEM	Non-existent memory reference error.*
ILL WRITE	Illegal write.*
SURL LATCH	Selected disk not ready.*
OVERRUN	Data late error.*
CWX COMP	Control word storage complete.*
BUSY	Synchronizer busy.
DONE	Data transfer terminated.*
PI0, 1, 2	Priority assigned by processor to synchronizer interrupt channel.*
WTEV PAR	Write even parity into processor memory.
*See Table 2-6 for further detail.	

2.3 INPUT/OUTPUT INSTRUCTIONS

The four PDP-10 I/O instructions that control the operation of the synchronizer are the DATAO, DATAI, CONO, and CONI instructions. The DATAO (data out) instruction has the form of DATAO N E where N is the 7-bit device selection number (170 for the synchronizer) and E is the 18-bit address (256K word of memory addressable). The DATAO instruction transfers the contents of memory location E to the I/O device selected by N. The 18-bit E address for the synchronizer is symbolically defined as INITWD (initial word). Location INITWD contains the 36-bit word required to initiate operation when the DATAO 170 instruction is executed by the computer. The format of INITWD is shown in Table 2-3.

The DATAI (data in) instruction has the format of DATAI N E. It transfers up to 36-bits of data from device N to the PDP-10 memory location E. For the synchronizer, the DATAI 170 E instructions transfers the data shown in Table 2-4.

The CONO (conditions out) has the format of CONO N E. It transfers the least significant 18-bits of effective address E (not the content of effective address) to device N. It first provides the CONO CLR pulse to clear control registers. It then provides the CONO SET pulse to strobe the bits into the control registers. The CONO 170 instruction format of the synchronizer is shown in Table 2-5.

The CONI (conditions in) has the format CONI N E. It transfers whatever device N puts onto the 36 data lines into memory location E. It supplies a 2.5 μs CONI pulse to gate the contents of the control register onto the 36 I/O data lines. The format of the CONI 170 instruction for the synchronizer is shown in Table 2-6.

2.4 OPERATION

Before initializing the synchronizer for a data transfer, the data-channel control word instructions must be placed into memory. The DATAO 170 INITWD instruction starts the synchronizer. If the synchronizer is already busy, the DATAO instruction is ignored. The DATAO instruction inserts the contents of location INITWD into the respective flip-flops and registers in the synchronizer and requests access to the data channel. Once the synchronizer has data channel access, it transfers the initial-control word address (bits 27-34 of INITWD) from the synchronizer to the data channel. Bits 27 through 34 of INITWD address the first 1000_8 even memory locations. Bit 35 for this purpose is sent as zero to the data channel, forcing the initial control word address to be even. Therefore, the initial control word must lie in an even-numbered location in one of the first 1000_8 memory locations.

The data channel stores the initial control-word address in its own register and fetches the initial control word normally consisting word count (WC) and data address (DA). The WC is the 2's complement of the number to the words to be transferred and the DA specifies their core memory address. After each word transfer the WC is incremented and the DA is incremented.

Table 2-3
DATAO 170 Format (INITWD)

Bits	Function	Description
0,1	Disk Selection	Selects one of the four disks assigned by the unit select switch.
2-10	Track Selection	Selects one of the 200 tracks. Bit-2 selects either upper or lower 100 tracks on a disk. Bits 3-10 comprise two BCD characters that selects one of the 100 tracks (0-99 BCD).
11-17	Segment Select	Comprises two BCD characters (0-79) that select one of 80 segments.
18-23	Initial Parity Character	Biases the initial longitudinal parity character recorded at the end of the first segment (see discussion on initial parity character).
24	DIS DPE STOP	Disable disk parity error stop. When set, prevents a disk longitudinal parity error from stopping operation.
25	DIS CPE STOP	Disable channel parity stop. When set, prevents a channel data parity error from stopping operation.
26	WRITE	When set, specifies the write mode (writing disk). When reset, specifies the read mode.
27-34	Initial Control Word Address	Stored in synchronizer until synchronizer gains access to data channel. Then, transferred to data channel so that data channel can fetch control word.
35	Even Parity	When set, specifies even parity for the data transfer between data channel and PDP-10 memory. If set, all data written into memory will have even parity, with one exception given below, thus allowing the operation of the parity check circuits to be verified. In all circumstances, control word into memory will have odd parity.

Table 2-4
DATAI 170 Format

Bit	Function
0-17	(Not used)
18-23	Initial parity register
24, 25	(Not used)
26	Sector Counter Select (1)
27	Sector Counter Select (0)
28-35	Sector Counter

Table 2-5
CONO 170 Format

Bit	Function
0-17	None
18,19	Select Sector Ctr
20	Reset disk designation error
21	Reset track select error
22	Reset disk not ready
23	Reset power supply failure
24	Reset disk parity error
25	Reset channel data parity error
26	Reset channel control parity error
27	Reset non-existent memory reference
28	Reset attempting to write in protected area
29	Reset overrun
30	Write Channel control word into memory
31	Reset busy (stop operation)
32	Reset done
33-35	P1 Bits, defines the priority (octal) assigned to synchronizer by processor.

Table 2-6
CONI 170 Format

Bit	Function	Description
0-4	None	None
5	MAINT SEG	Signifies that the maintenance segment switch on the maintenance panel is on and only the maintenance segment can be read or written upon.
6	PRTLTOLTOET	Protection area is less than, or less than or equal to, bounds switch.
7-17	STS	Content of bounds switches.
18	SC SCRCHCMP	Data transfer in progress.
19	SEARCH ERROR	The synchronizer is unable to find the addressed segment.
20	DSK DES ER	Disk designation error. Two disk files are designated with the same unit number and that unit number is selected by the program.

Table 2-6 (cont)
CONI 170 Format

Bit	Function	Description
21	TRACK SEL ER	Track select error. Indicates that the track select register is initially loaded or incremented (during track changing) to a non-BCD number.
22	SURL LATCH	Indicates that the selected disk file is not ready.
23	PS FAIL	Power failure or power transient of the +10 or -15 Vdc power supplies.
24	DISK PAR ERR	Disk parity error. During the read mode, a longitudinal parity error occurred on the data read from the disk.
25	CHAN PAR DAT	Channel data parity error. Indicates that a parity error occurred in the data transfer between data channel and PDP-10 memory.
26	CHAN PAR CON	Channel control word parity error. Indicates that a parity error occurred when the control word was fetched from PDP-10 memory.
27	NONEX MEM	Non-existent memory reference. Indicates that the data channel attempted a memory access that went unanswered.
28	ILLEGAL WRITE	A write operation was attempted in a protected area.
29	OVERRUN	Indicates that the data channel did not transfer data fast enough. The channel must be ready for a data transfer within approximately 13 μs.
30	CW XFER COMP	Indicates that the control word has been written into memory following a write-control-word request by the CONO 170 with bit 30 set.
31	BUSY	Indicates the synchronizer has been initialized and that it is either waiting for data channel access, searching, or transferring data. It is reset when operation is complete.
32	DONE*	Indicates operation has terminated. This is the only flag that will generate an interrupt.
33-35	PI Bits	Permits the program to assign a priority for priority interrupt by encoding the priority number into bits 33-35.

*The DONE seen by the program is slightly different from the DONE flip-flop. In particular, the DONE seen by program is the logical AND of DONE and NOT ACTIVE (ACTIVE=0). Thus, DONE to the program implies that the channel has also terminated.

The synchronizer now starts the search operation to determine when the addressed segment passes under the addressed track read/write head of the selected unit. The search operation starts if the following conditions are true.

a. The selected disk exists.

b. The selected track exists.

c. The selected segment exists.

d. A write operation is not being attempted in a protected area.

e. The voltages of the synchronizer are within tolerance.

f. The selected disk is ready.

g. Two disk units are not designated with the same number.

If any of the above conditions are not met, the DONE flag is turned on, the appropriate error status bit is asserted and the designated PI (priority interrupt) channel is asserted. Turning off DONE always removes the interrupt.

During a search operation, if the synchronizer is unable to find the segment address, the synchronizer and channel are terminated and DONE and SEARCH ERROR are turned on. A SEARCH ERROR condition may be cleared only by reinitiating the search or by an I/O clear operation.

The normal termination occurs when the channel fetches a zero control word. If writing, the synchronizer will fill the remainder of the segment with zeros and write the correct longitudinal parity prior to turning on DONE. If reading, the synchronizer will read through to the end of the segment and check parity before turning on DONE. Unfortunately, longitudinal parity failure in this case may, in fact, not really imply an error in the data in memory since it is not clear whether the error occurred in data read but not transferred.

Abnormal termination can be initiated by both the data channel and synchronizer. In either case, the synchronizer behaves as in normal termination except that the error flag, which caused the termination, is set along with DONE. It should be noted that DONE is the only flag that enables the priority interrupt channel. Moreover, the interrupt will not occur until the data channel terminates.

The data channel also terminates operation when it detects nonexistent memory reference (NON EX MEM) or a control word parity error when it fetched a control word. The nonexistent memory flag indicates the channel attempted a memory reference that went unanswered. After the data channel terminates, no data is transferred between synchronizer and data channel, however, the synchronizer continues until the end-of-segment. If writing, the synchronizer fills the remainder of the segment with zeros and the correct longitudinal parity is recorded.

The synchronizer terminates operation and sets the applicable error flag if any of the following conditions occur. (Refer to Table 2-6 for description of error flags.)

a. OVERRUN

b. CHAN PAR DAT (channel data parity error) and DIS CPE STOP not enabled.

c. DISK PAR ER and DIS DPE STOP not enabled.

d. ILLEGAL WRITE

e. TRACK SEL ER

f. SURL LATCH (selected disk file becomes not ready)

g. SEARCH ERROR

h. CONO 170 instruction with bit 31 set.

i. PS FAIL

When the CHAN PAR DAT, or OVERRUN errors occur, data channel operation terminates; however, the synchronizer continues until the end of segment before terminating and setting DONE. If writing, the remainder of the segment is filled with zeros. The PS FAIL error waits until the end of segment before terminating synchronizer and data channel. The remainder of the above errors terminate operation immediately.

If a channel is trying to access a nonexistent memory, the OVERRUN flag will probably also occur. The data channel will not terminate; however, until the 100 μs nonexistent memory delay elapses. DONE and the OVERRUN flag may therefore be on for some time prior to the interrupt channel activation.

2.5 INITIAL PARITY CHARACTER

The initial parity character is delivered with the DATAO 170. It biases the parity character and this bias will show up in the first segment written if writing was selected. If this segment is subsequently read and the same bias is used, no error will be indicated. If a zero bias is used on read, an error will be indicated and parity character read back will be that which was used as the bias on the original write. In general, the parity character read will be the exclusive-OR of the write bias and the read bias, and if it is not zero, an error will be indicated.

The write bias biases only the first segment written. The read bias, on the other hand, is carried over to all segments read in one operation. If stop is suppressed, the parity character read will be the exclusive-OR of all characters read and the bias.

This feature is primarily intended for maintenance purposes and it is anticipated that most programming will use a zero bias.

2.6 TRACK CHANGING

If the length of data transfer encompasses two tracks, the change from track to track occurs automatically. Changing from disk to disk does not occur. After the last track of the selected disk is accessed, the next transfer occurs at segment 0, of track 0, on that same selected disk.

2.7 WRITE PROTECTION

Four thumb wheel switches (Protect Level) on the maintenance panel select a track which is the boundary between the protected and the unprotected areas of file. A four position rotary switch (Protect Area) selects whether the area above or below the boundary is to be protected and whether the boundary is to be included in the protected area. The value in the Protect Level switch may be read by program and whether the protected area is below or above the boundary can also be sensed. The inclusion of the boundary cannot be sensed.

The disk selection thumb wheel is interpreted modulo 4 and the hundreds track select switch is interpreted modulo 2.

If more than one disk is on a system, the protected area includes all disks above or below the disk designated by the disk selection thumb wheel.

2.8 MAINTENANCE SEGMENT

An extra segment (the 81st) exists on the disk. During normal operation it provides the time to do track changing when reading or writing over track boundaries. It is possible to read and write this segment directly from the maintenance panel independent of the processor. It is also possible to read and write this segment under processor control if the MAINT SEG/NORMAL switch is in the MAINT SEG position. However, if this switch is in MAINT SET, no other segment can be accessed, track changing does not occur, and the operation terminates at the end of the segment. Protection is ineffective. The position of the MAINT SEG switch may be sensed by program.

2.9 DISK SELECTION

The system is capable of handling as many as four RD-10 files. The physical files, called A, B, C, and D, may be designated with any of the four valid disk numbers, 0, 1, 2, 3. This is accomplished by means of four 5-position rotary switches, on the maintenance panel, one for each disk. (The fifth position is an off position and effectively removes that file from the stable of those available.) If two files are designated with the same number, and that number is selected, the synchronizer terminates and an error condition is indicated. If no file is designated with the selected number, the Disk Not Ready condition is given and the synchronizer is terminated.

2.10 SECTOR COUNTER

This facility permits the program to examine the current segment address (contained in the sector counter) on any of the four disks files that are not engaged in a data transfer. Since each segment is 400 μs long, the current value is, of course, only valid for 400 μs. For 1 μs out of every 400,

the value is unsettled, therefore, to assure a correct value, the sector counter should be read twice and even three times if the first two readings disagree. The segments are sequential.

To read a sector counter, the CONO 170 instruction is issued with bits 18 and 19, binary encoded, to select the disk whose sector counter is to be read. The DATAI 170 is then issued, and the current value appears in bits 28-35, the value, of course, consists of two BCD characters. The number of the disk file that is selected for sector counter inspection appears encoded in bits 26 and 27.

2.11 LOCAL/REMOTE CONTROL

The maintenance panel LOCAL/REMOTE control switch determines local or remote control. In remote control, the processor controls the operation of the synchronizer and the maintenance panel CHANGE TRACK, WRITE, CLEAR, STOP, START, DATA SWITCHES, PARITY SWITCHES, and TRACK SELECT controls are inoperative. If the MAINT SEG/NORMAL switch is in MAINT SEG, the processor will read or write from only the maintenance segment on the processor selected track and disk. Track changing and write protection are not possible.

In local control, the synchronizer is completely off-line and all I/O instructions are disabled. Operation is controlled from the maintenance panel. The read or write operation occurs only on the maintenance segment. To specify the write mode, switch to WRITE position. To specify the read mode, do not switch to WRITE position. To change from write to read mode, depress CLEAR.

When the write mode is specified, the data in the AR is written onto the maintenance segment of the track and disk selected by TRACK SELECT. The PARITY SWITCHES generate the initial parity character. The operation starts when START is depressed. The search mode is enabled and it searches (as in normal operation) for the maintenance segment (segment 80). When found, the maintenance segment is recorded. If at this point the STOP switch is held depressed, the write operation stops after recording this one segment. If not, the operation recycles. If TRACK CHANGE was operated, write continues recycling, increments the track select register on each recycle. Thus, the AR data is sequentially recorded on the maintenance segments of consecutive tracks. If the TRACK CHANGE has not been operated, the writing continues without changing tracks.

The read operation is the same as write, except that the data is read from the maintenance track. If a one-cycle operation is desired, to be sure that only one cycle occurs, depress START while holding STOP depressed.

2.12 WRITE EVEN PARITY

When this feature is specified (by bit 35 of INITWD) all data (with one exception noted below) transferred to the memory is written with even parity. The control word, however, is always written

with odd parity. The PDP-10 operates with odd parity and using the even parity from the data channel permits check-out of parity check circuits, since parity errors should always occur on a data transfer using even parity.

CHAPTER 3
THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides a complete description of the theory of operation of the RC-10 Synchronizer. General and summary information of the synchronizer data channel and the RD-10 Disk Unit is discussed first. This is followed by a detailed logic description of the Synchronizer.

3.2 DF-10 DATA CHANNEL DESCRIPTION

A complete description of the DF-10 Data Channel is given in the DF-10 Data Channel Manual. However, in order to understand the operation of the RC-10, it is necessary to understand how the DF-10 communicates with the synchronizer. Therefore, a brief description of the DF-10 is given below.

When DATAO 170 is issued to start operation, it provides an initial control word address. The control word address is held by the synchronizer until it gains access to the data channel. When the synchronizer gains access to the data channel, it sends the initial control word address to the data channel which stores this address in the control word address register. The data channel then fetches the control word, normally consisting of WC (word count) and DA (data address). The WC and DA are stored in their respective data channel registers. The WC register specifies the number of data words to transfer and the DA specifies the core memory location. After a word transfer between core memory and the device communicating with the data channel, the WC is decremented and the DA is incremented. When the WC is reduced to zero, the number of words initially specified have been transferred. The control word address register is incremented and the next control word is fetched from core memory. If the control word contains all zeros, the end of communications is specified and the data channel terminates operation.

A number of devices can be connected to the data channel; however, the data channel communicates with only one at a time. To establish, maintain, and terminate communications, the following signals are exchanged between device and data channel.

Data Bus	This incorporates 36 bidirectional data pulse lines. These signals are 100 ns negative going pulses swinging from ground to -3V.
Channel Pulse	This 100 ns negative going pulse is sent from the Channel. It accompanies the data pulses when the Channel is sending data to the device. It also signifies a readiness to receive data when the device is trying to send data to memory.

Device Pulse	This signal is similar in function to the channel pulse signal. It accompanies the data when the device is sending, and signifies readiness to receive when data flow is toward the device.
Channel Start	This is a level (-3V for true) which is sent from the device to the channel. It will start the channel into operation when asserted.
Sawrite	This signal controls the direction of data transfer. When true, it signifies the device is writing some medium (reading memory). The timing is the same as that for CHANNEL START.
Channel Busy	This signal comes from the Channel and is asserted (-3V) sometime after CHANNEL START is asserted from the device. The device must not put anything on the bus until this signal is asserted. When this signal goes false after having been true, the Channel has terminated for one reason or another. CHANNEL START and CHANNEL BUSY must all be false for at least 400 ns prior to reassertion of CHANNEL START.
Write Control Word Request	This negative 100 ns pulse from the device causes the channel to store the current contents of the data address register and the control word address register into memory location B + 1 where B (an even number) is the Channel initial control word address. The contents of the control word address register go into bit positions 0 through 17 and the contents of the data address register into 18 through 35. Upon any Channel termination, an automatic WRITE CONTROL WORD REQUEST is made.
Write Control Word Complete	This pulse from the Channel signals the completion of the operation requested above. This pulse does not occur on the automatic transfer.
No Such Memory	This pulse is sent from the Channel as CHANNEL BUSY goes off and indicates that the memory addressed failed to respond.
Control Word Parity Error	If a control word is fetched from the memory by the Channel and this word has a parity error, CHANNEL BUSY is reset and this pulse is sent to the device from the Channel.
Data Word Parity Error	This pulse accompanies the data and the CHANNEL PULSE when a data word which was read from memory with a parity error is sent to the device.

The I/O devices attached to a data channel are arranged as shown in Figure 3-1 (only the pertinent signals are shown). In order for a device to gain access to the data channel, it must generate a CHANNEL START and receive a CHANNEL BUSY. If a device is not actively engaged with the data channel, it relays the CHANNEL START and CHANNEL BUSY. A device that is relaying CHANNEL START is prevented from generating its own CHANNEL START. A device that is busy with the data channel does not relay CHANNEL BUSY.

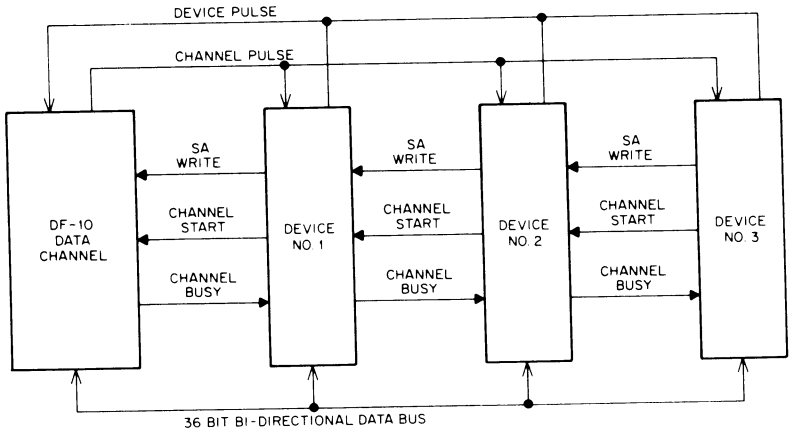

Figure 3-1 Data Channel Devices

To further examine data channel communication, assume that device 1 and 2 are not busy and device 3 initiates communication by asserting its CHANNEL START signal. It is applied to device 2 and since device 2 is not busy it relays the CHANNEL START. Similarly, device 1 relays CHANNEL START. The data channel acknowledges the CHANNEL START by asserting the CHANNEL BUSY. The data channel does not know which device requested access. The data channel knows only that it received a CHANNEL START and it responds by asserting CHANNEL BUSY. Furthermore, the data channel responds only to stimulus of the control signals by transferring data to and from the data bus or starting or stopping operation. It is the responsibility of devices to determine which has access.

Since devices 1 and 2 are not busy, they relay the CHANNEL BUSY signal to device 3. Upon receipt of CHANNEL BUSY, device 3 has access to data channel and can communicate via use of

data bus. Two things are required for a device to gain access to the data channel; the assertion of its own CHANNEL START and the receipt of CHANNEL BUSY.

To demonstrate this dual requirement, assume that device 2 is communicating with the data channel. It has asserted its CHANNEL START and received a CHANNEL BUSY. It does not relay CHANNEL BUSY to device 3. If now, device 3 attempts communications, it can assert CHANNEL START since it is not relaying CHANNEL START. Since device 2 is already generating a CHANNEL START, it essentially ignores the CHANNEL START from device 3. The CHANNEL BUSY is not relayed to device 3; therefore, device 3 does not gain access to the data channel because of two requirements; assertion of CHANNEL START and receipt of CHANNEL BUSY. Device 3 now must wait until Device 2 has finished with the data channel.

Either device 2 or data channel can terminate operation. The data channel terminates operation by removing CHANNEL BUSY and the device responds by negating CHANNEL START. The device terminates operation by removing CHANNEL START and the data channel responds by negating CHANNEL BUSY. After termination, device 3 is now free to communicate; however, the data channel requires at least 400 ns time between the negation of CHANNEL BUSY and CHANNEL START and the assertion CHANNEL START. In this case, this requirement is imposed upon device 2 (or any other device that is generating or relaying CHANNEL START and receives the on-to-off transition of CHANNEL BUSY). When termination occurs, the devices must inhibit the generation or relaying of CHANNEL START for 400 ns. The synchronizer incorporates the inhibit (INH) flip-flop for this purpose.

3.3 DISK INTERFACE SIGNALS

Table 3-1 shows the interface signals sent from the disk to the synchronizer and Table 3-2 shows the interface signals sent from the synchronizer.

Table 3-1
DISK to Synchronizer Signals

Signal	Description
RL1L RL2L RL5L RL6L RL7L RL8L	Read Levels - when true, indicate that binary ONES are being read from the disk. (lines RL3L and RL4L are not used when the 6-bit character format is used.) During address read, these lines contain the address information.
FCLP	File Character Clock Pulse - during Write the presence of the clock pulse indicates that the System Memory has accepted the character on the WLnL lines and the Control Unit may change the data. Duration of the pulse is 3-bit clock times.

	During Read, the presence of the Clock pulse indicates that a character is present on the RLnL lines. Duration of the pulse is 2 bit-clock times. The data on RLnL lines is present for 5-bit times when using the 6-bit character format.
LPCP	Longitudinal Parity Clock Pulse - when true indicates that the last (parity) character of a segment is being transferred. During a Read Operation, LPCP is coincident with the last FCLP. During Write, LPCP is true for the last two characters of the segment.
SACP	Start Address Clock Pulse - when true indicates that a segment address is about to be read. Duration of SACP is 3 1/2 bit times.
SURL	Storage Unit Ready Level - when true indicates that the System Memory is Ready.
INXD	Index Clock Pulse - when true indicates end of track; duration is 650 ± 100 ns.

Table 3-2
Synchronizer to Disk Signals

Signal	Description
TO1L TO2L TO4L TO8L T10L T20L T40L T80L	Track Select Lines - when true select one of one hundred tracks using binary coded decimal representation 00 through 99.
WL1L WL2L WL3L WL4L WL5L WL6L WL7L WL8L	Write Levels - when true, designate the binary ONES that will be written on the disk. Lines WL3L and WL4L are not used when the 6-bit character format is used.
WISL	Write Information Status - when true, conditions the System Memory for a Write operation. When false, the System Memory is conditioned for a Read operation.
ITSL	Information Track Select - when true, causes the Unit to perform a Read or Write operation. When false, the Unit is reading from the address track.
DSSL	Disk Surface Select Line - This is the hundreds bit of the Track Select Line.

3.4 SYNCHRONIZER FUNCTIONAL DESCRIPTION

This section provides an overall functional description of the RC-10 Synchronizer. As an aid to this description, a simplified block diagram (Figure 3-2) and a flow chart (Figure 3-3) are provided.

Operation starts when the PDP-10 program issues a DATAO 170 instruction. The instruction first examines the status of the BUSY flip-flop and if it is set, signifying that the synchronizer is already engaged in a data transfer, the DATAO 170 instruction is ignored. If synchronizer is not busy, the DATAO 170 instruction clears and normalizes control flip-flops and registers in preparation for the ensuing data transfer. It also transfers the contents of the I/O bus, which contains INITWD (described in Chapter 2) into its respective flip-flops and registers.

If the synchronizer is ready (i.e., selected disc, track, and segment exist, power OK, no illegal write, disk unit ready, and two disk units not selected), the synchronizer attempts to gain access to the data channel. If the synchronizer sees the CHANNEL BUSY signal, it must wait. In this case, the synchronizer relays CHANNEL BUSY from the data channel to the other device and relays CHANNEL START and SAWRITE from the device to the data channel.

When the data channel becomes free from another device, as evidenced by the removal of CHANNEL BUSY and CHANNEL START, the synchronizer can then gain access to the data channel. The synchronizer now generates its own SAWRITE and CHANNEL START. The data channel responds by asserting CHANNEL BUSY which is sent to the synchronizer. The synchronizer does not relay CHANNEL BUSY. The initial control word address which was temporarily stored in the AR (assembly register), is transferred to the data channel. The control word address defines the address in PDP-10 core memory of a 36-bit word which is divided into two parts; WC (word count) and DA (data address). This word is fetched by the data channel and placed into the control word register in the data channel. The WC defines the number of words that comprise the ensuing data transfer. The DA defines the PDP-10 core memory address which is to receive or send a word. For each word transfer between core memory and the synchronizer (via data channel), the WC is decremented and DA is incremented.

If SAWRITE is asserted, (meaning a write operation is specified), the data channel accesses core memory to obtain the first word to be recorded by the synchronizer. After the data channel receives the initial DEVICE PULSE from the synchronizer, it transfers this first 36-bit word to the AR register in the synchronizer.

The synchronizer by now has started the search operation. The search operation consists of searching for coincidence between the segment specified by SS register and the segment currently passing under the read/write heads in the disk unit.

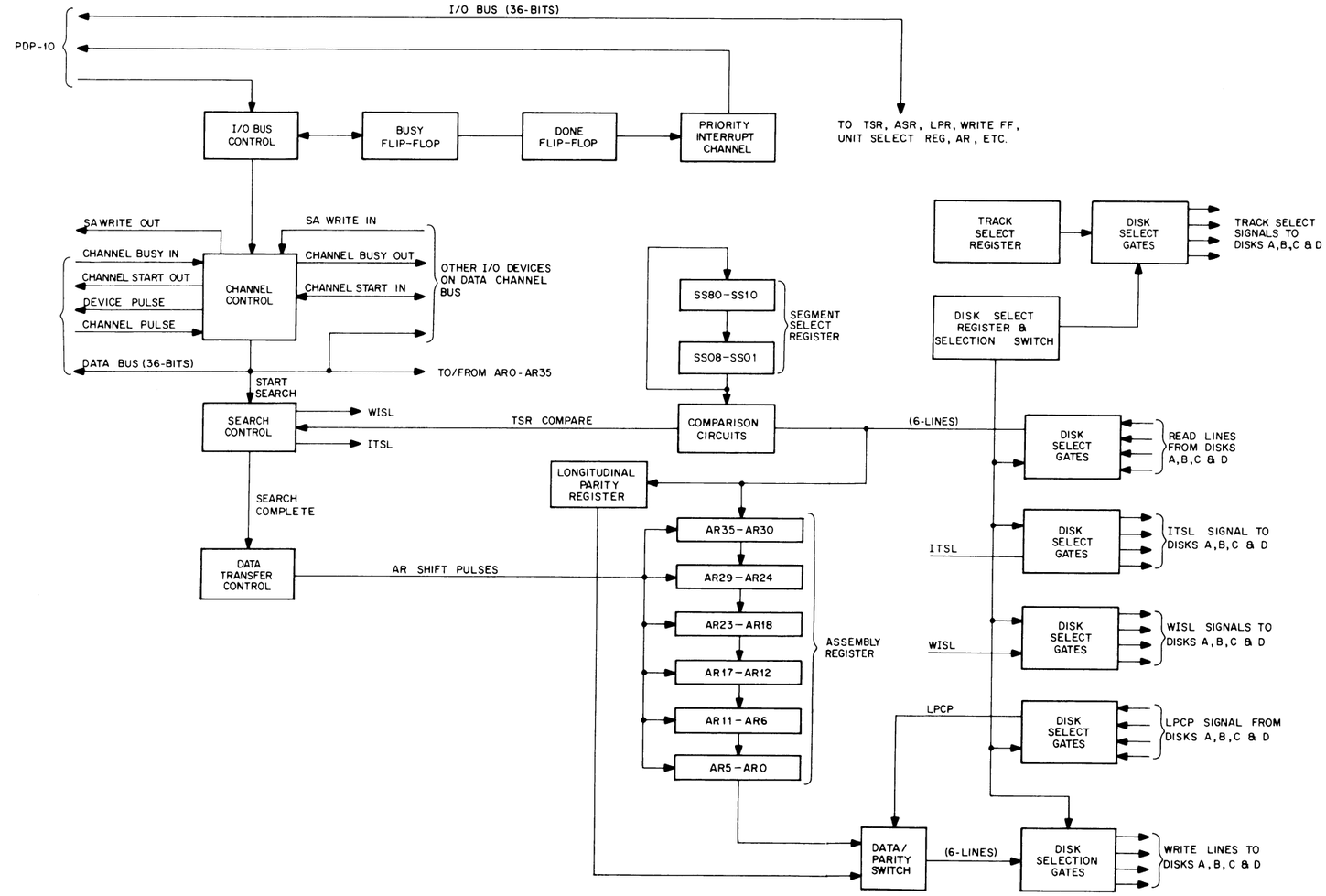

Figure 3-2 Synchronizer Simplified Block Diagram

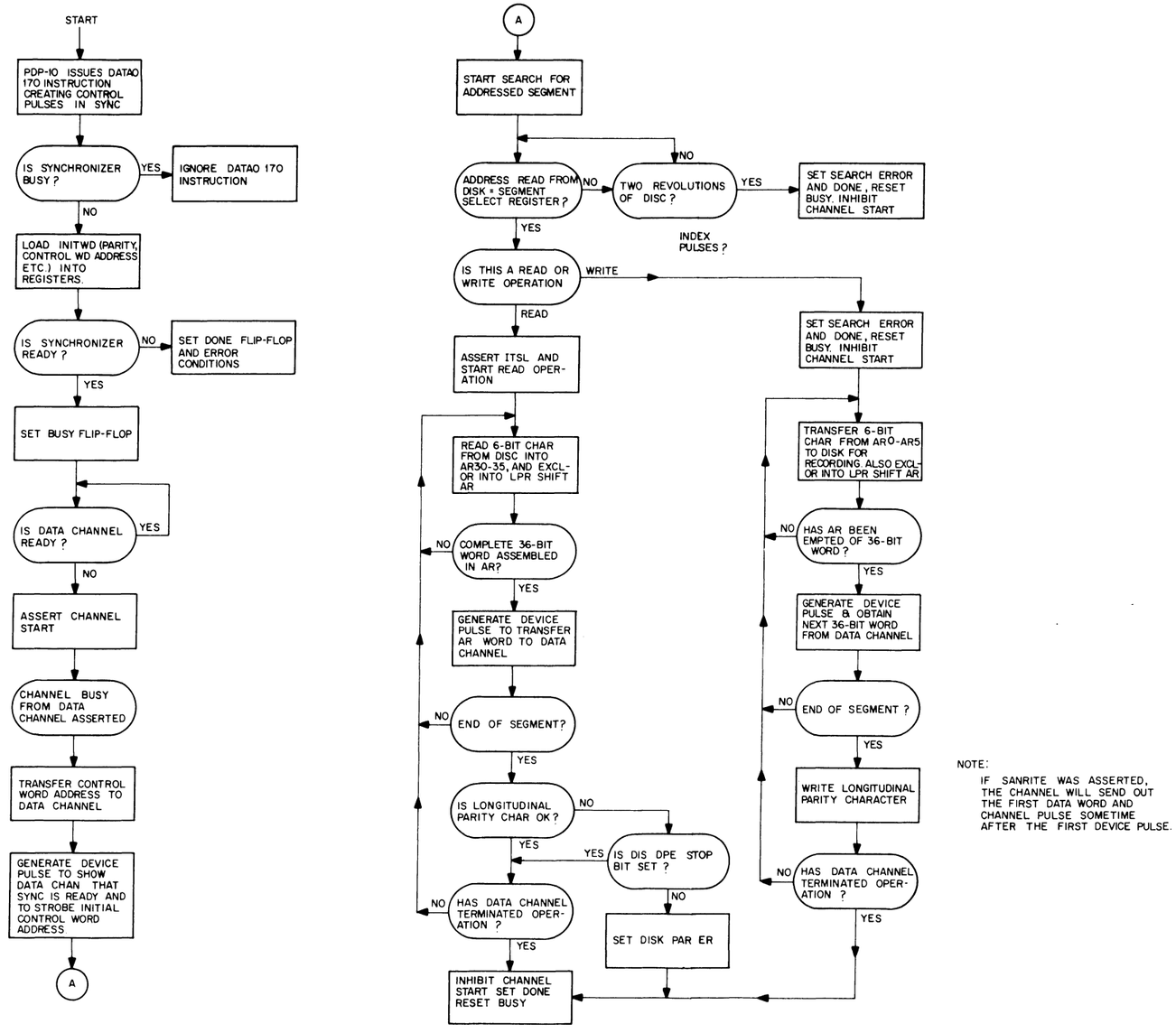

Figure 3-3 Flow Diagram of Normal Synchronizer Operation

When the ITSL signal from the synchronizer is not asserted, the disk unit puts only the data from the segment address track onto the read bus. As the disk rotates, each segment is prefaced (during previous segment) by its address which consists of two BCD characters. The least significant digit is read first. The SS register is synchronized to the address data being read so that the least significant from the disk and the least significant digit of the SS register are applied simultaneously to the comparison circuits. The SS register is then shifted and the most significant digit can be compared to most digits being next to be read from the disk. When there is identical comparison between the SS register and the address read from the disk, for both least and most significant digits, the search is complete and the data transfer cycle is enabled. If two rotations of the disk (i.e., two index pulses) finds that there has been no comparison, the SEARCH ERROR and DONE flip-flops are set and operation terminates.

If the data transfer is a read operation, the ITSL signal to the selected disk unit is asserted. The data read from the data tracks is now put onto the read bus. As each 6-bit character is read from the disk, it is transferred into AR30 - AR35 and the AR is shifted. It is also exclusive-ORed into the longitudinal parity register (LPR) to accumulate the longitudinal parity. After a complete 36-bit word has been assembled, it is put onto the data channel bus and the DEVICE PULSE is generated, which instructs the data channel to fetch the word from the bus. The read operation continues in this manner until the end of the segment is encountered at which time parity is checked.

At the end of each segment the control sees if the synchronizer or data channel has terminated operation. The data channel normally terminates operation when it fetches a zero control word. The synchronizer terminates operation when parity errors or some malfunction is detected.

For the write operation, the WISL and ITSL signals are asserted to condition the selected disk unit for the write mode. The AR0 through AR5-bits are sent to the selected disk for recording. The AR is then shifted and positions the next 6-bit character into AR0 through A5. The recorded character is also exclusive-ORed into the LPR.

After all 36-bits of an original AR word are written, the synchronizer clears the AR, generates the DEVICE PULSE, and obtains the next 36-bit word to record. At the end of each segment, the LPCP signal from the disk gates the longitudinal parity character from LPR to the write bus to record parity. As in the read operation, at the end of a segment, if a termination request has been given by the data channel operation terminates.

3.5 DETAILED LOGIC DISCUSSION

The following provides detailed logic discussion of the logic circuits for the synchronizer. The discussion makes reference to logic drawings in Chapter 6. The reference to the logic drawing is by its letter designation. For example, logic drawing D-BS-RC10-0-CC is referred to as "drawina CC."

Furthermore, the flow diagrams of the controlling modes of the synchronizer are included in Chapter 6. Where applicable, the flow diagrams should be consulted while reading this discussion.

3.5.1 IOB Control

Operation of the RC-10 Synchronizer starts when the program issues the DATAO 170 instructions with format as shown in Table 2-3. This generates IC IOB DATAO CLEAR pulse (upper left-hand portion of drawing IBC). If the synchronizer is not busy (-CXR BUSY B level is one) and the IBC DISK ADDR level is true, then the IBC INITIAL CLEAR pulse is generated. The IBC DISK ADDR level (right-hand portion of drawing IBC) is the result of decoding the 170 or device selection portion of the DATAO 170 I/O instruction. If the BUSY flip-flop (drawing CXR) is set indicating that the synchronizer is still busy with a previous data transfer, then the present DATAO 170 instruction is ignored.

The IBC INITIAL CLEAR pulse clears the GEN CLR flip-flop to remove the IBC GEN CLR B signal that holds key flip-flops and registers in the quiescent or clear state. The IBC INITIAL CLEAR generates IBC CLEAR TS that performs a general clear or normalizing of control flip-flops and registers in preparation for the impeding data transfer. (Refer also to flow chart of start drawing D-FD-RC10-0-F01).

The ensuing IC IOB DATAO SET pulse, which results from the DATAO 170, generates IBC SET TS1 and IBC SET TS2, if -CXR BUSY B, CC ACTIVE (0), and IBC DISK ADDR are true (drawing IBC). The SET TS pulses load the contents of INITWD into the applicable registers as outlined in the start flow chart.

The next operation to be performed determines if the synchronizer is ready to start operation. To do this, the status of the following conditions and errors may generate CXR PREVENT START which is sampled by CC PREVENT TEST.

a. Track Select Error (TSR TRACK SELECT ER).

b. Two disks designated with the same number (TSR DSK DES ER).

c. A write is attempted in a protected area (CXR WRITE B and TPC PROTECT are true).

d. The disk is not ready (SURL, Storage unit ready level from the disk is not true).

e. Power Supply out of tolerance (CXR PS FAIL).

If none of the above conditions are true, the CXR PREVENT START signal (drawing CXR) is not asserted. The SET TS1 signal strobes a 1 μs one-shot multivibrator that generates CC PREVENT TEST whose trailing edge samples the condition of CXR PREVENT START. If there are no errors, the BUSY flip-flop (drawing CXR) and the ACTIVE BUF flip-flop (drawing CC) are set. With ACTIVE BUF set, channel control operation is initiated. If any of the above conditions are in error, the DONE flip-flop is set and initiates a computer interrupt, if interrupt is enabled.

It should be noted that many of the control circuits shown on drawing IBC are concerned with local control and will be described in later paragraphs.

3.5.2 Channel Control

Before performing a data transfer operation, the synchronizer must gain access to the data channel. If the data channel is busy with another device, the synchronizer must wait until the data channel has completed its operation with the other device. For the ensuing description of channel control, it is assumed that the data channel is initially busy with another device.

The ACTIVE BUF (drawing CC) is set as previously described to request access to the data channel. The ACTIVE flip-flop, which signifies that the RC-10 synchronizer has access to the data channel, is of course reset since it is assumed that the data channel is busy with another device. The IC CHANNEL START IN signal will be asserted and it asserts CC CHANNEL START OUT. (Here we assume that the synchronizer is between active device and data channel.) Similarly, IC CHANNEL BUSY IN is relayed as IC CHANNEL BUSY OUT and IC SA WRITE IN is relayed as CC SA WRITE OUT.

The normal termination of a data transfer occurs when the data channel fetches a zero control word. It then terminates operation by removing the CHANNEL BUSY signal. The device that is busy recognizes the removal of CHANNEL BUSY as key to stop operation and thus inhibits its CHANNEL START out. On the other hand, the device can terminate the operation for reasons such as parity errors, etc., by removing its CHANNEL START. The data channel responds by inhibiting CHANNEL BUSY. Regardless of which terminates operations, it requires the negation of both CHANNEL START IN and CHANNEL BUSY IN before the synchronizer gains access to the data channel. When -IC CHANNEL BUSY IN, CC ACTIVE (0), and -IC CHANNEL START are true, the CC TERMINATE pulse (Figure 3-4) is generated to set the INH (inhibit) flip-flop. 250 ns later CC TERMINATE DELAY resets CHANNEL STARTED which in turn sets the ACTIVE flip-flop. Note that INH prevents ACTIVE from generating a CHANNEL START at this point. After another 250 ns, the CC RESET pulse is generated and resets the INH flip-flop. With CC INH reset, ACTIVE now generates a CHANNEL START which tells the data channel that the synchronizer is ready to start operation. CHANNEL START also prevents any other device on the bus (closer to the data channel) from gaining access to the data channel in the same manner that the CHANNEL STARTED flip-flop inhibits the synchronizer (note that CC CHANNEL START OUT holds CHANNEL STARTED in the set state).

The data channel responds to CHANNEL START by asserting CHANNEL BUSY. The receipt of CHANNEL BUSY by the synchronizer is the acknowledgment that it has access to the data channel. The synchronizer receives CHANNEL BUSY IN but does not relay it. The CHANNEL BUSY IN generates the CC STRTSCH (start search) to initiate the search operation. The CC STRTSCH generates the CC INADSTRB (initial address strobe) which in turn generates CC DATA STROBE 1 and 2. The DATA STROBES transfer initial-address bits, AR-27 through AR-35 (drawing AR2), to the data channel via the data channel bus.

The DATA STROBE 2 pulse generates CC DEVICE PULSE and resets the CHNPLS (channel pulse)

flip-flop if a read operation is specified. The DEVICE PULSE tells the data channel that the synchronizer is ready to start operation. If a write operation is specified, the data channel responds by transferring the first 36-bit word to the AR (assembly register-drawing AR) and sending CHANNEL PULSE. The DTC DATA RCVR EN signals (drawing DTC) enable the data transfer from data bus to AR during the write mode.

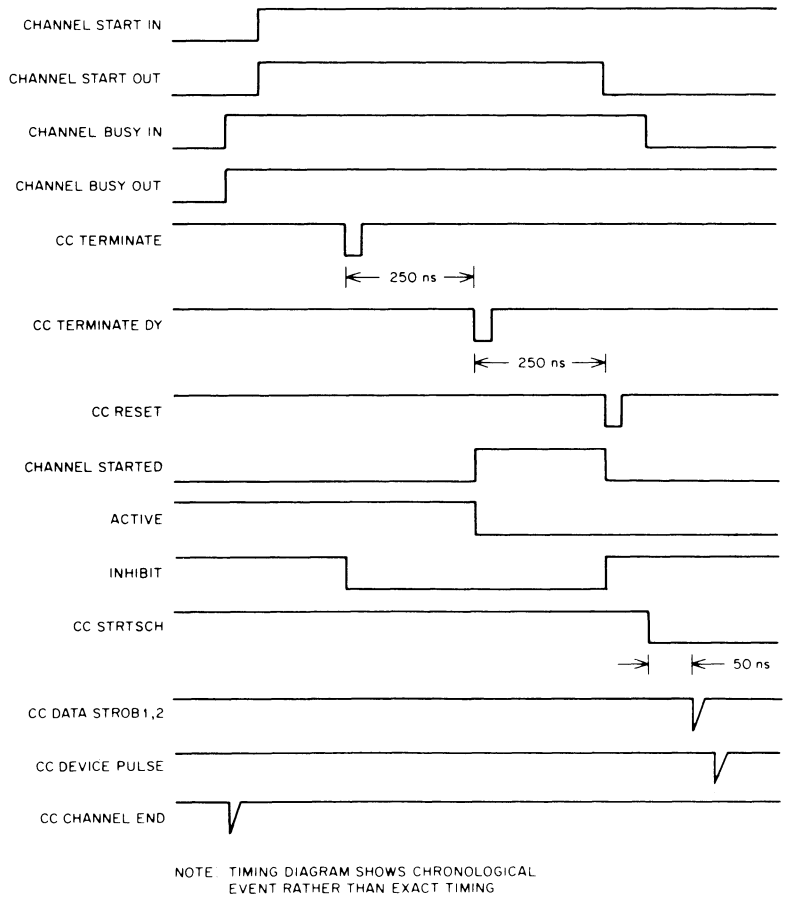

Figure 3-4 Channel Control Timing

It should be noted that the inhibit (INH) flip-flop is used to accommodate the data channel specification that requires the CHANNEL START and CHANNEL BUSY be false for at least 400 ns prior to reassertion of CHANNEL START.

Note also that CC DATA STROBE 2 also generates CC CLEAR AR. It is necessary to clear the AR when the write operation is specified, but not for a read. However, since the start-up procedure are common for both read and write, the AR is cleared.

The STRTSCH signal also turns off the ACTIVE BUF flip-flop. The ACTIVE BUF flip-flop is a request for data channel access and it must maintain this request until the synchronizer has confirmation

of data channel access. Since confirmation is via CHANNEL BUSY IN, when ACTIVE is true, STRSCH resets ACTIVE BUF.

3.5.3 Search Control

The assertion of CC STRTSCH initiates the search operation. It is ANDed with SC SEARCH READY (1) (which should be true at this time) to fire a 100 μs delay which sets SEARCH SYNC (drawing SC). The purpose of the delay is to allow the head selection network to settle. With ~~CC~~ SC SEARCH SYNC ON, the next DO SACP (start address compare pulse) leading edge will set ~~CC~~ SC SEARCH. The SACP signal from the disk signifies that the next two characters appearing on the read lines are segment address data. The synchronizer now searches for coincidence between the contents of the segment select register TSR SS 80 - TSR SS01, and the least significant BCD digit being read from the disk. The least significant BCD is read from the disk first and compared in value to SS 08-SS 01. The SS register is then shifted and comparison is made with the most significant BCD digit read and the SS register is shifted again. The details are given below (refer also to Figure 3-5).

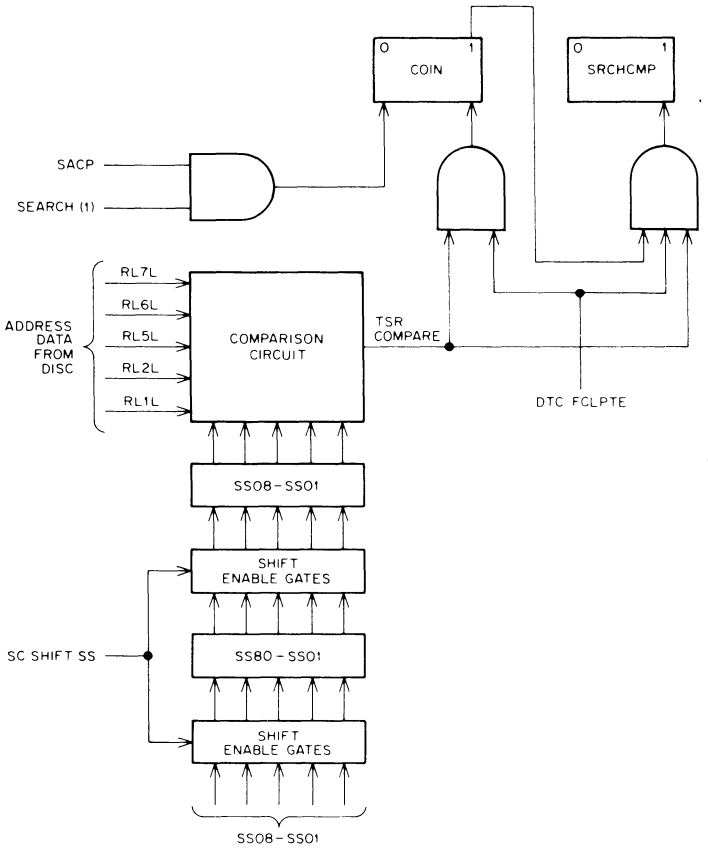

Figure 3-5 Simplified Diagram of Search

The DTC FCLPTE (drawing DTC), a pulse generated by the trailing edge of FCLP (digit clock) signal from the disk, is used to clock the operation. With SC SEARCH on, each DTC FCLPTE generates SC SHIFT SS (drawing SC) to shift the segment select register one BCD digit (drawing TSR, sheet 1). If TSR COMPARE (drawing TSR sheet 2) is true, DTC FCLPTE sets the SC COIN (coincidence) flip-flop signifying that the first BCD read from the disk compares identically to the first BCD in this SS register. The SS register is then shifted so that the most significant BCD digits can be compared.

If the next DTC FCLPTE finds COIN true and TSR COMPARE true, it sets the SRCHCMP (search complete flip-flop) indicating that since both BCD digits compared identically, the ensuing disk segment is the addressed segment. Since the search operation is complete, SRCHCMP resets SEARCH, SC COIN, and SC SEARCH READY.

If no comparison occurs for the second BCD digit, SC COIN is reset by DO SACP enabling the search to restart for the next segment. DO SACP occurs just before the least significant address digit comes from the disk.

With SRCHCMP true, the disk is ready to start the read or write operation. The read or write operation starts transferring data, the length of which is specified by the WC (word count) register in the data channel. The SS register specifies the address of the initial segment. Thereafter the data transfer automatically encompasses all segments within the length specified by the WC register. Similarly, the track select register (TSR) specifies the initial track address and continues from track to track if required by the specified data length. (The track select register is incremented and the SS register is reset to zero at index pulse time, INXP.) The data transfer operation then continues automatically on the new track at segment 0. The logic circuit implementation of this feature is described as follows.

The DO INXP (index pulse), which signifies end of track, generates the SC ORIGIN pulse (drawing SC). The SC ORIGIN pulse sets SEARCH READY, resets SRCHCMP, clears the SS register (drawing TSR, sheet 1), and increments the TS (track select) register (drawing TSR, sheet 1) by one. Note that the TS register is connected so that it increments in BCD format. With SEARCH READY set, SC SEARCH BEGIN is generated to strobe the 100 μs one-shot multivibrator that sets SEARCH SYNC. Thus, the search operation starts again and since the SS register is cleared, the data transfer continues on segment 0 of the next sequential track.

When a read operation terminates at the end of a segment, the synchronizer could be reading the first word of the next segment prior to the channel terminating, since the channel has to store the last word from the disk and fetch the zero control word. It is not possible to stop the disk from transmitting the entire segment. If a search now starts, the synchronizer may regard the tail-end of the block being read as address information, when in fact it is data. To alleviate this problem, the SC SEARCH READY flip-flop is installed. It turns off as soon as a search operation is completed and turns on again when it is safe to start a search operation.

3.5.4 Data Transfer Control

3.5.4.1 READ - With SRCHCMP set, the start of the read operation is enabled. SRCHCMP enables the ITSL (information track select-which enables the disk to perform read or write) for the selected disk (drawing DI). Since CXR WRITE is not true, the SC WISL (drawing SC) is not asserted, therefore, the selected disk is conditioned to read.

The DTC FCLPTE (trailing edge of FCLP) is now used to synchronize the data transfer of the 6-bit characters read from the disk to the synchronizer. It also is used to accumulate the longitudinal parity; that is, DTC FCLPTE generates DTC LOAD LPR (drawing DTC) so that for each 1-bit of DO RL8L-DO RL1L (the read lines from the disk), the respective bit of the LPR8-LPR1 (drawing LPR) register is complemented thus accumulating the longitudinal parity. DTC LOAD LPR also generates DTC SHIFT AR 1, 2, and 3 which loads the 6-bit character read from the disk into AR35-AR30 and shifts the 6-bit character within the AR register. DTC SHIFT AR1 also steps the shift counter DTC SHFTCT to monitor the number of 6-bit characters read from disk. Note that shift counter is a "split-tail" counter whose counting sequence is:

000 001 011 111 110 100 000

Thus, it requires six DTC SHIFT AR pulses for the counter to cycle. The counter was cleared when SC SEARCH was turned on. When the counter reaches zero, a complete 36-bit word has been assembled in the AR register and is ready for transfer to the data channel. The DTC SHIFT CT 0 PLS (pulse) signifies a zero-count in the counter and thus performs the following functions.

Assuming CHNPLS (drawing CC) is true, indicating that a CHANNEL PULSE has been received from the data channel, the DTC SHIFT CT 0 PLS generates CC SHIFT CT 0 PLS DLY which generates CC DATA STROBE 1 and 2. The DATA STROBES puts the 36-bit data word onto the data channel bus (AR drawings). The purpose of the 50 ns delay is to allow the AR register to settle down. DATA STROBE 2 generates the CC DEVICE pulse which accompanies the data to the data channel.

If the CHNPLS flip-flop has not been set by a channel pulse when DTC SHFT CT 0 PLS occurs, the DTC OVERRUN pulse (drawing DTC) sets the OVERRUN flip-flop (drawing CXR) to signify a data late error.

At the end of each segment, parity is checked. At the end of a segment DO LPCP (check character mark) signal from the disk becomes true. It enables the firing of the DTC CLR SHIFT CT (drawing DTC). The DO LPCP inhibits DTC SHIFT AR1-3. The check character read from the disk is exclusive-ORed into the LPR register. If the LPR register is not zero when the delay times out, CXR DISK PAR ERR (disk parity error) will be set to signify a parity error.

When DTC CLR SHIFTCT times out, it sets GAP (drawing DTC) signifying that the disk is

reading between segments. GAP will not be reset until the synchronizer assembles the next 36-bit word read from the disk. At this time, DTC SHIFTCT 0 PLS resets GAP. If during this period, CC ACTIVE is turned off by the data channel or the INH (inhibit) flip-flop gets set, the DTC FINISH pulse is generated. The DTC FINISH pulse terminates the operation by clearing SC SRCHCMP, CXR BUSY, and setting CXR DONE. The partial word in the AR is ignored.

3.5.4.2 WRITE - The start-up procedure for write is identical to read. For the write operation, the CXR WRITE flip-flop was initially set by the DATAO 170 instruction. The write operation starts when the SCHCMP flip-flop is set. Since CXR WRITE (1) is true, SCHCMP generates the SC WISL level to signify a write operation to the disk.

Since the data channel recognizes, via SAWRITE, that this is a write operation it has loaded the AR with first 36-bit word to be recorded. The FCLP now clocks the operation of transferring the 60-bit characters from AR0-AR6 to the disk and shifting the AR register. The leading edge of FCLP (i.e., FCLPLE) now generates DTC LOAD LPR which exclusive-ORs AR0-AR5 into the LPR register (drawing LPR) to accumulate the longitudinal parity character. The AR01-AR5 character is applied to enable gates (drawing DI) for routing to the selected disk.

As in the read operation DTC SHIFT AR pulses shift the AR and count-up the SHFTCT. When the SHFTCT recycles to zero, it generates DTC SHIFT CT 0 PLS to signify that a complete 36-bit word has been transferred to the disk and that it is ready for the next 36-bit word from the data channel. DTC SHIFT CT 0 PLS generates CC CLEAR AR and resets CC CHNPLS (drawing CC). After a delay to permit the AR to settle, it generates CC DEVICE PULSE signifying to the data channel that the synchronizer is ready to receive the next 36-bit word. The data channel responds by loading the AR register. Note that the function CC ACTIVE (1) IC CHANNEL BUSY IN CXR WRITE generates DTC DATA RCVR EN 1, 2, 3 signals (drawing DTC) that enable the strobes from the data channel bus (AR drawings) to insert data into the AR register.

The DTC SHIFT CT 0 PLS (via DTC WT OVERRUN TRIG) also strobes a 1.5 μs delay (drawing DTC) which after it times out, samples the CC CHNPLS to see if the data channel has responded by generating a CHANNEL PULSE. If no CHANNEL PULSE has been received, the CHNPLS flip-flop is still reset (drawing CC), therefore, the DTC OVERRUN pulse is generated and sets the OVERRUN flip-flop (drawing CXR) to signify an overrun condition.

When DO LPCP becomes true, signifying the end of segment and time for the recording of the longitudinal parity character, DTC CLR SHFTCT will be generated as in the read operation and the AR will not be shifted. Furthermore, the LPR register is now gated to the write data lines (drawing DI) to record parity.

The DTC GAP flip-flop is set and if CC ACTIVE is off (channel terminated) or CC INHIB is on (synchronizer terminating) DTC FINISH will be generated to terminate operation.

3.5.5 Data Transfer Termination

The normal termination of a data transfer occurs when the data channel fetches a zero control word. If so, it terminates the CHANNEL BUSY signal. The synchronizer recognizes the negation of CHANNEL BUSY as a signal to terminate operation. When CHANNEL BUSY goes to zero, it generates the CC CHANNEL END (drawing CC). The CHANNEL END pulse generates the CC TERMINATE pulse and resets the ACTIVE flip-flop. The CC TERMINATE sets the inhibit (INH) flip-flop and the CC RESET pulse (a 500 ns delayed CC TERMINATE pulse) resets the INH flip-flop to remove the CHANNEL START inhibit. As described previously, the 500 ns that the INH flip-flop is set is to meet the requirement that CHANNEL START cannot be asserted until 400 ns after the negation of both CHANNEL START and CHANNEL BUSY. The CC TERMINATE DY PULSE resets CHANNEL STARTED. The synchronizer thus has released control of the data channel and it is now free for another device.

When the data transfer control circuits (drawing DTC) detect the end of segment, the DTC GAP signal is enabled by CC ACTIVE (0) to generate the DTC FINISH pulses which resets the BUSY flip-flop (drawing CXR), sets the DONE flip-flop to generate an interrupt (if enabled) and resets SRCH CMP to terminate the data transfer to disk.

The data channel will also terminate operation when it detects a parity error in control word fetched from core memory or when core memory fails to acknowledge the transfer (NO SUCH MEMORY error). If either of these two conditions occur, the data channel stops operation by turning off CHANNEL BUSY.

There are two ways in which abnormal termination by the synchronizer occurs: when the inhibit (INH) flip-flop (drawing CC) is set and when the DTC FINISH pulse is generated.

The overrun error or a channel data parity error (if DIS CPE STOP is 0) sets the INH flip-flop. The overrun error (CXR OVERRUN (1)) was described previously in both the read and write description. When the INH flip-flop is set, it immediately terminates operation with the data channel by negating CHANNEL START. Signal INH (1) will generate DTC FINISH at the end of the segment (DTC GAP = 1) to reset BUSY and SET done.

The errors or abnormal conditions that generate DTC FINISH directly are:

Illegal Write

Track Select Error

Disk not ready (SURL LATCH)

Disk parity error

Power Supply error (waits until end-of-segment)

Search Error

CONO instruction with bit 31 set.

NOTE

When the data channel detects the initial control word as zero, the synchronizer must abort before any data is transferred. Thus, a special gate is added to the DTC FINISH pulse PA which triggers DTC FINISH if ACTIVE goes off before SC CHNPLS BUF comes on.

When the above errors or conditions occur, the DTC FINISH pulse is generated to set DONE and reset BUSY. When BUSY is reset, it sets the INH flip-flop to terminate data channel operation.

3.5.6 Condition Registers (Drawing CXR)

3.5.6.1 Search Error - This error indicates that the disk has made at least one rotation without finding the addressed segment. If the addressed segment is not found prior to INXP, the index pulse (INXP) sets the SEARCH ER BUF flip-flop. If the addressed segment is found during the next revolution SC SEARCH (1) enables the INXP to reset SEARCH ER BUF. If not, the INXP pulse sets the SEARCH ERROR flip-flop.

3.5.6.2 Write Even Parity - This flip-flop is set by the DATAO instruction if bit-35 is one.

3.5.6.3 Disk Parity Error - This flip-flop (DISK PAR ERR) is set during the read mode, if the LPR register is zero after the longitudinal parity character is read from the disk.

3.5.6.4 Illegal Write - This flip-flop is set if a write is attempted on a protected area of the disk. The TPC PROTECT signal is generated as follows. Four thumb wheel switches (drawing TPC sheet 2) select the unit and track number that defines the protection boundary. A four position rotary switch selects whether the protected area is above or below the selected boundary and whether the boundary is to be included in the protected area. Each of three track-number thumb wheel switches produce a BCD number. Each bit from each switch, is exclusive-ORed (compared) to its respective bit from the track select register (drawing TPC, sheet 1). The results are then combined and applied to the rotary selection switch (drawing TPC, sheet 2). If the selected track number fails within the selected boundary, signal TPC becomes true, and if the write mode is selected, the ILLEGAL WRITE flip-flop is set.

3.5.6.5 SCDS Flip-Flops - These flip-flops, which are selectively set by the CONO instruction bit 18 and 19, provide a selection of one of the four sector counters for program evaluation. Bits 18 and 19 are decoded to provide the unit number selection (CXR SC SEL 1-4). The CXR SC SEL signals are applied to the unit selection switch (drawing SCM). The asserted CXR SC SEL signal then enables the unit-selected sector counter. The selected bits (SCM SC 01, SCM SC 02, etc.) are then applied to the IOB

transmitter gates (drawing IOB) and if a DATAI instruction is executed, the bits are transferred to the PDP-10 for program evaluation.

3.5.6.6 Power Supply Failure - This flip-flop (PS FAIL) is set when the +10V or -15V go out of tolerance.

3.5.6.7 BUSY - This flip-flop signifies that the synchronizer is enabled to transfer data.

3.5.6.8 DONE - This flip-flop signifies that the synchronizer has terminated operation.

3.5.6.9 P10, P11, P12 - These flip-flops are selectively set by the CONO instruction to specify the program-selected priority for the synchronizer priority interrupt channel.

3.5.6.10 DIS DPE STOP (disable disk parity error stop) - When set, this flip-flop prevents the DISK PAR ERR (disk parity error) from terminating operation (see drawing DTC).

3.5.6.11 DIS CPE STOP (disable channel data word parity error stop) - When set, this flip-flop prevents the CHAN PAR PAT (parity error in channel data word transfer) from terminating operation.

3.5.6.12 WRITE - This flip-flop specifies the read/write mode of the synchronizer. When set by the initial DATAO 170 instruction, it specifies the write mode. When reset, it specifies the read mode.

3.5.6.13 SUPPRESS DD FAIL (Suppress disk designation failure) - When set, it suppresses indication of a disk designation failure by inhibiting TSR SEL DSK 0, 1, 2, 3. Note that if this bit is turned on while transferring data, SURL LATCH will come on halting the operation.

3.5.6.14 OVERRUN - This flip-flop signifies that the data channel transfer did not occur fast enough. It is set as described in the read and write operation.

3.5.6.15 CHAN PAR DAT - This flip-flop is set by a pulse from the data channel when a parity error occurs in the data transfer between data channel and core memory.

3.5.6.16 CHAN PAR CON - This flip-flop is set by a pulse from the data channel when a parity error occurs in the control word fetched from core memory.

3.5.6.17 NON EX MEM - This flip-flop is set by a pulse from the data channel when core memory fails to acknowledge the data transfer to or from the data channel.

NOTE

The NON EX MEM and CHAN PAR CON cause no further operation in the synchronizer. They terminate operation at the data channel. Their function in the synchronizer is only for program evaluation by the CONI instruction.

3.5.6.18 CW XFER COMP - This flip-flop is set by a pulse from the data channel, when the control transfer is complete, following the request for write control word (CC WR CON WD--drawing CC). This signal causes no further action in the synchronizer other than program evaluation by the CONI instruction.

3.5.6.19 SUPPRESS TS FAIL - When set, this flip-flop inhibits the generation of TSR TRACK SELECT ER (drawing TSR). The TRACK SELECT ER is generated when a non-BCD or illegal character is detected in the TS register.

3.5.6.20 SURL LATCH - When set, indicates that the disk file is not ready. If initially the selected disk file is not ready, CC PREVENT TEST sets SURL LATCH. After operation starts, if disk file becomes not ready, the BUSY level enables the transition of DO SURL to set SURL LATCH. See 3.5.6.13.

3.5.7 SC Prevent ORGN GLITCH

When counting from track to track, the TS register as it is incremented may momentarily produce an erroneous TRACK SELECT ER or TPC PROTECT. The erroneous indications are suppressed by SC PREVENT ORGN GLITCH. This signal occurs simultaneously with SC ORIGIN which is generated by DO INXP (drawing DTC).

3.5.8 Disk Selection

The four front-panel selection switches, DISKS A, B, C, and D permit the operator or programmer to assign a unit number to a physical disk (disk A, B, C, or D). The program selects the number instead of the disk. When the program selects a number via TSR DS0 and DS1, that number and only that number, must be selected by one of the selection switches (DISK A, B, C, or D). If not, a DSK DES ER occurs.

When a disk is properly selected, the appropriate TSR SEL DSKA, B, C, or D signal (drawing TSR, sheet 2) is enabled. All interface signals are enabled by this signal so that they are routed only to or from the selected disk (drawings DO, sheets 1 and 2, and DI).

3.5.9 Sector Counter

The sector counter along with sector counter multiplexer permits the program to examine the current segment address on any of the four disks if they are not in a read or write operation. If the program examines, the sector counter of a unit actively engaged in a read or write operation, it receives the segment address of the initial read or write transfer.

The sector counters are shown in drawing SCT. They normally count SACP pulses from the appropriate disk. At INXP time, the counter is set to 80.

3.5.10 Sector Counter Multiplexer

The sector counter multiplexer applies the program selected sector counter to the IOB transmitter gates bits SCDS (drawing CXR) which are set up by a CONO 170 instruction, define the disk number for sector counter surveillance. The decoded CXR SC SEL signal (drawing CXR) is routed through the appropriate selection switch (drawing SCM) and gates selected sector counter to the multiplexer output. The multiplexer output is coupled to the IOB transmitter gate (drawing IOB) for subsequent selection by the DATAI.

3.5.11 Local Control Operation

When the REMOTE-LOCAL switch is in LOCAL, the IBC LOCAL flip-flop is set as soon as SC GEN CLR becomes true. The IBC LOCAL B signal inhibits the I/O bus device address decoder, thus causing the synchronizer to become unselectable to the processor. Note that the processor will not be able to detect that a disk synchronizer is even connected to the I/O bus.

Operating the START pushbutton generates IBC LOCAL START, which turns off IBC MAINT STOP and triggers a one-shot that generates IBC LOAD TEST and IBC LOAD TEST 1 through 6. These signals do the following operations:

Turn off IBC GEN CLR

Fires IBC CLEAR TS which, clears the track select register, segment select register, and the LPR.

Sets LPR to the value in the PARITY SWITCHES

Sets AR to the value in the DATA SWITCHES

Sets the track select register to the value in the TRACK SELECT SWITCHES

Sets the segment select register to 80

On its trailing edge, sets CXR BUSY and fires the 100 μs delay that turns on SC SEARCH SYNC (drawing SC) to start the search

The search operates as previously described. When segment 80 is found, reading or writing occurs as before, with the exception that the DTC SHFTCTOPLS will not fire. As soon as DTC GAP comes on, DTC FINISH is generated turning off CXR BUSY. CXR DONE, however, does not come on. IBC GEN CLR will now come on and, if STOP has not been operated, a 100 μs delay will fire. When the delay has timed out, IBC LOCAL START will fire again reinitiating the operation. If track changing was selected, DTC FINISH generates SC ORIGIN counting the track select register.

CHAPTER 4
MAINTENANCE

This chapter contains the information for maintaining the RC-10 Synchronizer Control. Three categories of maintenance are provided: preventive, troubleshooting procedures, and corrective.

Preventive maintenance includes such routine periodic checks, as visual inspections, standard procedures involving cleaning and lubricating, minor mechanical adjustments, and occasional marginal checking to expose weakening conditions before they become malfunctions. It is primarily concerned with mechanical operations of the synchronizer.

It should be emphasized that good maintenance procedures are predicated upon a thorough knowledge of not only the RC-10 Synchronizer but also the disk file and the data channel. Therefore, if the maintenance technician is not familiar with the theory of operation, he should review Chapter 3 of this manual or the applicable sections of the RD-10 Disk File manual.

Troubleshooting procedures range from basic power-supply checks to logic troubleshooting techniques involving programmed operation of the PDP-10.

Corrective maintenance outlines the measures required for correcting any malfunction, after it has been isolated, by replacement of the module or defective part.

In addition to maintenance information, this section includes assembly-location information, to facilitate locating the circuits and parts within the system.

4.1 MAINTENANCE EQUIPMENT

The maintenance equipment specified in the PDP-10 Maintenance Manual is adequate for performing tests on the RC-10 Synchronizer. The Disk File Manual references special adjustment tools.

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically, during operating time of the equipment, to ensure satisfactory operation. Performance of such tasks forestalls failures induced by progressive deterioration or minor damage, which, if not corrected, cause eventual down-time. Data obtained during the performance of each task is recorded in a log book. Analysis of this data indicates the rate of circuit operation deterioration and provides information for determining when components must be replaced to prevent failure of the system.

The following mechanical checks must be performed at specified intervals determined by operating time and operating environment. Following is a list of the periodic checks and procedures required.

a. Clean the exterior and the interior of the equipment cabinet with a vacuum cleaner or clean cloths moistened in nonflammable solvent.

b. Clean the air filters at the bottom of the cabinets. Remove each filter by taking out the fan and housing (held in place by two knurled and slotted captive screws), wash in soapy water and dry in an oven or by spraying with compressed air. Spray each filter with Filter-Kote (Research Products Corporation, Madison, Wisconsin).

c. Lubricate door hinges and casters with a light machine oil, wiping off excess oil.

d. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder or replace any defective wiring or cable covering.

e. Inspect the following for mechanical security--switches, control knobs, lamp assemblies, jacks, connectors, transformers, fans, and capacitors. Tighten or replace as required.

f. Inspect all module mounting panels to assure that each module is securely seated in its connector.

g. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors showing these signs of malfunction.

4.3 TROUBLESHOOTING PROCEDURES

The troubleshooting procedures make use of the following diagnostic programs.

1. MAINDEC-10-5-5AA (Switch Test)
2. MAINDEC-10-5-5BA (Disk Test B)
3. MAINDEC-10-5-5CA (Disk Reliability Test)

Maximum utilization should be made of the maintenance panel and of local control. This mode is described in both Capters 2 and 3.

4.4 MODULE UTILIZATION

Table 4-1 contains a list of the modules used within the RC-10 Synchronizer. The applicable module information is contained within the Digital Logic Handbook C105 or within Volume 3 of the PDP-10 Maintenance Manual.

Table 4-1
Module Schematics

Drawing Number	Title
B133	Diode Gate
B134	Diode Gate
B135	Diode Gate
B137	Diode Gate
B141	Diode Gate
B152	Binary to Octal Decoder

Table 4-1 (cont)
Module Schematics

Drawing Number	Title
B156	Half Binary-to-Octal Decoder
B163	Diode Gate
B165	Diode Inverter
B212	Dual R-S Flip-Flop
B214	Four Flip-Flops
B311	Tapped Delay Line
B611	Pulse Amplifier
B683	50Ω or Bus Driver
B684	Bus Driver
B685	Diode Gate Driver
G704	2 MA Level Terminator
R001	Diode Network
R002	Diode Network
R201	Flip-Flop
R220	3-bit Shift Register
R302	Dual Delay Multivibrator
R303	Integrating One Shot
R401	Variable Clock
R601	Pulse Amplifier
R613	Pulse Amplifier
S111	Expandable NAND/NOR Gate
S202	Dual Flip-Flop
S203	Triple Flip-Flop
S205	Dual Flip-Flop
S602	Pulse Amplifier
S603	Pulse Amplifier
W010	Clamped Load
W102	Pulsed-Bus Tranceiver
W107	I/O Bus Receiver CKT
W505	Low Voltage Detector

Table 4-1 (cont)
Module Schematics

Drawing Number	Title
W514	Positive Level Converter
W693	DEC to CT μ Line Driver
W808	Relay

CHAPTER 5
INSTALLATION

This chapter provides information necessary for the installation of the RC-10 Synchronizer. For additional information consult the applicable PDP-10 installation document.

5.1 SITE PREPARATION

No special site preparation is required, except for the floor space dimensions outlined in Figure 5-1. As shown, adequate clearance for access must be provided. Both power and signal cables enter through holes provided in the bottom of the cabinet. Four wheels on the bottom of the unit allow the cabinet to be easily positioned, with clearance for the cables. No subflooring is normally required.

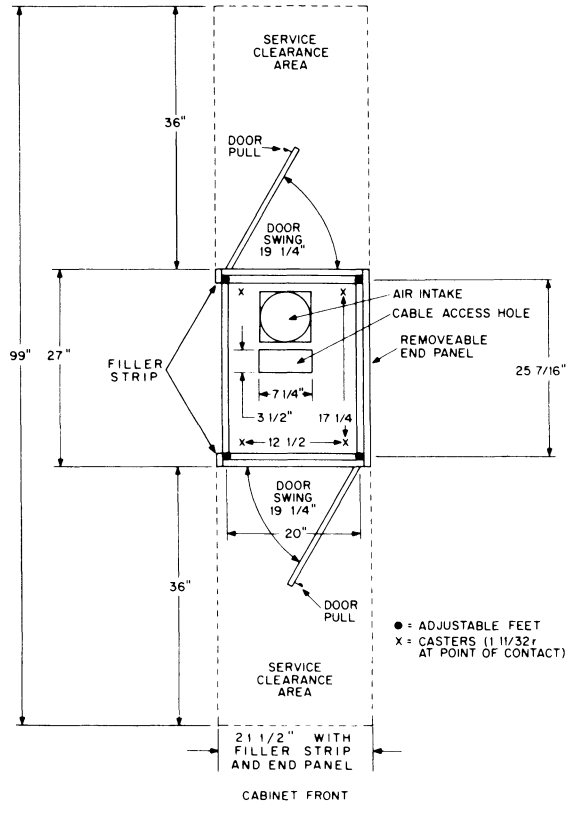

Figure 5-1 RC10 Cabinet Clearance Dimensions

5.2 ENVIRONMENTAL CONDITIONS

The in-cabinet air temperature must be maintained between +6°F and +100°F, and the recommended relative humidity between 20% and 80%. The installation site must also be as free as possible from excess dirt and dust, corrosive fumes and vapors, and strong magnetic fields.

CHAPTER 6
ENGINEERING DRAWINGS

This chapter contains a list of the standard block schematics, and engineering drawings necessary for understanding and maintaining the Synchronizer. The drawings are listed in alphanumeric sequence and are contained within volume 3 of the PDP-10 Peripheral Engineering Drawing set.

Engineering Drawings

Drawing Number	Title	Revision
D-BS-RC10-0-AR1 (Sheet 1)	Assembly Register Number 1	
D-BS-RC10-0-AR1 (Sheet 2)	Assembly Register Number 1	
D-BS-RC10-0-AR2 (Sheet 1)	Assembly Register Number 2	
D-BS-RC10-0-AR2 (Sheet 2)	Assembly Register Number 2	
D-BS-RC10-0-ARD	AR Data Gate	
D-BS-RC10-0-BWL	Display Connectors	
D-BS-RC10-0-CC	Channel Control	B
D-BS-RC10-0-CXR	Condition Register	A
D-BS-RC10-0-DC	Disk Connectors	
D-BS-RC10-0-DI	Disk Input Interface	
D-BS-RC10-0-DO (Sheet 1)	Disk Output Interface	
D-BS-RC10-0-DO (Sheet 2)	Disk Output Interface	
D-BS-RC10-0-DTC	Data Transfer Control	A
D-BS-RC10-0-IBC	I/O Bus Control	A
D-BS-RC10-0-IC (Sheet 1)	Channel and IOB Connectors	
D-BS-RC10-0-IC (Sheet 2)	Channel and IOB Connectors	
D-BS-RC10-0-IOB	I/O Bus Transmitters	
D-BS-RC10-0-IOBD	IOB Receivers	
D-BS-RC10-0-LPR	Longitudinal Parity Register	
D-BS-RC10-0-SC	Search Control	B
D-BS-RC10-0-SCM	Sector Counter MPX	
D-BS-RC10-0-SCT	Sector Counter	A
D-BS-RC10-0-SWP	Switch Panel	
D-BS-RC10-0-TPC (Sheet 1)	Track Protect Comparator	
D-BS-RC10-0-TPC (Sheet 2)	Track Protect Comparator	
D-BS-RC10-0-TSR (Sheet 1)	Track Select Register	A

Engineering Drawings (cont)

Drawing Number	Title	Revision
D-BS-RC10-0-TSR (Sheet 2)	Track Select Register	A
D-BS-RC10-0-TERM	Signal Terminations	B
D-IC-RC10-0-4	Power Wiring	
D-FD-RC10-0-F01	Flow Chart Start	
D-FD-RC10-0-F02	Flow Chart Channel Control	
D-FD-RC10-0-F03	Flow Chart Search	
D-FD-RC10-0-F04	Flow Chart Data Control	
D-FD-RC10-0-F05	Flow Chart End	
D-FD-RC10-0-F06	Flow Chart Manual Control	
D-TD-RC10-0-11	Disk Tuning 1	
D-TD-RC10-0-12	Disk Tuning 2	
D-TD-RC10-0-13	Disk Tuning 3	
D-TD-RC10-0-14	Disk Tuning 4	

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