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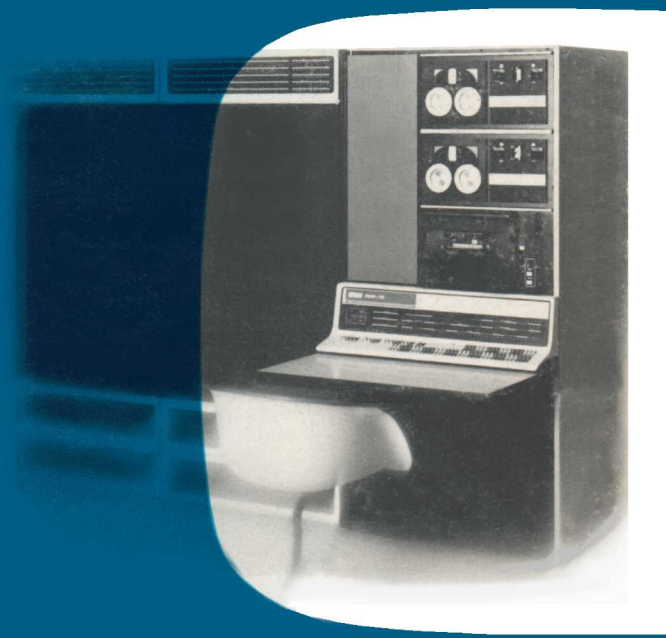
TM10 MAGNETIC TAPE CONTROL

PDP-10



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TM10
MAGNETIC TAPE CONTROL
MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION □ MAYNARD, MASSACHUSETTS

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Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

The TM10A or TM10B Magnetic Tape Control Unit controls a magnetic tape transport conforming to the transport bus specification, such as DEC Model TU-20 or TU-79. Both transports are capable of operating either 7-track or 9-track head configurations.

The TM10A tape control unit (Figure 1-1) uses the PDP-10 I/O bus to transfer data between PDP-10 core memory and tape control. An executive program monitors the data flag interrupt for data requests (either read or write) and data is transferred under the control of the I/O instructions. The executive program monitors the data transfers to determine when to stop operation.

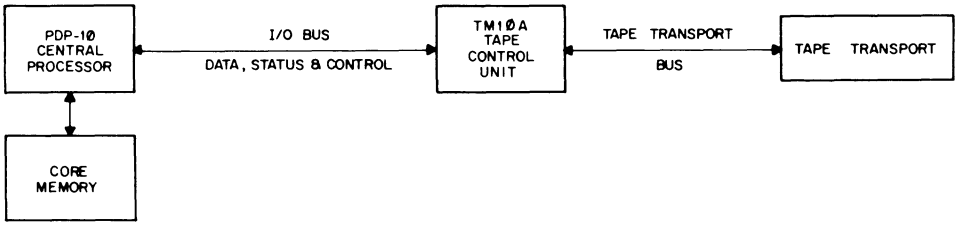


Figure 1-1 TM10A Tape Control Configuration

The TM10B (Figure 1-2) uses the DF10 Data Channel to transfer data between the TM10B and PDP-10 core memory. The computer program initializes the TM10B tape control and thereafter the tape control operates under control of the DF10 Data Channel to transfer data.

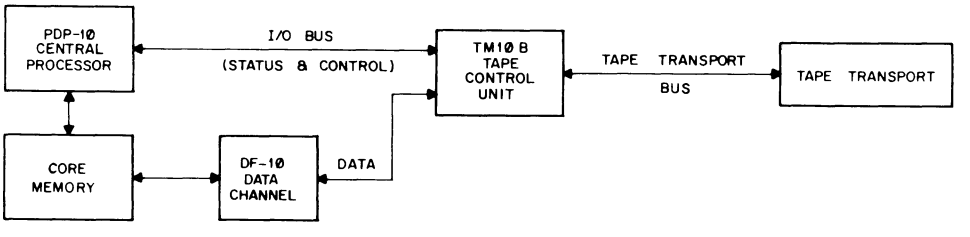


Figure 1-2 TM10B Tape Control Configuration

This manual, together with referenced documents, provides operation and maintenance information for both Model TM10A and Model TM10B Magnetic Tape Control Unit. The level of discussion

assumes familiarity with the PDP-10 Programmed Data Processor, and a working knowledge of DEC logic symbology. For circuits and operations common to both models, no distinction is made between either the TM10A or TM10B. However, for those circuits and operations that differ, this manual makes a clear distinction in describing the individual operation of each model.

1.1 PURPOSE

The TM10 (A or B) functions in either 7-track or 800 bpi 9-track operation; either the 200, 556, or 800 bpi density mode is selectable in 7-track operation. It can operate in either binary (odd) or BCD (even) parity mode. For writing on tape, the 36-bit data words are transferred from core memory to the data buffer in the tape control logic. The buffer logic supplies the data to the tape transport write logic as six 7-bit (6-bit character plus parity bit) characters for 7-track operation (four 9-bit characters for a 9-track operation). For reading, the sequence is reversed, information is read from tape as 7-bit characters and is sent to the data buffer. When a complete 36-bit word has been assembled in the data buffer, a word transfer is initiated to transfer the data buffer word into core memory.

The operations that can be performed by the tape transport, under the control of the TM10 are as follows.

REWIND	The transport rewinds the tape to the load point and stops.
WRITE	N words are written on tape as specified by the program.
WRITE EOF	An EOF (end-of-file) mark character is written on tape.
READ	N words are read from tape as specified by the program.
READ/COMPARE	N words are read from tape as specified by the program. After each complete word is read, it is compared to a word in memory producing a read-compare error when they don't compare.
SPACE FORWARD	The tape is spaced forward N records as specified by the program. If EOT (end-of-tape) is encountered, the tape stops.
SPACE REVERSE	The tape is spaced in reverse for N records as specified by the program. If BOT (beginning-of-tape) is encountered, the tape stops.

1.2 7-TRACK TAPE FORMAT

The 7-track system uses 1/2 in. tape with seven information channels; the format is shown in Figure 1-3. The left side of Figure 1-3 shows the tape in relation to the read and write heads. This tape is composed of a mylar base coated on one side with an iron oxide composition. The oxide, or dull side of the tape, faces the heads with the left edge toward the transport drive plate. The recording density is 200 cpi (characters per inch), 556 cpi, or 800 cpi. The method of recording is non-return-to-zero (NRZ).

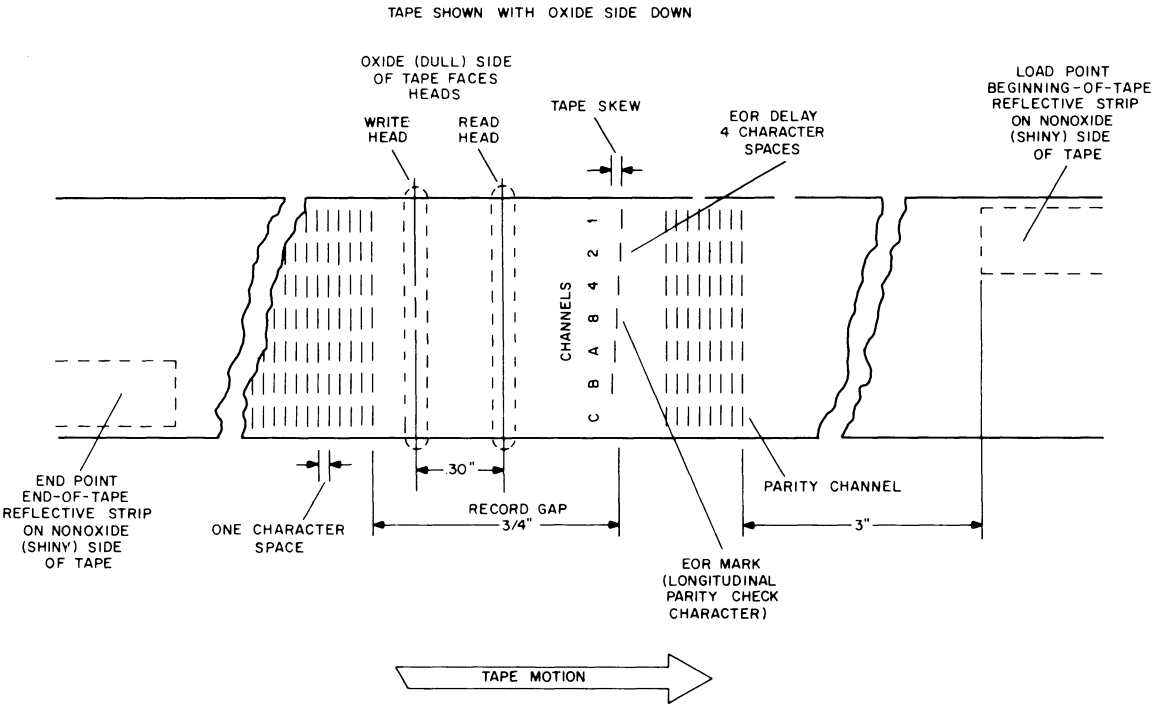


Figure 1-3 7-Track Tape Format

Although the tape has two basic states of remanent magnetization, the remanent magnetic state of the tape at a given position does not determine the value of the bit. A logical 1 is represented by a change of magnetization in either direction. A logical 0 is represented by a constant state of magnetization; therefore, writing a series of characters containing all 0s is equivalent to writing a section of blank tape. Each time a character is transferred into the tape transport write buffer, the NRZ writers produce an equivalent character on the tape. Because of the NRZ method of recording, however, a transfer into the write buffer is not a normal 1s transfer; instead, whenever a 1 bit is to be written in a given tape channel, the corresponding flip-flop is complemented to produce a change in the tape magnetization. When a 0 is written, the corresponding bit of the buffer remains in the initial stage, and there is no change in tape magnetization.

The structure and relative spacing of the individual tape characters are shown in the right portion of Figure 1-3. Each 36-bit computer word is divided into six 6-bit characters. However, the writers contain seven flip-flops corresponding to the seven tape channels; the seventh channel is a lateral parity channel. The parity of the character may be either odd (binary) or even (BCD) as specified by the program. In reading the tape, only 1s are detected.

The smallest unit of information that can be written on the tape is a record; since each computer word contains six 6-bit characters, a record contains N x 6 data characters, where N is the number of words that the processor transfers.

After the last data character of the record is written, the tape travels slightly over four character spaces of blank tape (EOR gap), and then clears the write buffer to produce an end-of-record character, the EOR mark. The bit configuration of the EOR mark produced by clearing the write buffer leaves an even number of 1 bits in each of the seven channels of the tape. All bits of the write buffer start in the 0 state; to end in the 0 state, they must undergo an even number of transitions. For this reason, the EOR mark is referred to as the longitudinal parity-check character (LPCC). Besides detecting changes in magnetization through the read heads, the tape transport also includes a photoelectric system for sensing the beginning and end of the tape.

1.2.1 Load Point and End Point

The load and end points of the tape are marked by reflective strips mounted on the side of the tape away from the head (Figure 1-3). These strips are detected by photodiodes which sense light reflected from them. In writing on a rewound tape, a gap of about 3 in. is left from the load point before writing begins. When the load point is sensed during a fast rewind condition, the sensing device shuts off the high speed rewind. Before the tape movement stops, however, the load point will be passed and the forward tape motion will be enabled to advance the tape back to the load-point strip.

1.3 9-TRACK TAPE FORMAT

The 9-track tape format shown in Figure 1-4 is similar to the 7-track format except that 9-track format has 9 tracks, the CRC (cyclic redundancy check) character has been added, and operation is only in the 800 bpi mode.

The tape control assembles four 8-bit characters per 36-bit word for recording on tape. Each 8-bit character is recorded with a parity bit which can be either odd or even. The first character recorded contains the most significant bits of the PDP-10 36-bit word.

1.3.1 CRC Character

To write the CRC character, the TM10 control incorporates a 9-position register CRC1 through CRC9 with the following track assignments:

Register Position	CR1	CR2	CR3	CR4	CR5	CR6	CR7	CR8	CR9
Track Number	4	7	6	5	3	9	1	8	2

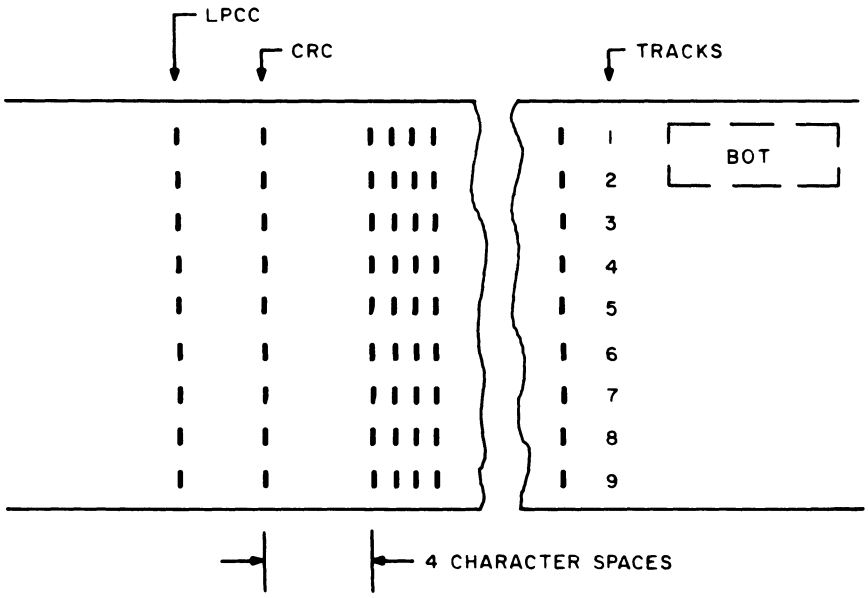


Figure 1-4 9-Track Tape Format

To derive the CRC character, all data characters are exclusive ORed into the CRC register. Between character transfers, the CRC is shifted one position, CRC1 to CRC2, etc., and CRC9 to CRC1. If shifting causes a 1 in CRC1, then the bits shifted into CRC4, CRC5, CRC6, and CRC7 are inverted. After the last data character has been added (exclusive ORed), the CRC register is again shifted and, if CRC1 becomes 1, the CRC4, CRC5, CRC6, and CRC7 are inverted.

To write the CRC character on tape, all bit positions except CRC4 and CRC6 are inverted. An odd parity CRC character occurs if the number of data characters within the block is even, and an even parity CRC character occurs if the number of data characters within the block is odd. The CRC character may contain all 0 bits; in that case, the number of data characters was odd.

The LPCC character for 9-track format is the same as for the 7-track format.

1.4 REFERENCED DOCUMENTS

The following documents contain information related to the TM10 Magnetic Tape Control Unit.

DEC-10-HMAA-D	PDP-10 Maintenance Manual, Volume I
DEC-10-HGAA-D	PDP-10 Systems Reference Guide
DEC-00-14AA-D	TU-20 Instruction Manual
C105	DEC Logic Handbook
DEC-10-I8BA-D	DF10 Data Channel Instruction Manual

CHAPTER 2
OPERATION AND PROGRAMMING

This chapter describes the programming of both the TM10A and TM10B systems to satisfy any detailed programming requirements. Frequently, however, the programmer will not need the detailed procedures for programming the TM10A and TM10B described since the PDP-10 monitor provides call statements to the magnetic tape I/O driver subroutine that satisfy most of his requirements. The applicable PDP-10 document should be consulted for these procedures and call statements.

The TM10A operates under complete control of an executive program for all tape operations. The executive initiates an operation by issuing a CONO 340 (CONO MTC) instruction. The format of this instruction (see Table 2-1 and 2-2) specifies the parameters, the particular tape function, and starts the operation. Request for data transfer (either to or from core memory) is accomplished by use of the data interrupt channel. For example, during a write operation the DATA REQUEST flag is raised to signify that the tape control requires the next 36-bit word to be recorded. The flag generates a DATA interrupt and the executive responds to this interrupt by issuing a DATAO 340 instruction to transfer the 36-bit word to tape control via the I/O bus. Moreover, the executive monitors the number of data transfers to determine when to stop the write operation. It stops the operation by issuing a CONO 344 (CONO MTS) with bit 35 set to 1. The program monitors tape status (Table 2-3) by use of the CONI 344 (CONI MTS) instruction.

Table 2-1
CONO/CONI 340 (MTC) Instructions

Bit	Name	Function
15-17	NEXT UNIT NUMBER	Specifies the next tape transport number selected for operation.
18-20	UNIT NUMBER	Specifies the current tape transport number selected for operation.
21	PARITY	1 = Odd; 0 = Even
22	CORE DUMP	0 = 4 Bytes; 1 = 4-1/2 Bytes
23-26	FUNCTIONS	Tape functions (see Table 2-2 for encoded functions).
27	NEXT UNIT ENAB	When set, enables the NEXT UNIT flag to generate an interrupt.

Table 2-1 (Cont)
CONO/CONI 340 (MTC) Instructions

Bit	Name	Function
28, 29	DENSITY	0 = 200 bpi; 1 = 556 bpi; 2 = 800 bpi; 3 = not used.
30-32	FLAG PIA	Specifies the priority assigned to the flag priority interrupt channel.
33-34	DATA PIA*	Specifies the priority assigned to the data priority interrupt channel.

*Used only on the TM10A, always contains 1s in TM10B.

Table 2-2
TM10 Functions

Function	Octal Code	Description
0000	0	No-op, clear interrupt flags
1000	10	No-op, interrupt when transport becomes idle.
0001	1	Rewind
0010	2	Read
1010	12	Read across record boundaries
0011	3	Read/Compare
1011	13	Rd/Cmp across record boundaries
0100	4	Write
1100	14	Write with long EOR gap
0101	5	Write end-of-file
0110	6	Space forward one or more records
1110	16	Space to end-of-file
0111	7	Space reverse one or more records
1111	17	Space reverse to end-of-file

Table 2-3
Status Register (CONI 344 Format)

Bit	Name	Interrupt
11	CW PAR ERR*	
12	NO-EX MEM*	
13	DATA PAR ERR*	Flag Channel
14	WT CW DONE*	Flag Channel
15-17	Character Counter	
18	TRANSPORT HUNG	Flag Channel
19	REWINDING	
20	BOT (beginning of tape)	
21	ILLEGAL OPERATION	Flag Channel
22	PARITY ERROR	
23	EOF (end-of-file)	
24	EOT (end-of-tape)	
25	READ/COMPARE ERROR	
26	RECORD LENGTH INCORRECT	
27	DATA LATE	
28	BAD TAPE	
29	JOB DONE	Flag Channel
30	TRANSPORT IDLE	
31	CHANNEL ERROR *	
32	WRITE LOCK	
33	7-CHANNEL TRANSPORT	
34	NEXT UNIT	Flag Channel, if enabled
35	DATA REQUEST	Data Channel**

*TM10B only

**TM10A only

The TM10B uses the DF10 data channel facility to transfer data from PDP-10 core memory to the TM10B. An executive program must control the operation of both the DF10 Data Channel and the TM10B. (Refer to the DF10 Data Channel manual for program control of the data channel.) The executive program starts operation when it issues a CONO MTC instruction as it did for the TM10A. But first, the program must issue a DATAO 344 to transfer the initial control word address for the data channel to the TM10B where it is held until the TM10B gains access to the data channel.

2.1 COMMAND BITS

Bits transmitted via CONO MTC, have the meanings shown in Tables 2-1 and 2-2. The unit number bits select one of eight transports. The parity bit selects even or odd parity checking; 0 for even, 1 for odd (preferred parity is odd). The core dump bit should be used with 9-channel transports only. With the core dump bit = 1 and 9-channel tape, the TM10 writes out 36-bit words onto 9-channel tape by splitting the data up among five 8-bit bytes.

Function encoding is shown in Table 2-2. A detailed description of each function is provided in the following paragraphs.

The NEXT UNIT INTERRUPT ENABLE is used in conjunction with the no-op function to allow testing of the transport status bits. If the control is not free when a CONO MTC is given, there will be a delay until the current transport can be deselected and the new one selected. The next unit interrupt allows the program to examine the transport status bits at the earliest opportunity. Without the enable bit, the next interrupt will occur when the transport becomes ready (which may be long delayed, by a rewind for instance).

Any one of three bit densities may be selected, 200 bpi, 556 bpi, or 800 bpi. The encodings for these are 00, 01, and 10, respectively; with encoding 11 currently acting the same as 10, but reserved for future revisions. If 9-track tape is being used without the core dump bit, the program must select 800 bpi.

2.2 STATUS BITS

Table 2-3 shows status bits as sensed by the CONI instruction. Any of six status bits shown in Table 2-3 can cause a flag's channel interrupt. TRANSPORT HUNG means that the TM10 has waited for one second and the selected transport has not completed its operation or else has been switched off-line during an operation.

ILLEGAL OP signifies that an improper command has been issued, such as write with the file protect ring out (write lock on). JOB DONE means that the TM10 has completed its command and is ready for a new command. The conditions under which JOB DONE is set are described separately

for each function. NEXT UNIT causes an interrupt only if the last command had the NEXT UNIT ENABLE bit a 1. NEXT UNIT means that the previous transport has been given a stop signal and the control is not tied up processing a command.

DATA REQUEST causes an interrupt on the data PI channel. This bit is turned off by a DATAO or DATAI MTC instruction, whichever is appropriate to the tape function.

The PARITY ERROR signifies incorrect parity, either lateral or longitudinal. Data that is written is read back and automatically checked for parity. EOF (end-of-file) means an end-of-file record was read from the tape. Both PARITY ERROR and EOF can be 1 during an operation, and yet be 0 at JOB DONE. In particular, if an end-of-file is read with odd parity, the PARITY ERROR bit will be on until the end of record when the control detects the end-of-file situation and turns off the PARITY ERROR bit. Also, when spacing reverse, if the lngitudinal parity character and the last data byte of any record are both end-of-file characters, the EOF bit will come on until the next-to-last byte is read.

The READ/COMPARE ERROR bit means that the data read from the tape was not the same as the data sent out by a DATAO MTC, during a READ/COMPARE operation. If the READ/COMPARE ERROR bit becomes 1, there are no further data requests or other interrupts until the end-of-record.

RECORD LENGTH INCORRECT is valid only for a READ or READ/COMPARE operation. See the explanation of READ below for a description of this bit.

DATA LATE means that the program did not respond quickly enough to a data request and thus has lost data. During a read operation there are no further interrupts until the end-of-record. During a write operation, the last word is written a second time followed by an end-of-record.

BAD TAPE means data was seen in the end-of-record gap. This could indicate missed characters or noise in the end-of-record gap, either of which are to be blamed on faulty tape.

The following four bits are always 1 in the TM10A.

The CW PAR ERR flag means that the DF10 channel encountered a core memory parity error when fetching a control word. This bit does not cause an interrupt but comes on coincidently with JOB DONE.

The NON-EX MEM bit signifies that the DF10 channel encountered NON-EXISTENT memory on a core memory reference. This bit does not cause an interrupt but comes on coincidently with JOB DONE.

The DATA PAR ERR flag means that the DF10 channel encountered a core memory parity error when fetching a data word. This bit causes an interrupt on the flag channel. This bit is cleared by CONO 344, 20.

The WT CW DONE flag indicates that the DF10 channel has written the current control word into initial address +1 (as requested). This bit causes an interrupt. It is cleared by CONO 344, 10.

The OR of these four flags appears in bit 31 of the CONI 344 status word as CHANNEL ERROR. In the TM10A, CHANNEL ERROR is always 0.

In addition to the two bits to clear channel flags, the CONO 344 has the WRITE CONTROL WORD bit (CONO 344, 4). This bit forces the DF10 to write its current control word into memory, a process that may be delayed by up to 170 μs. (See WT CW DONE above.) For the TM10B, if CW PAR ERR or NON-EX MEM comes on, no further data transfers take place and the tape will stop at the end of whatever record is in progress. If DATA PAR ERR is on, the channel will attempt to complete its command list. To stop the function immediately and get a JOB DONE at the end of the current record, the program may issue CONO 344, 1.

2.3 STOP BIT

The instruction CONO MTS, 1 sets a stop bit in the TM10. During a write operation, this bit indicates that the last word has been sent to the TM10. During a read or read/compare operation, this bit indicates that the program has finished with the current record and will not transfer any more words. During a spacing operation, this bit means stop at the end of the current record. This bit is operational in the TM10B but is used only in abnormal situations, such as data parity error.

2.4 TAPE FUNCTIONS (TM10A)

2.4.1 NO-OP (0)

Clears all status bits except those associated with the transport and NEXT UNIT.

2.4.2 NO-OP (10)

Loads a new current transport number and sets JOB DONE when the transport becomes ready. Note the NEXT UNIT ENABLE bit description.

2.4.3 REWIND (1)

Rewinds the selected transport. Sets JOB DONE as soon as the transport is up to speed. To interrupt at the end of a rewind, wait for JOB DONE and then use NO-OP (10).

2.4.4 READ (2)

Data is read in the forward direction only. The parity and density must be set the same as when the data was written. ILLEGAL OP is set if the transport is 9-channel and neither 800 bpi nor core dump mode is selected. The DATA REQUEST flag is raised whenever a 36-bit word is ready for

the processor. JOB DONE is set at the end of record. If the program issues a CONO MTS, 1 after the last word in a record is read, the RECORD LENGTH INCORRECT flag stays off; this flag comes on if the record ends prematurely (the program never issues CONO MTS, 1; or does so late) or if another data word follows the CONO MTS, 1; in the latter case, the following words are ignored. DATA LATE is set when the control assembles a 36-bit word and the program has not done a DATAI for the previous 36-bit word. The average DATAI rate must equal the word rate from the tape transport. The maximum time between DATAI's assuming the most favorable possible timing, is 2-1/6 times the word rate for 7-channel tape, 2-1/5 for 9-channel core dump mode, and 2-1/4 for 9-channel compatible mode. If an end-of-file is encountered in READ mode, there are no DATA REQUESTS and the EOF flag will be set along with JOB DONE.

2.4.5 READ ACROSS RECORD BOUNDARIES (12)

Like READ (2), except that JOB DONE is set only at the first end-of-record after an error, or at an end-of-file, or after CONO MTS, 1 is given, or if the number of characters in a record is not a multiple of six for 7-channel tape. Thus, a single BLKI can read in several records.

2.4.6 READ/COMPARE (3)

Data is read from the tape by the control and the program sends data from core via DATAO. The two words are compared in the control and, if equal, the process continues with the next pair of words. If not equal, there are no further DATA REQUEST flags and the READ/COMPARE ERROR flag is set at the end of record. The first DATA REQUEST occurs when the tape begins to move.

For other flags, modes and timing considerations, see READ mode.

2.4.7 RD/CMP ACROSS RECORD BOUNDARIES (13)

Like READ ACROSS RECORD BOUNDARIES (12), but compares.

2.4.8 WRITE (4)

Data may be written in any of three densities (200 bpi, 556 bpi, or 800 bpi) on 7-channel transports, at 800 bpi in IBM-compatible format on 9-channel transports, or at any of three densities in core dump mode on 9-channel transports. Either even or odd parity may be selected. When selecting even parity, care must be taken to never write a character of all 0s on tape, since such a character will be ignored while reading. A WRITE command to a write-locked tape results in the ILLEGAL OP flag and no tape motion. To terminate a record, the program must follow the last DATAO with the CONO MTS, 1. There will be no further data requests; JOB DONE is set when the read-after-writing

circuit reads and checks the longitudinal parity. The BAD TAPE flag could be set at this time. If the CONO MTS, 1 is not given, the TM10A raises the DATA LATE flag, rewrites the last data word, and then writes an end-of-record and stops. The first DATA REQUEST occurs when the tape starts moving. Other timing considerations are the same as for READ mode.

2.4.9 WRITE WITH EXTENDED EOR GAP (14)

Similar toWRITE (4)except that a 3-in. gap of blank tape (instead of 3/8 in.) is written prior to the start of the WRITE operation.

2.4.10 WRITE END OF FILE (5)

An end-of-file character and end-of-file gap are written on the tape. The parity is set automatically. The density must be set equal to that for the rest of the data on the tape (as must the CORE DUMP mode bit for 9-channel tape and densities other than 800 bpi.) The END-OF-FILE and JOB DONE flags are raised when the function is completed. ILLEGAL OP is raised and no tape motion results if the tape is write-locked. BAD TAPE nad PARITY ERROR can also be set indicating miswriting.

2.4.11 SPACE FORWARD (6)

Any number of records may be spaced with a single SPACE FORWARD command. For each record, the TM10A raises the DATA REQUEST flag. The program should respond with a DATAO MTC, or BLKO (the data word itself is irrelevant). If the program does not respond (or responds late), the TM10A spaces one record and stops the tape. If the program responds, the TM10 spaces one record and raises the DATA REQUEST flag again. To space a second record, the program must give another DATAO MTC. If the program gives a CONO MTS, 1 the TM10 does not raise the DATA FLAG again and stops at the end of the current record. To summarize: the TM10A spaces one record for each DATAO from the program except that one record is spaced for 0 DATAOs. The TM10 stops spacing at an end-of-file, regardless of DATAOs. The TM10 also stops spacing at the first end of record following the EOT marker. JOB DONE is raised when the TM10 has finished spacing the last record.

The same density in which the tape was written must be selected. At lower density, the TM10 can miss an end-of-file mark. Parity is not relevant. CORE DUMP must be selected to allow a density of 200 bpi or 556 bpi on 9-channel tape. Other relevant flags are BAD TAPE and EOF.

2.4.12 SPACE FORWARD TO END OF FILE (16)

Spaces any number of records and stops only for END-OF-FILE or EOT. The DATA REQUEST flag is never raised. Otherwise, this function is similar to SPACE FORWARD (6).

2.4.13 SPACE REVERSE (7)

Spaces one or more records in reverse. The control of the number of records spaced is the same as forSPACE FORWARD (6). Regardless of the number of DATAOs given, the TM10 stops a SPACE REVERSE operation at an END-OF-FILE or at the BOT (beginning of tape, or loadpoint) marker. The EOT marker is ignored. ILLEGAL OP is raised if SPACE REVERSE is attempted and the tape is at the BOT at the start of the operation (no tape motion results). Otherwise, this function is similar to SPACE FORWARD (6).

2.4.14 SPACE REVERSE TO END-OF-FILE (17)

Spaces any number of records in reverse and stops only for END-OF-FILE or BOT. The DATA REQUEST flag is never raised. Otherwise, this function is similar to SPACE REVERSE (7).

2.5 TAPE FUNCTIONS (TM10B)

2.5.1 NO-OP (0)

Clears all status bits except those associated with the transport and NEXT UNIT.

2.5.2 NO-OP (10)

Loads a new current transport number and sets JOB DONE when the transport becomes ready or sets TRANSPORT HUNG after one second. Note the NEXT UNIT ENABLE bit description.

2.5.3 REWIND (1)

Rewinds the selected transport. Sets JOB DONE as soon as the transport is up to speed. To interrupt at the end of a rewind, wait for JOB DONE and then use NO-OP (10).

2.5.4 READ (2)

Data is read in the forward direction only. The WC register in the data channel specifies the number of words to read. The parity and density must be set the same as when the data was written. ILLEGAL OP is set if the transport is 9-channel and neither 800 bpi nor core dump mode is selected. JOB DONE is set at the end of record. Tape begins to move when the data channel is seized. If the data channel terminates operation after the last word in a record is read, the RECORD LENGTH INCORRECT flag stays off; this flag comes on if the record ends prematurely (data channel never terminates

operation) or if another data word follows the data channel termination; in the latter case, the following words are ignored. DATA LATE is set when the control assembles a 36-bit word and the data channel has not transferred the previous 36-bit word.

2.5.5 READ ACROSS RECORD BOUNDARIES (12)

Like READ (2), but JOB DONE is set only at the first end-of-record after an error, or at an end-of-file, or after the data channel terminates operation, or if the number of characters in a record is not a multiple of six for 7-channel tape.

2.5.6 READ/COMPARE (3)

Data is read from the tape by the control and the program sends data from core data channel. The WC register in the data channel specifies the number of words to read/compare. The two words are compared in the control and, if equal, the process continues with the next pair of words. If not equal, the READ/COMPARE ERROR flag is set at the end of record.

In READ/COMPARE mode (3 or 13), the data channel supplies the first data word before the TM10 is ready to receive it. Therefore, the first word of data from memory must be a 0. The second word from memory must match the first word from tape, and so on. The 0 word may be inserted conveniently into the data stream through use of the data channel's data-chaining facility. If the first word from memory is not 0, a READ/COMPARE ERROR always occurs.

For other flags, modes, and timing considerations, see READ mode.

2.5.7 RD/CMP ACROSS RECORD BOUNDARIES (13)

Like READ ACROSS RECORD BOUNDARIES (12), but compares.

2.5.8 WRITE (4)

Data may be written in any of three densities (200 bpi, 556 bpi, or 800 bpi) on 7-channel transports, at 800 bpi in IBM-compatible format on 9-channel transports, or at any of three densities or in core mode on 9-channel transports. The WC register in the data channel specifies the number of words to write. Either even or odd parity may be selected. When selecting even parity, care must be taken never to write a character of all 0s on tape, since such a character will be ignored while reading. A WRITE command to a write-locked tape results in the ILLEGAL OP flag and no tape motion. To terminates a record, the data channel terminates CHANNEL BUSY. JOB DONE is set when the read-after-writing circuit reads and checks the longitudinal parity. The BAD TAPE flag could be set at this time.

2.5.9 WRITE WITH EXTENDED EOR GAP (14)

Similar toWRITE (4)except that a 3-in. gap of blank tape (instead of 3/8 in.) is written prior to the start of the WRITE operation.

2.5.10 WRITE END-OF-FILE (5)

An end-of-file character and end-of-file gap are written on the tape. The parity is set automatically. The data channel is not used for this operation. The density must be set the same as for the rest of the data on the tape (as must the CORE DUMP mode bit for 9-channel tape and densities other than 800 bpi.) The END-OF-FILE and JOB DONE flags are raised when the function is completed. ILLEGAL OP is raised and no tape motion results if the tape is write-locked. BAD TAPE and PARITY ERROR can also be set indicating miswriting.

2.5.11 SPACE FORWARD (6)

For this operation, the data channel uses its WC register to count the number of records to space. When the specified number of records are spaced, the data channel terminates operation. However one record is spaced for a 0 WC. The TM10 stops spacing at an end-of-file, regardless of the WC and also at the first end of record following the EOT marker. JOB DONE is raised when the TM10 has finished spacing the last record.

The same density at which the tape was written must be selected. At lower density, the TM10 can miss an end-of-file mark. Parity is not relevant. CORE DUMP must be selected to allow 200 bpi or 556 bpi on 9-channel tape. Other relevant flags are BAD TAPE and EOF.

2.5.12 SPACE FORWARD TO END-OF-FILE (16)

Spaces any number of records and stops only for END-OF-FILE or EOT. The data channel is not used for this operation. Otherwise, this function is similar to 6-SPACE FORWARD.

2.5.13 SPACE REVERSE (7)

Spaces one or more records in reverse. Control of the number of records spaced is the same as forSPACE FORWARD (6). Regardless of the records specified by the data channel, the TM10 stops a SPACE REVERSE operation at an EOF or at the BOT (beginning of tape, or loadpoint) marker. The EOT marker is ignored. ILLEGAL OP is raised if SPACE REVERSE is attempted and the tape is at the BOT at the start of the operation (no tape motion results). Otherwise, this function is similar to SPACE FORWARD (6).

2.5.14 SPACE REVERSE TO END-OF-FILE (17)

Spaces any number of records in reverse and stops only for EOF or BOT. The data channel is not used. Otherwise, this function is similar to SPACE REVERSE (7).

2.6 TM10 COMMAND TIMING

At an end of record, the TM10A raises the JOB DONE flag before stopping the tape. If the program supplies a new command to the same transport requiring the same direction of motion as the previous command, the tape never stops moving provided the program does not take too long. The exact duration of "too long" depends on the stopping characteristics of the particular transport involved. If the program is slow, or if the direction of motion is different for the new command, the tape is automatically stopped and the command is held up until the transport becomes idle. If the new command is for a different transport number, the TM10 retains the old transport number until the appropriate time for giving the stop signal. Thus, CONI MTS will return the former unit number until that unit is stopped, whereupon the unit number is automatically changed to the new one. The TM10 then waits for the newly selected unit to become idle before starting it in motion. If this waiting period is more than 1s, the TRANSPORT HUNG flag is raised.

If a CONO MTC, is given before the JOB DONE flag comes on, the command in progress is aborted.

2.7 9-TRACK TAPE

Nine-track tape provides eight data channels and one parity bit across the width of the tape. To be IBM compatible, the program must select 800 bpi and odd parity. In this mode, four 8-bit bytes are written from each 36-bit word and 4 bits are ignored. The bytes are left justified packed as by the byte instructions. During reading, the rightmost 4 bits of the 36-bit words are loaded with the parity error bits corresponding, left to right, with the 4 data bytes.

Nine-track tape provides an error correcting feature whereby a suitable program can detect if errors are in one channel of the tape, or more than one channel. Once the bad channel is identified, the record can be reread and the bit in the bad channel will be complemented on every parity error. This feature is based on the cyclic redundancy character (CRC). During writing, a suitable CRC character is computed and automatically written on the tape in the end of record gap by the TM10. During reading, the CRC character from the tape is obtained by waiting for JOB DONE (and doing a CONO MTS, 2 in the TM10A only followed by a DATAI MTC, without waiting for the DATA REQUEST flag. See the Proposed American Standard for Recorded Magnetic Tape, Communications of the ACM, Volume 9, Number 4, April 1966, page 285, for further details.

In order to facilitate the use of 9-channel tape for binary data applications (36-bit words) and to take advantage of the two extra channels, the TM10 has a CORE DUMP mode. In this mode the program may select any density. Thirty-six bit words are written in 5 bytes (as opposed to 6 on a 7-channel tape). The first four bytes are the four leftmost 8-bit bytes of the word. The fifth byte contains 0s in the left two bits and the rightmost six bits of the data word in the right six bits. During reading, the two bits that overlap in the above scheme are ORed together. The parity error bits are not obtainable in this mode. However, the CRC character is written correctly. The end-of-file character on 7-channel tape is 17 (octal) with a 0 parity bit. On 9-channel tape, the end-of-file is 023 with a 0 parity bit. In either case, the end-of-file is a 3-in. gap of erased tape followed by a single-character record. On 9-channel tape, the end-of-file record does not include a 0 CRC character.

CHAPTER 3
THEORY OF OPERATION

This chapter provides a complete description of the theory of operation of the TM10A and TM10B Magnetic Tape Control Units. General and summary information of the data channel is presented first. This is followed by a detailed logic description of the circuits common to both the TM10A and TM10B; where the TM10A and TM10B differ is also fully discussed. The logic drawings referenced in this discussion are contained in Volume III of the PDP-10 Peripheral Device Engineering Drawing Set, DEC-10-I6CA-D, these logic drawings are referenced only by the last suffix. For example, logic drawing D-BS-TM10-0-CM1 is referenced as drawing CM1.

3.1 DF10 DATA CHANNEL DESCRIPTION

A complete description of the DF10 Data Channel is given in the DF10 Data Channel Instruction Manual. However, in order to understand the operation of the TM10B, it is necessary to understand how the DF10 communicates with the TM10B. Therefore, a brief description of the DF10 is given below.

This description is relevant for the TM10B and not for the TM10A. The MTS DATAO instruction is issued to provide an initial control word address. The control word address is held by the TM10B until it gains access to the data channel. When the TM10B gains access to the data channel, it sends the initial control word address to the data channel which stores this address in the control word address register. The data channel then fetches the control word normally consisting of WC (word count) and DA (data address). The WC and DA are stored in their respective data channel registers. The WC register specifies the 2's complement of the number of data words to transfer and the DA specifies the core memory location minus 1. DA is incremented by 1 prior to the first transfer. After a word transfer between core memory and the device communicating with the data channel, the WC is decremented and the DA is incremented. When the WC is reduced to 0, the number of words initially specified have been transferred. The control word address register is incremented and the next control word is fetched from core memory. If the control word contains all 0s, the end of communications is specified and the data channel terminates operation.

A number of devices can be connected to the data channel; however, the data channel communicates with only one at a time. To establish, maintain, and terminate communications, the following signals are exchanged between device and data channel.

DATA BUS	This incorporates 36 bidirectional data pulse lines. These signals are 100 ns negative going pulses swinging from ground to -3V.
CHANNEL PULSE	This 100 ns negative going pulse is sent from the channel. It accompanies the data pulses when the channel is sending data to the device. It also signifies a readiness to receive data when the device is trying to send data to memory.
DEVICE PULSE	The signal is similar in function to the channel pulse signal. It accompanies the data when the device is sending, and signifies readiness to receive when data flow is toward the device.
CHANNEL START	This is a level (-3V for true) which is sent from the device to the channel. It will start the channel into operation when asserted.
SA WRITE	This signal controls the direction of data transfer. When true, it signifies the device is writing some medium (reading memory). The timing is the same as that for the CHANNEL START.
CHANNEL BUSY	This signal comes from the channel and is asserted (-3V) sometime after CHANNEL START is asserted from the device. The device must not put anything on the bus until this signal is asserted. When this signal goes false after having been true, the channel has terminated for one reason or another. CHANNEL START and CHANNEL BUSY must all be false for at least 400 ns prior to reassertion of CHANNEL START.
WRITE CONTROL WORD REQUEST	This negative 100 ns pulse from the device causes the channel to store the current contents of the data address register and the control word address register into memory location B + 1, where B (an even number) is the channel initial control word address. The contents of the control word address register go into bit positions 0-17 and the contents of the data address register into 18-35. Upon any channel termination, an automatic WRITE CONTROL WORD REQUEST is made.
WRITE CONTROL WORD COMPLETE	This pulse from the channel signals the completion of the operation requested above. This pulse does not occur on the automatic transfer.
NO SUCH MEMORY	This pulse is sent from the channel as CHANNEL BUSY goes off and indicates that the memory addressed failed to respond.
CONTROL WORD PARITY ERROR	If a control word is fetched from the memory by the channel and this word has a parity error, CHANNEL BUSY is reset and this pulse is sent to the device from the channel.
DATA WORD PARITY ERROR	This pulse accompanies the data and the CHANNEL PULSE when a data word which was read from memory with a parity error is sent to the device.

The I/O devices attached to a data channel are arranged as shown in Figure 3-1 (only the pertinent signals are shown). In order for a device to gain access to the data channel, it must generate a CHANNEL START and receive a CHANNEL BUSY. If a device is not actively engaged with the data channel, it relays the CHANNEL START and CHANNEL BUSY. A device that is relaying CHANNEL START is prevented from generating its own CHANNEL START. A device that is busy with the data channel does not relay CHANNEL BUSY.

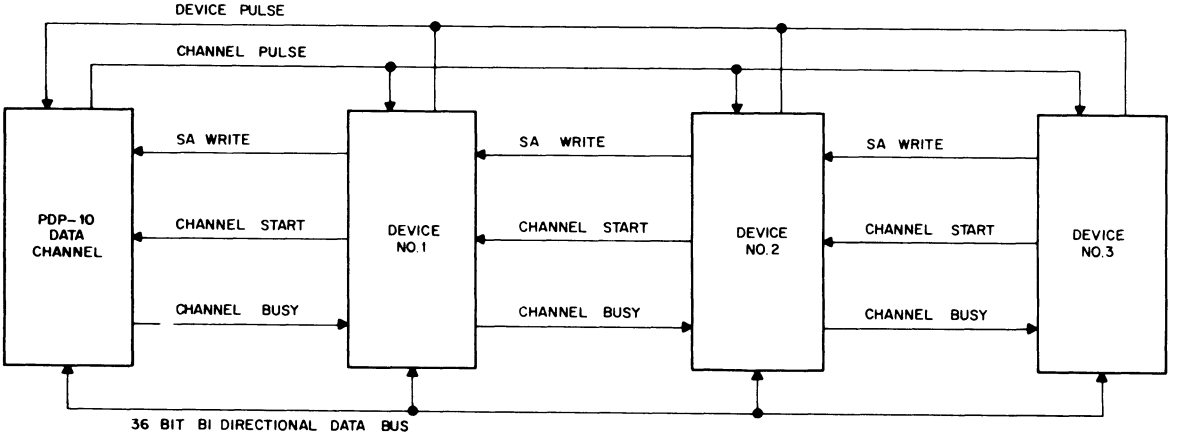


Figure 3-1 Data Channel Interface

To further examine data channel communication, assume that devices 1 and 2 are not busy and device 3 initiates communication by asserting its CHANNEL START signal. CHANNEL START is applied to device 2 and since device 2 is not busy it relays the CHANNEL START. Similarly, device 1 relays CHANNEL START. The data channel acknowledges the CHANNEL START by asserting the CHANNEL BUSY. The data channel does not know which device requested access; the only thing it knows is that it received a CHANNEL START and it responds by asserting CHANNEL BUSY. Furthermore, the data channel responds only to stimulus of the control signals by transferring data to and from the data bus or starting or stopping operation. It is the responsibility of devices to determine which has access.

Since devices 1 and 2 are not busy, they relay the CHANNEL BUSY signal to device 3. Upon receipt of CHANNEL BUSY, device 3 has access to the data channel and can communicate via the data bus. A device requires two conditions to gain access to the data channel: the assertion of its own CHANNEL START and the receipt of CHANNEL BUSY.

To demonstrate this dual requirement, assume that device 2 is communicating with the data channel. It has asserted its CHANNEL START and received a CHANNEL BUSY. It does not relay CHANNEL BUSY to device 3. If now, device 3 attempts communications, it can assert at CHANNEL START since it is not relaying CHANNEL START. Since device 2 is already generating a CHANNEL START, it essentially ignores the CHANNEL START from device 3. The CHANNEL BUSY is not relayed to device 3; therefore, device 3 does not gain access to the data channel because of the two requirements: assertion of CHANNEL START and receipt of CHANNEL BUSY. Device 3 now must wait until device 2 has finished with the data channel.

Either device 2 or the data channel can terminate operation. The data channel terminates operation by removing CHANNEL BUSY and the device responds by negating CHANNEL START. After termination, device 3 is free to communicate; however, the data channel requires at least 400 ns time between the negation of CHANNEL BUSY and CHANNEL START and the assertion CHANNEL START. In this case, this requirement is imposed upon device 2 (or any other device that is generating or relaying CHANNEL START and receive the on-to-off transition of CHANNEL BUSY). When termination occurs, all devices must inhibit the generation or relaying of CHANNEL START for 400 ns.

3.2 NRZ RECORDING

The actual technique of recording on magnetic tape is called the non-return-to-zero (NRZ) method. In this method, a reversal of the direction of magnetization in a channel represents a 1 bit, a lack of reversal represents a 0 bit. Writing is achieved by using a flip-flop to control the direction of magnetizing current in each channel write head; the group of flip-flops is called the write buffer. By applying the 1s lines to the complement inputs of the write-buffer, each channel reverses its flux only when a 1 bit is to be written for a character. Further, the write buffer accumulates the LPCC (longitudinal parity check character) to be written as an EOR character. When the write buffer is cleared at EOR time, the LPCC character is thus written automatically.

The NRZ recording method provides self-clocking during reading since a transition (or flux reversal) in any channel, signifying a 1 bit for that character in that channel, is used to strobe or sense all seven channels for that character. Ideally, all transitions for a single character would be sensed simultaneously by the 7-channel read head. In fact, tape skew makes these transitions (if more than one in a single character) nonsimultaneous on reading. There may be a difference in alignment of the read head with respect to the write head recording the tape (static skew). The tape alignment to the read head is apt to vary during tape travel (dynamic skew). To accommodate these timing variations between channels due to skewing, the first detected transition for a character initiates a delay before the character is strobed. This delay is selected to accept the maximum skewing produced at the linear tape transport speed with the designated tape density.

A simplified block diagram of the tape system write and read paths for a single channel is presented in Figure 3-2. The write path (WP) is shown at the top of the figure. The WRITE flip-flop in the write amplifier is complemented at each WP pulse if the data buffer for that particular character contains a 1. When gated by a WRITE ENABLE signal, the write amplifier drives one or the other of the two opposing directions at the write head. If the WRITE ENABLE level is not present, no current flows through the coil. Whenever a 1 is to be written on a tape, the WRITE flip-flop is complemented by the WP pulse. The transition of the WRITE flip-flop terminates the current in one direction and starts it in the other direction, changing the direction of the tape magnetization, and thus writing a 1 on tape. As long as the WRITE flip-flop remains in the same state, the current flows in the same direction, and 0s are written on the tape. The tape is then magnetized in the same direction over a series of character spaces.

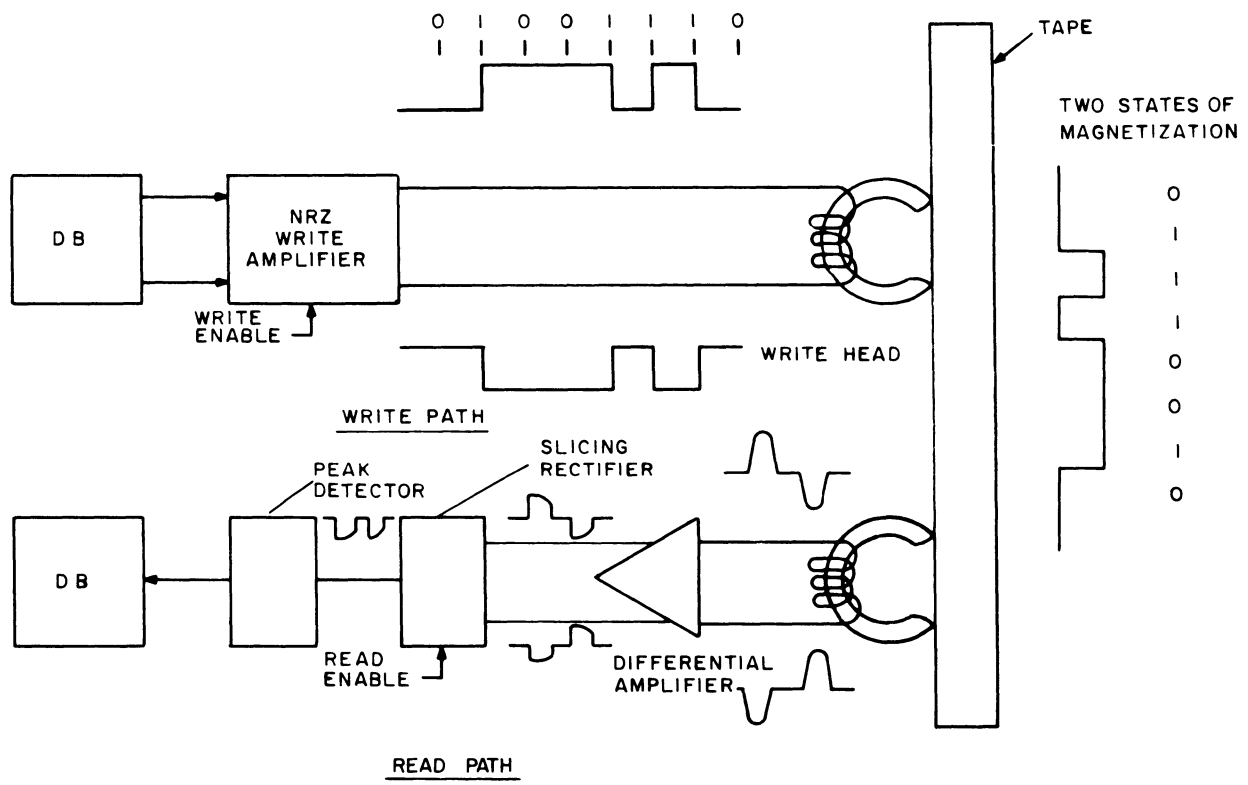


Figure 3-2 Tape Write and Read Signal Flow

The read path is shown at the bottom of Figure 3-2. The tape reaches the read heads shortly after traversing the write head. As long as the direction of tape magnetization remains constant, no current flows through the read head coil. Each change in the direction of tape magnetization induces a current in the read head. The read current produced by two consecutive tape 1s is shown in the waveform near the read head. These signals are applied to a differential read amplifier to provide ampli-

fication for different mode signals, but only fractional amplification for common mode signals. The output of the read amplifier is then sent through a slicing rectifier. The rectifier output pulse is of a single polarity although input pulses are of both polarities from the read amplifier. No slice output is generated, however, unless the input exceeds a designated voltage threshold level. A low-level noise input cannot generate an output pulse. Next, the slicing rectifier output is applied to a peak detector. The peak detector produces a logic pulse output at the peak of the input pulse.

3.3 SYSTEM DESCRIPTION

3.3.1 TM10A

A simplified block diagram of the TM10A is shown in Figure 3-3. Assuming a write operation, the program issues a CONO 340 I/O instruction. It is decoded by the I/O bus control circuits to generate the MTC CONO pulses that load the specified parameters (i.e., write, parity mode, density, etc.) into the command register. The appropriate motion commands are transferred to the selected tape transport. A short delay is implemented to provide the tape inter-record gap. During this delay, the DATA REQUEST signal enables the data interrupt channel to generate an interrupt. The executive program responds to the interrupt by issuing a DATAO 340 which loads the hold register (HR) The program cannot respond quickly enough to load the buffer register (BR) directly before recording (or reading) starts. Therefore, the hold register is provided to buffer the data between the PDP-10 and the buffer register. Whenever the buffer register is empty, the TM10A transfers the data word in the hold register to the buffer register and generates a DATA REQUEST to obtain the next word to be written.

After the inter-record gap delay and buffer register loading, the write operation begins. Assuming 7-track operation, the buffer register 36-bit word must be divided into six 6-bit characters for writing on tape. The character counter sequences the 6-bit character from the data buffer. As a 6-bit character is written from the high-order bits of the buffer register, the character counter is incremented to sequence the next low-order 6-bit character. After the six 6-bit characters from the data buffer are written, the DATA REQUEST is set to initiate another word transfer to the buffer register via the hold register.

Operation continues in this manner until the program determines that the desired number of words have been written, at which time the TM10A tape control is notified via a CONO MTS, 1 instruction. The LPCC character is written and write operation terminates. The tape continues in the forward motion until the read circuits detect the end-of-record passing under the read head. Tape motion ceases, the deceleration delay is initiated (time allotted for tape to stop), and the JOB DONE flag is set.

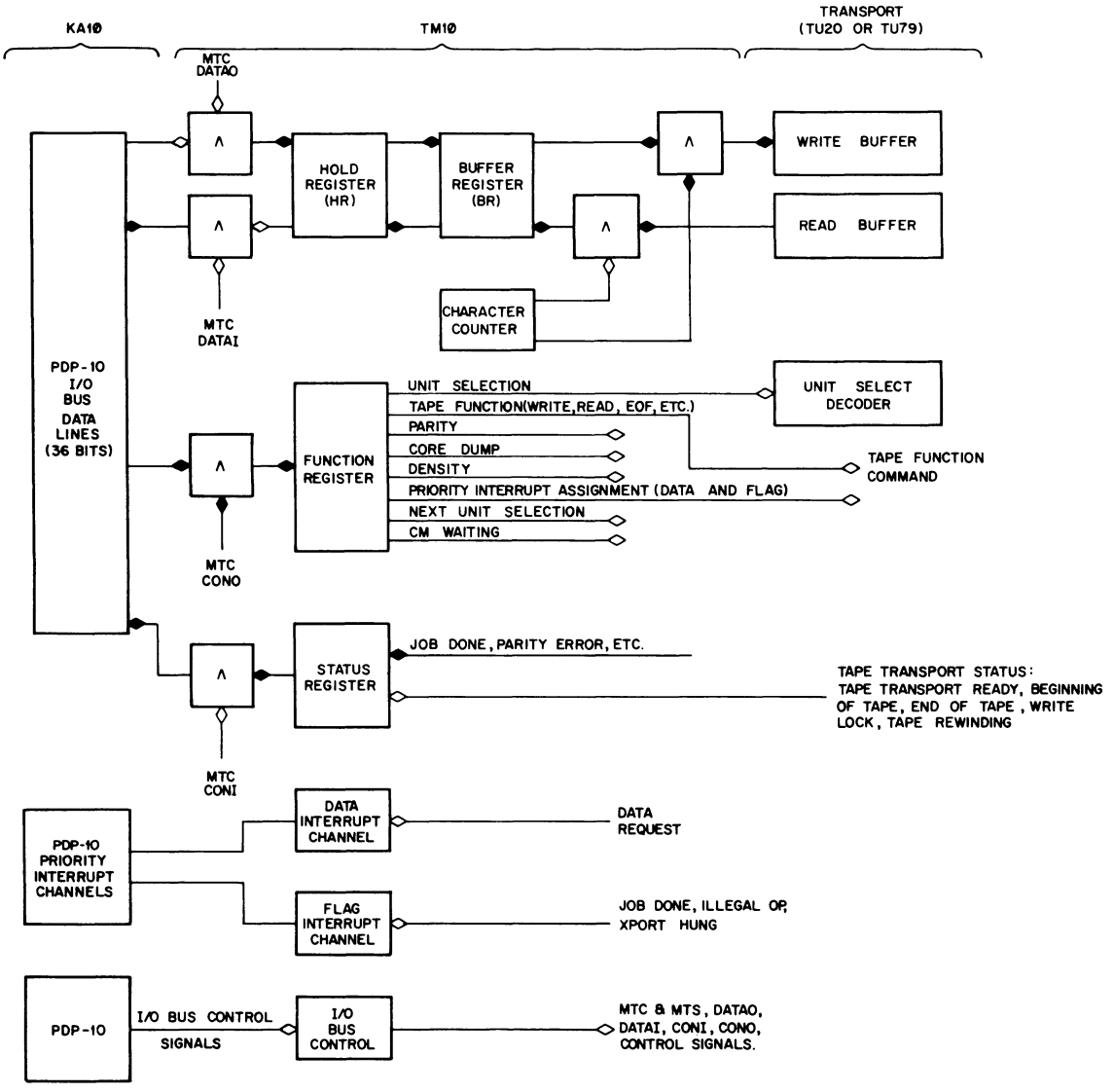


Figure 3-3 TM10A Tape Control Block Diagram

For the read operation, the initial programming sequence is similar to the one for the write operation. As 6-bit characters are read from tape, they are sequenced into the buffer by the character counter. When the buffer register is full the data is transferred to the HOLD register and the DATA REQUEST initiates a programmed transfer of the data into core memory. Operation continues until the read circuits detect the end-of-record.

As shown in Figure 3-3, the tape control status can be transferred to the PDP-10 by using the appropriately coded CONI instructions. Moreover, the JOB DONE flag and the error bits generate an interrupt separate from the DATA REQUEST interrupt.

3.3.2 TM10B

A simplified block diagram of the TM10B is shown in Figure 3-4. Assuming a write operation, the program issues a CONO 340 and a DATAO 344 instruction. The DATAO 344 is decoded by the I/O bus control circuits to generate MTS DATAO which loads the control word initial address register. The content of this register will be subsequently transferred to the DF10. The CONO 340 instruction is decoded to generate the MTC CONO pulses that load the specified parameters (write, read, parity mode, density, etc.) into the function register.

Before writing can begin, the TM10B must gain access to the data channel. Therefore, it makes a request by generating CHANNEL START. If data channel is not busy, it responds with CHANNEL BUSY. The TM10B sends the initial control word address to the data channel. The channel control circuits then generate the OK TO GO signal.

A short delay is implemented to provide the tape inter-record gap delay. The DEVICE PULSE requests the first 36-bit data word to be recorded. The data channel responds by loading the buffer register.

After the inter-record gap delay and buffer register loading, the write operation begins. Assuming 7-track operation, the buffer register 36-bit word must be divided into six 6-bit characters for writing on tape. The character counter sequences the 6-bit character from the data buffer. As a 6-bit character is written from the high-order bits of the data buffer, the character counter is incremented to sequence the next low-order 6-bit character. After the six 6-bit characters from the data buffer are written, the DEVICE PULSE initiates another word transfer to the buffer register via the data channel.

Operation continues in this manner until the data channel fetches a 0 control word signifying that the required data has been recorded. The data channel thus removes the CHANNEL BUSY signal to terminate operation. The LPCC character is written and write operation terminates. The tape

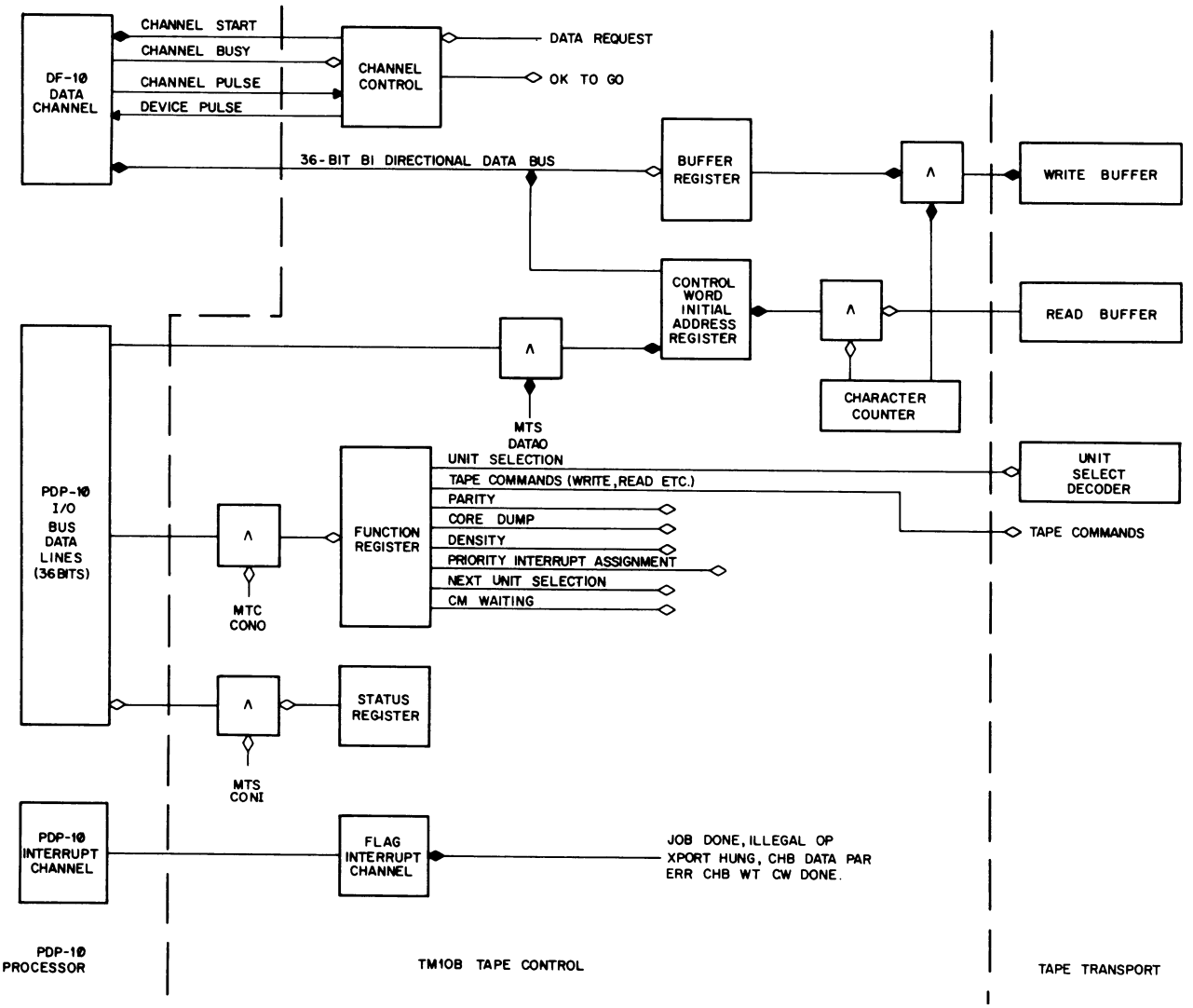


Figure 3-4 TM10B Tape Control Block Diagram

continues in the forward motion until the read circuits detect the end-of-record passing under the read head. Tape motion ceases, the deceleration delay is initiated (time allotted for tape to stop), and the JOB DONE flag is set.

For the read operation, the initial programming sequence is similar to write. As 6-bit characters are read from tape, they are sequenced into the buffer register by the character counter. When the buffer register is full, the DEVICE PULSE initiates a data channel transfer of the buffer register word into core memory. Operation continues until the read circuits detect the end-of-record.

3.4 TM10A INITIAL OPERATION

The MTC CONO instruction loads the parameters (tape function, density mode, unit number, priority interrupt channel numbers, etc.) into the command register as shown on drawing CM1 and CM2. The tape function register (CM FCN0-FCN3) is decoded to specify the operation. Since we are assuming initial operation, the content of CM NEXT UNIT (0-2) register (drawing CM2) is transferred to CM UNIT (0-2) register (drawing CM1). The T GO signal is false at this time. The CM UNIT register (via drawing TB) selects the desired tape drive.

The MTC CONO SET pulse also sets the CM WAITING flip-flop (drawing CM2). After a 1 μs delay, the CM UNIT OK flip-flop is set. If the selected tape unit is ready (signal TB TUR is true), the CM LEGAL TEST pulse is generated. This pulse tests the legal conditions (drawing ST). If any of the following illegal conditions are true, the ST ILLEGAL OP flip-flop is set.

a. Writing on a protected tape (CM WRITING and TB WL are true).

b. Write mode and tape is at end-of-tape (WRITING and TB EOT true).

c. Space reverse and tape at beginning of tape (CM SP REV and TB BOT true).

d. 9-channel operation and not 800 bpi density; and not core dump mode.

If the ST ILLEGAL OP flip-flop gets set, an interrupt is generated (drawing CM2), and the operation terminates. Assuming no illegal operation, the CM LEGAL TEST DONE signal generates CC OK TO GO which fires the CM MT GO pulse. (Note the jumper between H15 pins U and V which is present only on TM10A). The CM MT GO sets the T GO flip-flop (drawing T2) to start the operation as described in Section 3.6. The CM NO-OP DONE pulse (if present) sets the ST JOB DONE flip-flop.

3.5 TM10B INITIAL OPERATION

Operation of the TM10B starts when the PDP-10 processor issues an MTS DATAO instruction to transfer the data channel initial control word initial address and an MTC CONO instruction to set up initial parameters. The MTS DATAO instruction loads the IA27-IA34 (initial address, drawing CC) register with the control word initial address. This will be subsequently transferred to the data channel.

The MTC CONO instruction loads the parameters (tape function, density mode, unit number, priority interrupt channel number, etc.) into the command register as shown on drawing CM1 and CM2. The tape function register (CM FCN0 - FCN3) is decoded to specify the operation. Since we are assuming initial operation, the CM NEXT UNIT 0 - 2 register (drawing CM2) is transferred to CM UNIT 0-2 register (drawing CM1). The T GO signal is false at this time. The CM UNIT register (via drawing TB) selects the desired tape drive.

The MTC CONO SET pulse also sets the CM WAITING flip-flop (drawing CM2). After a 1 μs delay, the CM UNIT OK flip-flop is set. If the selected tape unit is ready (signal TB TUR is true), the CM LEGAL TEST pulse is generated. This pulse tests the legal conditions (drawing ST). If any of the following illegal conditions are true, the ST ILLEGAL OP flip-flop is set.

a. Writing on a protected tape (WRITING and TB WL are true).

b. The write mode specified and the tape is at end-of-tape (WRITING and TS EOT true).

c. A space reverse, specified and tape is at beginning of tape (CM SP REV and TB BOT true).

d. 9-channel operation and not 800 BPI density and not core dump mode.

If the ILLEGAL OP flip-flop gets set, an interrupt is generated (drawing CM1), and the operation terminates. Assuming no illegal operation, the CM LEGAL TEST DONE signal (drawing CM2) sets the CC CHN SYNC (drawing CC) to request access to the data channel. Note on drawing CM2 that the W990 module is removed for TM10B operation. Therefore, we must wait for the CC OK TO GO signal which signifies that the tape control has access to the data channel for those operations that require the data channel. For operations not requiring the data channel, the CC NEED CHANNEL signal (drawing CC) immediately generates CC OK TO GO.

With CC CHN SYNC set, the TM10B requests access to the data channel. The TM10B must now wait until it gains access to the data channel. If the data channel is busy with another device, the TM10B must wait until the data channel has completed its operation. For the ensuing description of channel control, it is assumed that the data channel is initially busy with another device.

The CC NEED CHANNEL (drawing CC) is true as previously described to request access to the data channel. The CC ACTIVE flip-flop, which signifies that the TM10 control has access to the data channel, is reset, since it is assumed that the data channel is busy with another device. The CHB CHANNEL START IN signal (drawing CHB) will be asserted and it asserts CHB CHANNEL START OUT. (Here we are assuming that the TM10B is between another device and the data channel.) Similarly, CHB CHANNEL BUSY IN is relayed as CHB CHANNEL BUSY OUT and CHB SA WRITE IN is relayed as CHB SA WRITE OUT.

The normal termination point of a data transfer is when the data channel fetches a 0 control word. It then terminates operation by removing the CHANNEL BUSY signal. The device that is busy recognizes the removal of CHANNEL BUSY as the key to stop operation and thus inhibits its CHANNEL START out. On the other hand, the device can terminate the operation for reasons such as parity errors, etc., by removing its CHANNEL START. The data channel responds by inhibiting CHANNEL BUSY. Regardless of which terminates, it requires the negation of both CHANNEL START IN and CHANNEL BUSY IN before the TM10B gains access to the data channel. When CHB CHANNEL BUSY IN, CC ACTIVE (0), and CHB CHANNEL START are true, the CC TERMINATE pulse is generated to set the CC INHIB (inhibit) flip-flop. Two hundred and fifty nanoseconds later CC TERMINATE DY clears the CC CHANNEL STARTED which in turn sets the CC ACTIVE flip-flop. Note that INHIB prevents ACTIVE from generating a CHANNEL START at this point. After another 250 ns, the CC RESET pulse is generated and resets the INHIB flip-flop. With CC INHIB reset and CC GRAB CHANNEL true, ACTIVE now generates a CHANNEL START which tells the data channel that the TM10B is ready to start operation, assuming no illegal status (ST ILLEGAL OP (0) true). CC GRAB CHANNEL is true due to CC CHN SYNC (1) being true. CHANNEL START also prevents any other device on the bus (closer to the data channel) from gaining access to the data channel in the same manner that the CHANNEL STARTED flip-flop inhibits the TM10B (note that CHB CHANNEL START OUT holds CC CHANNEL STARTED in the set state).

The data channel responds to CHANNEL START by asserting CHANNEL BUSY. The receipt of CHANNEL BUSY by the TM10B is the acknowledgement that it has access to the data channel. The TM10B receives CHANNEL BUSY IN (CHB CHN BUSY IN, drawing CHB) but does not relay it. The CHB CHN BUSY IN signal ANDed with CC ACTIVE generates CC CHN SEIZED.

The CC CHAN SEIZED generates the CC DATA TO CHN pulses which transfer the content of BR to the channel bus (drawings CHND 1 and 2). This transfer sends the initial address data contained in BR 27 - BR 34 to the data channel. CC CHAN SEIZED now generates CC MT START and CC OK TO GO. The CC OK TO GO signal (drawing CM2) now generates CM MT GO which sets the T GO flip-flop to start the operation as described in Sections 3.4 and 3.5. CM MT GO also generates the initial device pulse (CHB DEV PLS, drawing CHB) to inform the data channel that the tape control is ready to transfer data. Since the tape control has access to the data channel, the CM MT GO pulse clears CC CHN SYNC and CC WAIT DEL.

Operation now continues as explained in Section 3.6 with the inter-record delay, after which data is read from or recorded onto the tape. The subsequent data transfer between tape control and data channel is described in Section 3.13.

3.6 INTER-RECORD GAP DELAY

According to tape format, between each record there is an inter-record gap. Assuming that the tape is stopped, before reading or writing the tape must attain operating speed within the inter-record gap. To provide the inter-record gap, the tape control timing circuits incorporate a timing delay which is explained as follows: the T GO flip-flop (drawing T2) is set as previously described; the T GO signal performs the following functions.

a. Sets the T ACCEL (acceleration delay) flip-flop (drawing T1).

b. Generates the SET TAPE FCN pulse (drawing T2 which shuts the transport status off the bus and sends to the transport, the command direction, forward reverse, rewind, and write (drawing TB). The transport that receives the command sets the function into the tape transport register.

c. Generates the TB MOVE signal (drawing TB) to move the tape in the specified direction.

The T ACCEL flip-flop being set generates T ENABLE MUC (drawing T1) which enables the motion up-counter (MUC on drawing MT). For the write command the T ACCEL signal sets the BC DATA REQ flip-flop (drawing BC2) to obtain the first word to be recorded to the data buffer. T ENABLE MUC (drawing MT) now generates MT COUNT pulses at the 800 bpi clock frequency of the selected tape transport. The MUC bits are decoded so that the thirtieth MUC pulse sets the MT DLY SYNC flip-flop (MT DLY XFERRED will be 0 at this time). MT DLY SYNC synchronizes the motion transfer sequence to enable the motion-delay characteristics from the selected tape transport to appear on the read buffer lines. The binary number, representing motion delay duration represents the start-stop characteristics and operating speed of the attached tape transport. The next MT COUNT pulse generates the MT STROBE DELAY pulse which strobes the contents of the read buffer lines into the MT register, (drawing MT); the MT register is the timing register that provides the necessary acceleration or deceleration delay. MT STROBE DELAY then sets the MT DLY XFERRED flip-flop (indicating transfer complete) and clears the DLY SYNC flip-flop. The next MT COUNT pulse generates a DOWN COUNT pulse and begins to count down the MT register. The MT COUNT pulses continue producing DOWN COUNT pulses on every thirty-second MT COUNT pulse. Since the MT DLY XFERRED flip-flop is set thereafter, the thirtieth and thirty-first pulse will not reinitialize the MT register. When the MT register has counted down to a 1, the next DOWN COUNT pulse strobes the MT register to 0 and produces the MT IRD OVER (inter-record delay over) pulse. The IRD OVER pulse clears the T DEACCEL and T ACCEL flip-flops, thus ending the acceleration or deceleration delay. It should be noted that the delay sequence just described is used for deceleration of the tape following a tape spacing function as well as the acceleration of the tape before a tape spacing function.

The MT IRD OVER pulse, enabled by the T ACCEL signal, generates the T BEGIN OP pulse (drawing T1) which initiates the write and write end-of-file operations. If the rewind command is selected, the T BEGIN OP pulse clears the T GO flip-flop which frees the tape control for a new command to a different tape transport while the previously selected tape transport rewinds.

3.7 WRITE

The write operation is initiated by the T BEGIN OP pulse which sets the T SYNC WRITE flip-flop (drawing T1). The T CLOCK, which is the clock pulse for the selected density mode, clocks the write operation. The WD CLOCK DEL (drawing WD2), which is a delayed T CLOCK, is enabled to set WRITE ENABLE (drawing T1). The WRITE ENABLE signal then enables the T CLOCK pulses to generate T WP (write pulses, drawing T2). The WD CLOCK DEL pulses increment the character counter (BCC0-BCC2) in order to disassemble the 36-bit word in the data buffer into the appropriate 6-bit (7-track operation) or 8-bit (9-track operation) characters that are to be recorded. In the 7-track operation there are six characters per word. In 9-track operation, there are four characters per word. (In 9-track core dump operation, there are five characters per word.)

For 7-track operation, the character count circuits sequentially generate BC 1ST/7, BC 2ND/7, BC 3RD/7, ...BC 6TH/7 signals (drawing BC1) which sequentially disassemble the 36-bit data buffer word into 6-bit characters and apply them to the bus of the tape transport. In a similar manner, the 9-track decoding signals are formed. Drawing WD1 shows the decoding of the 36-bit buffer register word for both 7-track and 9-track operation.

The T WP pulse also produces T RECORD DATA pulses (drawing T2) which are sent to the tape transport to record the characters on the tape. For 9-track operation the write pulse (T WP) exclusive ORs the characters into the CRC register (drawing WD2) one character at a time. The CRC register then performs the necessary manipulation of the data to conform to 9-track format. The characters are also decoded in the write parity circuit (drawing WD2) and the parity bit pertaining to that character is sent to the tape transport to be recorded.

When a complete word has been written on tape, the BC ENB DATA REQ signal (drawing BC1) is generated. This signal enables the WD DEL pulse to generate BC WRITING SET DF (drawing BC1) which in turn sets the T DATA FLAG flip-flop (drawing T2) to request the next 36-bit word to be recorded. The next word to be recorded is transferred into the buffer register. The manner in which data transfers between core memory and buffer register occur is described in Section 3.13

Operation continues until the desired number of words are transferred as indicated by BC LAST WORD signal. (The BC LAST WORD signal generation is described in later paragraphs.) When the last character of the last word has been written, BC LAST WORD enables the generation of BC LAST COUNT and BC LAST BYTE. BC LAST BYTE enables the WD DEL to clear the WRITE ENABLE (drawing T1) flip-flop and T WP to set the WRITE EOR flip-flop. Since we are at the end-of-record, a 4-character space must be left on tape and the the LPCC character must be written. This is accomplished as follows.

The WRITE EOR (1) signal enables T CLOCK pulses to count up the EOR1 and EOR2 counter (drawing T1) to produce the required 4-character space signified by the 4 CHAR pulse. For the 7-track system, the 4 CHAR pulse generates the T WRITE LPCC pulse which is sent to the tape transport to write the longitudinal parity check character.

For a 9-track system, the CRC character is written following the first 4-character space. The EOR1 and EOR2 counter recycles for a second 4-character space count and then the LPCC is written.

Tape motion continues at full speed until the read circuits detect the end-of-record passing under the read head in the tape transport. When the read circuits detect the end-of-record, the T RECORD OVER pulse sets T DEACCEL to initiate the deceleration delay (refer to the READ discussion for generation of T RECORD OVER pulse). At the start of the deceleration delay, MT STROBE DELAY ANDed with T STOP sets the ST JOB DONE flip-flop (drawing ST). If the interrupt is enabled, JOB DONE flag generates a flag interrupt (drawing CM2) signifying that the record has been completed. Subsequently, at the end of the deceleration delay, the MT IRD OVER pulse is produced and clears T DEACCEL. The T STOP signal enables MT IRD OVER to generate CM CLR GO (drawing CM2) which clears the T GO flip-flop, terminates the MOVE signal, and stops the tape thus completing the write operation.

3.8 CONTINUED OPERATION

If the CM CONTINUE flip-flop (drawing CM2) is set when CM CLR GO occurs, then CM LEGAL TEST is generated to start operation again for the function specified. The CM CONTINUE flip-flop is set if the new function command does not require a change of tape direction and a different unit is not selected (-CM STOP TAPE is true). If a different tape unit has been selected for operation, then -T GO and CM WAITING set CM UNIT OK after a 1 μs delay to allow the transport bus to settle down.

For the TM10B, the data channel is released as soon as it fetches a 0 control word. The tape, of course, continues through the deceleration delay. If the program wishes to continue operation with the same unit, it issues the appropriately coded MTC CONO instruction. The MTC CONO SET pulse sets CC WAIT DEL. If the new function doesn't require a reversal of tape direction, then CC GRAB CHANNEL is generated to request access to the data channel for the ensuing function. In this manner, the data channel request is in process while waiting for the deceleration delay to terminate. Signals CM UNIT OK and TB TUR (tape unit ready) generate CM LEGAL TEST to start operation.

3.9 WRITE END-OF-FILE MARK

After the inter-record delay, the T BEGIN OP pulse sets the T SYNC EOF flip-flop (drawing T1) which synchronizes the tape operation to write the 17_8 EOF character on 7-channel tape or 023_8 on 9-channel tape. SYNC EOF enables the next T CLOCK pulse to set the WRITE EOR flip-flop. The transition of WRITE EOR, enabled by CM WR EOF, generates the T RECORD DATA pulse (drawing T2) which is sent to the tape transport to write the EOF character on tape. WRITE EOR then enables the 4-character sequence prior to LPCC character; WRITE EOR enables the T CLOCK pulses (drawing T1) to increment EOR1 and EOR2 to a 4-count and generate the T 4TH CHAR pulse. For a 7-track system, T 4TH CHAR generates T WRITE LPCC (drawing T1) which writes the LPCC character. For a 9-track system, the first T 4TH CHAR pulse writes a 0 CRC character; a second T 4TH CHAR pulse is generated to write the LPCC. Operation terminates when the read circuits detect missing data and begin the deceleration of the tape.

3.10 READ

After the initial programming sequence sets up for reading and the inter-record delay sequence is complete, operation begins when the read circuits in the tape transport detect data. For each character detected, the tape transport sends to the tape control a TB RD SKEW OVER pulse (drawing TB). TB RD SKEW OVER pulse produces the T READ STROBE (drawing T1); and ERF (0) enables the T RD STROBE to generate the T READ pulse. The character counter (BCC0-BCC2, drawing BC1) is 0 at this time; therefore, BC 1ST/7 signal enables the T READ pulse to strobe the 6-bit character from the tape transport into the BR0-BR6 bits of the buffer register (drawing BR1). The T READ pulse also increments the character counter. Parity is check by the T READ STROBE (drawing RD) by setting the RD LATERAL PAR ERR flip-flop when an error occurs. Note that T READY FOR DATA (drawing T1) enables the parity detection circuit only at the appropriate time. The READ STROBE also accumulates the LPCC character (drawing RD) by complementing the LPCC register for those bits that are 1. Operation continues in this manner until the buffer register is full. The character count now generates BC 6TH/7 (assuming 7-track operations) which initiates a data transfer from the buffer register to the processor (drawing BC1). The BC 6TH/7 signal, enabled by -BC LAST WORD, generates BC ENB DATA REQ which generates BC READING SET DF which in turn sets the DATA FLAG flip-flop (drawing T2) As explained later, the DATA FLAG enables the transfer of data to the processor.

Operation continues in this manner until the read circuits detect missing data, thus signifying end-of-record. It should be noted that if the processor specifies a record length less than the record length read, only the number of words specified by the processor are transferred t ;y. If the

length specified by the processor is greater than the record length read, the entire record, of course, is transferred into memory. In any case, the detection of end-of-record by read circuits is the determining factor for stopping operation. This is accomplished as follows.

The first T READ STROBE, which signifies that the first character has been read from tape is enabled by CM MOTION FWD and T DEACCEL (0) to set the DATA PRESENT flip-flop (drawing T1). DATA PRESENT then permits the T CLOCK pulse to toggle the EOR 3 flip-flop. As long as data is present, the T READ STROBE (B) clears EOR3 before EOR4 can be set. When data is missing, the READ STROBE does not occur and EOR4 gets set. The next T CLOCK pulse sets the SYNC REC OVER flip-flop which enables the WD CLOCK DEL to generate T RECORD OVER. T RECORD OVER sets T DEACCEL to initiate the deceleration delay and thus terminate operation. The LPCC register (drawing RD) should be 0 at JOB DONE time; if not, -RD LPCC = 0 (drawing ST) generates a ST PAR ERR (parity error).

3.11 READ/COMPARE

In the read/compare operation (CM RD/CMP, drawing CM1), a complete 36-bit word is read from tape and assembled into the buffer register. After the word is assembled, the data transfer is initiated to obtain the word from processor memory for comparison. The word from memory is exclusive ORed into the buffer register. Consequently, the data buffer should contain all 0s (BC BR = 0, drawing BC2); if not, the ST R/C ERROR (read/compare error, drawing ST) is set.

Operationally, the read/compare mode is similar to the read mode with the exceptions that follow. In the read/compare mode of operation, the data transfer cycle is initiated (via READING SET DF, drawing BC1) to obtain a word from memory to compare to the buffer register. During the word transfer, the CM WRITE OR RD/CMP signal permits the BC HR TO BR XOR pulses (drawing BC2) to exclusive OR the word from memory into the buffer register (drawing BR1 and BR2). (The discussion on Data Transfer explains more explicitly how the data transfer to the buffer register is accomplished.) The buffer register is then decoded to determine if it contains all 0s. The read/compare error prevents any data transfer cycles. The ST R/C ERROR signal generates T STOP CONDITION (drawing T2). T STOP CONDITION prevents (via BC LAST WORD, drawing BC1) any further data requests. Operation continues until the read circuits detect the end-of-record. At that time the program may examine read/compare status and if a read/compare error is found, the program can further examine its internal structure to determine the memory location that was in error.

3.12 DENSITY MODES

Three different tape densities are available: 800, 556, and 200 cpi (characters per inch). Bits CM DENS0 and DENS1 of the command circuits (drawing CM1) select the densities. The different recording densities are effected by changing the clock pulse frequency. For 800 cpi operation, the

800 bpi clock pulses from the tape transport are enabled by CM 800 to produce the T CLOCK pulse (drawing T1); for 556 cpi operation, the 556 bpi CLOCK pulses from the tape transport are enabled by CM 556 to produce T CLOCK pulses. For 200 cpi operation, the 800 bpi clock is counted-down by flip-flops TA and TB producing T ENABLE 200 every fourth count to enable the 800 bpi clock to produce T CLOCK pulses.

3.13 DATA TRANSFER

3.13.1 TM10A

There are two flip-flops, BC DATA SYNC and BC DATA REQ (drawing BC2), that control the data transfer operation. BC DATA REQ flip-flop requests data (during write or read/compare) from the processor and during read requests that the processor take the data that has been read from tape. When set, BC DATA REQ enables the data priority interrupt to the computer. Through the interrupt and sense circuits, the processor is made cognizant of the request.

During write BC DATA SYNC when set specifies that the HR (hold register) is loaded and ready to load the buffer register. It waits for T DATA FLAG (1) to specify that the buffer register is ready for the next data word. Similarly, during read, BC DATA SYNC specifies that the HR is ready to receive data from the buffer register.

During the write mode, the buffer register must be loaded and ready to go as soon as the inter-record delay is complete. To accomplish this, T ACCEL(1) (which occurs at the beginning of inter-record delay) generates BC WRITING SET DF (drawing BC1) and sets BC DATA REQ (drawing BC2). BC WRITING SET DF sets the T DATA FLAG flip-flop (drawing T2). Note that the T SET DF pulse, which sets T DATA FLAG, generates BC BR CLR (drawing BC1) to clear the buffer register. The BC DATA REQ signal enables the DATA priority interrupt channel (drawing CM2).

The processor responds (i.e., the executive program responds) to the interrupt by putting the 36-bit word onto the I/O bus and generating the MTC DATAO instruction. The MTC DATAO CLR pulse clears the HR (drawing HR) and the MTC DATAO SET pulse strobes the data into the HR. The MTC DATAO CLR pulse also clears BC DATA REQ. The MTC DATAO SET pulse also sets BC DATA SYNC. With T DATA FLAG (1) true, the BC BUFFERS READY signal is generated and clears BC DATA SYNC. It further generates BC HR TO BR XOR which, in turn, generates CHND 00 through CHND 35 (drawing CHND 3). The CHND pulse then exclusive-OR the HR into the buffer register (drawing BR1). For write mode, the buffer register was previously cleared, therefore, the exclusive-OR function transfers the content of HR into BR. However, for the read/compare operation, the buffer register contains the

assembled 36-bit word when the exclusive -OR function occurs, thus effecting the read/compare function. Subsequently, BC BUF RDY DEL is generated which sets BC DATA REQ. The data interrupt is again generated to load the HR.

The buffer register is now loaded (assuming with mode) and subsequently the HR will be loaded from the processor. As soon as the inter-record delay is complete, writing begins. After the first 36-bit word has been written, the T DATA FLAG flip-flop is set which, as explained above, transfers the content of the HR into the BR and subsequently (via BC BUF RDY DEL) sets the BC DATA REQ flip-flop. Operation continues in this manner until the desired number of words have been written as determined by the executive program. When this occurs, the executive program issues an MTS CONO instruction with bit 35 set. This clears the BC DATA XFER ACT (data transfer active) flip-flop which was initially set by the CM MT GO pulse (drawing BC1). During a write operation, BC LAST WORD is not asserted until BC DATA SYNC is cleared because, until this is so, the HR contains another data word to be written on the tape that has not yet been transferred to the BR. The BC LAST WORD signal is generated and, as explained for the write operation, as soon as the last character of the buffer register has been recorded, BC LAST BYTE prepares the circuits to write the LPCC. Since BC DATA XFER ACT is no longer set, BC BUF RDY DEL can no longer set the BC DATA REQ flip-flop. The T DEACCEL (1) and BC LAST WORD (drawing T1) generate T STOP. The ensuing MT STROBE DELAY pulse is enabled by T STOP to set the JOB DONE flip-flop (drawing ST).

For the read operation, the BC DATA SYNC is initially set by CM READ and T ACCEL. When the first word read from the tape has been assembled in the BR, the T DATA FLAG flip-flop is set. Thus, BC BUFFERS READY clears DATA SYNC and generates BC LOAD HR which transfers the BR content into HR. Subsequently, BC BUF RDY DEL sets BC DATA REQ to generate the data interrupt. The executive program responds to the interrupt by executing a MTC DATAI to obtain the word from the HR. MTC DATAI also resets BC DATA REQ and sets BC DATA SYNC.

When the required number of words have been read, the executive program issues a MTS CONO instruction with bit 35 set which clears BC DATA XFR ACT (drawing BC1) BC LAST WORD is generated which in turn generates BC LAST BYTE. BC LAST WORD ANDed with T DEACCEL (drawing T 1) generates T STOP which set the ST JOB DONE flip-flop (drawing S1). JOB DONE now generates a flag interrupt to inform the executive program of the JOB DONE status.

3.13.2 TM10B

The data transfer between the TM10B Magnetic Control Unit and PDP-10 memory is accomplished by the DF10 Data Channel. Previous paragraphs described the initial operation of data channel whereby the TM10B control requested and received access to the data channel.

After the TM10B has gained access to the data channel (when CC CHN SEIZED becomes true), the T GO flip-flop is set by CM MT GO. The CM MT GO pulse also generates the initial device pulse (CHB DEV PLS, drawing CHB) to tell the data channel that it is ready to start operation. If it is a write operation, as signified by CHB SA WRITE being asserted, the data channel responds by putting the 36-bit word onto the channel bus and generating the CHB CHN PLS (channel pulse). The data channel also responds with the data pulses (a pulse is a 1; no pulse is a 0) that come in on the data channel bus (drawing CHND1 and CHND2). The CC DATA FROM CHAN signal enables these input pulses to generate the CHND 00 - CHND 35 pulses. These pulses strobe data into the BR (buffer register, drawings BR1 and BR2). The HR00 (1) - HR35 (1) signals are at ground. They are grounded through pins C, E, and R of the W990 modules which are inserted in place of the S205 modules (used only for TM10A) as shown on drawing HR. The BR was initially cleared by BC BR CLR. The BC BR CLR pulse (drawing BC1) was generated from T SET DF (drawing T2) which was generated from BC WRITING SET DF (drawing BC1).

Simultaneous with the loading of BR the CHB CHN PLS sets the BC DATA SYNC flip-flop (drawing BC2). The CHB CHN PLS (still assuming a write operation) also generates the CC COMPLETION pulse (drawing CC) which strobes the 1 μs one-shot to generate BC XFER DONE. The BC XFER DONE signal resets the T DATA FLAG flip-flop (drawing T2).

The magnetic tape control now operates as previously described to write the 36-bits from BR onto tape. When all 36-bits have been written, the T DATA FLAG flip-flop is set by WRITING SET DF. The T DATA FLG (1) signal is ANDed (drawing BC2) with BC DATA SYNC to generate BC READY and after the 1 μs delay, the BC BUFFERS READY pulse. The BC BUFFERS READY pulse resets BC DATA SYNC and generates the CHB DEV PLS for the data channel. Again the data channel responds by loading the BR and generating the CHB CHN PULSE. Subsequently, the T DATA FLAG flip-flop is cleared by BC XFER DONE.

The write operation continues until the data channel fetches a 0 control word. When this occurs, the data channel terminates the CHB CHN BUSY signal which then generates the CC CHAN END (drawing CC). The CC TERMINATE pulse sets the INHIB flip-flop to prevent the CHANNEL START signal from being generated or relayed from another device. After a delay, CC RESET resets the INHIB flip-flop to permit normal data channel operation.

The CC CHAN END pulse also resets CC ACTIVE (drawing CC). The CC CHN SEIZED signal goes false. CC MT START now goes false and generates T STOP CONDITION (drawing T2). T STOP CONDITION (drawing BC1) generates BC LAST WORD which in turn generates BC LAST BYTE. BC LAST BYTE resets WRITE ENABLE and sets WRITE EOR (drawing T1). Operation continues in the manner previously described to write EOR mark and terminate the write operation when end-of-record is detected by read circuits.

It should be noted that the channel is released as soon as it fetches a 0 control word. How-However, tape operation continues through the decleration delay. If program control desires to continue operation with the same unit, it issues an MTC CONO instruction appropriately coded for the next function. This MTC CONO instruction sets CC WAIT DEL (drawing CC). If the new function doesn't require a reversal of tape direction, then CC GRAB CHANNEL is generated to request access to the data channel for the ensuing function. In this manner, the request for data channel access is in process while tape control waits for the deceleration delay to terminate.

The data transfer of the read operation using the data channel, starts (assuming data channel seized) when the first 36-bit word has been assembled in the BR. The READING SET DF signal (drawing BC1) sets the T DATA FLAG flip-flop (drawing T2). BC DATA SYNC (which was set by the initial CHB CHN PLS) enables T DATA FLAG to generate BC BUFFERS READY (drawing BC2) which generates the CHB CHN DEV PLS. The data from the BR is applied to the data channel bus (drawing CHND 1 and 2). The BC BUFFERS READY pulse generates the CC DATA TO CHN pulses. These pulses strobe the BR data onto the data channel bus. The data pulses on the channel bus trigger corresponding GND00 - 35 pulses which complement those BR flip-flops which contain 1s thus clearing the BR.

The BC BUFFERS READY pulse also generates CC COMPLETION (drawing CC) which after a delay (drawing BC2) generates BC XFER DONE. BC XFER DONE clears the T DATA FLAG flip-flop. The read operation continues in this manner until the data channel fetches a 0 control word. When it does, the CHB CHN BUSY signal goes false to terminate operation as described previously.

3.14 ERRORS

3.14.1 Data Late Errors

The data late error indicates that an extraneous word was either written or read from tape before the data transfer facility could supply another word for write, or store the present data buffer word for read. The ST DATA LATE flip-flop (drawing ST) is set when T DATA FLAG is still set (indicating that the data transfer to or from the BR has not occured) when the BC COUNT or T STROBE CRC pulse occurs.

3.14.2 Parity Error

As discussed during write and read operation, the parity error is the result of either a longitudinal or lateral parity error.

3.14.3 Read/Compare Error

The read/compare error was discussed in the read/compare discussion.

3.14.4 Record Length Incorrect

During read or read/compare operation, this error signifies that the record-length specified differs from the record-length read from tape. The ST REC LEN INC flip-flop (drawing ST) is set for a long record by the READ STROBE (enabled by BC LAST WORD and T ERF which indicates end-of-record) and by the ~~RECORD OVER~~ T STOP COND A pulse (enabled when the -BC LAST WORD and CM FCN ϕ (ϕ) which specifies more data) for a short record.

3.14.5 Bad Tape Error

This error indicates that data was in the inter-record gap. The BAD TAPE flip-flop (drawing ST) is set by the T READ STROBE (indicating data present) which is enabled by T DEACCEL and T INTO RECORD.

3.15 ILLEGAL COMMANDS

The ST ILLEGAL OP flip-flop (drawing ST) is set by the CM MT GO pulse when one of the following events occur.

a. 9-track operation specified and density not set to 800 bpi.

b. Write or write EOF operation specified and the write-lockout bit (WL) from the tape transport is set.

c. Beginning-of-tape status and a reverse motion specified.

d. ~~EOT (end of tape) sensed and a WRITE command specified.~~

3.16 SPACE

There are two commands for spacing records: space forward and space reverse. The initial operation (for either TM10A or TM10B) of space forward or space reverse is accomplished in a similar manner to read or write. The program initiates operation by loading the command register with the space command. Operation is initiated and a record is read. The read strobe is monitored for end-of-record. While spacing over a record, no data is transferred; however, the BC DATA REQ flip-flop is set at the beginning of every record by CM SP RECORD and T ACCEL (B).

Note that CM SP RECORD is the result of CM SPACING ANDed with CM FCN (0) 0 which specifies spacing only one record. Therefore BC DATA REQ is set only for CM SP RECORD and not for SPACING RECORD.

End-of-record detection, as in normal operation, produces the T RECORD OVER pulse which initiates the deceleration delay. However, in a spacing operation it also initiates a data channel transfer, by setting T DATA FLAG (drawing T2). The T DATA FLAG initiates a transfer in a manner as explained previously for the TM10A or TM10B. The purpose of the transfer is to determine whether to stop or to space over another record. If the controlling device (data channel for TM10B, executive program for TM10A) responds (with a CHB CHN PULSE or DATAO MTC respectively) and does not terminate the operation, an additional record is spaced.

After spacing over the required number of records, the TM10A or TM10B terminates operation in a manner as previously described.

The detection of end-of-record in the space reverse mode is different from that for a forward motion, since the LPCC is always the first character detected. This is accomplished by the INTO RECORD flip-flop (drawing T2). The READ STROBE, which occurs as the result of the LPCC character, sets the INTO RECORD flip-flop. Note that DATA PRESENT will not be set by this READ STROBE. The next READ STROBE occurs when the last character of the record (the first in reverse motion) moves under the read head; this READ STROBE sets the DATA PRESENT flip-flop. When no more READ STROBES occur, EOR 3 (drawing T1) remains set and the next CLOCK pulse sets EOR 4; the following CLOCK pulse generates RECORD OVER, which initiates the deceleration delay.

3.17 SPACE TO END-OF-FILE

In this mode, the space forward or space reverse mode is specified and the tape spaces forward or reverse as described in Section 3.16. The difference, however, is that the tape continues spacing over records until the end-of-file, beginning-of-tape and space reverse, or end-of-tape and space forward occur. The logic implementation of this feature is as follows.

This mode is specified by CM FCN (0) bit a 1. Therefore, CM SPACING does not generate CM SP RECORD which would otherwise generate BC DATA REQ at the start of a record. Since BC DATA REQ is not set, the T STOP CONDITION (drawing T2) is not generated by CM SPACING and BC DATA REQ (1). Instead, T STOP CONDITION waits for CM SP REV ∧ TB BOT, T ERF ∧ ST EOF (end-of-file), or CM SP FWD ∧ TB EOT.

3.18 READ OR READ/COMPARE ACROSS RECORD BOUNDARIES

This operation is similar to read or read/compare except that tape continues after a record is read. This mode is specified by the read or read/compare command with CM FCN0 set to 1. In read or read/compare operation with CM FCN0 set to 0, if operation is not terminated by a CONO MTS, 1 then it is terminated by gate A24-H on drawing T2. This gate generates T STOP CONDITION at the

end-of-record (T ERF (1)) when CM FCN0 is 0. With CM FCN0 at 1, read or read/compare operation continues until end-of-record with T DATA FLAG set or the end-of-record and the record read does not contain a multiple of six characters for 7 channel operation (i.e., ~BCC = 0 is true). These conditions generate T STOP CONDITION. Also, any other error will stop operation at the end-of-record. Of course, a CONO MTS, 1 will stop operation.

3.19 READ-IN MODE

The read-in mode permits a completely assembled program to be loaded from an I/O device without a resident memory loader program. When the tape control is selected for read-in mode, tape unit 0 is automatically selected and the tape is rewound to beginning-of-tape on that unit. The read mode is then automatically selected to read one record into memory. This record should contain information specifying further loading procedures.

The read-in mode is initiated by the operation at the PDP-10 control panel. The control panel controls permit selection of an I/Odevice for the read-in mode. When the tape control is selected, the IOBC MTC SEL signal is enabled by the control panel selection and the IOBC RDI PULSE sets the CM RD IN flip-flop (drawing CM2). The CM RD IN signal ANDed with ST JOB DONE (0) sets the rewind code into the command function register (drawing CM1). The CM RD IN signal also sets the CM WAITING flip-flop to start operation. CM WAITING sets CM UNIT OK which in turn generates CM LEGAL TEST (assuming TB TUR is 1) and subsequently CM MT GO sets the T GO flip-flop. Subsequently, MT IRD OVER generates T BEGIN OP which resets T GO and ST JOB DONE. During this time, the T SET TAPE FCN signal has transferred the rewind command to unit 0.

With ST JOB DONE coming on and CM RD IN still set, the read command is strobed into the CM FCN register, and core dump, 556 bpi density, and odd parity are set into their respective flip-flops (drawing CM2). CM RD IN sets the CM UNIT OK flip-flop again. When the tape has rewound, the TB TUR level comes on and generates CM LEGAL TEST and subsequently CM MT GO. CM MT GO starts the read operation which is the same as described previously except that the ST JOB DONE status remains on.

CHAPTER 4
MAINTENANCE

Maintenance procedures are classified into two major categories; preventive maintenance and corrective maintenance. Preventive maintenance procedures are repeated periodically to ensure that system performance is not degrading. Corrective maintenance procedures are performed in the event of equipment malfunctions. For a list of suggested maintenance equipment refer to the PDP-10 Maintenance Manual.

4.1 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the TM10 and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks forestalls possible future failure by correcting minor damange and discovering progressive deterioration at an early stage. A log book used to record data found during the performance of each preventive maintenance task will indicate the rate of circuit operation deterioration and provide information to determine when components should be replaced to prevent failure of the equipment. These tasks consist of mechanical checks, which include cleaning and visual inspections; checks of specific elements such as the power supplies, and marginal checks which aggravate borderline conditions or intermittent failure so that they can be detected and corrected. All preventive maintenance tasks should be performed as a function of conditions at the installation site and the downtime limitations of equipment use. Perform the mechanical checks at least once each month or as often as required to allow efficient functioning of the air filters. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. For a typical application, a schedule of every four months or 700 equipment operating hours, whichever occurs first, is suggested.

4.1.1 Mechanical Checks

Assure good mechanical operation of the equipment by performing the following steps and the indicated corrective action for any substandard conditions found:

a. Clean the exterior and the interior of the equipment cabinet by using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

b. Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and housing, which are held in place by two knurled and slotted captive screws. Wash the filters in soapy water, dry in an oven or by spraying with compressed gas, and spray with Filter-Kote (Research Products Corporation, Madison, Wisconsin) before replacing them in the cabinets.

c. Lubricate door hinges and casters with a light machine oil. Wipe off excessive oil.

d. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC enamel.

e. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.

f. Inspect all mounting panels of logic to assure that each module is securely seated in its connector.

g. Verify that all bus cables are firmly seated in their respective connectors.

h. Inspect power supply capacitors for leaks, bulges, or discolorations. Replace any capacitors giving these signs of malfunction.

4.1.2 Weekly Checks

The transport timing should be checked weekly with the transport timing test (MAINDEC-10-04GA-D).

4.1.3 Monthly Checks

Check the power supply output. It should fall within the ranges listed below. Measure the output ripple with an oscilloscope; if it is greater than the limit given, the power supply at fault may be considered defective.

Nominal Output	Acceptable Range	Maximum Peak-to-Peak Output Ripple	
		60 Hz	50 Hz
+10V	+ 9.5 to 11.5V	.7V	.9V
-15V	-14.5 to 16.5V	.5V	.6V

Run the reliability test (MAINDEC-10-04HA-D) and margin all racks except L to these limits.

+10V	+2 to + 20V
-15V	-12 to -18V (Do not exceed these limits)
Panel L	+6 to +18V, -15V: -12 to -18V

Individual rack margin limits can be found in the TM10A Acceptance Test Specifications.

NOTE

To insure reliable operation of the tape transport unit, the maintenance procedures outlined in the tape transport manual should be performed as specified.

4.2 CORRECTIVE MAINTENANCE

Corrective maintenance is any maintenance procedure performed to correct a malfunction within the TM10 Magnetic Tape Control. The best tool for corrective maintenance is a sound knowledge of TM10 operation. Test equipment suggested is a broadband oscilloscope and a standard multimeter. A suggested approach for localizing any fault and method for correcting it is as follows.

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the drum system.

b. System troubleshooting to locate the fault to within a module through the use of signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of a malfunction.

e. Validation test to assure that the fault has been corrected.

f. Log entry to record pertinent data.

4.2.1 Preliminary Investigation

Before proceeding into any detailed troubleshooting procedure, check that cables and modules are secured, test jumpers are removed, and switches are placed in their correct position. The programmer should check the program on which the malfunction occurred.

4.2.2 System Troubleshooting

Do not attempt to troubleshoot the tape control unit without first gathering all information possible concerning the fault, as outlined under Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings, and note all indicator light operations before and at the time of the error. Careful checks should be made to assure that the system is actually at fault before continuing with corrective maintenance procedures. Loose or faulty cable connections can often give indications very similar to those caused by internal malfunctions. Faulty ground connections between pieces of equipment are a common source of trouble.

If the fault has been determined to lie within the tape control unit, but cannot be localized to a specific logic function, perform the diagnostic program procedure (Table 4-1). When the location of the fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation tests should be employed to locate the source of the fault.

Table 4-1
Diagnostic Programs

Program No.	Description	Equipment
MAINDEC-10-04AA	Static Test	TM10A
MAINDEC-10-04BA	Dynamic Test P1	TM10A
MAINDEC-10-04CA	Dynamic Test P2	TM10A
MAINDEC-10-04DA	Static Test	TM10B
MAINDEC-10-04EA	Dynamic Test P1	TM10B
MAINDEC-10-04FA	Dynamic Test P2	TM10B
MAINDEC-10-04GA	Transport Timing Tests	TM10A and TM10B
MAINDEC-10-04HA	Reliability Tests	TM10A and TM10B

4.2.3 Signal Tracing

If the fault has been located within a functional logic element, program the PDP-10 to repeat some instruction in which all functions of that logic element are utilized. If this test is to be performed without the use of the computer, control flip-flops or register flip-flops can be cleared or set manually by momentarily supplying a ground potential to the appropriate flip-flop output terminals. Counting operations of registers can be checked by supplying count pulses to the register from the output of a variable clock. Under these conditions, use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep may be synchronized with any control signal by connecting the trigger input to the appropriate module terminal on the wiring side (front) of the equipment. Trace output signals from the connector back to the origin, and trace input signals from the connector to its final destination. The signal-tracing method can be used to determine with absolute certainty the quality of pulse amplitude, duration, rise time, and the correct timing sequence of this signal. If an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

4.2.4 Intermittent Failures

Intermittent failures caused by poor wiring connections can often be revealed by vibrating the modules while running a repetitive routine, such as the diagnostic program. Often, wiping the handle of a screwdriver across the back of a suspect row of modules is a useful technique. By repeatedly starting the program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules

in the connector, the module connector for wear and misalignment, and the module wiring for cold solder joints or wiring kinks.

4.2.5 Module Circuits

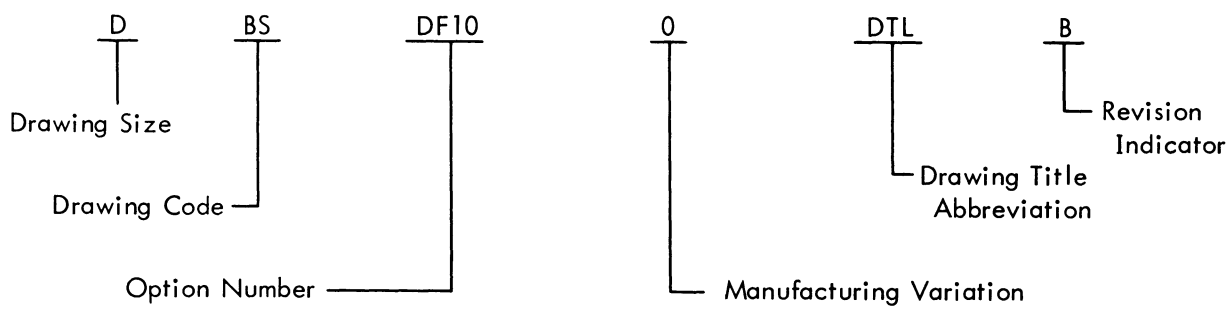
Circuit schematics of each module are supplied in either the Logic Handbook, C-105 or the PDP-10 Special Circuits Handbook, and should be referred to for detailed circuit information. The basic functions and specifications for standard modules are presented in the Digital Logic Handbook (C-105).

CHAPTER 5
ENGINEERING DRAWINGS

The engineering drawings for the TM10 Magnetic Tape Control Unit are contained in Volume III of the PDP-10 Peripheral Device Engineering Drawing Set and are supplied in addition to a complete set of drawings with each system. Should any discrepancy exist between the drawings in Volume III and those supplied with the equipment, assume the latter drawings are correct.

5.1 DRAWING TERMINOLOGY

The engineering drawing number for the TM10 contain six fields of information, separated by hyphens. A typical example of a drawing number is shown below.



The drawing size, option number, and the drawing title abbreviation are self-explanatory. The manufacturing variation letter identifies the variation that the drawings reflect. For example: 0 reflects drawing applicable to all variations; A reflects the 60 Hz equipment; etc. The drawing code identifies the type of drawing. A list of the common drawing codes follows.

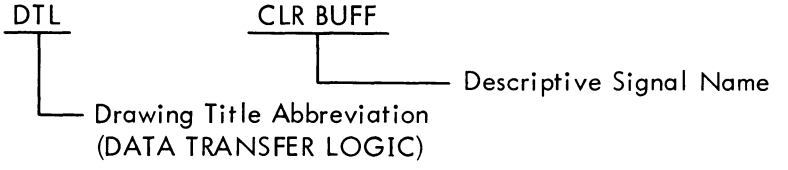
1. BS - Block Schematic or Logic Diagram
2. CL - Cable List
3. CS - Circuit Schematic
4. FD - Flow Diagram
5. IC - Interconnection Drawing
6. KS - Key Sheet
7. MU - Module Utilization
8. RS - Replacement Schematic

9. SD - System Diagram

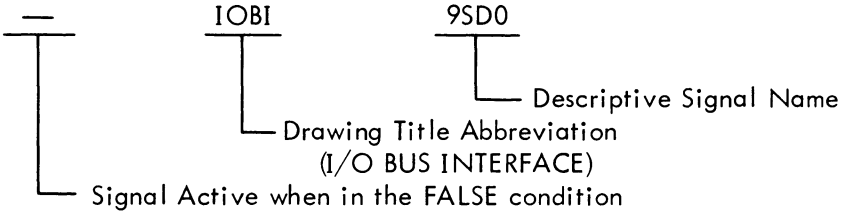
10. PL - Parts List

Signal names on the drawings cross reference the signal to the drawing where the signal originates. Two typical examples of signal names are shown below.

Example 1:



Example 2:



5.2 LOGIC SYMBOLS

The DEC standard logic symbols are shown at the input of most circuits to specify enabling condition required to produce a desired output. These symbols represent either standard DEC logic levels or standard DEC pulses.

Typical engineering symbols are shown in Figure 5-1.

5.3 LOGIC LEVELS

All logic signals are either standard DEC logic levels or standard DEC pulses. A standard DEC logic level is either a ground (0 to -0.5V or -3V (-2.5 to -4.0V). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (——◇) indicates that the signal is a level and that ground presents assertion; a solid diamond (——◆) indicates that the signal is a level and that -3V represents assertion.

All logic levels applied to the conditioning-level inputs of capacitor-diode gates must be present either 100 or 400 ns (depending upon the module used) before an input triggering pulse is applied to the gate.

The standard DEC negative pulse is indicated by a solid triangle (——▶) and goes

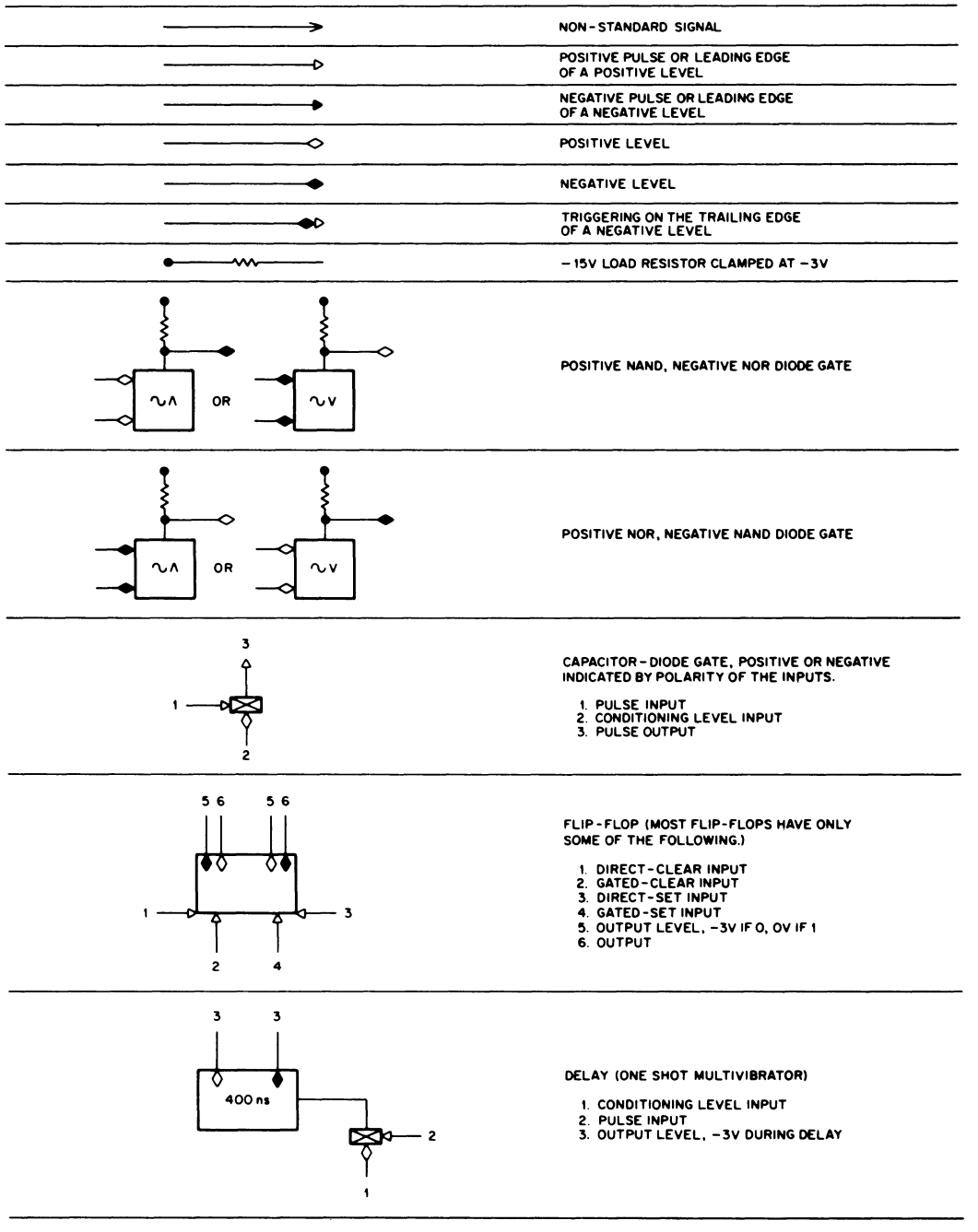


Figure 5-1 DEC Standard Logic Symbols

from ground (0 to -0.5) to -3V (-2.5 to -4.0V). The standard DEC positive pulse, indicated by an open triangle (——▷), goes from -3V to ground. The width of the standard pulses used in this equipment is either 100 or 400 ns, depending upon the module and application.

Occasionally, the trailing edge transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (——◆▷) is drawn to indicate this fact. The triangle is drawn solid if the negative (ground to -3V) transition triggers circuit action. The shading of the diamond is opposite that of the triangle to indicate triggering on the trailing edge.

Any other signal is nonstandard and is indicated by an arrowhead(——→) pointing in the direction of signal flow.

5.4 FLIP-CHIP PULSES

FLIP-CHIP circuit operation in the DF10 uses the DEC R-, S-, and B-series pulses. The pulse produced by the R-series or S-series modules start at -3V, goes to ground (-0.2V) for 100 or 400 ns, then returns to -3V. The rise time of the leading edge from 10% to 90% should be less than 60 ns. An idealized pulse is shown in Figure 5-2.

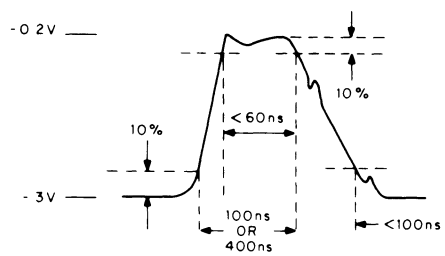


Figure 5-2 R-Series and S-Series Pulses

The B-series pulse starts at 0V, goes to -3V and returns to 0V. The pulse width must be between 30 and 40 ns at the -1V level and greater than 15 ns at the -2V level. Glitches on the bottom of the pulse should not be more positive than -2.5V, overshot should not exceed +4.0V, and no ring should be below -0.5V. The B-series pulse is idealized in Figure 5-3.

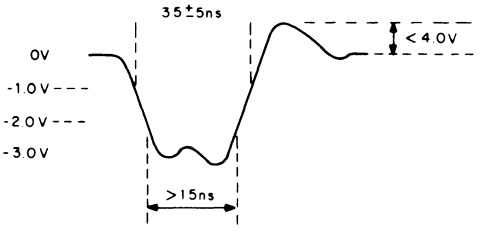


Figure 5-3 B-Series Pulse

5.5 ENGINEERING DRAWING LIST

The engineering drawings that are supplied with the TM10 will be found in Volume III of the PDP-10 Peripheral Engineering Set.

Drawing No.	Title
D-UA-TM10A-0-0	Mag Tape Control TM10A
A-PL-TM10A-0-0	Mag Tape Control TM10A
D-BS-TM10-0-BC1	Buffer Control
D-BS-TM10-0-BC2	Buffer Control
D-BS-TM10-0-BR1	Buffer Register
D-BS-TM10-0-BR2	Buffer Register
D-BS-TM10-0-CC	Channel Control for Channel Interface
D-BS-TM10-0-CHB	Channel Bus Logic Signals
D-BS-TM10-0-CHND 1	Channel Data Interface
D-BS-TM10-0-CHND 2	Channel Data Interface
D-BS-TM10-0-CHND 3	Channel Data
D-BS-TM10-0-CM1	Command
D-BS-TM10-0-CM2	Command
D-BS-TM10-0-HR	Hold Register
D-BS-TM10-0-IND	Indicator Connectors
D-BS-TM10-0-IOB	I/O Bus Data Interface
D-BS-TM10-0-IOBC	I/O Bus Control
D-BS-TM10-0-MT	Motion Timing
D-BS-TM10-0-RD	Read Data
D-BS-TM10-0-ST	Status Bits
D-BS-TM10-0-T1	Timing

Drawing No.	Title
D-BS-TM10-0-T2	Timing
D-BS-TM10-0-TB	Transport Bus
D-BS-TM10-0-WD1	Write Data
D-BS-TM10-0-WD2	Write Data
D-CP-TM10-0-TERM	Terminators
D-MU-TM10-0-MU	Module Utilization
D-MU-TM10A-0-MU	TM10A Module Utilization
A-PL-TM10-0-MU	Module Count
A-CP-TM10-0-COMP	External Component List
D-DI-TM10-0-1	Drawing Index List
D-AD-7005642-0-0	Wired Assembly
A-PL-7005642-0-0	Wired Assembly
D-IC-TM10-0-2	Wire, Power AC and DC