Digital Equipment Corporation
Maynard, Massachusetts

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PDP-10
Maintenance Manual

RP10 DISK PACK SYNCHRONIZER

Volume 1

DEC-10-H5EC-D (1)

PDP-10
RP10 DISK PACK SYNCHRONIZER MAINTENANCE MANUAL VOLUME 1

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Edition November 1969
2nd Printing May 1970
2nd Edition November 1970
3rd Edition August 1971

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ILLUSTRATIONS

*** Denotes figures revised since the November 1970 printing.**

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TABLES

***Denotes figures revised since the November 1970 printing.**
****Denotes figures added since the November 1970 printing.**

Chapter 1
General Information

1.1 INTRODUCTION

The RP10 Disk Pack Synchronizer, shown in Figure 1-1, provides the interface logic between the DF10 Data Channel and as many as eight of the DEC Type RP01 or RP02 Disk Pack Drives. The RP10 operates under control of the PDP-10 I/O Bus and, in turn, controls the RP01 or RP02 (see Figure 1-2). These units provide the PDP-10 computer with on-line auxiliary storage for between 1.28 and 40 million 36-bit words. Direct access to core memory is obtained through the DF10 Data Channel.

The RP10 is housed in a 19-in. cabinet containing eight module racks. Indicator and switch panels are located on the top front of the unit. These comprise monitoring and switch register facilities for data, address, and control. The unit contains the standard margin check voltage bracket, +10 and -15 Vdc power supplies and power control, and built-in cooling fans.

The RP10 is shipped complete and factory tested including all interconnecting cabling to the PDP-10 and the RP01/02 Disk Packs. Two types are available: the RP10-A for 60-Hz operation, and the RP10-B for 50-Hz operation.

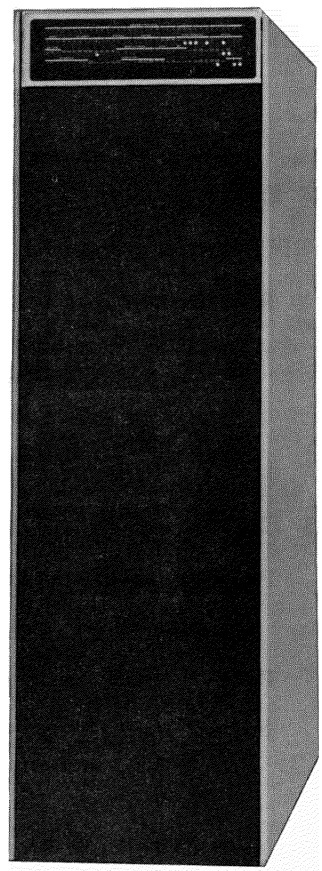


Figure 1-1 DEC Type RP10 Disk Pack Synchronizer

1.2 SPECIFICATIONS

Physical, environmental, electrical, and performance specifications for the RP10 Disk Pack Synchronizer are given in the paragraphs that follow.

1.2.1 Physical

Dimensions

Width = 21 in.
Height = 69 in.
Depth = 27 in.
Weight = 390 lb

Service Access Dimensions

Front = 36 in.
Rear = 36 in.

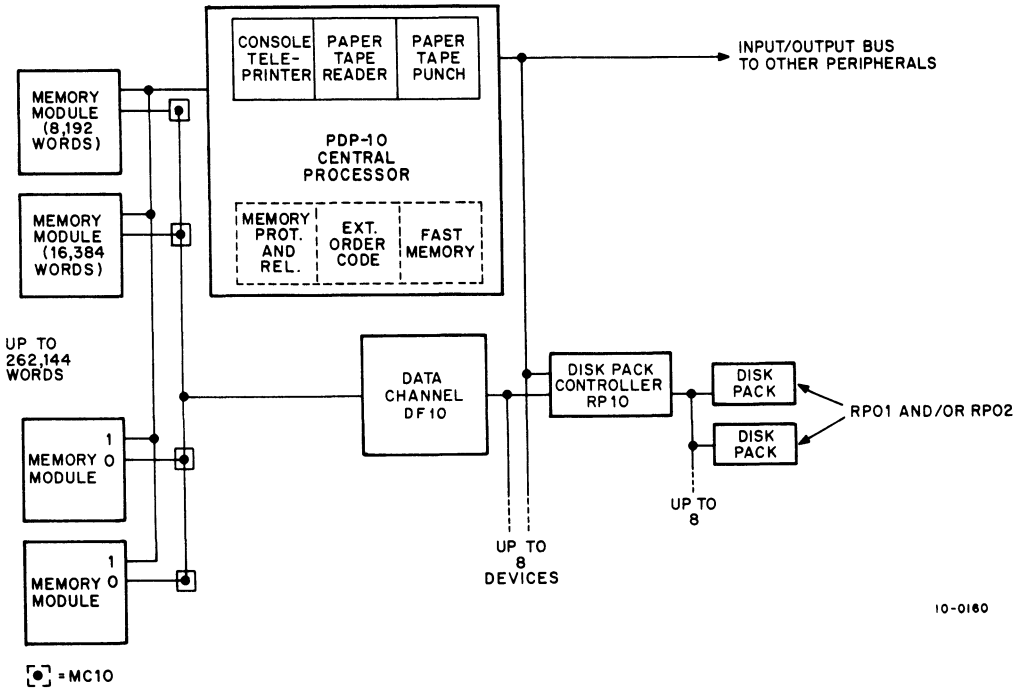


Figure 1-2 Typical PDP-10 System with
RP10 Disk Pack Synchronizer

1.2.2 Environmental

The RP10 operates under normal conditions of humidity, shock, and vibration.

Recommended Ambient

Operating Temperature = 60° to 95°F
Storage Temperature = 40° to 110°F
Humidity = 20% to 80% Relative
Wet Bulb = 78°F (Max)

1.2.3 Electrical

Power Requirement at Line Cord

115 Vac, 1-phase, 60 Hz @ 8.0A

Power/Heat Dissipation = 9000W/3000 Btu/Hr

Internal Power - From 4 self-contained Type 728 Power Supplies and one self-contained Type 844 Power Control.

+10 Vdc
-15 Vdc

Unit Cable Lengths

50 ft (Max)

1.2.4 Performance

Word Transfer Time

When synchronizing RP01 = 30 μs
When synchronizing RP02 = 15 μs

Positioning Time

Track-to-track = 20 ms
Average = 50 ms
Maximum = 80 ms

Latency Time

Average = 12.5 ms
Maximum = 25 ms

1.3 INTERFACE REQUIREMENTS

The RP10 Synchronizer is designed to interface with any of the RP01/02 Disk Pack options listed in Table 1-1. Figure 1-3 is the Interface Block Diagram for the system. A complete description of the RP01/02 is contained in the vendor manuals for the Disk Drives. These manuals are supplied with each piece of peripheral equipment.

Table 1-1
RP01/02 Features Compatible with RP10
Logic Configuration

Feature	Variations
Input Voltage and Frequency	208/230 Vac $\pm$10%, 60 Hz $\pm$1/2 Hz 220/380 Vac $\pm$10%, 50 Hz $\pm$2 Hz
NOTE **All drives in a given system must be driven by the same voltage and the same frequency.**	
Recording Density (bit cell time)	RP01 = 800 ns RP02 = 400 ns
Number of Drives	RP01 = 1 - 8 RP02 = 1 - 8
NOTE **May be intermixed.**	

1.3.1 RP10/RP01/02 Interface

There are two cable assemblies through which the RP10 connects to the RP01 or RP02 Disk Pack (see Figures 1-4 and 1-5); these assemblies and their functions are listed in Table 1-2. The electrical specification of the RP10/RP01/02 interface is shown in Figure 1-4.

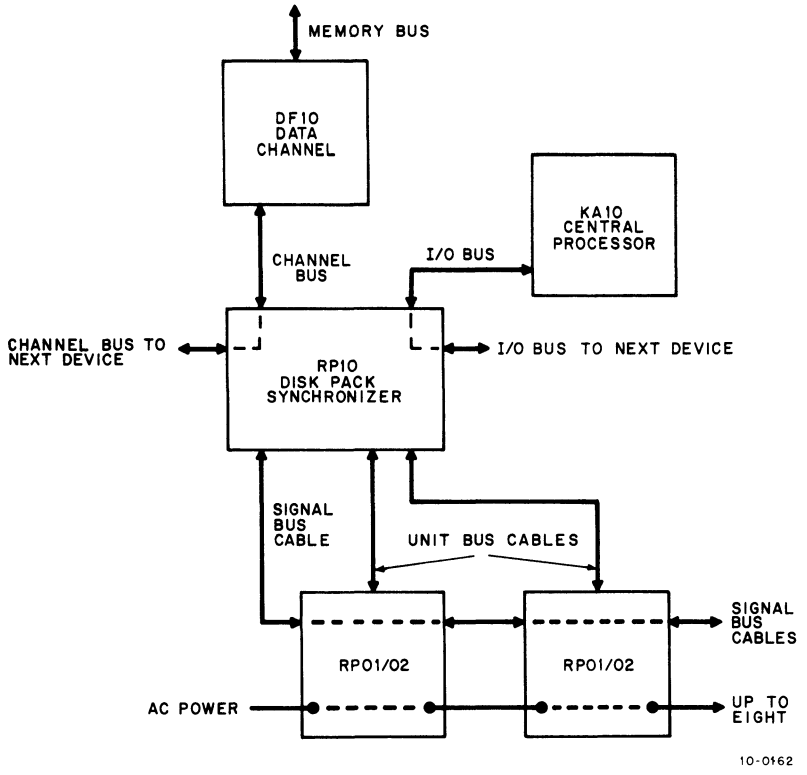


Figure 1-3 RP10/DF10/RP01/RP02/I/O Interface

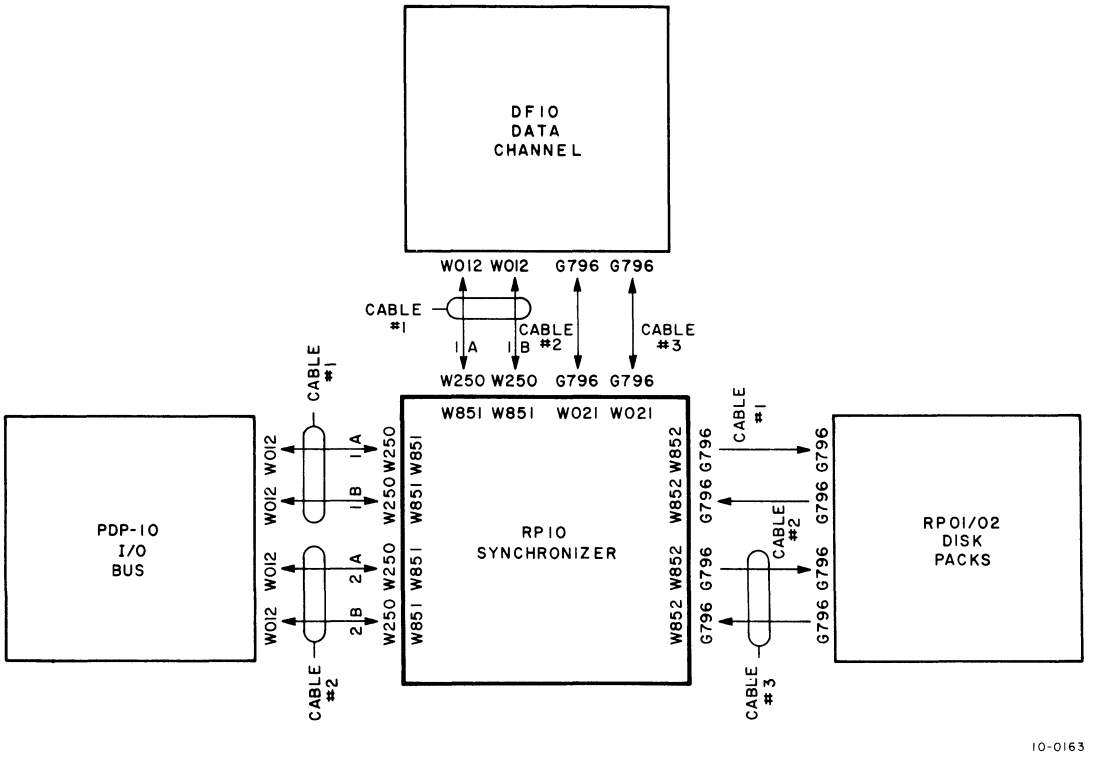


Figure 1-4 RP10/RP01/02 Electrical Interface

Table 1-2
RP10/RP01 and RP02 Interface Chart

Between		Function	Cable Type
RP10	RP01/02		
P/R-21	J3	Address and Control Bus Lines Cylinder Address Bus Lines	G796-G796
P/R-22	J5	Tag lines, Unit Select, Write Data, +36 Vdc in, Controlled Ground, 'Attention', Unit Selected, Ready, On-Line, Index Pulse, Sector Pulse, File Unsafe, Seek Incomplete, End of Cylinder, Read Data, Read Only, Write Current Sense.	G796-G796

The RP10 feeds the Disk Pack with eight multifunction address and control bus lines, three tag lines, a unit select line, a write data line, sequence out, +5V to terminator, and controlled ground. The Disk Pack feeds the RP10 with 'attention', ready, on-line, index pulse, sector pulse, file unsafe, seek incomplete, end of cylinder, read data coax, eight cylinder address lines, read only, and selected unit sector pulse.

1.3.2 RP10/DF10 Interface

There are three cable assemblies through which the RP10 connects to the DF10 Data Channel (see Figures 1-5 and 1-6). These assemblies and their functions are listed in Table 1-3.

Table 1-3
RP10/DF10 Interface Chart

Between		Function	Cable Type
RP10	DF10		
P/R-1/2	K/L-31/32	Chan Cable No. 1	W250-W012
P/R-11	K-21	Chan Cable No. 2	G796-G796
P/R-12	L-21	Chan Cable No. 3	G796-G796

1.3.3 RP10/I/O Interface

There are two cable assemblies through which the RP10 connects to the PDP-10 I/O Bus (see Figures 1-5 and 1-6). These cable assemblies are listed in Table 1-4; the signals they carry are also included.

Table 1-4
RP10/I/O Interface Chart

Between		Function	Cable Type
RP10	I/O Bus		
P/R-13/ 14/17/18	Cable 1	IOB 00-35	W250-W012
P/R-15/ 16/19/20	Cable 2	IOB Reset, IOBD DR SPLIT, IC IOS 03-09, DATAO, DATAI, CONO, CONI, RD1PLS, RD1 DATA, PI 1-7	W250-W012

1.3.4 Disk Pack/Disk Pack Interface

Two cable assemblies run serially between all Disk Pack Units. These cables carry sequence out plus all signal and control interconnections between the RP10 and the first Disk Pack. The sequence out from the RP10 is relayed to the next drive when this drive is up to speed and is drawing its running current (not more than 5A, RP01, or 7A, RP02).

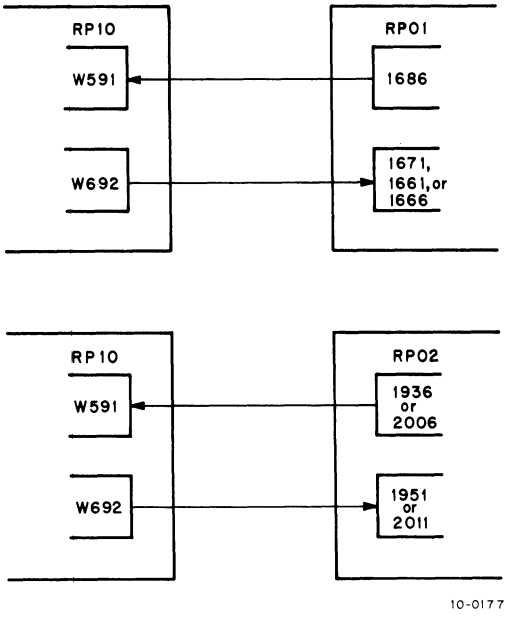


Figure 1-5 RP10 Interface Wiring Diagram

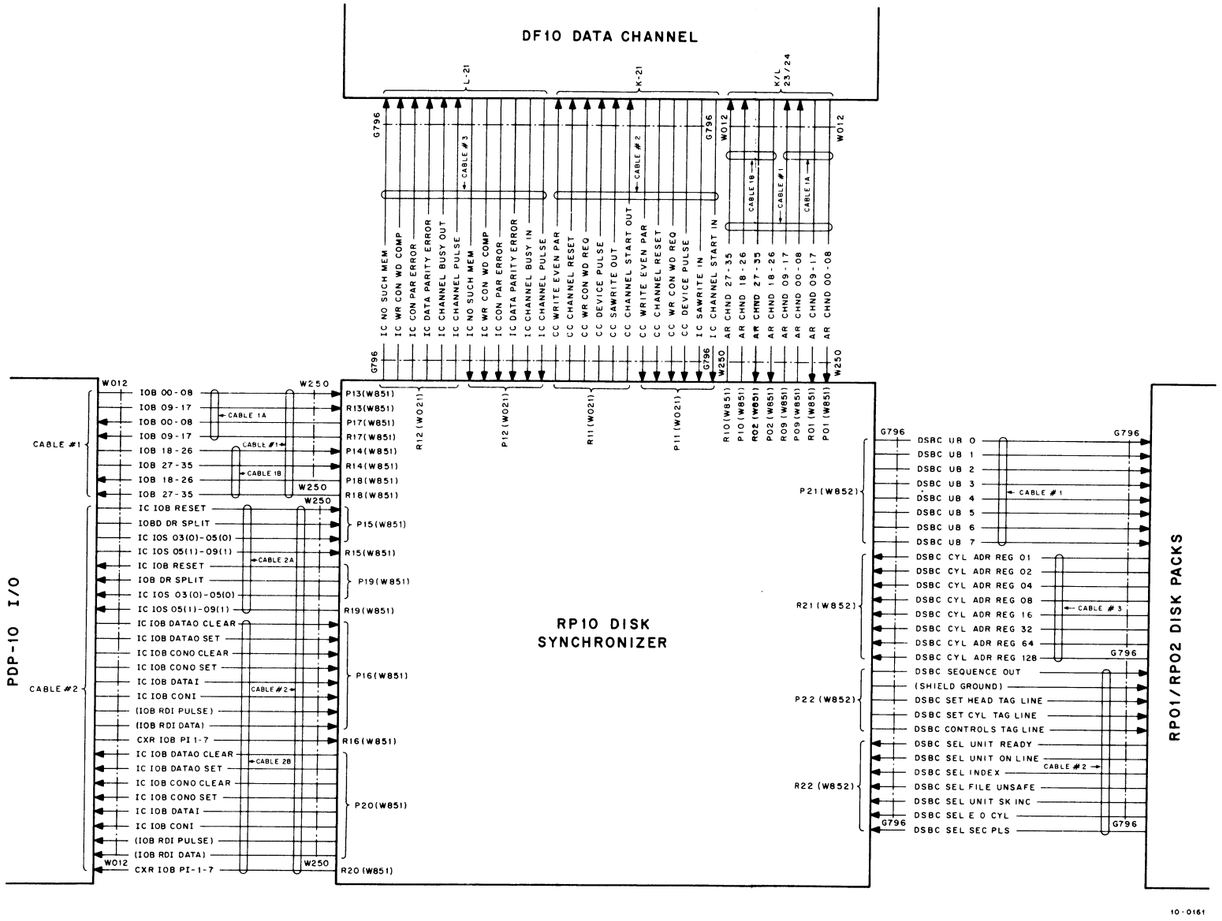


Figure 1-6 RP10 Cable Diagram

1.4 EQUIPMENT SUPPLIED

Table 1-5 lists the equipment supplied with the RP10 Disk Pack Synchronizer.

Table 1-5
Equipment Supplied

Quantity Per Equipment	Description	Part Type No.	Quantity Per Equipment	Description	Part Type No.
1	Synchronizer	RP10	1	Cable G796 to G796	C-IA-7005469-13
2	Cables W250 to W012	D-IA-7005459-12	1	Cable G796 to G796	C-IA-7005469-6
5	Cables W250 to W012	D-IA-7005459-24	1	Cable G796 to G796	C-IA-7005469-7
2	Cables W250 to W012	D-IA-7005459-15	1	Cable, Grounding	
1	Cable W250 to W012	D-IA-7005459-8	1 set	Spare Modules	
2	Cables W250 to W012	D-IA-7005459-11	1 set	Diagnostic Tapes	MAINDEC 10-D5OB MAINDEC 10-D5MA MAINDEC 10-D5NB
2	Cables G796 to G796	C-IA-7005469-10	1 ea.	Maintenance Manual (2 volumes)	DEC-10-H5EB-D
1	Cable G796 to G796	C-IA-7005469-2	1 set	Engineering Drawings	

1.5 REFERENCE DOCUMENTS

The following documents supplement the information contained in this manual:

PDP-10 System Reference Manual
DF10 Data Channel Maintenance Manual
PDP-10 Site Preparation Guide
PDP-10 Interface Manual
Vendor Manual for RP01/RP02 Disk Pack Drive

This material is available from the nearest DEC Field Office or from:

Digital Equipment Corporation
Direct Mail Department
146 Main Street
Maynard, Massachusetts 01754

1.6 GLOSSARY

The abbreviations used throughout this manual are defined in Volume II of this manual.

Chapter 2
Installation

2.1 GENERAL

This chapter contains information required for installation of the RP10 Disk Pack Synchronizer. The installation procedures are not complex because the RP10 is shipped complete and factory tested. When the equipment is received, all modules are in place and, all intra-bay cabling has been installed. The unit has been tested extensively while operating as part of a standard PDP-10 System. Turn-on and checkout procedures are included herein to confirm operation of the equipment after it has been installed.

The equipment rack should be located as near as possible to the DF10 Data Channel, preferably next to the DF10 frame. Bolt the equipment rack to the main rack in four places using the hardware provided. Cable lengths and the location of the RP01/RP02 drives are the major factors governing placement of the RP10.

2.2 UNPACKING

The following paragraphs describe the RP10 unpacking procedures.

2.2.1 Special Handling

No special handling procedures are required for the RP10 beyond the normal care afforded any piece of scientific equipment of comparable size and weight. However, particular care should be exercised in the use of cranes or hoists to prevent damage to the unit.

2.2.2 Inspection

On receipt of the equipment, inspect it for visible damage such as dents and abrasions that may have occurred in transit. Inspect the logic modules for foreign matter that may have lodged in them during shipment. Any damage should be reported immediately to both the Carrier and Digital Equipment Corporation. Check the contents of the carton with the shipping document and with Table 1-5 of this handbook. Immediately report any omissions or incorrect parts to Digital Equipment Corporation.

2.2.3 Power Requirements

The RP10 is equipped with self-contained power supplies and power control. The +10 Vdc and -15 Vdc requirements of the unit are provided by four DEC Type 728 Power Supplies and a DEC Type 844 Power Control. Modifications for accommodating either 50- or 60-Hz operation are made within the basic unit. These are designated as RP10-A for 60-Hz and RP10-B for 50-Hz operation. Power is supplied from an 8A, 115 Vac, single-phase source. The RP01/02 Drives require a three-phase line. Power requirements per phase are listed in Table 2-1.

Table 2-1
RP01/RP02 Power Requirements

Type of Drive	Number of Drives		
	1-3	4-6	7 or 8
RP01	8A	16A	23A
RP02	12A	24A	36A

NOTE
Three-phase power is required for from one through any number of drives. Each unit is a single-phase device but is connected on a phase rotation basis.

PDP-10 Systems operate from three-phase, Y-connected, 4-wire plus earth ground power mains. Standard voltages are 115/200 Vac ±10%, 60 Hz ±1/2 Hz and 230/400 Vac ±10%, 50 Hz ±1/2 Hz. Other common voltages can also be accommodated. A system earth ground connection must be supplied through the power cords in addition to the ground bus requirement.

The RP10 is supplied with terminal lugs, a 3-wire cord, and in North America, a 5-wire Hubbell #3521 male plug (mates with Hubbell #3520). One wall power cord is required for every RP01/02.

Terminal lugs are suitable for No. 10 to No. 18 AWG wire (0.04 to 0.12 in., 1 to 3 mm).

2.3 INSTALLATION PROCEDURE

To install the RP10, proceed as follows:

Step	Procedure
1	Ensure that all power is removed from the PDP-10 System and from the RP01/02 Disk Packs.
2	Remove the shipping skid from the bottom of the rack and discard it.
3	Remove the front and rear panel doors, and both side panels from the RP10.
	NOTE **Overall dimensions are given in Figure 2-1.**
4	Set the rack in place next to the DF10 Data Channel and lower the floor pads on both units to prevent rolling.
5	Bolt the RP10 rack (in four places) to the DF10 rack already in place.
6	Install the grounding cable to the bottom horizontal rack member. Tie the ground lead to the next grounded rack or to a system grounding bus.
7	Install separate grounds (No. 4 standard PDP-10 ground bus) from each drive to the RP10 (star ground system).
8	Connect cables according to the site plan and cabling list supplied with each installation (see Figure 2-2).

Step	Procedure
8 (Cont)	**NOTE** **Inspect all cable connectors for shipping and handling damage; install them carefully and securely. All power and signal cables should be routed 1 ft apart, if possible. Power and signal cables should cross at a 90° angle.**
9	Locate the drives and level each to within 5°.
10	Connect the remote turn-on power cable from the lower REMOTE CONTROL power outlet on the power control unit of the preceding rack to the upper REMOTE CONTROL power receptacle of the RP10.
11	Connect the Margin Check Remote Control Cable from J1 of the preceding Power Connector Assembly Bracket to J2 of the same bracket on the RP10.
	NOTE **If the RP10 is the last unit in the Margin Check bus, install the terminating plug in J1 of the RP10 Power Connector Assembly Bracket.**
12	Connect the RP10 power cable, already connected and secured to the Power Control Unit, to the system source of ac power.
13	Install any I/O bus termination plugs required (refer to DEC-10-HIFB-D, PDP-10 Interface Manual).
14	Replace side panels and panel doors.
15	On the drives, carefully remove tape from heads (installed for shipping purposes).
16	Inspect each head to ascertain that it is resting on the proper launching block.
17	Before attempting ON-LINE operation, Head and Servo Alignment must be checked and, if necessary, adjusted with C.E. Packs and an OFF-LINE Tester. See considerations in Paragraph 5.3.4. To load a disk pack on the drive, refer to Paragraph 3.3.1.
18	Using the OFF-LINE Tester perform the following steps on each drive as described in the Vendor Maintenance Manual: 1. Adjust voltage and high/low voltage sense. 2. Adjust positioner as described in Vendor Manual. 3. Perform head alignment with C.E. Pack after completing a Thermal Equilibrium Procedure as described in Paragraph 5.3.4.2d.
	NOTE **When using the OFF-LINE Tester, do not have either a cable or terminator block on 'signal out'.**

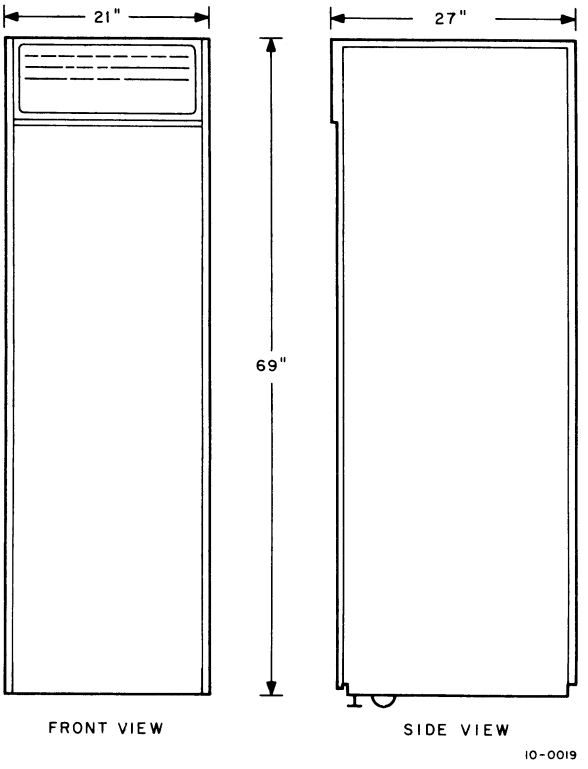


Figure 2-1 RP10 Overall Dimensions

2.4 TURN-ON AND CHECKOUT PROCEDURES

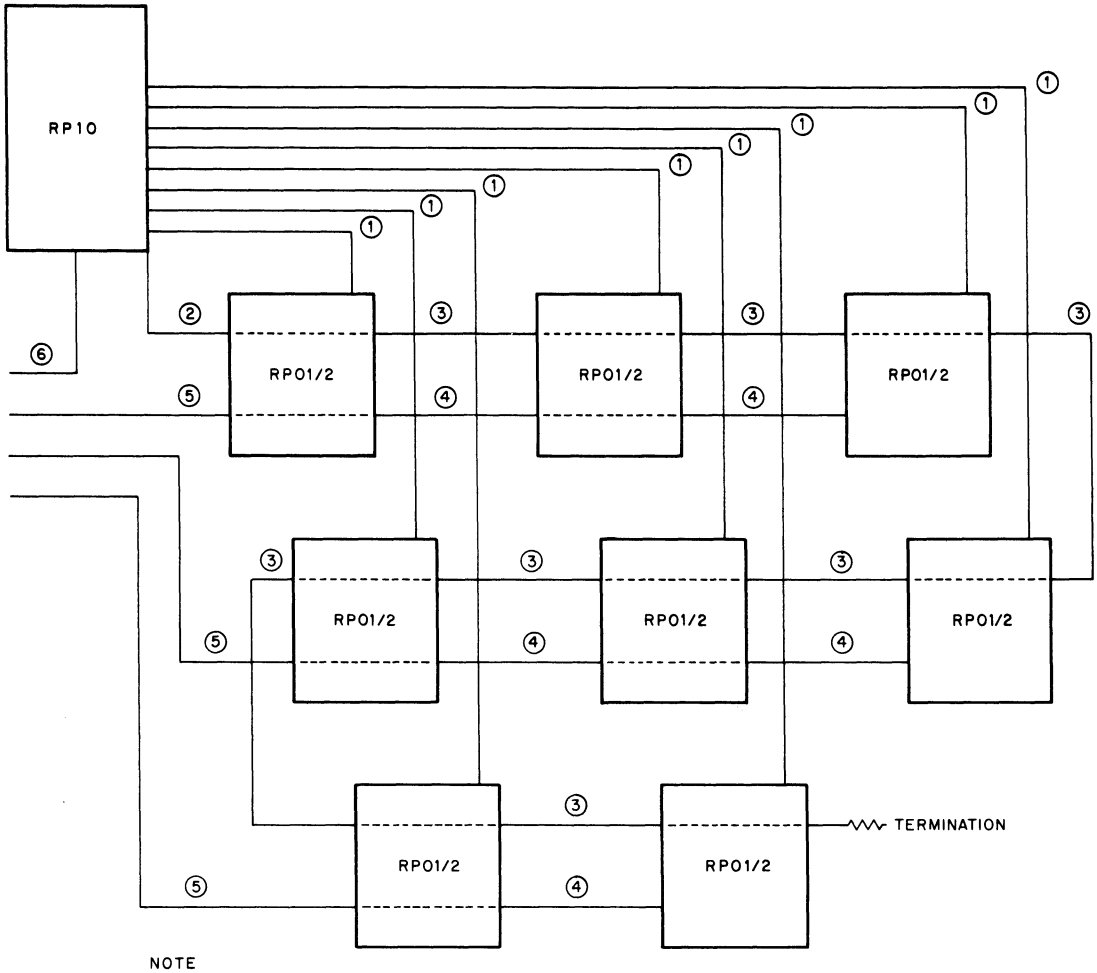
When the RP10 has been installed, verify its operation by proceeding as follows:

Step	Procedure
1	Set all switches on switch panel to the down position. Make certain that all margin check switches are in the OFF position.
2	Apply power to PDP-10 computer system and RP01/02 Disk Pack Drives. The POWER indicator lamp should light.
3	Set LOCAL/OFF/REMOTE switch on the DEC Type 844 Power Control panel to LOCAL position.
4	Set PWR circuit breaker and the power switch located on Power Control panel to ON. The cooling fans should begin to operate.
5	Refer to the MAINDEC Diagnostic Routine and RP10 System Test Procedure to conduct final checkout of RP10 Synchronizer.

NOTE

Run diagnostics and reliability programs using scratch packs or maintenance packs. Scratch packs used for reliability testing must be Mapped before they can be used with Monitor system because the entire surface is subject to writing by Reliability Test.

Step	Procedure
6	Refer to Chapter 5 for any adjustments required during, or as a result of, this installation procedure. Adjustment procedures for the drives are contained in applicable Vendor Manuals.



NOTE
1 TOTAL COMBINED LENGTHS OF 2,3 CANNOT EXCEED 100FT.(30m)
2 ALL RP10 SYSTEM POWER CORDS MUST BE PLUGGED IN SOCKETS LOCATED PHYSICALLY AND ELECTRICALLY NEAR EACH OTHER.
3 ONE WALL POWER CORD IS REQUIRED FOR EACH GROUP OF 3 RP01/2's.

LEGEND

① Unit Cable (One per Drive)	15 FT (4.5m)	70-6601-1
	25 FT (7.5m)	70-6601-2
	40 FT (12.0m)	70-6601-3
② RP10-RP01/02 Signal Cable	15 FT (4.5m)	70-6463-1
	25FT (7.5m)	70-6463-2
	40FT (12.0m)	70-6463-3
③ RP01/02-RP01/02 Signal Cable	8FT (3.6m)	70-6465-1
	25FT (7.5m)	70-6465-2
④ RP01/02-RP01/02 Power Cord	8FT (3.6m)	70-6600-1
	25FT (7.5m)	70-6600-2
⑤ RP01/02 Wall Power Cord	25FT (7.5m)	70-6464
⑥ RP10 Power Cord	25 FT (7.5m)	70-5128

10-0534

Figure 2-2 RP10-RP01/RP02 Signal and Power Connections

Chapter 3
Operation

3.1 GENERAL

Chapter 3 contains operating and programming information required to operate the RP10 Disk Pack Synchronizer. Also included in this chapter is an identification of the controls and indicators. A brief summary of RP01/02 characteristics is given as an introduction to RP10 programming considerations.

3.2 CONTROLS AND INDICATORS

The controls and indicators for the RP10 are located on the top front of the unit. The indicators are all located on one panel and the controls on another. The controls and indicators are shown in Figure 3-1 and defined in Table 3-1. Power controls and indicators are located behind the rear panel door on the Type 844 Power Control.

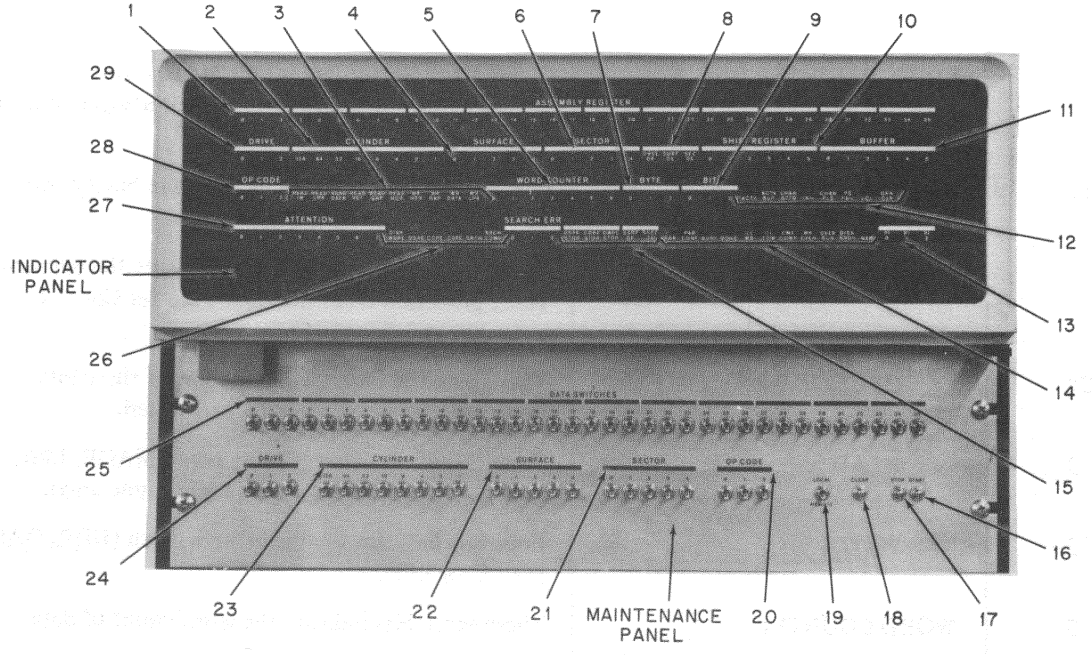


Figure 3-1 RP10 Controls and Indicators

Table 3-1
RP10 Controls and Indicators

Index No. (Figure 3-1)	Name	Function
1	ASSEMBLY REGISTER 00-35	These thirty-six indicator lamps light when their associated Assembly Register bit is set to 1. These lamps indicate the contents of the Assembly Register AR00-AR35.
	Data Address Register	These twenty-one indicator lamps light when their associated Data Address Register bit is set to 1. These lamps indicate the contents of the register as follows;
29	DRIVE	These three bits indicate which of eight possible disk drives has been selected.
2	CYLINDER	These eight bits indicate which track cylinder on the selected drive has been selected.
4	SURFACE	These five bits indicate which surface of the selected drive has been selected.
6	SECTOR	These five bits indicate which sector of the selected drive surface track has been selected.
8	Designation Error	These three indicator lamps indicate the data address component in error. Tied to the Header comparator, they indicate either DRIVE DE, SURF DE, or SEC DE designation error.
10	SHIFT REGISTER 0-5	These six indicator lamps indicate the contents of the Shift Register by lighting when their associated bit is set to 1.
11	BUFFER 0-5	These six indicator lamps indicate the binary contents of the Shift Register Buffer.
	Data Channel	These thirteen indicator lamps indicate the command being processed from the Data Transfer Control assembly as follows;
28	OP CODE 0-2	Three bits, the binary combination of these bits indicates the operation to be performed.
3	READ	Six bits indicate what is being read; IMAGE, LPR, DATA, GAP, HDR, or REF (a VFO sync area).
3	WRITE	Four bits indicate what is being written (HDR, GAP, DATA, or LPR).
5	WORD COUNTER	These seven bits indicate the word count of data.
7	BYTE 0-2	These three bits indicate the shift count of bytes.
9	BIT 0-2	These three bits indicate the bit count.
12	Status Bits	These eight indicator lamps indicate the status of the following conditions;

Table 3-1 (Cont)
RP10 Controls and Indicators

Index No. (Figure 3-1)	Name	Function
12 (Cont)	ACTV	This bit indicates that the Synchronizer has asserted CHAN START OUT and will have control of the channel next, or has control of the channel.
	ACTV BUF	This bit indicates that the Synchronizer wants control of the channel.
	CHAN STTD	This bit indicates that some device has control of the channel.
	INH	This bit indicates that the CC Inhibit flop is set.
	CHAN PLS	This bit indicates that a Channel Pulse has been received since the last Device Pulse was sent.
	PS FAIL	This bit indicates that the RP10 Power Supply outputs are out of tolerance.
	LCL	This bit indicates that the Synchronizer is in Local mode.
	GEN CLR	This bit indicates that the Synchronizer is idle.
27	ATTENTION 0-7	These seven indicator lamps indicate that an interrupt has been received from a drive, and that it has not been serviced and cleared by a CLEAR ATTENTIONS op code.
	Parity Error	These four indicator lamps indicate the parity component in which an error has been detected, as follows;
26	DISK WDPE	Parity Error in the Disk Word.
	DSPE	Parity Error in the Longitudinal Parity Word of a disk sector.
	CCPE	Parity Error in the Channel Control Word.
	CDPE	Parity Error in the Channel Data Word.
26	SRCH	This bit indicates that a search operation is in progress.
26	SRCH COMP	This bit indicates that the Synchronizer has found the first sector to be transferred in a read or write data command.
26	SEARCH ERR 0-2	These three bits count the number of index pulses seen while the search flop is on. If all bits are on, the controller shuts down. After SRCH COMP is set, bit 2 will be set, if a header (other than the first header in a multiple sector operation) was read incorrectly.
15	Disabling Bit Status	These three bits indicate whether or not certain flags have been disabled as follows;
	DSPE STOP	This bit indicates that Disk Sector Parity Error will not stop read commands.

Table 3-1 (Cont)
RP10 Controls and Indicators

Index No. (Figure 3-1)	Name	Function
15 (Cont)	CDPE STOP	This bit indicates that the Channel Data Word Parity Error will not stop write commands.
	DWPE STOP	This bit indicates that the Disk Word Parity Error will not stop read commands.
14	Status Bits	These eleven bits indicate the status of the following conditions;
	PAR	This bit indicates that the DTC Parity flop is set.
	PAR CONT	This bit indicates that the Parity Control flop is set.
	BUSY	This bit indicates that the Synchronizer is busy executing a data transfer command.
	DONE	This bit indicates that the DONE flag has been raised and the Synchronizer is no longer busy.
	ILL WR	This bit indicates that a write command has been suppressed because the READ-WRITE/READ ONLY switch on the addressed drive is in the READ ONLY position. Indicates a write operation was in process when a sector pulse was received.
	ILL COM	This bit indicates that a command to the Synchronizer during a data transfer has been suppressed.
	CWX COMP	This bit indicates that transfer of the initial control word address is complete.
	WR EVEN	This bit indicates that even parity is being written into memory on all data words read from the disk.
	OVERRUN	This bit indicates that the channel did not send a channel pulse between two device pulses.
	DISK NRDY	This bit indicates that the drive selected is either not ready, unsafe, or off line.
	NXM	This bit indicates that the channel tried to access a non-existent memory location.
13	PI 0-2	These three bits indicate the interrupt channel to which the unit has been assigned.
25	DATA SWITCHES 0-35	These thirty-six toggle switches permit toggling in any 36-bit data word to be written into disk-pack memory for testing purposes. Signals SWP DATA 00 through 35 are generated.
	Data Address	These twenty-one toggle switches permit toggling in any 21-bit disk-pack memory address into which the DATA SWITCHES word is to be written. These switches function as follows;

Table 3-1 (Cont)
RP10 Controls and Indicators

Index No. (Figure 3-1)	Name	Function
24	DRIVE 0, 1, 2	These three toggle switches determine which of eight disk drives is selected by generating signals SWP DRIVE 0, 1, 2 in eight possible binary combinations.
23	CYLINDER	These eight toggle switches determine which track-cylinder on the selected drive is selected by generating combinations of signals as follows;
	128	SWP CYL 128
	64	SWP CYL 64
	32	SWP CYL 32
	16	SWP CYL 16
	8	SWP CYL 8
	4	SWP CYL 4
	2	SWP CYL 2
	1	SWP CYL 1
22	SURFACE 0-4	These five toggle switches determine which surface of the selected drive and track-cylinder is selected. This is accomplished by generating binary combinations of signals SWP SURF 0-4.
21	SECTOR 0-4	These five toggle switches determine which sector of the selected surface, track-cylinder, and drive is selected. This is accomplished by generating binary combinations of signals SWP SEC 0-4.
20	OP CODE 0-2	These three toggle switches determine the operation to be performed by the disk pack by generating binary combinations of signals SWP OP 0-2.
19	LOCAL/REMOTE	This toggle switch places the RP10 in Local mode or Remote mode by generating the signal SWP LOCAL SET when in the up position and SWP LOCAL CLR when in the down position.
18	CLEAR	This pushbutton switch, when pressed, clears all registers and stops the current operation by generating the signal SWP CLEAR. Inoperative in Remote mode.
17	STOP	This pushbutton switch, when pressed, stops data transfer immediately by generating the signal IBC STOP. Inoperative in Remote mode.
16	START	This pushbutton switch, when pressed, initiates an operation by generating SWP START. Inoperative in Remote mode.

3.3 OPERATION

The following paragraphs give a detailed description of the operation of the RP10 Disk Pack Synchronizer.

3.3.1 Loading, Unloading, and Storage of RP01P/02P Disk Packs

NOTE

The RP01/02 START/STOP switch should be left in the STOP position until an RP01/02 Disk Pack has been loaded and the cover has been closed.

To load a disk pack on the Disk Pack Drive, proceed as follows:

Step	Procedure
1	Make certain that power has been removed from the drive and/or the PDP-10.
2	Holding the disk pack, enclosed in its plastic container, by the top handle; rotate the bottom cover latch and remove.
	NOTE **The disk pack will remain attached to top cover.**
3	Raise the cover on the drive and lower the pack, with its cover attached, into the well provided until the pack seats on its conical hub.
4	Rotate the top cover latch and disk assembly clockwise until the pack is properly seated and secure.
	CAUTION **Do not overtighten the pack; snug fit is sufficient.**
5	Once installed, rotate the top cover latch in the opposite direction and remove the top plastic cover by lifting it out of the well.
6	Return the top and bottom covers to live storage.
7	Close the lid on the drive and reapply power.

To unload a disk pack from the Disk Pack Drive, proceed as follows:

Step	Procedure
1	Make certain that power has been removed from the drive and/or the PDP-10.
2	Wait for the automatic breaks to stop the drive before raising the lid on the drive.
	NOTE **If the lid is opened when the drive is powered up, power is automatically removed and braking action is applied.**
3	Remove the plastic top cover from its bottom cover and lower the top cover into the well over the disk pack.

Step	Procedure
4	Once top cover is seated, rotate the top cover latch counter-clockwise until a clicking sound occurs.
5	Rotate the latch in the opposite direction to loosen the pack from its hub.
6	Holding the bottom cover ready, raise the cover and pack assembly out of its well and place it firmly on its bottom cover.
7	Rotate the bottom cover latch until it is snug; then, return the encased disk pack to live storage.
8	Close the cover on the disk pack drive and reapply power.

Store the RP01/02P Disk Pack in its plastic container in the same ambient conditions prevailing at the drive.

The maintenance panel is used to operate the RP10 in Local mode; the indicator panel monitors this operation. For general operation of the RP10, proceed as follows:

Step	Procedure
1	Place the LOCAL/REMOTE switch on the maintenance panel in LOCAL position.
2	Set OP CODE switches for desired operation.
3	Set address desired in DRIVE, CYLINDER, SURFACE, and SECTOR switches.
4	To select data to be written, set the 36-bit DATA switches on the maintenance panel.
5	Depress the START pushbutton. The Synchronizer will perform the selected operation, terminate, restart, and repeat the operation.
6	To discontinue operation, depress the STOP pushbutton. The Synchronizer will terminate at the conclusion of the operation.

NOTE

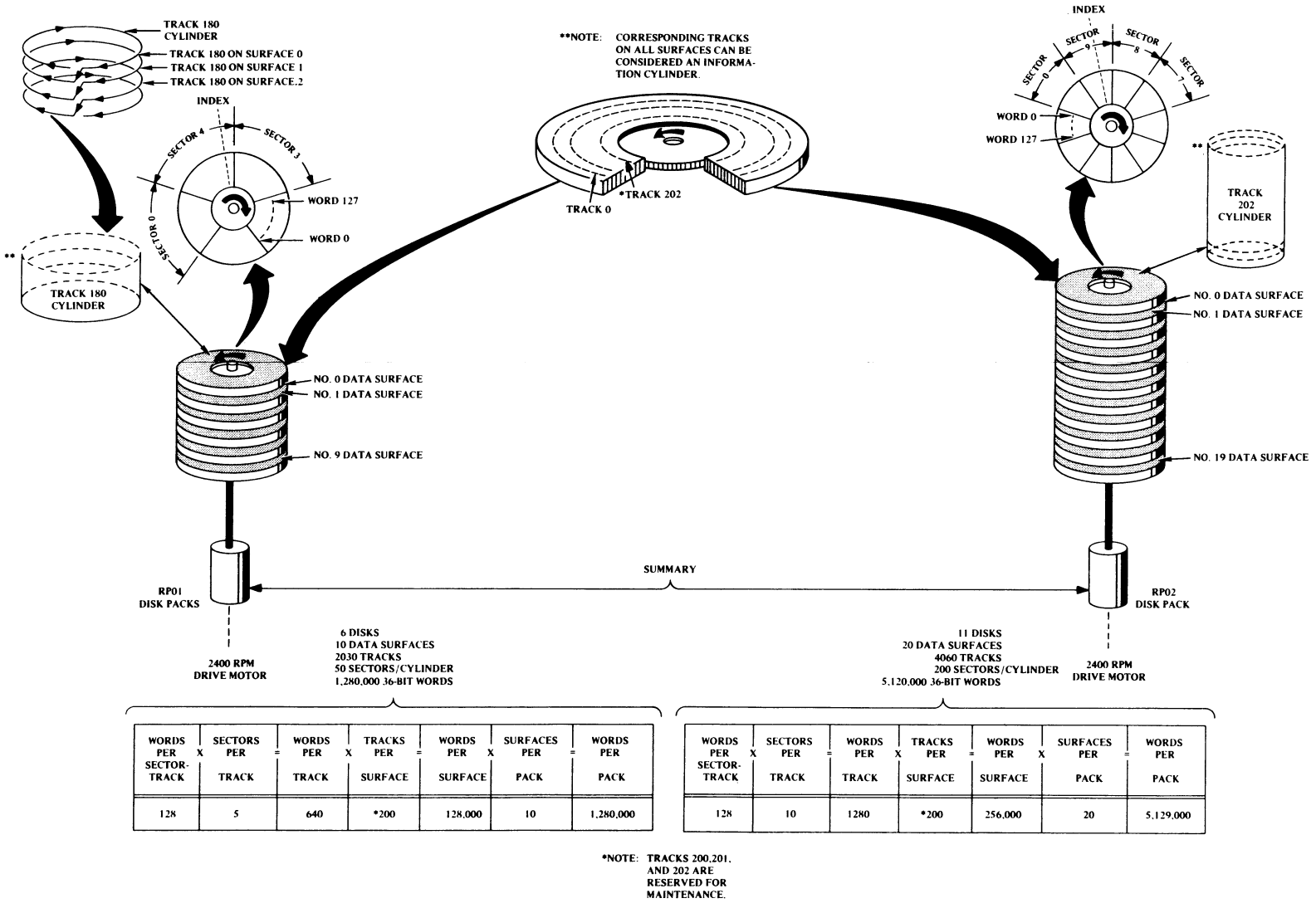
For single-cycle operation, hold the STOP pushbutton while depressing START. Depressing CLEAR will clear all registers and stop operation.

3.4 PROGRAMMING

Programming of the RP10 is predicated on the requirements imposed by the RP01/02 Disk Packs; therefore, a brief summary of the file is given here as an introduction to programming techniques (see Figures 3-2 and 3-3).

3.4.1 RP01/02 Disk Pack Characteristics

The total capacity of the RP01 Disk Pack is 46,125,440 bits, which is equivalent to 1,559,040 36-bit words; the total capacity of the RP02 Disk Pack is 205,793,280 bits, the equivalent of 5,716,480 36-bit words. In actual practice, however, the two outside surfaces on both Disk Packs are not used and, on all surfaces, tracks 200, 201, and 202 are reserved as spares. When these conditions are recognized, and when parity is added to each word, the relative characteristics are as depicted in the Summary portion of Figure 3-2. This yields a total data word capacity of 1,280,000 36-bit words for the RP01 and 5,120,000 36-bit words for the RP02.



WORDS PER SECTOR-TRACK	X	SECTORS PER TRACK	=	WORDS PER TRACK	X	TRACKS PER SURFACE	=	WORDS PER SURFACE	X	SURFACES PER PACK	=	WORDS PER PACK
128		5		640		*200		128,000		10		1,280,000

WORDS PER SECTOR-TRACK	X	SECTORS PER TRACK	=	WORDS PER TRACK	X	TRACKS PER SURFACE	=	WORDS PER SURFACE	X	SURFACES PER PACK	=	WORDS PER PACK
128		10		1280		*200		256,000		20		5,129,000

*NOTE: TRACKS 200,201, AND 202 ARE RESERVED FOR MAINTENANCE.

Figure 3-2 RP01/RP02 Disk Pack Characteristics

Each of the RP01 and RP02 Disk Packs contain 203 cylinders. Movable heads connected to a common positioning actuator access one cylinder at a time. Track-to-track, average, and maximum positioning times are 20, 50, and 80 ms, respectively. Rotation speed is 2400 rpm providing 12.5 ms average and 25 ms maximum latency times. Data is recorded by a double-frequency, nonreturn-to-zero technique. Data is formatted into 128-word sectors, individually addressable.

The RP01 has 10 read/write heads and the RP02 has 20. Recording frequencies are 1.25 x 10^6 bits/sec for the RP01 and 2.5 x 10^6 bits/sec for the RP02. Each RP01 track contains five sectors and each RP02 track contains 10 sectors. Word transfer rates are 30 μs for the RP01 and 15 μs for the RP02.

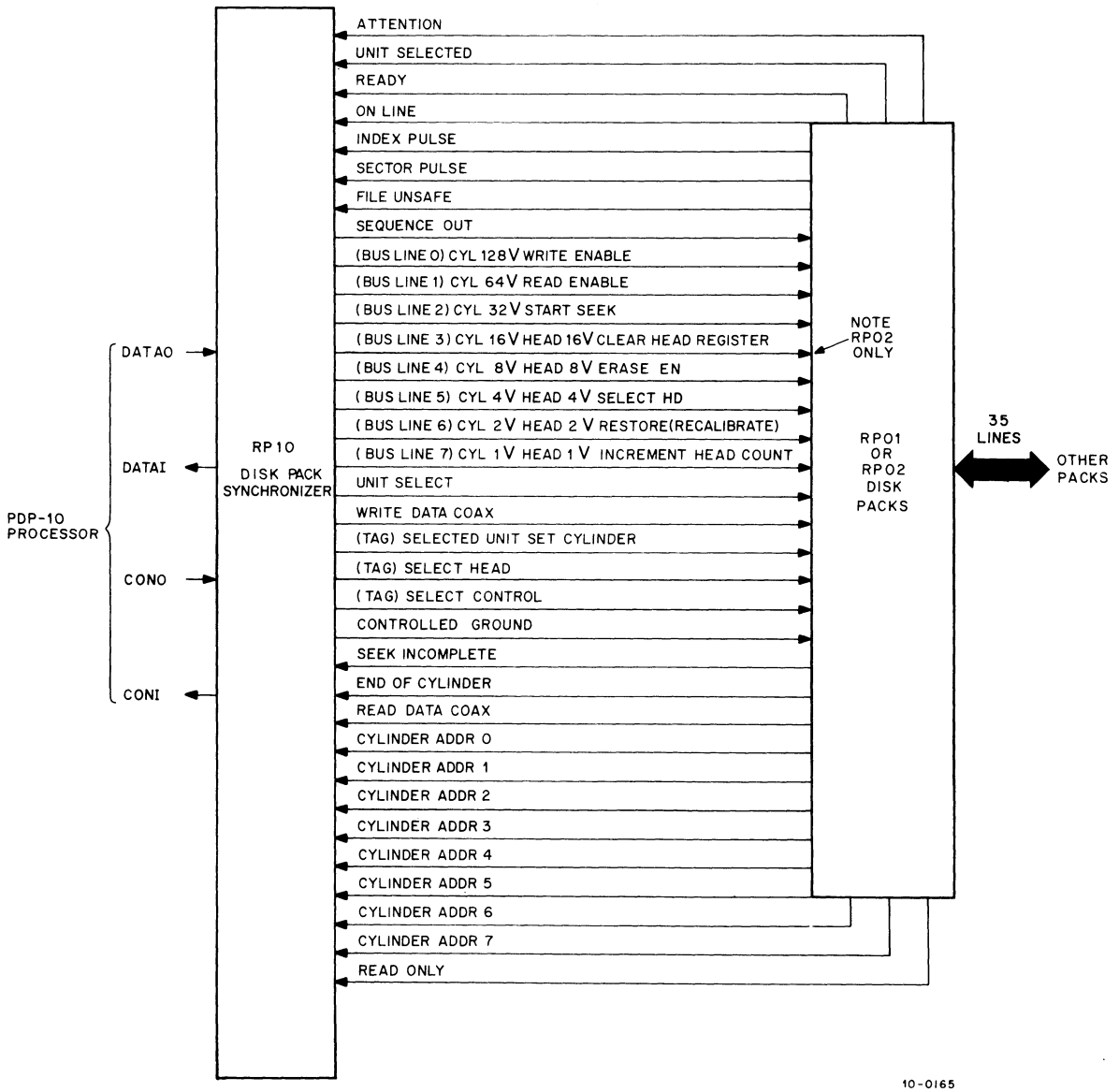


Figure 3-3 RP10/RP01/RP02 Data Control Signals

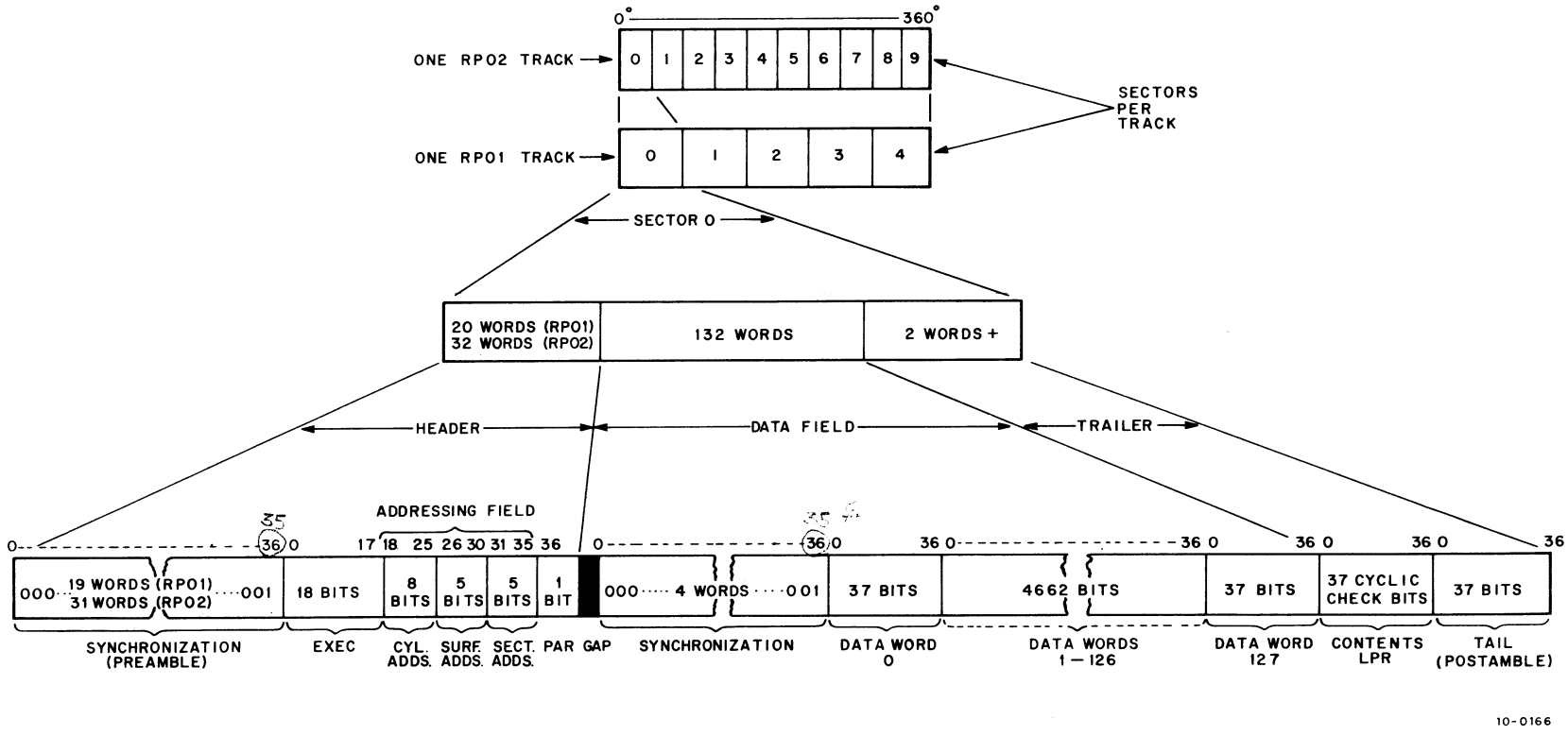


Figure 3-4 RP01/RP02 Data Format

Data formats for information recorded on the disks are arranged as shown in Figure 3-4. These data formats consist of a twenty-word header field on the RP01 (thirty-two on RP02), a data field of 132 words, followed by a two-word trailer.

The first 18 words in the RP01 header field (30 words in RP02) consist of zeros to allow the read circuitry to synchronize with the data. The 19th (31st on RP02) word contains an octal one (000000000001). The last header field word comprises the addressing field.

The first three words in the data field function as a READ DISENABLE/WRITE ENABLE field. The next data field word is used for synchronization, and contains an octal one (000000000001). These words are followed by 128 36-bit words, each followed by its own 37th parity bit.

The first word in the trailer field contains the contents of the longitudinal parity register, and the last word (tail or postamble) contains a second LPR.

NOTE

When executing a Write Header command, the first 24 words in an RP01 or the first 36 words in an RP02 are written without parity. Therefore, both bits must be in data and the first bit of the word following the header is interpreted as the parity bit of the header when read back.

Addressing is effected by the 18-bit partitioned binary number, defined as word two in the header. The partitioning has been selected to provide sequential access to the entire memory with a minimum of positioning operations.

The Exec area (Figure 3-4) is determined by the executive program (monitor, operating system) and is ignored by the interface, except for parity checking.

The cylinder address, an unsigned binary number which functions as the track address (positioner), contains eight bits to describe the 313_8 tracks. The outer track cylinder is represented by 000_8, and the inner track cylinder is represented by 312_8.

The surface address, a five-bit, unsigned binary number, selects one of 10 disk surfaces for the RP01 (codes 00_8 to 11_8 are legal), and selects one of 20 disk surfaces for the RP02 (codes 00_8 to 23_8 are legal). Other codes are illegal (nonexistent).

The sector address, a five-bit, unsigned binary number, selects the proper sector on a track. One of five sectors is selected on the RP01 (codes 00_8 to 04_8 are legal), and one of 10 sectors on the RP02 (00_8 to 11_8 are legal). Other codes are illegal (nonexistent).

In the RP01/02 there is one record per sector (see Figure 3-4). The sector mark defines the beginning of a record. All records are fixed length with a data field of 128 36-bit words plus parity. A header field associated with each record is used to identify the record and ensure that cylinder, surface, and sector selection is correct before writing or reading a record.

3.4.2 RP10 Programming

The RP10 modes of operation are position (seek cylinder), recalibrate, read data, write data, write header and data, and clear attentions. Channel instructions must be placed in memory prior to initiating a data transfer in the synchronizer.

3.4.2.1 **DATAO Information (see Figure 3-5)** – A DATAO 250 instruction either performs a positioning operation or initiates a data transfer, if the synchronizer is not already busy. The RP10 is capable of executing the six instructions mentioned in the preceding paragraph. The instructions are described below (DATAO 254 is used if a second RP10 is installed in a PDP-10 System).

a. Position Instruction (seek cylinder) – The Position instruction word, shown in Figure 3-6, is divided into four fields:

(1) Op Code: The Op Code is 4_8.

(2) Drive: The Drive field indicates the disk drive addressed. All codes are legal if the drives exist.

(3) Cylinder: The Cylinder field specifies the cylinder sought. Codes 000_8 through 312_8 are legal. Others are nonexistent.

(4) Bits 14-35: These bits are spares.

Execution of a position instruction requires 3 to 5 μs of synchronizer time and 20 to 150 ms of drive time. Positioning is controlled by a difference count of the present address register and the cylinder address register that is loaded by this instruction. When a zero difference count (compare) is reached, the heads are positioned.

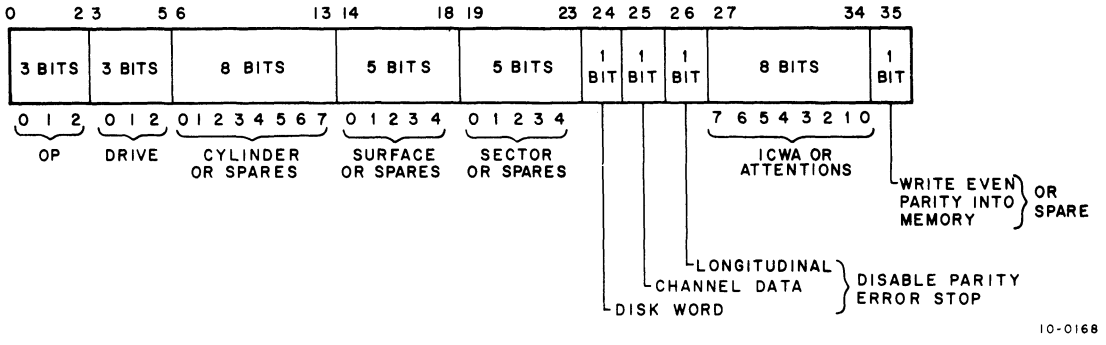


Figure 3-5 DATAO Instruction Word Format

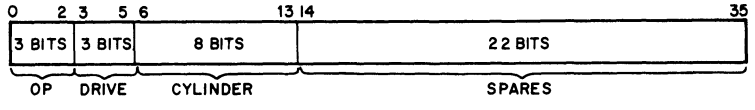


Figure 3-6 Position Instruction Word

b. Recalibrate Instruction – the Recalibrate instruction word, shown in Figure 3-7, is divided into three fields:

(1) Op Code: The Op Code is 7_8.

(2) Drive: The Drive field indicates the disk drive addressed. All codes are legal if the drives exist.

(3) Bits 6-35: These bits are spares.

Execution of a recalibrate instruction moves the positioner to cylinder zero by force. Positioning is not controlled by the difference count from the current address register, which may be wrong.

c. Read Data Instruction - The Read Data instruction word, shown in Figure 3-8, is divided into ten fields:

(1) Op Code: The Op Code is 0_8.

(2) Drive: The Drive field indicates the disk drive addressed. All codes are legal if the drives exist.

(3) Cylinder: The Cylinder field specifies the cylinder on which the data to be read resides. Codes 000_8 through 312_8 are legal. Other cylinders are nonexistent.

NOTE

The heads must have been previously positioned; this field is for verification only.

(4) Surface: The Surface field indicates the recording surface on which the data to be read resides. Codes 00_8 through 11_8 are legal on RP01. Codes 00_8 through 23_8 are legal on RP02. All others are nonexistent.

(5) Sector: The Sector field indicates the sector on which the data to be read resides. Codes 00_8 through 04_8 are legal on RP01. Codes 00_8 through 11_8 are legal on RP02. All others are nonexistent.

(6) Bit 24: This bit is set to 1 to disable longitudinal parity error stop. If not disabled, the discovery of a longitudinal parity error stops data transmission and sets the longitudinal parity error bit.

(7) Bit 25: This bit is a spare.

(8) Bit 26: This bit is set to 1 to disable the disk word parity error stop. If not disabled, the discovery of a disk word parity error stops data transmission and sets the disk word parity error bit.

(9) ICWA: The ICWA field specifies bits 27-34 of the Initial Control Word Address. All binary values above 17_8 are legal.

NOTE

The channel cannot access the fast registers.

(10) Bit 35: This bit, when set, causes the channel to write even parity into memory on all data words read from the disk.

The Read Data instruction causes data to be read until either the channel shuts down or the end of the cylinder is reached.

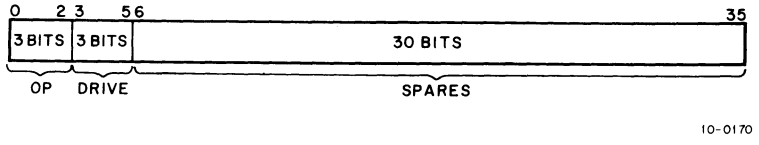


Figure 3-7 Recalibrate Instruction Word

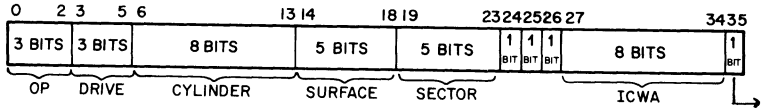


Figure 3-8 Read Data Instruction Word

d. Write Data Instruction – The Write Data instruction word, shown in Figure 3-9, is divided into ten fields:

(1) Op Code: The Op Code is 1_8.

(2) Drive: The Drive field indicates the disk drive addressed. All codes are legal if the drives exist.

(3) Cylinder: The Cylinder field specifies the cylinder on which the data is to be written. Codes 000_8 through 312_8 are legal. Other cylinders are nonexistent.

NOTE

The heads must have been previously positioned. This field is for verification only.

(4) Surface: The Surface field indicates the recording surface on which the data is to be written. Codes 00_8 through 11_8 are legal on RP01. Codes 00_8 through 23_8 are legal on RP02. All others are nonexistent.

(5) Sector: The Sector field indicates the sector on which data is to be written. Codes 00_8 through 04_8 are legal on RP01. Codes 00_8 through 11_8 are legal on RP02. All others are nonexistent.

(6) Bit 24: This bit is a spare.

(7) Bit 25: This bit is set to 1 to disable channel data word parity error stop. If not disabled, the discovery of a channel data word parity error stops data transmission and sets the channel data word parity error bit.

(8) Bit 26: This bit is a spare.

(9) ICWA: The ICWA field specifies bits 27-34 of the initial control word address. All binary values above 17_8 are legal.

NOTE

The channel cannot access the fast registers.

(10) Bit 35: This bit is a spare.

This instruction causes data to be written until either the channel shuts down or until the end of the cylinder is reached.

NOTE

If the last (or only) sector to be written is shorter than 128 words, the remainder of the field is filled with words "all zeros."

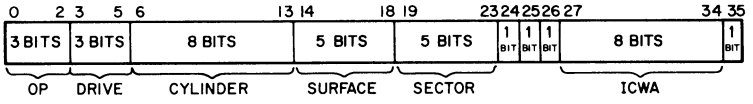


Figure 3-9 Write Data Instruction Word

e. Write Header and Data Instruction – The Write Header and Data instruction word, shown in Figure 3-10, is divided into nine fields:

(1) Op Code: The Op Code is 3_8.

(2) Drive: The Drive field indicates the disk drive addressed. All codes are legal if the drives exist.

(3) Surface: The Surface field indicates the recording surface on which the headers and data are to be written. Codes 00_8 through 11_8 are legal on RP01. Codes 00_8 through 23_8 are legal on RP02. All others are nonexistent.

(4) Bits 19-24: These bits are spares.

(5) Bit 25: This bit is set to 1 to disable channel data word parity error stop. If not disabled, the discovery of a channel data word parity error stops data transmission and sets the channel data word parity error bit.

(6) Bit 26: This bit is a spare.

(7) ICWA: The ICWA field specifies bits 27-34 of the initial control word address. All binary values above 17_8 are legal.

NOTE

The channel cannot access fast registers.

(8) Bit 35: This bit is a spare.

This instruction formats the disk. The RP10 searches for an index mark, then writes header and data fields as shown in Figure 3-4. The programmer supplies headers and data as described in Paragraph 3.4.1. The synchronizer writes one track of headers and data and adds the data word parity bits and the trailer field.

f. Clear Attentions Instruction – The Clear Attentions instruction word, shown in Figure 3-11, is divided into five fields:

(1) Op Code: The Op Code is 5_8.

(2) Drive: The Drive field indicates the disk drive addressed. All codes are legal if the drives exist.

(3) Bits 6-26: These bits are spares.

(4) Bits 27-34: These bits clear attentions 0-7, respectively.

(5) Bit 35: This bit is a spare.

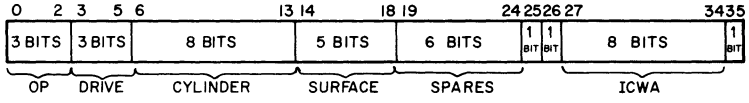


Figure 3-10 Write Header and Data Instruction Word

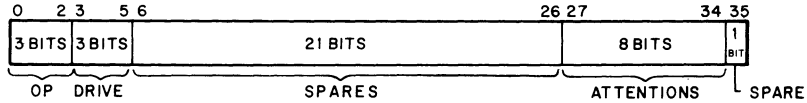


Figure 3-11 Clear Attentions Instruction Word

g. No Op Instruction – The No Op instruction word, shown in Figure 3-12, is divided into three fields:

(1) Op Code: The Op Code is 6_8.

(2) Drive: The Drive field indicates the disk drive addressed. All codes are legal if the drives exist.

(3) Bits 6-35: These bits are spares.

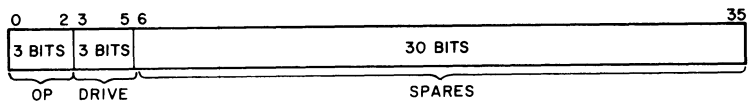


Figure 3-12 No Op Instruction Word

3.4.2.2 DATAI Information – A DATAI 250/254 Instruction supplies the programmer with information concerning the disk and cylinder selected, as defined below and illustrated in Figure 3-13 (250 for RP01 or 254 for RP02):

a. *Disk Selected* – This field indicates the disk most recently selected by a legal DATAO. IOB 0-2

b. *Cylinder Address Register* – This field displays the contents of the drive's cylinder address register. IOB 3-10

c. *Seek Incomplete* – This bit indicates that the drive was unable to complete the most recent position command addressed to it. The error recovery procedure is: issue a recalibrate command, which clears this error condition. IOB 11

d. *On Cylinder* – This bit indicates that the heads are positioned on the cylinder specified by the cylinder address register bits of this instruction word, and that data transfer may proceed. IOB 12

e. *On Line* – This bit indicates that *1)* the ENABLE/DISABLE switch is in the ENABLE position, *2)* a disk pack is mounted, *3)* the dust cover is closed, *4)* the spindle is up to operating speed, and *5)* the heads are mounted on the disk. IOB 13

f. *File Unsafe* – This bit indicates that either *1)* a head is selected when not on a cylinder, *2)* more than one head has been selected simultaneously, *3)* read and write were selected at the same time, *4)* write and/or erase were selected when the file was not ready, *5)* write current was sensed when write was not selected, *6)* write was selected with no write current, *7)* erase current was sensed without erase being selected, or *8)* write was selected without erase current. IOB 14

NOTE

The interface provides hardware to prevent any of these conditions from being caused by programming errors. To clear this bit, depress the STOP and START buttons. A full power-down/power-up sequence, requiring over one minute, must follow.

g. *No Such Drive* – When this bit is true, it indicates that the drive addressed does not exist. In this case, the other bits of this instruction word are meaningless. IOB 15

h. *Read Only* – When this bit is true, it indicates that the drive's READ-WRITE/READ ONLY switch is in the READ ONLY position. IOB 16

i. *Write Header Lockout* – This bit, when set, prevents headers from being written. IOB 17

j. *Sector Counter* – These bits indicate the state of this disk's sector counter. The sector counter is cleared by an Index Pulse and counts sector pulses. IOB 18-22

k. *Attentions* – These indicate which drives are requesting an interrupt due to Seek Incomplete or Seek Complete. IOB 27-34

3.4.2.3 CONO Information – A CONO command is illustrated in Figure 3-14 and described below:

a. Clear: These bits perform the following clear operations;

(1) Bit 20: When this bit is set to a 1, it clears the power supply failure (PS FAIL) flag only if the power supply fail conditions have been corrected.

(2) Bit 21: When this bit is set to a 1, it clears the search error (SRCH) flag.

(3) Bit 22: When this bit is set to a 1, it clears the overrun (OVERRUN) flag.

(4) Bit 23: When this bit is set to a 1, it clears the no such memory location (NXM) flag.

(5) Bit 24: When this bit is set to a 1, it clears the Channel Control Word Parity Error (CCPE), the Disk Sector Parity Error (DSPE), the Disk Word Parity Error (DISK WDPE), and the Channel Data Parity Error (CDPE) flags.

(6) Bit 25: This bit is a spare.

(7) Bit 26: When this bit is set to a 1, it clears the Illegal Write (ILL WR) flag.

(8) Bit 27: When this bit is set to a 1, it clears the Illegal Command While Busy (ILL COM) flag.

(9) Bit 28: When this bit is set to a 1, it clears the Sector Designation Error (SEC DE) flag.

(10) Bit 29: When this bit is set to a 1, it clears the Surface Designation Error (SURF DE) flag.

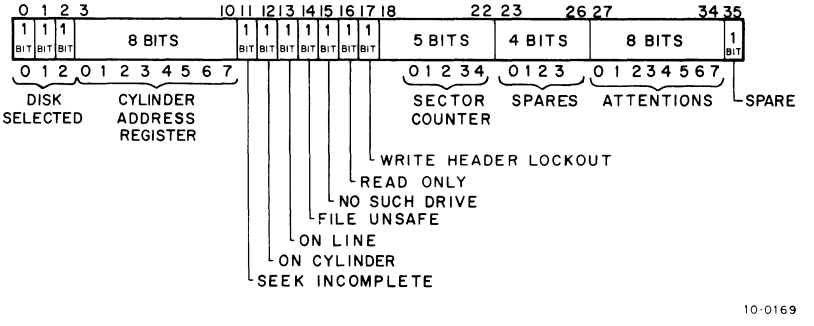


Figure 3-13 DATAI Instruction Word Format (Revised)

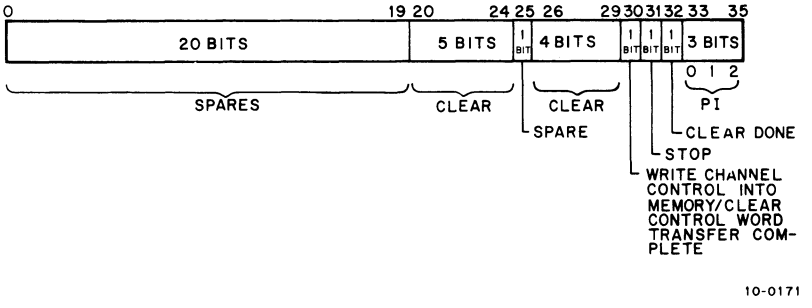


Figure 3-14 CONO Instruction Word Format

b. Write Channel Control Word into Memory: This bit causes the data channel to store the current contents of the data address register and the control word address register into memory location B + 1 where B (an even number) is the Initial Channel Control Word Address. The corresponding CONI bit signifies completion of the operation. Any channel termination causes the control word to be written, but CONI bit 30 will only be set when the operation was requested by the synchronizer via CONO. This bit, when it is set to a 1, clears the Control Word Transfer Complete (CWX COMP) flag. IOB 30

c. This bit stops transmission immediately. Part of last word and last sector transmitted is indeterminant. IOB 31

d. Clear: This bit clears the Done (DONE) flag. IOB32

e. PI 0, 1, 2: (PI Assignment) These bits assign a priority interrupt channel to the synchronizer. IOB 33-35

3.4.2.4 CONI Information – A CONI command is illustrated in Figure 3-15 and described in the following paragraphs:

a. *Channel Control Word Parity Error* – This bit indicates that the Channel Control Word contained a parity error. This error condition cannot be disabled. The error flag is cleared by a CONO with bit 24 set to a 1. IOB 14

b. *Disk Sector Parity Error* – This bit indicates that the checksum bits, at the end of a sector which has been read by the most recent read data command, do not yield a modulo-two sum of 1. Unless disabled, this error terminates data transmission. The error flag is cleared by a CONO with bit 24 set to a 1. IOB 15

c. *Channel Data Word Parity Error* – This bit indicates that the word read from memory during execution of the most recent write data or write header and data instruction contained incorrect parity. Unless disabled, this error terminates data transmission. If the instruction was write data, the remainder of the sector is filled with 0s and correct parity is added. If the instruction was write header and data, the results are indeterminate. IOB 16

d. *Disk Word Parity Error* – This bit indicates that the word read from the disk during execution of the most recent read data instruction contained incorrect parity. Unless disabled, this error terminates data transmission. IOB 17

e. *Search Complete* – This bit indicates that the search for the sector to be read or written has been completed. IOB 18

f. *End of Cylinder* – When this bit is set to 1, it indicates that the most recently executed read data, write data, or write header and data instruction attempted to transfer too much data and, as a result, incremented the head address register past the last surface on the disk. On the RP01, the register is incremented to 12_8. On the RP02, the register is incremented to 24_8. This bit is cleared by the next data transfer instruction to the same disk drive. IOB 19

g. *Power Supply Failure* – This bit indicates that the interface power supply voltages are out of tolerance. When this occurs, the interface terminates at the end of the current sector and turns on both the done bit and the power supply failure bit. The power supply failure bit cannot be cleared until the error condition has been corrected. IOB 20

h. *Search Error* – This bit indicates that the cylinder, surface, and sector fields of the most recently executed read data or write data instruction could not be matched (compared) with corresponding fields of any sector on the addressed track. This could occur because either *1)* there was a bad spot in the header field, *2)* the instruction contained the wrong fields, *3)* the program did not previously position the heads to the proper cylinder, *4)* the disk drive positioning mechanism is in need of adjustment, *5)* the PDP-10 System has failed, or *6)* a header was read incorrectly after search complete was set during a multiple sector transfer. IOB 21

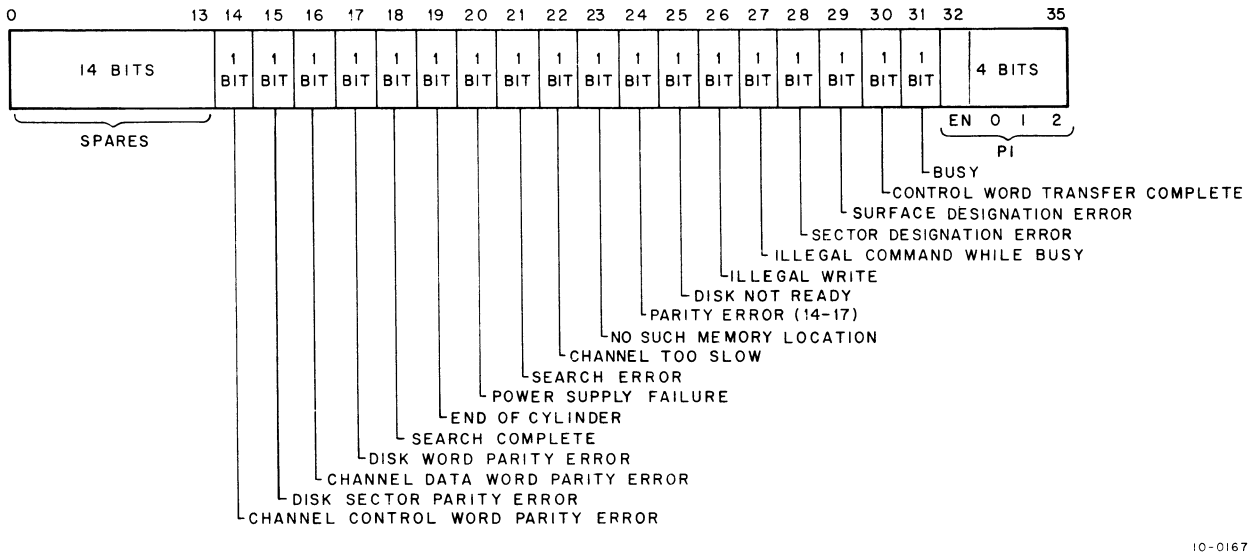


Figure 3-15 CONI Instruction Word Format (Revised)

i. *Channel Too Slow* – This bit indicates that the channel failed to respond to a request for a data word, or failed to accept a data word fast enough during a data transfer. If the instruction was a read data, data transmission is terminated. If the instruction was a write data, the remainder of the sector is filled with 0s and proper parity is added. If the instruction was a write header and data, the results are indeterminate. IOB 22

j. *No Such Memory Location* – This bit indicates that the channel attempted to access a nonexistent memory location. IOB 23

k. *Parity Error (14-17)* – This bit (24) is true when any one of bits 14 through 17 are true. Clearing this bit clears bits 14 through 17. IOB 24

l. *Disk Not Ready* – IOB 25

m. *Illegal Write* – This bit indicates that a write header and data or write data instruction was received which addressed a disk drive whose READ-WRITE/READ ONLY switch was in the READ ONLY position, or a WRITE was in process when sector pulse was received. IOB 26

n. *Illegal Command While Busy* – A DATAO to the RP10 was issued while BUSY flag was on. The second command is ignored. IOB 27

o. *Sector Designation Error* – This bit indicates that the sector addressed by the most recent read data or write data instruction does not exist (greater than 04_8 on the RP01 and greater than 11_8 on the RP02). IOB 28

p. *Surface Designation Error* – This bit indicates that the surface addressed by the most recent read data, write data, or write header and data instruction does not exist (greater than 11_8 on the RP01 and greater than 23_8 on the RP02). IOB 29

q. *Control Word Transfer Complete* – This bit indicates that the channel control word was written into memory only when that request was made by the synchronizer via CONO. IOB 30

r. *Busy* – This bit indicates that the synchronizer is currently executing a data transfer command. IOB 31

s. *PI Enable* – This bit indicates that the PI condition has been enabled. It is the result of (DONE ∨ ATTENTIONS)∧~ BUSY. IOB 32

t. *PI 0, 1, 2* – (PI Assignment) These bits indicate the priority interrupt channel currently assigned to the RP10. IOB 33-35

Chapter 4
Theory of Operation

4.1 GENERAL

This chapter discusses the principles of operation of the RP10 Disk Pack Synchronizer. A general block diagram discussion, a brief sequence of operation, and functional descriptions of the various operational circuits used in the synchronizer are also included.

4.2 GENERAL BLOCK DIAGRAM DISCUSSION

The RP10 Disk Pack Synchronizer is shown in general block diagram form in Figure 4-1. The RP10 acts as an intermediary between the I/O Bus, the DF10 Data Channel, and the RP01, or RP02 Disk Pack Drive. For purposes of this discussion, a knowledge of the PDP-10 I/O Bus, the DF10 timing diagrams, and the operation of the RP01/02 Disk Pack Drives is assumed.

The PDP-10 Processor communicates with the RP10 Disk Pack Synchronizer via four basic I/O instructions; *1)* Conditions Out (CONO) which transmits the control word to the RP10 control register thereby specifying the desired operation, *2)* Conditions In (CONI) which transmits the contents of the RP10 control and/or status register to the processor, *3)* Data Out (DATAO) which transmits processor data to the RP10 data register, and *4)* Data In (DATAI) which transmits the contents of the RP10 status and drive address registers to the processor.

The RP10 communicates with the RP01 or RP02 Disk Pack via the 35 lines shown in Figure 4-1. There are eight address and control lines; three tag lines; and one line each for sequence out, unit select, controlled ground, and write data. These lines carry information from the synchronizer to the disk. The disk communicates with the synchronizer over eight cylinder address lines; and one line each for attention, unit selected, ready, on-line, index pulse, sector pulse, file unsafe, seek incomplete, end-of-cylinder, read data coax, heads extended, and read only.

In the PDP-10 System, several RP10 Disk Pack Synchronizers can be attached to one data channel. As shown in Figure 4-2, the RP10 will gate nothing onto the channel bus until it receives the CHANNEL BUSY signal from the data channel. While inactive, the RP10 relays CHANNEL BUSY, CHANNEL START, and SAWRITE in the appropriate directions on the channel bus. On receipt of ~CHANNEL BUSY, it asserts its own CHANNEL START and SAWRITE, and becomes active.

4.3 SEQUENCE OF OPERATION

In these discussions, reference is made to the flow charts and logic diagrams listed in Chapter 6 and contained in Volume 2 of this manual. These are general descriptions intended to clarify some of the more obscure points in the diagrams. They do not trace each signal on a gate-by-gate basis.

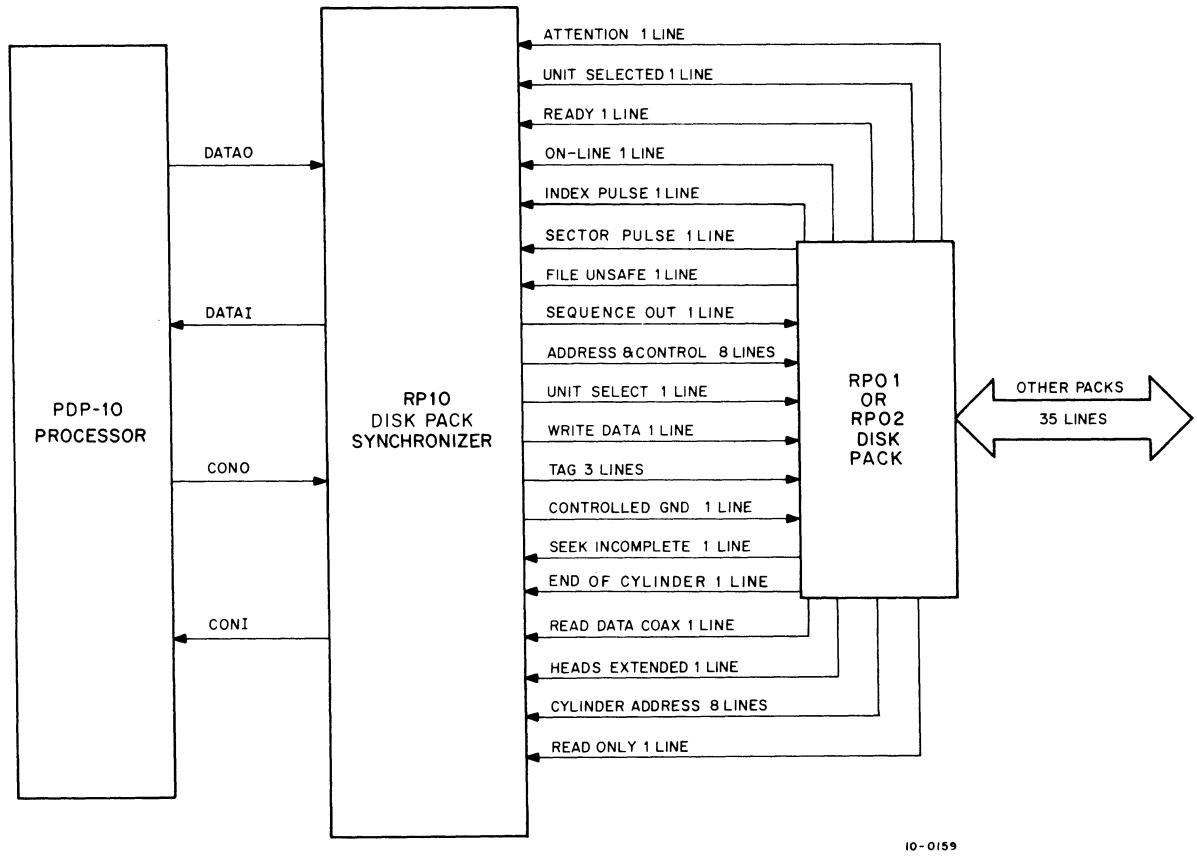


Figure 4-1 RP10 General Block Diagram

The RP10 receives commands (instructions) via DATAO 250 (254 for a second RP10 in a PDP-10 System). The Flow Chart FCS (Start) describes the receipt and decoding of instructions. Note that IBC INITIAL CLEAR does not clear SR or SR BUF registers. If the command is a No Op or Clear Attentions, execution is completed. If it is a Restore (recalibrate), or Seek, the RP10 exits through S2 to execute the command. If the command received is a Data Transfer, the RP10 exits through S5 to clear and set the head register in the drive, and through S4 to start the data channel. When the RP10 receives control of the data channel, it exits from FCCC through CC2 to begin data transfer.

4.3.1 Write Data or Read Data

If the command is Write Data or Read Data, DTC SEARCH is set and the RP10 begins searching for the sector addressed by the DAR CYL, DAR SURF, and DAR SEC registers. The 10-μs delay DTC SECTOR DLY allows the drive's head register to be incremented in a multiple track operation before setting DTC READ REFUSE. (The term REFUSE denotes useless information and not the act of rejection.)

DTC READ HEADER is set by the first 1-bit read off the disk after the 350-μs delay for DTC SEARCH SYNC times out. The delay is included so that DTC READ HEADER cannot be set by a 1 which might be read before the READ DATA SEPARATOR is in sync. When DTC READ HEADER is set, the next 36 bits are read into the LPR register. These bits and the 37th are exclusive ORed into the DTC PARITY flop. When the DTC PAR CON flop turns off, a 600-ns delay is fired that allows time for the LPR to shift the last character in, and for all signals to settle.

When DTC SRCH COMP STROB times out, the state of the DTC PARITY flop and the HCDE HEADER COMPARE signals are sampled. If they are correct, they set DTC SEARCH COMP and clear DTC SEARCH. HCDE HEADER COMPARE is true when the contents of the low-order 18 bits of the LPR match the contents of DAR CYL, DAR SURF, and DAR SEC registers. On a multiple sector read or write, the RP10 checks the cylinder and the parity bits, but does not check sector and surface bits.

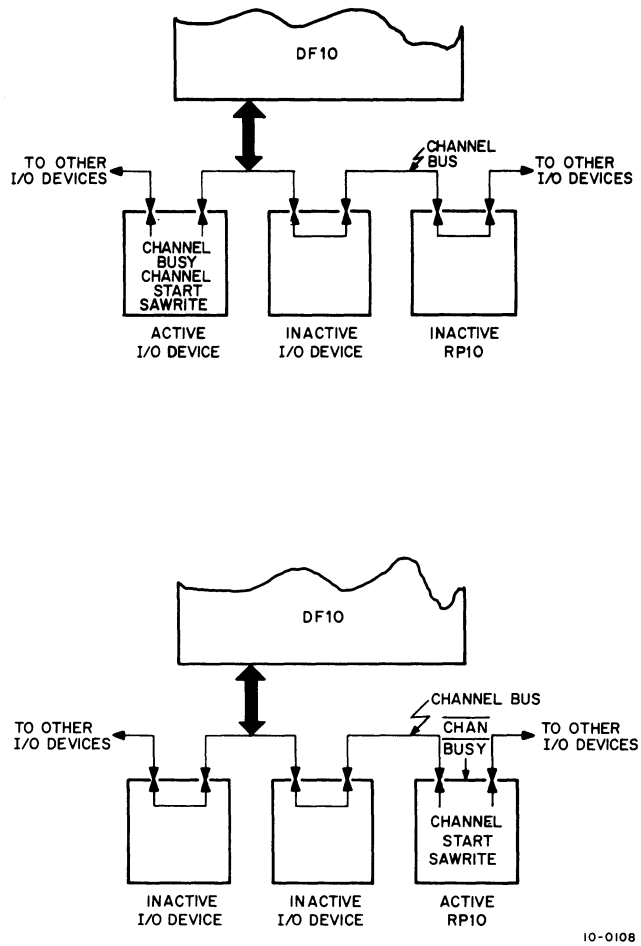


Figure 4-2 RP10 Active and Inactive Functions

If the operation is write data, the RP10 exits from FCSC to FCRW. The 3-μs delay prevents the write current from destroying the last few bits of the header. Four 36-bit words (consisting of 0s) are then written without parity. Following this, the DTC PAR CONT flop is set and a 1 is written as a trigger for subsequent read operations. This field is written during every write to ensure that the Read Data Separator is lined up with data. A lack of alignment can occur for two reasons; *1)* the gap is discontinuous, and therefore the signal is unpredictable, or *2)* the speed of the drive on which the header was written differs from that of the drive on which data was written.

After DTC WRITE DATA is set, the RP10 exits to the FCM2 subroutine to write the data. It returns when the 128-word word counter overflows and the WDC WORD COUNT EQ 00 becomes true. At this time, DTC WRITE LPR is set and DTC WRITE DATA is cleared. The RP10 again exits to the FCM2 subroutine to write the contents of the LPR on the disk twice. The second LPR is written as guard bits to ensure that the last bits of the LPR are not destroyed when write current is removed. The DTC SET WRITE is then cleared and the tunnel erase heads must be turned off after write is removed or FILE UNSAFE will occur. The tunnel erase is used to narrow the width of the data track as written by the read/write poles. This prevents crosstalk between tracks. At this point, DTC GAP is set. If the channel has terminated during the write operation, or if there has been an OVERRUN, or CHAN DATA PE, the operation is shut down. Otherwise, the RP10 waits for the next DSBC SEL UNIT SEC PLS and continues on FCSC.

If the operation is read data, the RP10 exits through SC2. The Read Data Separator is enabled by DTC BETA GAP, during which it resyncs in preparation for a read data operation. DTC BETA GAP is cleared in 44 μs for an RP02 or in 88 μs for an RP01. At that time, if DTC SEARCH COMP is cleared, it is an indication that the RP10 has not completed its seek operation. At this time, DTC READ GAP, which was set by the trailing edge of DTC SRCH COMP STROBE, is cleared and the RP10 waits for the next DSBC SEL UNIT SEC PLS to try again. If DTC SEARCH COMP has been set by DTC SRCH COMP STROBE, however, the RP10 waits for the first 1-bit from the disk, which signals the start of the data area. When the first 1-bit is received, DTC READ DATA is set, clearing DTC READ GAP and the RP10 exits from FCRW to FCM1 subroutine. It returns when 128 words have been read, and the WDC WORD COUNT register overflows to 0. DTC READ LPR is then set, and DTC READ DATA is cleared.

After reading one more word, sector parity is checked. If any bit of the LPR register is zero, CXR DISK SEC PE is set. In either case, DTC GAP is set, and the RP10 waits for the next DSBC SEL UNIT SEC PLS and then continues on FCSC.

4.3.2 Write Headers and Data (Format)

If the command is write headers and data (Format), the RP10 exits from FCSC to FCWH where it waits, first for a DSBC SEL INDEX pulse and then for a DSBC SELECTED SECTOR. After a delay, it sets DTC WRITE HEADER, and exits to the FCM2 subroutine to write 36 words (24 in RP01) without parity. The RP10 then exits to FCRW, sets DTC WRITE DATA, clears DTC WRITE HEADER, and returns to FCM2 to write 128 words with parity. When the WDC WORD COUNT register overflows to zero, the RP10 returns to FCWH, sets DTC WRITE LPR, clears DTC WRITE DATA, and exits to FCM2 to write the LPR on the disk twice.

NOTE

The second writing of the contents of the LPR is a convenient way to write guard bits.

After the second LPR is written, the RP10 returns to FCWH, clears DTC WRITE LPR, keeps the erase heads turned on for 20 μs, sets DTC GAP and waits for the next DSBC SELECTED SECTOR.

4.3.3 Local/Remote

Local and Remote mode operation are straightforward and can be followed directly on FCL. Major differences in the two modes are listed below:

a. Local Mode

(1) The DAR CYL register is tied to the CYLINDER switches.

(2) CC ACTIVE BUF is held off so that the data channel is not started.

(3) The AR is loaded from the DATA switches rather than from the AR CHND00-35 Channel Data Lines.

(4) The Initial Control Word Address is not loaded.

(5) The RP10 is logically disconnected from the PDP-10 I/O bus (it will not respond to its device code and will not set its DONE and PI Enable signals).

(6) IBC SET DAR ETC does not fire, therefore, the status registers are not set by information present on the I/O bus.

b. Remote Mode

(1) DTC FINISH clears IBC BUSY, sets IBC DONE, and interrupts the PDP-10 on the assigned PI Channel; whereas in Local Mode, DTC FINISH clears IBC BUSY and, if the SWP STOP switch is not depressed, the entire operation is repeated after a 100-μs delay.

4.4 RP10 RECORDING TECHNIQUE

Disk pack systems are susceptible to a phenomenon termed "pulse crowding." This phenomenon can occur when a series of 1s are recorded on a track. As the pulse density increases, the location of the recorded 1s crowd each other with the result that they may actually reside either ahead of, or in back of, the location in which they were recorded. The resultant locations can shift in either direction; consequently, a means is provided in the RP10 to read through a precisely-timed "window", enabling original timing to be recovered.

The RP10 uses a double-frequency, nonreturn-to-zero (NRZ) recording technique. A 5-MHz clock signal is divided to produce two 2.5-MHz signals with a 180 degree phase relationship (see DWG RP10-0-RDS). When writing, the leading 2.5-MHz signal continuously records 1 bits on the disk surface, while the trailing signal samples the data to produce data bits. If the data to be written is continuous 0s, a 2.5-MHz signal is recorded on the disk surface. If the data to be written is continuous 1s, then a 5.0-MHz signal is recorded. Therefore, for any given data cell, the recorded frequency is either 5 MHz for a 1 data bit, or 2.5 MHz for a 0 data bit.

To recover data recorded in this manner, the 0s rate frequency component must be removed, which is done by using a phase-locked oscillator (RDS) similar to a sample-and-hold circuit. The RDS samples the 0s rate pattern in the preamble of each record, phase-locking on this pattern, and then maintains phase through the record, making only minor corrections with the use of the 0s rate component of each data cell. The RDS then removes the 0s rate component with which it is familiar, leaving only the recovered data.

The 0s rate component (2.5 MHz for RP02 or 1.25 MHz for RP01) removed from the raw data stored on the disk is also used. This signal is the main source of timing in the RP10 Synchronizer. The RP01/02 has no clock track; this system provides self-clocking.

4.5 RP01/02 ADDRESSING METHOD

The RP01/02 Disk Pack consists of six (or eleven respectively) evenly-spaced recording platters mounted on a single shaft. The top- and bottom-most surfaces are not used for recording; instead, the bottom surface has a metal disk attached to it. The disk contains twenty evenly-spaced notches with an additional notch termed the Index.

A circuit that is designed to detect these notches, also divides the pulses they produce into either five or ten equal sectors. These sectors are addressed by a five-bit register which is part of the Data Address Register (see DWG RP10-0-DAR). The sector addresses are coded 00_8 through 04_8 when using an RP01 drive, and 00_8 through 11_8 when using an RP02 drive. All other codes are illegal and, if given, result in the appropriate interrupts.

A separate read/write head is provided for each of the inner recording surfaces. These heads are mounted in parallel and in vertical alignment to each other and are attached to a common head tower. The heads are selected by an additional five-bit register in the Data Address Register designated DAR SURF00-04. Head addresses are coded 00_8 through 11_8 for the RP01 drives, and 00_8 through 23_8 for RP02 drives. All other codes are illegal and, if given, result in the appropriate interrupts.

The position of all heads, vertically aligned with respect to the vertical axis that passes through the center of all surfaces, is called a cylinder. Head positioning is controlled by a linear positioning motor and detenting mechanism that is designed to stop the heads at any one of 203 different cylinder locations. These cylinders are coded 00_8 through 312_8 from the outer-most cylinder to the inner-most cylinder, respectively. Cylinders are addressed by an eight-bit register called DAR CYL01-128 in the Data Address Register.

The intersection of a cylinder, head, and sector address defines a unique sector that is the smallest addressable unit in the system. Each sector has a header word that uniquely defines that sector.

4.6 RP10 REGISTER ORGANIZATION

The register organization of the RP10 is given in Figure 4-3. The various signals which control the flow of data originate in the Data Transfer Control (DTC). Serial information from or to the disk is assembled or dispersed by the six-bit Shift Register. The data is then processed in parallel, through the Shift Register Buffer, and is transferred to or from the Assembly Register and Longitudinal Parity Register in six-bit bytes.

In read mode, DTC READ BIT translates information bit-by-bit as it is read from the disk. Each bit enters the shift register at SR5 and is shifted through the register by DTC SHIFT SR. When the register is filled, DTC LD BUFFER FM SR transfers the six-bit byte to the SR BUF where it loads AR30-35 at a DTC SHIFT AR time. It also exclusive ORs the byte into LPR 30-35 by DTC LOAD LPR. Subsequent bytes are then assembled by DTC SHIFT AR, DTC LOAD LPR, and DTC SHIFT LPR. At the end of six byte transfers, the AR contains the word read, and the LPR contains the parity for that word.

In write mode, the first six bits of a 36-bit word, which has been previously assembled in the AR, is loaded by a 1s transfer into the SR by DTC LD SR FM AR and into SR BUF by DTC LD BUFFER FM AR. While these six bits are being serially transferred to the disk by DTC SHIFT SR, they are also exclusive ORed into LPR30-35 by DTC LOAD LPR. At the end of the six transfers, the contents of the AR are written on the disk, and the LPR contains the parity for that word. Thus, the SR must be cleared before loading. It is cleared by WRITE ENABLE, which feeds 0s into the SR during each shift. Only five shifts are used during a write; therefore, the state of SR0 is indeterminate during a load from the AR, and it is jam transferrred.

When DTC LD SR FM LPR is issued, the contents of the LPR are written on the disk through the Shift Register by DTC SHIFT SR.

4.7 RP10 REGISTERS

4.7.1 Assembly Register

The RP10 Assembly Register is shown in Figure 4-4 and in DWG RP10-0-AR. The register is arranged in groups of six flops, each group individually feeding the next lower-order group of six. Input is at AR30-35 by ARD30-35 H or ~ARD30-35 H ANDed with DTC SHIFT AR H. Each flop can also be set by its individual panel switch (SWP DATA SW00-35 H) if ANDed with ~IBC LOAD TEST H. The setting of each flop, when ANDed with CC DATA STROBE L, results in the AR CHND XX L version of that bit. When AR CHND XX L is ANDed with DTC DATA RCVR EN L, it direct sets the flop from which it originated.

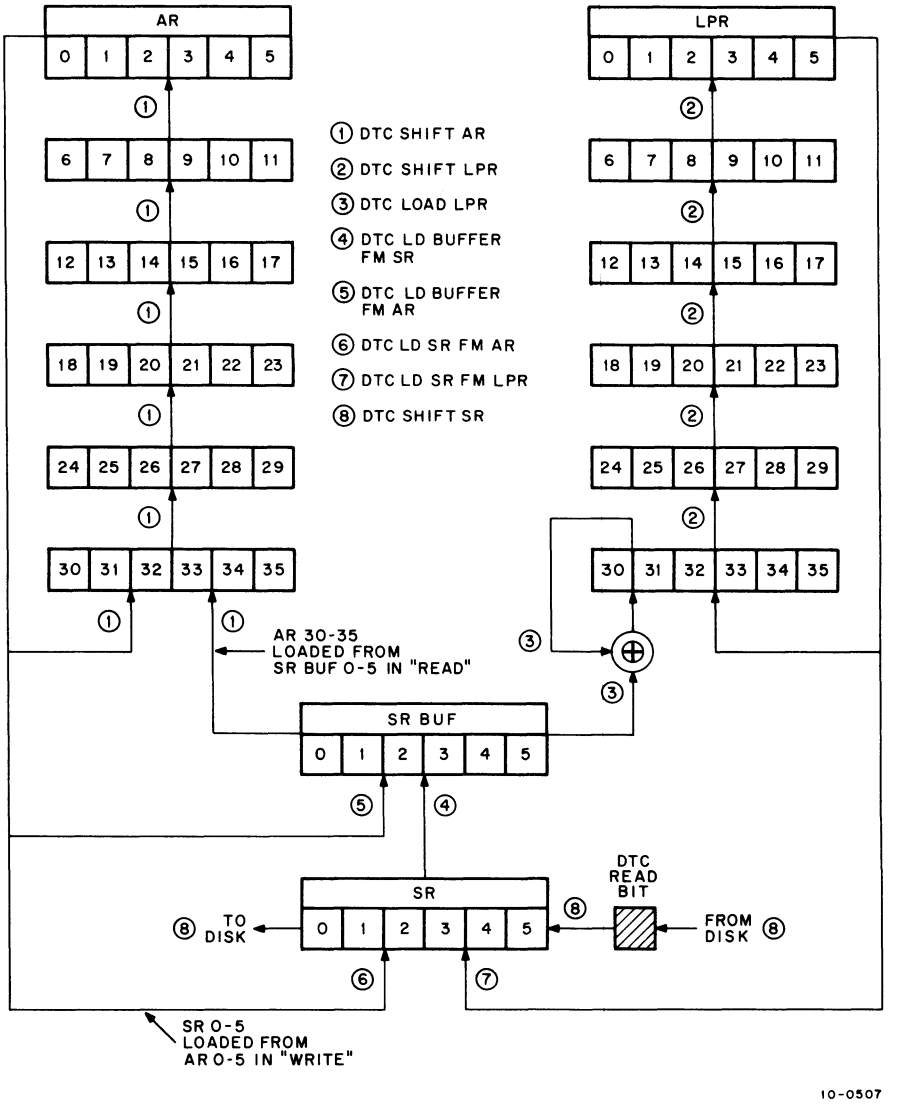


Figure 4-3 RP10 Register Organization

4.7.2 Assembly Register Data Gate

The RP10 Assembly Register Data Gate is shown in Figure 4-5 and DWG RP10-0-ARD. The data gate connects the Assembly Register output and the Shift Register Buffer, and functions as an input switcher for the AR. The register consists of four sets of six AND gates and two sets of six OR gates. One set of OR gates feeds the set inputs of AR30-35 with ARD30-35 H. The other set of OR gates feeds ~ARD30-35 to the AR reset inputs.

Input to the AR Data Gate is either from the Shift Register Buffer (SR BUF0-5) or the output of the Assembly Register (AR00-05). Inputs from the AR are enabled by the write condition (DTC WRITE ENABLE L) while inputs from the Shift Register Buffer are enabled by the read condition (DTC READ ENABLE L).

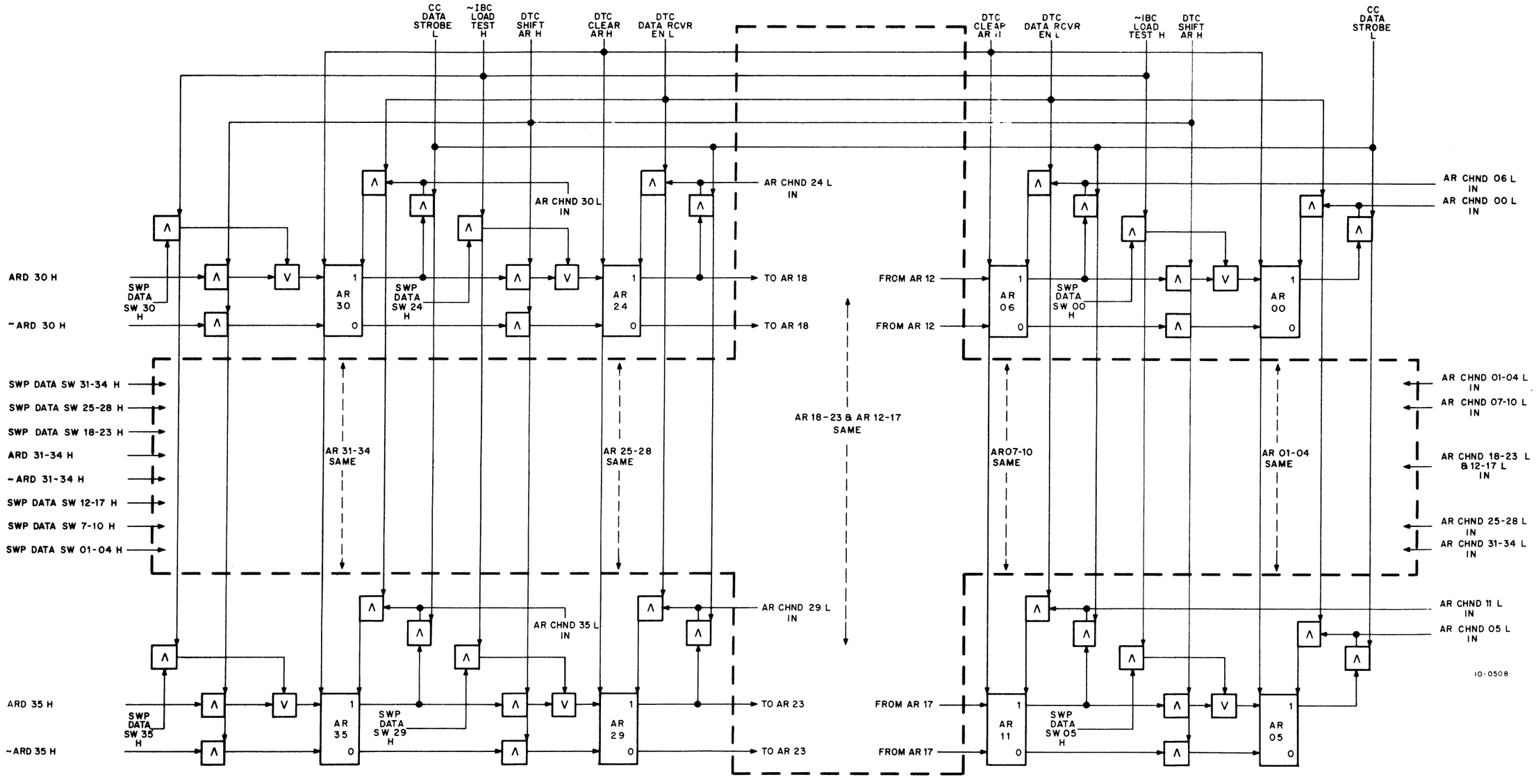


Figure 4-4 RP10 Assembly Register Simplified Block Diagram

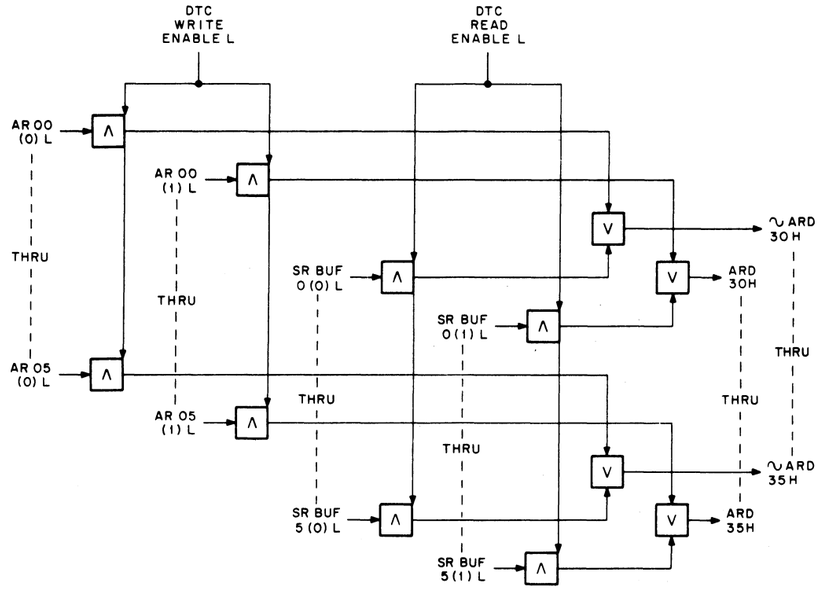


Figure 4-5 RP10 Assembly Register Data Gate,
Simplified Block Diagram

4.7.3 Condition Register

The RP10 Condition Register is shown in Figure 4-6 and in DWG RP10-0-CXR. This register monitors various conditions in the controller, raises indications when these conditions are in error, and provides a means of clearing the conditions or controlling them remotely. In the condition register, all flops are cleared by IBC INITIAL CLEAR except the three error stop disabling flops (DSPE, CDPE, DWPE), which are cleared by IBC GEN CLR (1) H, and the three priority interrupt flops (PI0-2), which are cleared by IBC CON CLR H.

During a CONO command, the CXR PI0-2 flops are conditioned by the state of IOBD 33-35 H ANDed with IBC CONSET H. When the outputs of PI0-2 are decoded, they determine the priority interrupt channel assigned to the RP10 (CXR IOB PI1-7 H). During a CONI command, the priority interrupt channel currently assigned is indicated. The decoder is enabled by CXR PI ENABLE H, which is the combination of either IBC DONE (1) H or any DTC ATTN0-7 (1) H ANDed with IBC BUSY (0) L and IBC LOCAL (0) L. IOBD 35 H, when set during a Read Data instruction and ANDed with IBC SET DAR ETC A, H, sets CXR WRITE EVEN PAR flop. This flop causes the channel to write even parity into memory on all data words read from the disk.

The output CXR PARITY ER L is the OR of CXR CHAN DATA PE(1) H, CXR CHAN CONT PE(1) H, and CXR DISK SEC PE(1) H. The disk sector parity error flop is set by CXR SEC PARITY ERROR H 600 ns after DTC READ LPR goes false, thus indicating that the checksum bits at the end of a sector (which has been read by the most recent Read Data command) do not yield a modulo-two sum of 1.

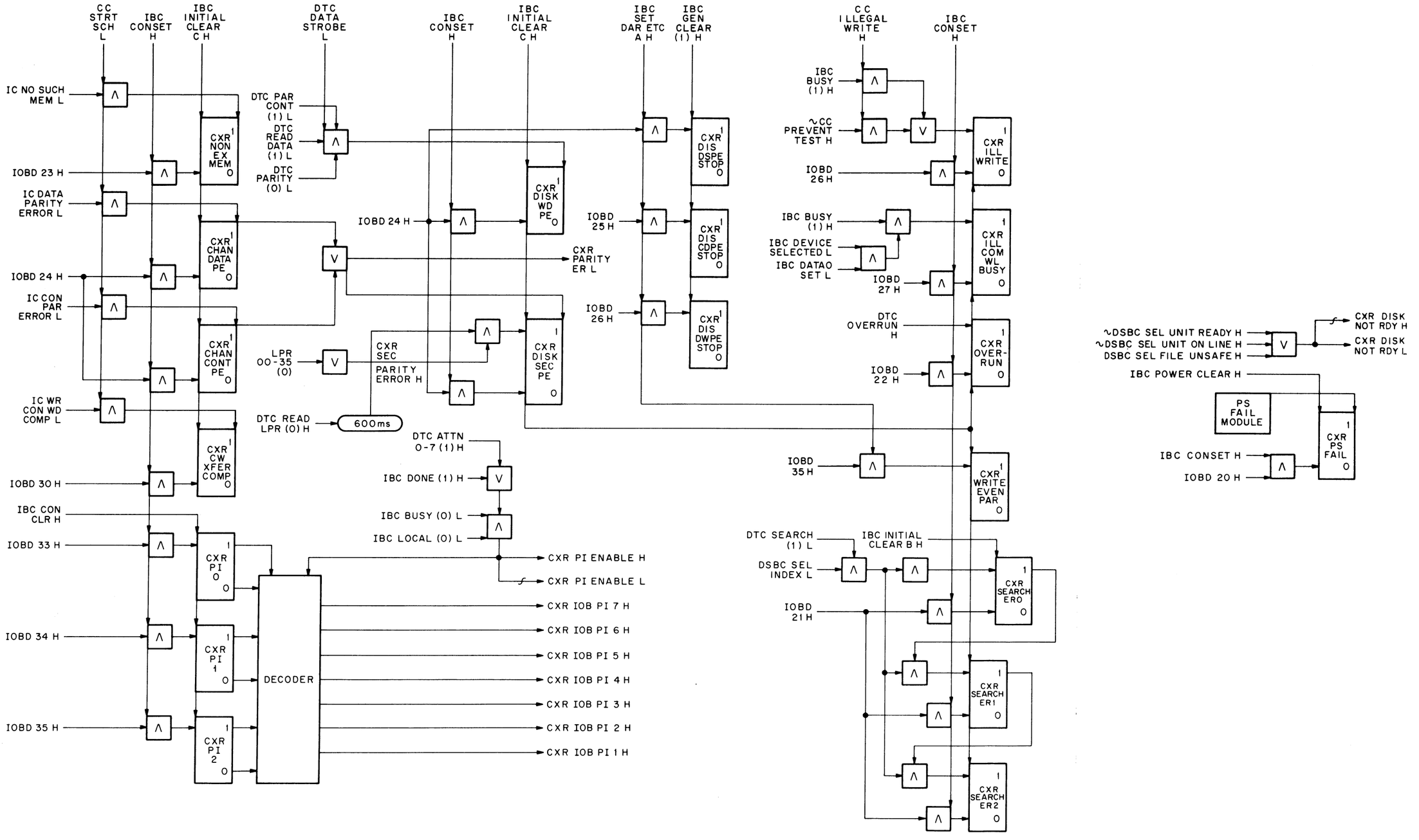


Figure 4-6 RP10 Condition Register, Block Diagram

The channel control parity error flop is direct set by IC CON PAR ERROR L and CC STRTSCH L. It is cleared during a CONO by IOBD 24 H, which also clears the channel data parity error flop.

The CXR CHAN DATA PE flop is direct set when IC DATA PARITY ERROR L is ANDed with CC STRTSCH H. IC DATA PARITY ERROR L is true during a CONI when either Channel Data Word Parity Error, Channel Control Word Parity Error, Disk Word Parity Error, or Disk Sector Parity Error are true. The flop is cleared during a CONO by the combination of IBC CONSET H and IOBD 24 H, which, in turn, clears the parity error conditions (IOBD 14-17 of that same word). The CXR DISK WD PE flop is cleared when IOBD 24 H is true and is direct set on a DTC DATA STROBE L by ANDing DTC PAR CONT(1) L with DTC READ DATA (1) L and DTC PARITY (0) L.

The CXR NON EX MEM flop is direct set by IC NO SUCH MEM and CC STRTSCH L. During a CONI, this flop indicates that the channel attempted to access a nonexistent memory location. During a CONO, the flop is reset by the combination of IOBD 23 H and IBC CONSET H.

The CXR CW XFER COMP flop is direct set by IC WR CON WD COMPL. This condition causes the channel to store the current contents of the data address register and the control word address register in memory location B + 1, where B (an even number) is the Initial Channel Control Word Address. The corresponding CONI bit, IOBD 30, indicates that the operation is complete. Any channel termination causes the control word to be written, but CONI bit 30 is only set when the operation was requested during a CONO.

The Search Error flops (CXR SEARCH ER0-2) count DSBC SEL INDEX L pulses from the disk presently in search mode (DTC SEARCH (1) L). During a CONI, they indicate that the cylinder, surface, and sector fields of the most recently executed read data or write data instruction could not be compared with corresponding fields of any sector on the addressed track. If SRCH COMP was set and a header (other than the first header in a multiple sector operation) was read incorrectly, bit 2 will be set. If IOBD 21 H is set during a CONO, it is ANDed with IBC CONSET H to reset all three flops, thereby clearing the SRCH flag.

There are three flops that can be set during a DATAO instruction to disable certain parity error stops to data transmission. IOBD 24 H, when set during a Read Data instruction, is ANDed with IBC SET DAR ETC A H to set CXR DIS DSPE STOP. Under this condition, a longitudinal parity error sets the longitudinal parity error bit, but will not terminate data transmission. When IOBD 25 H is set during a Write Data instruction or a Write Header and Data instruction, it prevents a channel data word parity error from stopping transmission. IOBD 25 H is ANDed with IBC SET DAR ETC A H to set the CXR DIS CDPE STOP flop. If IOBD 26 H is set during a Read Data instruction, it will disable the disk word parity error stop in a similar manner by setting the CXR DIS DWPE STOP flop.

The CXR ILLEGAL WRITE flop is set by CC ILLEGAL WRITE L when either IBC BUSY is true or CC PREVENT TEST is false. During a CONI, this indicates that a Write Header and Data or Write Data instruction addressed a disk drive whose READ-WRITE/READ ONLY switch was in the READ ONLY position, or it indicates that a write operation was in process when a sector pulse was received. This flop can be reset during a CONO by setting IOBD 26 H at IBC CONSET H time, thereby clearing the ILL WR flag.

The CXR ILL COM WL BUSY flop is set during IBC DATAO SET L by IBC DEVICE SELECTED L and IBC BUSY (1) H, thus indicating that a DATAO was issued while the BUSY flag was up. This causes the second command to be ignored. It is reset during a CONO (IBC CONSET H) by IOBD 27 H, which clears the ILL COM flag.

CXR OVERRUN is set by DTC OVERRUN H to indicate, during a CONI, that the channel failed to respond to a request for a data word, or failed to accept a data word fast enough during a data transfer. During a CONO, IOBD 22 H ANDed with IBC CONSET H clears the OVERRUN flag by resetting this flop.

Whenever the interface power supply voltages are out of tolerance, the PS FAIL module will direct set the CXR PS FAIL flop and turn on DONE causing the transfer to terminate at the end of the current sector. This flop cannot be reset until power supply voltages are within tolerance. At that time, IOBD 20 H ANDed with IBC CONSET H clears the PS FAIL flop.

CXR DISK NOT RDY is an output of the condition register. This signal results from either DSBC FILE UNSAFE, ~DSBC SEL UNIT READY H, or ~DSBC SEL UNIT ON LINE H.

4.7.4 Data Address Register

The RP10 Data Address Register is shown in Figure 4-7 and in DWG RP10-0-DAR. This register defines the entire data address and consists of four sub-registers to describe the drive selected (3 bits), the cylinder desired (8 bits), the surface on which the data resides (5 bits), and the specific sector to be located (5 bits). The setting of the flops is effected either by switch panel controls which direct set the appropriate flops during local mode operation (IBC LOCAL (1) L), or by the individual states of IOBD bits 03-23 received during a DATAO and enabled by IBC SET DAR ETC A/B H. All flops are cleared by IBC INITIAL CLEAR A/B H.

4.7.5 Longitudinal Parity Register

The RP10 Longitudinal Parity Register is shown in simplified form in Figure 4-8 and in DWG RP10-0-LPR. Data from SR BUF00-05 is exclusive ORed and applied to LPR30-35 by DTC LOAD LPR H. On receipt of each DTC SHIFT LPR B or C, the contents of each column of flops are shifted to the next lower order set of six flops. LPR00-05 are tied back to LPR30-35 through AND/OR gating. All flops are cleared by DTC CLEAR LPR H.

4.7.6 Shift Register

The RP10 Shift Register is shown in simplified form in Figure 4-9 and in DWG RP10-0-SR. The circuit comprises a six-bit shift register interconnected to a six-bit shift register buffer. Input is at SR5.

SR BUF00-05 flops are all direct set by the OR of SR0-5 and AR00-05, each ANDed by its DTC enabling signal. The signals designated as SR0-5(L)L and SR BUF00-05(L) L feed individual lights on the indicator panel.

4.8 RP10 Control Circuits

4.8.1 Channel Control

The RP10 Channel Control is shown in DWG RP10-0-CC. The circuit serves as an interface with the DF10 Data Channel. In order for the RP10 to gain access to the data channel, it must transmit CHANNEL START to the channel and it must receive CHANNEL BUSY from the channel. If the synchronizer is not actively engaged with the data channel, it relays the CHANNEL START and CHANNEL BUSY to another I/O device and is prevented from generating its own CHANNEL START.

Either the RP10 or the DF10 can terminate operation. If the DF10 terminates operation, it removes CHANNEL BUSY, and the RP10 negates CHANNEL START. If the RP10 terminates operation, it removes CHANNEL START, and the DF10 negates CHANNEL BUSY. At this time, the RP10 inhibits the generation or relaying of CHANNEL START for 500 ns, a requirement imposed by the DF10.

In operation, the RP10 requests access by generating CHANNEL START and is answered by CHANNEL BUSY from the channel. This acknowledges that the RP10 has access. The RP10 then generates DEVICE PULSE, which transfers the ICWA to the channel where it is processed and evaluated. When this is completed, data transfer begins, the direction of which is determined by SAWRITE.

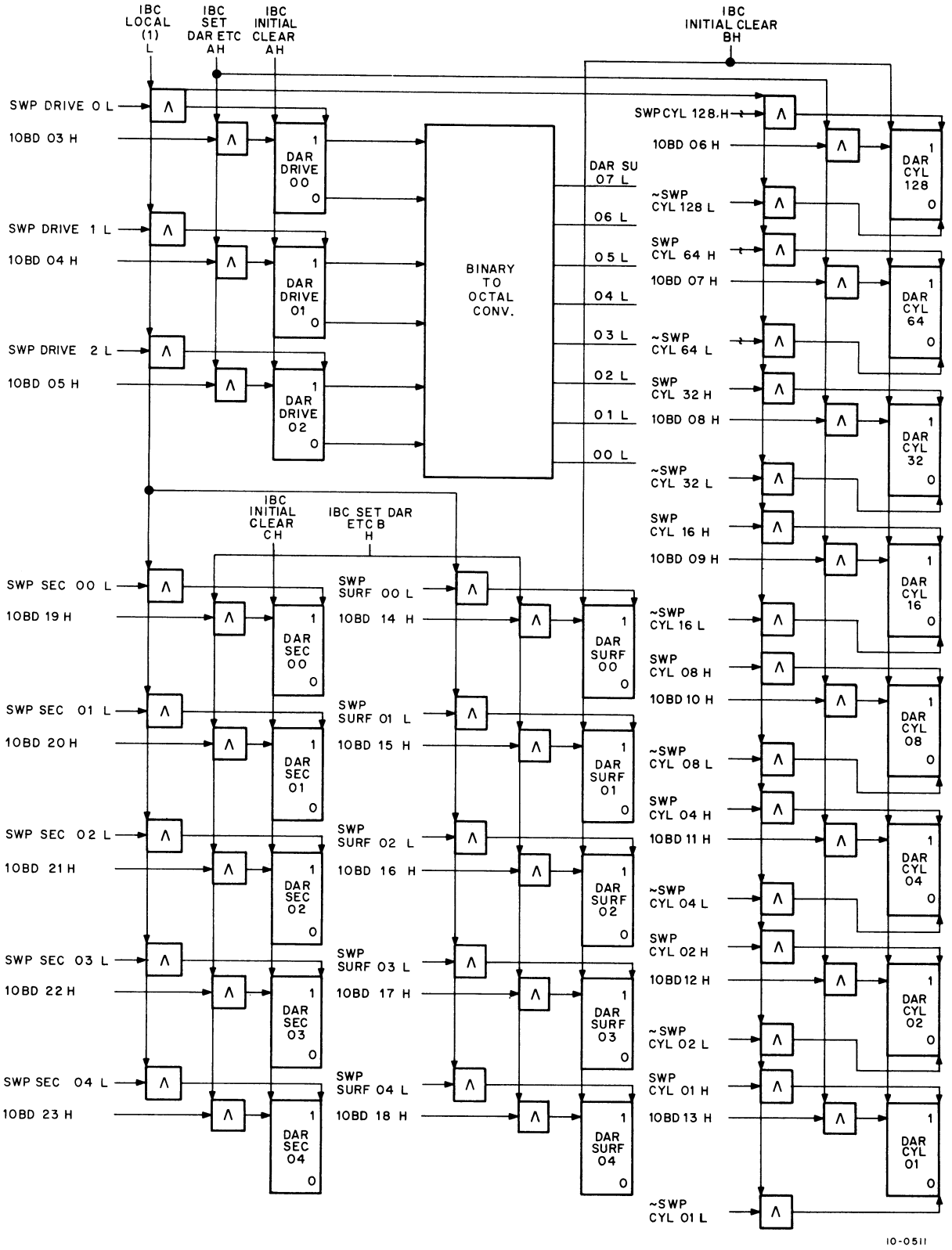


Figure 4-7 RP10 Data Address Register, Block Diagram (Revised)

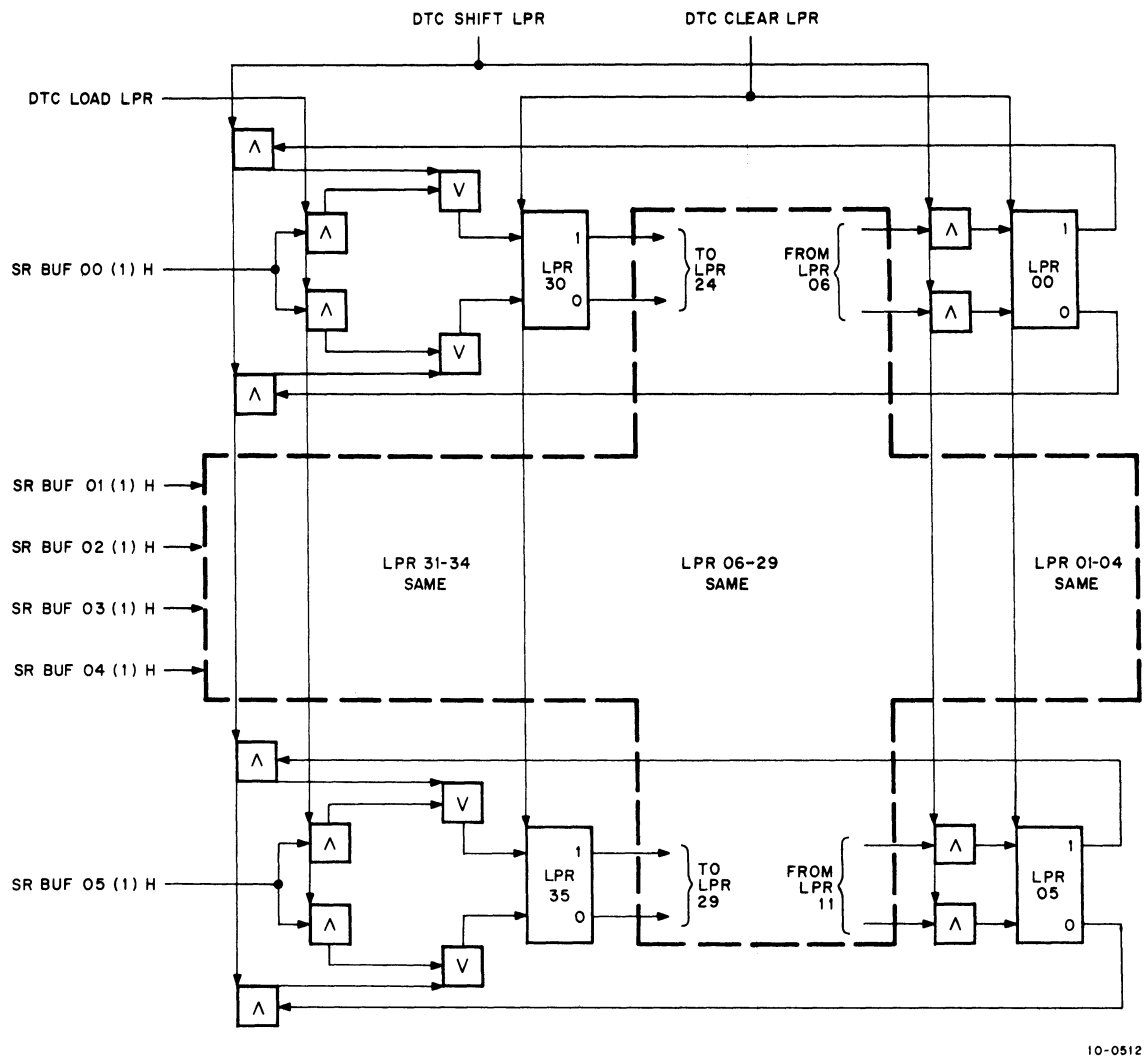


Figure 4-8 RP10 Longitudinal Parity Register, Block Diagram

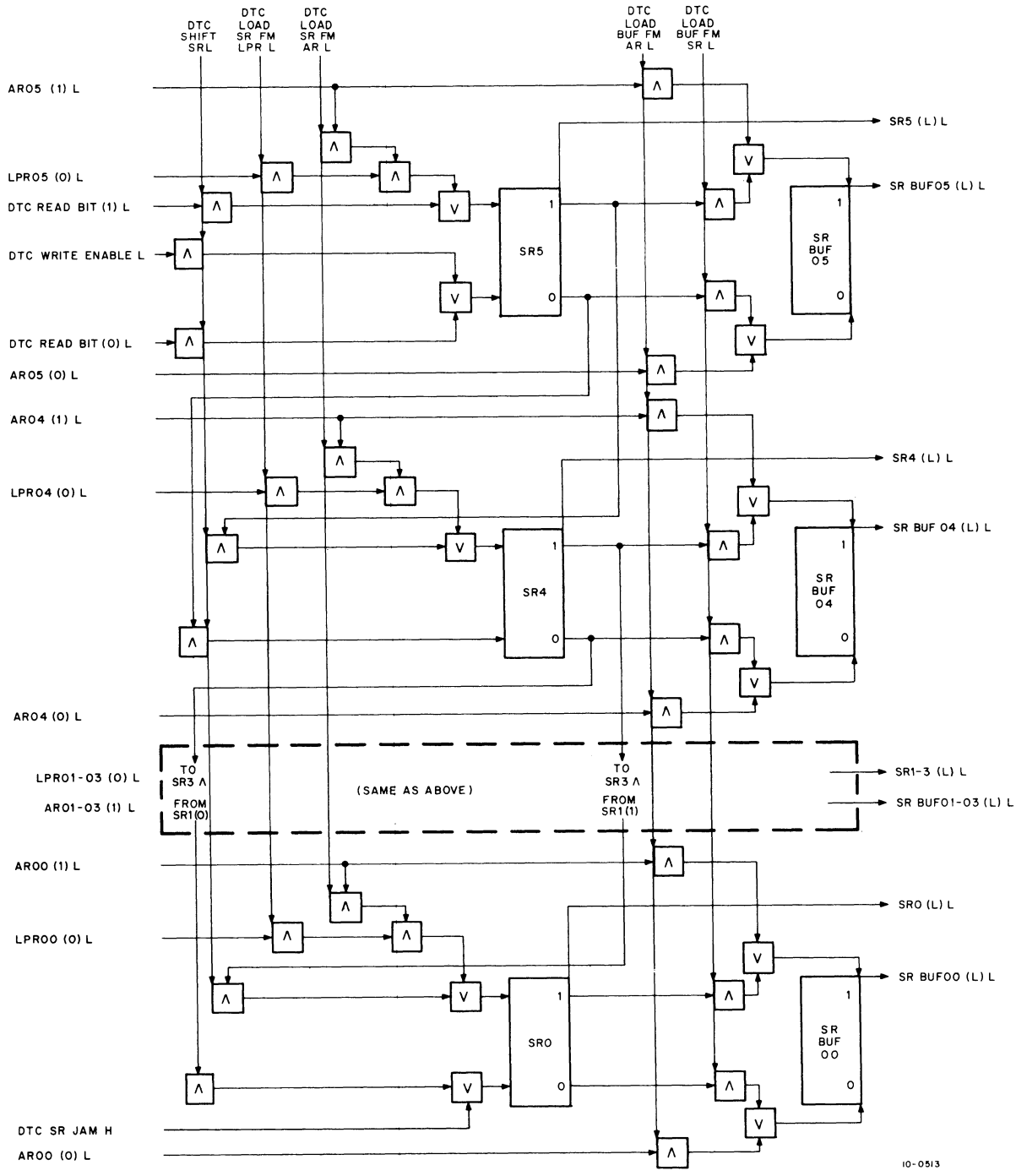


Figure 4-9 RP10 Shift Register, Block Diagram

Synchronization of transfers between the Data Channel and the RP10 is achieved by a CHANNEL PULSE issued by the channel and DEVICE PULSE generated by the RP10. Regardless of the direction of transfer, these pulses alternate on each word transferred and perform a bookkeeping function on that transfer.

When the channel has a word ready for transfer during a write, it issues a CHANNEL PULSE to the RP10 implying that it may take the word. When the RP10 has taken that word, it sends a DEVICE PULSE to the channel indicating that it is ready for the next word. When the next word is ready, the Data Channel issues another CHANNEL PULSE; when that word is transferred, the RP10 issues another DEVICE PULSE. This dialogue continues until the desired number of words have been transferred.

When the channel is ready to receive a word from the RP10 during a read, it issues a CHANNEL PULSE to the RP10 indicating its readiness. When the RP10 places the word on line, it sends a DEVICE PULSE to the channel indicating that it may take that word. When transfer is complete, the Data Channel issues another CHANNEL PULSE; when that word is on line, the RP10 issues another DEVICE PULSE. This dialogue continues until the desired number of words have been transferred.

The CHANNEL and DEVICE pulses alternate under normal operation; this fact is used as a bookkeeping arrangement on transfer. If any pulse occurs twice without the other, an error or overrun is indicated.

At termination, the data channel sets IDLE and removes the CHANNEL BUSY which results in the resetting of the CC ACTIVE flop in the RP10.

4.8.2 Data Transfer Control

The RP10 Data Transfer Control is shown in DWG RP10-0-DTC. This circuit functions as a traffic manager; it determines the mode of operation of the synchronizer and the direction in which information will flow between Disk and Processor.

As shown in Figure 4-10, the DTC OP CODE 00-02 flops are cleared by IBC INITIAL CLEAR A H. These OP CODE flops can be either set by IOBD00-02 H in combination with IBC SET DAR ETC B H, or direct set by SWP OP0-2 L when ANDed with IBC LOAD TEST C L. When the outputs are decoded, they result in one of various operation commands to the device.

4.8.2.1 Read Data – If DTC READ DATA COM H is decoded, it sets the DTC SEARCH flop if ANDed with CC STRTSCH H and enables the DTC READ GAP flop to be set after the header is read when triggered by the leading edge of ~DTC SRCH COMP STRB H (see Figure 4-11). Note that each flop pertains to a portion of the disk format.

a. When DTC SEARCH flop sets, it ANDs with DTC SEARCH SYNC H to set DTC READ REFUSE (DTC SEARCH SYNC is DTC SECTOR DLY H + 350 μs). When the READ REFUSE flop sets, it conditions the setting of DTC READ HEADER flop which is set on receipt of DTC READ CLOCK PULSE L if DTC READ BIT (1) L is present and if the READ HEADER flop is reset at that time.

b. When DTC READ GAP flop sets, it ANDs with DTC BETA GAP H (the OR of DTC SRCH COMP STROB H and either DTC RP01 H or DTC RP02 H) and DTC SET READ DATA H to set DTC READ DATA flop. The ORed delays (88 μs for RP01 and 44 μs for RP02) are adjusted for the relative gap widths at nominal rotating speeds for each disk type. When DTC SET RD/WR LPR H is present, DTC READ DATA (1) L sets DTC READ LPR flop when WDC WORD COUNT EQ 00 L is asserted, thereby signalling the end of data. When the LPR flop sets, it resets the DTC READ DATA flop.

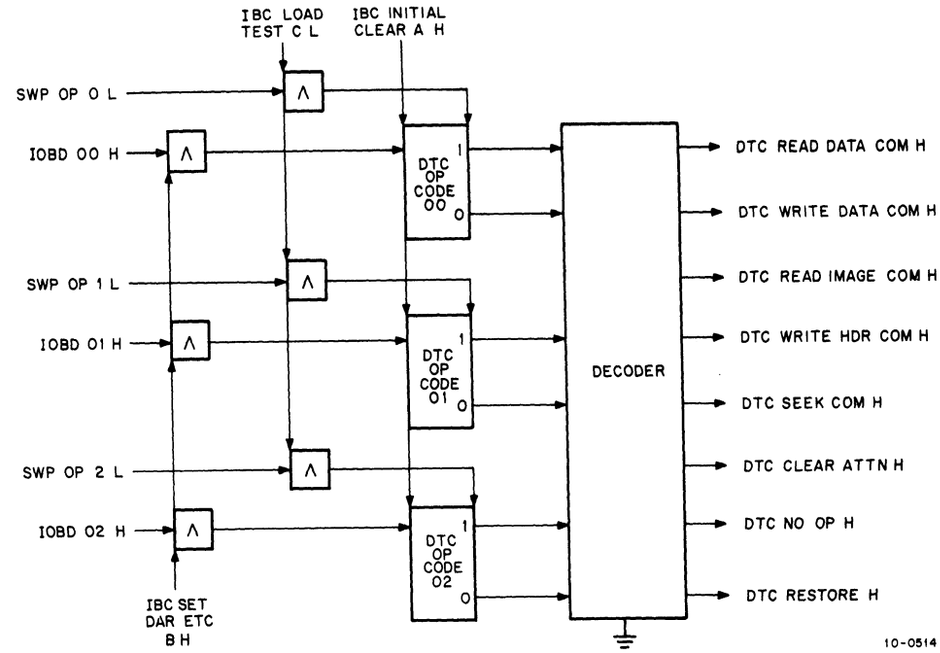


Figure 4-10 DTC OP Decoding, Block Diagram (Revised)

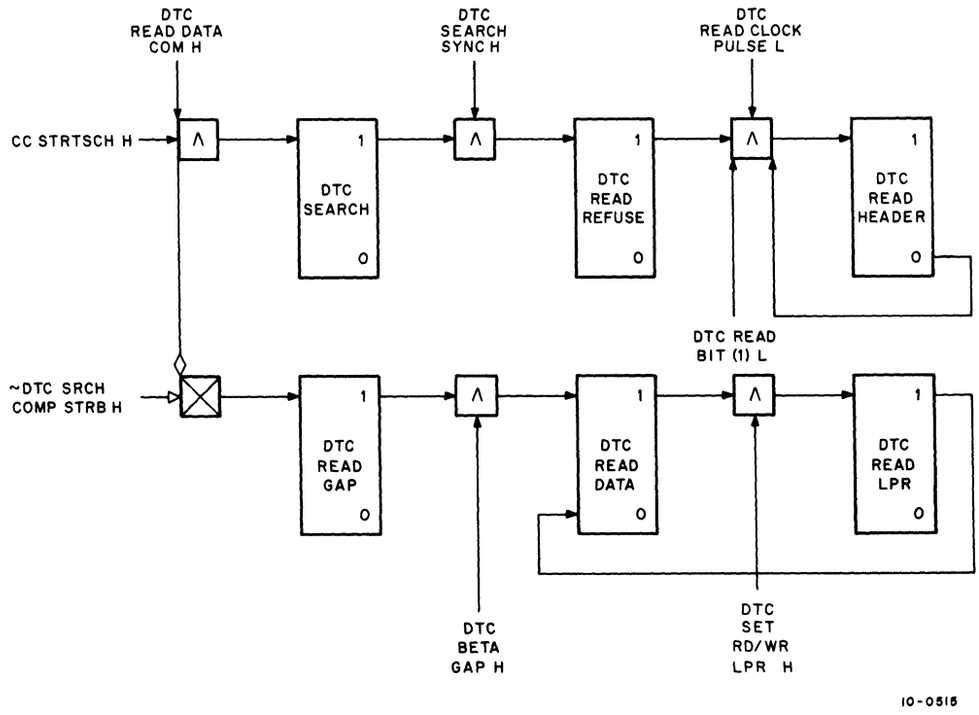


Figure 4-11 DTC Read Data Command, Block Diagram (Revised)

4.8.2.2 **Write Data** – If a DTC WRITE DATA COM H is decoded, it sets the DTC SEARCH flop if ANDed with CC STRTSCH H, and enables setting of the WRITE GAP flop after the header is read (see Figure 4-12).

NOTE

Each flop pertains to a portion of the disk format; the synchronizer must read a header before writing data.

a. When DTC SEARCH flop sets, it sets READ REFUSE flop and, in turn, sets READ HEADER flop in the same manner as in a read data operation. Assertion of DTC CLR READ HDR H resets DTC READ HEADER flop. After a 3-μs delay, DTC READ HEADER (0) H sets WRITE GAP (the delay prevents the header parity bit from being destroyed).

b. When WRITE GAP flops sets, it conditions the setting of DTC WRITE DATA flop. WDC DATA WD CT04 (1) L ANDed with the condition DTC PAR CONT→O, sets the DTC WRITE DATA flop to indicate that a sync bit has just been written. DTC WRITE DATA (1) H resets DTC WRITE GAP flop and conditions the setting of DTC WRITE LPR. When DTC SET RD/WR LPR H goes High, WRITE LPR will set, thereby clearing DTC WRITE DATA flop.

2.8.2.3 **Write Headers and Data** – If a DTC WRITE HDR COM H is decoded (see Figure 4-13), it conditions DTC W H INDEX flop which sets when DSBC SEL INDEX goes High. In addition, DTC WRITE HDR COM H enables DTC WRITE DATA flop to set on a DTC WRITE CLOCK DLY L when either *(a)* WDC DATA WD CT01 and 04 are on a 1 and an RP02 is in use (~DTC RP01 L), or *(b)* WDC DATA WD CT02 and 03 are on a 1 and an RP01 is in use (DTC RP01 L).

a. When DTC W H INDEX flop sets (it can only be set if the DTC W H LOCKOUT switch is disabled), it ANDs with DTC SECTOR DLY H to set DTC WRITE HEADER flop. (DTC SECTOR DLY is a 10-μs delay on DTC SELECTED SECTOR II ∧ IBC BUSY (1) H to allow setting of Head Register in multiple sector reads and writes.) DTC WRITE HEADER (1) H then asserts DTC WRITE ENABLE L. If CC ACTIVE is false at this time, it asserts DTC OVERRUN H and also ANDs with IBC LOCAL (0) L to generate DTC SHIFT CT 0 PLS H/L. In addition, it generates DTC SET WRITE H and ORs with DTC WRITE DATA (1) H to yield DTC WRITE HDR ∧ DATA L which conditions the setting of DTC PREVENT TERM flop.

b. When DTC WRITE DATA flop sets, it resets DTC WRITE HEADER and sets DTC WRITE LPR flop when WDC WORD COUNT EQ 00 L is asserted. The setting of WRITE LPR flop resets DTC WRITE DATA. The DTC WRITE LPR flop resets when WDC DATA WD CT06 (1) H and DTC PAR CONT (0) H coincide.

4.8.2.4 **Clear Attentions** – If IOBD 00, 01, and 02 are decoded as 101 (the CLEAR ATTENTIONS command), IBC SET DAR ETC B produces DTC CLEAR ATTN. When combined with IOBD 27-34, this resets any of the DTC ATTN flip-flops (see Figure 4-14). Note that if an IBC CLEAR ATTN H or an IC CROBAR H is received, all DTC ATTN flops will be cleared simultaneously. These flops are set by DTC ATTN 00-07 H, representing up to eight possible drives. The DTC ATTN signals are received as MPX ATTN 00-07 L from the multiplexer and are inverted prior to being applied to their respective flops.

4.8.2.5 **Restore** – If DTC RESTORE H is decoded, it ANDs with IBC SET DAR ETC DLY H to generate the DTC TAG and BUS LINE strobes (see Figure 4-15). In addition, DTC RESTORE H is ANDed with DTC BUS LINE STROBE H and is sent to the disk as DSBC UB 6 L.

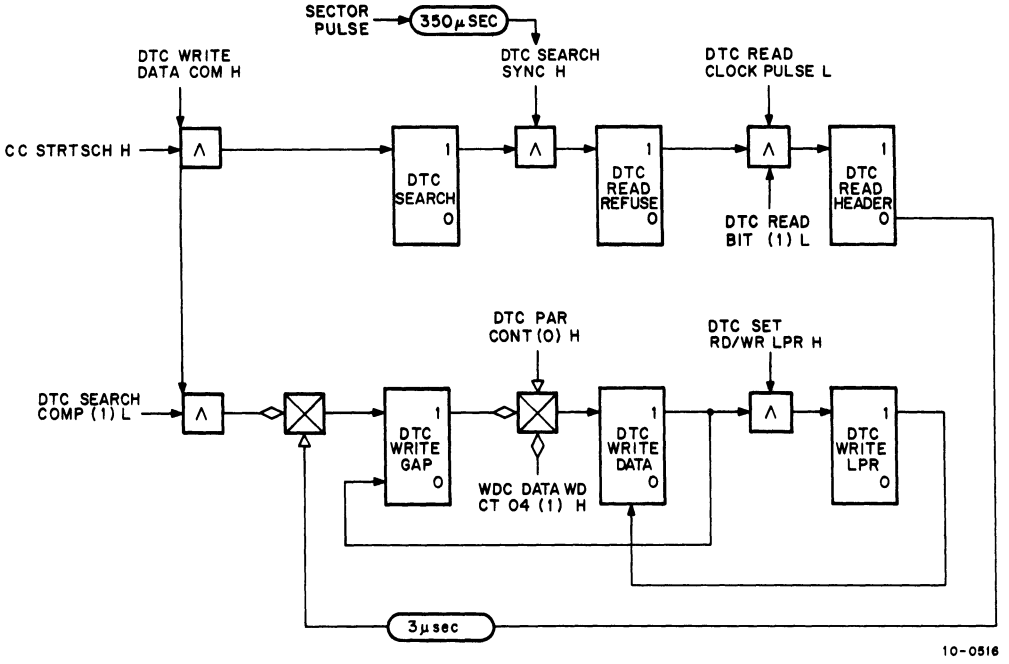


Figure 4-12 DTC Write Data Command, Block Diagram (Revised)

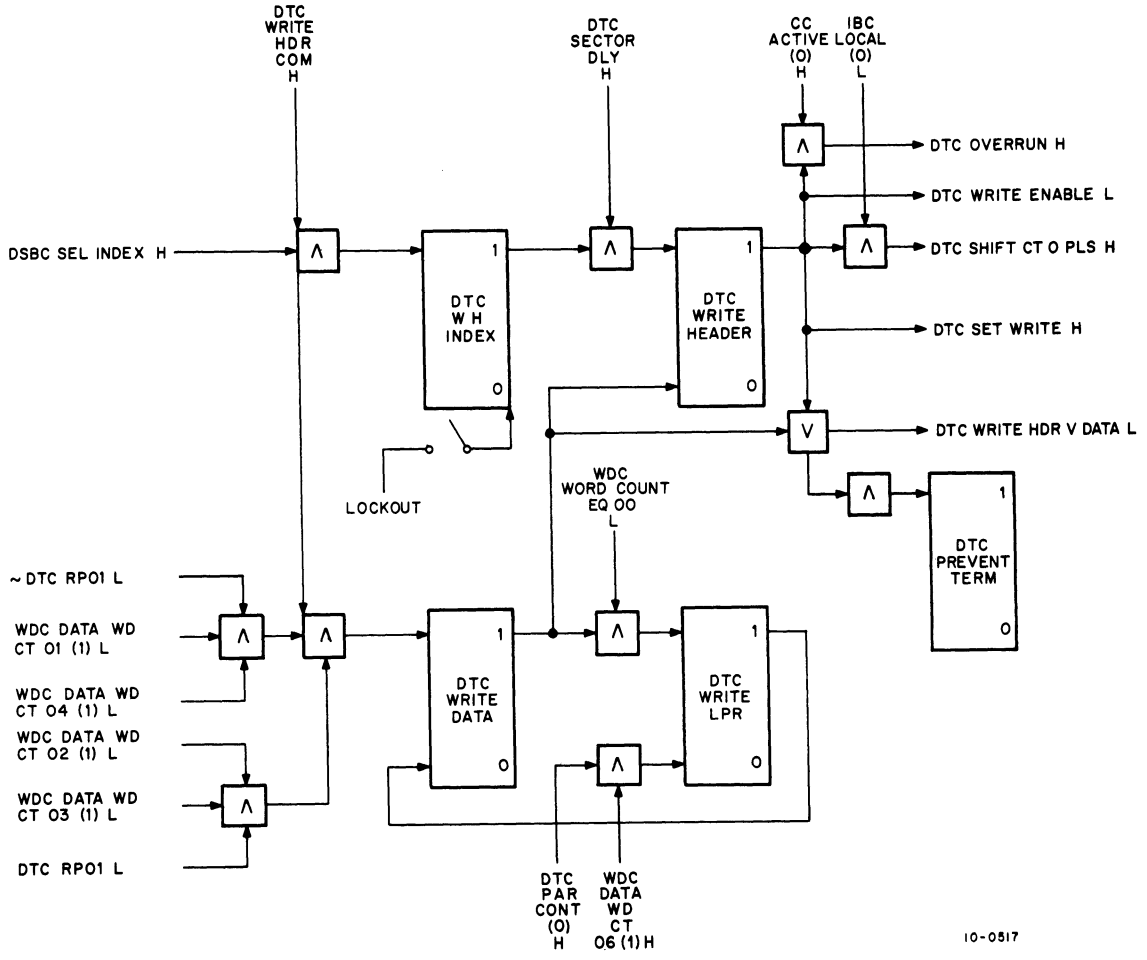


Figure 4-13 DTC Write Headers and Data Command, Block Diagram

The Tag Lines indicate how information present on the Bus Lines is to be used. The Bus Lines contain either control information or address information. The Tag and Bus Line Strobe waveforms are shown in Figure 4-16. Note that on input of either DTC SET HD ADV (1) L, DTC SET HD REG (1) L, DTC CLEAR HD REG (1) L, DTC SET CYL (1) H, DTC SEEK START (1) L, or DTC RESTORE H as described above, the resultant signal encounters various delays that control the set and reset times of an S202 Type flop. The resultant Tag and Bus Line Strobes are sent to the disk drivers shown in DWG RP10-0-DSBC along with their appropriate disk commands where they are decoded. The Bus Line Strobes condition the gates. Then, in the middle of the Bus Line Strobe, when the lines have had time to settle, the Tag Lines strobe the information down the line to the disk.

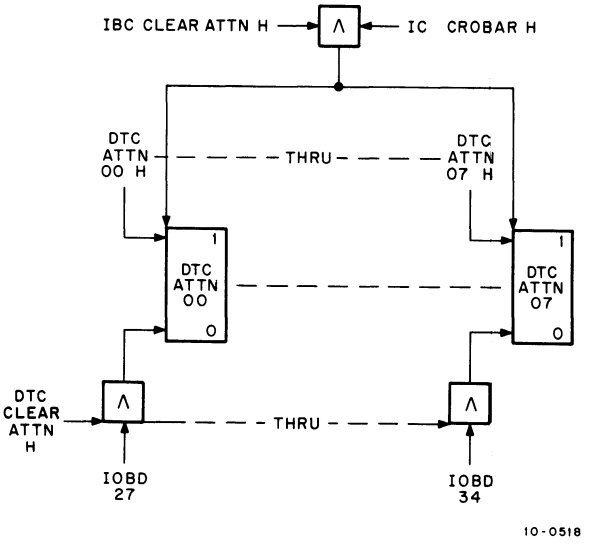


Figure 4-14 DTC Clear Attentions Command, Block Diagram (Revised)

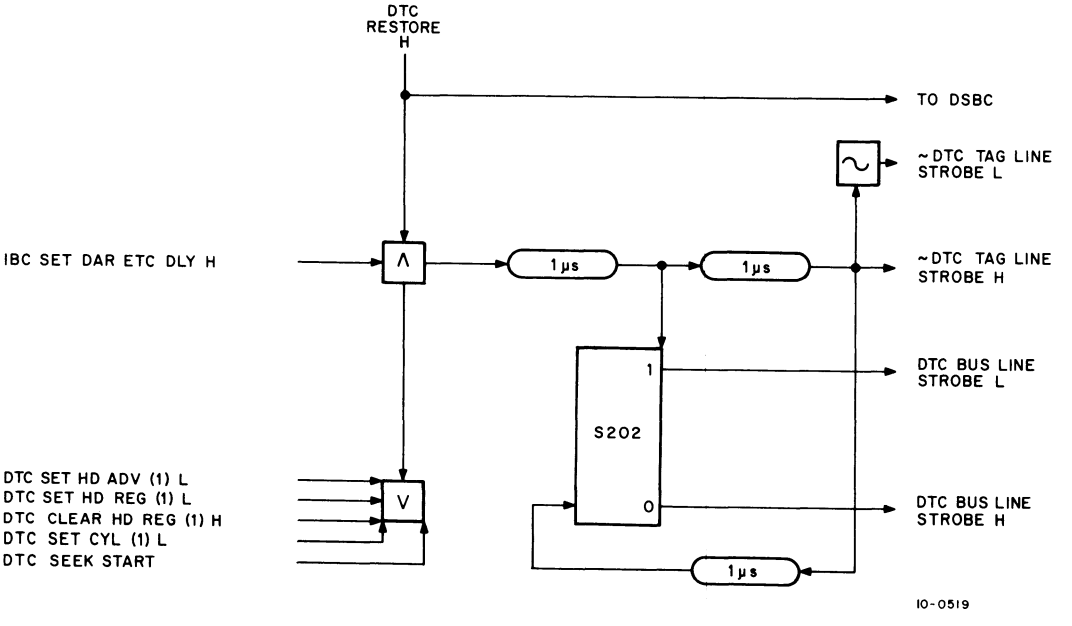


Figure 4-15 DTC Restore Command, Block Diagram

4.8.2.6 **Seek** – If a DTC SEEK COM H is decoded, it ANDs with IBC SET DAR ETC DLY to set DTC SET CYL flop (see Figure 4-17). When DTC SET CYL flop sets, it initiates the BUS LINE STROBEs and conditions the setting of DTC SEEK START flop by ~DTC BUS LINE STROBE H. DTC SEEK START (1) L is ANDed with DTC BUS LINE STROBE H in DWG RP10-0-DSBC where it is sent to the disk as DSBC UB 2 L.

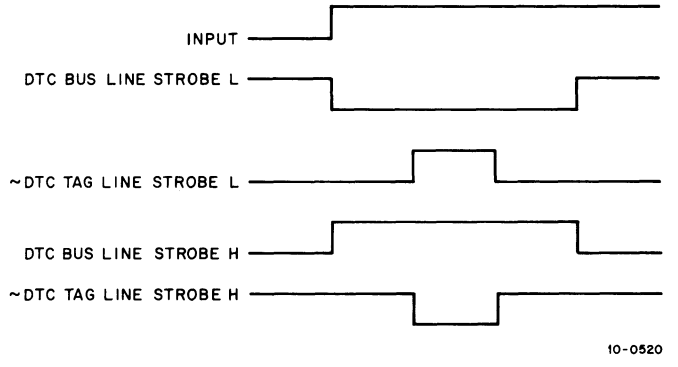


Figure 4-16 Tag and Bus Line Strobe Waveforms

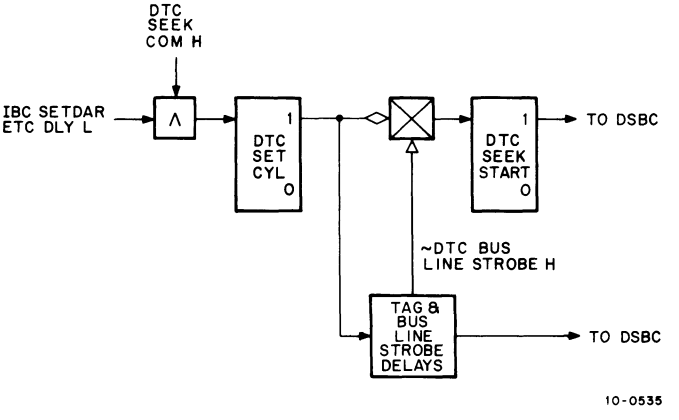


Figure 4-17 DTC Seek Command, Block Diagram

4.8.3 I/O Bus Control

The RP10 I/O Bus Control regulates the interchange of data and control signals on the bidirectional I/O bus lines which carry data and status information, device selection codes, and control signals between the RP10 Synchronizer and the PDP-10 Processor (see DWG RP10-0-IBC).

The device select code bits IC IOS03-09 L are ANDed with IBC LOCAL (0) L to yield IBC DEVICE SELECTED H and IBC DEVICE SELECTED L. If the selection bits contain the RP10 device selection code (250 or 254) and if the RP10 is not in local mode, the RP10 is selected. This is the basic activating level for all RP10 functions. The performance of all basic instructions depends on the presence of this level.

When the READIN or RESET switch is pressed on the PDP-10 Processor or when a programmed reset is issued, IC IOB RESET L is generated, which halts all motion in the RP10 and clears all conditions that initiate an interrupt. This condition prevails until the RP10 is reactivated by a CONO command.

In the RP10, IC IOB RESET L ANDed with IBC LOCAL (0) L, results in IBC POWER CLEAR H and L which is used in the following ways in the device;

a. To direct set IBC GEN CLR.

b. To generate, after 1-μs delay, IBC CLEAR ATTN.

c. To assert IBC CON CLR H which is ANDed with IOBD 32H to set IBC DONE.

d. To set IBC DONE.

e. To set IBC STOP.

f. To reset IBC LOCAL.

The IBC LOCAL START flop is held in the direct reset condition when the switch panel START switch is in the 0 condition (~SWP START L), the switch panel STOP switch has been depressed (IBC STOP (1) L), and IBC BUSY is on a 0. By activating the START switch (SWP START H), the IBC LOCAL START flop will set. As a result, the IBC STOP flop resets and the IBC GEN CLR flop is set (if ~SWP OP00 L is present). IBC GEN CLEAR (1) L conditions the set gate on IBC LOCAL flop, which can then be direct set by SWP LOCAL SET L.

4.8.4 RP10 Read Data Separator

The Read Data Separator (RDS) is shown in DWG RP10-0-RDS. This circuit enables the controller to read information from any disk pack that has been previously recorded by an RP10, irrespective of drive speed differentials between time of write and time of read, or any other variables that might cause the recorded data to reside on the disk in an unpredictable manner (provided those variables are within certain predetermined limits). During a read, the circuit supplies the controller with clock pulses (via Data Window → 0) and DATA OUT pulses (indicating that a 1 bit was read). A crystal clock is used to strobe data pulses and clock pulses at the time the data is recorded; consequently, the average frequency of data read from the disk should be constant. However, in reality it is not. Due to a phenomenon called "bit shift", timing between individual pulses varies somewhat because of speed variations in drives and a phenomenon inherent to magnetic devices termed "pulse crowding."

Figure 4-18 illustrates the effects of these variables. In "a" of Figure 4-18, the ideal theoretical waveforms are shown for raw data consisting of all 0s, 0s and 1s, and all 1s. In "b", the effects of pulse crowding are shown wherein the location of a pulse just recorded will be displaced by the next recorded pulse. The pulse crowding effect becomes more pronounced the closer pulses occur to one another. Because of this effect *1)* there appears to be no displacement of clock pulses when recording an all 0s data pattern, *2)* there is a predictable + and - shift of clock pulses either side of 1s in an alternate data pattern, and *3)* there is an unpredictable variance in clock pulses when recording an all 1s data pattern.

In "c" of Figure 4-18, the effect of drive speed differentials is shown on an all 0s data pattern, first with speed of write greater than speed of read, and then with the opposite conditions true. In the third waveform of "c", the effect of pulse crowding has been added to a speed variation.

NOTE

The individual shifts of clocks from their normal positions vary from pulse to pulse producing an overall variance called "jitter."

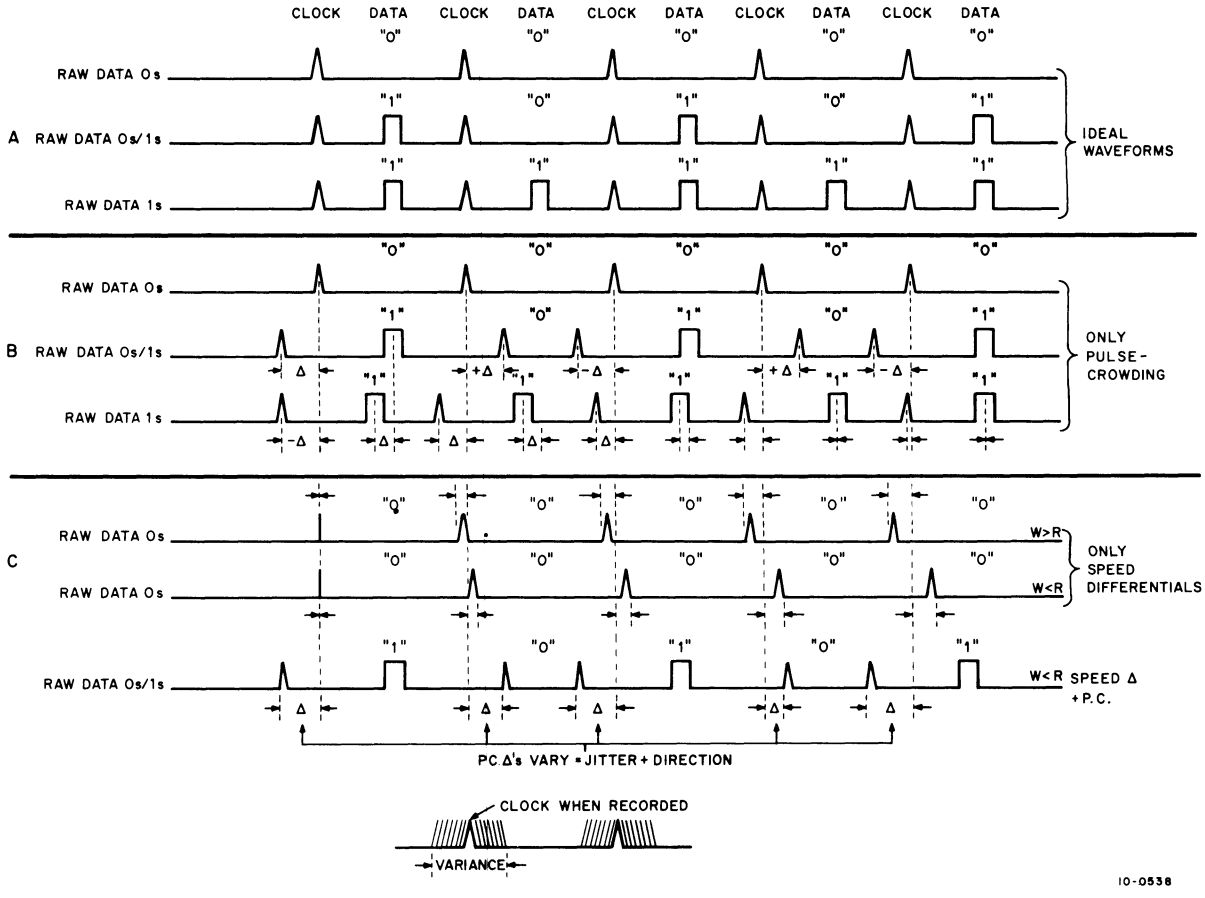


Figure 4-18 Sources of Jitter in Disk Playback

There is no guarantee that an individual disk pack will always be read on the same drive on which it was written, or that the drive speed of write will be exactly the same as the speed of read even on the same drive. Therefore, a means must be provided that enables the controller to read data in a jitter environment provided the jitter does not exceed certain specified limits. The reading of this data is accomplished by a timed sampling method called "windowing" in which the controller is forced to read during a variable period of time after the average occurrence of each clock pulse. The time period is a function of the deviation of each clock pulse from normal with respect to the deviation of the previous clock pulse. A one-shot type of separator cannot be used because a single value measured from one pulse cannot be found which provides a full window for the next and only the next pulse. However, because bit shift is measured by the time difference (either plus or minus) from the time a bit was recorded, windowing can be achieved if the window generator is aligned with the time each pulse was recorded rather than on the actual pulse detected and by aligning on the average of the clock bits coming in rather than on each succeeding bit.

This averaging is achieved by the VFO clock circuit comprising: flops RDS ERR A and B, the module B410, and the analog circuit G589 or G590. In operation, the VFO clock frequency slows down before the first sync field because no pulses have been coming in (0 frequency). Thus, the VFO clock requires considerable time to come up to frequency (see Figure 4-19). For this reason, the first sync field in the format must be approximately 350 μs. The second sync field need not be as long (88 μs for RP01 and 44 μs for RP02) because the VFO clock is up to frequency and needs only to realign itself slightly as a result of the switching discontinuity from reading the header to writing data.

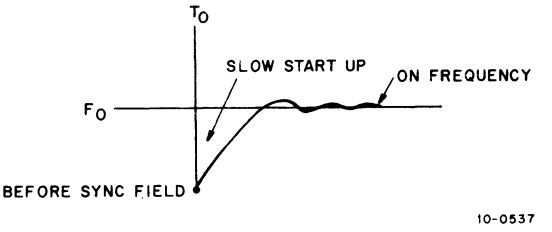


Figure 4-19 VFO Startup Waveform

During each sync field the RDS must use all clock pulses received to achieve synchronization. Window generation must be disabled at these times because misalignment can mask some clock pulses. The signal RDS SYNC FIELD ENBL is generated during these periods to bypass window selection. This signal is removed after sufficient time has passed to ensure that the window is in alignment. To provide the averaging effect, the data window is toggled by the VFO clock rather than by incoming clock pulses that contain the jitter. The RDS ERR A and B flops serve as a phase comparator. When these two flops are in different states, correction voltage is applied to the VFO clock. The correction voltage, resulting in either faster or slower VFO operation, is determined by the flop set to a 1. Neither flop remains on a 1 for any length of time. When both flops are on a 1, a clear pulse is generated which resets both flops. Thus, the amount of time one flop is on a 1 while the other is on a 0 represents the time difference between the pulses that set the flops. The correction voltage that is applied forces the pulses to align.

The two set pulses are generated by RDS DIVIDE 2 → 1 and RDS CLOCK DLY. The RDS DATA WIND and RDS CLOCK WIND are toggled by the VFO clock through RDS DIVIDE 2, which halves the clock frequency; therefore, the comparator can control the toggling rate. The data window's edge is aligned to RDS CLOCK OUT (see Figure 4-20) while the clock window is aligned to RDS DIVIDE 2 → 1 and the data pulse may fall anywhere within the data window. DTC SET READ L is applied to the clear inputs to ensure that the DTC READ BIT is cleared when executing a write.

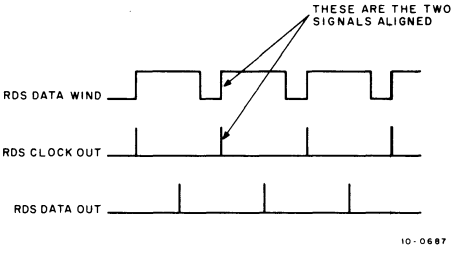


Figure 4-20 RDS DATA WIND Waveform

A block diagram of the Read Data Separator is shown in Figure 4-21. The functional elements include a pulse shaper, a sync separator, a window positioner, a phase comparator, and a separate differential amplifier/filter for each voltage controlled oscillator (VCO). Two VCO's are provided; one for RP01 drives, the other for RP02 drives. In addition, the RDS contains a frequency divider and an optimizer that loops back to control output gating of incoming data.

During the preamble or synchronization period, the input from the disk (MPX RAW DATA H) is fed to two AND gates each of which is enabled by the type of disk drive not in use. If an RP02 is in use, the gate enabled by ~DTC RP01 ENABLE H is turned on. If an RP01 is used, the opposite is true.

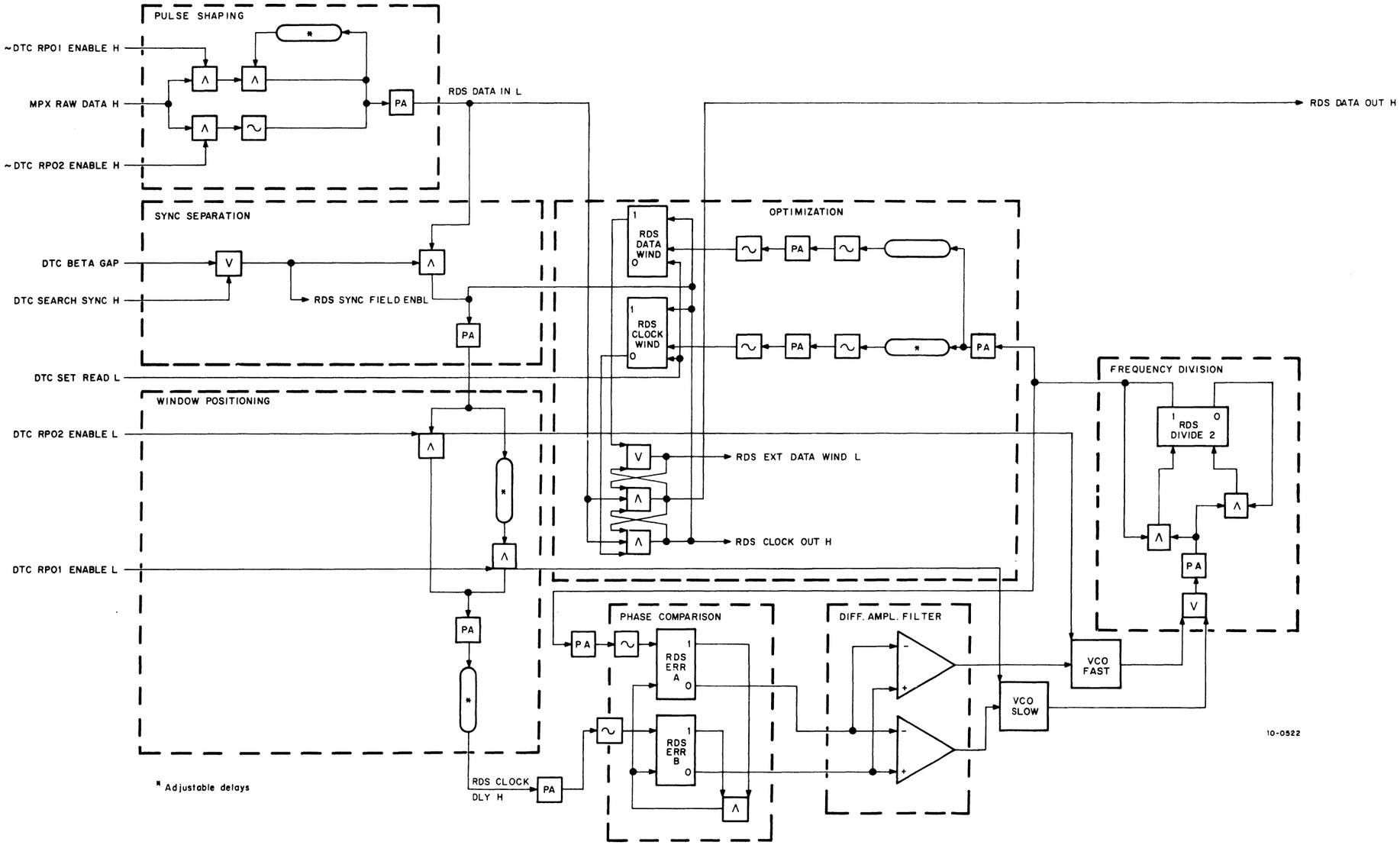


Figure 4-21 RP10 Read Data Separator, Block Diagram (Revision 1)

The RDS CLOCK DLY H is used as a reference signal in setting RDS ERR B, while RDS DIVIDE 2 is used to set RDS ERR A. If both RDS ERROR flops are set, a signal is generated that resets both flops. As such, they function as a phase comparator (see Figure 4-22).

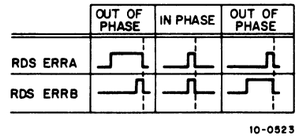


Figure 4-22 RDS Error Flops Waveforms

The outputs of RDS ERR A and B are fed to two differential amplifiers; each provides control voltage for individual voltage controlled oscillators (VCOs). Only one VCO is enabled at any time by the type of drive in use. The differential amplifiers are equipped with low-pass filters that remove jitter and random frequencies in the pulse train, thereby effectively averaging the frequency of the incoming bits. Any difference in the set times of RDS ERR A and RDS ERR B appears as a differential input to the differential amplifiers and causes an output to the VCO of such a polarity as to correct the error in VCO frequency, thereby synchronizing the VCO to the incoming clock bits.

The frequency of each VCO is set at the 1s rate component of the disk drive it serves. Consequently, VCO SLOW is set to operate at approximately 2.5 MHz while VCO FAST operates at approximately 5.0 MHz. The output from the enabled oscillator is used to complement a frequency divider flop (RDS DIVIDE 2) whose 1s output, in turn, is applied to a window gating network (see Figure 4-23).

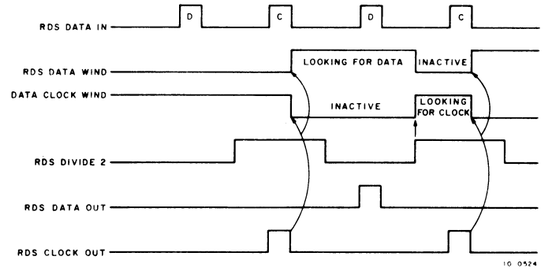


Figure 4-23 Optimum Window Generation Waveforms

The RDS DIVIDE 2 (1) pulse train, which is essentially a clock window, is applied to the RDS DATA WIND and RDS CLOCK WIND flops in complemented fashion through a latching arrangement of gates. The RDS DATA WIND and RDS CLOCK WIND flops are reset by the separated clock pulse RDS CLOCK OUT H. On the TE of RDS CLOCK OUT, the data window is opened and the clock window is closed. These conditions prevail until the RDS DIVIDE 2 once again transitions to the 1 state. At this time, the data window is closed and the clock window is opened.

When the data window has been generated, the two delay lines associated with RDS CLOCK DLY H are adjusted to set the data and clock pulses in the center of their respective gating waveforms.

4.9 RP10 COUNTERS

The sector and word counters are described in the following paragraphs.

4.9.1 Sector Counters

The RP10 sector counter consists of eight separate sector counters which operate independently to count sectors on eight possible Disk Pack Drives (see Figure 4-24 and DWG RP10-0-SC). Each counter utilizes the raw sector pulse train from its associated drive; a pulse that is detected by the transducer and from which index pulses have not been removed. If two pulses less than 350 μs apart are detected, the logic interprets this as an index pulse or sector 0. This detected index pulse then forms SCC X CLR PLS H, which is used to clear the sector counter. The SCC X + 1 pulse is formed from all other sector pulses (other than at index time) and is used to increment the sector counters.

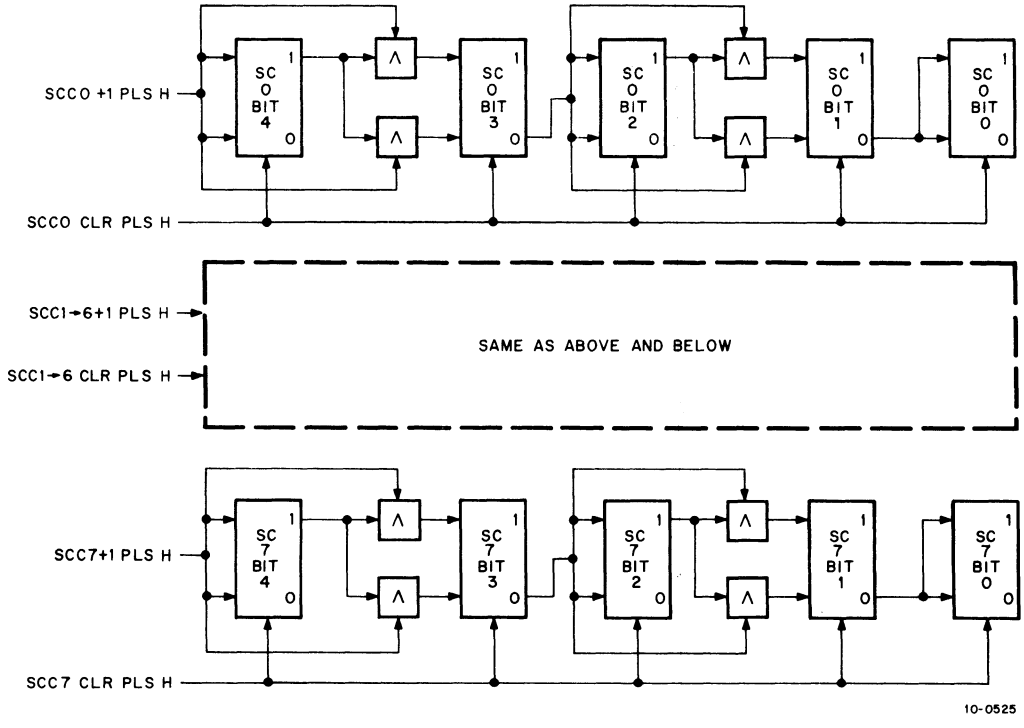


Figure 4-24 RP10 Sector Counter, Block Diagram

4.9.2 Sector Counter Buffer

The RP10 Sector Counter Buffer is shown in Figure 4-25 and in DWG RP10-0-SCB. The state of the selected sector counter is fed into the buffer from the multiplexer by SCB FM SC REG JAM L. This normally occurs 250 ns after the selected sector counter has changed its count. However, when IBC DOD C H is true (this is the time when the sector counter bits are being strobed onto the I/O bus), the sector counter buffer is prevented from changing. An SCB FM SC REG JAM L may have been suppressed during that time; therefore, an SCB FM SC REG JAM L is unconditionally generated on ~IBC DOD C H. IBC DATAO SET L is used to update the Sector Counter Buffer with the DATAO that selects the drive. This prevents transfer of the old sector count back to the processor with a DATAI, when de-selecting one drive and then selecting a new one.

4.9.3 Sector Counter Control Pulses

A simplified block diagram of the RP10 Sector Counter Control Pulses circuit is shown in Figure 4-26. Thedetailed logic appears in DWG RP10-0-SCC. This circuit comprises eight identical sections of logic. Each section receives the DTC SEC PLS X L for a particular drive, and produces three control signals. The signal SCC X

CHANGE COUNT L is the result of inversion, pulse amplification, and reinversion. Each sector pulse is also delayed by 500 μs, ANDed with the output of the pulse amplifier, and inverted to produce SCC0 + 1 PLS H. The output of the delay (~SCC X SS) is also ANDed with the inverted output of the pulse amplifier to yield SCC X CLR PLS H. These outputs are then applied to the sector counter and the sector counter multiplexer.

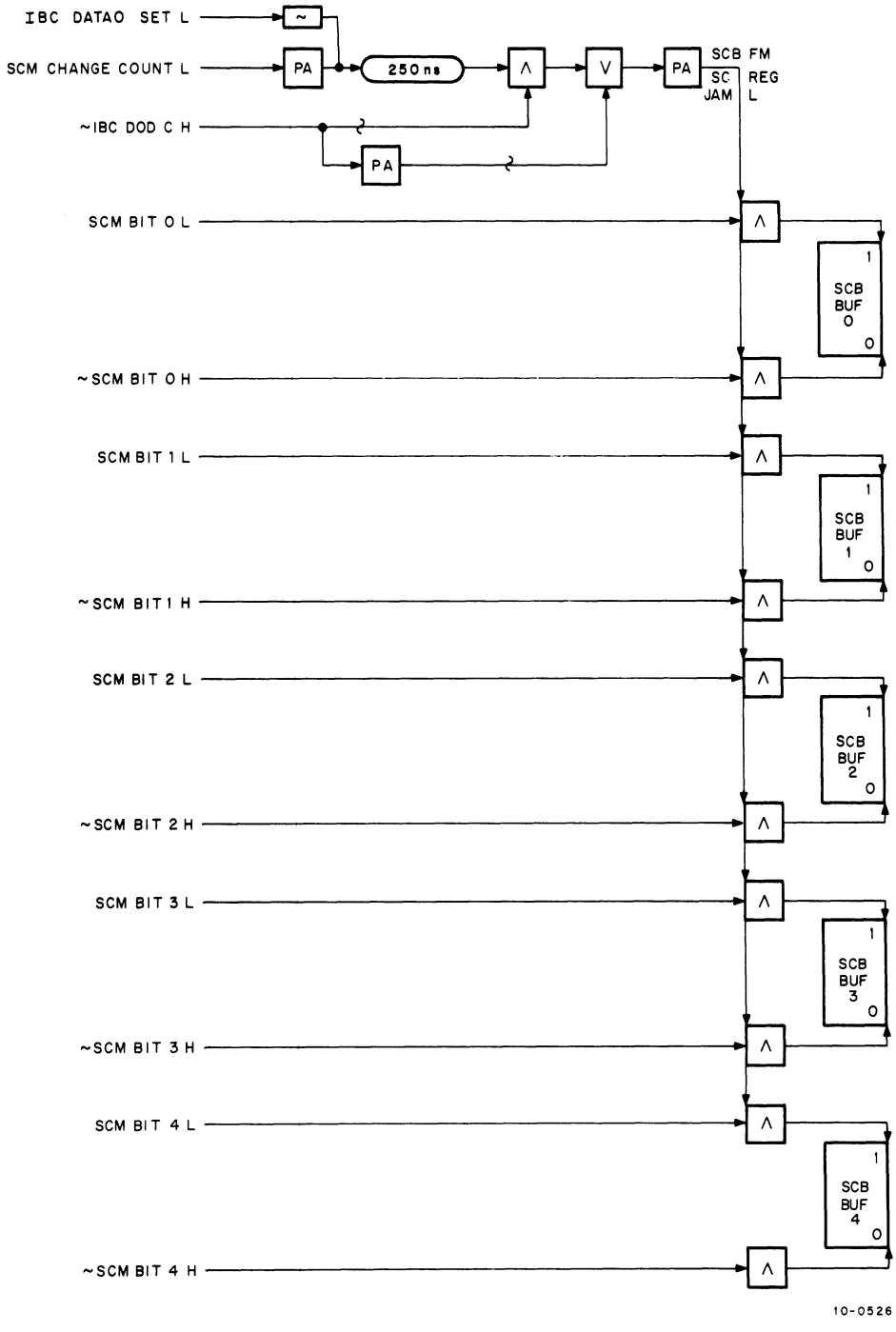


Figure 4-25 RP10 Sector Counter Buffer, Block Diagram (Revised)

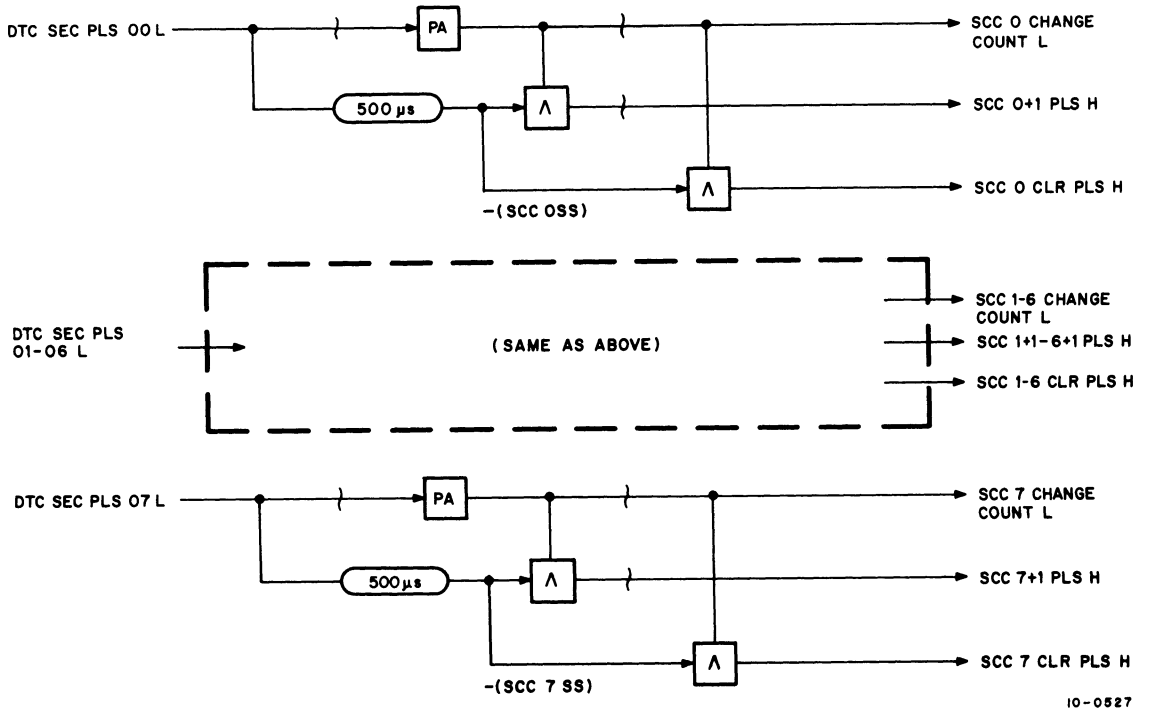


Figure 4-26 RP10 Sector Counter Control Pulses, Simplified Block Diagram

4.9.4 Sector Counter Multiplexer

The RP10 Sector Counter Multiplexer (DWG RP10-0-SCM) is shown in block diagram form in Figure 4-27. The Sector Counter Multiplexer selects the outputs from one of the sector counters contained in the RP10 (eight counters are provided; one for each drive). Selection is determined by the DAR SEL DRIVE 0-7 L signals – each DAR SEL DRIVE signal corresponds to a specific disk drive. The DAR SEL DRIVE signals also enable selection of one of the eight SCC CHANGE COUNT L signals.

4.9.5 Word Counters

The RP10 Word Counters are shown in block diagram form in Figure 4-28 and in DWG RP10-0-WDC. The circuit contains two 3-bit ring-tail counters that count the six bits per byte and the six bytes per word being shifted. The circuit also contains a modulo 128 counter to count the number of words in each data field.

Input is from DTC SHIFT BIT CNT L. This signal is generated in the Data Transfer Control and results from either DTC READ IMAGE (1) L and DTC READ CLOCK PULSE L; DTC WRITE CLOCK L, DTC WRITE ENABLE L, and DTC PAR CONT (0) L; or DTC READ ENABLE L, DTC READ CLOCK PULSE L, and DTC PAR CONT (0) L.

Each DTC SHIFT BIT CNT L increments the WDC BIT SHFTCT counter by 1. At the count of 5, the gated inputs to WDC WD CT +1 A & B and WDC BYTE CT +1 become enabled. The next DTC SHIFT BIT CNT sets the three flip-flops at the same time that the bit shift counter returns to 0, producing DTC BIT SHFTCT EQ 0. Setting WDC BYTE CT +1 produces an increment input to the BYTE SHFTCT counter, thus, causing it to increment by 1. The three +1 flip-flops are cleared by DTC DATA CLOCK DLY and reset again at each BIT SHFTCT of 5. If WDC BYTE SHFTCT EQ 5 is true when the +1 flip-flops are set, the WDC DATA WD CT register increments by 1. Each complete cycle of the BYTE SHFTCT register increments the word counter until it reaches overflow at word 128. This produces WDC WORD COUNT EQ 0 L, which indicates the end of a particular data field.

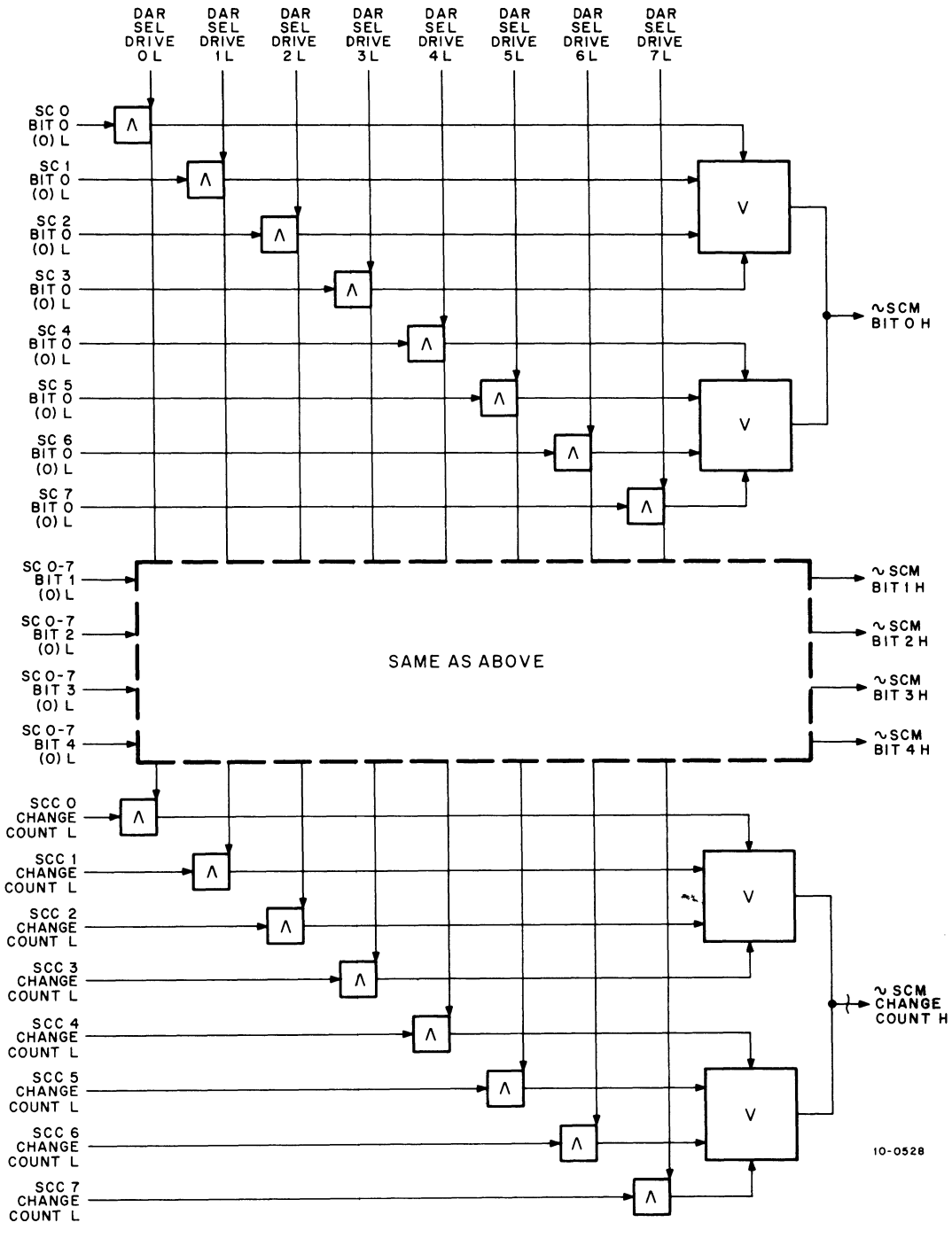


Figure 4-27 RP10 Sector Counter Multiplexer, Block Diagram

The bit and byte count flops are cleared by DTC CLEAR SHFTCT H. The word count flops are cleared by WDC CLEAR DATA WD CT H, which is the ORed result of DTC SELECTED SECTOR, DTC WRITE GAP, or DTC WRITE HEADER.

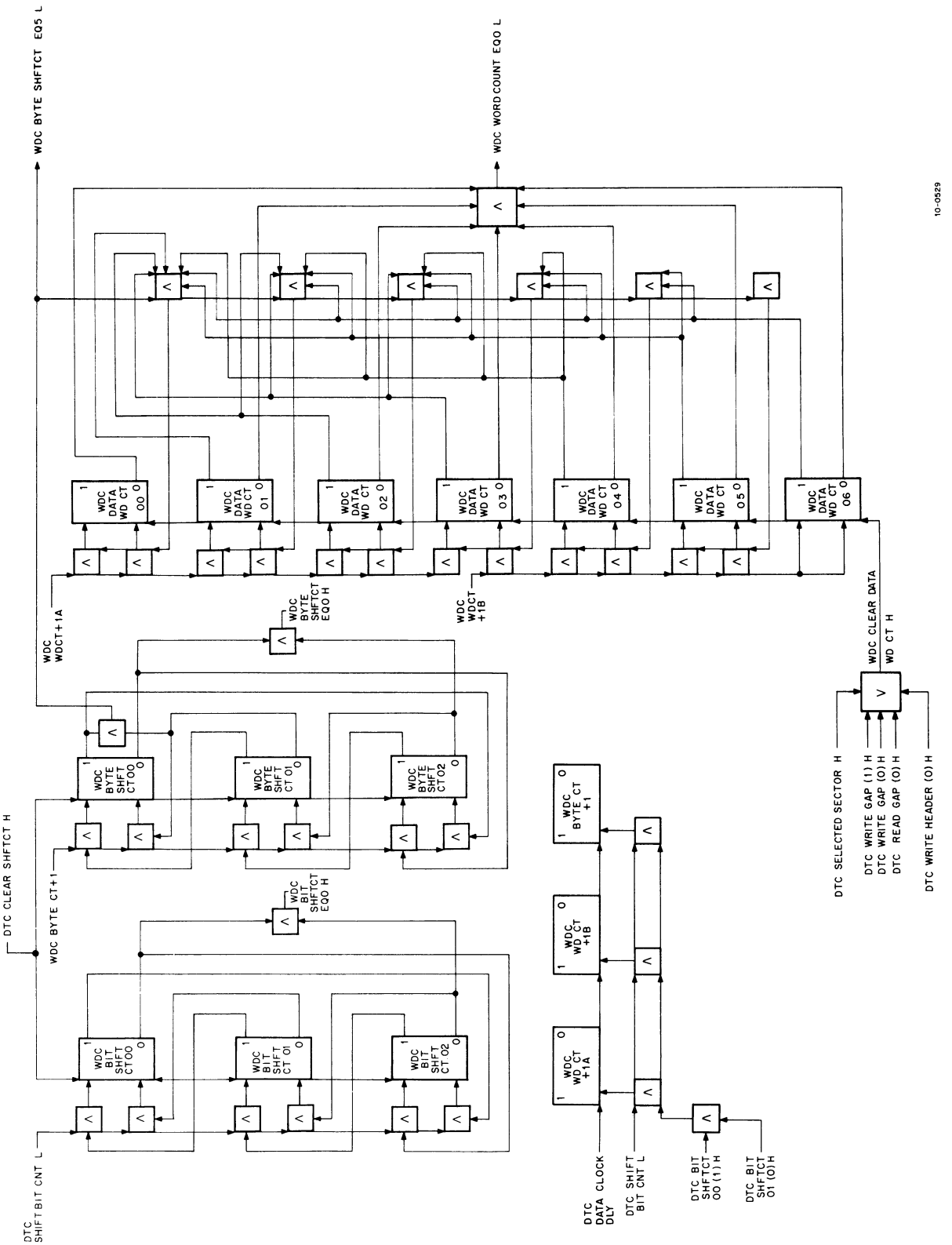


Figure 4-28 RP10 Word Counters Block Diagram (Revised)

4.10 RP10 COMPARATORS

4.10.1 Header Compare and Designation Error

The RP10 Header Comparator and the circuit that brings up a designation error are shown in Figure 4-29 and in DWG RP10-0-HCDE. Header comparison is indicated by no output (HCDE HEADER COMPARE L) from the composite AND/OR gating associated with cylinder and surface/sector comparison. The comparison operation is split in two to provide header protection by continuous monitoring of cylinder address (-HCDE CYL COMP H). Protection is realized any time a lack of cylinder comparison is combined with the completed search operation (DTC SEARCH COMP (1) L) to generate HCDE HDR READ ER H. This error condition immediately terminates operation by setting CXR SEARCH ER 2 on -DTC SRCH COMP STROB H, which fires DTC FINISH and shuts down the controller.

The states of each cylinder, surface, and sector flop in the data address register are individually ANDed with the opposite state of equivalent bits in the LPR. The results of each ANDing are ORed to produce an output if any one bit state does not compare with its counterpart.

Logic is provided to indicate that a drive, not included in the system, has been designated (HCDE DRIVE DES ERROR H). The SEL DRIVE signals from the data address register are applied to an OR gate in this comparator. The input to the gate can be jumpered for any illegal drives, thereby producing an error indication if one of these drives is commanded.

The sector and surface designation error portion of this circuit contains a flop for each error. These flops are set by decoding the appropriate flops in the data address register. The error flops are reset by ANDing IBC CON CLR H with IOBD 28 H for sector designation error and IOBD 29 H for surface designation error. Signal DTC RP01 L is applied to the designation error logic to allow decoding of illegal addresses for either an RP01 or an RP02 drive. The setting of each flop is conditioned by the ANDing of DTC OP CODE00 (0) L and IBC SET DAR ETC DLY L. Both designation error flops are cleared by IBC INITIAL CLEAR C H.

4.11 RP10 DATA FLOW

The flow diagrams contained in Volume 2 of this manual are discussed in the following paragraphs.

4.11.1 Starting

On receipt of DATAO 250 or 254, IC IOB DATAO CLEAR generates IBC INITIAL CLEAR if IBC BUSY and CC ACTIVE are both false. The assertion of IBC INITIAL CLEAR generates CLR IBC GEN CLR if IOBD 00 is false when IBC LOCAL is false. The INITIAL CLEAR signal also clears ILLEGAL WRITE, ILL COM WL BUSY, OVERRUN, DISK WD PE, DISK SEC PE, PARITY ERROR, PREVENT TERM, WRITE EVEN PAR, SEARCH ER 0-2, NON EX MEM, CHAN DATA PE, CHAN CONT PE, and CW XFER COMP in the Condition Register; the cylinder, surface, sector, and drive registers in the DAR; and the OP CODE register in the DTC. In addition, when IBC INITIAL CLEAR is asserted, it clears SET CYL, SEEK START, NO SECTOR, INDEX, SET HD ADV, CLEAR HD REG, SET HD REG, HEAD SET, CHN PLS BUF, and DTC4 C13M, also in the Data Transfer Control and it clears IBC DONE and both sector and surface designation errors in the HCDE.

When IBC INITIAL CLEAR is generated, it results in DTC CLEAR A and B which clear AR0-17 and AR18-35, respectively. It is used also to generate DTC CLEAR SHFTCT (which, in turn, clears the bit and byte counters) and to generate the DTC CLEAR PAR PLS which results in DTC CLEAR PARITY and CLR DTC PAR CONT.

With all of the above conditions cleared, receipt of IC IOB DATAO SET results in IBC DATAO SET. If the controller is busy, IBC BUSY is set. This signal ANDed with IBC DEVICE SELECTED (true only if IBC LOCAL is false) generates the ILL COM WL BUSY condition to indicate that a command was given to the control before it finished a previous command. If the synchronizer is not busy (IBC BUSY (0)), IBC SET DAR ETC A and B is generated.

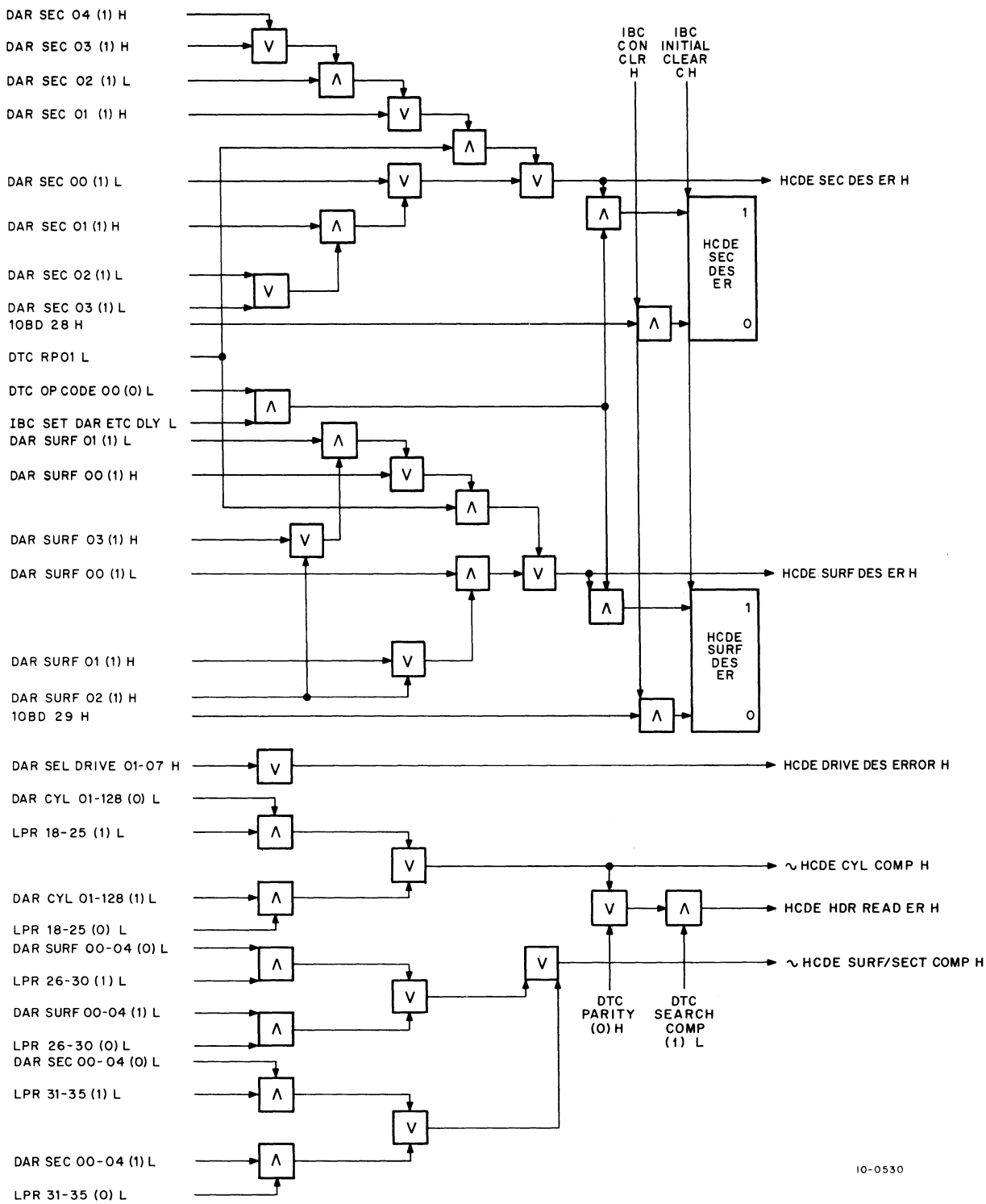


Figure 4-29 RP10 Header Compare and Designation Error, Simplified Block Diagram (Revised)

The A version of this signal loads the drive and cylinder registers in the DAR and sets disable stops in the condition register for Disk Sector Parity Error (if IOBD 24 is set), Channel Data Parity Error (if IOBD 25 is set), or Disk Word Parity Error (if IOBD 26 is set), and SET CXR WRITE EVEN PAR (if IOBD 35 is set).

The B version of IBC SET DAR ETC sets the Surface, Sector, and Op Code Registers in the DAR. The Op codes are directed to the Data Transfer Control where they are decoded into the commands listed in Table 4-1.

Table 4-1
Data Transfer Control Commands

DTC OP CODE Bits			DTC Command
0	1	2	
0	0	0	Read Data
0	0	1	Write Data
0	1	0	(Not Used)
0	1	1	Write Hdr
1	0	0	Seek
1	0	1	Clear Attn
1	1	0	No Op
1	1	1	Restore (Recalibrate)

If the decoded command is NO OP or CLEAR ATTN, the commands are executed. If the command is RESTORE or SEEK and the controller is in Local Mode, IBC LOCAL START (DWG RP10-0-FCL) will assert CLR IBC SET DAR ETC DLY. If the RP10 is not in Local Mode (IBC LOCAL (0)), IBC BUSY (0) and IBC DEVICE SELECTED will assert CLR IBC SET DAR ETC DLY, which is combined with IBC LOCAL (0) to generate SET IBC LOAD ICWA. This ICWA signal then loads the Initial Control Word Address contained in IOBD 27-34 into bits 27-34 of the Assembly Register.

After a 500 ns delay, SET IBC SET DAR ETC DLY generates CLR IBC LOAD ICWA and with DTC CLR ATTN clears the appropriate ATTN 0-7, as specified by IOBD 27-34. If a seek command is decoded, SET IBC SET DAR ETC DLY sets DTC SET CYL which, in turn, starts the Seek operation. If a restore command is given, SET IBC SET DAR ETC DLY sets DTC BUS LINE STROBE directly, thus enabling DSBC UB 6 to execute the command. When a data transfer command is received (OP Code 00 on a 0), SET IBC SET DAR ETC DLY triggers CC PREVENT TEST. If HCDE SEC DES ER is asserted at this time, 1→ HCDE SEC DES ER results. If HCDE SURF DES ER is asserted at this time, 1→ HCDE SURF DES ER results. Either of these conditions raises DTC FINISH, thereby terminating operation.

When CC PREVENT TEST fires, it starts the 1 μs CC PREVENT TEST TIMEOUT. At the end of this delay, the conditions for CC PREVENT START are checked. The channel will not start (CC PREVENT START) if a drive designation error has been detected (HCDE DRIVE DES ERROR), the power supply voltage has dropped (CXR PS FAIL (1)), a sector designation error has been indicated (HCDE SEC DES ER), the disk is not ready (CXR DISK NOT RDY), or a surface designation error has been detected (HCDE SURF DES ER). In addition, the channel will not start if the drive is in read only mode (DSBC SEL UNIT RD ONLY) and either of the two write conditions has been commanded (DTC OP CODE 00(0) ∧ DTC OP CODE 02 (1)).

If CC PREVENT START is true, IBC DONE and IBC GEN CLR are both set. This condition generates CXR PI ENABLE if IBC BUSY and IBC LOCAL are both false and clears DIS DSPE STOP, DIS CDPE STOP, and DISABLE DWPE STOP in the condition register. If CC PREVENT START is not true, IBC BUSY and CC ACTIVE BUF are set. This condition sets CC ACTIVE after 40 ns, if IC CHAN STARTED is on a 0 (proceed on DWG RP10-0-FCCC to start the channel). In addition, the combination of IBC BUSY (1) and CC ACTIVE BUF (1) sets DTC CLEAR HD REG if DTC OP CODE 0 is false, thereby clearing and setting the head register in the drive as shown in DWG RP10-0-FCDC.

If CC ILLEGAL WRITE is asserted at the time of CC PREVENT TEST TIMEOUT, CXR ILLEGAL WRITE is set.

4.11.2 Recognizing Headers

CC ACTIVE BUFF sets as a result of CC PREVENT TEST H and ~CC PREVENT START to indicate that the RP10 is ready to assume control of the data channel as soon as the channel is free. If CC CHAN STARTED is on a 0 (indicating that no device further down the daisy chain is accessing the channel), CC ACTIVE sets. This condition results in CC CHAN START OUT and, when the channel is ready, it sends IC CHAN BUSY IN to the RP10. At this point, the RP10 has control of the data channel and asserts CC STRT SCH.

Assertion of CC STRT SCH sets DTC SEARCH and the RP10 then waits for the first sector pulse. On receipt of the sector pulse, DTC SECTOR DLY H is triggered. This delay allows the drive head register to increment during multiple surface data transfers (see Paragraph 4.11.6). The delay then triggers a 350-μs delay (DTC SEARCH SYNC) which sets READ REFUSE. When READ REFUSE sets, it turns on the read circuitry (see Paragraph 4.11.5). The separator's window is bypassed during this time, but after the delay times out, DTC READ HEADER is conditioned for setting by detection of a 1 bit and the window bypass is removed.

The 36 bits following the 1 bit are read into the LPR (see Paragraph 4.11.7), and when a full word has been loaded, the Byte Counter and Bit Counter return to 0. At this time, DTC PAR CONT sets indicating that the parity bit is about to be read. The clock pulse following the parity bit clears PAR CONT (see Paragraph 4.11.10), and when parity control clears, DTC SRCH CMPR STRB is triggered. This strobe has a 600 ns delay to allow for gate delays throughout the compare circuitry. When it times out, DTC SRCH COMP is set if no parity error occurred and the headers compare. The headers are checked via HCDE COMPARE signal which determines if the address bit is a 1 and the data bit a 0, or the address bit is a 0 and the data bit a 1. If either of these conditions is true for any bit between 18 and 35, HCDE HEADER COMP is false. The data bits in the LPR are checked against the address bits in the DAR. If they compare, DTC SRCH COMP sets, and DTC SEARCH clears. If they do not compare, DTC SEARCH remains set. An R302 delay is fired unconditionally (88 μs for RP01 or 44 μs for RP02) producing BETA GAP. The BETA GAP bypasses window selection in the separator to allow resynchronization of the separator. This is necessary due to the discontinuity between the header portion, which is written once, and the data portion, which can be written any time on any drive. At this point, the flow changes to either a read or a write.

4.11.3 Reading Data

When DTC SRCH COMP STRB times out (after the header has been read), it sets READ GAP. However, if DTC SRCH COMP did not set, DTC READ GAP clears when BETA GAP times out and the controller waits for the next sector pulse. If DTC SRCH COMP did set, READ GAP remains set, and the detection of the first 1 bit then sets READ DATA. After 200_8 words are read with parity (see Paragraph 4.11.7), DTC READ LPR sets, and the next 37 bits are exclusive ORed into LPR 0-35 and LPR 36 (see Paragraph 4.11.10). When DTC PAR CONT switches to a 0, indicating that the 37th bit has been read, DTC READ LPR clears thereby setting DTC GAP and triggering a 600-ns delay. The delay, in turn, sets CXR DISK SEC P E if any LPR bit is not on a 1.

4.11.4 Writing Data

After SEARCH COMP has been set, the transition of DTC READ HEADER to 0 sets DTC WRITE GAP after a delay of 3 μs. This delay ensures that the first bits written will not destroy the last few bits of the header. When WRITE GAP sets, the controller writes 0s onto the disk without parity. After four words of 0s have been written, WRITE DATA is set, and parity control switches to a 1. Parity is then written for the last sync word (this parity bit is the 1 bit that sets READ DATA during a read operation). After 200_8 words of data are written (see Paragraph 4.11.8), DTC WRITE LPR sets, and the contents of the LPR are written on the disk. The controller then writes a second LPR as guard bits and, after this has been done, DTC GAP sets. The DTC ERASE flop, which controls erase current in the drive, is turned off 20 μs after writing has stopped to allow data that was written to pass under the erase heads before they are turned off.

4.11.5 Commanding the Drive

Drive commands and data are sent out on the same eight bus lines. Three tag lines indicate whether the information on these lines is data or commands. The information on the bus lines is strobed into the drive by bringing up the tag signal in the middle of the command. The only exceptions to this are read and write commands. When either of these commands is issued, both the bus line and tag line remain true throughout the time that read or write is true. These commands are executed by making SET WRITE or SET READ true by ORing the various write flops or read flops.

NOTE

All read or write flops are cleared by the next flop transition to a 1 state. This ensures that SET WRITE or SET READ do not momentarily go false if one flop should be slow.

4.11.6 Reading Multiple Sectors

Multiple sector reads are performed only in on-line mode (not local). During on-line operations, normal terminations are performed via the channel going ~BUSY. If the channel stays active after transferring a sector, the RP10 continues reading. When DTC SRCH COMP STRB H is fired, if the cylinder portion of the succeeding header was read incorrectly, CXR SRCH ER 2 is set. This causes DTC FINISH to fire and shut down the controller.

If the last sector read was sector 9 (4 in RP01), the controller moves down one surface. An advance head command to the drive, which increments the drive's head register by 1, accomplishes this move. The controller enables to determine which sector it is reading or writing after the first sector; therefore, the program must keep track of surfaces and sectors. After reading sector 9 (4 in RP01), an index pulse occurs that sets DTC INDEX. The next sector pulse then sets DTC ADV HEAD, which increments the drive's head register. If reading is initiated on sector 9 (4 in RP01), the index pulse occurs before DTC SRCH COMP sets and DTC INDEX is set by DTC SRCH COMP.

NOTE

The index pulse occurs within 500 ns of the sector pulse for sector 9 (4 in RP01), and not sector zero.

If the heads are advanced when the drive is on the last surface, the drive sends back EOC (End of Cylinder), which terminates operation.

4.11.7 Loading Words

4.11.7.1 Header Words – When DTC READ HEADER sets, header bits are shifted into the SR, and the Bit Counter is incremented (the bit counter is a counter that returns to 0 after six counts). When the Bit Counter returns to zero, the SR is loaded into the LPR (it is actually an exclusive-OR operation, but the LPR has already been cleared). The Byte Counter is incremented each time the Bit Counter returns to 0. When the Byte Counter returns to 0, the Word Counter is incremented. When the Byte and Bit Counters both return to 0, a full header word has been read.

4.11.7.2 Data Words – Data words are loaded in the same fashion as header words except that they are loaded into the AR as well as the LPR. Each time the AR is full, the RP10 issues a device pulse indicating to the channel that data is on the lines. The channel responds with a channel pulse when it is ready to receive another word. DTC SUPR BUF LD is used to prevent the buffer from being loaded during the first byte of data, because the Byte Counter is on a zero. Each parity bit is exclusive ORed into LPR 36.

4.11.8 Transferring Words

4.11.8.1 Write Header – The header words are loaded into the SR and SR BUF directly from the AR. The Bit, Byte, and Word Counters function exactly as they do in reading.

4.11.8.2 Write Data – Each data word is loaded into the AR by a channel pulse, only after a device pulse has been issued to the data channel indicating that the RP10 is ready to receive that word. The LPR is loaded only from the SR BUF.

4.11.9 Writing Headers

The WRITE HEADER command starts with sector zero and writes around the pack. It is impossible to write any sector without first having written sector zero. This is mainly a software function. The controller starts writing on the sector following index and writes 36-bit words continuously until the second sync field has been written, at which time the WRITE DATA mode is entered. The controller writes without parity; if parity were used, the sync field would contain 1s. Thus, because the header is checked for correct parity, the first bit of the first word following the header word appears as the parity bit. The software must calculate parity and supply the correct bit. This operation continues for each sector.

4.11.10 Generating Parity

The PARITY CONTROL flop toggles to a 1 each time 36 bits have been read, except during the sync zones, which are indicated by READ REFUSE (1), READ GAP (1), WRITE HEADER (1), or WRITE GAP (1). The PARITY flop is toggled for each 1 bit read or written. If this flop is on a 0 at the end of 36 bits (PARITY CONTROL → 1), a 1 is written.

During read, the parity bit toggles both the PARITY flop and the LPR 36 flop. This operation is required because LPR 36 (parity bit of LPR word) is read differently than it is written. LPR 36 is written as the parity of the LPR word but is read as the exclusive OR of the parity bits of all the data words.

4.11.11 Terminating

All terminations occur when DTC FINISH is generated. Gate conditions that fire DTC FINISH are listed below by triggers. Each gate indicates a different condition.

CXR SEARCH ERR (1) – Indicates that three index pulses have been received since attempting to read a header and, therefore, the header can not be found or read.

CXR ILL WRITE (1) – Indicates that a write operation was commanded on a write-locked drive.

CXR DISK NOT RDY – Indicates that the controller tried to communicate with a drive that was not ready. A file unsafe condition will cause this termination.

CXR DISK SEC P E – Indicates that a disk sector parity error occurred, and that the stop disable was not set.

CXR DISK WD P E – Indicates that a disk word parity error occurred, and that the stop disable was not set.

IBC CONSET – Indicates a programmed halt.

HCDE SURF DES ER (1) – Indicates that the data transfer command specified a nonexistent surface.

DTC GAP (1)∧(CC ACTIVE (0)∨CC INHIBIT (1)∨CXR PS FAIL) – The combination of these conditions terminates all write operations and normal read operations. DTC GAP prevents termination until the controller is between sectors. It terminates if CC ACTIVE (0) (data transfer complete), CC INHIBIT (1) (overrun or channel data parity error), or CXR PS FAIL (1) (power supply failure) are true. The presence of CC PREVENT TERM 0 prevents termination during a write until the next sector pulse is received. This operation allows erase to stay on longer than write.

DSBC SEL UNIT E O CYL – Indicates that a data transfer did not terminate via the data channel before the drive head register was incremented past its last surface.

CC ACTIVE (0)∧CHN PULS BUF (0) – Indicates that channel access was lost and gained prior to receiving the first channel pulse.

HCDE SEC DES ER (1) – Indicates that the read command specified a nonexistent sector.

Chapter 5
Maintenance

5.1 INTRODUCTION

Maintenance of the RP10 conforms to the accepted maintenance procedures of all electronic equipment presently in use, i.e., an optimum amount of preventive procedures, performed on a routine schedule, can eliminate many costly equipment breakdowns and can forecast failures before they occur. When a specific item does fail, the design of the equipment allows for quick replacement of modular elements, thus restoring the main equipment to service in a minimum of time. A design objective of the RP10 Disk Pack Synchronizer is to provide a dependable and relatively maintenance-free assembly. This chapter contains both preventive and corrective procedures.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled downtime. These tasks consist of visual inspection, operational checks, adjustment, and replacement of marginal components.

The preventive maintenance schedule depends on the environmental and operating conditions that exist at the installation site. Under normal environmental and work-load conditions, the recommended preventive maintenance schedule consists of inspection and cleaning every 600 hours of operation or every 4 months, whichever occurs first. However, relatively extreme conditions of temperature, humidity, dust, and/or abnormally heavy work loads demand more frequent maintenance.

5.2.1 Preventive Maintenance Procedures

Preventive maintenance procedures for the RP01 and RP02 Disk Pack Drives are not included in this manual. For these procedures refer to the Vendor maintenance manual supplied with the equipment.

5.2.1.1 **Mechanical Checks** – Inspect the RP10 periodically as follows:

a. Visually inspect the unit for general condition.

b. Clean the interior and exterior of the rack using a vacuum cleaner or clean cloth moistened in nonflammable solvent.

c. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

5.2.1.2 **Test Equipment Required** – Maintenance activities for the RP10 require the standard test equipment and special materials listed in Table 5-1, in addition to standard handtools, cleaners, test cables and probes. Special test equipment required for any adjustments are given as part of the adjustment procedures.

Table 5-1
Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 453
Clip-on Current Probe	Tektronix	Type P6016
X10 Probe	Tektronix	P6008
Recessed tip, 0.065 in. for wire-wrap terminals	Tektronix	206-052
Hand Unwrapping Tool	Gardner-Denver	500130
Hand-Operated Wire-Wrap Tool with a 26263 bit for 24 AWG Wire and 18840 Sleeve	Gardner-Denver	14H1C
Module Extender	DEC	Type W980
Diagnostic Self-Test Routine	DEC	MAINDEC-10-D5MA MAINDEC-10-D5NB MAINDEC-10-D50B

5.2.1.3 **Electrical Checks** – Perform the power supply output checks described in Table 5-2. Use a multimeter to make the output voltage measurements with the normal load connected. Use an oscilloscope to measure the ripple content on all dc outputs of the supply. Voltage measurements should be made at the logic racks. The +10 and -15 Vdc power supplies are not adjustable; therefore, if any output voltage or ripple content is not within specifications, consider the power supply defective and initiate troubleshooting procedures.

Table 5-2
Power Supply Output Checks

Measurement Terminals at Power Supply Output	Nominal Output (Vdc)	Acceptable Output Range (V)	Maximum Output Ripple (mVrms)
Red (+) to Black (-)	+10	+9.5 to 11.0	800
Black (+) to Blue (-)	-15	-14.5 to -16.0	100

NOTE

This power supply is the Type 728 (728A for 50 Hz) located at the bottom of the RP10 rack.

5.2.1.4 **Electronic Checks** – Perform the following electronic checks.

a. Critical Delays – Check the critical delays in the RP10 every six months to determine that they are still within specified tolerances. These delays are listed in Table 5-3, also included in Table 5-3 is a list of allowable tolerances for each module. Replace or adjust any modules that are found to be out of tolerance.

b. Margins – Check the margins for the RP10 and its companion DF10 every six months. Refer to the Margin Check Paragraph in the PDP-10 KA10 Central Processor Maintenance Manual, Volume 1, and to Tables 5-4 and 5-5.

NOTE

Before margining the RP10, remove power and remove the W505 (PS FAIL) Module at location M02. Replace the module after margining.

Table 5-3
Critical Delay Modules

Drawing No.	Module Type	Signal Name	Location	Nominal Value	Tolerance
DTC-3	R302	DTC TAG LINE STROBE	F30E-M	1 μs	±20%
DTC-3	R302				
IBC-2	R302	IBC SET DAR ETC DLY	H25E-M	500 ns	±20%
IBC-2	R302	IBC LOAD TEST	B20N-V	2 μs	±20%

Table 5-4
DF10 Voltage Margins

Rack Row	Voltage +10V Low	Voltage +10V High	Voltage -15V Low	Voltage -15V High
A	2.5	17.5	-18	-12
B	2.5	17.5	-18	-12
†††C	3.0	17.5	-18	-12
†D	3.5	17.5	-18	-12
E	2.5	17.5	-18	-12
††F	6.0	17.5	-18	-12
††H	6.0	17.5	-18	-12
J	2.5	17.5	-18	-12
K	2.5	17.5	-18	-12
L	2.5	17.5	-18	-12

†The B130 Modules limit the +10V margins of panel D.
††The B685 Modules limit the +10V margins of panels F and H.
†††The R303 Module for NON-EXMEM limits the +10V margins of panel C.

Table 5-5
RP10 Voltage Margins

Rack Row	Voltage			
	+10V		-15V	
	Low	High	Low	High
A	2.5	17.5	-18	-12
B	2.5	17.5	-18	-12
C	2.5	17.5	-18	-12
D	2.5	17.5	-18	-12
E	2.5	17.5	-18	-12
F	2.5	17.5	-18	-12
H	2.5	17.5	-18	-12
†J	6.0	17.5	-18	-12
K	2.5	17.5	-18	-12
L	2.5	17.5	-18	-12
†M	6.0	17.5	-18	-12
††N	6.5	14.0	-18	-12
††P	6.5	14.0	-18	-12
††R	6.5	14.0	-18	-12
†††S	7.5	15.0	-18	-12
†††T	7.5	15.0	-18	-12

†B685 limits +10V margins of panel J.
††W591 and W692 limit +10V margins of panels N, P, and R.
†††B410 limits +10V margins of panels S and T.

5.3 CORRECTIVE MAINTENANCE

The logic description provided in this manual permits the use of standard troubleshooting techniques for isolating the trouble quickly and efficiently. For economical maintenance under most conditions, replace the inoperative module with a spare module and return the defective module to DEC for repair or replacement.

5.3.1 General Corrective Procedures

Before beginning troubleshooting procedures, make certain that the processor portion of the PDP-10, the DF10, and I/O Interface are operating properly. Refer to the specific maintenance manual to determine the status. Also examine the maintenance log to determine if the fault has occurred before and note what steps were taken to correct the condition. Note also if a cyclic condition has occurred. Visually inspect the physical and electrical security of all cables, connectors, modules, and wiring. Check the indicator lamps for operation and their glass covers for cleanliness. In particular, check the security of ground connections between racks. Faulty grounds can produce a variety of faults.

5.3.2 Diagnostic Testing

DEC provides special diagnostic programs (MAINDECs) to assist in localizing faults within the equipment. Functionally, the programs fall into two categories: test and reliability. Test programs isolate genuine go/no-go type hardware failures that are easily recognizable, while the reliability programs isolate failures that are more difficult to detect because they are marginal in nature and/or occur infrequently or sporadically. The family of test programs are written so that, when run successively, they test the equipment beginning with small portions of the hardware and gradually expand until they involve the entire machine. To accomplish this, they are built around instructions and portions of instructions whose demands on equipment capabilities progress from simple transfers and skips to the most involved data manipulations and computations. As portions of the system are proven operable, they become available to succeeding tests for use in checking out unproven portions of the machine.

To perform a diagnostic routine on the RP10 alone, run tests MAINDEC-10-D5MA and MAINDEC-10-D5NB. If the RP10 is operating correctly, both tests should run without failure.

5.3.2.1 Vibration Tests – Many malfunctions can be located by performing a voltage margin check while running diagnostics. The RP10 should be margined while running D5MA or D50B. The associated DF10 should be margined while running D5NB. In addition, a vibration test may be performed while margining the RP10 and DF10 together.

5.3.3 Adjustment Procedures

The following adjustment procedures must be performed when it has been determined by diagnostics and trouble-shooting techniques that a specific element is at fault but does not need replacement.

5.3.3.1 Read Data Separator Calibration – If parity errors are occurring from random drives, surfaces, or bits, the read data separator (RDS) is probably at fault. This failure can be caused by a bad module or by poor alignment. If it is determined that a module is at fault, the module should be replaced with one known to be good; otherwise, the following procedure should be performed. The purpose of this calibration procedure is to adjust the variable elements of the RDS so that data being read from the disk pack drive is correctly separated into data bits and clock bits under all combinations of bit shift and speed variations from the drive, and worst case circuit conditions in the RDS.

All delays used in the portion of the circuitry required for operation from RP02 drives are also active when RP01 drives are being used. Therefore, all adjustments for operation with an RP02 are always required, even if RP01 drives alone are to be used.

The calibration procedure is carried out using the crystal clock in the controller, and a drive is not required in order to set up the read data separator. The jumpers connected in steps 2 and 3 of the procedure ensure that all necessary signals are present.

Equipment required for this calibration procedure is as follows:

a. Dual-trace oscilloscope, Tektronix Type 453, Tektronix Type 454, or equivalent.

b. Oscilloscope probes fitted with short (i.e., 3-in. or less) grounding leads.

c. Jumper leads, 5 red jumpers (4-in.) and 1 yellow/white jumper (24-in.).

NOTE

The differential delay between probes should be less than 2 ns. This should be checked by connecting both probes to a convenient waveform (e.g., T22 H), setting the oscilloscope time base to 5 ns/div. (10 ns/div., if using 453) and measuring the delay between the channels at the -1.5V level.

The following calibration procedure must be strictly adhered to. Make all adjustments as precisely as possible.

Step	Procedure
1	Remove Module Type B152 at location J29.
2	Connect the following pins to ground: *a.* E32 (DTC RP01 L) *b.* C10F (DTC READ HEADER (1) H) *c.* L22N (DTC WRITE HEADER (1) H) *d.* L24N (DTC READ CLOCK PULSE L) *e.* S15J (Provides RDS SYNC FIELD ENB L)
3	Connect K24U (CRYSTAL CLOCK OUTPUT, 400 ns period) to S25J (MPX RAW DATA H).
4	Set oscilloscope to trigger internally from channel 1; set vertical sensitivity to 1V/div. and time base to 50 ns/div. negative trigger.
5	Connect channel 1 to T22H and adjust lower potentiometer on module B410 in location T22 until negative-going pulse width on oscilloscope is 50 ns measured at -1.5V points.
6	Connect S25E (MPX RAW DATA H) to ground, place channel 1 on T29V, set for positive trigger, and adjust module B312 at location T29 until width of the pulse to ground is 50 ns measured at -1.5V points. Remove ground on S25E.
7	Connect T22V to ground.
8	Connect channel 1 to T22H. Set time base for 100 ns/div. Adjust upper potentiometer on module B410 in location T22 until pulses occur at intervals of 200 ns. Remove ground on T22V.
9	Connect channel 1 to S24L and channel 2 to S24V. Adjust B312 at location S24 until the delay between S24L and S24V is 80 ns.
10	Connect channel 1 (only channel 1 is needed) to S28P and adjust B312 at location T25 until the square-wave seen at S28P is 200 ns to -3V and 200 ns to ground.
11	Set oscilloscope to 1V/div. Set to negative trigger, internally from channel 1. Set the time base to 10 ns/div. for A453 and 5 ns/div. for A454.
12	Connect channel 1 to S32M and channel 2 to T30H. Adjust B312 in location S24 until the falling edge of channel 1 waveform is aligned with the rising edge of channel 2. Measure at -1.5V (see Figure 5-1).

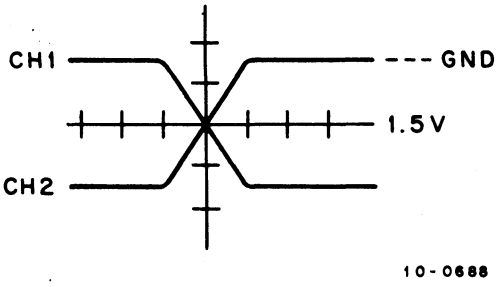


Figure 5-1 RDS Waveform No. 1

Step	Procedure
13	Set time base 20 ns/div. and connect channel 1 to M30S. Adjust calibrate control on time base until the pulses are exactly 10 divisions apart on the oscilloscope face measured at -1.5V points. (If the pulses cannot be adjusted to 10 div apart, repeat using 50 ns/div. range setting.)
	NOTE **The time base is now calibrated on this range to be 20 ns/div. Do not move the calibrate control or the range (time/div) control for the remainder of the RP02 procedure unless instructed to do so.**
14	With channel 1 connected to T24D (RDS ERR A (0) H), and channel 2 connected to T24N (RDS ERR B (0) H), and time base set for 20 ns/div, adjust the upper potentiometer on module B410 in location T22 until the waveforms seen on channel 1 and channel 2 are exactly the same. ("Exactly", in this context means within the limits of oscilloscope resolution and operator ability.)
15	Connect channel 1 to S32M (RDS CLOCK WIND (0) L), set for negative trigger, connect channel 2 to S32L and adjust B312 module at location T25 until the delay between the negative-going edge of channel 1 and channel 2 is equal to 105 ns measured at 1.5V point (see Figure 5-2).

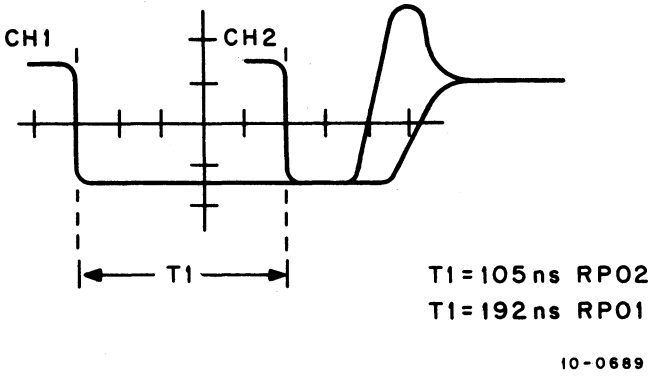


Figure 5-2 RDS Waveform No. 2

16	Remove the following jumper to ground: E32D

Step	Procedure
17	If the RP01 is not to be used with the system, remove the following jumpers: *a.* C10F to ground *b.* L22N to ground *c.* L24N to ground *d.* S15J to ground *e.* K24U to S25J Replace the module Type B152 at location J29. **NOTE** **This completes the calibration of the RP02 section of the RDS.**
18	If the RP01 is to be used with the system, proceed as follows: *a.* Jumper point E32H to ground. *b.* Check that the following points are connected: C10F to ground L22N to ground L24N to ground S15J to ground K24U to S25J *c.* Check that the module Type B152 is removed from location J29.
19	Set oscilloscope to trigger internally from channel 1, vertical sensitivity set to 1 V/div, and time base on 50 ns negative trigger.
20	Connect channel 1 to S22H and adjust lower potentiometer on module B410 in location S22 until pulse width on oscilloscope is 50 ns measured at the -1.5V points.
21	Connect channel 1 to S32L (RDS DATA IN L), connect channel 2 to T27N and adjust module B312 in location T26 until delay between channel 1 and channel 2 is 250 ns.
22	Connect S22V to ground.
23	Connect channel 1 to S22H. Set oscilloscope time base to 200 ns/div. Adjust upper potentiometer on module Type B410 in location S22 until pulses occur at 400 ns intervals. Remove S22V from ground.
24	Connect channel 1 to S28P and adjust B312 at location T26 until the square-wave seen at S28P is 400 ns to -3V and 400 ns to ground.
25	Set time base on oscilloscope to 50 ns/div. Connect channel 1 to M30S and adjust calibrate control on the oscilloscope time base until the pulses are exactly 10 divisions apart on the oscilloscope face measured at the -1.5V points. **NOTE** **The time base is now calibrated on this range to be 40 ns/div. Do not move the calibrate control or the range (time/div.) control for the remainder of the RP01 procedure unless instructed to do so.**

Step	Procedure
26	Connect channel 1 to T24D and channel 2 to T24N. Set time base for 100 ns/div. and adjust the upper potentiometer on module B410 in location S22 until the waveforms seen on channel 1 and channel 2 are exactly the same.
27	Connect channel 1 to S32M (RDS CLOCK WIND (0) L) set for negative trigger. Connect channel 2 to S32L and adjust B312 module in location T26 until the negative-going edges of channel 1 and channel 2 are 192 ns apart. Measure at the -1.5V point (see Figure 5-2).
	NOTE **This completes the calibration of the RP01 system.**
28	Remove the following jumpers: *a.* E32H to ground *b.* C10F to ground *c.* L22N to ground *d.* L24N to ground *e.* S15J to ground *f.* K24U to S25J
29	Replace module Type B152 in location J29.

The following adjustments are performed in the preceding calibration procedure:

Step 5 adjusts the output pulse from B410 to a width of 50 ns.

Step 6 adjusts the delay line in T29 so that incoming pulses, which are 70 ns ± 15 ns, are standardized to a 50 ns pulse width before being fed to the remainder of the RDS circuitry.

Step 7 adjusts the variable input resistor of the B410 clock to a setting at which a phase lock condition can be obtained in the phase lock loop. This phase lock loop consists of the B410 voltage controlled oscillator, phase error comparator flip-flops (called RD RDS ERR A and RDS ERR B), and a differential error amplifier and filter G589 or G590.

Step 10 adjusts the delay which is used to set the data and clock pulses correctly with respect to their gating waveforms. The gating waveforms are generated by the flip-flops S28 and T32, and ensure that all data bits are gated out of S32H (RDS DATA OUT H), and all clock bits are gated out of S32N.

Step 14 adjusts the width of the gating waveform which is used to gate the data bits and clock bits.

Step 15 finally adjusts the setting of the variable input resistor in B410 so that the phase lock loop achieves its lock with a phase error of zero degrees between the internal oscillator (B410) and the incoming serial stream of data and clock bits.

Step 20 adjusts the width of the output pulse from B410 to 50 ns.

Step 22 adjusts the variable input resistor of B410 to a setting which allows a phase lock condition to be established between the B410 internal oscillator and the incoming clock and data bits.

Step 26 provides a final adjustment to the variable input resistor of B410 to establish the optimum phase lock condition between the incoming serial stream of data and clock bits and the B140 internal oscillator.

Step 27 adjusts the delay used to set the data bits and clock bits correctly to their respective gating waveforms.

5.3.4 General Troubleshooting Guides

The following paragraphs contain suggested methods of correcting recurring problems. Also, refer to DEC Field Service Manuals and DEC Tech Tips published periodically.

5.3.4.1 Disk Pack Compatibility – To determine if two disk packs are compatible, run CTEST and swap packs as directed. If any errors occur, the drives are considered to be incompatible.

NOTE

Before running compatibility tests, the drive should have passed all diagnostics with a pack formatted on that drive.

If the drives are found to be incompatible, they should be aligned as described in the Vendor Maintenance Manual.

CAUTION

C.E. (Customer Engineering) Packs are *not* indestructable. Their specially recorded track can be destroyed rendering the pack unusable. Extreme care should be exercised in their use. C.E. Packs should only be used when aligning heads or checking head alignment. They should *never* be used for any other troubleshooting or alignment procedures.

5.3.4.2 Proper Use of C.E. Packs – The following procedures should protect and may extend indefinitely the usable life of C.E. Packs. For both RP01 and RP02:

Step	Procedure
1	Do not connect the tester until all power has been removed from the drive.

CAUTION

Before cables are removed, all power must first be removed from all drives (via S1) as well as from the RP10. Failure to do so can result in damage to the steering diodes in the power sequencing network.

2	Set the drive to READ ONLY condition.

CAUTION

Always disable write amp by switching to READ ONLY before using C.E. Packs to insure safety of specially recorded elliptical tracks.

3	Apply power to drive the S1, then apply power to tester.
4	Press UNIT DESELECT on tester.

NOTE

This step is necessary to prevent accidental writing over the test track, which would effectively destroy its usefulness.

For RP01 only:

Step	Procedure
1	Remove HEAD SELECT (switch 4 on tester).
2	Remove all head plugs.
3	Insert head alignment plug into desired head socket.
4	Mount the C.E. Pack on the drive.

CAUTION

Whenever a different head is to be tested, or a head plug removed or inserted, always *remove* HEAD SELECT level (switch 4 on the tester). It is also recommended to position off cylinder 73 when repositioning the Head Alignment Plug.

For RP02 only:

Step	Procedure
1	Note that the Head Alignment Plug is not used with the RP02.
2	It is not necessary to remove a head plug while the C.E. Pack is on the drive.

Head and Pack Thermal Equilibrium:

Step	Procedure
1	Before heads are adjusted, thermal equilibrium procedures should be followed. The temperature stabilization cycle, which assures standard operating temperature during head alignment, consists of first running the drive with C.E. Pack installed and all covers on for one hour and 15 minutes, then running the drive with C.E. Pack installed and the two top covers off for an additional 20 minutes before attempting alignment.
2	Use *only* the special tools for maintenance (i.e., beryllium screwdriver, torque wrench, etc).

NOTE

All RP01 and RP02 Vendor Manuals are serialized and contain specific information pertaining to that drive (i.e., ECO's, updated prints, etc). Each manual must be maintained as Engineering Documentation.

When a C.E. pack is used on a Memorex drive, the READY signal will not occur. Therefore, jump B05 test point three to ground. This indicates to the drive logic than an index pack is being used, instead of a sectored pack.

5.3.4.3 Search Errors – Search Errors can be caused by a variety of conditions. A known formatted pack should be run. If search errors occur on only specific surfaces of a drive, the read logic should be checked. If search errors occur from all drives, the RDS operation should be checked. To do this, sync off J09M (DTC SEARCH) going high and view L21N (DTC READ BIT). This bit should be on a 1 for approximately 100 μs for RP02s and for 250 μs for RP01s. If DTC READ BIT is not on a 0 after 100 μs (250 μs for RP01), or if it never transitions to a 1, the separator is at fault. However, if READ BIT performs correctly the Header Compare, LPR, Header Read Control, or Shift Register is at fault.

5.3.4.4 Parity Errors – If parity errors occur from one drive, the read or write logic in that drive should be checked. If all parity errors occur from word 0, the RDS Sync Field Enable is probably not being produced. If errors do not exhibit a repetitive pattern, the RDS is at fault. If an AR bit is faulty, this is particularly easy to see and scope in local mode. Remember that the controller tries to read headers three times before terminating; therefore, the separator's operation can be quite marginal before search errors occur.

5.3.4.5 Failure to Restore – If the Memorex drive fails to restore, the logic can be checked by moving the actuator by hand. Proceed as follows:

Step	Procedure
1	Connect the off-line tester.
2	Remove power from bobbin.
3	Install a jumper to prevent T2 from becoming true (Seek Incomplete).
4	Wiggle head assembly at full forward stop. This gives a forward velocity signal that is needed to complete the restore sequence. The code 202 should now be seen in the cylinder address lights (force count).
5	Move the coil backwards by hand. Observe that the address register counts down.
6	When address reaches 0, the detent should pick.

NOTE

The address might not reach 0 because the pull may not be smooth causing a tooth to be counted more than once.

5.3.4.6 Disk Pack Reliability Test Map Limitations – The MAP routine in MAINDEC 10-D50B cannot guarantee detection of all weak or bad spots on the disk pack surface. The best procedure for developing an initial list of questionable or faulty disk pack sectors is to note all failures relating to data errors during acceptance and to enter the MAP data manually using the manual entry feature of D50B's MAP routine. The MAP routine will write the map data onto the appropriate sectors of the pack for Monitor reference.

5.3.4.7 Cleaning – For trouble-free operation take the same environmental care as is indicated for tapes (refer to Paragraph 6.10 in the PDP-10 *System Reference Manual*). In particular, the heads and the packs should be kept clean.

Materials and equipment needed for cleaning are as follows.

a. Lint-free wipers (cloth or paper), such as Kimwipes Type 900-S, Stock No. 3415 (about 8 x 5 in.)

b. Isopropyl alcohol, at least 90%, such as Merck or NF (99% by weight) or Lilly (91% by volume)

NOTE

Store alcohol in its original container or in a glass jar.

c. Q-tips and pipe cleaners

d. Wooden tongue depressors, 6 x ¾ in.

NOTE

Do not use plastic depressors (the alcohol softens them).

e. A high-intensity light or other strong light source

f. A piece of white cardboard or stiff paper (8½ x 11 in.).

Inspect the heads for dirt accumulation at least twice monthly (weekly for around-the-clock operation). When necessary, clean them carefully with a Q-tip soaked in alcohol, and clean out the two holes in each head with a pipe cleaner, also soaked in alcohol. Keep all cabinet and pack filters clean and fresh. Dirty heads can be caused by poor head flight due to poor air flow through the pack or cabinet. Always replace a single head that collects dirt while others in the same drive remain clean.

Do not clean all of the packs at an installation just for the sake of cleaning them. If a pack is subject to random errors, or if vital information that is not duplicated elsewhere cannot be retrieved, and the problem is not alleviated by cleaning the heads, then clean the pack. In any event, depending on environmental conditions, test all packs every few months by cleaning a couple of surfaces at random in each; clean all surfaces in any pack in which dirt is discovered.

To clean a pack, mount it on a drive from which the upper case panels have been removed or on a free-standing spindle mechanism that allows the pack to be turned by hand with the cover removed. Place the light with the white cardboard as a background so that plenty of light shines into the pack. Follow this procedure for cleaning each surface.

Step	Procedure
1	Position the light so the surface is clearly visible.
2	Wrap a fresh wiper around a depressor with wiper extending 3/8 in. beyond the wood at one end.
3	Soak one side of the wrapped depressor with the alcohol (be sure to wet the full width of the depressor).
4	Spin the pack by hand at 40-60 rpm (use the flat top surface of the plastic bezel on the top of the pack).
5	With the pack spinning, insert the prepared depressor with the protected end toward the center, and press the wet side against the surface. Maintain the pack spin while applying about 5-10 pounds pressure against the surface; wet the surface across the full width of the tracks. The pressure may be lightened as the surface dries, but be sure to keep the wiper on the surface with the pack spinning until the surface is completely dry and has a high gloss. Keep the pack spinning while removing the depressor, and check the wiper for dirt.
6	Inspect the surface carefully for scratches. If a scratch corresponds in position to a bad sector as determined by the program, then further cleaning is unlikely to make the sector usable.

WARNING

Do *not* attempt to use the drive motor when cleaning a pack. Always turn drive power off and spin the pack manually.

Do not clean a pack if either the pack or the alcohol is below 40°F (otherwise water vapor might condense on the surface).

Chapter 6
Drawings

6.1 GENERAL

The RP10 engineering drawings and an accompanying signal glossary are included in Volume 2 of this maintenance manual. A list of engineering drawings is provided in Table 6-1.

Table 6-1
RP10 Engineering Drawings

Number	Title
A-ML-RP10-A	RP10 Master Drawing List
D-DI-RP10-0-1	RP10 Drawing Index List
D-UA-RP10-0-0	RP10 Unit Assembly
A-PL-RP10-0-0	RP10 Parts List
A-PL-RP10-0-MC	Parts List Disk File Interface
A-PL-7006194-0-0	Wired Assembly RP10
A-PL-7006195-0-0	Cable Set RP10
D-FD-RP10-0-FCA	Flow Chart Asynchronous and Sector Counters
D-FD-RP10-0-FCCC	Flow Chart Channel Control
D-FD-RP10-0-FCCI	Flow Chart Channel Interface
D-FD-RP10-0-FCDC	Flow Chart Disk Control
D-FD-RP10-0-FCE	Flow Chart End
D-FD-RP10-0-FCL	Flow Chart Local
D-FD-RP10-0-FCM1	Data Transfer Control Micro 1
D-FD-RP10-0-FCM2	Data Transfer Control Micro 2
D-FD-RP10-0-FCRI	Flow Chart Register Interconnections
D-FD-RP10-0-FCRW	Flow Chart Read/Write
D-FD-RP10-0-FCS	Flow Chart Start
D-FD-RP10-0-FCSC	Flow Chart Search
D-FD-RP10-0-FCWH	Flow Chart WR Headers and Data
D-BS-RP10-0-AR	Assembly Register
D-BS-RP10-0-ARD	Assembly Register Data Gate
D-BS-RP10-0-CC	Channel Control
D-BS-RP10-0-CXR	Condition Register
D-BS-RP10-0-DAR	Data Address Register
D-BS-RP10-0-DSBC	Disk Signal Bus Connectors
D-BS-RP10-0-DTC	Data Transfer Control

Table 6-1 (Cont)
RP10 Engineering Drawings

Number	Title
D-BS-RP10-0-HCDE	Header Compare and Designation Error
D-BS-RP10-0-IBC	I/O Bus Control
D-IC-RP10-0-IC	Interconnecting Cables
D-IC-RP10-0-INDC	Indicators
D-BS-RP10-0-IOB	IOB Transmitter
D-BS-RP10-0-IOBD	IOB Data Receiver
D-BS-RP10-0-LPR	Longitudinal Parity Register
D-BS-RP10-0-MPX	Multiplexer
D-BS-RP10-0-RDS	Read Data Separator
D-BS-RP10-0-RDS	Read Data Separator Calibrations
D-BS-RP10-0-SC	Sector Counter
D-BS-RP10-0-SCB	Sector Counter Buffer
D-BS-RP10-0-SCCC	Sector Counter Control Pulses
D-BS-RP10-0-SCM	Sector Counter Multiplexer
D-BS-RP10-0-SR	Shift Register
D-IC-RP10-0-SWP	Switch Panel
D-CL-RP10-0-TERM	Pulse and Level Terminations
D-BS-RP10-0-WDC	Word Counters
D-MU-RP10-0-AD	Module Utilization A-D
D-MU-RP10-0-EJ	Module Utilization E-J
D-MU-RP10-0-KN	Module Utilization K-N
D-MU-RP10-0-PT	Module Utilization P-T
D-IC-RP10-0-3	Wiring Power DC and AC
D-AD-7006194-0-0	Wired Assembly (RP10)
C-AD-7006195-0-0	Cable Set (RP10)
D-SP-RP10-0-CEPT	CE Pack Tracks

READER'S COMMENTS

RP10 DISK PACK SYNCHRONIZER
MAINTENANCE MANUAL
DEC-10-H5EC-D (1)

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