RON MOOPHEAD

Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-9
Maintenance Manual

RF09/RS09 DECDISK SYSTEM

Volume I

DEC-09-H9ZA-D

RF09/RS09
DECDISK SYSTEM MAINTENANCE MANUAL VOLUME 1

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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Chapter 1
DECdisk System

1.1 INTRODUCTION

The DECdisk system is a computer peripheral that stores digital data on fixed-head rotating disks in a serial format. The data can be randomly accessed at selectable speeds and, when necessary, protected from overwriting.

1.1.1 DECdisk System Description

DECdisk is a peripheral designed for the PDP-9, PDP-9L, and PDP-15 computers. Each DECdisk system consists of a controller and from one to eight disk drives. The controller connects to the computer's I/O Bus and communicates to the processor for control and status information. For data information, the controller communicates to memory through the data channel. Each disk drive connects to the controller through a parallel disk bus. Both control and data information pass through the parallel disk bus.

There are two models of controllers and one type of drive. Table 1-1 lists these models and the computers on which they are used. Figure 1-1 illustrates the system configurations. This manual is primarily concerned with the RF09/RS09 DECdisk system used with the PDP-9 and PDP-9L computers.

Table 1-1
DECdisk Model Numbers

Controller Model	Disk Drive Model	Related Computer System
RF09	RS09	PDP-9, PDP-9L
RF15	RS09	PDP-15

1.1.2 Storage of Digital Data on Fixed-Head Rotating Disks

Each RS09 disk drive consists of a rotating disk, a hysteresis synchronous motor, a matrix of 128 fixed read/write heads, and the electronics required to drive the heads (see Figure 1-2).

The 128 magnetic read/write heads ride on the surface of the rotating disk, which is nickel-cobalt plated. Each read/write head covers a separate track on the nickel-cobalt surface; thus, disk action is similar to the operation of many circular tapes running simultaneously in continuous loops.

Each track on the disk can store 2048 eighteen-bit data words. As a track fills, the system automatically moves to the next track. The disk rotates at 1800 rpm (60 Hz power) and can, therefore, transfer a word every 16 μs.

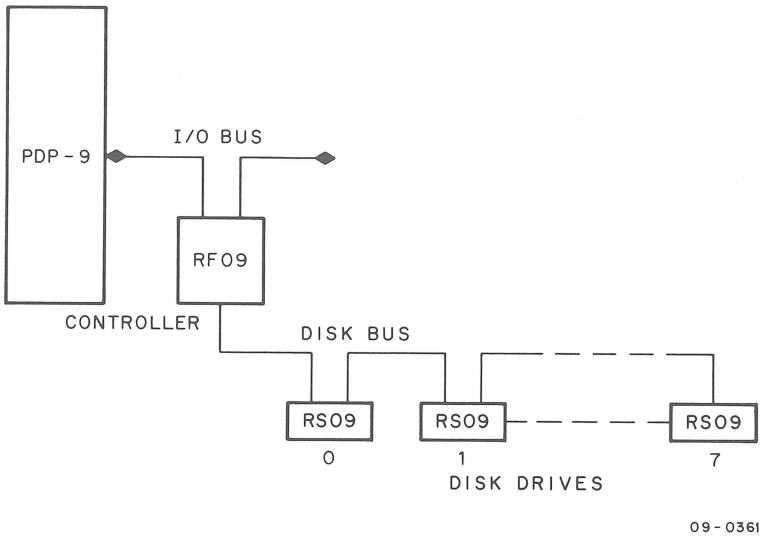


Figure 1-1 DECdisk System Configurations

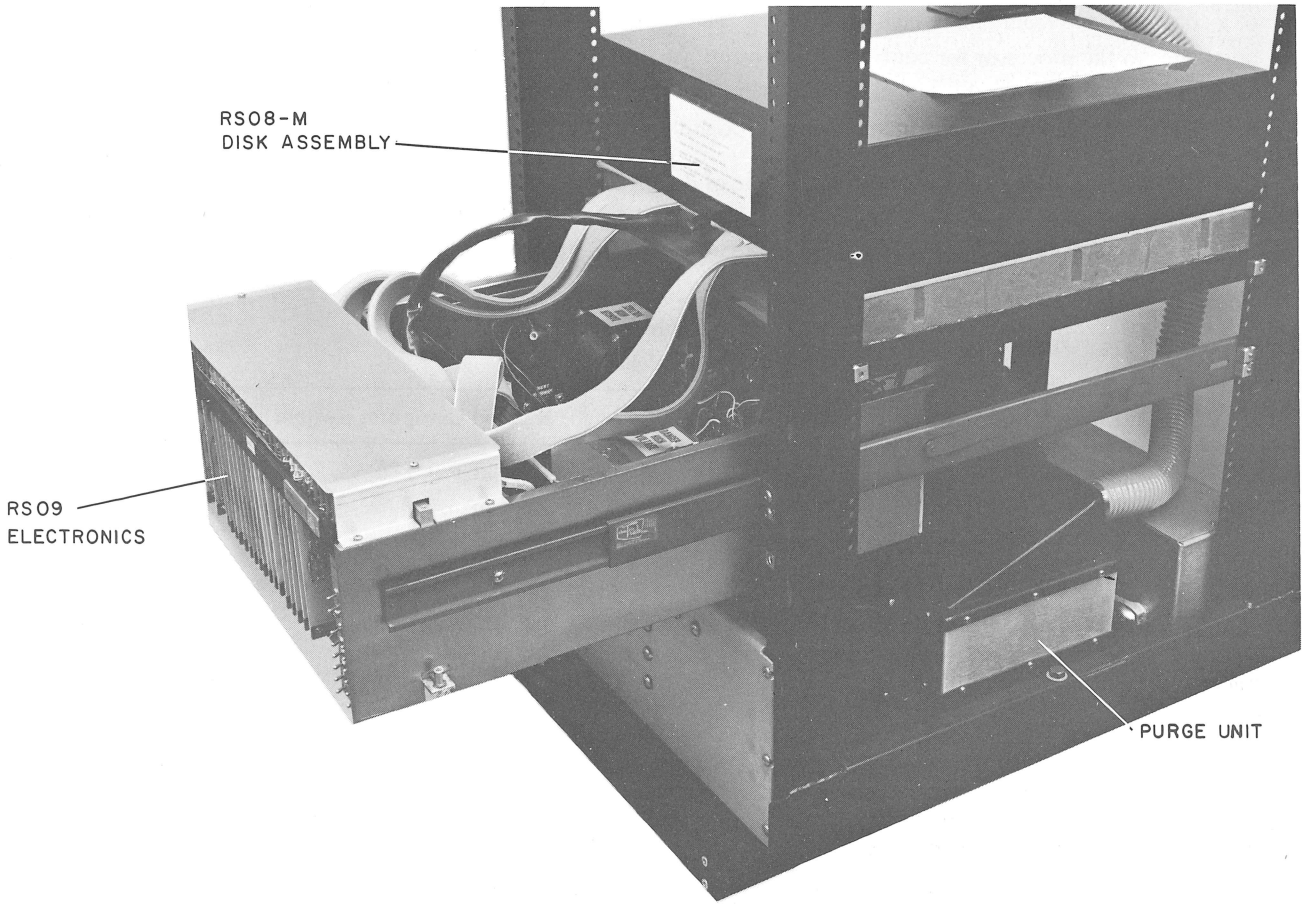


Figure 1-2 RS09 Disk Drive

The storage capacity of each disk is 262,144 words (2048 words x 128 heads). Total system capacity is 2,097,152 words (8 disk drives x 262,144 words).

1.1.3 Storage of Data in a Serial Format

The DECdisk system stores the data on each disk in a serial format. The serial format causes the bits of each word to be recorded one at a time along a single track, rather than all at once across eighteen tracks. Therefore, only 1 of a possible 128 data heads is actively reading or writing data at a single time.

1.1.4 Random Accessing of Data

The DECdisk is a random-access storage system. Each disk is logically segmented into 2048 slices or words, and each slice is preassigned a number or address from 1 to 3777_8. The controller, in response to the computer, can select at random any track of a disk and any address along that track to read or write a word (see Figure 1-3).

1.1.5 Data Accessing at Selectable Speeds

There are three speeds (switch-selected by the operator) at which data can be transferred between the disk surface and the computer. The highest speed transfers a data word with each successive address, covering a track in one revolution. The medium speed transfers every second word of a track in the first revolution, and then transfers the alternate words on the same track during the second revolution. The slowest speed takes four revolutions to cover a complete track. Once the operator has selected the desired speed, the controller hardware controls proper interleaving of the words. However, the data should be read back at the same speed at which it was written to avoid scrambling the data.

1.1.6 Data Protection from Over-Writing

Sixteen switches are available on each RS09 drive to protect disk-stored data. Each switch can inhibit the computer from over-writing on eight separate tracks.

1.2 DECDISK OPERATION

Information flow within the DECdisk system is determined by the recording format on the disk surface and the internal architecture of the controller. The following paragraphs describe the operation of the disk recording format and the system architecture.

1.2.1 Disk Surface Recording Format

As previously described, 128 read/write heads covering 128 concentric tracks ride on each disk surface. The circumference of each disk is logically divided into 2048 data segments or addresses, and in each segment of any track a complete 18-bit computer word can be stored. A 2049th segment called a gap is provided to give the heads time to switch tracks. This segment has no address and stores no data or timing tracks. It is used as a marker to notify the controller each time a revolution has been completed.

Each data segment must store, in addition to its data word, two control bits; and each disk, in addition to its data tracks, must contain six control tracks. The control bits are recorded with the data bits; the control tracks are prerecorded on the disk surface at the factory. Figure 1-4 illustrates the location of these bits and control tracks.

Data is recorded serially on each track in 20 bit words; 18 bits are data bits, and two bits are parity and guard bits, respectively. Each 20-bit word unit is identified by an address that is prerecorded on a special track before the disk is connected to the computer in the plant. This address is recorded serially on the B track (see Figure 1-4)

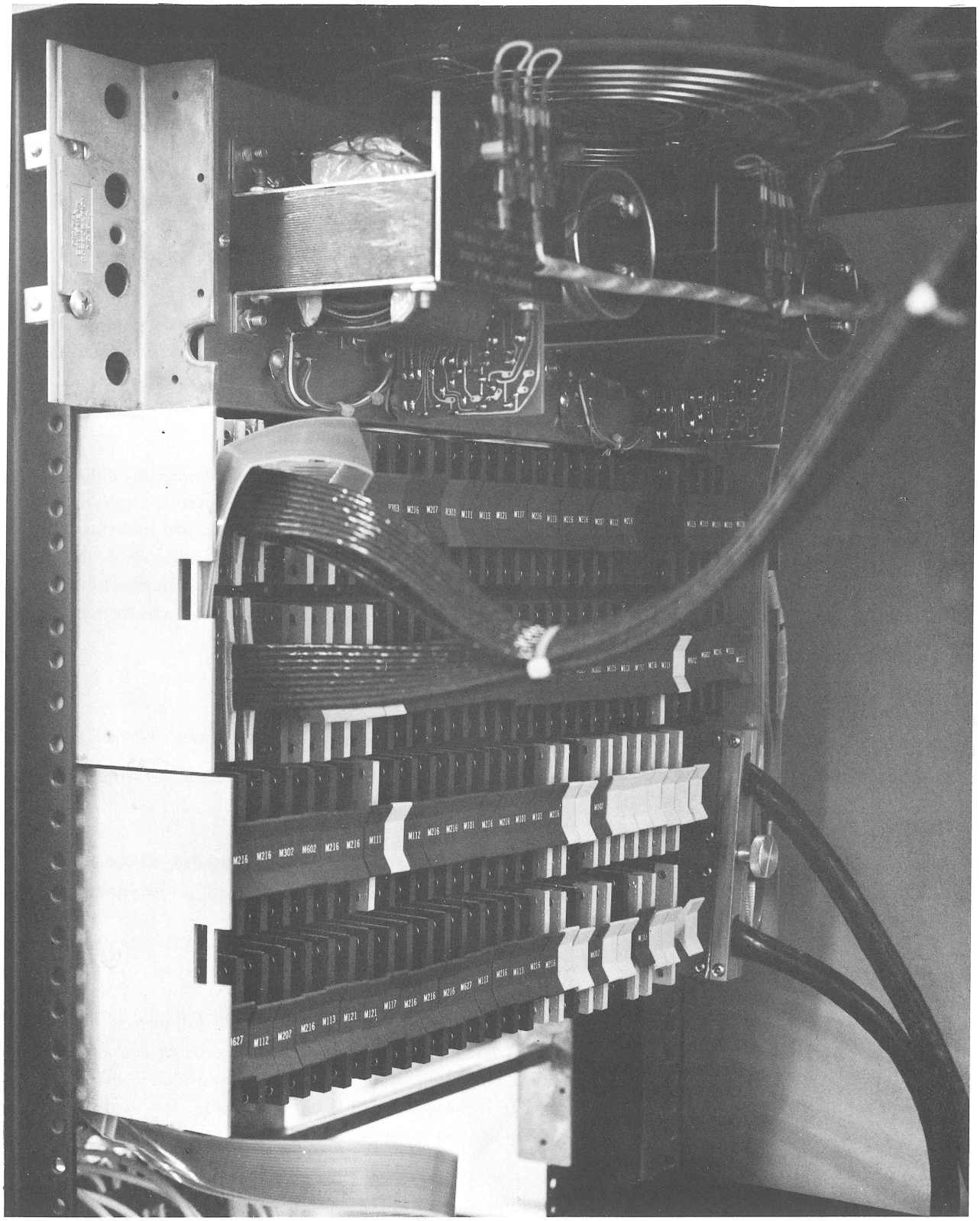


Figure 1-3 RF09 Controller

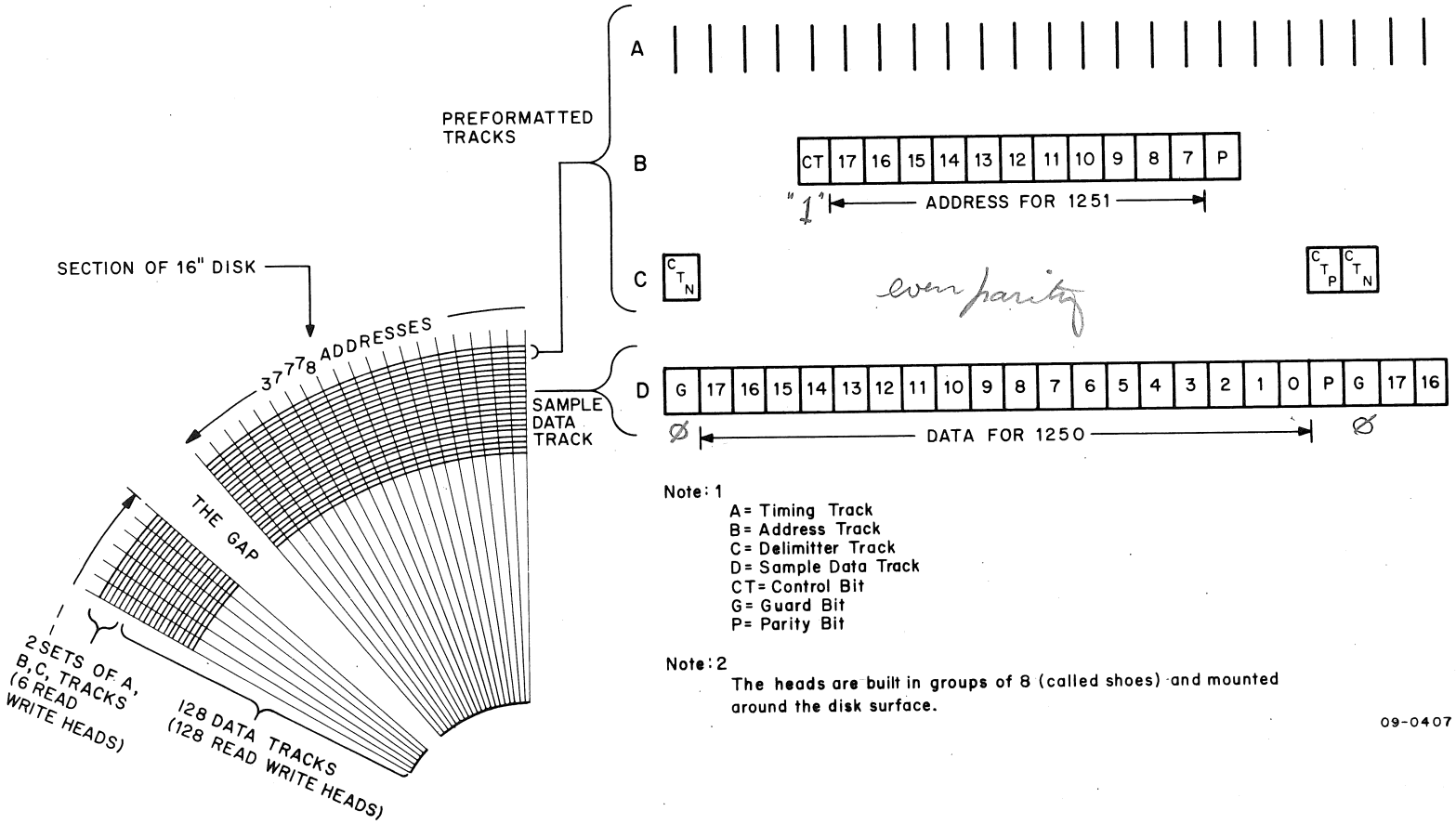


Figure 1-4 Disk Surface Recording Format

exactly one word before the word with which it is associated. The controller can then assemble and identify the address before the heads reach the word itself. Each address is 13 bits long; 11 bits supply addressing data, 1 bit is a control bit, and 1 bit is a parity bit.

There are five additional prerecorded tracks on the disk surface. The A track is a prerecorded track with pulses 800 ns apart that are used to strobe data into or out of the data tracks. The C track is a track used to delimit each word unit. The controller relies on the C track to signal when a word has been assembled or written. The controller can then notify the computer to accept the word read or to supply another word to be written. Each of the three prerecorded tracks described – the A, B, and C tracks – are copied on three spare tracks that are used if one of the original tracks is accidently erased in the field. If the spare tracks are damaged, all the timing tracks can be rewritten in the field with a special timing track writer (see Chapter 7).

1.2.2 DECdisk Architecture

In this manual, the DECdisk system architecture is presented in three parts; the Control section, the Data Transfer section, and the Maintenance section (shown in Figures 1-5, 1-6, and 1-7 and 1-8, respectively). Through the Control section, the software operating system initializes the controller by selecting the disk drive (RS09) to be used, the track address within that drive (Data Track Matrix) to be used, and the first address within the track to be used. One of three functions is then selected: READ the disk; WRITE on the disk; or WRITE CHECK what has already been read or written. The Data Transfer section assembles the word off the selected track for a READ operation, or writes the word bit by bit onto the track during a WRITE operation. This section also notifies the computer when it has assembled a word or needs another word to write, and the data is transferred through the three-cycle data channel. When the last word has been transferred, the computer issues an overflow pulse to the controller. An interrupt then occurs, and transfers are stopped. The Maintenance section simulates either the disk surface head signals or RS09 output signals and is used exclusively for testing the DECdisk system.

1.2.2.1 The Control Section – The block diagram of the Control section in Figure 1-5 shows 11 relatively independent sections. Some of these sections contain registers, and the bits of these registers are numbered according to the position they occupy when they are read from or into the accumulator of the Central Processor.

Three of these registers – the Disk Number, the Track Address, and the Word Address – are set by the software system to select the disk (one of a possible eight), the track within that disk (the read/write head matrix), and the starting address within the track. Each time a word is transferred, the word address is automatically incremented by one to prepare for the next word. When the Word Address Register overflows, the track address is automatically incremented; and when all tracks have been exhausted, the Disk Number Register is incremented. These registers continually step from word to word, track to track, and disk to disk until the system has been covered.

NOTE
Incrementing occurs during a valid operation only.

After the system has been covered, the computer is notified that it has run out of disks. The dead space (gap) shown in Figure 1-4 is used to give the controller time to switch tracks when it needs to do so.

The Word Address Register is constantly being compared to the contents of the Segment Register, which in turn is sampling the "B" or address track. When the "C" or delimiter track indicates that a valid address in the Segment Register, the word address is compared with the assembled address; and if the two match, an ADDRESS OK signal is passed to the data transfer logic. This signal informs the data transfer logic that the data

NOTES:

1. The READ/WRITE data heads are mounted on shoes in groups of 8 and each shoe is mounted on a card. The cards are mounted around the underside of the disk so that each head covers a different track. The timing card has 1 shoe.
2. The cards are cabled from the RS09 READ/WRITE logic and selection matrix, which in turn cable to the controller.
3. Each RS09 has both input and output cable slots. The signals are cabled in parallel from drive to drive to a maximum of 8.
4. The track address register selects the head according to the folowing bit configuration:

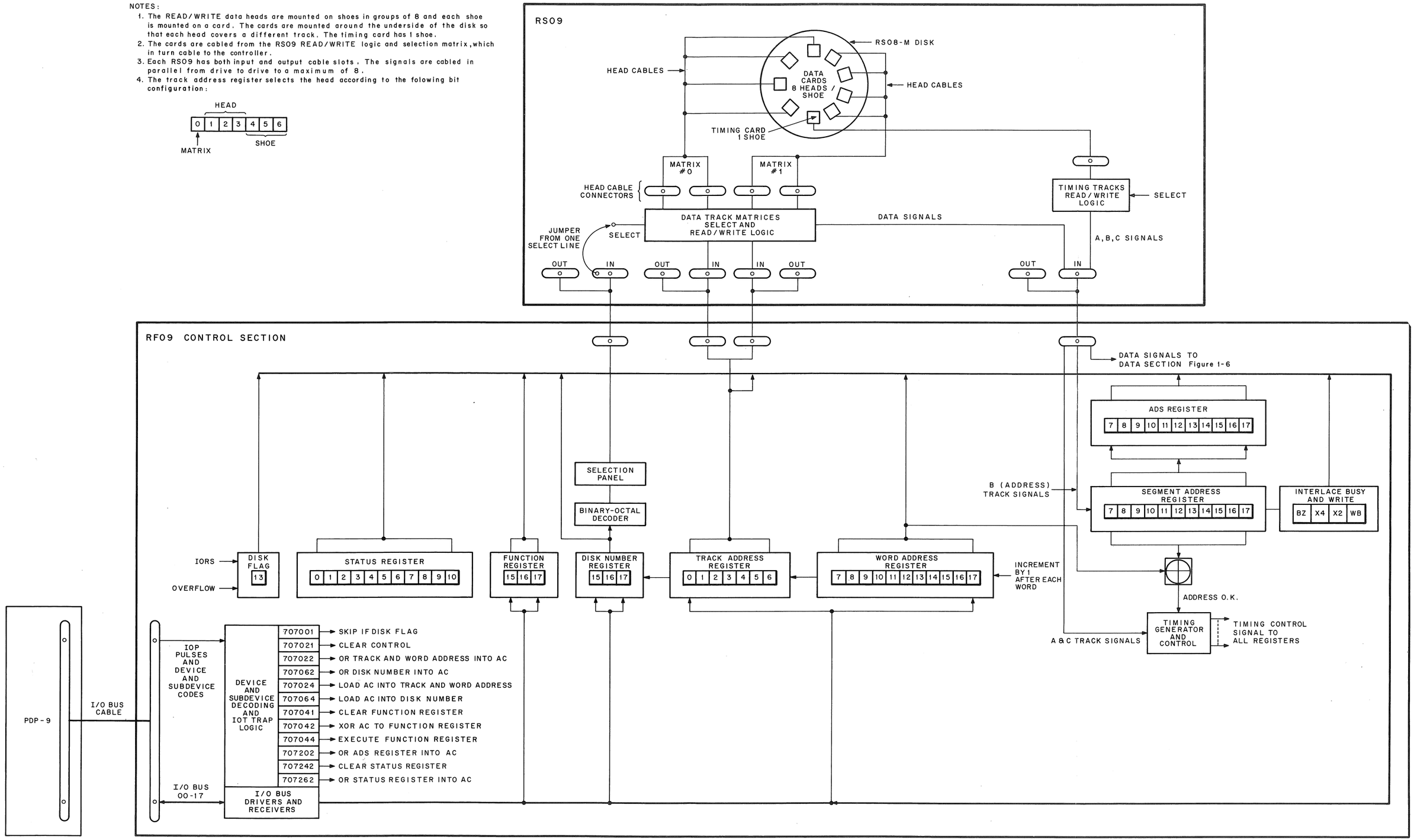


Figure 1-5 DECdisk Control Section 09-0413

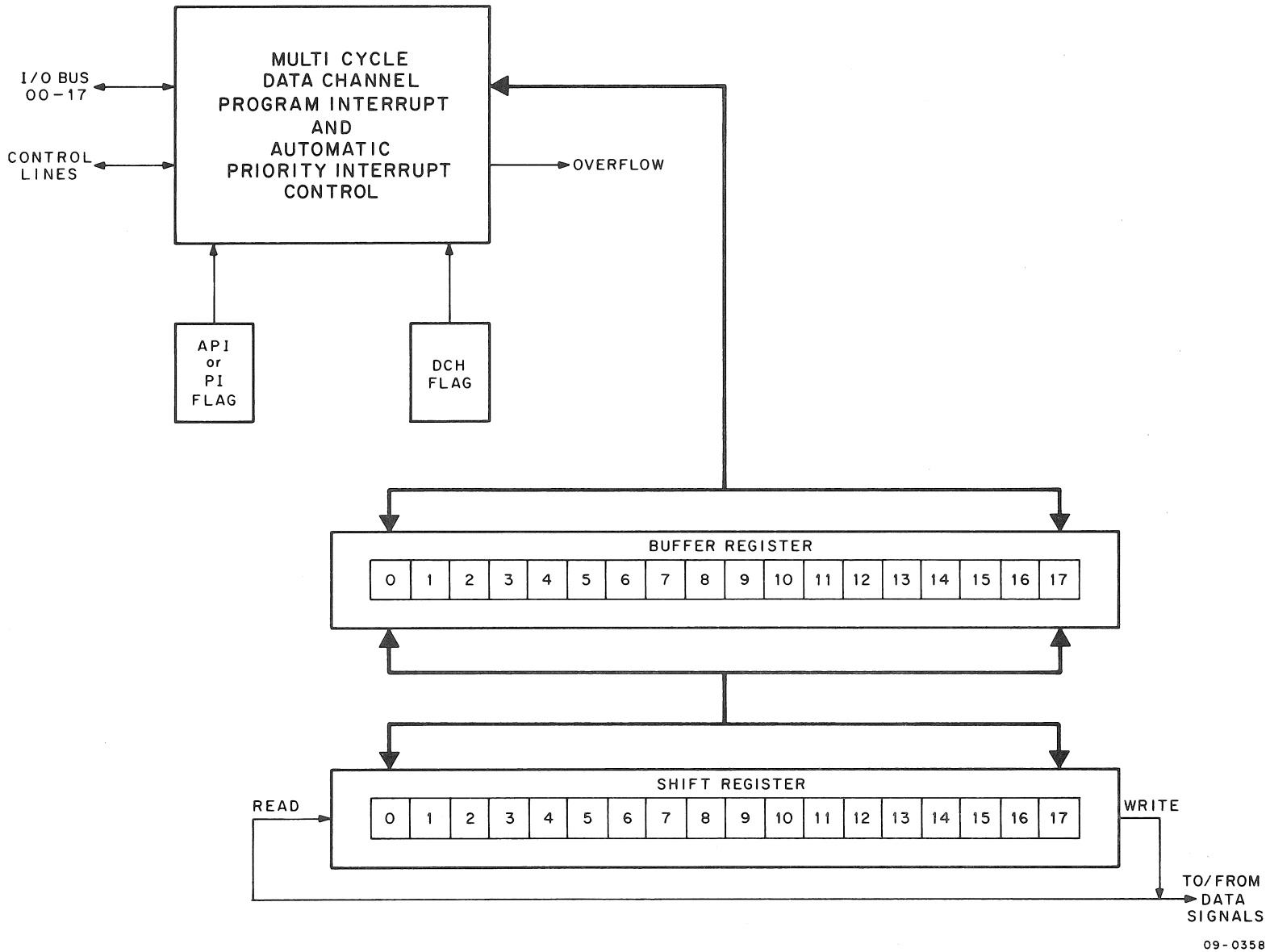


Figure 1-6 DECdisk Data Transfer Section

it wants to read is presently passing over the read head of its selected channel, or that the space in which the data transfer logic wants to write is about to come under the read/write heads.

The interlace logic is used by the operator to reduce the transfer rate of the disk to either a medium or a low speed. The medium speed cuts the rate in half by adjusting the final address of the Disk Segment Register so that only every second address is used in the first revolution of the disk, and the alternate addresses are picked up from the same track on the subsequent revolution. The low speed cuts the transfer rate by four. Each address is then adjusted to require four revolutions of the disk before a complete track is filled. Bits X4 and X2 indicate low and medium speed, respectively, and are set if these speeds are selected by the operator. The flag BZ sets whenever a valid operation is under way, and WB sets when writing is taking place. All of these bits can be read into the accumulator under program control.

The ADS Register receives each valid current segment address from the Segment Register. The current segment address is then available to the accumulator in the ADS Register under program control. Note that the ADS Register receives the current address, and not the adjusted address for low or medium speed transfers.

There are three bits in the Function Register, which is double buffered. Bits 15 and 16 specify the function that is to be performed by the controller. The function is loaded into the first buffer, and an execute IOT (DSCN) is issued to load it into the second buffer for execution. At the end of an operation, or if an error occurs, the second buffer is cleared and execution stops. The operation can then be continued by issuing a DSCN IOT execute. Table 1-2 shows the bit configuration needed to select each function. Bit 17, also contained in the Function Register, enables the interrupt and API logic of the control.

Table 1-2
The Function Register Bit Configuration

Function	Bit 15	Bit 16
No Effect	0	0
Read	0	1
Write	1	0
Write Check	1	1

The timing generator and control logic receive the A and C track signals and generate all of the system timing and control pulses necessary to carry out the various macro operations (such as shifting the Segment Register and incrementing the Word Track and Disk Address Registers).

The 10-bit Status Register reflects the state of the system after it has performed its specified operation. Any timing or parity errors that have occurred during the operation are indicated here. Table 1-3 summarizes the function of each bit.

1.2.2.2 **The Data Transfer Section** – The data transfer section, shown in Figure 1-6, has 4 subunits; two 18-bit registers and two controls. During a READ operation, a word is assembled into the Shift Register. If the word has been assembled from the selected address (ADDRESS OK), and the C track indicates that a valid word has been assembled; the contents of the Shift Register are then jammed into the Buffer Register. The computer is notified that a word is ready for transfer, and a multi-cycle data break occurs. At the same time, the Shift Register is assembling the next word. The word count (WC) and current address (CA) for the DECdisk are in locations 36_8 and 37_8, respectively.

During the WRITE operation, the computer transfers the word to be written into the Buffer Register where it waits for the ADDRESS OK signal. When this signal arrives, the word is immediately transferred to the Shift Register and is serially shifted from there onto the selected track.

During a WRITE CHECK operation, which is designed to allow the programmer to compare data in memory with corresponding data on the disk, the memory word is fed into the Buffer Register and then into the Shift Register where it is compared bit by bit with the serial data directly from the disk. If a discrepancy or a parity error exists, the DISK flag is posted.

The instruction set, listed in Table 1-4, allows the computer to clear, load, or read from each of seven registers in the control section. The following points should be noted:

a. The DISK flag is posted under two conditions;

(1) at the end of the operation, and

(2) if one of the six error conditions occur.

The DISK flag causes either a PI or an API interrupt if these interrupts are enabled in both the controller and the computer.

b. Whenever the DISK flag is posted, the second buffer of the Function Register is cleared, and the operation stops. The first buffer does not clear; and the operation can either be continued by issuing the execute IOT, or altered by changing its code and then issuing the execute instruction.

c. The ADS Register reflects the current position of the disk and not the adjusted address. A program can read its contents and calculate the nearest possible address to which it could transfer its first word (taking into account the speed setting), set the address into the Address Register, and, thereby, reduce the initial latency time. (The ADS Register can be one address late.)

d. The disks are not synchronized with each other. When the control transfers from disk to disk, the control itself has no way of knowing the next disk location in its revolution. The ADS Register locates the next disk.

e. During an operation, the Disk, Track, and Word Address registers automatically increment as the system rotates from word to word, track to track, and disk to disk. At all other times, these registers remain constant.

Table 1-3
Status Register Bit Functions

Bit	Flag Name	Function
0	ERR	This ERRor flag is the logical OR of the error conditions of bits 1 to 7. When this bit is set, it causes an interrupt and conditions the skip IOT. It also inhibits the current operation until a continue IOT is issued.
1	HDW	The disk HarDWare Error is set if the control detects missing bits from the A, B, or C track. A set HDW causes the control to freeze for further evaluation. (During a "freeze" condition, writing is stopped and the A timing pulses are inhibited.) A freeze is disabled with an I/O RESET, a CAF, or the DECdisk clear IOT.

Table 1-3 (Cont)
Status Register Bit Functions

Bit	Flag Name	Function
2	APE*	The Address Parity Error flag is set if a parity error occurs when the address is being assembled, provided that the control has been programmed to READ/WRITE or WRITE CHECK. This flag does not set if the disk is idling. APE also freezes the control.
3	MXF	A Missed X (Trans)Fer flag is set if the disk requested a data transfer from the computer and did not get it for 2-3 revolutions. A 130 ms timer triggers to post the MXF flag. Either a data channel failure or a data channel overload initiates this flag. When analyzing an MXF error, the following points should be considered: *a.* The computer increments its current address in the cycle before it transfers its data. *b.* The controller increments its disk or track address when it requests a transfer during a read operation, but only after a transfer is acknowledged during a WRITE or WRITE/CHECK operation.
4	WCE	When the Write Check Error flag is set, the controller has discovered during a WRITE CHECK that the word from memory differs from its corresponding word on the disk. The error flag is raised and all further checking is stopped. The word being checked is in disk location WA-1 (Word Address minus 1), and its corresponding word is in memory address CA-1 (Current Address minus 1).
5	DPE*	The Data Parity Error status bit is set whenever the data parity bit does not agree with the computed parity of the data word just read. The control transfers the data word containing the parity error and raises the error flag. No further transfers occur until the program intervenes. The WA-1 contains the disk address of the word in error. The CA contains the memory address of the word in error.
6	WLO*	The Write LockOut error bit is set when an attempt is made to write into a protected region on the disk. READ or WRITE CHECKING a protected area is permitted. (See the Operator's Controls Section, paragraph 1.3, for details of this protection.)
7	NED	If a disk which does not exist is called for under program control or sequenced into during data transfers, the Non Existence Data flag is raised to signal the error. (For details on how disks are assigned, see the Operator's Controls Section, paragraph 1.3.)
8	DCH	The Data CHannel Timing Errors status bit is set whenever the processor has not completed a DCH transfer before the disk control is ready to transfer data. No error flag is raised. This status bit is intended as a warning that the DCH channel is overburdened.

*Note that the hardware is designed to allow only the first of these three errors to set during an operation.

Table 1-3 (Cont)
Status Register Bit Functions

Bit	Flag Name	Function
9	PGE	The ProGramming Error status bit is set whenever the program issues an illogical command to the disk. Furthermore, if the command directly conflicts with the operation of the control, the command is ignored. No error flag is raised. This status bit is provided as a warning to the programmer.
10	XFC	When the job requested via the program (either READ, WRITE, or WRCHK) is finished, the (X) TransFer Complete flag indicated by this bit interrupts the processor and conditions the SKIP IOT.

Table 1-4
The DECdisk Instruction Set

Code	Mnemonic	Description
707001	DSSF	Skip if Disk Flag. The Disk flag is raised for either an error condition (ERR) or when transfer is complete (XFC). This flag is indicated on bit 13 of the Input/Output Read Status (IORS) facility. If the Program Interrupt (PIE) and/or Automatic Priority (API) is enabled, the DSSF flag causes the program to be interrupted.
707021	DSCC	Clear the Disk Control and disable the "freeze" status of the control. This IOT is the only command honored by the control when a "freeze" is caused by either a timing track hardware or an Address Parity Error and forces the control to abort the operation in progress. It effectively Power Clears the DISK CONTROL.
707022	DRAL	OR the contents of the Address Pointer O (AP0) into the AC. Bits 0 through 6 contain the track address and bits 7 through 17 contain the word address of the next word to be transferred.
707062	DRAH	OR the contents of the Disk Number (AP1) into the AC. Bits 15, 16, and 17 contain the Disk Number. Bit 14 is read back if a data transfer has exceeded the capacity of the Disk Control (causes a NED error status).
707024	DLAL	Load the contents of the AC into the AP0.
707064	DLAH	Load the contents of the AC (15, 16, 17) into the Disk Number (AP1).
707041	DSCF*	Clear the Function Register, Interrupt Mode.
707042	DSFX*	XOR the contents of AC bits 15-17 into the Function Register (FR). The use of each bit is the same as described for bits 15-17 of the Status Register.
707044	DSCN*	Execute the condition held in the FR. Since the AP contains the next available word (because it is incremental), this IOT can be used to continue after having changed the Word Count (WC) and Current Address (CA) held in core memory, or it can be microcoded with the Clear (DSCF) and XOR (DSFX) instructions to execute a new function at different address.

*These instructions may be microcoded in any combination.

Table 1-4 (Cont)
The DECdisk Instruction Set

Code	Mnemonic	Description
707202	DLOK	OR the contents of the 11-bit Disk Segment Address (ADS) into the AC. The ADS Register contains the real-time segment address, which is useful for minimizing access times. The address read always indicates the physical position of the disk (that is, one address of 2048 for one revolution (360°) of the disk, independent of the transfer rate being used).

Register Configuration

BZ	X4	X2	WB		ADDRESS OF DISK SEGMENT (ADS)
0	1	2	3	7	17

When reading the ADS Register, the most significant four bits contain the status condition explained below.

AC Bit	Name	Function
0	BZ	Busy. The disk has been commanded to transfer data and it is not finished. When reading the ADS Register, this is an indication that if the Address Pointer is used by the programmer to determine the Track Address (TA), the Track Address may not be valid if the ADS Register contains 3777 (since the TA may be changing at this time).
1	X4	The control is set to transfer every fourth word. The effective transfer rate is, therefore 64 μs per word.
2	X2	The control is set to transfer every other word. The effective transfer rate is, therefore, 32 μs per word.

If neither X4 nor X2 is set, the control is operating at its highest rate or 16 μs per word.

AC Bit	Name	Function
3	WB	Write Bit. This bit is used primarily for maintenance purposes. It is the intermediate storage location for the data being transferred to the disk during WRITE.

707242	DSCD	Clear the Status Register and Disk Flag.
707262	DSRS	OR the contents of the Disk Status Register with the Accumulator (AC). Status at the point of interrupt is as follows: AC 0 Error (ERR) 1 Disk Hardware Error (HDW)

Table 1-4 (Cont)
The DECdisk Instruction Set

Code	Mnemonic	Description
707262 (Cont)		2 Address Parity Error (APE) 3 Missed Transfer (MXF) 4 Write Check Error (WCE) 5 Data Parity Error (DPE) 6 Write Lockout (WLO) 7 Non Existent Disk (NED) 8 DCH Timing Error (DCH) 9 Program Error (PGE) 10 Transfer Complete (XFC) AC 15, 16, and 17 Function Register states are as follows: (If Bit 17 is a 1, the API and PI logic in the controller is enabled.) **Bit 15 (F0)** **Bit 16 (F1)** 0 0 No Effect 0 1 READ 1 0 WRITE 1 1 WRCHK

1.2.2.3 Maintenance Section – The Maintenance section provides a means to test each unit of the DECdisk system without running the other units. Signals that usually come from the read/write heads of the disk surface can be simulated by the controller under IOT control with the logic shown in Figure 1-7. Similarly, signals from the RS09 output cables can be simulated by the controller with the logic shown in Figure 1-8. In this way, the controller can be tested without the disk drive, and the RS09 electronics can be tested without the disk surface. A more detailed explanation of these signals is found in Chapter 2.

The Buffer Register, which is normally available to the data channel alone, can be accessed from the Central processor under the control of maintenance IOTs.

The Maintenance section also allows signals transmitted over cables between the controller and the RS09 disks to perform active functions while they are themselves active. Therefore, if a wire in the cable is broken, a function is disabled rather than uncontrollably activated.

Table 1-5 lists the maintenance IOTs, and Figures 1-9 and 1-10 shown simplified versions of some of the maintenance logic for the simulator section.

Table 1-5
Maintenance IOTs

Code	Mnemonic	Description
707204	DGHS	Generate Simulated Head signals. This maintenance IOT causes the control to generate analog signals that simulate the disk head signals, as received directly from the head. The AC is used to determine the sequence of pulses to be generated, and the bit rate is controlled by the diagnostic program. Each IOT, in effect, is treated as though it were one cell space on the disk. The function of the AC bits is shown in Figure 1-9.

Table 1-5 (Cont)
Maintenance IOTs

Code	Mnemonic	Description
707204		The bits are arranged as shown to provide for data packing, since only the bits that appear in the AC in bit cell 1 position are used when the IOT is generated. An RAR can then be used to position the data for the next Simulated Head Signal. When either of the maintenance IOTs (707204 or 707224) is used, a Maintenance Control flip-flop is set that inhibits the effect of control delay timeouts, which are a result of the lower data rates encountered under program simulation. If subdevice Bit 0 (MB12) is used when issuing the above IOTs, the Maintenance Control flip-flop is cleared.
707224	DGSS	Generate Simulated Disk signals. This IOT causes the control to generate Simulated Disk Interface signals within the control. No disk is necessary. The AC is used to determine the sequence of pulses to be generated and the bit rate is controlled by the diagnostic program. Each IOT, in effect, is treated as though it were one cell space on the disk. The function of the AC bits is shown in Figure 1-10. The bits are arranged as shown to provide for data packing, since only the bits which appear in the AC in bit cell 1 position are used when the IOT is generated. An RAR can then be used to position the data for the next Simulated Head Signal.
707002	DRBR	OR the contents of the Buffer Register with the AC. This is a function normally performed by the data channel.
707004	DLBR	Load the contents of the AC into the Buffer Register. This is a function normally performed by the data channel.

1.3 THE OPERATOR'S CONTROLS

There are three groups of operator controls on the disk system. These include a three-position switch to select the transfer rate, a jumper panel to assign the address of each disk, and a series of write lockout switches to protect regions from being written onto each disk. The first two controls are part of the controller itself, and the write lockout switches are available on each disk drive.

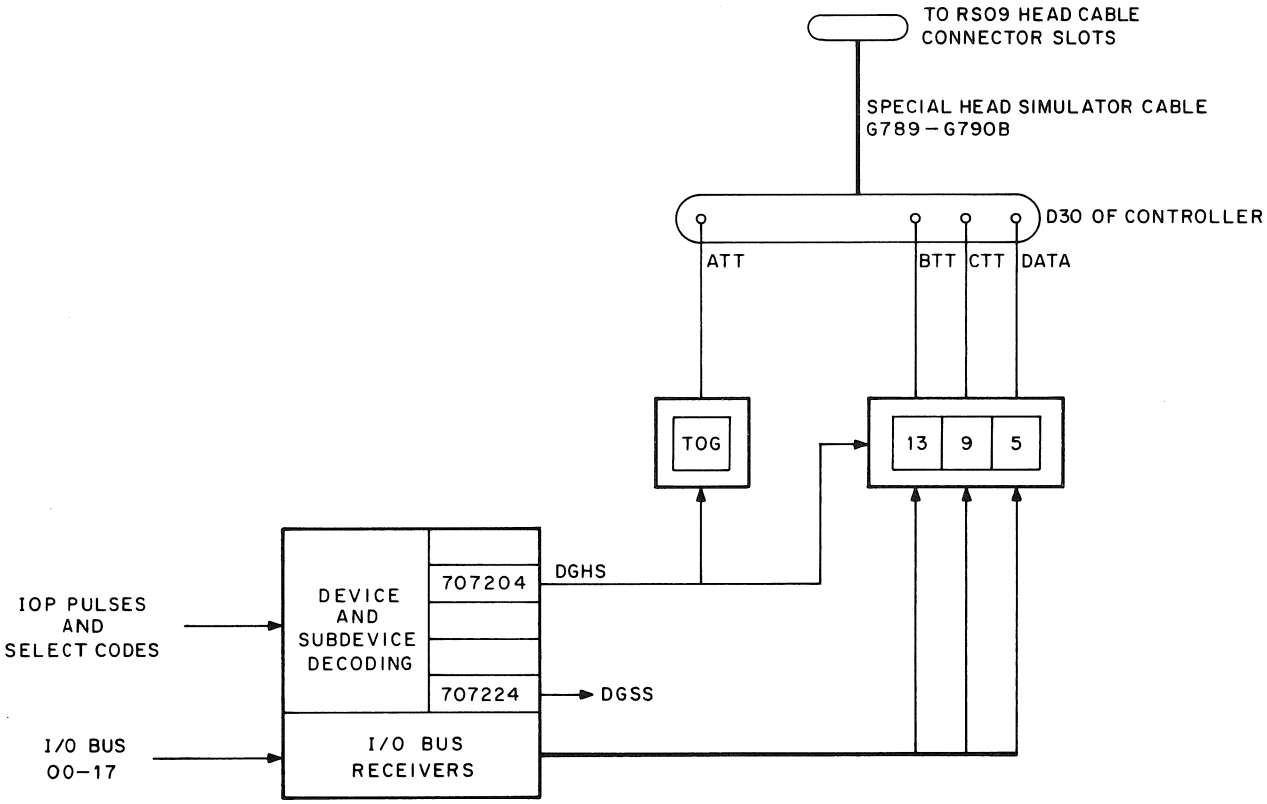
1.3.1 Transfer Rate Selection

The operator can select a high, medium, or low transfer rate by positioning the rate selection switch at HI, MED, or LOW.

At the high speed, data is transferred to or from each word on a disk channel every 16 μs.

At the medium speed, the rate is halved to every 32 μs, not by slowing down the disk, but by requiring the disk to rotate twice in order to fill a channel completely. During the first rotation, every second address is read from or written into; in the second rotation the remaining addresses are used. All this is done automatically without extra coding. However, the programmer must ensure that the disk is read at the same speed at which it was written, or the data becomes unintelligible.

At the low speed, every fourth address is used on the first revolution, and the remaining addresses are picked up on the successive three turns. The transfer rate is one word every (4 x 16) 64 μs. The programmer is not



NOTES:
1. TOG is complemented when DGHS is released.
2. Bits 13, 9, and 5 are set from corresponding AC bits.
3. The letters ABCD indicate which track is simulated.
   D is for all data tracks.

09-0393

Figure 1-7 Simulating the Disk Surface with the Maintenance Logic

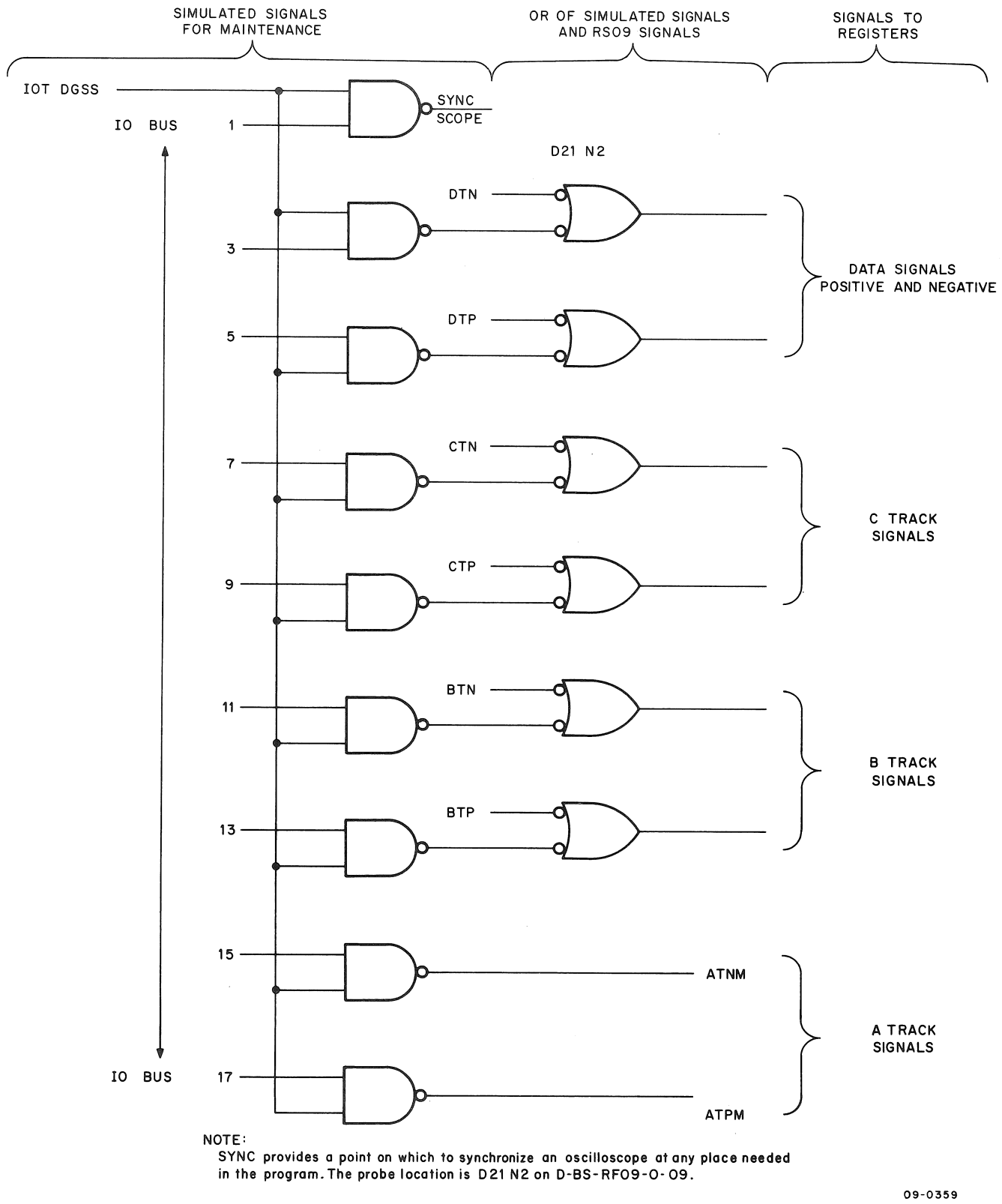


Figure 1-8 Simulating the RS09 with the Maintenance Logic

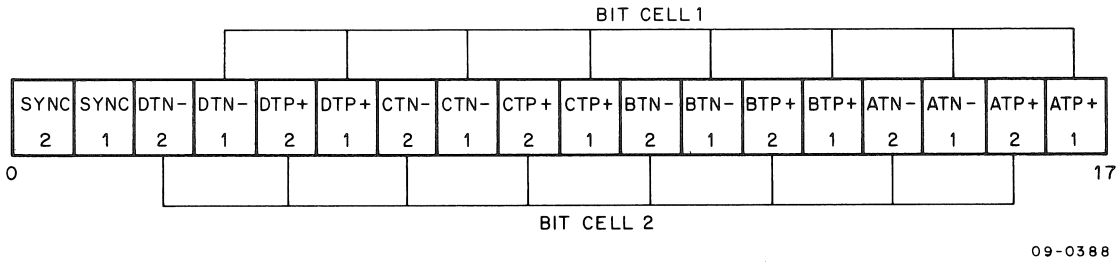


Figure 1-9 AC Bit Usage for IOT DGSS

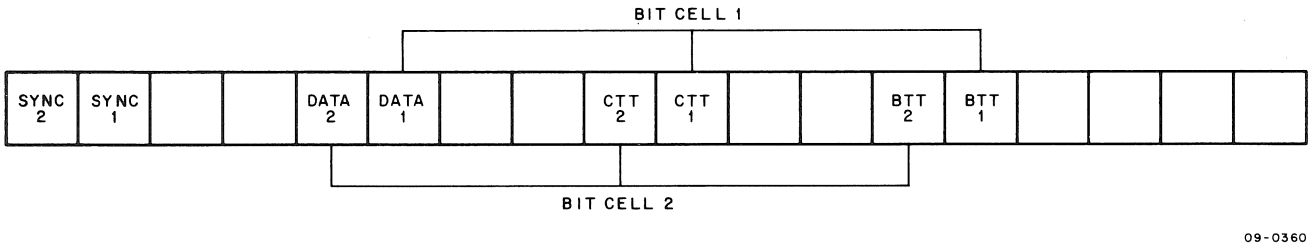


Figure 1-10 AC Bit Usage for IOT DGHS

required to do any extra coding, as the hardware completes the operation. The programmer must, however, ensure that the data is read and written at the same speed. Table 4-2 explains address modification for the two lower speeds by the Segment Register. Note that the PDP-9/L Computer should be used only at medium or low speeds.

1.3.2 Disk Address Selection Jacks

The jacks shown in Figure 1-11, which are part of the controller, are used to assign selection numbers to the RS09 disk drive. The select wire of each drive is wired to an individual plug in the DISK bank. The select decoder of the controller is wired to the DISK SELECTION jacks. Each disk can be assigned any address by plugging the appropriate DISK SELECTION jack into that disk's plug of the DISK bank. Any jacks that are not assigned should be plugged into one of the NONEXISTENT DISK plugs; a selected nonexistent-disk error can then be detected.

1.3.3 Write Lockout Switches

There are 16 lockout switches on each disk drive (labeled 00 through 74). Each switch protects 8 tracks on the disk. Switch 00 protects tracks 0 to 7_8, switch 04 protects tracks 10_8 through 17_8, and so on, up to track 170_8. When any one of these switches is set to DISABLED, the 8 tracks that they protect cannot be written on. If the program tries to write in such a protected area, the WLO flag (Write LockOut) is posted and writing is inhibited. Figure 1-12 shows the lockout switches. Note that switch 00 actually protects the first head of each shoe, switch 04 the second head, etc. For the programmer, this translates into successive tracks in blocks of 8.

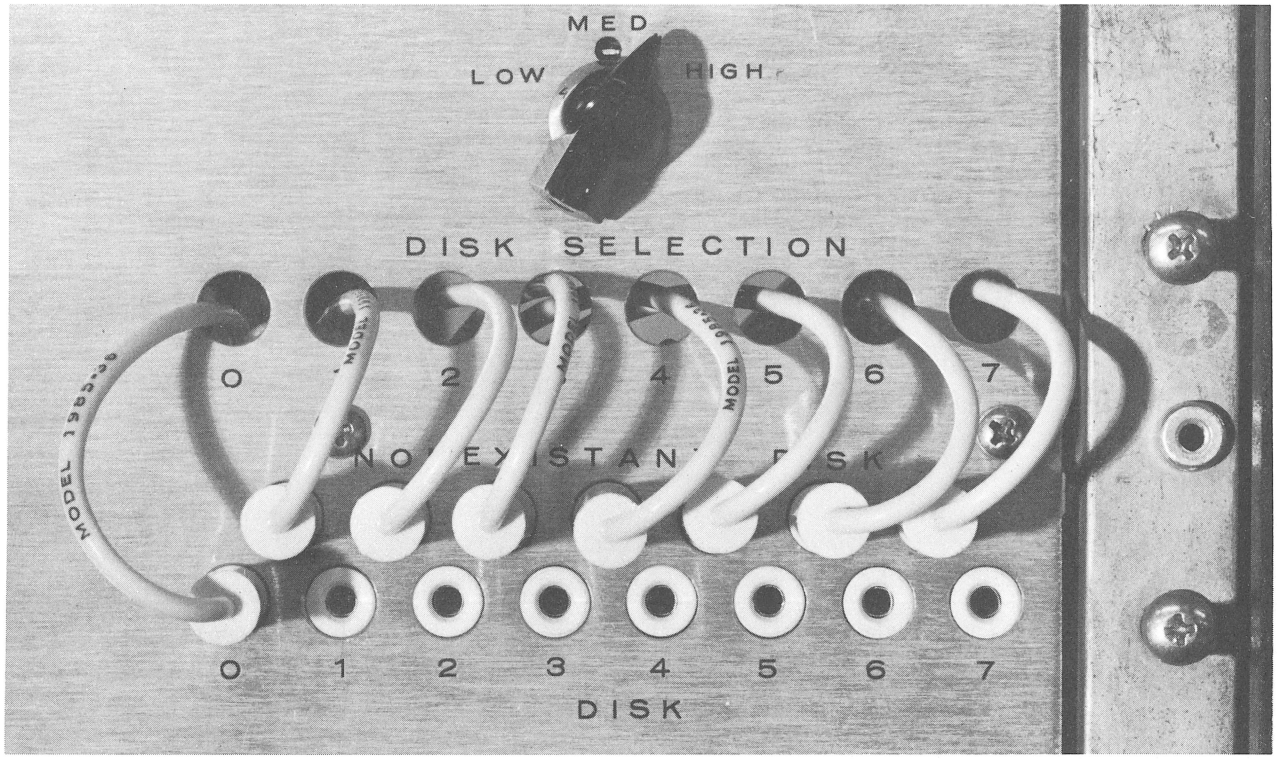


Figure 1-11 Transfer Rate Selection Switch and Disk Address Select Jacks

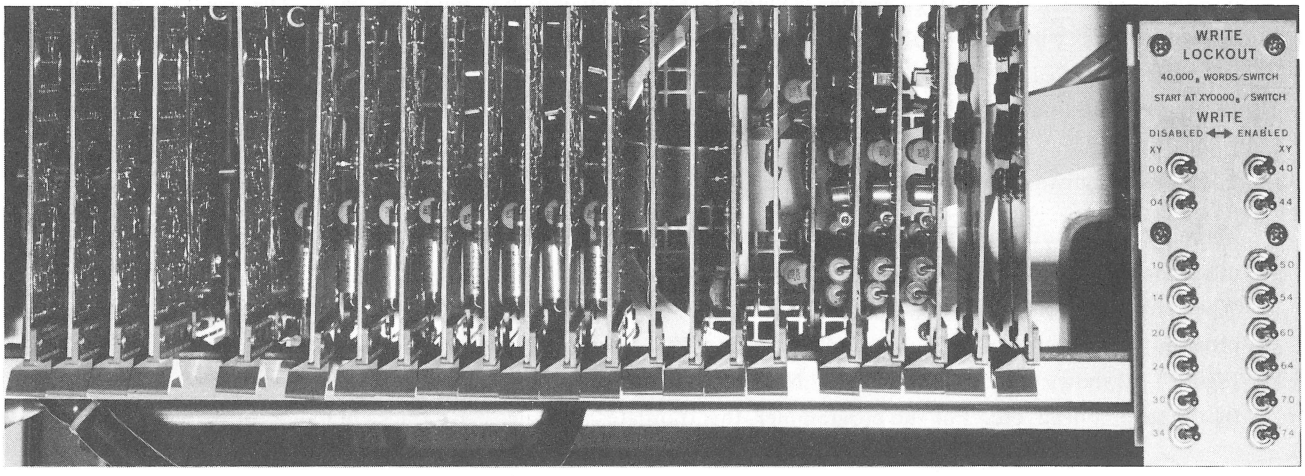


Figure 1-12 Write LockOut Switches

1.4 THE OPERATOR'S INDICATORS

The operator has at his disposal an extensive indicator panel that reflects the state of the DECdisk system (see Figure 1-13). If a light on the panel is lit, the bit it reflects is set. Table 1-6 summarizes the meaning of each light.

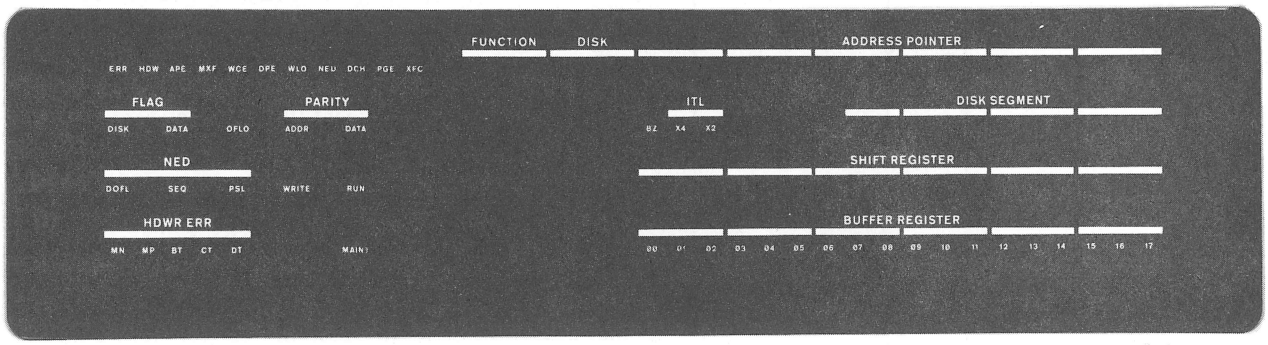


Figure 1-13 Indicator Panel

Table 1-6
The Indicator Panel

Indicator Group	Indicator Name	Indication When Lit
STATUS	ERR, HDW, APE, MXF, WCE, DPE, WLO, NED, DCH, PGE, XFC	The Status Register bits described in Table 1-3 are set.
FUNCTION	-	Three bits of the Function Register decoded in Table 1-2 are set.
DISK	-	Three bits of the Disk Selection Register are set.
ADDRESS POINTER	-	The first 7 bits from left to right indicate the contents of the Track Address Register, and the following 11 bits indicate the content of the Word Address Register.
FLAG	DISK	This level is the logical OR of the two conditions that cause an API or PI break – the ERROR flag and the TRANSFER COMPLETE flag.
	DATA	The flag that requests a multicycle data break is set.
-	OFLO	The computer has overflowed its Word Count Register and has set this flag to stop further transfers.
PARITY	ADDR	A parity error on the B or address track has been detected.
	DATA	A parity error on the current data track has been detected.

Table 1-6 (Cont)
The Indicator Panel

Indicator Group	Indicator Name	Indication When Lit
	BZ	The disk is presently BUSY and engaged in a data transfer.
ITL	X4	When this bit is set, the operator has selected the LOW transfer rate, and every fourth bit is being transferred. (ITL = interlace.)
	X2	Same indication as X4, except that the operator has selected the MED transfer rate.
NED	DOFL	During a transfer, the control sequenced into the ninth disk, which does not exist. (NED = Non Existent Disk.)
	SEQ	During a transfer, the control sequenced into a disk unit that does not exist. The difference between DOFL and SEQ is that in SEQ a disk could be added, i.e., the system capacity was not exceeded. With DOFL, the control asked for a disk address greater than 7_8.
	PSL	A nonexistent disk unit was specified by the program. It was not sequenced under a transfer; the error was a direct programming mistake.
	WRITE	A WRITE operation is taking place.
	RUN	The control is busy and properly synchronized.
HDWR ERR	MN	A missing negative pulse or extra positive pulse from the ATT track bipolar signal pair was detected.
	MP	A missing positive or extra negative pulse from the ATT track bipolar signal pair was detected.
	BT	Any pulse of the bipolar signal pair from the BTT track was detected as missing or extra.
	CT	Any pulse of the bipolar signal pair from the CTT track was detected as missing or extra.
	DT	Any pulse of the bipolar signal pair from the addressed data track was detected as missing or extra.
	MAINT	The controller is in Maintenance mode, which is explained in detail in Chapter 4.

1.5 PROGRAMMING EXAMPLES

The following program can be used to READ, WRITE, or WRITE CHECK any number of words that can be accommodated in core memory. The program is set up from a calling sequence table that lists the word count,

current address, disk number, track number, the address of the first word in the track, and the function to be performed. The execute subroutine that follows enters these variables in their respective registers and commands the disk to execute.

```
                                  /Calling Sequence Table
CALTAB      JMS DO                /Jump to execute subroutine
            0 (WC)                /2's complement of number of words to be transferred
            0 (CA)                /Start of memory core data table less 1
            0 (AP0)               /Disk starting word address and track
            0 (AP1)               /Disk number
            0 (FR)                /Function (READ, WRITE or WRITE CHECK) desired
            X                     /Continue program sequence

                                  /Execution Subroutine
DO          0                     /Enter execution subroutine
            LAC DO                /Fetch pointer
            DAC 10                /Deposit pointer in Auto Index Register
            LAC * DO              /Fetch word count
            DAC 36                /Deposit in Word Count Register
            LAC * 10              /Fetch current address
            DAC 37                /Deposit it in CA Register
            LAC * 10              /Fetch disk starting word and track address
            DLAL                  /Deposit it into its registers
            LAC * 10              /Fetch disk number
            DLAH                  /Load into Disk Number Register
            LAC * 10              /Fetch the function
          { DSCF                  /Clear the Function Register
†         { DSFX                  /XOR the Function Register
          { DSCN                  /Execute the condition held in the Function Register
            JMP * 10              /Exit the disk subroutine
```

†Note that these instructions are usually microcoded into 707047.

In this example, a pointer (DO) is set into Auto Increment Register 10. Each time the register is indirectly addressed, it is first incremented by a one. The effective address for the first entry is the WC; for the second, the CA; and so on, down the calling sequence table to the FR. With this technique, the execution subroutine sets up the disk and the multi-cycle data break to carry out the prescribed operation.

The DISK flag is posted if either an error occurs during the transfer or the transfer is completed successfully. The DISK flag causes a PI or API break (if they are enabled) to locations 0_8 or 63_8, respectively, and the program tests for an error or sets up the next transfer from the selected location. The DISK flag can also be tested by the DSSF instruction if PI or API are not used. The following subroutine lists this procedure.

NOTE

IORS may be used to better advantage. DECdisk Flag is indicated in IORS bit 13.

```
PI          0                     /Store the link, extend mode (PDP-9) protect and PC + 1
            JMP FLGS              /
FLGS        IOT SKPA              /Skip if device A flag
            SKP                   /Go to next device
```

FLGS (cont)

```
        JMS DEVA        /Handle device A
        IOT SKPB        /Skip if device B flag
        SKP             /Go to next device
        JMS DEVB        /Handle device B
          .
          .
          .
        DSSF            /Skip if DISK flag
        SKP             /Go to next device
        JMS DISK        /Handle disk
          .
          .
          .
        ION             /Turn PIE on
        JMP * PI        /Return to main program
```

For systems with API, the following instruction is required:

```
   63   JMS DISK        /API setup
```

The program is now aware that the DISK flag has been set. To determine if a successful transfer has taken place, read the status word into the AC by the DSRS IOT. AC bit 0 is the logical OR of all significant error conditions, and it can be quickly tested by the skip on positive accumulator (SPA) instruction. If no skip occurs, an error exists; and the next step is to determine the error and take the required action. The following program illustrates these points.

```
DISK    0               /Store PC + 1, link, EXD (PDP-9) and protect
        DSRS            /Disk read status
        DAC SAVE        /Save the status
        SPA             /Test for an error condition
        JMP ER          /Go to error routine
        JMP XFC         /Go to transfer complete routine. Set program flag.
        DBR             /API debreak and restore command
        JMP I DISK
```

The API and PI subroutines normally differ in that the API is kept as short as possible so that it does not tie up the API channel and hold up other devices. Techniques for programming the API are explained in its manual. For simplicity, the same handler for both PI and API is used in this manual.

The error flags that cause an interrupt or API break can be classified into three categories, according to the action that should be initiated upon their occurrence. HDW (APE and MXF) and timing errors such as BT, CT, etc., indicate hardware malfunctions; and, if they persist, the need for a Field Service Engineer. WLO and NED show that either an operator error was made when the system was initiated, or that the data transferred exceeds the capacity of the system to store it. This situation can be corrected by the operator. If WCE or DPE occur, the program itself can take corrective action by checking if the error persists, and then rewriting the erroneous data. Only if a parity error persists should the operator be notified.

The first two classes of error flags should be tested first. If they caused the interrupt (HDW, APE, and MXF; WLO and NED), the program is stopped; and the status is left in the accumulator for the operator to interpret. If the last set of errors occurs, further action can be expected from the program.

EXAMPLE:

```
ER      LAC STATUS      /Get the status
        AND (346000     /Mask out all but the first two classes
        SNA             /Skip if an error occurs
        JMP REWRIT      /It was a soft error, go to rewrite
        LAC STATUS      /It was a hard error, store the status and
                         notify the operator
```

Note that the error flags are arranged in descending order of importance so that they can also be tested by successive RTL's and skips on link and SMA's.

```
REWRIT                  /The parity error was discovered during a READ or a
                        /WRITE CHECK.
                        /The program can either halt, go back and repeat the
                        /operation several times to see if the error is still there, or
                        /go back and rewrite all the data that has been written
                        /erroneously and then retest it, or both.
```

1.6 PROGRAMMING WITH THE ADS REGISTER

The contents of the ADS Register reflect the current position of the disk surface. This information is available to the program through the IOT instruction DLOK, and can be used to reduce the time it takes to transfer a file between the disk and core memory. Consider the following example, which is illustrated in Figure 1-14.

Assume that a file 1777_8 words long is to be transferred from core memory onto a disk. Let the current address (CA) and the word count (WC) be 2000_8 and the 2's complement of 1777_8 (1024_{10}), respectively. Let address pointer 0 (AP0) = 050000 and let address pointer 1 (AP1) = 0. The function is set to WRITE and the transfer rate to HIGH.

Assume further that after the calling sequence has been set up by the program, the ADS Register is read into the AC and found to be set to location 660_8. The program would then determine the nearest address that it could begin transferring data, taking into account the amount of coding that must be processed before the start IOT is issued, and the time it takes to switch tracks if a track must be switched (200 μs), plus set up time. About 240 μs or 15_{10} addresses later is a reasonable figure. The projected ADS address (PADS) is 677_8 in this example, therefore.

The PADS falls within the area on the disk where the file is to be transferred. The program can now make one of two decisions. It can wait until the disk rotates around to location 0 before it starts to transfer data, or it can begin transferring the file at location 677_8. One way to manage this is to divide the file in core into two subfiles. The first subfile will start at core location 2677_8 and transfer to disk location 677_8. It will overflow 1101_8 words later. The second subfile will start at the original CA location 2000_8, transfer to disk location 0, and overflow 677_8 words later. In this way, the file is transferred in one revolution in its proper sequence, and the time saved from the previous method is approximately the time it takes for one quarter of a revolution.

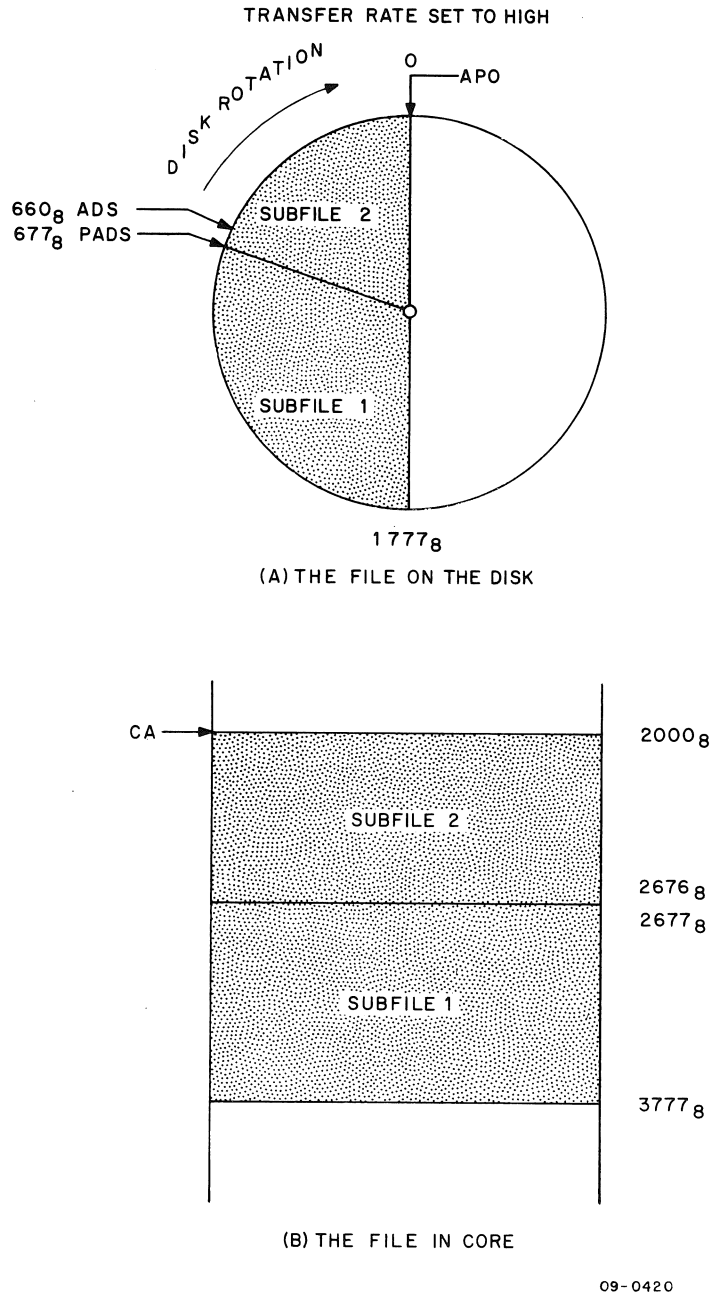


Figure 1-14 Calculating Fast Access Calling

The more general problem of calculating the two subfiles and determining the PADS address for all three transfer rates is somewhat more complicated. Recall that the ADS Register does not give the adjusted address of the Disk Segment Register during medium or low speed transfers. During medium transfer rates, this adjusted address can be found by rotating the ADS Register (the 11 least significant bits) one to the right. During low speed transfers, the adjusted address is calculated by rotating the 11 least significant bits 2 places to the right. The first address for which this is done may not be an address that falls into one of the revolutions where the data is stored for this file. The next address should be tried, and if the transfer rate is LOW, then the following two until either all four revolutions are exhausted; and the program concludes that the disk is not over the file area on any revolution, or until a valid PADS is determined. The flow diagram of Figure 1-15 illustrates the process. Assume for example that a PADS is calculated and falls into the section shown in Table 1-7. If the transfer rate is HIGH, then any address from 74 to 105 is acceptable to test to determine if it falls within the file area. If the transfer rate is medium, it is possible that only every second address belongs to the file. The second line converts the high speed addresses to their appropriate medium speed address. If, for example, it is found that address 75 converted to 2036 does not fall within the data file, then the program must go on to address 76. Converted, this address is 37 to the medium speed transfer. It may be that 37 does fall within the file area, and the program can begin transferring its file at that point. If low speed transfer rates were used, then four addresses (one for each revolution), may have to be tested for valid PADS points.

Table 1-7
Adjusted ADS Register for Medium and Low Transfer Rates

Transfer Rate	Address									
HIGH	74	75	76	77	100	101	102	103	104	105
MEDIUM	36	2036	37	2037	40	2040	41	2041	42	2042
LOW	17	1017	2017	3017	20	1029	2020	3020	21	1021

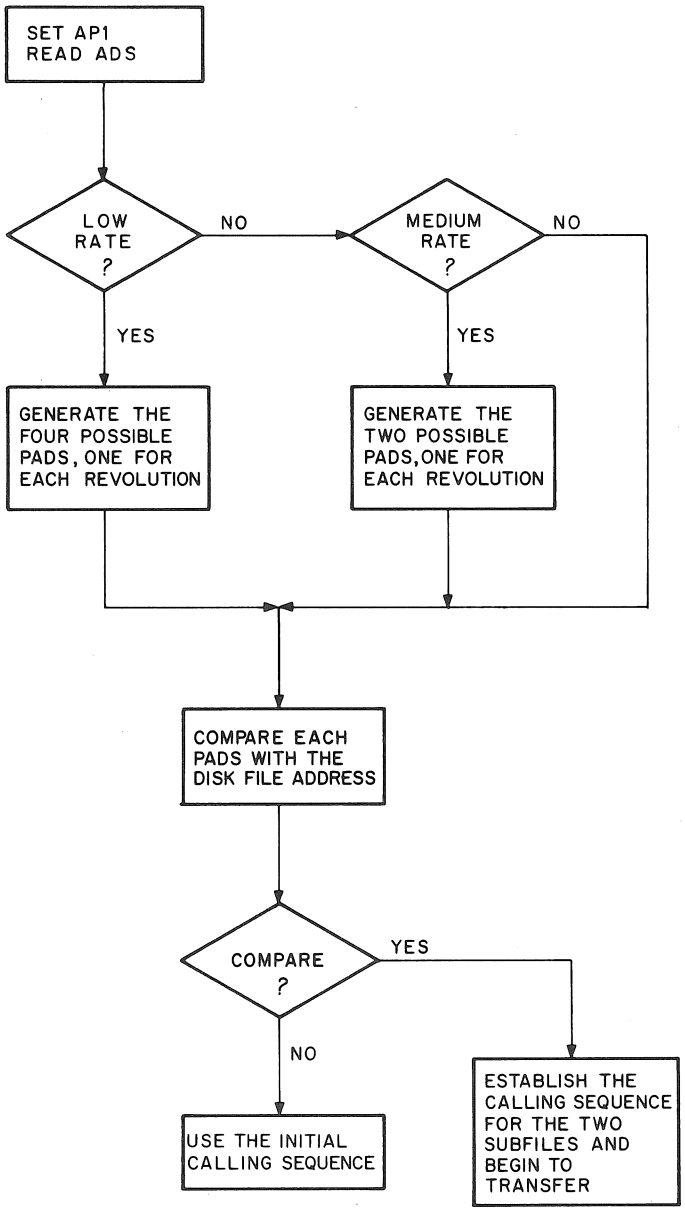
1.7 PROGRAMMING MULTIPLE DISK SYSTEMS

Sequencing from track to track and disk to disk is program transparent except for the latencies that occur when switching from disk to disk. The disks are not synchronized. The latency can be reduced by using the ADS Register. Ensure that when the ADS register is read, the correct disk has been selected; i.e., that address pointer 1 has been properly set up.

If API is set to a disk that does not exist in the system, or if the program sequences into a nonexistent disk such as disk 9 in an 8 disk system, then an error flag is posted. Note that the eighth disk does not overflow and wrap around to disk 0.

1.8 USING DECDISK IN A SYSTEM

There are several points which should be considered when DECdisk is programmed into the system. DECdisk is almost as reliable as the main core memory and considerably more reliable than industry compatible tape. However, the disk should always be supported by another bulk memory unit, typically DECtape or industry compatible tape. It takes about 30 seconds to fill a DECtape reel from DECdisk, and each disk surface fills two such reels. Data files should be regularly dumped from the disk into its support memory, as the data files are generated. How often this is done depends on the application; in most systems, this job can become a background activity except when very important files are under construction.



09-0421

Figure 1-15 Flow Diagram of the Subroutine That Uses the ADS Register

DECdisk may cause one irretrievable error in 2 x 10^9 bits transferred. With most information, this is not a problem. However, if the error occurs during the transfer of system software or the accumulation of a payroll file, the result could be disastrous. For this reason, several error detecting technqiues have been devised. These are listed with short explanations in Table 1-8.

Table 1-8
Disk Data Checks

Name	Explanation
Lateral Parity Checking	This test is automatically performed by the hardware each time a word is read, written or write checked.
WRITE CHECK	This function checks the disk itself. It compares the file in core with the file as it should have been written in memory. The checking is done at the controller, however, so that consistent errors in the data paths are not detected.
WRITE then READ	This technique copies the file onto the disk, and then reads it back into core into a different area. The two files are then checked for consistency. This technique tests the disk, the data paths, and core memory itself. The overhead is high.
Longitudinal Parity Check	When a table or file is built, a longitudinal checksum is calculated with it. Whenever the table is transferred, the checksum is recalculated and compared with the original. This technique tests the disk and the data paths and core, but the overhead is very high.
Error Detecting and Correcting Codes	Hamming codes that automatically correct some errors when they occur can be generated for each word. The overhead when this is done with software is usually prohibitive.
One additional short test can be run on a file after it has been transferred: Add the original word count to the original AP0 and compare the result to the AP0 just after the transfer. They should be identical.	

1.9 SUMMARY OF DECDISK CHARACTERISTICS

The following is a summary of the DECdisk System characteristics:

a. Storage Information

(1) fixed head

(2) serial, random access

(3) 8 disks per controller

(4) 128 data tracks per disk

(5) 2048 eighteen-bit words per track

(6) 262,144 eighteen-bit words per disk

(7) 2,097,152 eighteen-bit words per disk system

b. System Transfer Rates

Three switch-selectable speeds: 16 μs per word;
32 μs per word;
64 μs per word.

c. Protection

Tracks on each disk are protected from a WRITE operation in groups of eight (a total of 16,384 words).

d. Access

(1) 16.7 ms (average) when the ADS Register is not used

(2) 240 μs if the ADS Register is used

e. Reliability

Six recoverable errors and one nonrecoverable error in 2×10^9 bits transferred. (A recoverable error is defined as an error that occurs only once in four successive reads.)

f. Core Locations

Automatic Priority Interrupt	-	63 on level 1
Data Channel	-	36 (WC)
	-	37 (CA)

Chapter 2
DECdisk Modules

2.1 INTRODUCTION

This chapter provides descriptions of special modules used in the DECdisk system.

2.1.1 Types of Modules

DEC builds three series of compatible below-ground logic (the B-, R- and S-series), two series of compatible above-ground logic (K- and M-series), an extensive line of modules to interface different types of logic (W-series), a line of special purpose modules (G-series), and a line of support hardware for its module line (H-series).

With few exceptions, the DEC below-ground logic operates with logic levels of ground to -0.3V (upper level) and -3.2V to -3.9V (lower level), using diode gates that draw input current at ground. Figure 2-1 shows the voltage spectrum of negative logic systems.

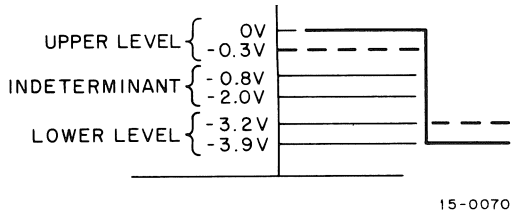


Figure 2-1 Voltage Spectrum of Negative Logic Systems

The compatible above-ground logic generally operates with levels of ground to +0.4V (lower level) and +2.4 to +3.6V (upper level), using TTL or TTL-compatible circuits with inputs that supply current at ground and outputs that sink current at ground. Figure 2-2 shows the TTL logic voltage spectrum.

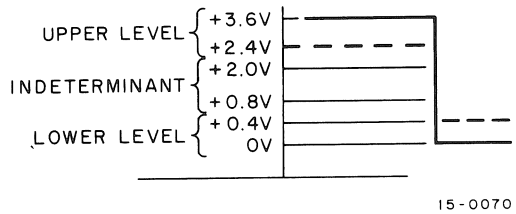


Figure 2-2 Voltage Spectrum of TTL Logic

The use of DEC's **Digital Logic Handbook**, 1970 edition, is recommended for readers of this manual who are not familiar with the basic principles of digital logic and the type of circuits used in DEC logic modules.

2.1.2 Measurement Definitions

Timing is measured with the input driven by a gate or pulse amplifier of the series under test and with the output loaded with gates of the same series (unless otherwise specified). Percentages are assigned with 0 percent indicating the initial steady-state level and 100 percent indicating the final steady-state level, regardless of the direction of change.

Input/output delay is the time difference between input change and output change, measured from 50 percent input change to 50 percent output change. Rise and fall delays for the same module are usually specified separately.

Risetime and falltime are measured from 10 percent to 90 percent of waveform change, either rising or falling.

2.1.3 Loading

Input loading and output driving for TTL Logic are specified in "units", with one unit equivalent to 1.6 mA. The inputs to low-speed gates usually draw 1 unit of load. High speed gates draw 1.25 low-speed units, or 2 mA.

2.2 G085 DISK READ AMPLIFIER

Circuit Description: The G085 Disk Read Amplifier is a double-height module consisting of an ac-coupled amplifier with a bandwidth (-3 dB) from 20 kHz to approximately 1 MHz, followed by a slicer (see Figures 2-3, 2-4, and 2-5). The maximum voltage gain (under potentiometer control) is approximately 60 dB (1000). Common mode rejection ratio is approximately 40 dB. The amplifier is insensitive to any power supply ripple voltage less than 5 percent. Pin AM reduces the gain by approximately 30 percent when its input is low. The nonrectified slice output is gateable, and the slice point can be varied by logic inputs. A potentiometer is provided to adjust the slice. Pins at AT and AV are provided as amplifier test points. Proper grounding is critical in this module. G085 ground pins should not be bussed. Pins AS and AC should be connected to analog ground, and BF and BC should be connected to logical ground. All amplifier connections must be isolated from fast rise-time signals.

Inputs: Voltage levels are 0 and -3V, except at the input to pins AE and AF.

Pin	Function	Load or Input Voltage
AE,AF	Read Head Input	approx. 15 mV peak-to-peak
AM	Read Gain Control	2 mA
BU,BV	Read Slice Control	2 mA
BS,BT	Read Slice Control	2 mA
BP,BR	Enable Output	2 mA

Outputs: Voltage levels are 0 and -3V except at AV, which provides +20V for the timing track center taps.

Pin	Function	Drive
BE,BD	Signal Output	10 mA

Input/Output Delay: 120 ns

Power Dissipation: 2W at +20V
1.5W at -15V

Application: The G085 module is used to detect and amplify timing tracks and data signals for the disk systems RS08 and RS09.

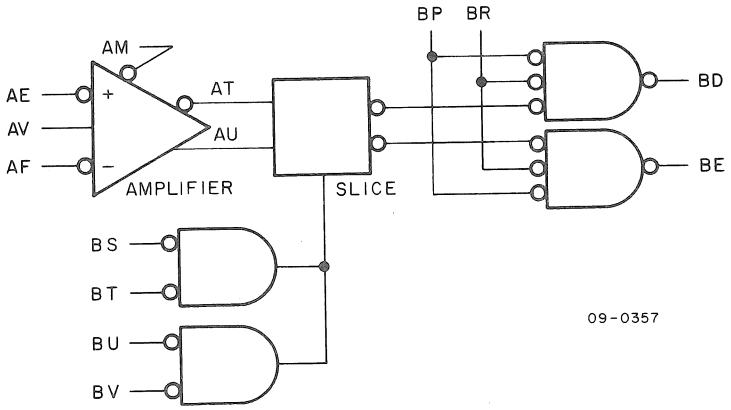


Figure 2-3 G085 Disk Read Amplifier and Slice, Block Schematic

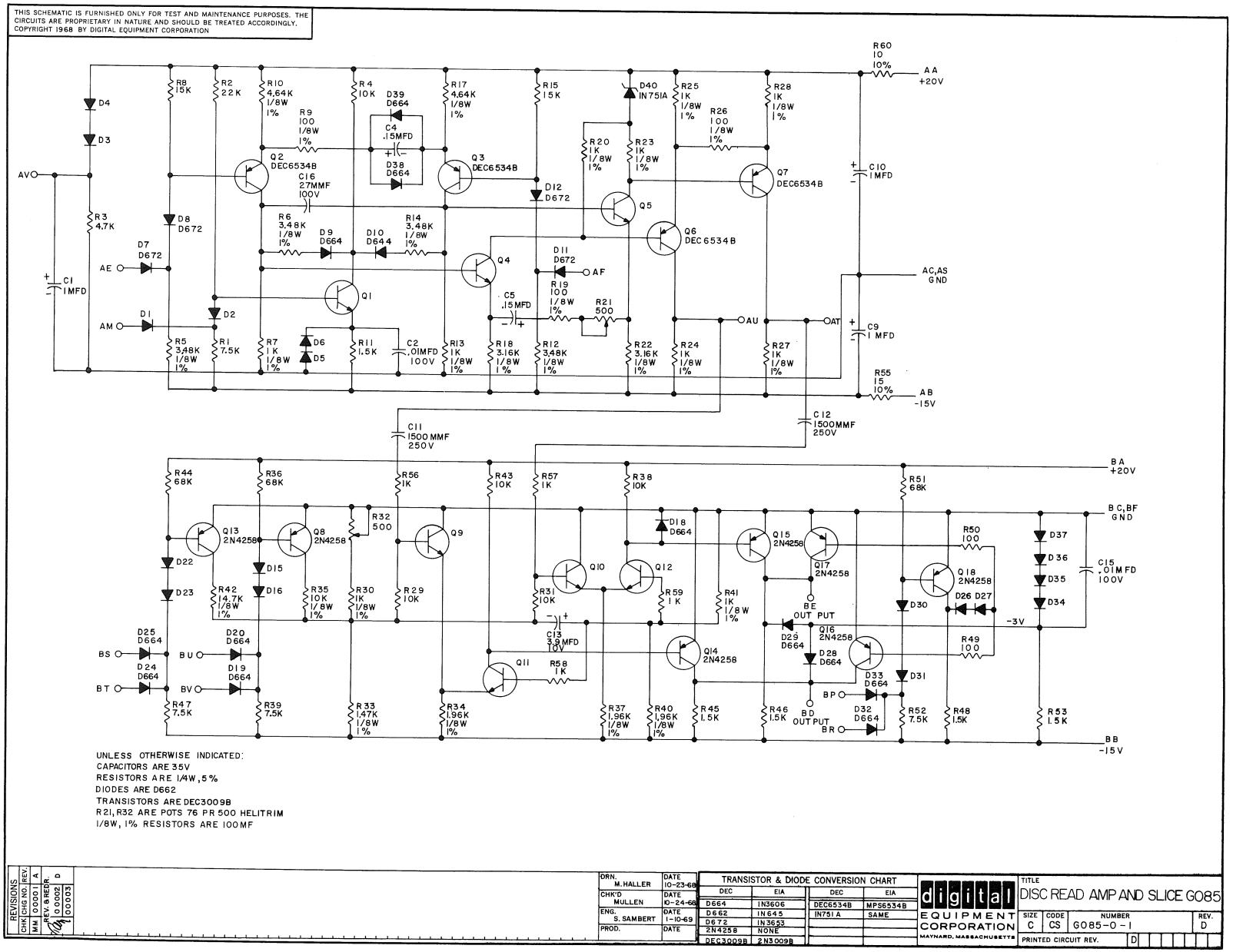


Figure 2-4 G085 Disk Read Amplifier and Slice, Circuit Schematic

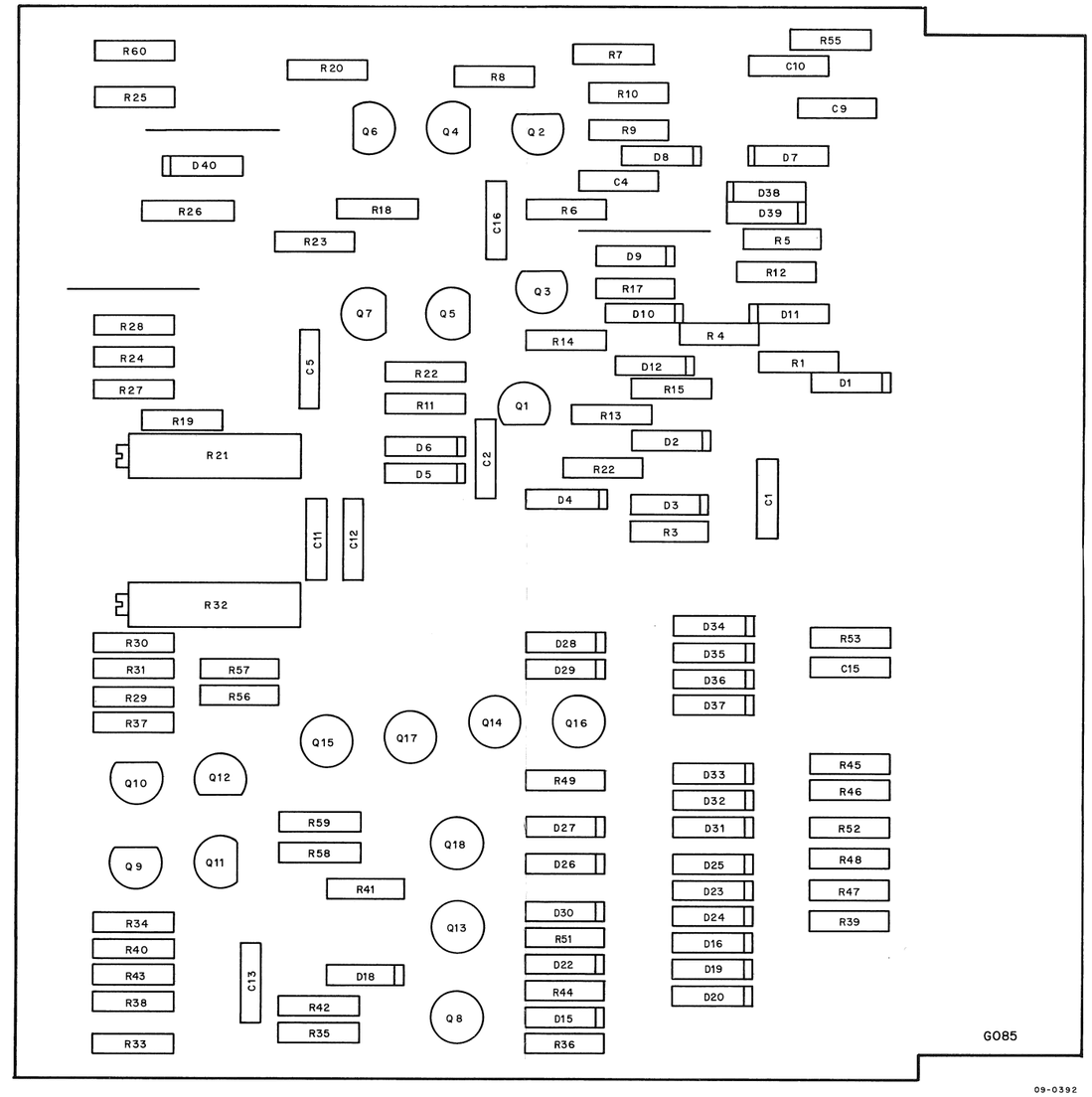


Figure 2-5 Disk Read Amplifier and Slice, Parts Location Diagram

2.3 G285 SERIES SWITCH

The G285 Series Switch is a single-height module consisting of two 4-input AND gates, each driving the base of two driver transistors (see Figures 2-6, 2-7, and 2-8). When a gate is enabled, it in turn switches its corresponding transistors that form part of the select and read/write matrix of the disk or memory.

Inputs: Voltage levels to the gates are 0 and -3V. In levels to the signal inputs L and M are 0 and -15V.

Pin	Function	Load
D,E,F,H,S T,V,M	Gate Enabling Inputs	1 mA shared among inputs at ground
L,M	Signal Inputs	

Outputs: Voltage levels are 0 and -15V (i.e., the input signal gated through the transistor). Each switch pole can drive up to 150 mA. Reverse voltage transients up to 100V do not destroy the switch circuits. Output pins J, K, R, and P must be returned through the load to +10V. The common pins (L and M) to both sets of switches must be returned to -15V. The switches will pass 1 MHz current. The voltage drop for 100 mA is approximately 1V.

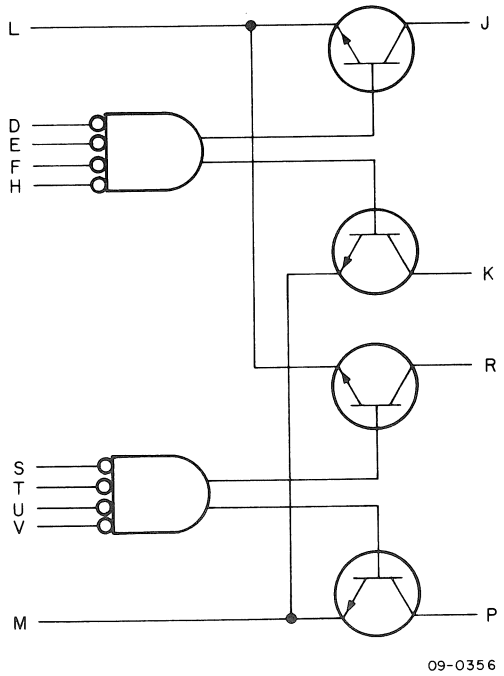


Figure 2-6 G285 Series Switch, Block Schematic

Input/Output Delay: 1 μs

Power Dissipation: 1.5W

Application: This series switch is used together with the G290, the G286, and the G085 to form the Read/Write head matrix described in Paragraph 3.1.

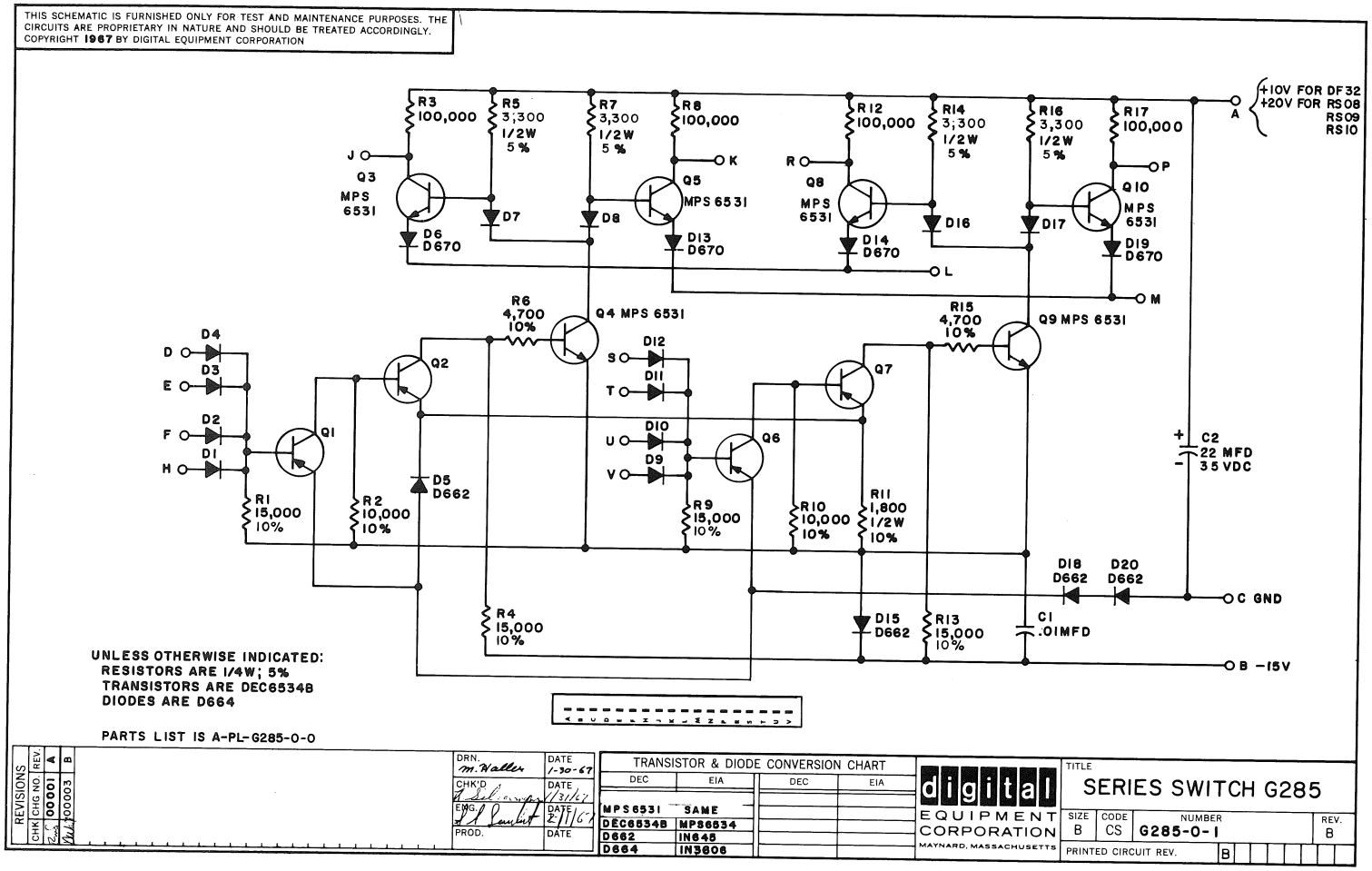


Figure 2-7 G285 Series Switch, Circuit Schematic

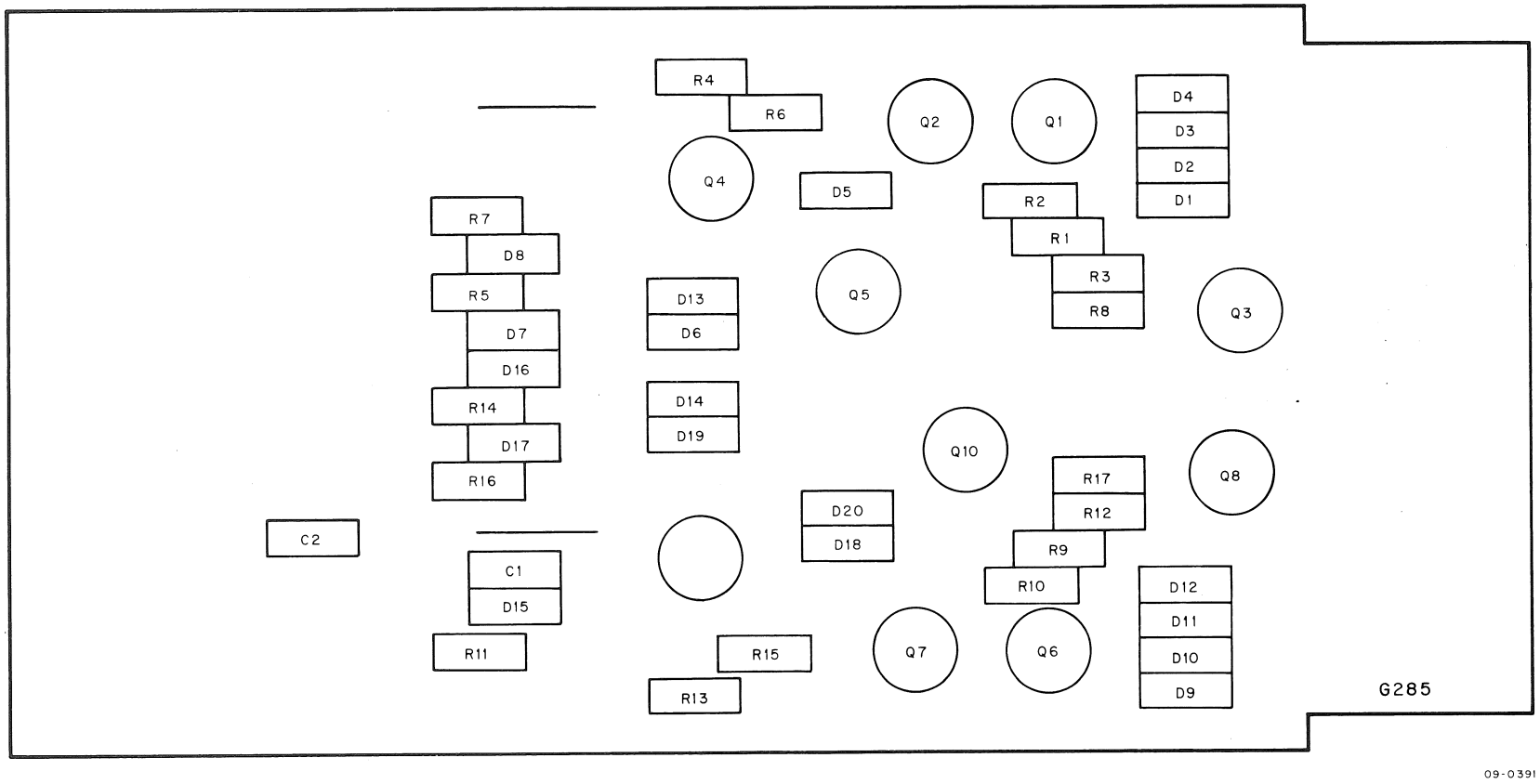


Figure 2-8 G285 Series Switch, Parts Location Diagram

2.4 G286 CENTERTAP SELECTOR

The G286 Centertap Selector is a single-height module consisting of four AND gates, each of which drives a power output stage that applies a +20V level to its output pin when enabled by the gate (see Figures 2-9, 2-10, and 2-11).

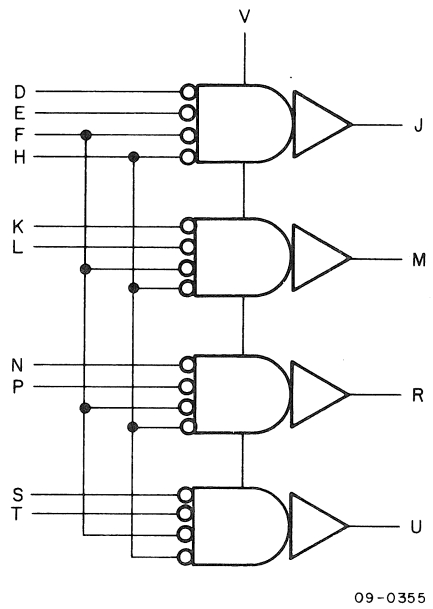


Figure 2-9 Centertap Selector, Block Schematic

Inputs: Voltage levels are 0 and -3V.

Pin	Function	Load
D,E,K,L,N,P,	Gate inputs	1 mA shared among inputs at ground in each circuit
S,T,F,H	Gate inputs	

Outputs: Each output is +20V when the AND gate is enabled and 0V when the gate is not enabled. Each output drives 150 mA at +20V.

Input/Output Delay: 500 ns

Power Dissipation: 1.4W

Application: This module supplies the +20V read/write level to the coil of each head it drives in the matrix. Refer to Paragraph 3.4 for a more detailed description.

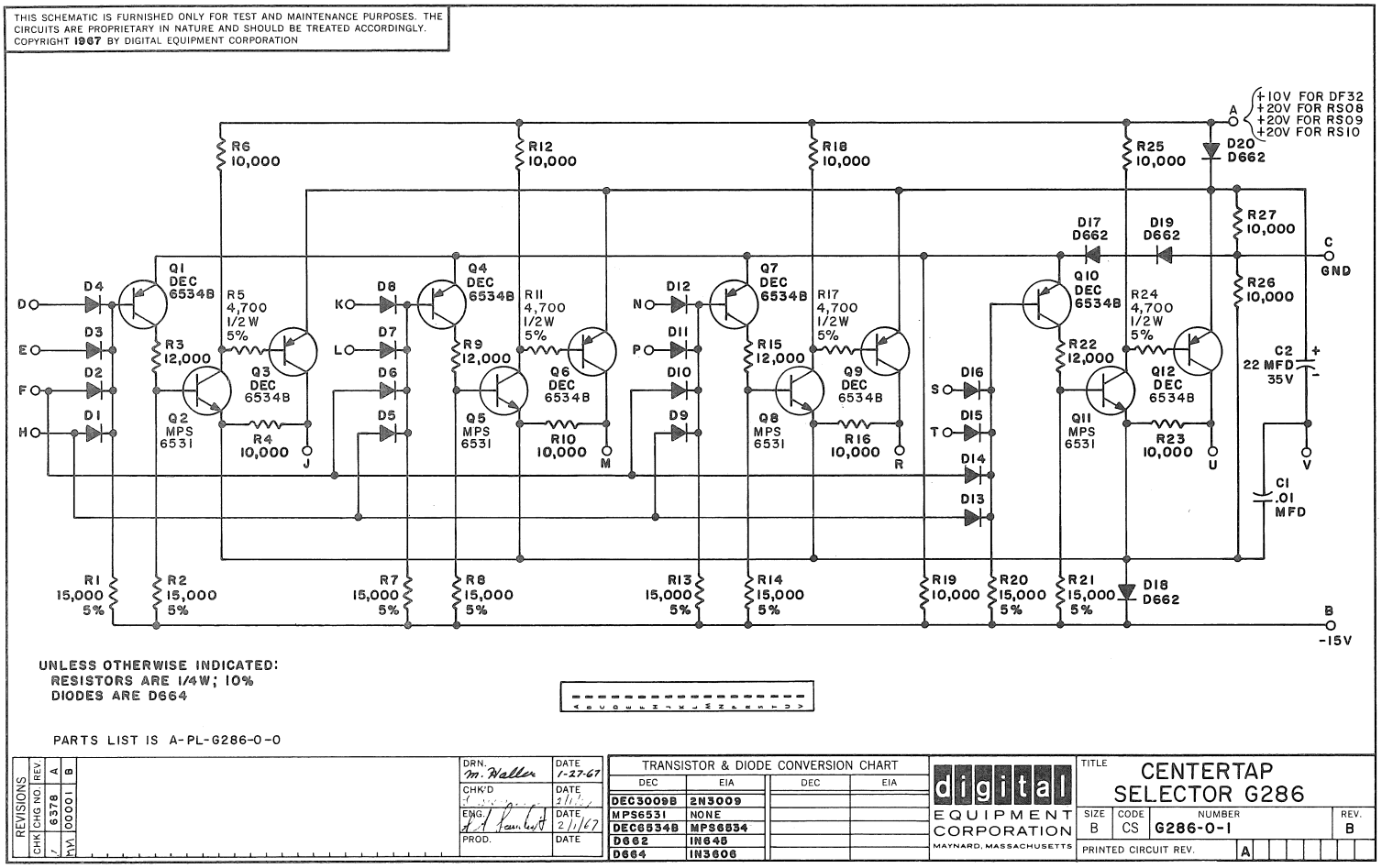


Figure 2-10 G286 Centertap Selector, Circuit Schematic

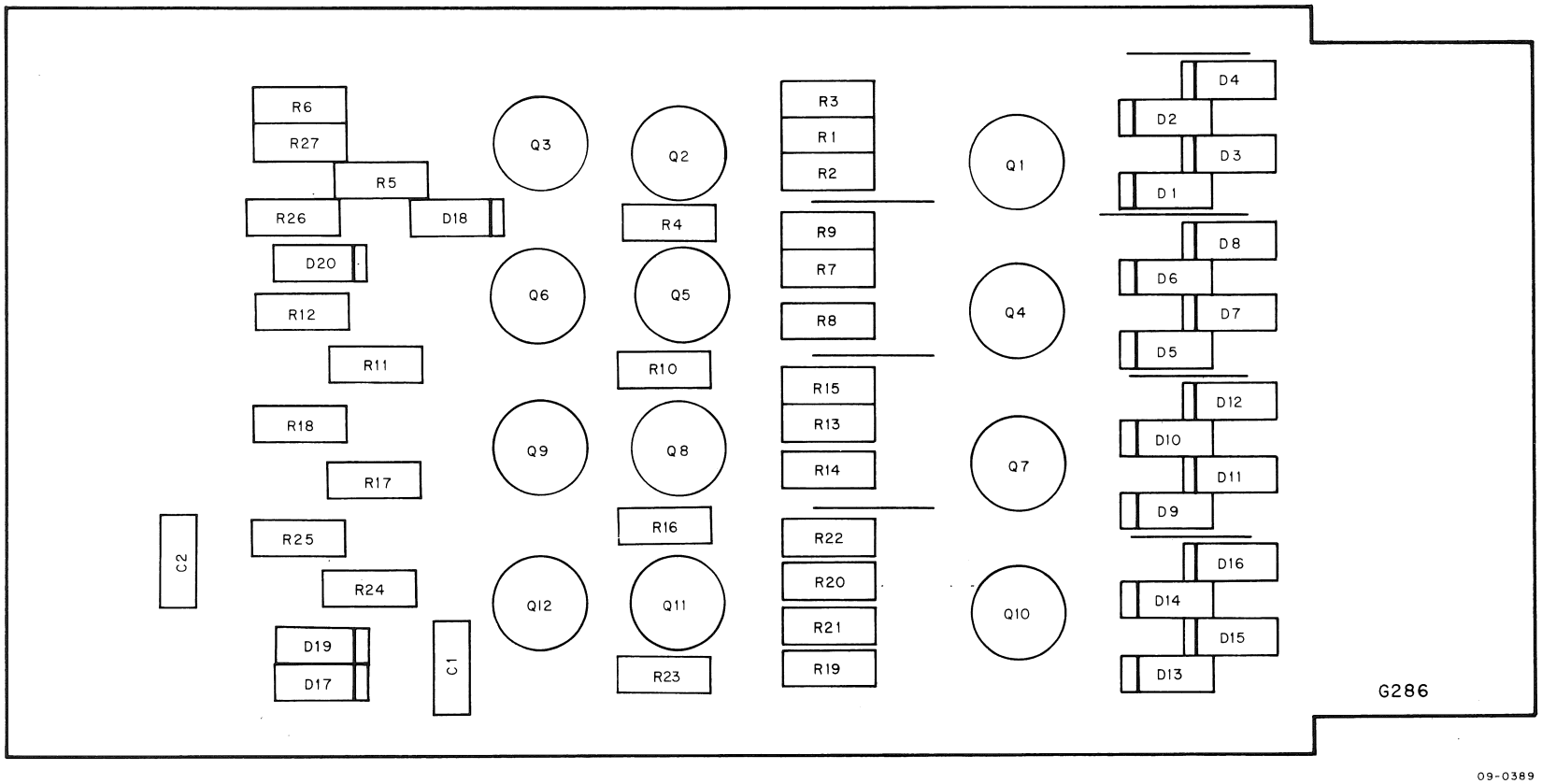


Figure 2-11 G286 Centertap Selector, Parts Location Diagram

2.5 G290 WRITER FLIP-FLOP

The G290 Writer Flip-Flop is a single-height board containing one JR flip-flop driving two AND gates and two power drivers. There are several gates to the input of the flip-flop (see Figures 2-12, 2-13, and 2-14).

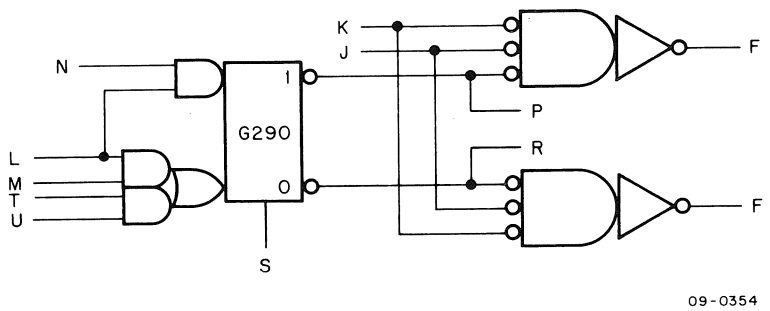


Figure 2-12 G290 Writer Flip-Flop, Block Schematic

Inputs: Voltage levels are 0 and -3V.

Pin	Function	Load
N,M,T,U,	Inputs to flip-flop	Each gate is a 1 mA
L	Input to flip-flop	load shared among
S	Direct Clear	its grounded inputs
K,J	Enable input to output driver gate	

Outputs: The E and F outputs are -15V or an open collector. The P and R outputs are 0 and -3V.

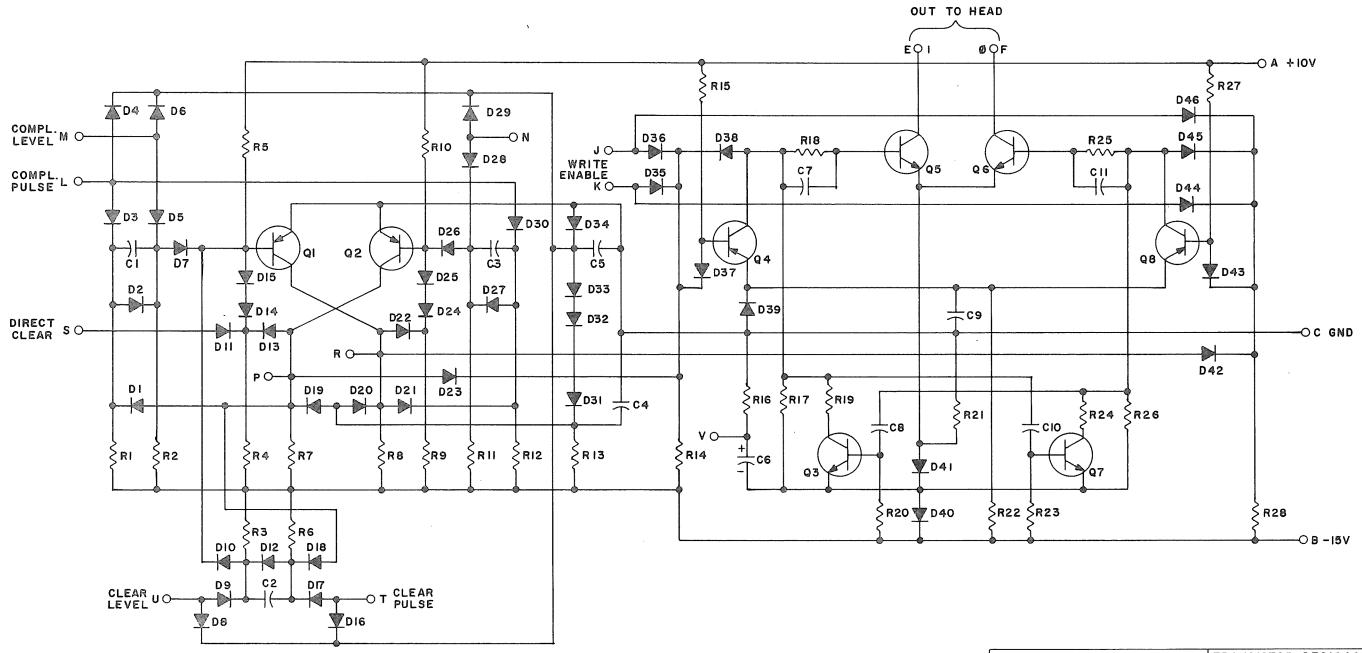
Pin	Function	Drive
E,F	Output to G285 Series Switch	150 mA
P,R	Test output of flip-flop	10 mA

Input/Output Delay: 90 ns

Power Dissipation: 1W

Application: This module supplies the -15V write voltage to the G285 Series Switch. Details are given in Paragraph 3.4.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION



Q5,Q6	TRANSISTOR DEC1008-S	1502155
Q4,Q8	TRANSISTOR DEC6534B	1503409-01
Q3,Q7	TRANSISTOR DEC3009B-S	1503100
Q1,Q2	TRANSISTOR 2N4258	1503321
R19,R24	RES. 100 1/4W 5% CC	1300229
R16	RES. 10 1/4W 10% CC	1300170
R15,R27	RES. 10K 1/4W 10% CC	1300481
R14,R28	RES. 3.3K 1/4W 5% CC	1300439
R25,R26	RES. 1.5K 1/4W 5% CC	1300391
R7,R8,R13,R17,R18,R20-R23,		
R5,R10	RES. 100K 1/4W 5% CC	1302466
R1-R4,R6,R9,R11,R12	RES. 7.5K 1/4W 5% CC	1301422
D37,D39,D40,D41,D43	DIODE D662	1100113
D14,D15,D24,D25,D31-D34,		
D35,D36,D38,D42,D44-D46	DIODE D664	1100114
D1-D13,D16-D23,D26-D30,		
C8,C10	CAP. 56MMF 100V 5% D.M.	1000012
C7,C11	CAP. 220MMF 100V 5% D.M.	1000021
C6	CAP. 47MFD 20V 20% S.TANT	1000079
C4,C5,C9	CAP. .01MFD 100V 20% DISC	1001610
C1,C2,C3	CAP. 82MMF 100V 5% D.M.	1000015
	PARTS LIST	A-PL-G290-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

REVISIONS: CHK | CHG NO. | REV.

DRN. M. Weller DATE 1-10-69
CHK'D W. Moore DATE 1-15-69
ENG. J. Hogan DATE 3/-
PROD. DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	1N645	DEC1008	MM1008
D664	1N3606		
2N4258	SAME		
DEC3009B	2N3009		
DEC6534B	MPS6534		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE WRITER FLIP FLOP G290

SIZE C | CODE CS | NUMBER G290-0-1 | REV

PRINTED CIRCUIT REV. A

Figure 2-13 G290 Writer Flip-Flop, Circuit Schematic

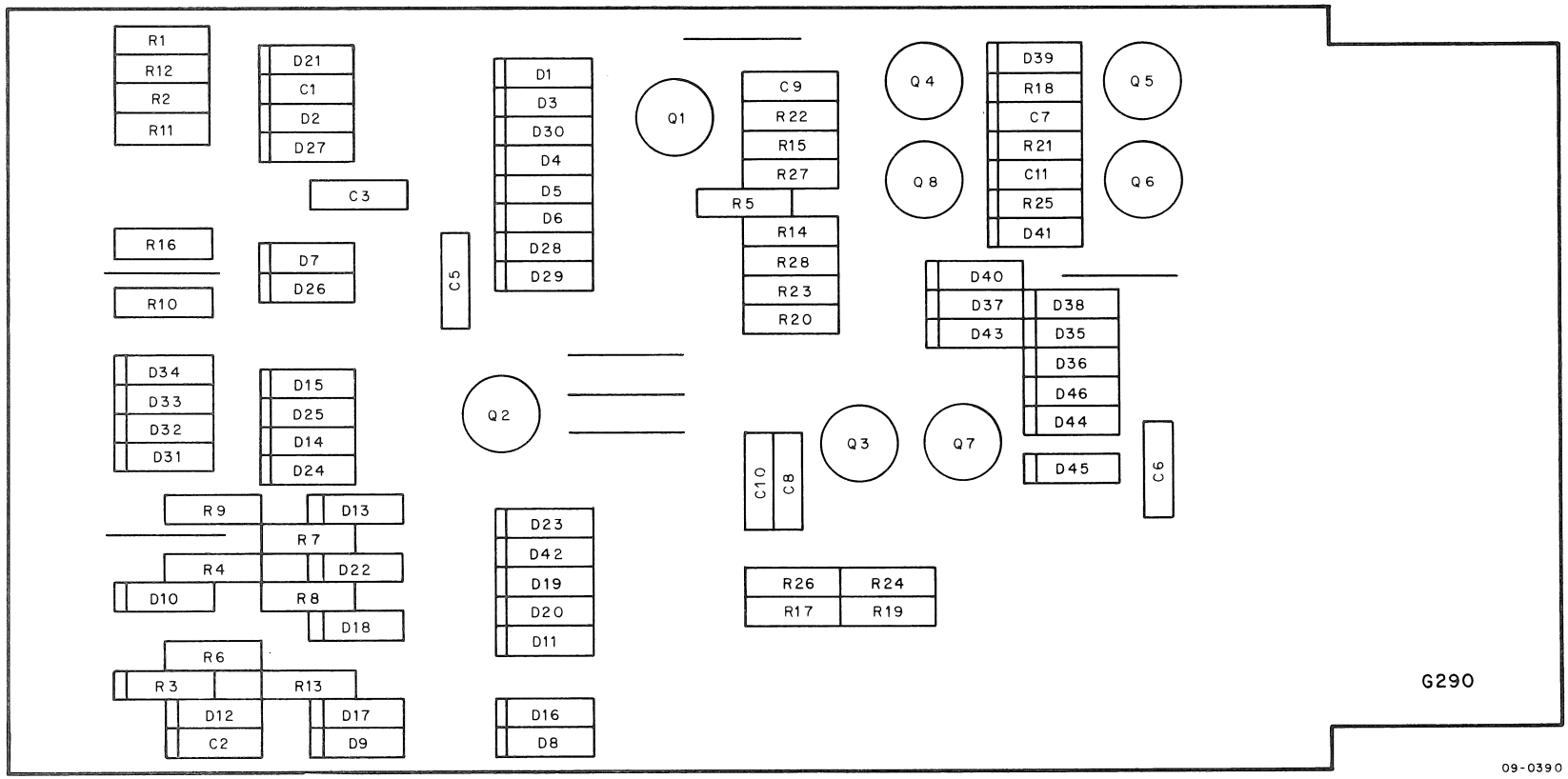


Figure 2-14 G290 Writer Flip-Flop, Parts Location Diagram

2.6 G681 B TRACK MATRIX

The G681 Track Matrix is a single-height board containing the resistors and diodes for eight DECdisk read/write heads (see Figure 2-15). A complete description of the G681's use in the read/write circuitry is given in Chapter 3.

2.7 G711 RF08 TERMINATOR BOARD

The G711 RF08 Terminator Board is a single-height board containing 15 terminating resistors that present 100Ω to ground at each input pin (see Figure 2-16).

Inputs:	100Ω to ground
Outputs:	None
Power Dissipation:	Approximately 90 mW per terminator
Application:	This board must plug into the output cable slot of the last RS09 on each DECdisk cable bus.

2.8 G775 INDICATOR PANEL

The G775 Indicator Panel is a connector card that provides isolation for logic levels and allows these levels to directly drive indicator bulbs without using light drivers (see Figure 2-17). The connector is designed to be used with the indicator panel, which supplies the necessary bias voltage.

Inputs:	All inputs are 0 and -3V with 3 units of load each.
Outputs:	The output connects a Flexprint cable to the indicator board.
Power Dissipation:	150 mW

2.9 G789 SIGNAL SIMULATOR CONNECTOR

The G789 Signal Simulator Connector is a connector board for Flexprint used on the RF09 side of the head-simulator cable (see Figure 2-18).

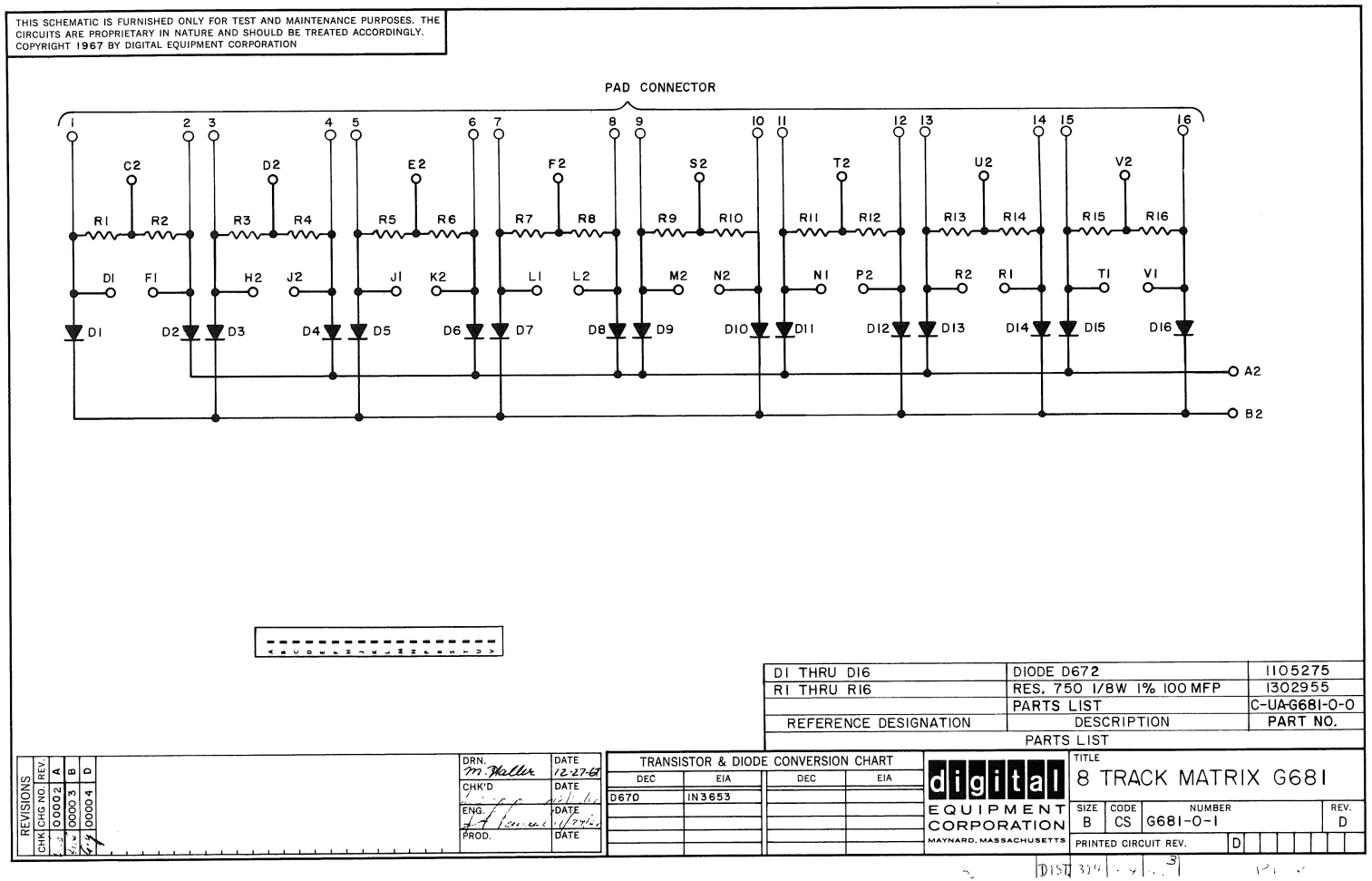


Figure 2-15 G681 Track Matrix, Circuit Schematic

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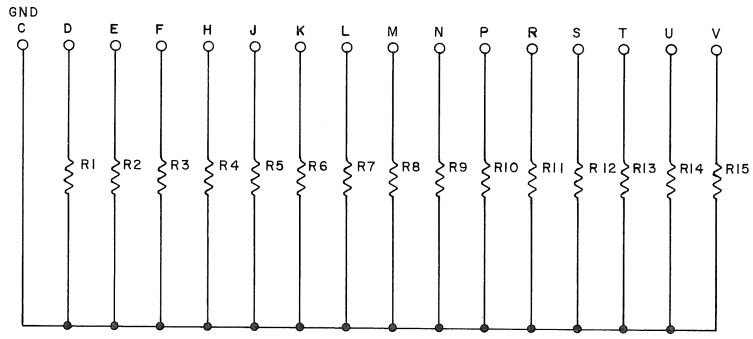


REFERENCE DESIGNATION	DESCRIPTION	PART NO
R1 - R15	RES. 100 1/4W 5% CC	1300229
	PARTS LIST	A-PL-G711-0-0

PARTS LIST

REVISIONS		
CHK	CHG NO.	REV.

DRN. M. Weller	DATE 8-2-68	
CHK'D. M. Fuller	DATE 8-9-68	
ENG. R. Briemo	DATE 9-9-68	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE RF08 TERMINATOR BOARD G711

SIZE	CODE	NUMBER	REV.
B	CS	G711-0-1	

PRINTED CIRCUIT REV. A

Figure 2-16 G711 RF08 Terminator Board, Circuit Schematic

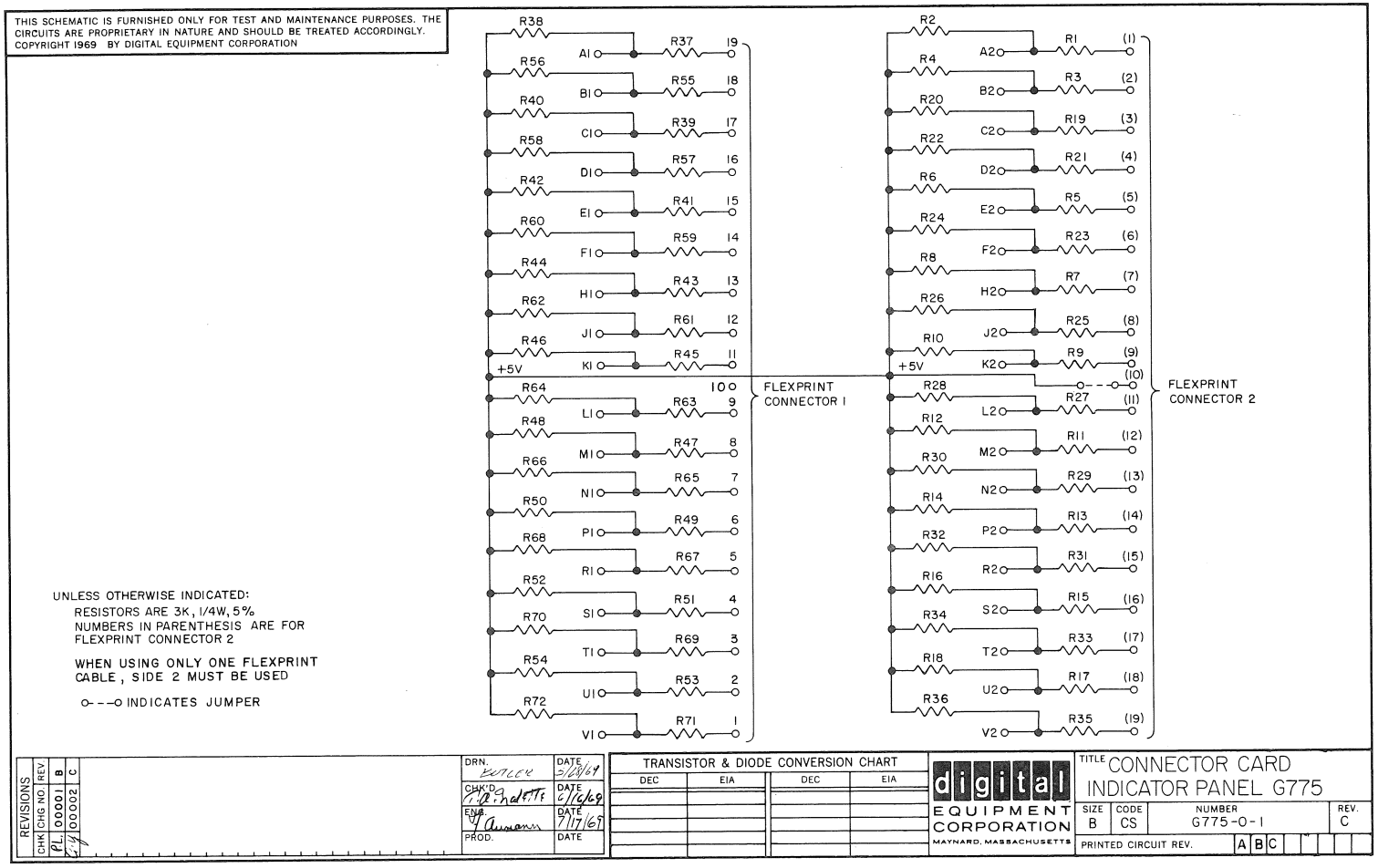


Figure 2-17 G775 Connector-Card Indicator Panel, Circuit Schematic

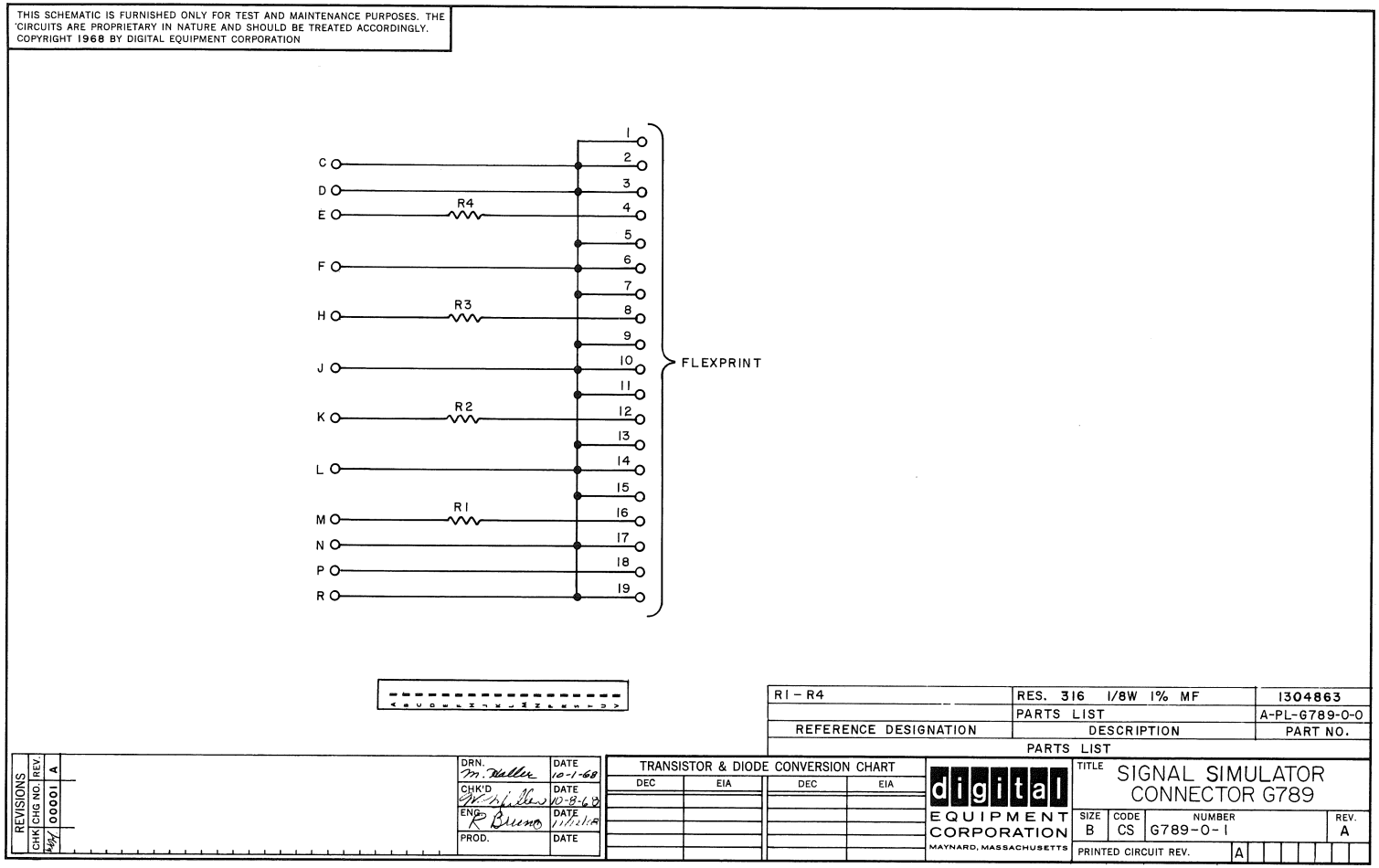


Figure 2-18 G789 Signal Simulator Connector, Circuit Schematic

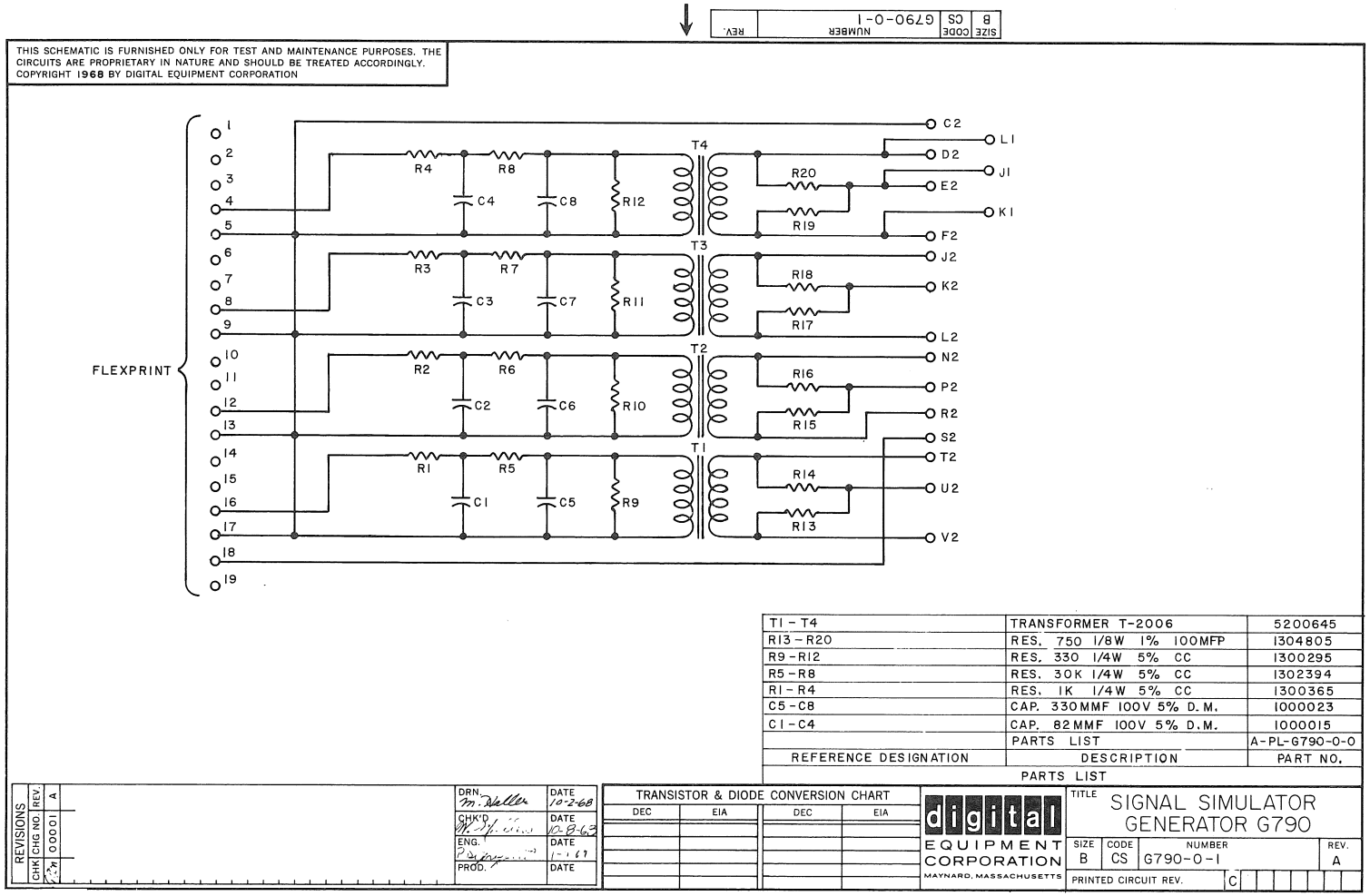
2.10 G790 SIGNAL SIMULATOR GENERATOR

The G790 card is on the RS09 side of the head-simulator cable. The card consists of 4 transformer networks that accept the outputs of the maintenance flip-flops and convert their transitions to signals that resemble the signals from the read heads of the disk assembly (see Figure 2-19).

2.11 G821 REGULATOR CONTROL

The G821 Regulator Control is a single-height board serving as a voltage regulator that supplies +5 Vdc to the TTL logic of the timing track writer. It is capable of supplying a maximum current of 6A, provided it is supplied with an air circulation of at least 200 cfm. Without cooling, the G821 is rated at 2A. This module was designed to be used with the PDP-15 memory and incorporates several features specifically serving the PDP-15 memory. For example, it supplies a 1A driver that is enabled when a memory OK signal is returned from memory. However, this feature is not used by the timing track writer.

Inputs:	Ordinarily, the inputs are rated at 8 Vdc, 11 Vdc, and -15 Vdc supplied by the PDP-15 power supply. However, the timing track writer uses +10 Vdc and -15 Vdc.
Outputs:	The timing track writer uses the regulated +5 Vdc output. This output can be varied between 4.5 and 5.5 Vdc by a potentiometer on the module. At 5 Vdc the regulation is 2 percent with a ripple of 25 mV peak-to-peak. The circuit schematic is given in Figure 2-20.



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
T1 - T4	TRANSFORMER T-2006	5200645
R13 - R20	RES. 750 1/8W 1% 100MFP	1304805
R9 - R12	RES. 330 1/4W 5% CC	1300295
R5 - R8	RES. 30K 1/4W 5% CC	1302394
R1 - R4	RES. 1K 1/4W 5% CC	1300365
C5 - C8	CAP. 330MMF 100V 5% D.M.	1000023
C1 - C4	CAP. 82MMF 100V 5% D.M.	1000015
	PARTS LIST	A-PL-G790-0-0

PARTS LIST

Figure 2-19 G790 Signal Simulator Generator, Circuit Schematic

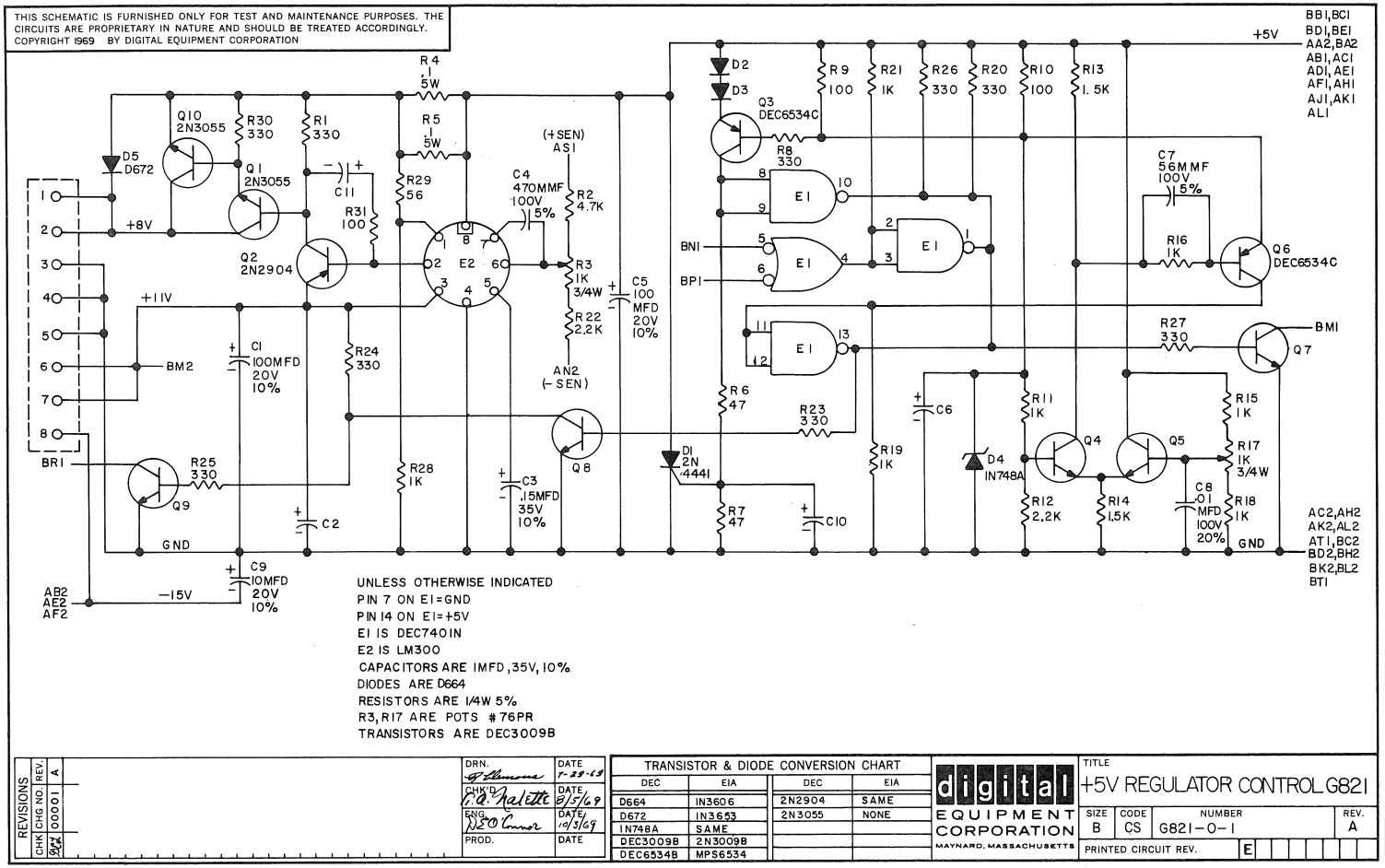


Figure 2-20 G821 +5V Regulator Control, Circuit Schematic

2.12 M104 MULTIPLEXER MODULE

The M104 Multiplexer Module is an M-series single-height module that contains a single multiplexer subsystem (see Figures 2-21, 2-23, and 2-24).

Inputs:

Input Pin	Load (Units)
H2	2.5
S2	1
H1	6
E2	3
N1	1
F2	1-1/4
K2	68Ω Termination
S2	1

Outputs: The output gates can drive as follows:

Output Pin	#Loads It Can Drive
U2	5
J2	8
P1	9
S1	10
E1	10
F1	10
M2	PDP-15 I/O Bus Compatible (30 units)
J1	7

Power: 1W

Application: The M104 module has been designed specifically for positive logic controllers of PDP-9 or PDP-15 peripherals. It is used in all controllers that make use of the API or data channel facilities in the I/O processor. It accepts a request from the controller logic at its FLAG (1) H input and synchronizes this request to the I/O SYNC H pulses issued from the I/O processor. These pulses are fed into SYNC of the M104 and immediately set the REQ flip-flop. The REQ flip-flop can be monitored through pins J2 and U2. The I/O processor responds to a request with a GRANT, and ENA is set. This flip-flop is generally used to gate any address information onto the bus; e.g., the API trap address or the word count address of the multicycle data break. The next SYNC pulse sets ENB. This flip-flop is generally used to control data-gating and transfer direction; e.g., device selector enable and RD RQ.

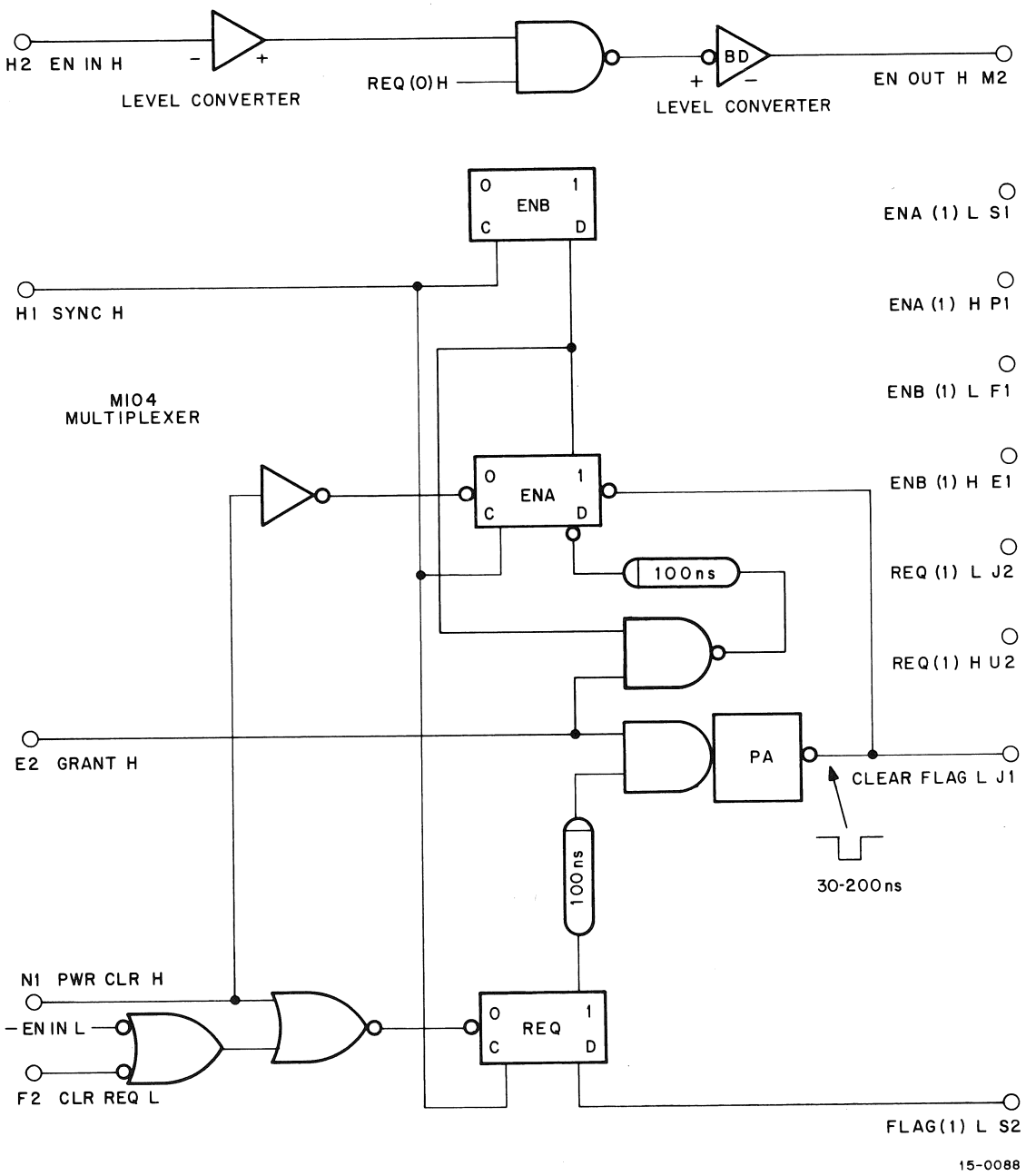


Figure 2-21 M104 Multiplexer, Block Schematic

The REQ flag can be reset through pin F2 (CLR RQ) by the controller logic. Pin N1 should be tied to POWER CLEAR or its equivalent.

The enabling level ENABLE IN holds REQ off if it arrives as a negative level. When REQ is set (if ENABLE IN is positive), ENABLE OUT goes negative and the next peripheral on the bus receives it as a negative ENABLE IN. In this way the M104 establishes priorities among devices on the same API level or among devices that use the data channel. A timing diagram for the M104 is given in Figure 2-22.

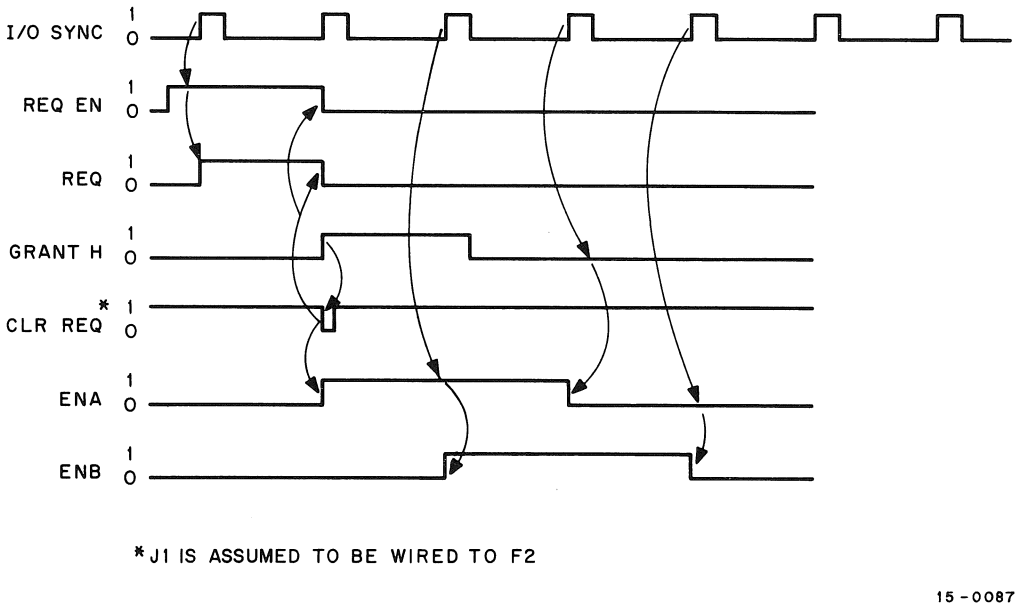


Figure 2-22 M104, Multiplexer Timing Diagram

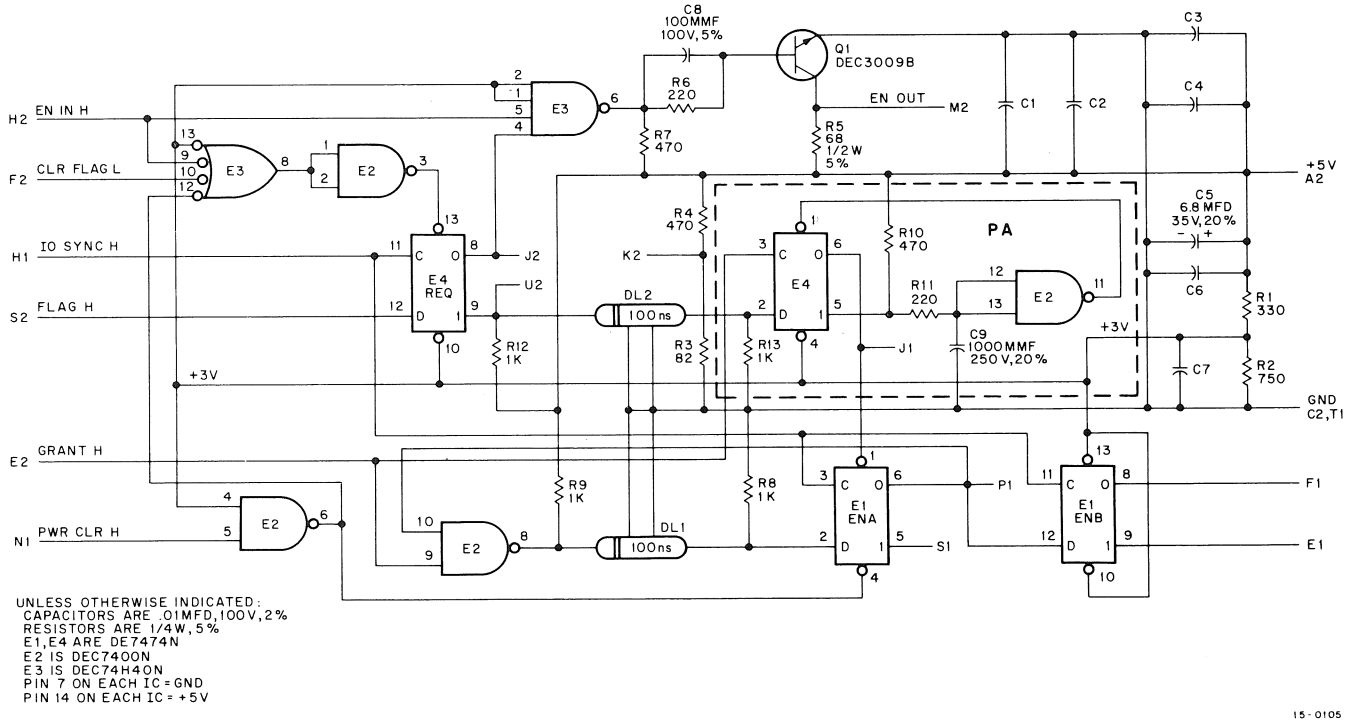


Figure 2-23 M104 Multiplexer, Circuit Schematic

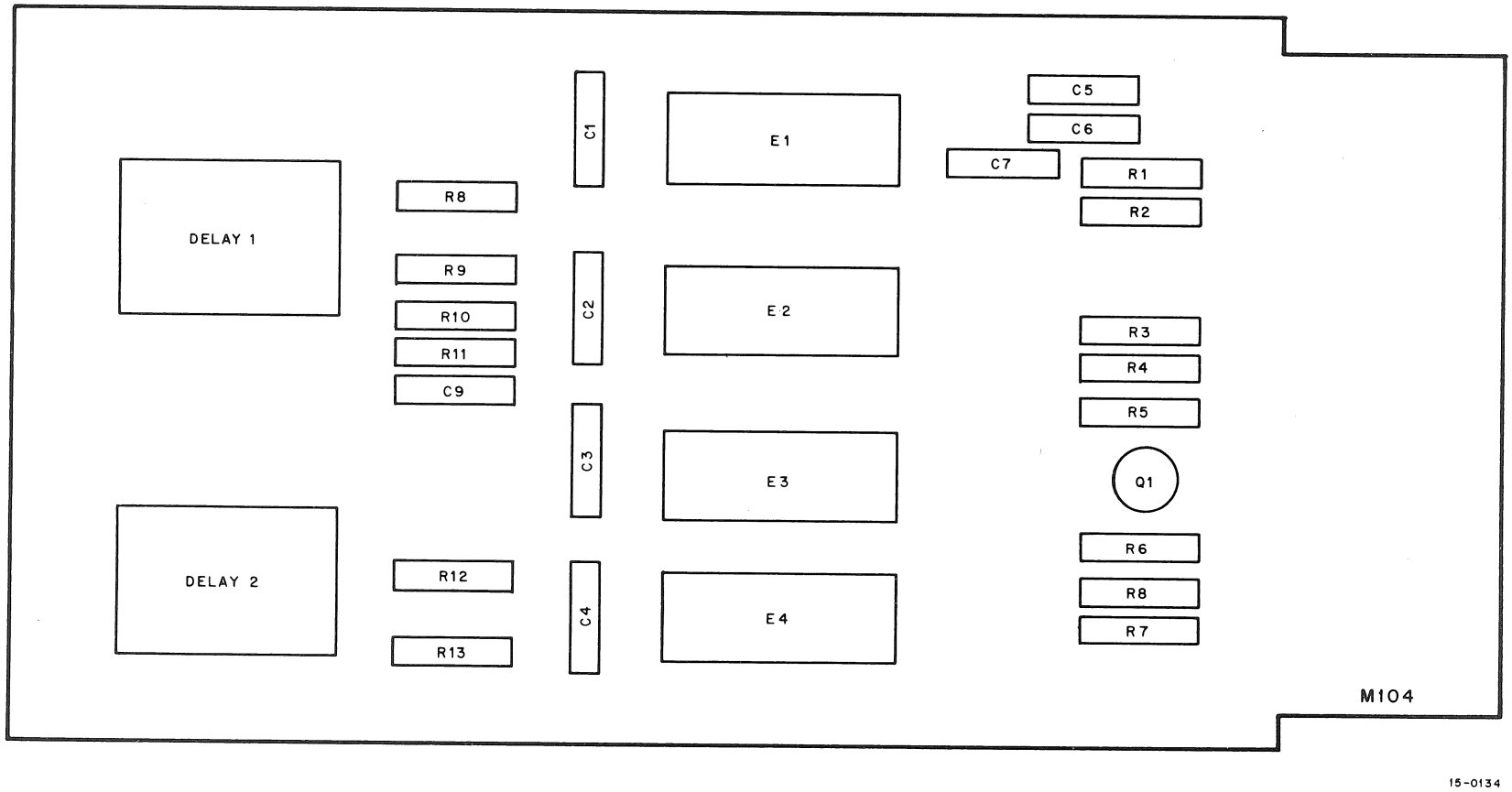


Figure 2-24 M104 Multiplexer, Parts Location Diagram

2.13 M216 SIX FLIP-FLOPS

M216 is a single-height module containing six D flip-flops (see Figure 2-25). All flip-flops operate independently except for their clear line, which is shared among three flip-flops.

Data must be present at the D input 20 ns before the clock pulse and should remain 5 ns after the leading edge of the clock pulse has passed the threshold voltage. The flip-flop settles in 50 ns. The CLOCK, DIRECT SET, and CLEAR inputs must be present for at least 30 ns.

Inputs: Voltages are standard TTL levels.

Pin	Function	Load
B1,D2,H1,L2,N1,S2	C Inputs	2 units
C1,E2,J1,M2,P1,T2	D Inputs	1 unit
D1,F2,K1,N2,R1,U2	DIRECT SET	2 units
A1,K2	DIRECT CLEAR	9 units

Outputs: Voltages are standard TTL levels. Each output is capable of driving 10 unit loads.

Input/Output Delay: 50 ns

Power Dissipation: 435 mW

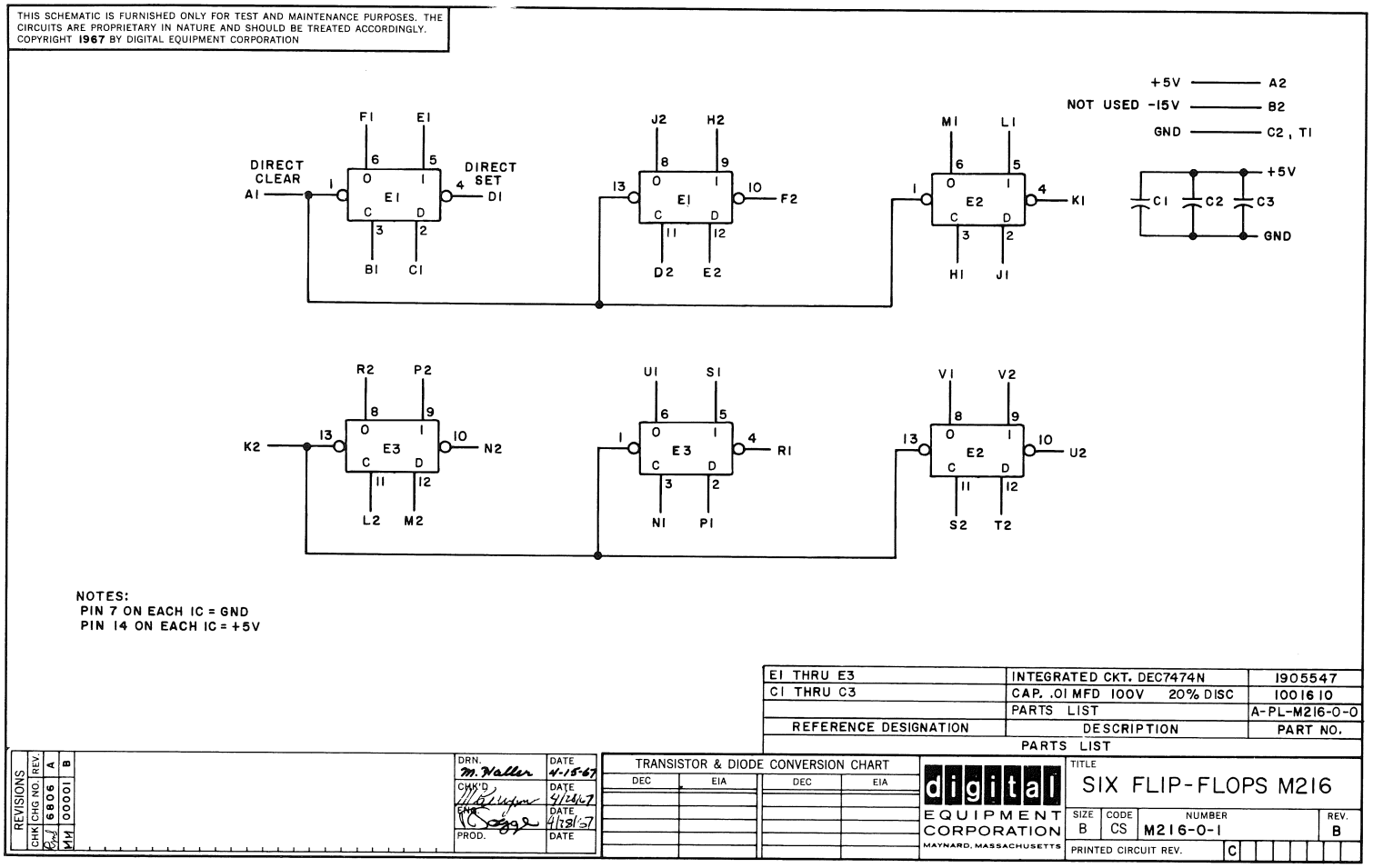


Figure 2-25 M216 Six Flip-Flops, Circuit Schematic

2.14 M311 TAPPED DELAY LINE

M311 is a single-height board containing two tapped delay lines (see Figures 2-26 and 2-27). Each delay line has ten taps, providing fixed delays from 25 ns to 250 ns. An input NAND gate to the delay line provides an additional delay of 10 ns. Input impedance of the delay line is 100Ω at ±5%.

Inputs: Voltages are standard TTL levels. Input loading is 1.25 units.

Outputs: Voltages are standard TTL levels. Each output can drive 1.25 units. Maximum total drive is 6 units. Wire lengths should be kept to a minimum (less than 6 inches).

Input/Output Delay:

Pin	Delay
K2,J2	35 ns
L2,K1	60 ns
M2,L1	85 ns
N2,M1	100 ns
P2,N1	135 ns
R2,P1	160 ns
S2,R1	185 ns
T2,S1	210 ns
U2,U1	235 ns
V2,V1	260 ns

Power Dissipation: 850 mW

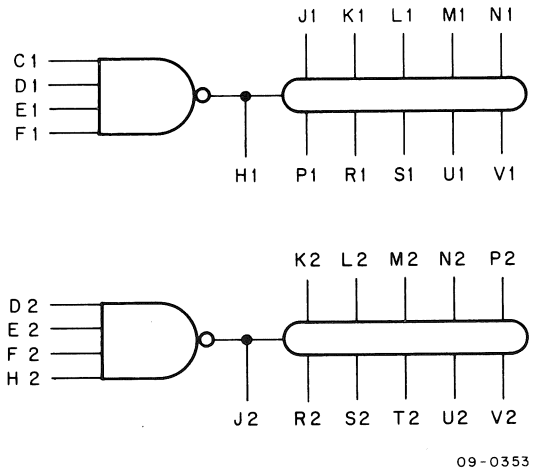


Figure 2-26 M311 Tapped Delay, Block Schematic

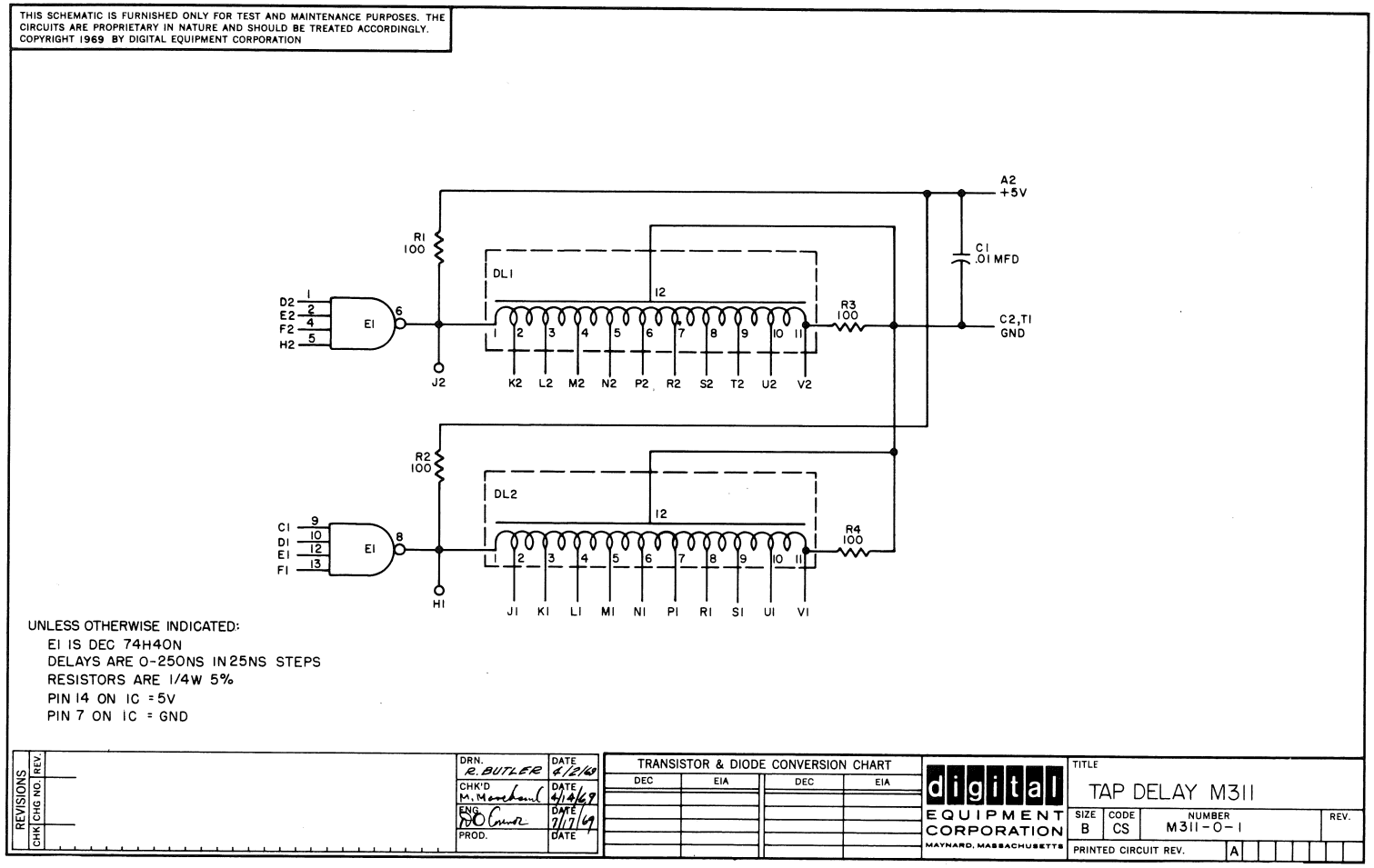


Figure 2-27 M311 Tapped Delay, Circuit Schematic

2.15 M149 9 X 2 NAND "WIRED OR" MATRIX

The M149 is a single-height module containing two sets of 9-open collector NAND gates wired together in an OR function to form nine output pins. The M149 also includes a pulse amplifier (see Figure 2-28).

Inputs:	Voltages are standard TTL levels. Input loading is 1 unit per input.
Outputs:	Voltages are standard TTL levels. Each output except V1 is an open collector that can sink 16 mA. The output at V1 can drive 10 unit loads.
Input/Output Delay:	10 ns at output
Power Dissipation:	350 mW
Application:	This module is generally used to gate signals onto an open collector bus.

2.16 M500 NEGATIVE RECEIVER MODULE

M500 is an M-series single-height module containing eight I/O bus receivers that can accept negative logic levels and convert them to positive levels (see Figures 2-29, 2-30, and 2-31). Each M500 receiver has a negative input clamped to 0V and -3V. The threshold switching level is -1.5V with an input current of 100 μA.

Inputs:	Minimum input impedance at 0V: 30 kΩ Maximum current load to bus: 100 μA Inputs are standard negative logic levels of 0 and -3V.
Outputs:	Fan Out Output No. 1: 12 units Output No. 2: 11 units Input/Output No. 1 delay: 50 ns Input/Output No. 2 delay: 40 ns Outputs are standard TTL logic levels.
Power Dissipation:	750 mW max from -15V 800 mW max from +5V
Application:	The M500 module was designed to receive PDP-9 I/O bus signals for devices using positive logic. It provides a high input impedance.

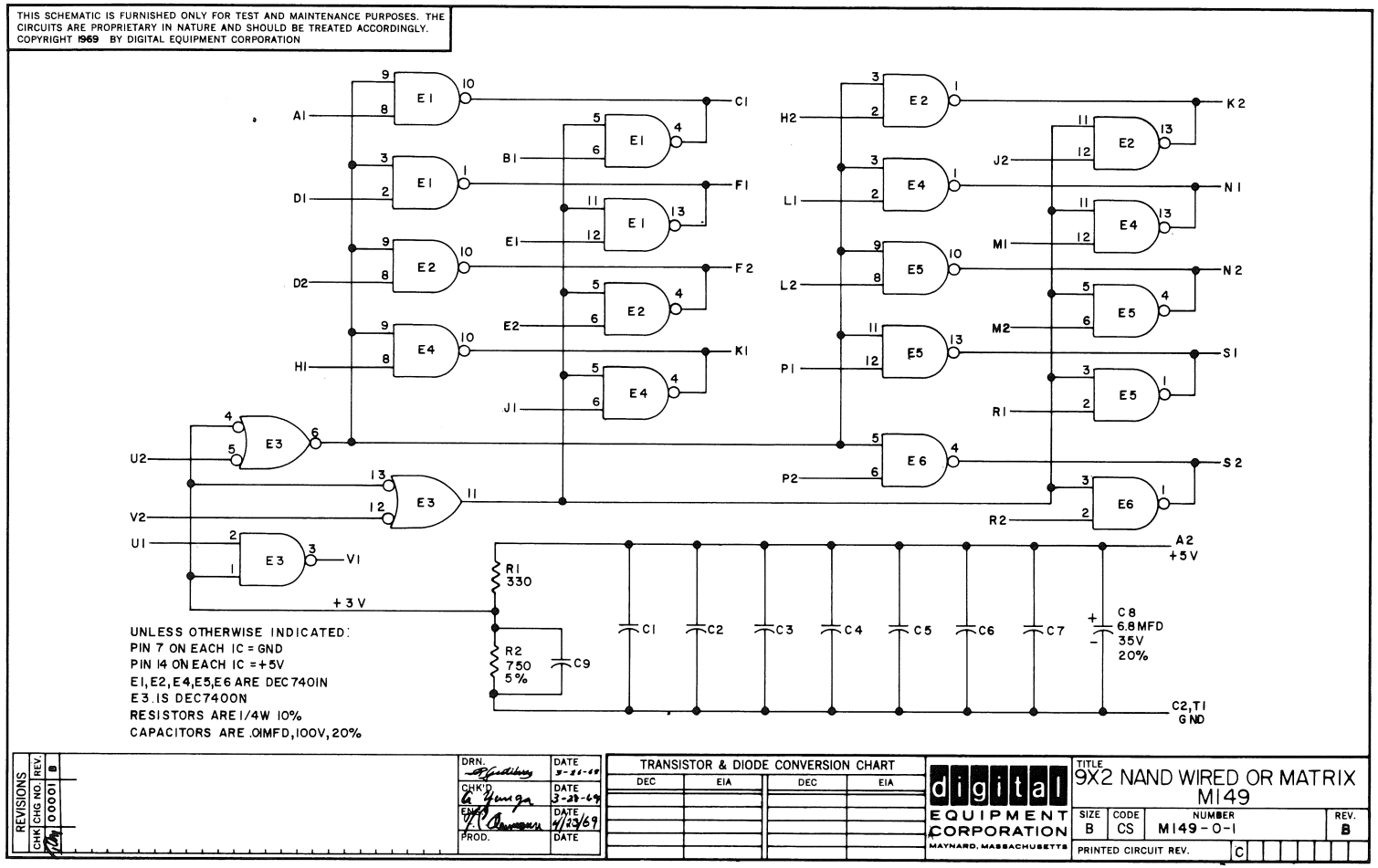


Figure 2-28 M149 9 x 2 NAND Wired OR Matrix

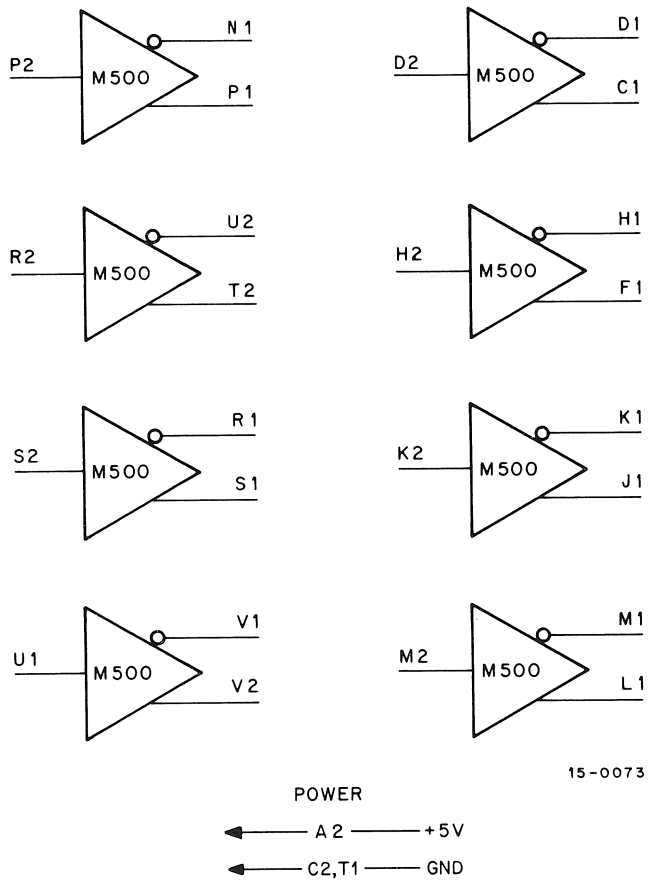


Figure 2-29 M500 Negative Receiver, Block Schematic

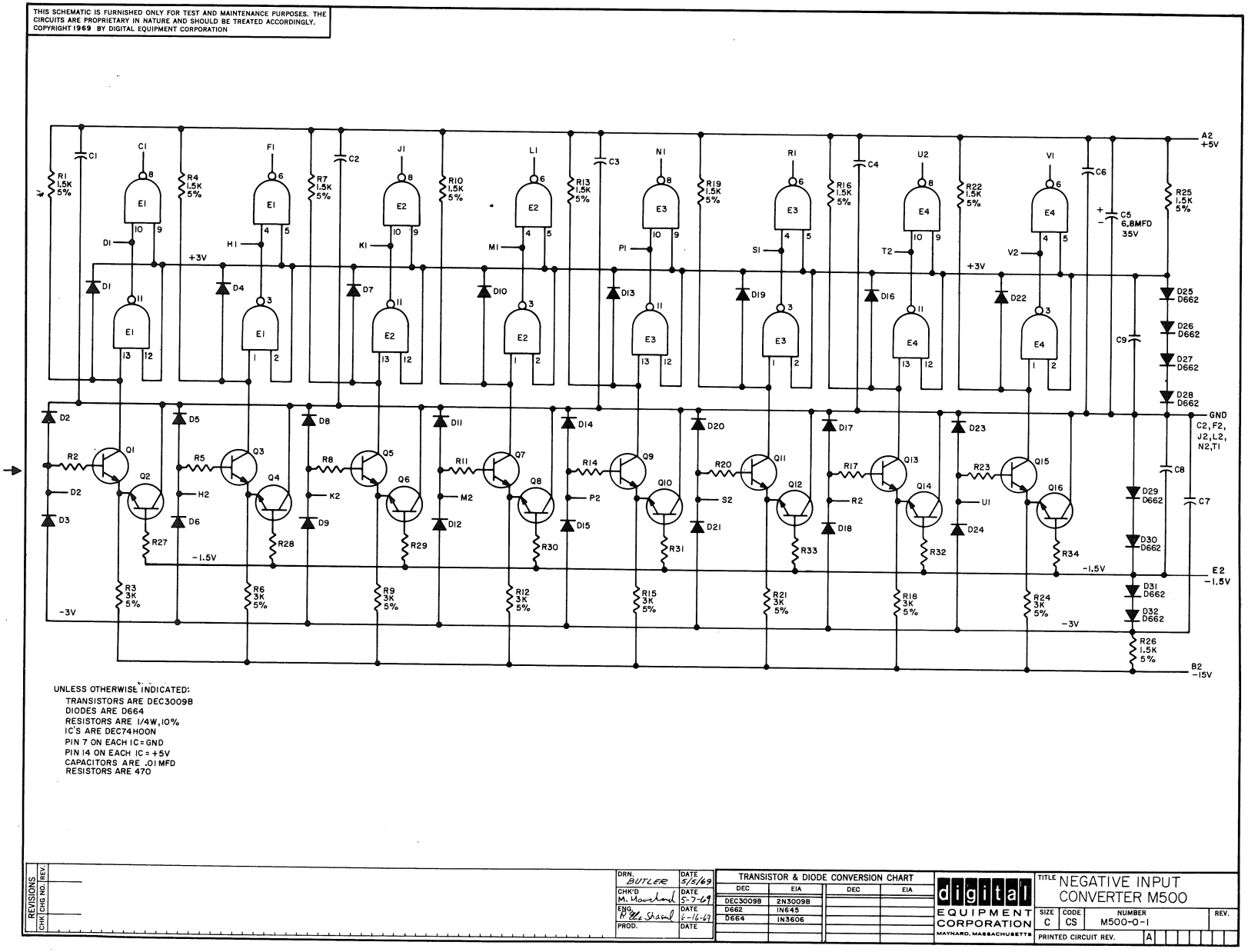


Figure 2-30 M500 Negative Receiver, Circuit Schematic

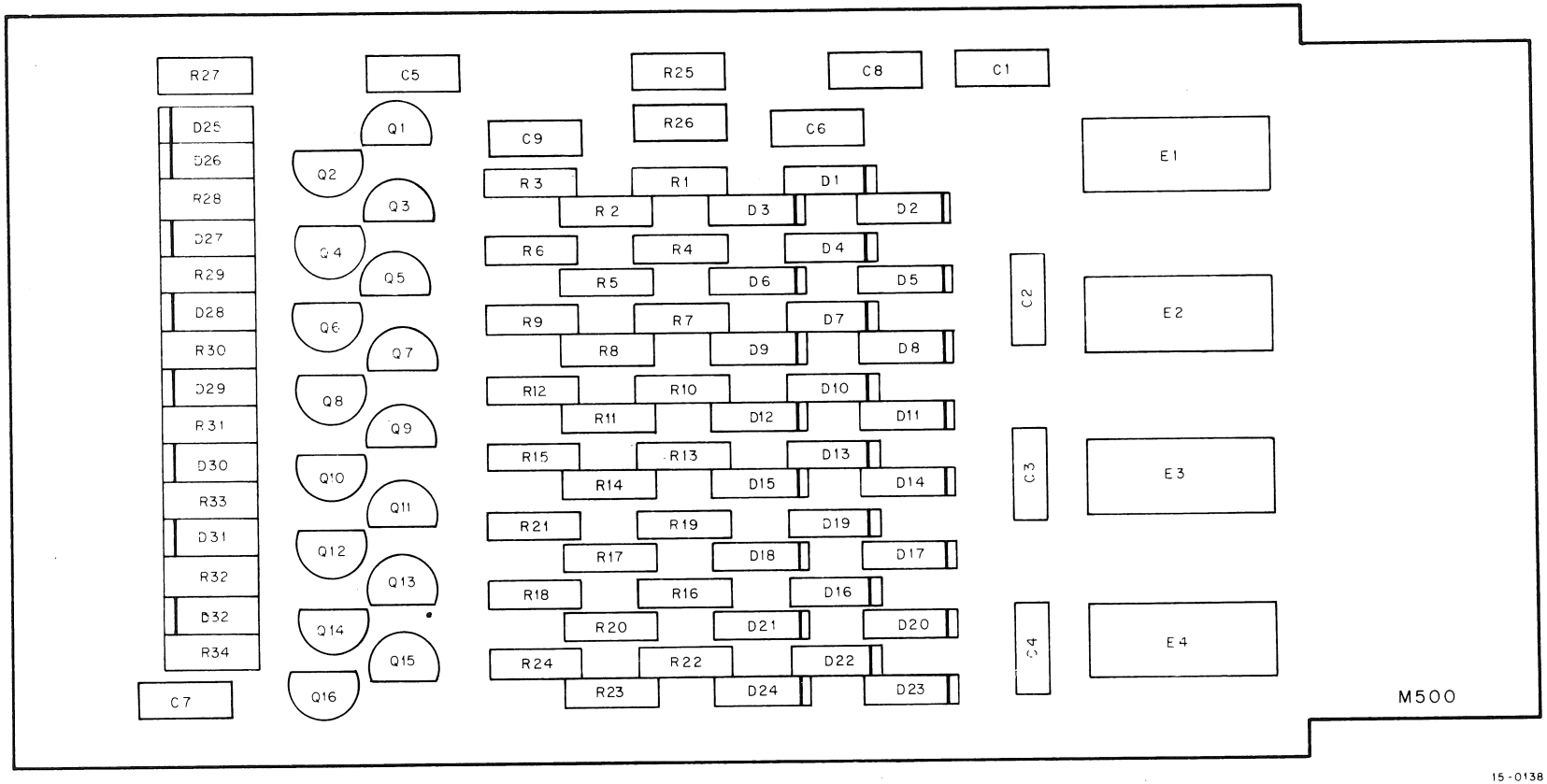


Figure 2-31 M500 Negative Receiver, Parts Location Diagram

2.17 M632 NEGATIVE DRIVER MODULE

The M632 is an M-series single-height module containing eight driver circuits (see Figures 2-32, 2-33, and 2-34). It accepts positive logic signals and converts them to negative logic levels.

Each driver consists of a TTL input gate and a negative open-collector output driver clamped to ground and -3V.

Inputs:	Standard TTL levels – input current load at 0V is 1.25 units.
Outputs:	Outputs are standard negative logic levels. Risetime: 15 ns Falltime: 15 ns with 1.5 kΩ to -15V at output
Input/Output Delay:	50 ns max
Power Dissipation:	600 mW from -15V max 900 mW from +5V max
Application:	The M632 is used to convert positive logic signals to negative logic levels that drive the PDP-9 negative I/O bus. The M632 is pin compatible with the M622.

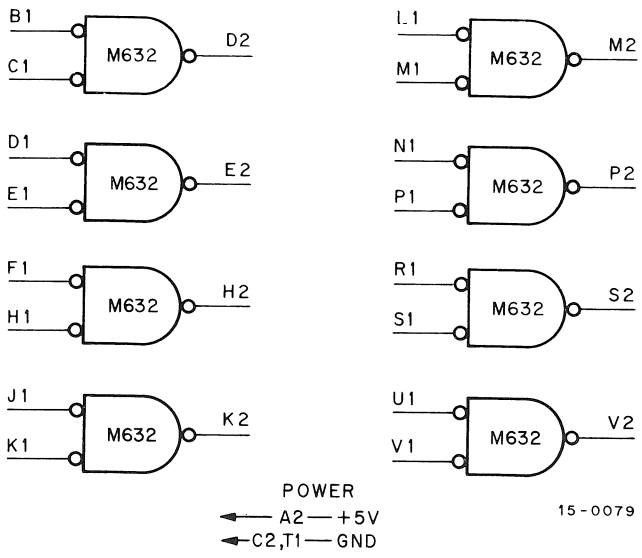


Figure 2-32 Negative Driver, Block Schematic

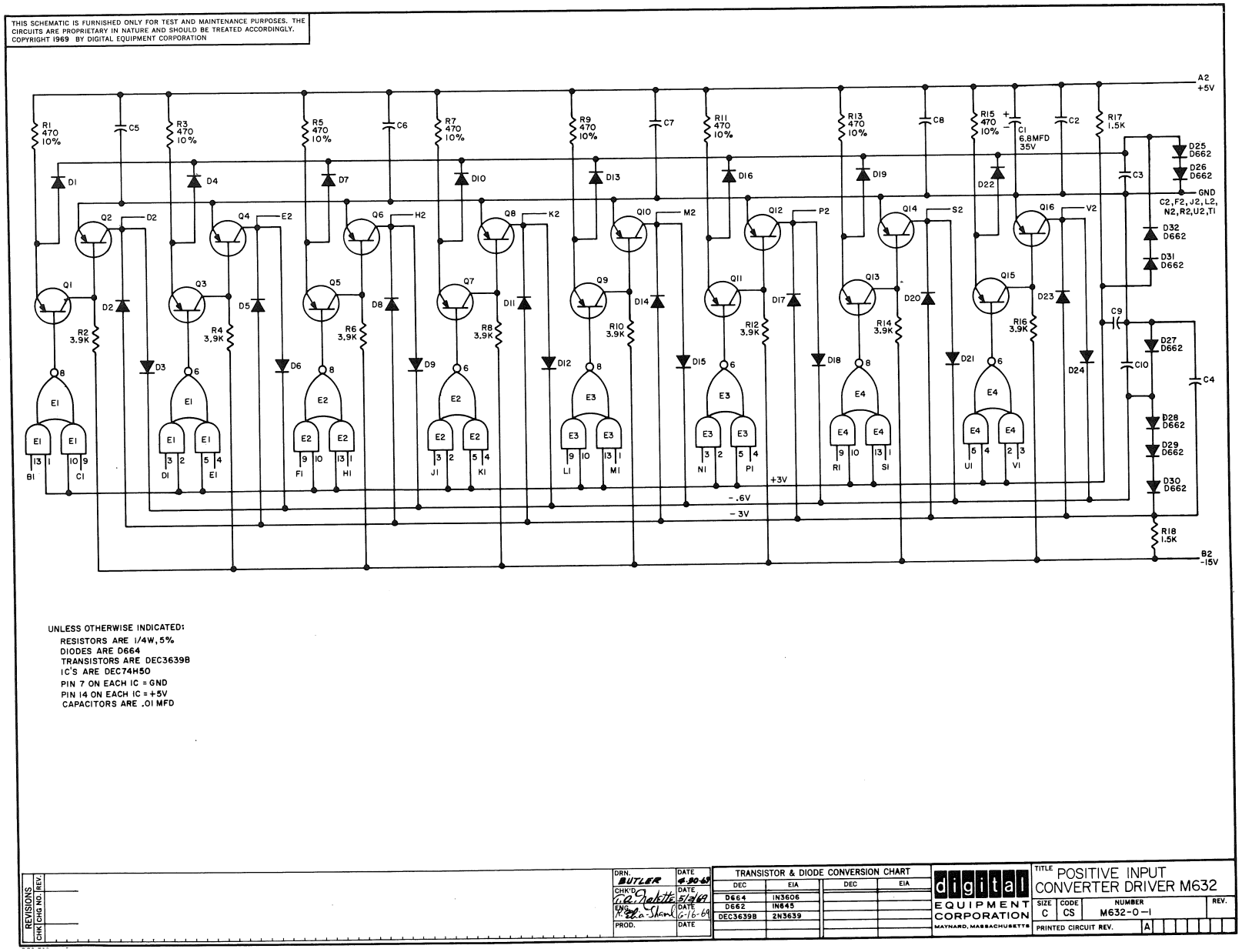
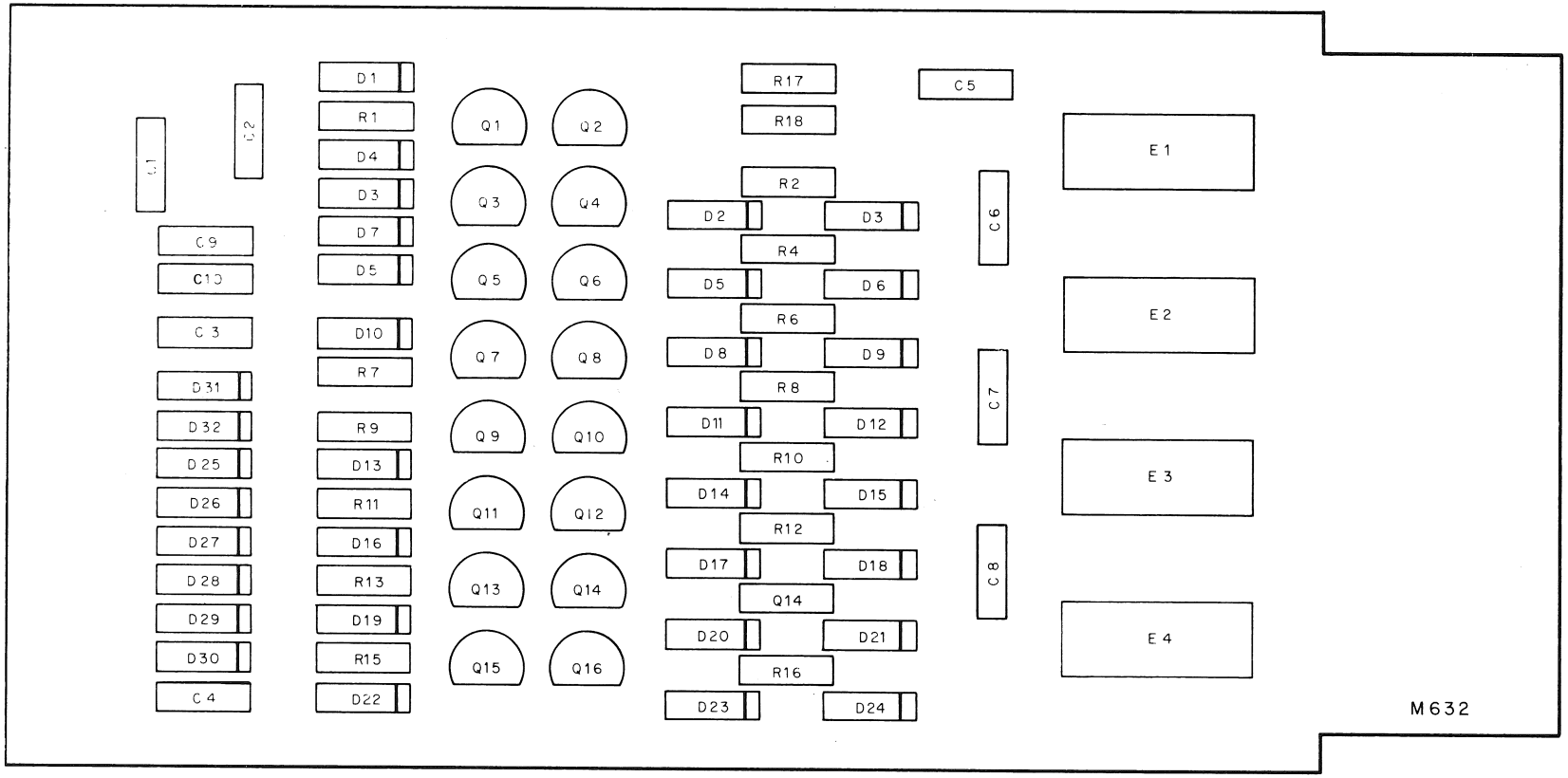


Figure 2-33 M632 Negative Driver, Circuit Schematic



15-0140

Figure 2-34 M632 Negative Driver, Parts Location Diagram

2.18 705B POWER SUPPLY

The 705B Power Supply provides the logic power needed for the DECdisk system (see Figures 2-35 and 2-36). It is designed for 50/60 Hz single-phase input.

The 705B can be driven from the following voltage and frequency combinations by selection of the appropriate taps.

100 Vac ± 15%	50 Hz ± 2%
115 Vac ± 15%	50 Hz ± 2%
200 Vac ± 15%	50 Hz ± 2%
215 Vac ± 15%	50 Hz ± 2%
230 Vac ± 15%	50 Hz ± 2%
120 Vac ± 15%	60 Hz ± 2%
240 Vac ± 15%	60 Hz ± 2%

The 705B supply includes a primary autotransformer to supply 5A at 120 Vac, regardless of any line voltage fluctuations.

Logic Power: The dc-output voltages, as stated below, must be maintained under the following conditions:

Line variations of ± 15% of nominal line voltage.
Load variations of 1/2-load to full load.
Line frequency variations of ± 2% nominal line frequency.

Output Voltages:	+10 Vdc	I (max)	3.5A
		Regulation	+9.4 Vdc to +11.0 Vdc
		Ripple (max)	300 mV
	-15 Vdc	I (max)	24A
		Regulation	-14.5 Vdc to -16 Vdc
		Ripple (max)	700 mV
Two Floating 10 Vdc:	Each	I (max)	4A
		Regulation	9.4 Vdc to 11.0 Vdc
		Ripple (max)	300 mV

Under loss of power for 25 milliseconds, the drops for the various output dc-voltages are as follows:

+10 Vdc	1V
±19 Vdc	1V
-15 Vdc	2.5V

Input Surge Current Under Full Load:

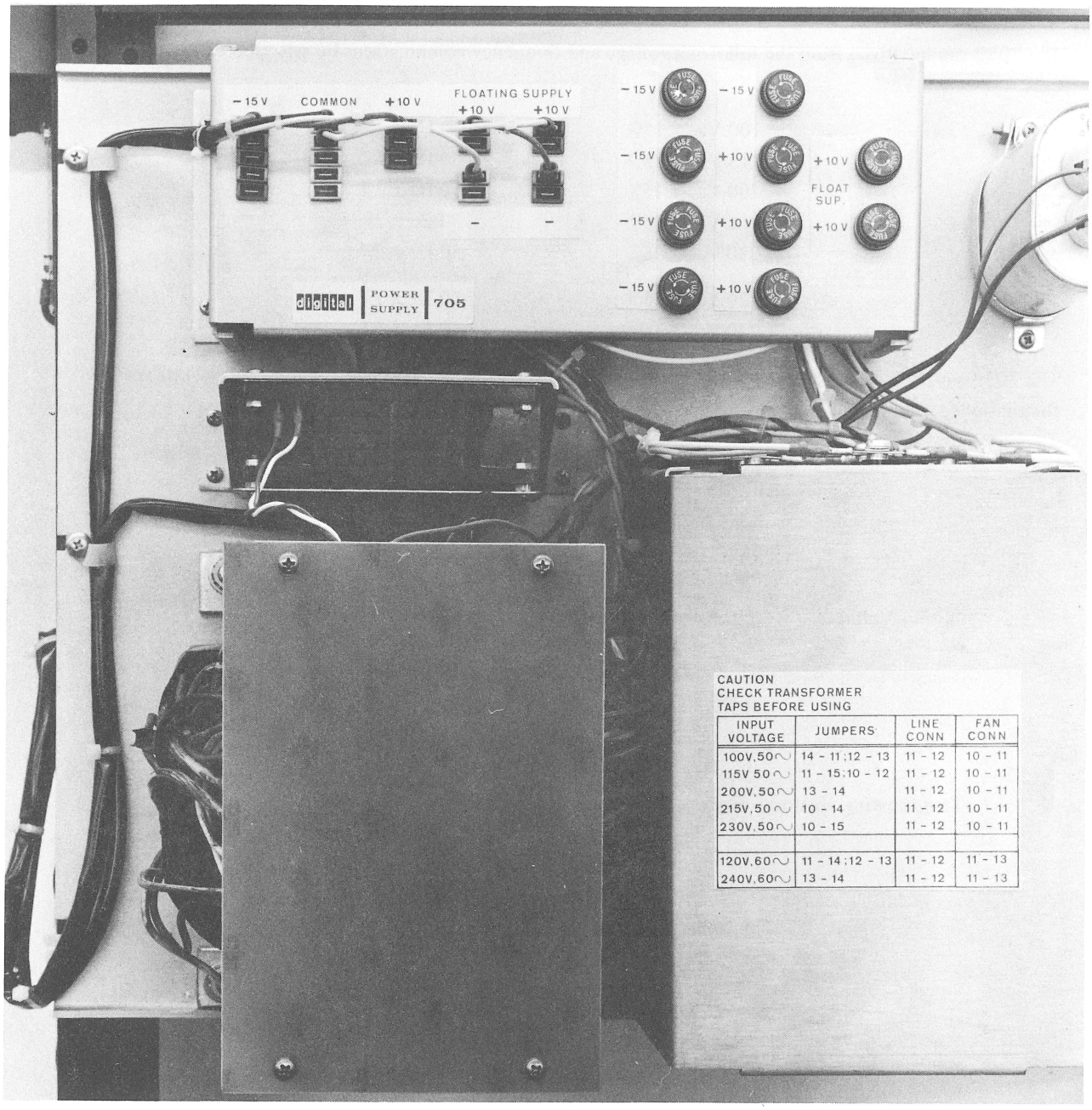
7.5A at 120 Vac, 60 Hz input

Recurrent Peak Current Input:

5.0A at 120 Vac, 60 Hz input

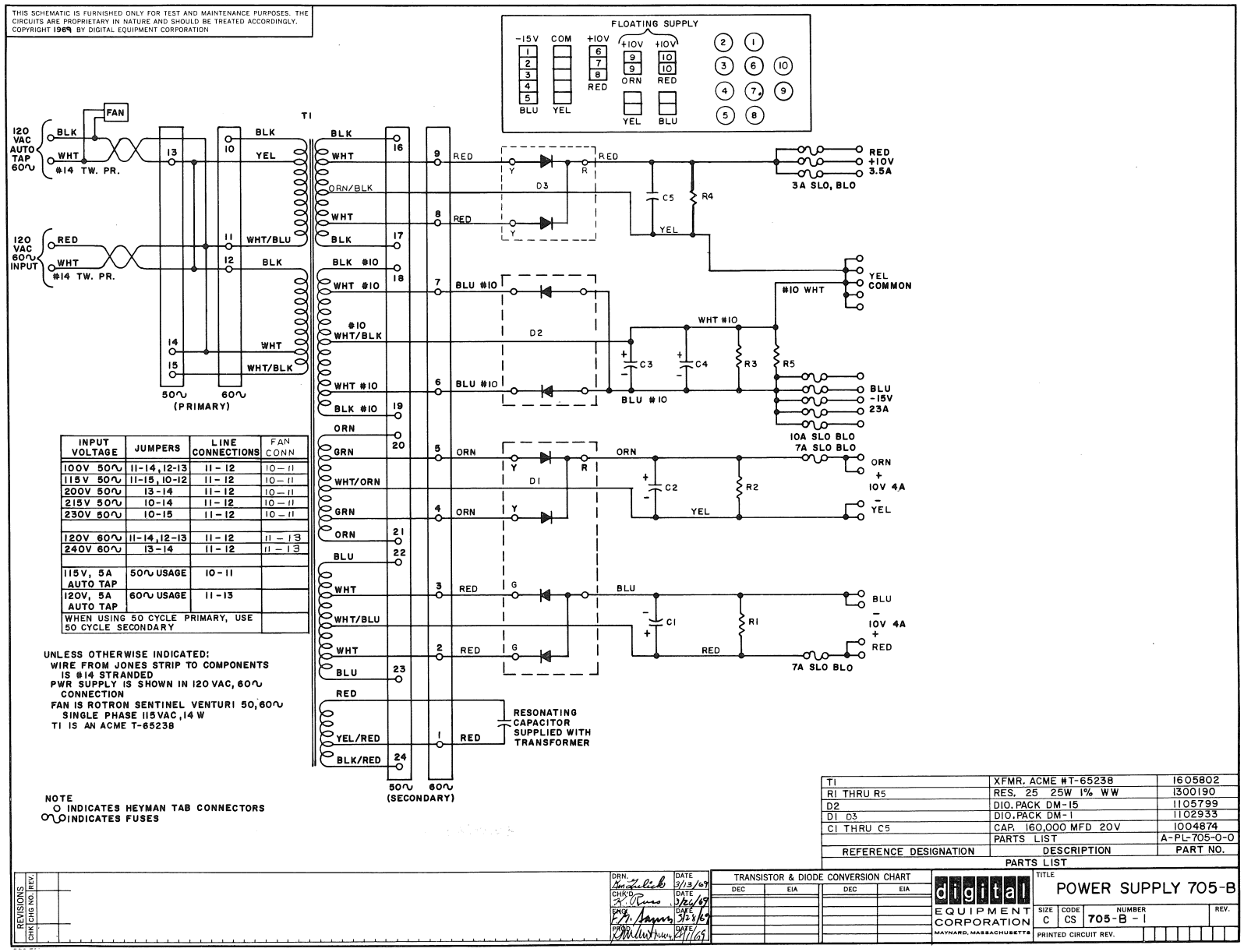
2.19 716 INDICATOR SUPPLY

The 716 Indicator Supply is designed to be used with the PDP-15 system indicator panels (see Figure 2-37). Its output is between 7 and 9 Vdc at 4.5A (black and orange terminals). An ac-signal source is also supplied at the white and blue terminals. Neither terminal should be grounded. This signal can be used as a clock or trigger for a synchronizing system.



INPUT VOLTAGE	JUMPERS	LINE CONN	FAN CONN
100V,50∿	14 - 11;12 - 13	11 - 12	10 - 11
115V 50∿	11 - 15;10 - 12	11 - 12	10 - 11
200V,50∿	13 - 14	11 - 12	10 - 11
215V,50∿	10 - 14	11 - 12	10 - 11
230V,50∿	10 - 15	11 - 12	10 - 11
120V,60∿	11 - 14;12 - 13	11 - 12	11 - 13
240V,60∿	13 - 14	11 - 12	11 - 13

Figure 2-35 705B Power Supply



INPUT VOLTAGE	JUMPERS	LINE CONNECTIONS	FAN CONN
100V 50~	11-14, 12-13	11-12	10-11
115V 50~	11-15, 10-12	11-12	10-11
200V 50~	13-14	11-12	10-11
215V 50~	10-14	11-12	10-11
230V 50~	10-15	11-12	10-11
120V 60~	11-14, 12-13	11-12	11-13
240V 60~	13-14	11-12	11-13
115V, 5A AUTO TAP	50~ USAGE	10-11	
120V, 5A AUTO TAP	60~ USAGE	11-13	
WHEN USING 50 CYCLE PRIMARY, USE 50 CYCLE SECONDARY			

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
T1	XFMR. ACME #T-65238	1605802
R1 THRU R5	RES. 25 25W 1% WW	1300190
D2	DIO. PACK DM-15	1105799
D1 D3	DIO. PACK DM-1	1102933
C1 THRU C5	CAP. 160,000 MFD 20V	1004874
	PARTS LIST	A-PL-705-0-0

PARTS LIST

Figure 2-36 · 705B Power Supply, Circuit Schematic

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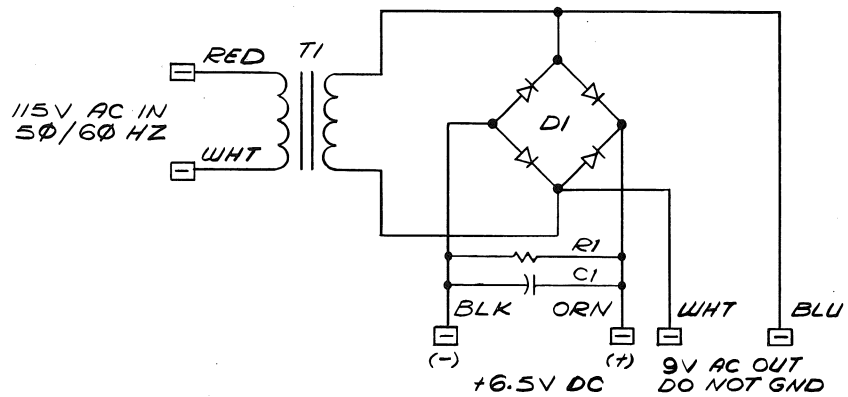


C1	CAP 18,000 MFD 10V DC	1009437
R1	RES 5 Ω 25W, W.L.	1300165
	PARTS LIST	D-UA-716-B-0
T1	XMFR#F69-U TRIAD	1609588
D1	DIODE PACK DM-2	1105392
REF DESIGNATION	DESCRIPTION	PART NO

PARTS LIST

FIRST USED ON OPTION/MODEL
716-B

REVISIONS: REV. | CHG NO. | CHK

DRN. Robichaud	DATE 10-9-69	
CHK'D. B. Healy	DATE 10-28-69	
ENG. J. Zeh	DATE 1-5-70	
PROD. G. Bundy	DATE 1-6-70	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE CIRCUIT SCHEMATIC 716B

SIZE	CODE	NUMBER	REV.
B	CS	716-B-1	

PRINTED CIRCUIT REV.

Figure 2-37 716 Indicator Supply, Circuit Schematic

2.20 855 POWER CONTROL

The 855 Power Control accepts a 30A power cord at either 115 or 230 Vac, filters the voltage, and delivers the voltage to either a switched or an unswitched output. A circuit breaker at the input controls all power. The switched output can be controlled locally or remotely by setting the LOCAL, REMOTE, OFF switch. Both sides of the ac line are switched. Figure 2-38 shows the unit, and Figure 2-39 shows its circuit schematic.

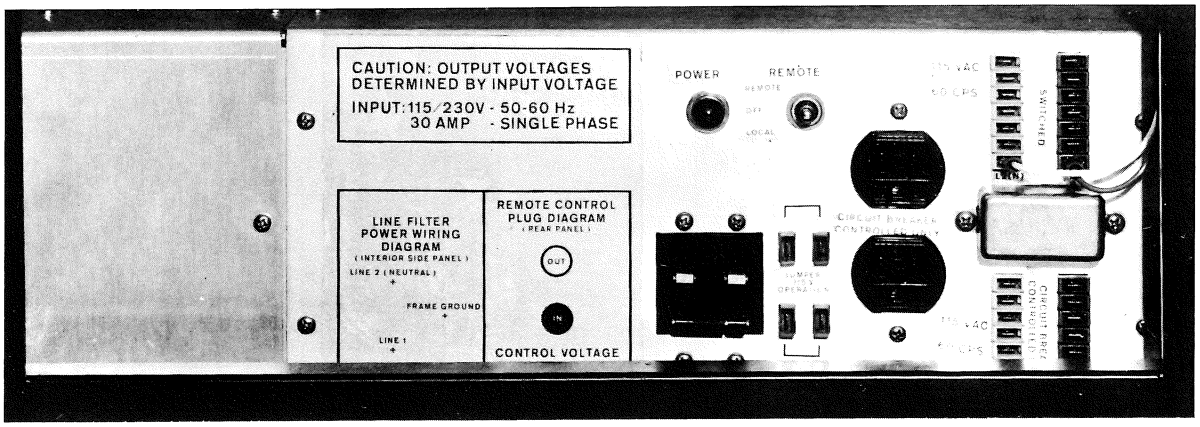


Figure 2-38 855 Power Control

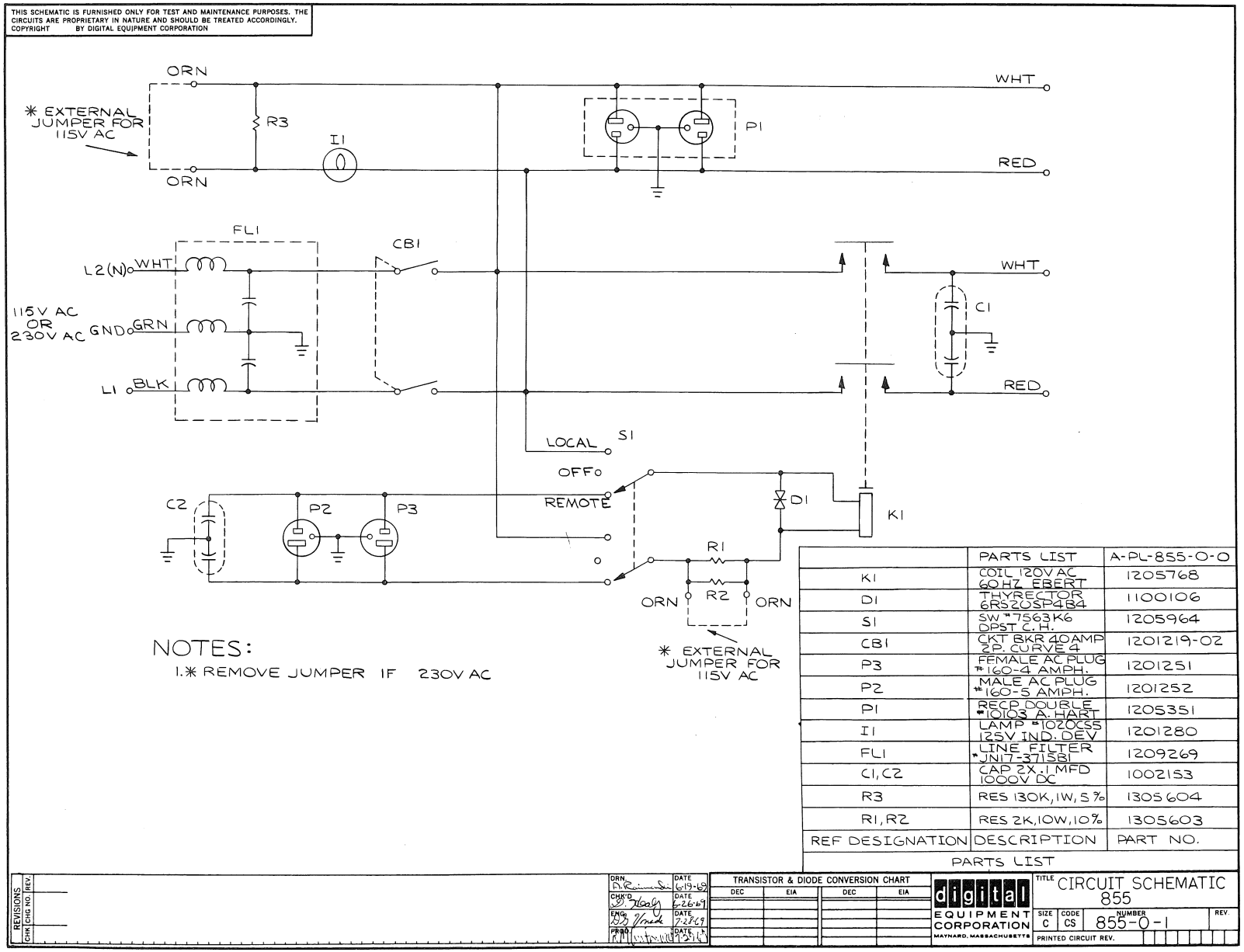


Figure 2-39 855 Power Control, Circuit Schematic

Chapter 3
RS09 Disk Drive

The RS09 disk drive (see Figures 3-1 and 3-2) consists of two assemblies; the RS08-M disk assembly, and the RS09-P disk electronics. The two units are functionally integrated and shall be referred to in Chapter 3 as a single unit, the RS09.

3.1 READ/WRITE HEADS

There are three basic considerations involved in designing and constructing a magnetic recording for reproduction. These are:

1. A device that can translate an electrical signal into a magnetic field.
2. A magnetizable medium that conforms to and retains the field.
3. A device that can detect the magnetic field and convert it to a signal that can be identified with the original.

These three elements take the physical form of the record head, the disk surface, and the reproduce head. With electronic amplification and a disk drive added to these elements, a basic magnetic disk is formed. In some applications the record head and reproduce head are combined into one head, the read/write head.

The read/write head can be compared to a transformer with a single winding. When current flows in the winding, the current produces a magnetic flux similar to that in the core of a transformer. The core is made of a closed ring with a nonmagnetic gap. The gap is bridged by the magnetic surface of the disk, and the flux detours around the gap into the disk surface to complete its path. When the disk is moved across the gap, the magnetic material is subjected to a flux (polarity) that is proportional to the signal current on the head winding. As the material leaves the head gap, each particle retains the state of the magnetization that was last imposed on it by the protruding flux. Thus, the actual recording takes place at the trailing edge of the gap. Figure 3-3 illustrates this process.

To reproduce this signal, the magnetic pattern on the disk surface is moved across the head; and the magnetic gap detours the magnetic flux through the core itself. The flux lines are proportional to the magnetic gradient of the magnetized surface, and the induced voltage of the head winding follows the law of electromagnetic induction: $e = \frac{N d\Phi}{dt}$. Thus, the output is the differential of the input. The waveforms recorded on the disk surface are determined by the method of recording used. There are two basic recording schemes used in digital systems, RZ and NRZ. In general, both methods operate by saturating the magnetic coding in one of two directions.

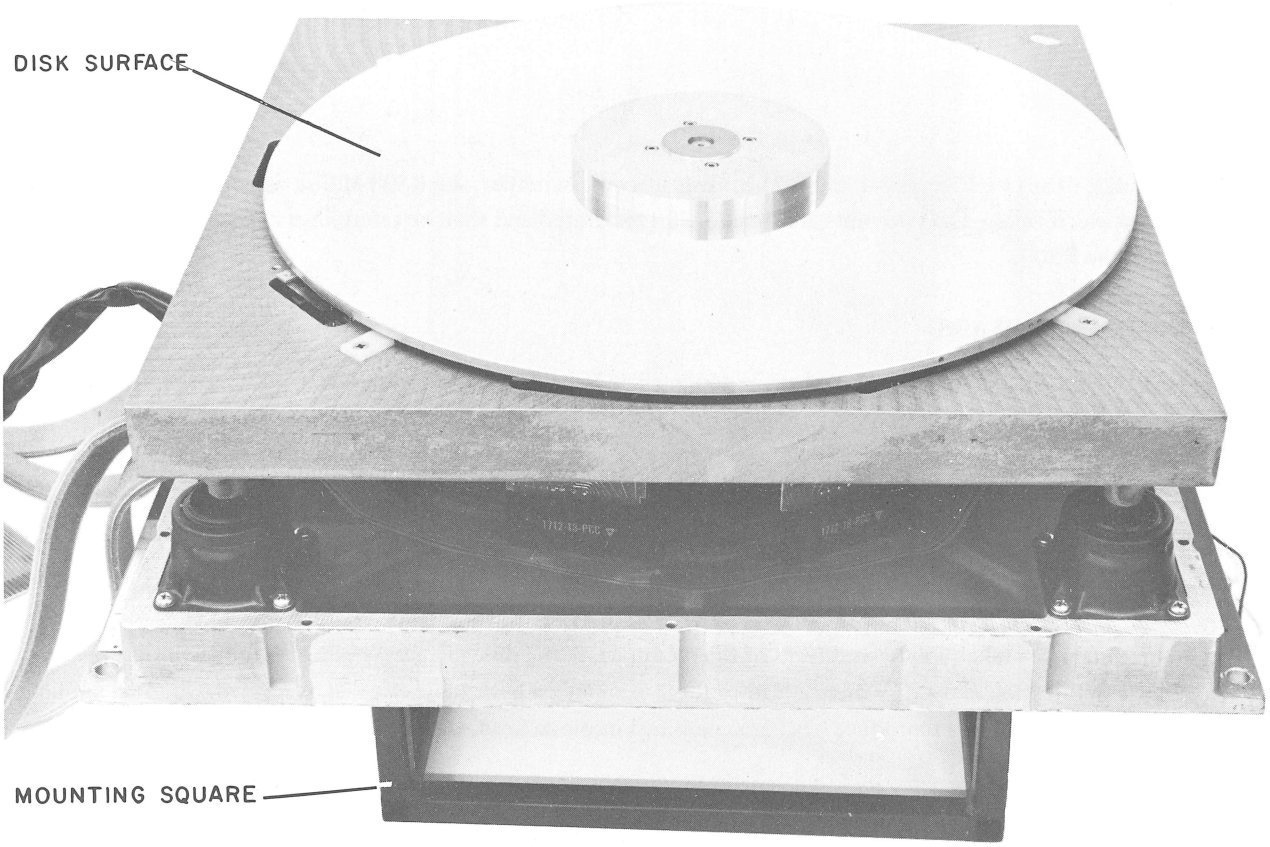


Figure 3-1 Disk Assembly With Cover Removed

Figure 3-2 Disk Assembly With Cover and Surface Removed

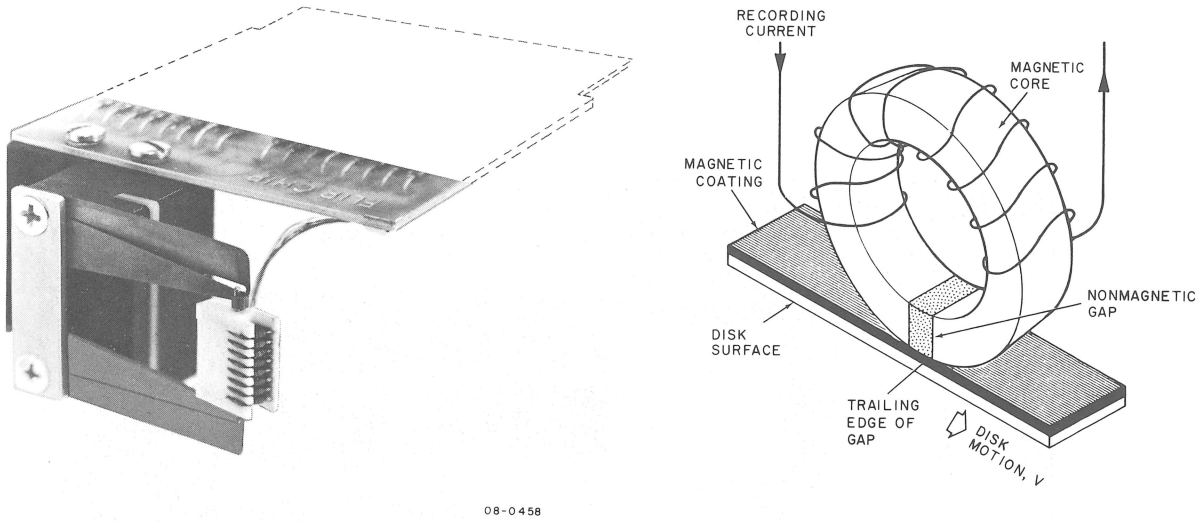


Figure 3-3 (a) DECdisk Head Assembly and (b) Simplified Diagram of the Magnetic Recording Process

3.2 DIGITAL RECORDING TECHNIQUES

There are two basic methods of recording digital data on a magnetic disk, **return to zero** (RZ) and **nonreturn to zero** (NRZ). The names refer to the nature of the head current, which in the first case stabilizes at zero when a bit is not being written, and in the second case stabilizes at either a positive or a negative head current between bits. There are several different ways of recording binary digits with these two methods. One technique in RZ recording recognizes one state of saturation as a binary one, and the other state as a zero; the zero state represents nothing. DECdisk, which uses NRZ, has no fixed state of magnetization assigned to either digit; rather, the state of magnetization is reversed every time a binary one is to be recorded, but left where it is if a binary zero is to be recorded. The NRZ method is more efficient than the RZ method in that more data is recorded with fewer flux reversals. However, the RZ technique provides for a self-clocking format. Figure 3-4 illustrates differences in the head current waveform of the two methods.

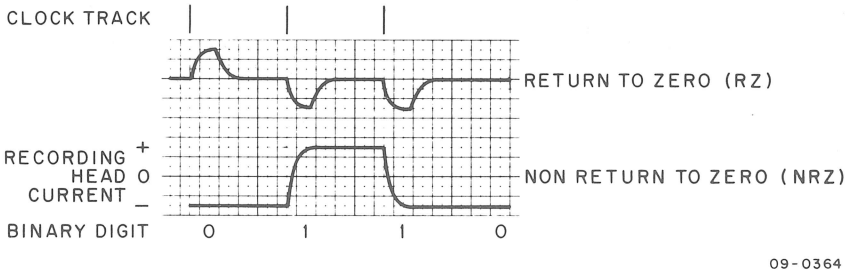


Figure 3-4 NRZ and RZ Recording Formats

The fact that the DECdisk NRZ does not present a self-clocking format (some form of reference clock must be present to determine where the zeroes fall) suggests that a clock must also be recorded along with the data. A clock track called the A track is recorded on one channel of the disk, and used as a timing reference to read and to write digits. Two more tracks called B and C are also recorded to identify individual data words on the disk so that they can be retrieved.

3.3 THE READ/WRITE HEAD ELECTRONICS

In the DECdisk system, data is stored serially on 128 tracks around the disk surface (refer to Chapter 1). Only one of these tracks is engaged in reading or writing at any one time, although 128 heads are continually riding over each track. At the same time, the A, B, and C tracks are continually being read and used to clock data onto or out of the data tracks. A particular track is selected by the controller through a matrix selection system. Once selected, a particular head reads or writes according to instructions from the controller. Since all of the heads in the matrix are identical, only one has been selected to illustrate the read/write operation. Refer to Figure 3-5. (The characteristics of the modules in this figure are given in Chapter 2.)

The data bit to be recorded is clocked by the A time clock into the G290 flip-flop, which drives the electronics of the head.

The coil L represents the head winding, which is the center leg of a simple bridge consisting of resistors R1 and R2; diodes D1 and D2; and the switching transistors T1 and T2. When the control reads or writes from this head, it does so by selecting the appropriate G286 Center Tap Selector and the corresponding G285 Series Switch. This combination applies +20V to node A, switches on transistors T1 and T2, and forward biases the diodes D1 and D2. Current (approximately 5 mA) flows into the G085 read amplifier to -15V. If the G290 writer has not been selected, this condition leaves the bridge balanced and no current flows through the coil. This is the case during a READ operation; the changing magnetic field from the disk surface induces a voltage into the coil that is seen across the input of the G085 reader, subsequently amplified, and sliced to appear at OUT. The polarity of the voltage across the coil, which is a function of the direction of flux change induced into the head, determines the relative polarity of the + and - OUT signal.

During a WRITE operation, the same voltages are applied by the G285 and G286 modules, but the bridge is unbalanced by a -15V level applied to the emitter of either T1 or T2 by the G290. This forces approximately 45 mA through the head coil in one of two directions, depending on which transistor sees the -15V. The transistor selected is a function of the writer flip-flop in the G290.

When a one is to be written, the flip-flop is complemented by the clock; the -15V is switched from one transistor to the other; the current changes direction; and the resultant change in magnetic flux produces the field that is recorded on the disk surface. Note that current is always flowing in the coil; the current never returns to zero (NRZ). Because the three timing tracks are always selected, the G286 is replaced with the +20V center tap from the G085, and the diodes feed directly into the read amplifier's input.

Figure 3-6 shows some of the waveforms that occur in the read/write head circuitry. The read voltage, a bell shaped pulse, peaks approximately 400 ns after the CLOCK pulse. This voltage is amplified and sliced to appear either at +OUT or -OUT, depending on the voltage polarity. Note that the NRZ format used by this system always produces alternate pulses at +OUT and -OUT. A positive pulse cannot be followed by another positive pulse, nor a negative pulse by another negative pulse. This characteristic is utilized to detect errors in the A, B, C, and data tracks.

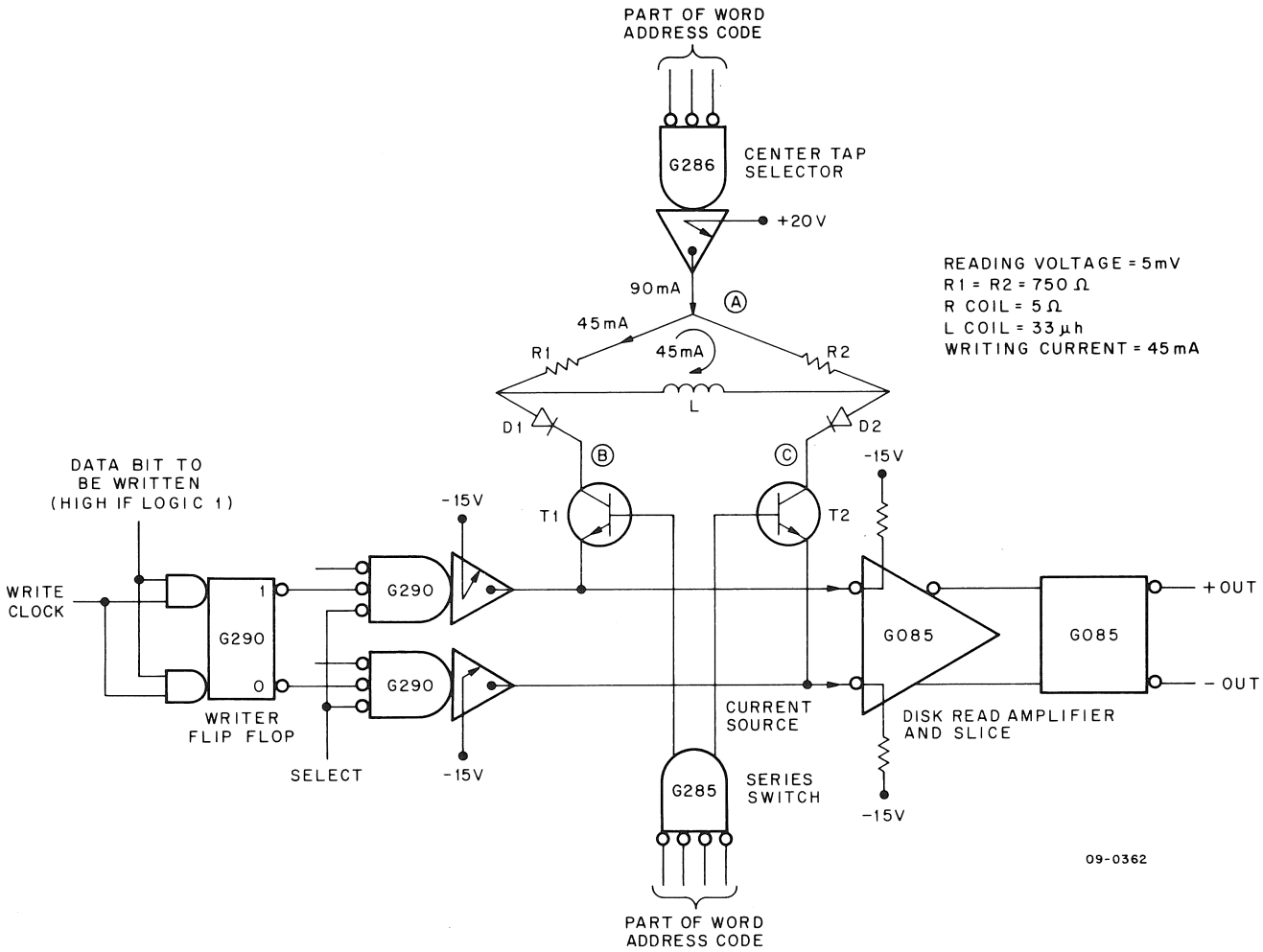


Figure 3-5 DECdisk READ/WRITE Electronics

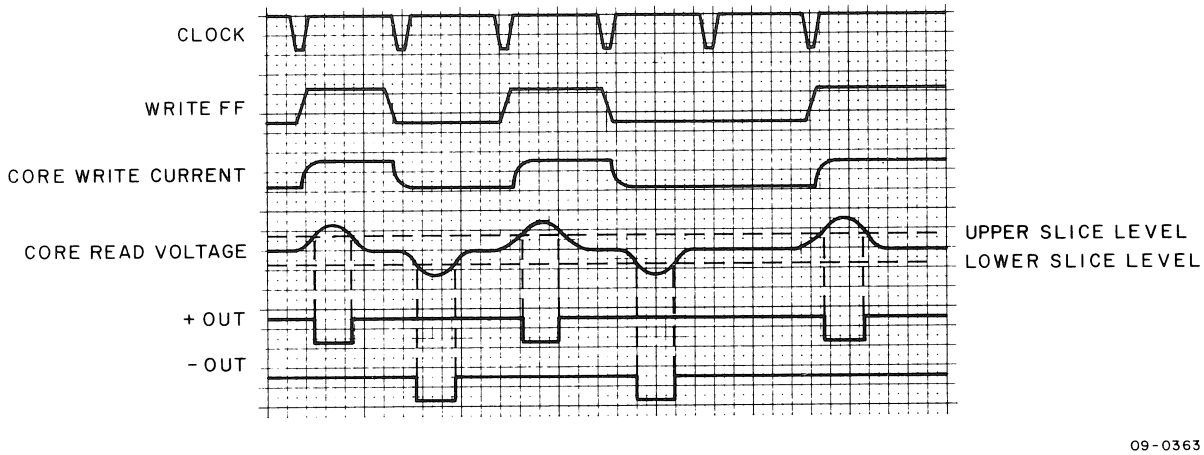


Figure 3-6 READ/WRITE Electronics Waveforms

3.4 THE DECDISK SIGNAL FORMAT

The selection of specific areas on the disk to write into or read out of is accomplished on DECdisk by dividing the circumference of the disk into 2048 segments (3777_8) in such a way that each segment of any track records a complete word. One track (the B track) is then assigned to record the address of each segment, and this track is made available to the controller, which assembles and identifies these segments. Another track (the C track) is needed to delineate the segment, since the length of the address is less than that of the words. Each of the three prerecorded tracks (the A, B, and C tracks) are duplicated on three more tracks, to be used if the first set is destroyed in the field. If this occurs, the Field Engineer reverses the position of one end of the timing track head cable to activate the spare tracks.

Thus, the disk surface is actually divided into 134 tracks by 134 read/write heads, each riding slightly above the disk and covering a narrow circular ribbon of the disk surface. The heads are mounted in groups of 8 on a unit called a shoe. The data shoes are set on cards, which are then inserted into slots under the disk surface. The slots are spread around the circumference of the disk as shown in Figure 3-2.

The shoe that contains the six prerecorded tracks is mounted alone on a card (shown in Figure 3-2).

The relative positions of all the timing and data tracks are shown in Figure 3-7. The signal counter is a reference, not a track itself. The gap area shown is a breather space for the DECdisk system at the point where it switches its head from track to track. The timing pulses stop during this period. There is also a buffer zone on either side of the gap where no data or addresses are recorded.

It is important to note that:

1. The address refers not to the segment in which it is but to the following segment. This allows the controller time to assemble the address and identify the address before the actual data area appears under the data heads.
2. The first bit of each address, the control bit, is always a binary one. The first bit of each data word, a guard bit, is always a binary zero.
3. Each address and data bit calculate a parity bit, which they deposit at the end of the word. Parity ensures that an even number of ones is in each word.

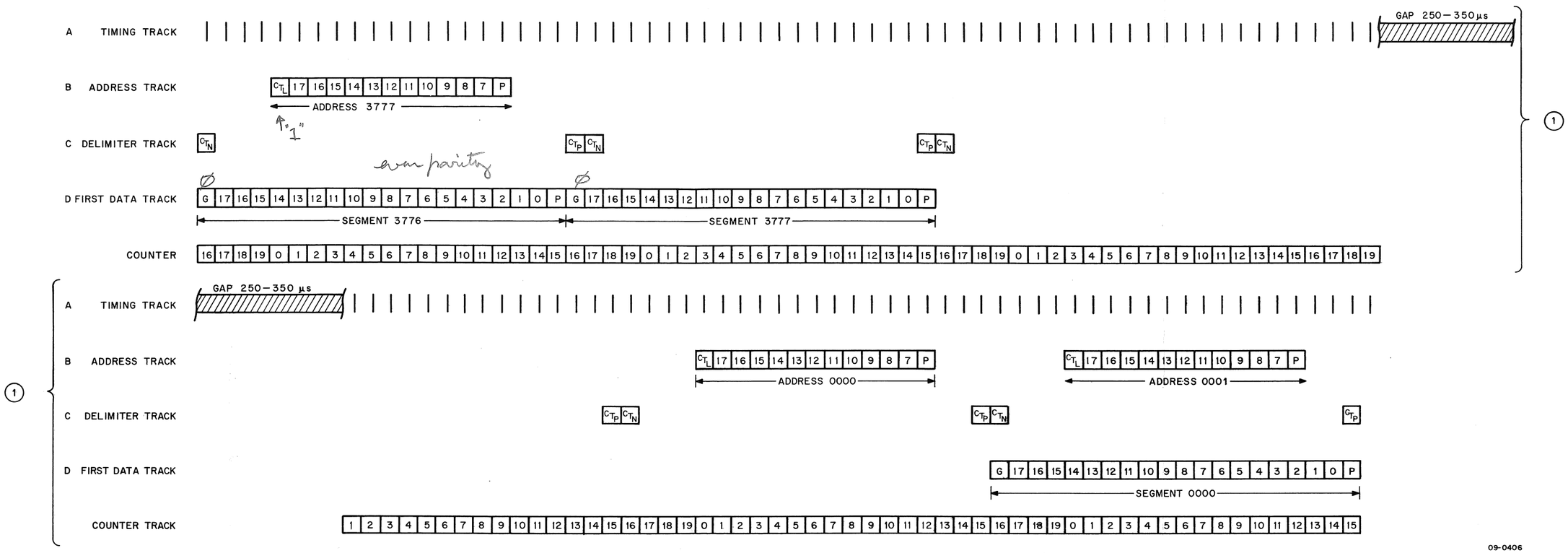


Figure 3-7 DECdisk Format

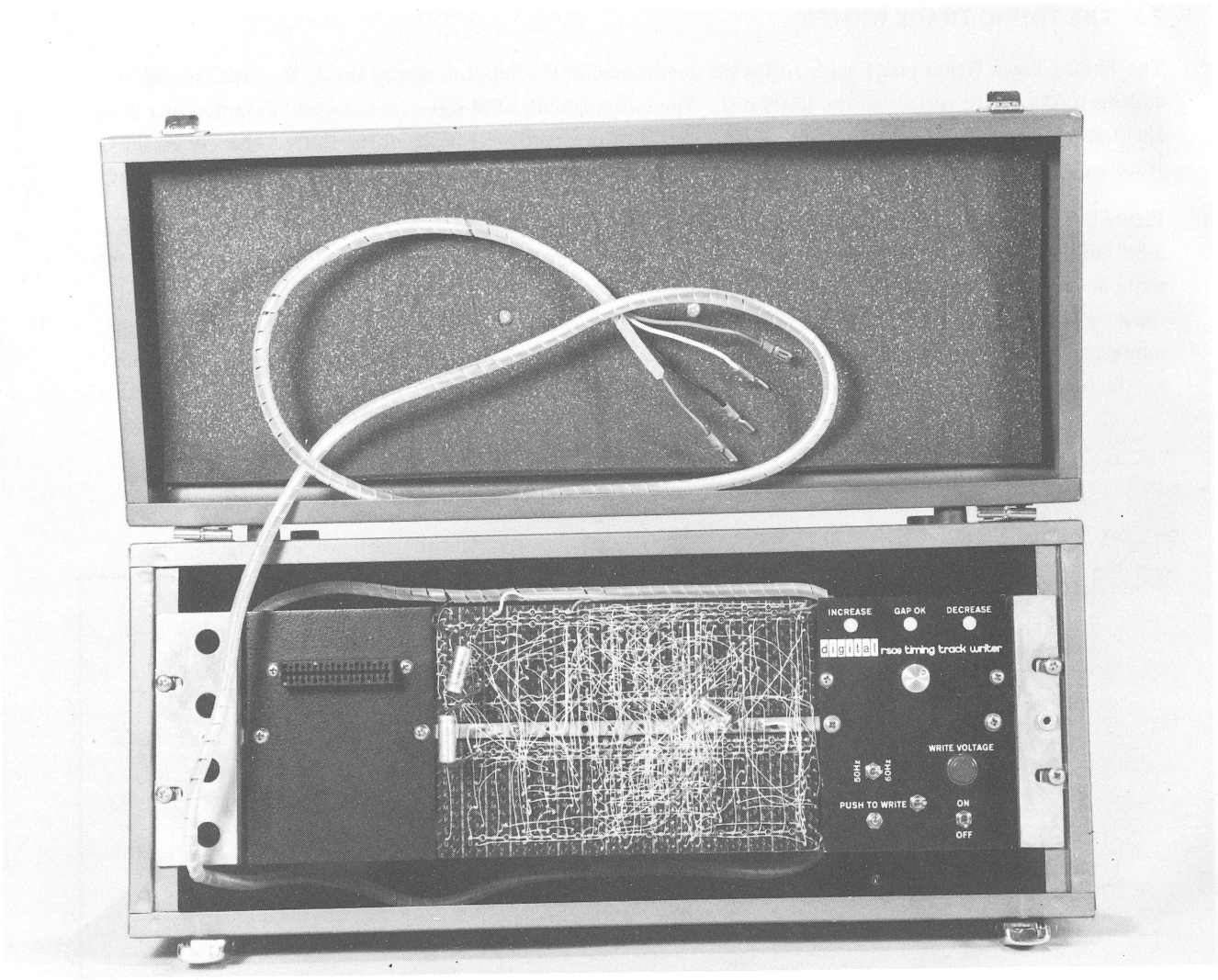


Figure 3-8 Timing Track Writer

4. The address always starts at bit 0 of the counter or bit 14 of the data word in its segment. The C track pulses are recorded at bits 15 and 16 of the reference counter.

The preceding observations are particularly important when the disk is to be preformatted; that is, when the A, B, and C tracks are to be prerecorded at the factory onto the disk surface (this function is performed by the Timing Track Writer, which is explained in the Paragraph 3.5).

3.5 THE TIMING TRACK WRITER

The Timing Track Writer (see Figure 3-8) is the device used in the depot to record the A, B, and C timing and address tracks on the surface of the RS09 disk. The writer is built of M-series modules and mounted in a single H911 panel. It needs no computer and cables directly to the read/write heads of the RS09. This allows the RS09 units to be preformatted before they are checked out (if the heads, disk, and disk drive are functional).

Figure 3-9 is the block diagram of the Timing Track Writer. It consists of a clock, an 11-bit serial counter, a 5-bit modulo 20 counter, the logic to measure the length of the gap, and the drivers and receiver for the read/write heads. When the clock is enabled by a manual switch, and the WRITE OFF switch is turned on, equipment operation begins. The disk must be rotating and the writer cabled to it. The counter keeps track of the number of bit cells, the decoding of the correct time when the C track pulses should be written, and the times at which the shift counter should start and stop its shifting.

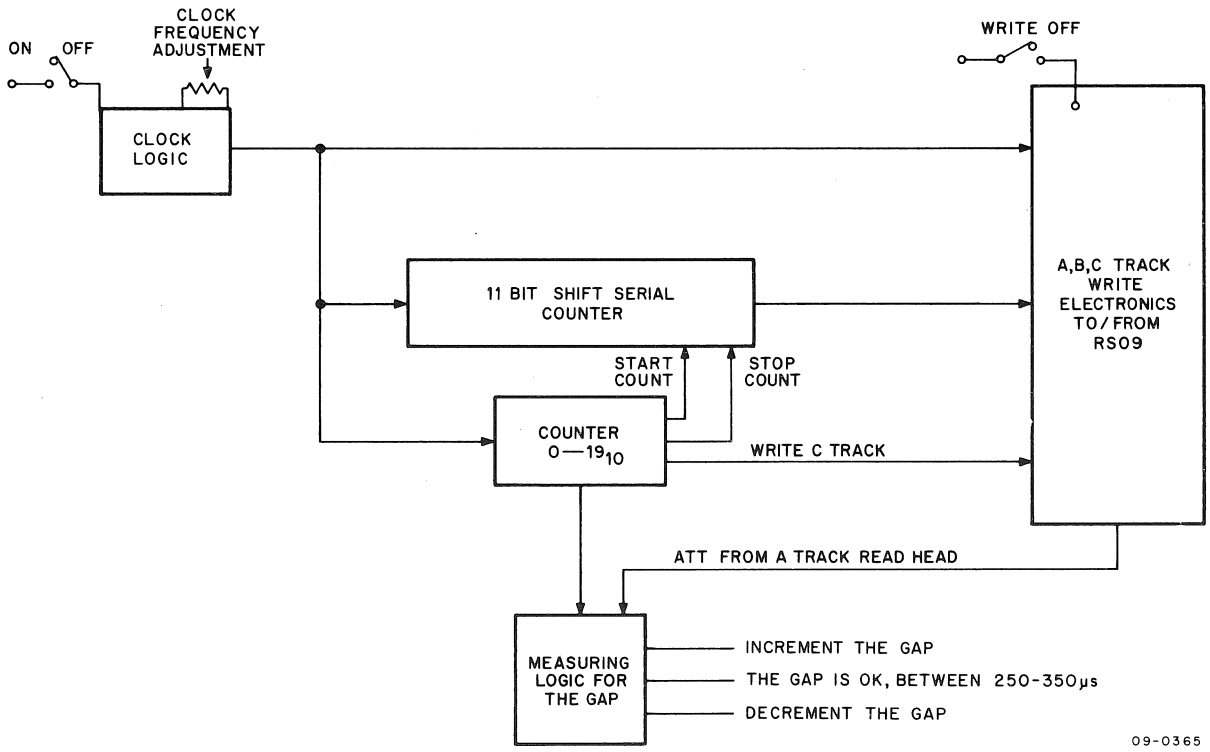


Figure 3-9 Timing Track Writer, Block Diagram

The 11-bit serial counter starts at all zeroes and then shifts its contents from the least significant bit onto the B or address track and, at the same time, back into its most significant bit. The counter then automatically increments itself by one for the next address.

Meanwhile, the clock is recording the A or timing track. When the gap comes up at the end of the revolution, the gap-measuring logic examines the time between the last clock bit and the first appearance of an A timing track pulse. If the time is less than 250 μs, a light (INC) flashes on to inform the operator to increase the clock frequency. If the time is greater than 350 μs, light DEC flashes on; and the operator should decrease the clock frequency. When the clock frequency is set so that the gap lies between 250 and 350 μs, the OK light flashes on, and the operator knows that the disk has been preformatted properly. Both sets of timing are recorded at the same time.

NOTE

The Engineering Drawings of the DECdisk system are identified by a code; i.e., Drawing D-BS-RS09-TA-3. Consult Volume 2 of this manual for the drawings referred to in the following description.

Assume that the WRITE OFF switch is enabled. The switch shown in Drawing D-BS-RS09-TA-3 is set, and it triggers a 100 ms delay that times out and issues a CLR (H) to initiate the system. During this delay, the disk is cleared of any signals. The CLR H signal clears the WA serial counter and the BC counter shown in Drawing D-BS-RS09-TA-4. It also sets the Write Enable flag (WR EN), which in turn enables the M401 clock. The clock drives a 2-bit ring counter made up of flip-flops CLK and A CLK. These flip-flops provide the main timing pulses for the counters and timing tracks. The two flip-flops are 90° out of phase.

The BC counter begins to count; the level C00 EN is asserted on a count of 19, and the next pulse sets C00. At the same time, the guard bit is written. C00 also enables the Word Address Register to start writing into the B track by setting WR ADR and gating WA 00 to the input of the G290. Meanwhile, the A CLK has been writing timing pulses 800 ns apart onto the A track. The WA serial counter shifts its address, and at the same time serially increments itself by shifting its least significant bit into the flag CRY, detecting the first 0 to appear, and forcing a 1 into the most significant bit at that point. All 1s before this 0 are shifted back as 0s, and all bits after this point are shifted back the way they emerge. The feedback function is the exclusive OR of CRY and WA00. CRY is initialized to a 1, and reset on the first 0 it sees from the WA Register.

When the counter reaches 11, the C11 flag (Drawing D-BS-RS09-TA-2) is set and the address writing stops. The flag WR ADR is reset, as is the G290 if an odd parity existed in the address. (This parity is written.)

When the counter reaches 15, the C track writing is enabled and the CTP and CTN pulses are recorded. The flag LADR (Last Address) is set when C11 is cleared while CRY is still on a 1. This signifies that the last segment is approaching, i.e., that CRY stayed on through a complete string of 1s for address 3777. When WA01 comes up, at the count of 2 after overflow the WR CLR flag shown on Drawing D-BS-RS09-TA-3 is set by C11 to prepare the logic for the approaching gap. The WR EN flag is cleared on C00, and all writing stops. The R303 delay of print disables the output of the read amplifier until it recovers after writing; when the read amplifier sets, it passes the A track through its reader. At the same time two M302 delays are also set, and they time out to 250 μs and 350 μs. If the A track passes any timing track pulse before 250 μs are up, the flag INC is set to tell the operator to increase the clock frequency (increase the gap time). If the next A track timing pulse comes between 250 μs and 350 μs, the OK flag is set. The DEC flag sets if the A pulse arrives after 350 μs, and the operator should decrease the clock frequency (decrease the gap time). If either INC or DEC occur, the system is cleared out and starts again. Otherwise, the system stops formatting, having completed its job.

Drawing D-BS-RS09-TA-3 shows a SYNC flag that sets as soon as the clock begins to issue pulses. This flag is useful as a sync point because it switches precisely at the start of the format.

Drawings D-FD-RS09-TA-5 and D-TD-RS09-TA-6 show the flow diagram and timing, respectively, for the writer. Note that the preceding explanation applies when the PDP-9/PDP-15 switch is turned to PDP-9.

Chapter 4
DECdisk Logic

The logic of the DECdisk system is explained in this chapter by presenting the logic of the DECdisk subsections. (L on logic diagrams used in this chapter indicates LOW when true.) Simplified logic diagrams are presented in this chapter. For a more detailed description, consult the appropriate Engineering Drawings in Volume 2 of this manual.

4.1 SIGNAL ERROR DETECTING CIRCUITS

There are four circuits in the controller that detect errors in the signals from the disk drive on the A, B, C, and data tracks. These error detecting circuits are explained below.

4.1.1 Error Detection Logic for the A Timing Track

The A track records the main clock pulse for each disk of the DECdisk system. A pulse train with a period of 1.6 μs is recorded. On playback, both negative and positive transitions are detected by the read electronics. The receiver slices each transition at a predetermined level, and the two pulses are combined to form a pulse train with a period of 800 ns.

Figure 4-1 shows the logic which is used by the controller to detect either a dropout or an extraneous pulse on the A timing track. The logic flows from left to right.

The positive and negative sliced outputs from the A timing track head appear as ATTP H 31 and ATTN H 31, respectively. These outputs drive M602 pulse amplifiers, which in turn trigger M302 delays set for 1.2 μs. These delays feed back to the input gate that enabled them, and for the period that they are set, they inhibit any other pulses from passing into the system. During this time, there should be no other pulses except noise spikes. The two delays are then logically OR'd together to produce the signal ATOK (A Timing Track OK). ATOK releases registers in the controller, and a start up sequence begins. Whenever the gap is reached, or an A track pulse is dropped; ATOK is removed and the controller is essentially turned off. When ATOK returns, the controller starts up up again. Figure 4-2 is the A Track Error Detection Timing Diagram.

The outputs of the two amplifiers are also logically OR'd, and the resultant pulse train is called ATPN H 1. These pulses, together with the original pulse amplifier outputs, are fed into four flip-flops. If the circuit sees a negative pulse, immediately after a negative pulse, this logic sets the MPEN flip-flop. The error could have been caused by a dropped positive pulse or an extraneous H added negative pulse. If the circuit sees a positive pulse immediately following a positive pulse, the flip-flop MNEP is set. Note that as soon as either error flip-flop is set, it inhibits any additional sliced inputs from entering the controller.

The signals APE (1) L, ATPN L 9, ATNM L 9, and A TEST L are related to other parts of the controller and are covered in later portions of this text. BTER and CTER are flags posted when similar errors occur on the B or C track respectively.

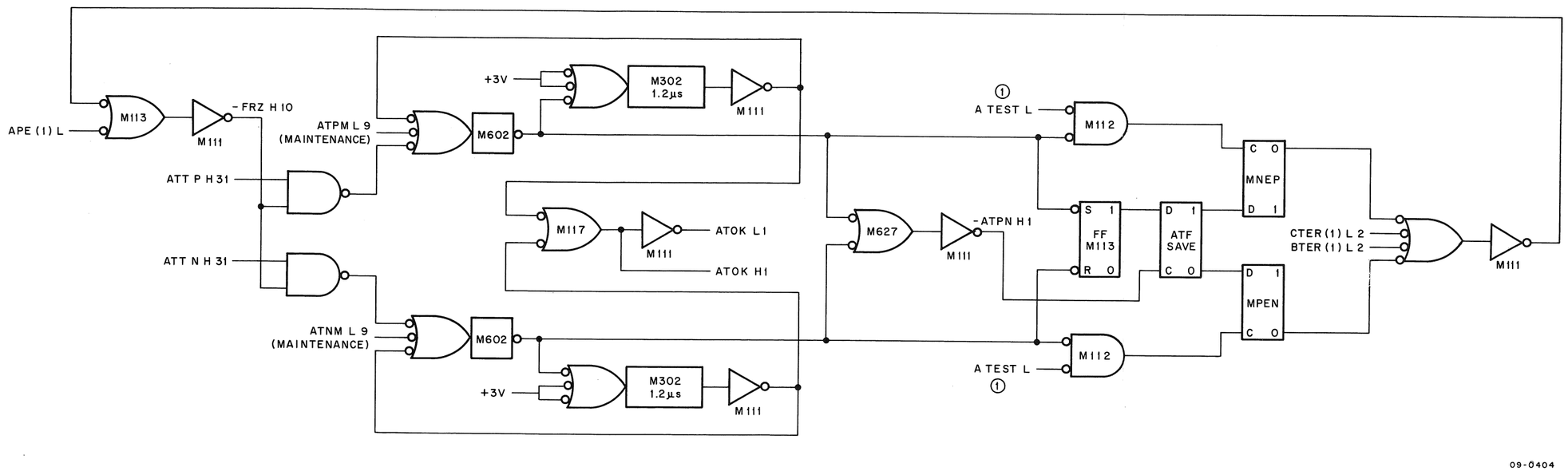


Figure 4-1 A Track Error Detection

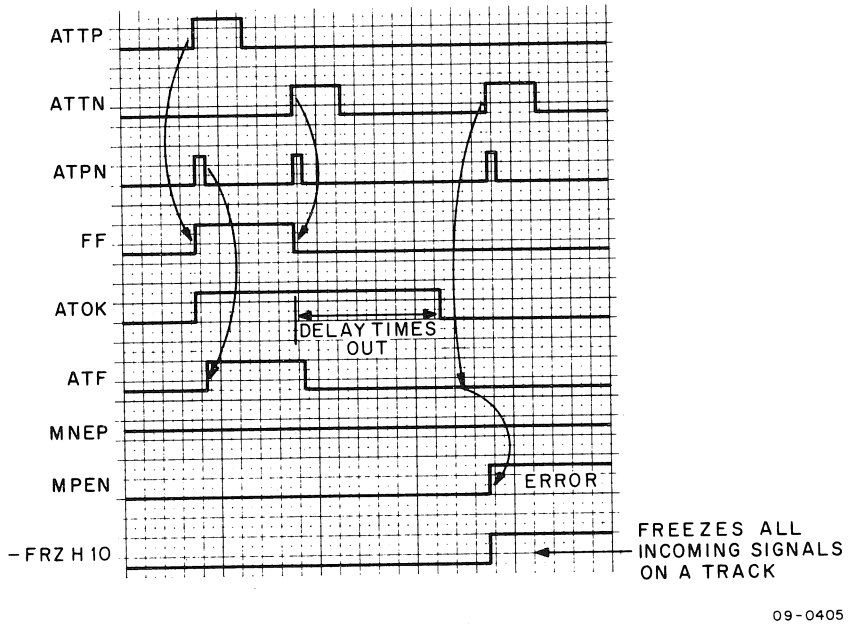


Figure 4-2 A Track Error Detection, Timing Diagram

4.1.2 Error Detection Logic for the B and C Tracks

On the B track, the disk has stored the address of each segment. Since this is not a predictable clock-pulse, it is not possible to inhibit the time between signals. However, the preceding explanation of the A track applies with respect to positive and negative outputs; that is, a positive pulse cannot be followed immediately by another positive pulse, and a negative pulse cannot be followed by another negative pulse. Furthermore, the B track is strobed into its register by a narrow A track pulse at the optimum time, and is, therefore, extremely reliable. The logic of Figure 4-3 shows the error detection technique designed for the B track. (The C track logic is identical.)

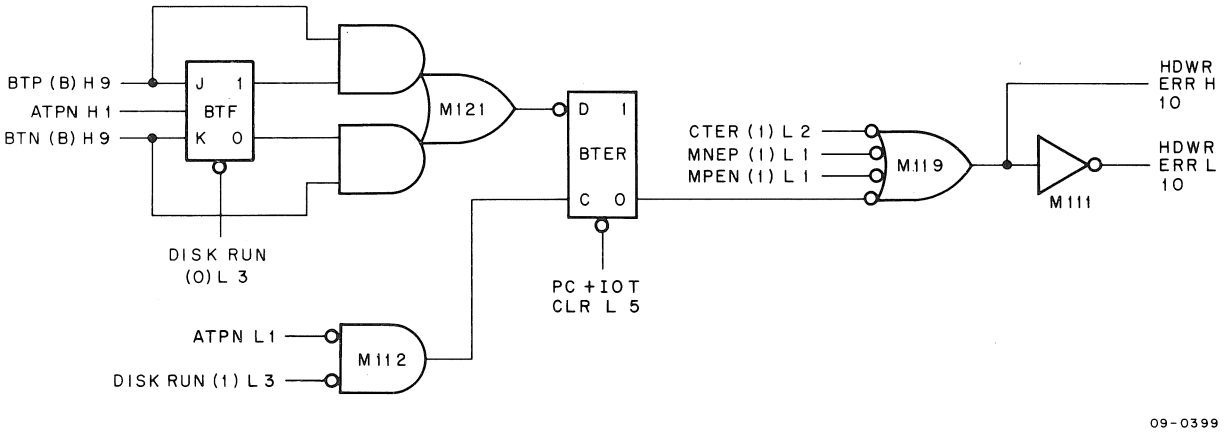


Figure 4-3 B Track Error Detection

The JK flip-flop BTF is enabled by BTP and BTN, and clocked by ATPN. If two positive or negative signals follow in sequence, the error flag BTER is set. The ATPN signal is inhibited (Figure 4-1), and all action stops. This testing occurs only when the disk is on RUN, or performing an operation. When it is rotating but not performing, no errors are detected. Figure 4-4 is the B track timing diagram.

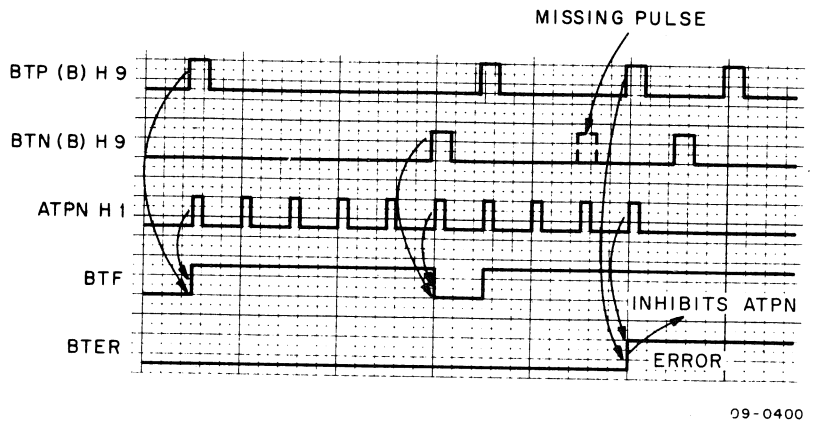


Figure 4-4 B Track Timing Diagram

4.1.3 Error Detection Logic for the Data Tracks

The delay inhibit circuits of the A track cannot be employed in the data track. (The data track logic is shown in Figure 4-5.) However, if two identical pulses are detected in tandem, the DTER flag is posted, followed by DTE. The two flip-flops PDT and NDT follow the input pulses and store them, a procedure that is necessary to compensate for skew between the data heads and the timing track heads. This skew does not occur among the A, B, and C tracks because the heads are all mounted on the same shoe; that is, they are mechanically interconnected.

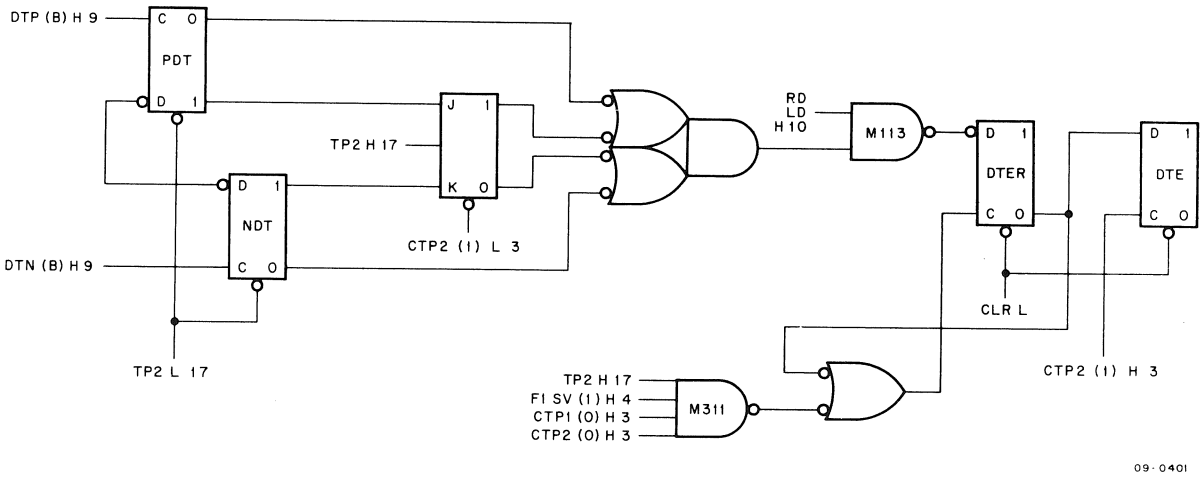


Figure 4-5 Data Track Error Detection Logic

TP2 L 17 is the ATPN pulse delayed, and CTP2 (1) L3 is a counter generated by the B track. Note that ATPN is not inhibited; DTER latches and stays on until it is cleared. DTE sets at the end of the word. Figure 4-6 is the timing diagram of the data track.

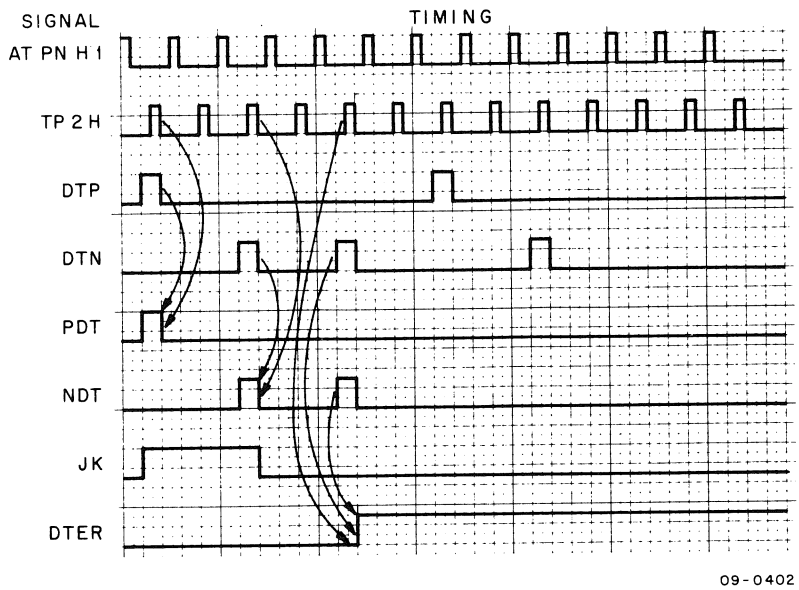


Figure 4-6 Data Track Timing Diagram

4.2 THE CONTROL SECTION LOGIC

There are 11 major subsections in the control section logic that interact to establish the primary functions performed by the system.

4.2.1 The IOT Decode and Trap Logic

The IOTs listed in Table 4-1 are decoded in the controller (Drawing D-BS-RF09-0-05). A related logic feature, the IOT Trap Logic, is shown in Figure 4-7.

If a program issues an IOT that conflicts with the then current DECdisk system operation, the erroneous IOT is trapped by the IOT trap logic; and an error flag is posted. The trap logic consists of a STOP flag, three pulse amplifiers, and three flip-flops. Critical IOTs set the STOP flag and inhibit the pulse amplifiers from setting the corresponding IOP flip-flop. These flip-flops are used in the control rather than the control pulses themselves for such IOTs. The pulse amplifiers give the STOP flag time to examine each IOT and, when necessary, inhibit the IOT from setting its flag. The IOP 4 pulse is double-buffered, which serves to provide a clear and load series for several registers. D IOP 4 is used to clear, and L IOP 4 sets the data into the applicable register. Some IOTs are allowed to function even though they occur during an operation because they do not affect the controller. These particular IOTs use the IOP pulses directly. Table 4-1 summarizes the effect that IOTs have on the trap logic. The mnemonic PE indicates that when a related IOT is issued during a valid disk operation, the Program Error flag is set. IN indicates that the IOT is stopped.

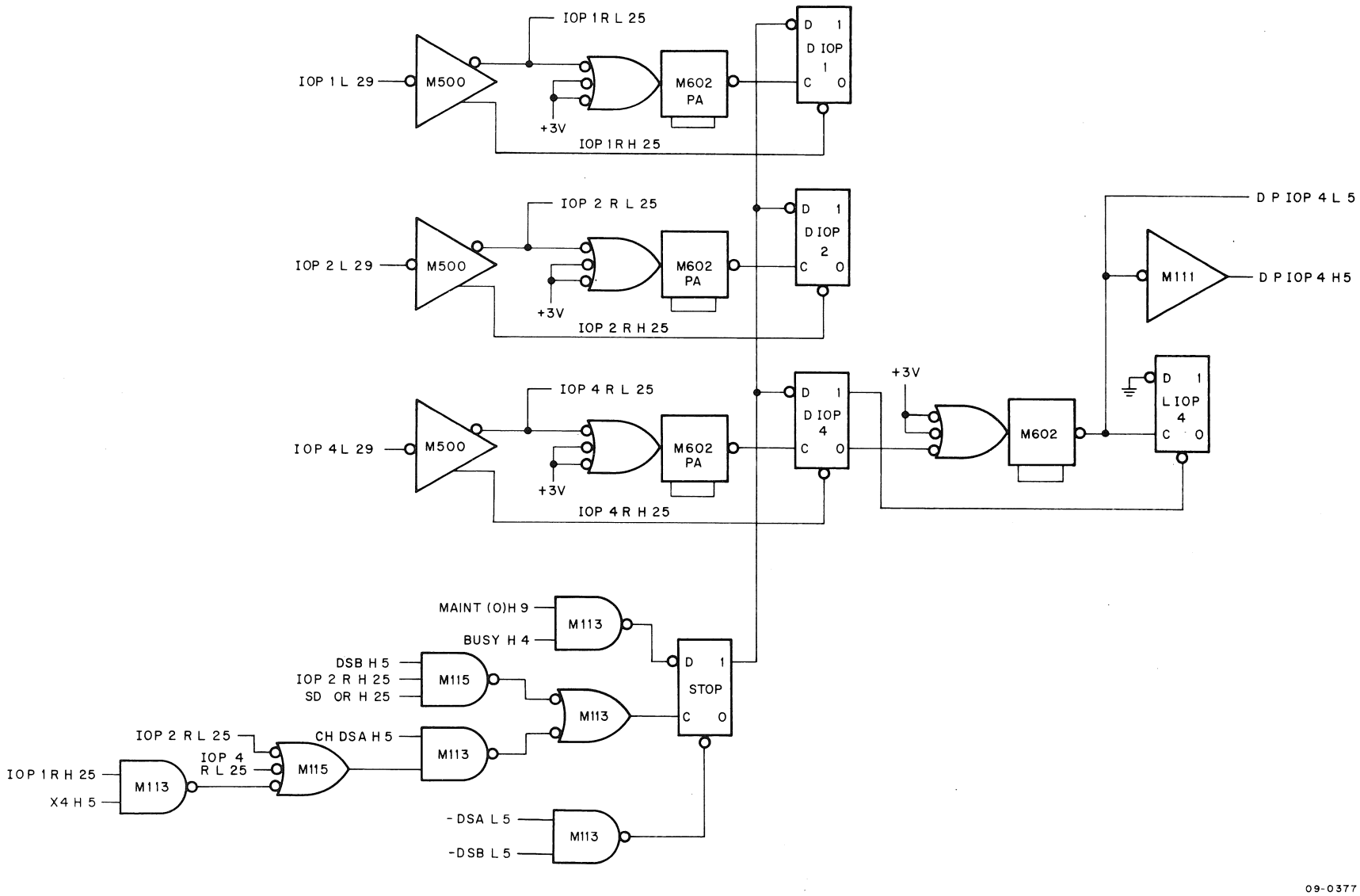


Figure 4-7 IOT TRAP Logic

Table 4-1

IOT Decode Effect on Trap Logic

Device Select Code A (DSA) = 70

	SD = 0_8		SD = 2_8		SD = 4_8		SD = 6_8	
IOP 1	DSSF (SKP)		DSCC (IOT CLR)		DLAL (CLR FNRG)	PE IN		
IOP 2	DRBR (BR→AC)	PE	DRAL (APO→AC)	PE	DSFX (AC∨FNRG)	PE IN	DRAH (AP1 →AC)	PE
IOP 4	DLBR (AC→BR)	PE IN	DLAL (AC→APO)	PE IN	DSCN (IOT CONT STATUS CLR)	PE IN	DLAH (AC→API)	PE IN

Device Select Code B (DSB) = 72

	SD = 0_8	SD = 2_8	SD = 4_8		SD = 6_8	
IOP 1						
IOP 2	DLOK (ADS→AC)		DSCD (STATUS CLR)	PE IN	DSRS (STATUS→AC)	PE
IOP 4	DGHS (DISK MAINT)	DGSS (CTL MAINT)	DISK MAINT (CLR MAINT MODE)		CTL MAINT CLR MAINT MODE	

FNRG = Function Register (FO, F1, INT)
PE = Program Error
IN = Inhibit IOT

4.2.2 The Function Register

There are three bits to the Function Register, each of which is double buffered. Figure 4-8 shows the logic and tabulates the purpose of each bit. The first three flip-flops – F0 SV, F1 SV, and INT SV – are loaded from the computer under IOT command. When the system is ready to execute the command, an IOT CONTINUE is given, which jams the instruction word into the next three flip-flops. The controller now acts on the order. If, during the operation, a major error occurs, bits F0 or F1 of the second Buffer Register are cleared and the operation stops until the error can be repaired. When the programmer wants to resume the operation, he should issue the continue command to continue the process.

F0 and F1 are cleared when the correct number of transfers are completed between the processor and control. F1 is cleared by the I/O OFLO pulse ANDed with EN B (DCH channel multiplexer). F0, however, is not cleared until SRI and the OFLO flag is set. This guarantees transfer of the last word from the processor buffer during WRITE and WRITE CHECK operations.

4.2.3 The Timing Generator

Figure 4-9 shows the timing generator logic, which begins in the RS09 disk drive and is cabled to the controller. Much of this logic has been covered in detail under the description of A track error detection (Paragraph 4.1.1). Note that ATOK L clears the CTP register. ATPN, the combined timing pulses, is fed through several delays to generate TP1 L 17 and TP2 L 17.

The first CTP of the C track initializes a 3-bit Shift Register (CTP1, CTP2 and CTP3), which is subsequently shifted by ATP. Pulses appear on the C track only at the end of each word cell. The three flip-flops are used to set up the data transfers to and from the Shift Register after the word is assembled. Figure 4-10 is a timing diagram for the timing generator. Familiarization with this circuit is important because the timing generator signals are used throughout the controller.

4.2.4 The Unlock Sequence Logic

Figure 4-11 illustrates the use of both ATOK and the C track. The first time CTP3 is set after ATOK is asserted and a valid operation is specified in the Function Register, the DISK RUN flag is posted. DISK RUN resets when ATOK falls out; this occurs during the gap or when an A track pulse is lost, or when the Function Register is cleared and CTP3 occurs. When DISK RUN is set, the controller is assured that a valid C track signal has been detected with at least three valid ATPN pulses, and meaningful address decoding can begin.

The following sequence must be completed:*

1. ATOK
2. ATP and CTP
3. 3 good ATP's (no ATOK) sets CTP3 and enables DISK RUN.
4. ATP CTP3 set DISK RUN
5. Continued good ATP's and CTL shifted through 12 positions into CTL FF

4.2.5 The Track and Disk Address Register

The Track and Disk Address Registers are initiated by the computer with an IOT instruction. When the disk is on RUN (that is, when the disk is performing an operation in the data area of the disk), these registers

*ATOK must be present always.

BIT 15	BIT 16	BIT 17	FUNCTION
F0	F1	INT	
0	0	X	NOTHING
0	1	X	READ
1	0	X	WRITE
1	1	X	WRITE CHECK

NOTE:
INT enables the PI or API logic in the controllers.

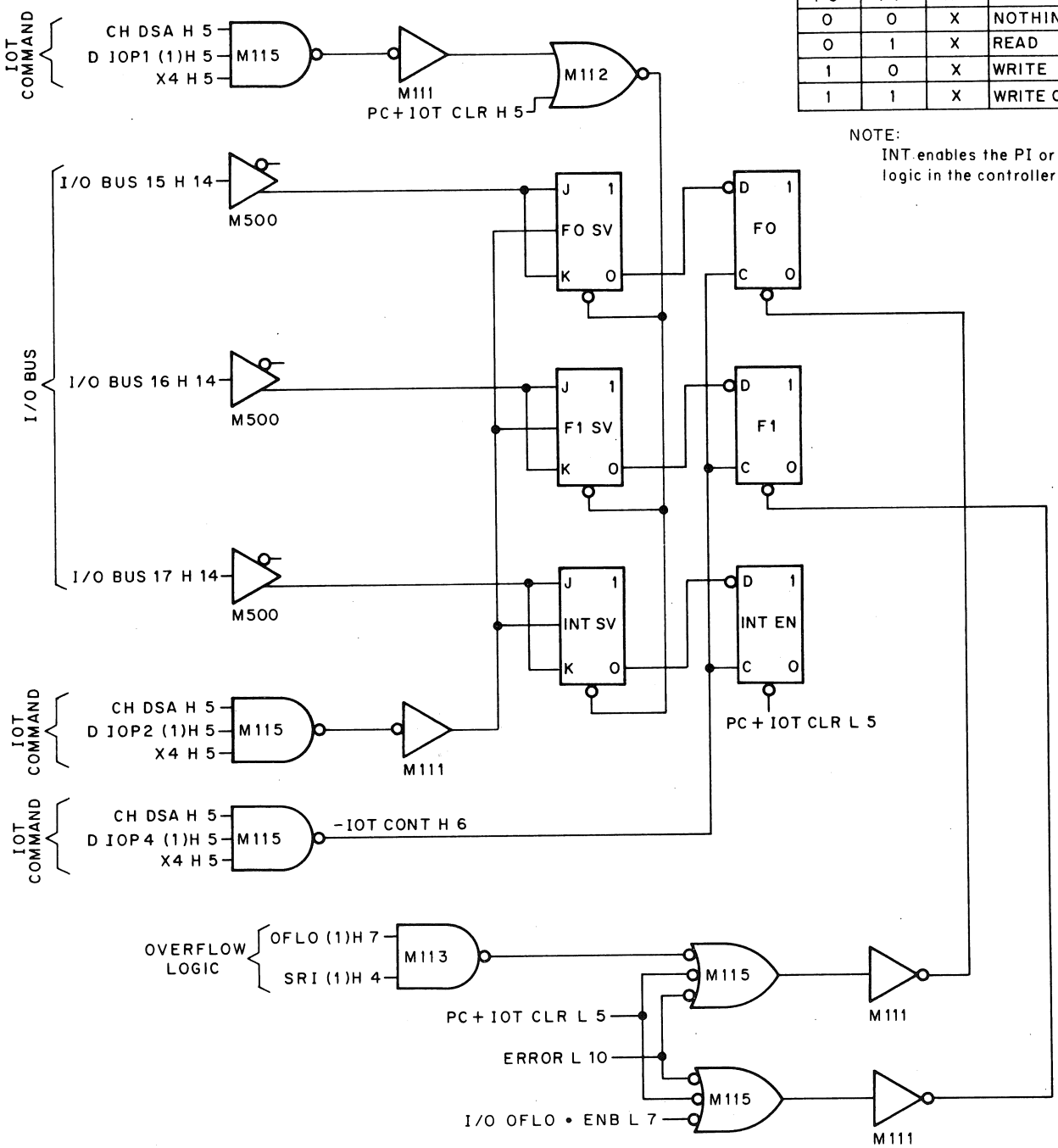
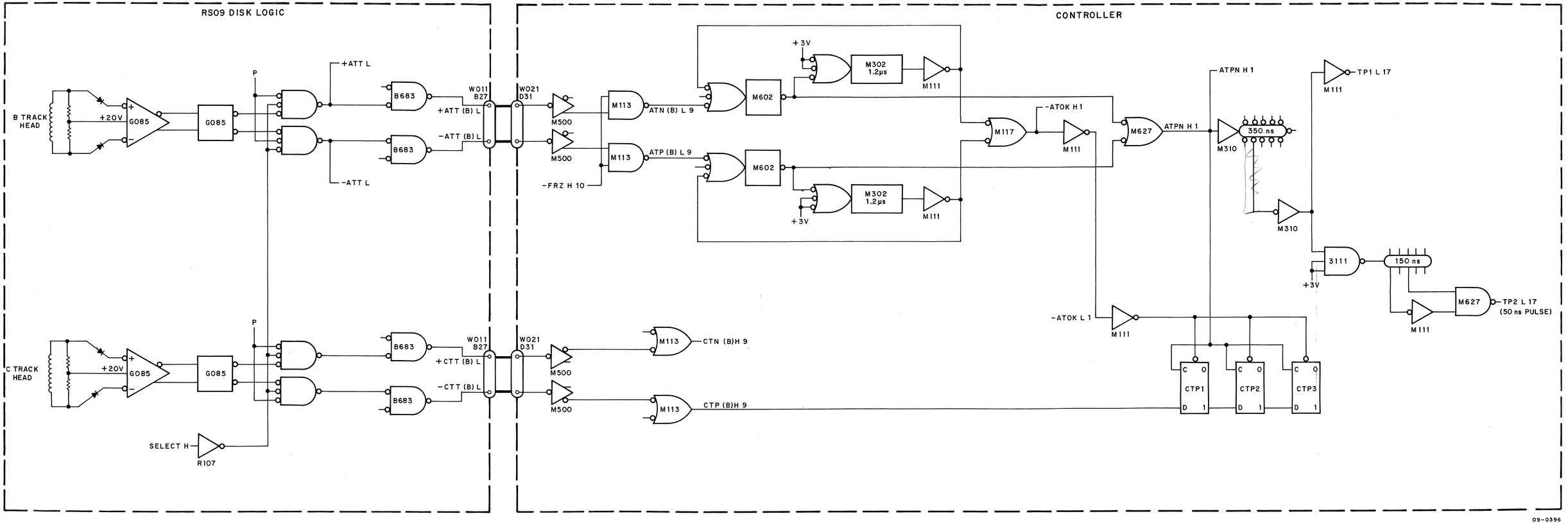


Figure 4-8 Function Register

09-0378



09-0396

Figure 4-9 Timing Generator

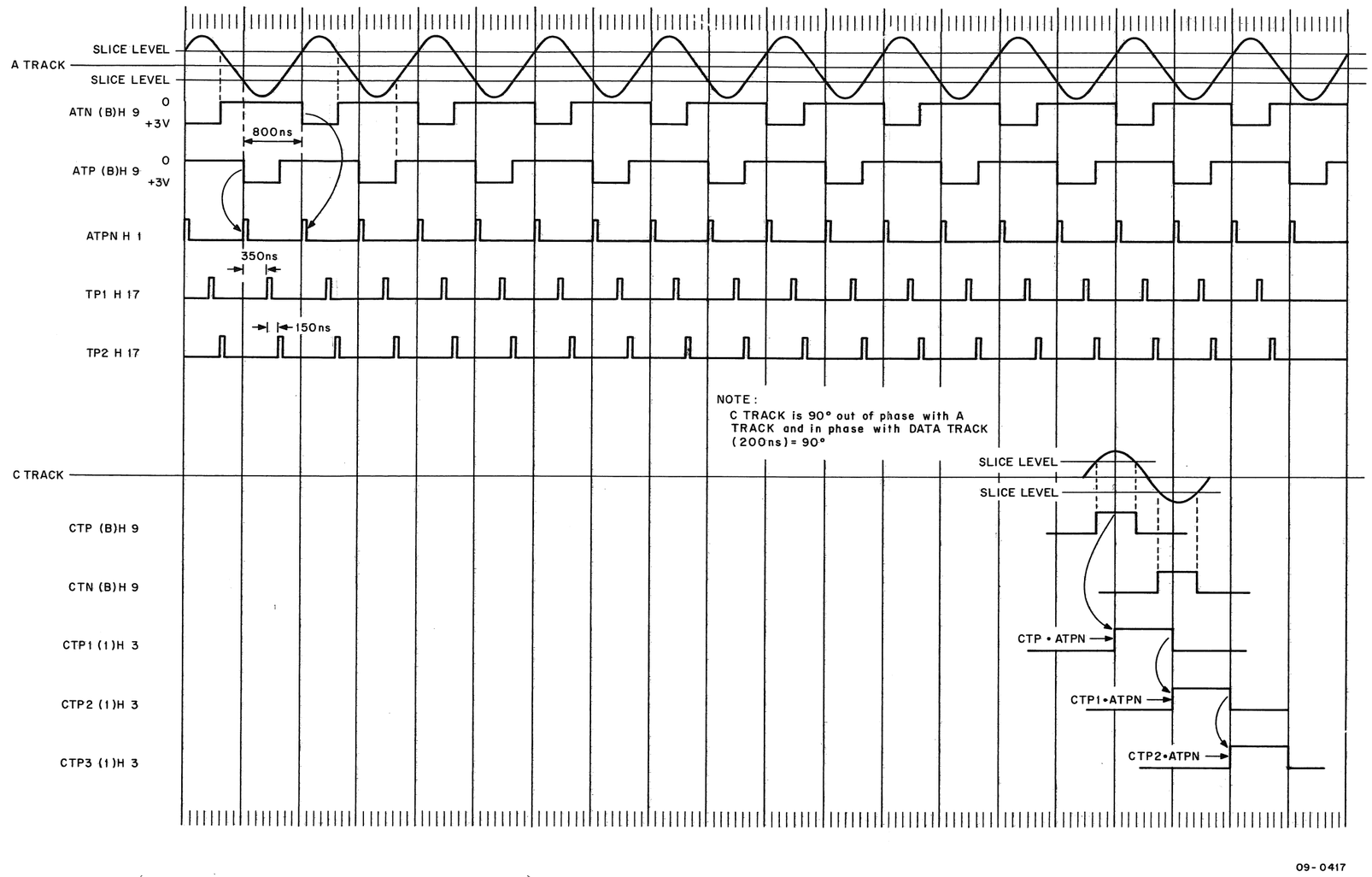


Figure 4-10 Timing Generator, Timing Diagram

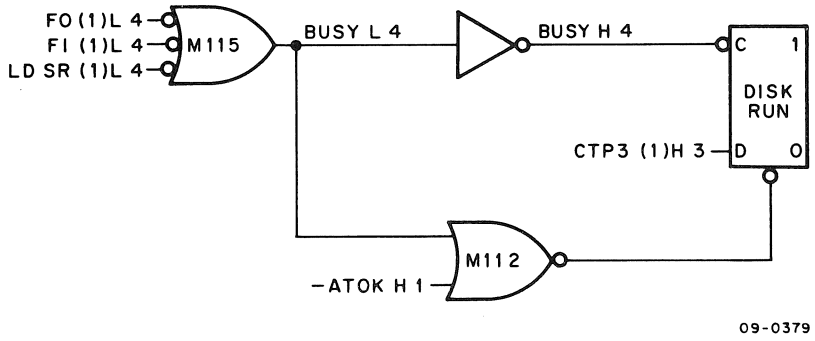


Figure 4-11 Unlock Sequence Logic

automatically increment as each channel and each disk fills up. The incrementing is done in the gap when the DISK RUN flag clears. Figure 4-12 shows the logic of these registers. WA 07 (0) H 13 is the most significant bit of the Word Address Register. When this bit clears (because the word address overflows), it sets INC TA. When the disk reaches the gap (and, therefore, after the last word has been read or written); INC TA is cleared when DISK RUN clears, and the TA Register is incremented. Similarly, the INC DA is set when the Track Address Register overflows at the beginning of the gap and the Disk Address Register is incremented. When DISK RUN sets, INC DA is cleared.

4.2.6 The Word Address Register

The Word Address Register is loaded from the computer and incremented each time a word is read or written by the flags SR0 (1) L 3 and SRI (1) L 4. These flags are covered in the read/write logic explanation (Paragraphs 4.3.2 and 4.3.3).

The Word Address Register is continually being compared to the Disk Segment Register, which holds the address of the segment cell about to rotate under the read/write head.

4.2.7 The Disk Segment Register and Transfer Rate Select Logic

Figure 4-13 shows a simplified version of the logic used by the Disk Segment Register and its associated interleave logic. Timing for the logic is given in Figure 4-14. The address pulses enter the Segment Register at gate 1. Initially all flip-flops are held on zero until the disk reaches its normal speed. DISK SYNC then sets. CTP 3 (1) L 3 then clears the system at the end of each word.

When the Segment Register begins to fill, the first bit of every address is always a 1. When this bit reaches the CTL flip-flop, the logic sees that a valid address has been assembled. The CTL then inhibits the B track inputs at gate 1 and enables the register to rotate. The clock pulse DS CLK L 12 may not stop, however, depending on the states of the three transfer rate switches HIGH H 12, MED H 12, and LOW H 12. Only one of these levels can be enabled at a time. If HIGH H 12 is on, then CTL is gated with it; and the DS CLK L 12 is stopped. Simultaneously, EQ CMP EN H 12 is sent to the comparison logic, and the contents of the Segment Register are compared to the contents of the Word Address Register. However, if MED H 12 is enabled, the contents of CTL are pulsed into the X MED Register before the comparison signal is sent out. The Segment Register is rotated once to the right by the same pulse. If LOW H 12 has been enabled, another clock pulse is allowed to shift the CTL bit into the X LOW Register before a comparison is made, and the Segment Register is rotated twice with its original address.

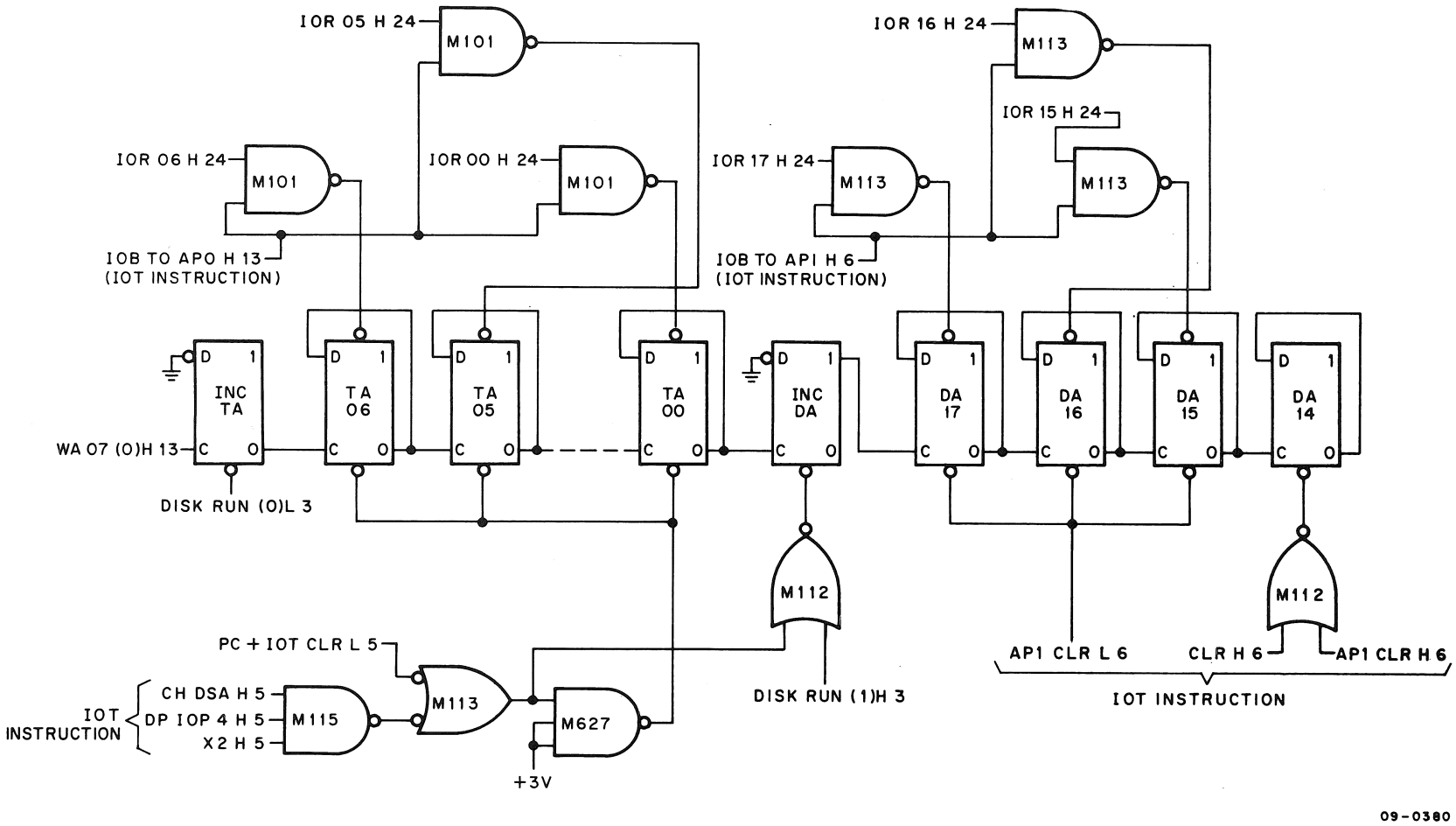
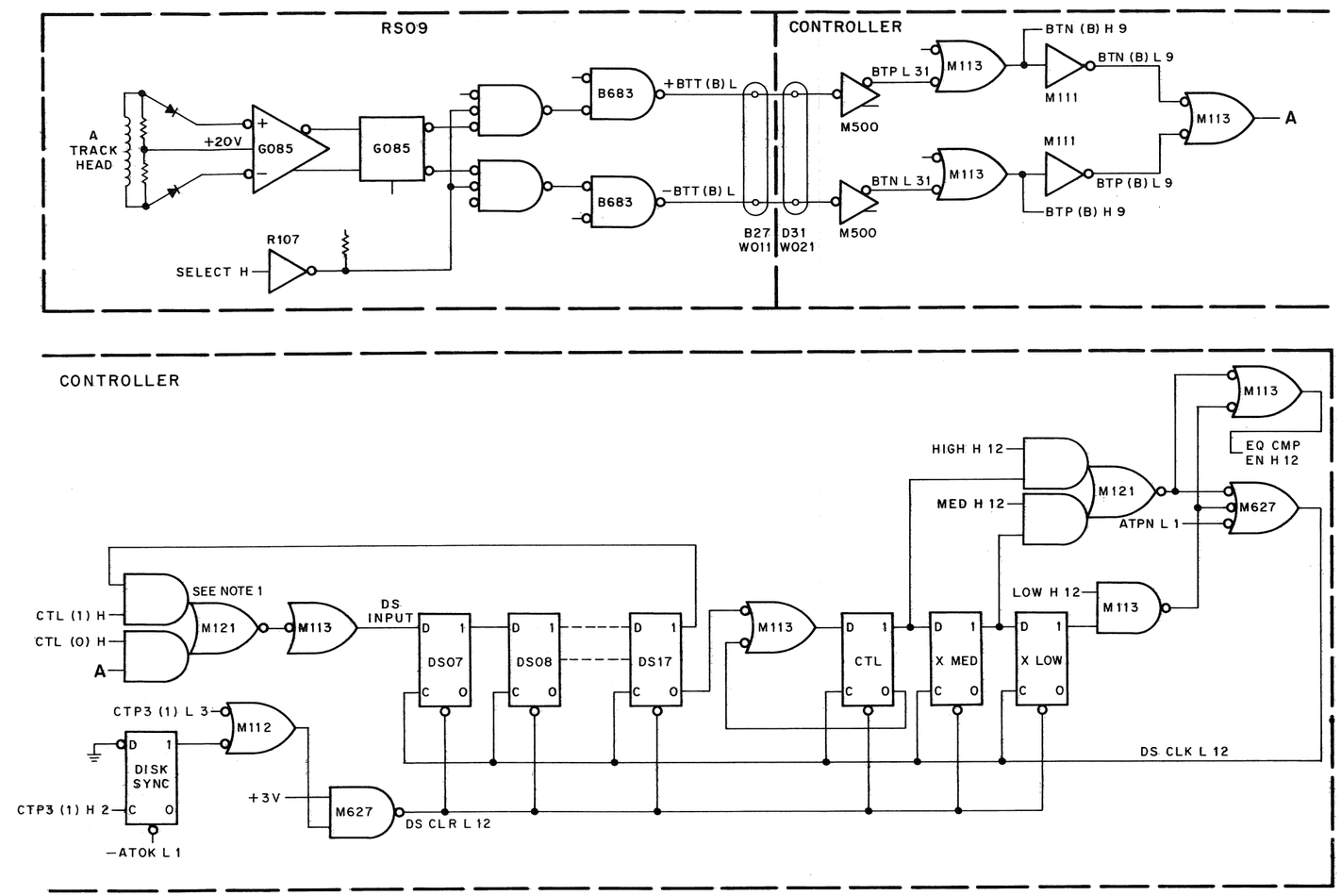


Figure 4-12 Track and Disk Address Register



NOTES:
1. CTL, XMED, XLOW determine when the EQ COMP EN H 12 signal comes, i.e, the comparison check between the two addresses.
2. The DS shifts until CTL is set, then it starts to shift around.
3. At the end of the word the registers are cleared.

Figure 4-13 Disk Segment Register and Transfer Rate Select Logic

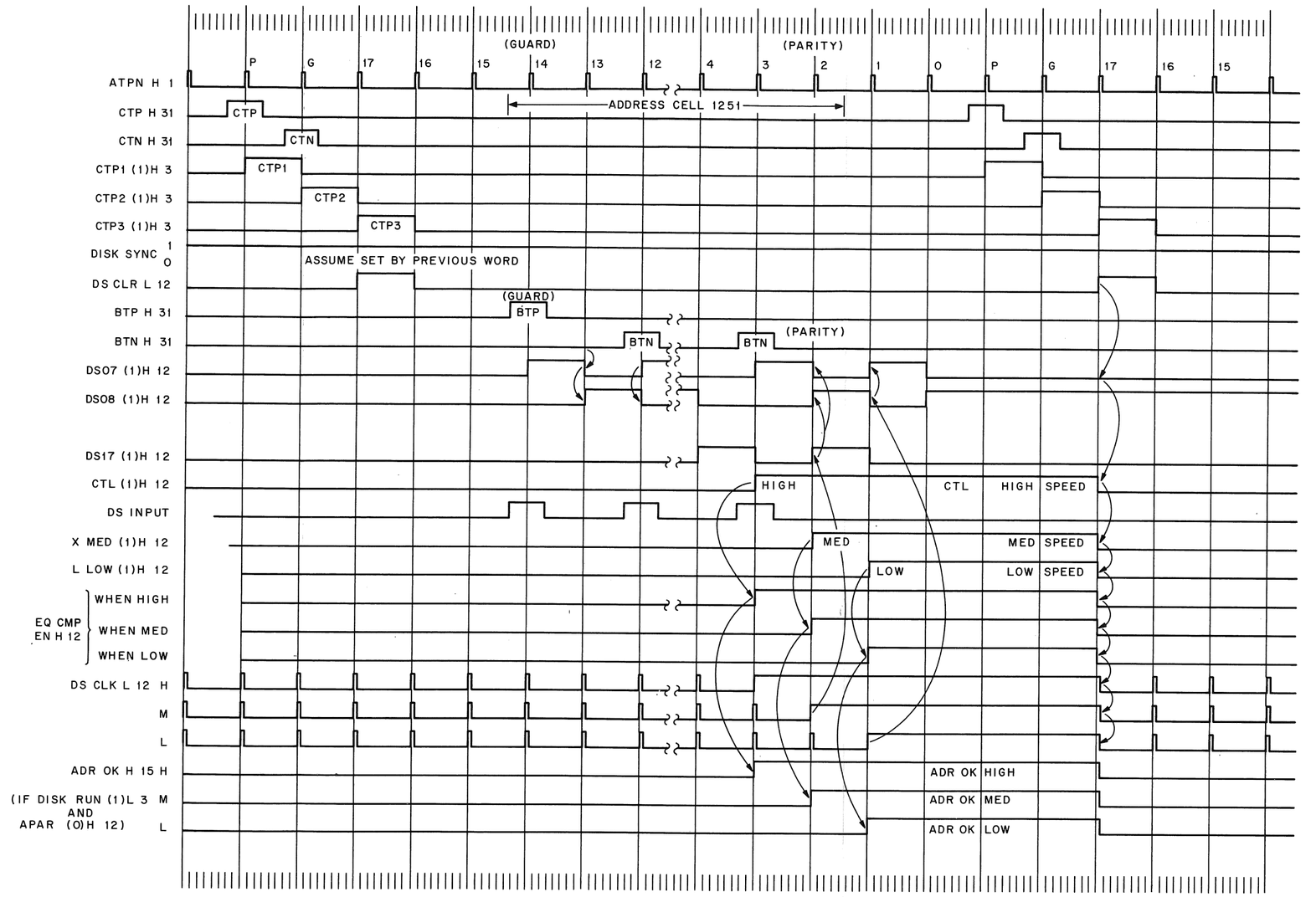


Figure 4-14 Disk Segment Register, Timing Diagram

Rotating the register once or twice to the right forces the disk to accept every second or fourth address as the valid address it was seeking. By rotating once, every second address is transformed into a number that is equal to every successive address. Alternately, by rotating twice, every fourth address transforms into a number that equals every successive address. The Word Address Register sees no difference; it takes either twice or four times as long to get the comparison. Table 4-2 illustrates the way this transformation occurs for a 3 bit register. (Table 4-2 assumes that the Word Address Register was loaded with 2, and the Segment Register was at 1.)

Table 4-2
Rotating The Disk Segment Register

Contents of Word Address Register	Contents of Disk Segment Register	Contents of Disk Segment Register Rotated Once	Equal Comparison	
010	001	100	NO	
	010	001	NO	
	011	101	NO	
	100	010	YES	FIRST
011	101	110	NO	ROTATION
	110	011	YES	
100	111	111	NO	
				GAP
	000	000	NO	
	001	100	YES	
101	010	001	NO	
	011	101	YES	SECOND
110	100	010	NO	ROTATION
	101	110	YES	
111	110	011	NO	
	111	111	YES	
				GAP
000	000	000	YES	
001	001	100	NO	FIRST
	010	001	YES	ROTATION
010	011	101	NO	NEXT
	100	010	YES	TRACK
011	101	110	NO	

When an equal comparison is found, the Word Address Register is incremented; and the data is transferred to or from that address.

4.2.8 Equal Comparison Gating

Figure 4-15 shows a simple block diagram of the equal-comparison gating between the Disk Segment Register and the word Address Register. The two registers are compared in parallel with a series of EXCLUSIVE OR gates. If they compare favorably without a parity error on the address track to invalidate the comparison, and if the controller is performing and DISK RUN is set; then ADDRESS OK (ADR OK H 15) informs the control logic to continue its operation.

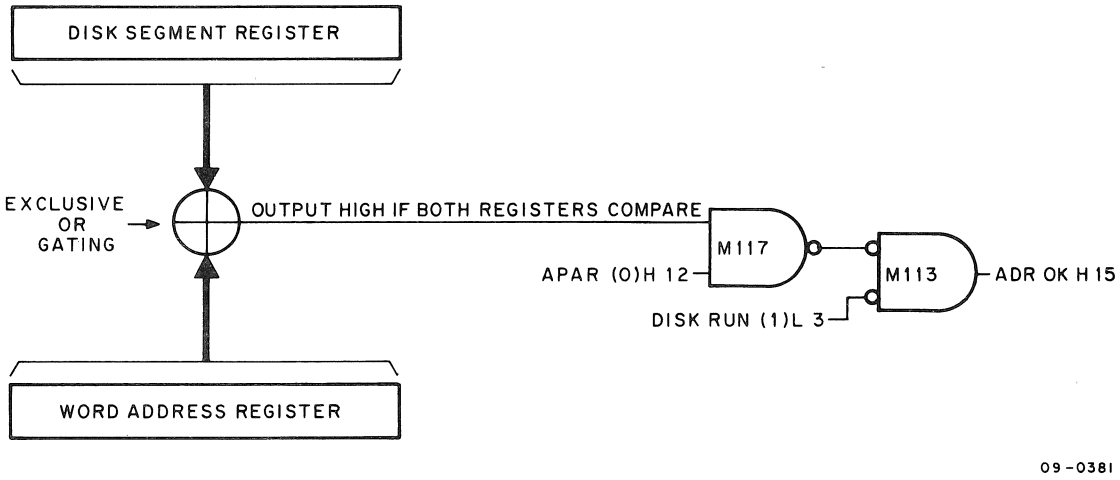


Figure 4-15 Equal Comparison Gating

4.2.9 The Address of the Disk Segment Register (ADS)

After a valid address has been assembled into the Disk Segment Register, the address is transferred to the ADS Register (see Figure 4-16) and becomes available to the programmer under IOT command. The transfer takes place when CTL sets but before XMED, provided that the programmer is not reading the current contents of the ADS. The flip-flop that strobes the DS into the ADS is reset when CTL resets or at TP2 (if XMED is set). Note that the address placed into the ADS Register is the real segment address, and not the address calculated by the disk segment logic for low or medium transfer speeds. The address is accurate to within one segment.

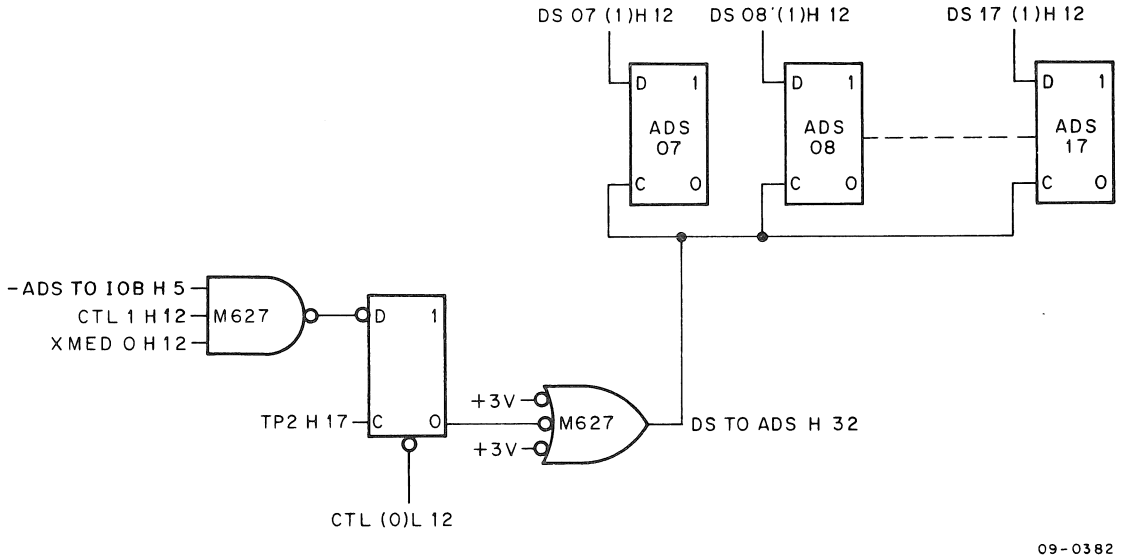


Figure 4-16 ADS Register Logic

4.3 THE DATA SECTION LOGIC

4.3.1 The Buffer and Shift Registers

The Buffer and Shift Registers are continually passing data back and forth during the course of a data transfer. The Buffer Register accepts the data word from the computer during a multi-cycle data break and passes the word down to the Shift Register for writing on the disk surface. Alternately, during a READ operation, the Shift Register assembles a word off the disk and passes it on to the Buffer Register to be transferred to the computer. Figure 4-17 shows the data paths between the two registers. The Buffer Register is filled from the bus (IOR 00 – IOR 17) with the pulse IOB TO BRH H 19. The Buffer Register transfers data to the Shift Register under the command BR TO SR H 17. The Shift Register in turn transfers an assembled word to the Buffer Register with the BR TO SR H 17 signal. The logic that controls these signals is explained in conjunction with READ/WRITE and WRITE CHECK operation (Paragraphs 4.3.2, 4.3.3, and 4.3.4).

4.3.2 The WRITE Operation and its Associated Logic

Figures 4-18, 4-19, and 4-20 show the logic and timing affecting the controller during a WRITE operation. Assume that the WRITE function has been loaded into the Function Register and that all other registers have been duly initiated (see Figure 4-18). The continue IOT is issued (IOT CONT H 6), and it posts the first DATA FLAG. The three-cycle data break responds by loading the first word into the Buffer Register with the signal IOB TO BR H 19. At the same time the WB FULL flag is set, indicating to the controller that the Buffer Register has valuable information in it that must not be written over. The disk rotates and checks for equal comparison between the Segment Register and the Word Address Register. As soon as ADR OK is seen, the level LS EN H 4 enables the AND gate, which drives the D input to the critical flip-flop SRI. On the first CTP (1) H 3, which indicates that the cell to be written into is almost under the read head, SRI is set. SRI then increments the Word Address Register, jams the Buffer Register into the Shift Register with the signal BR TO SR H 17, sets LD SR (1) H 4, and clears WB FULL.

The Shift Register immediately begins to shift the data word out into flip-flop WR DA, which is driven down a cable to the disk drive itself. (See Figure 4-20.) The data bits are clocked into the G290 writer and through the heads to be written as flux changes on the surface of the disk. Note that the disk must be selected, a WRITE operation must be in process (LD SR and FI SV (0) H 4), and no lockout switch can be enabled (LOCK H), or the data bits are disabled at the input gates of the writer.

Gate 1, which AND's CTT (L) and ATT (L), clears the G290 Register before and after the data word is written. If the G290 flip-flop ends the word on a zero, the word had even parity; i.e., an even number of 1s in it. This gate has no effect. If the word had odd parity, the G290 ends up a 1 and is cleared by this gate; the flux change records another 1 and also generates the even parity that a complete word should have. In this way, each word is guaranteed to have the even parity for which it is checked during READ operation.

4.3.3 The READ Operation and its Associated Logic

Figures 4-21, 4-22, and 4-23 show the logic and timing affecting the controller during a READ operation. (See Figure 4-21.) The logic up to DASV was explained in the description of the error detection circuitry (Paragraph 4.1.1). Each time PDT or NDT is set and subsequently reset by TP2, indicating that a 1 bit has arrived, DASV goes to a 1. The SR CLK H 17 pulse then shifts the data down the Shift Register until the word is completely assembled.

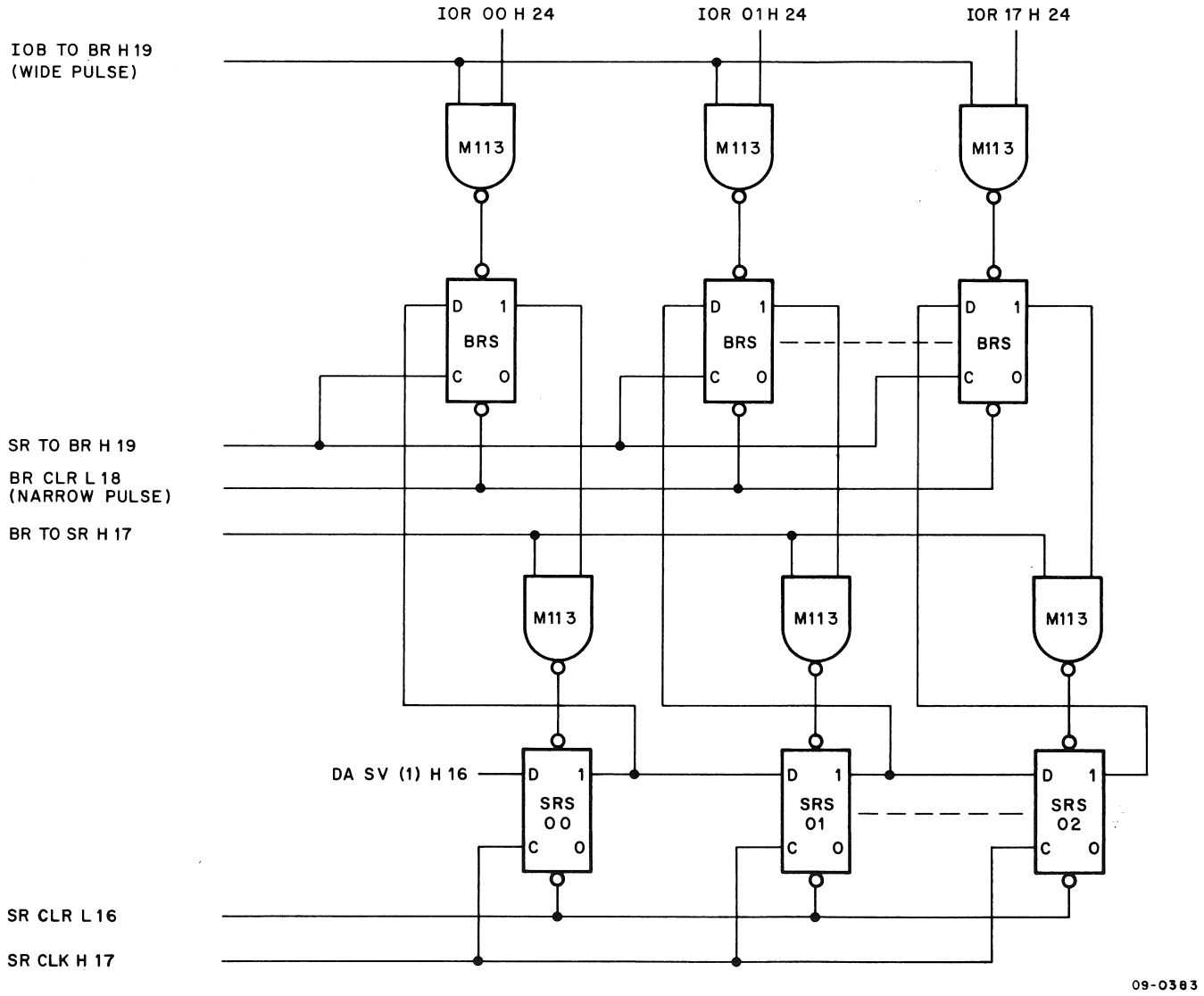


Figure 4-17 Buffer Register and Shift Register Interconnections

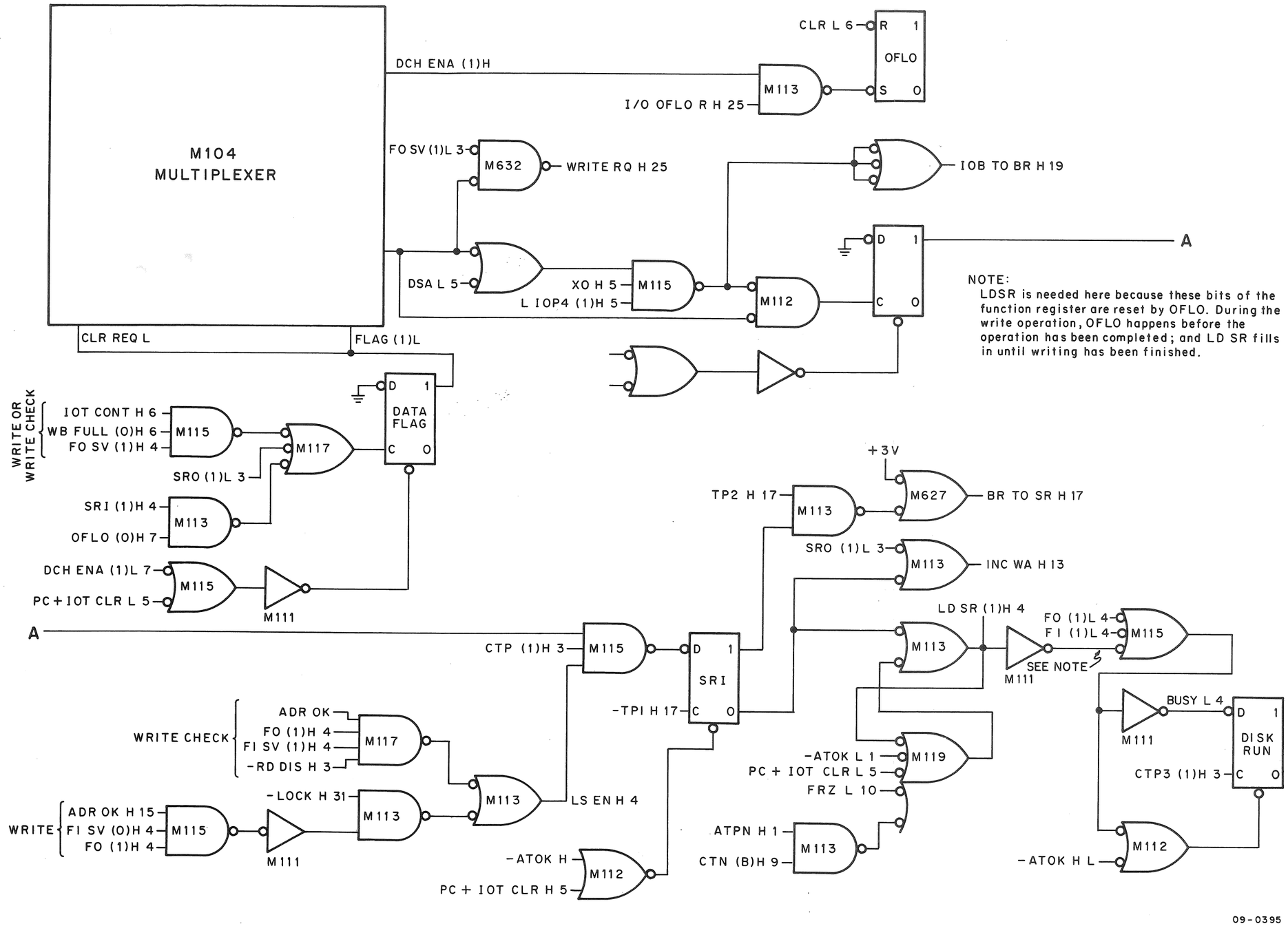


Figure 4-18 DCH Control for WRITE and WRITE CHECK

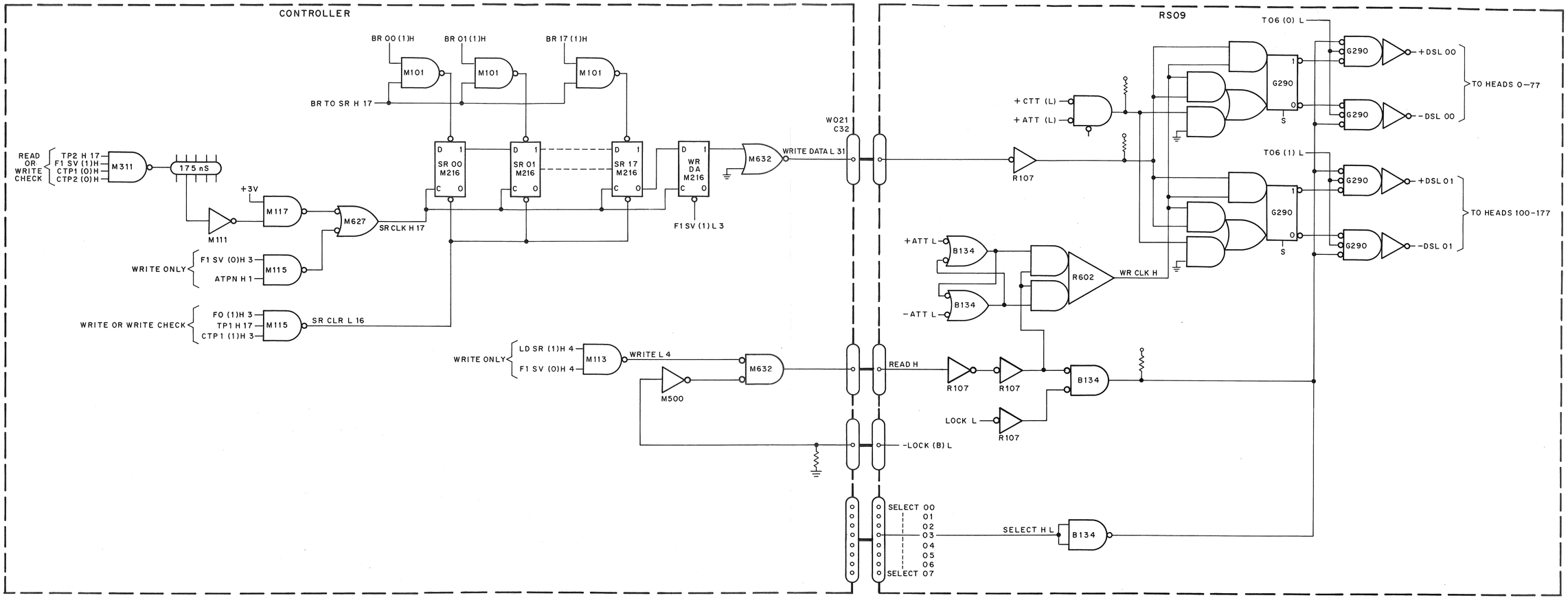
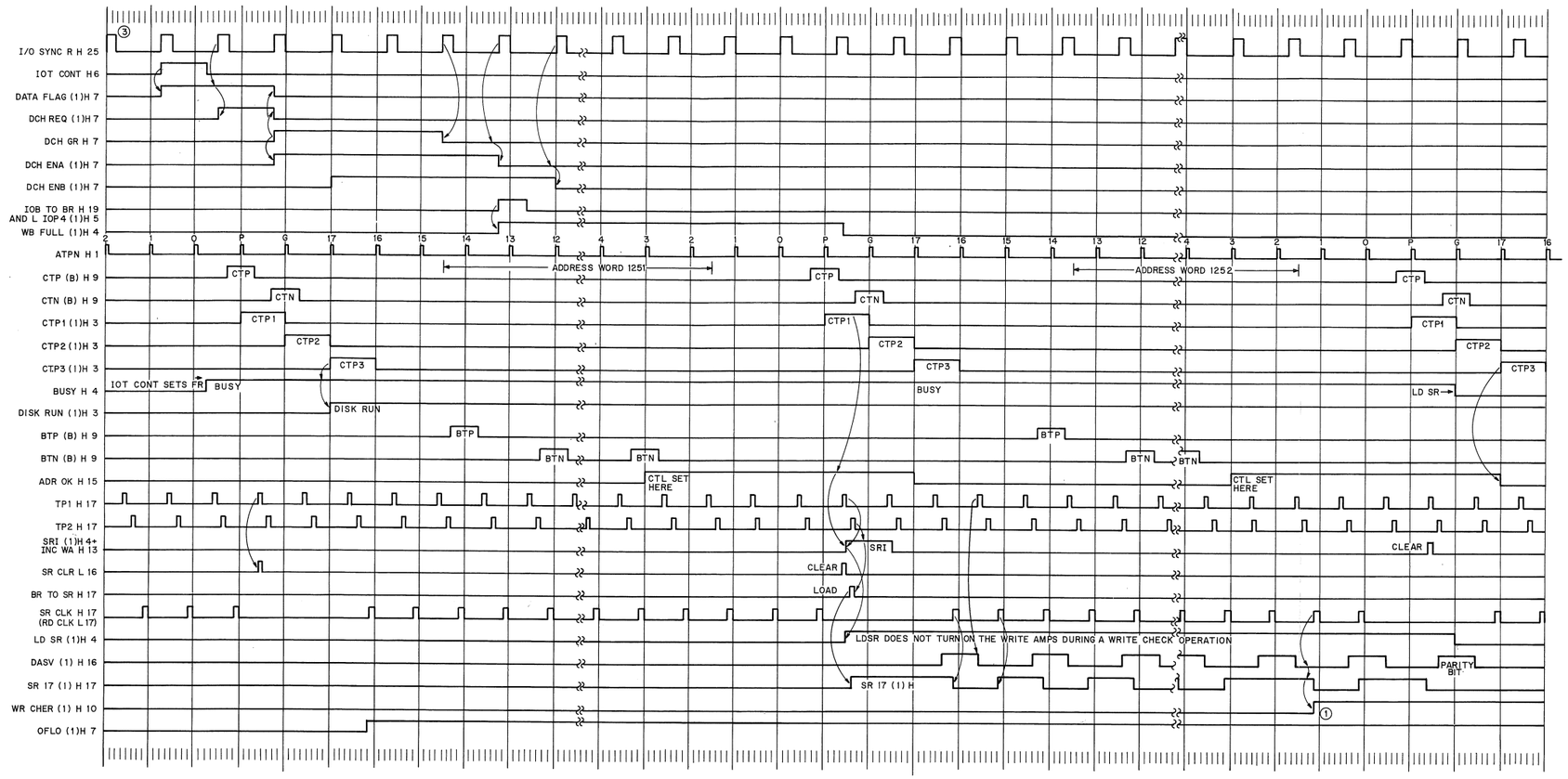


Figure 4-19 WRITE Circuitry



NOTE:

1. The WR CHER (write check error) is posted here because SR17 and DASV are not the same at this point. Since parity is ok it suggests that the word was read into the computer wrong.
2. The write check timing is very similar to the write timing, except that the write amplifiers are inhibited and the shift register is allowed to read the disk data. Reading is done after the data to be compared is in the shift register. SR17 and DASV are compared bit by bit as the SR is shifted.
3. I/O sync is asynchronous with all controller timing pulses.

Figure 4-20 WRITE Operation for One Word In Address 1251

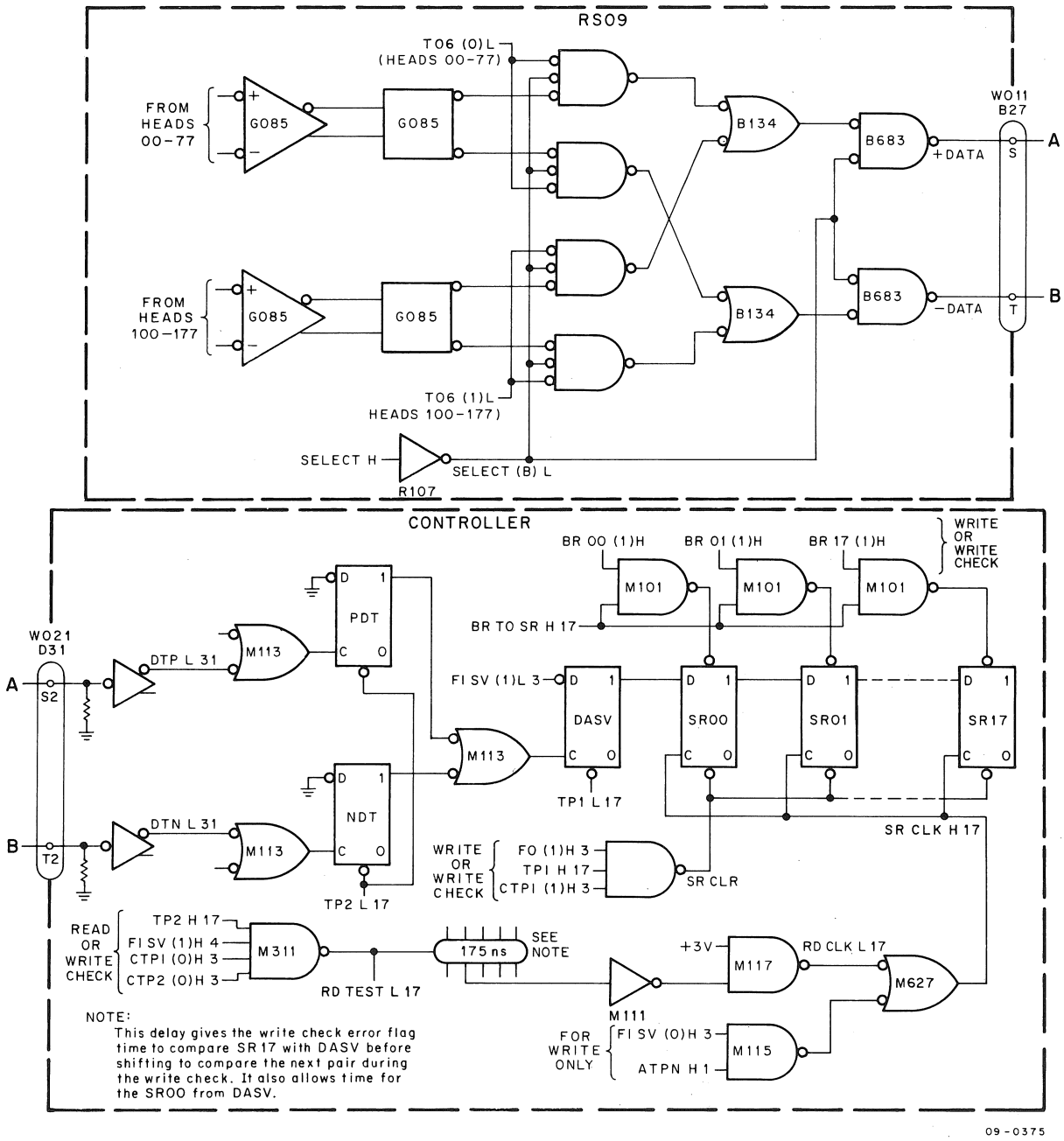


Figure 4-21 READ and WRITE CHECK Logic

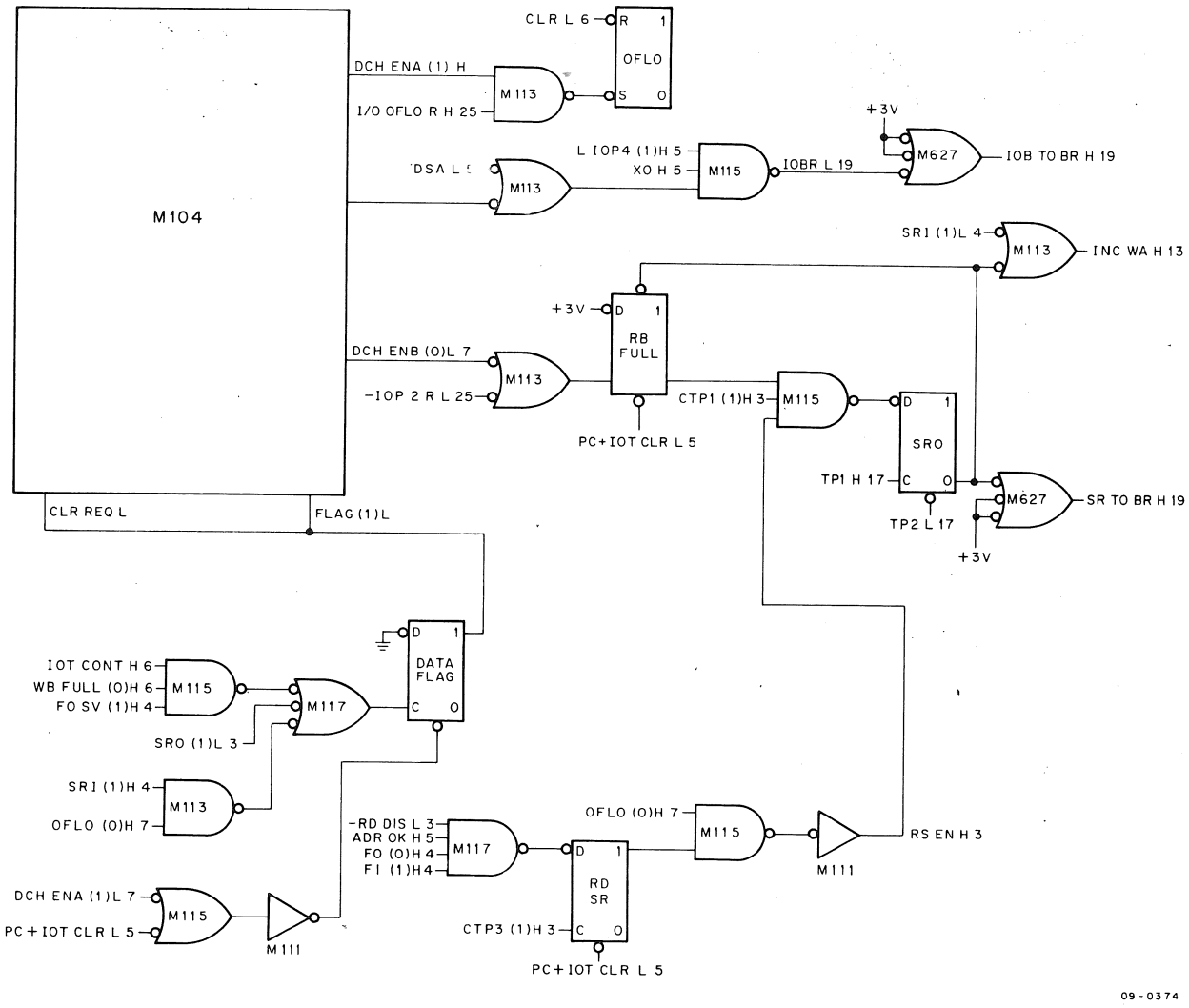


Figure 4-22 DCH Control for READ

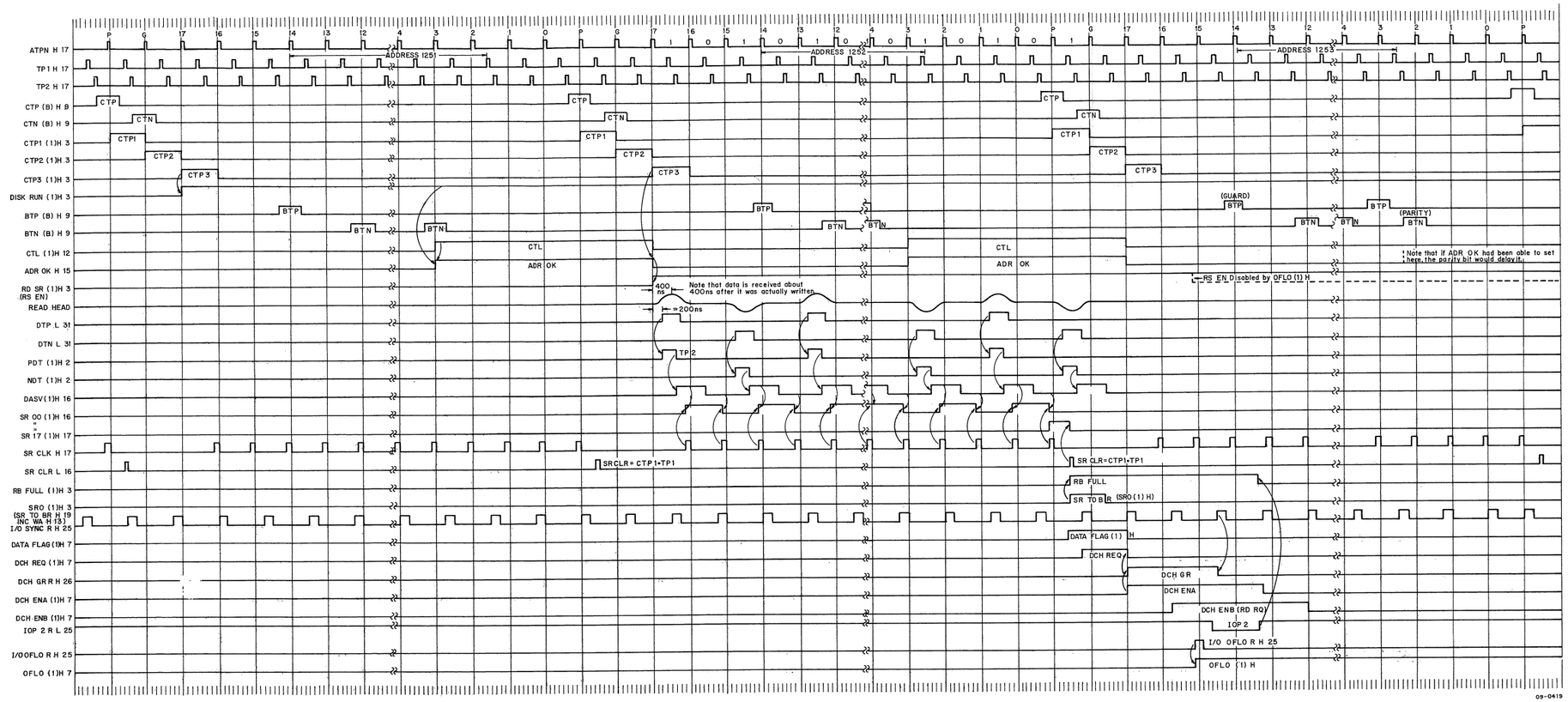
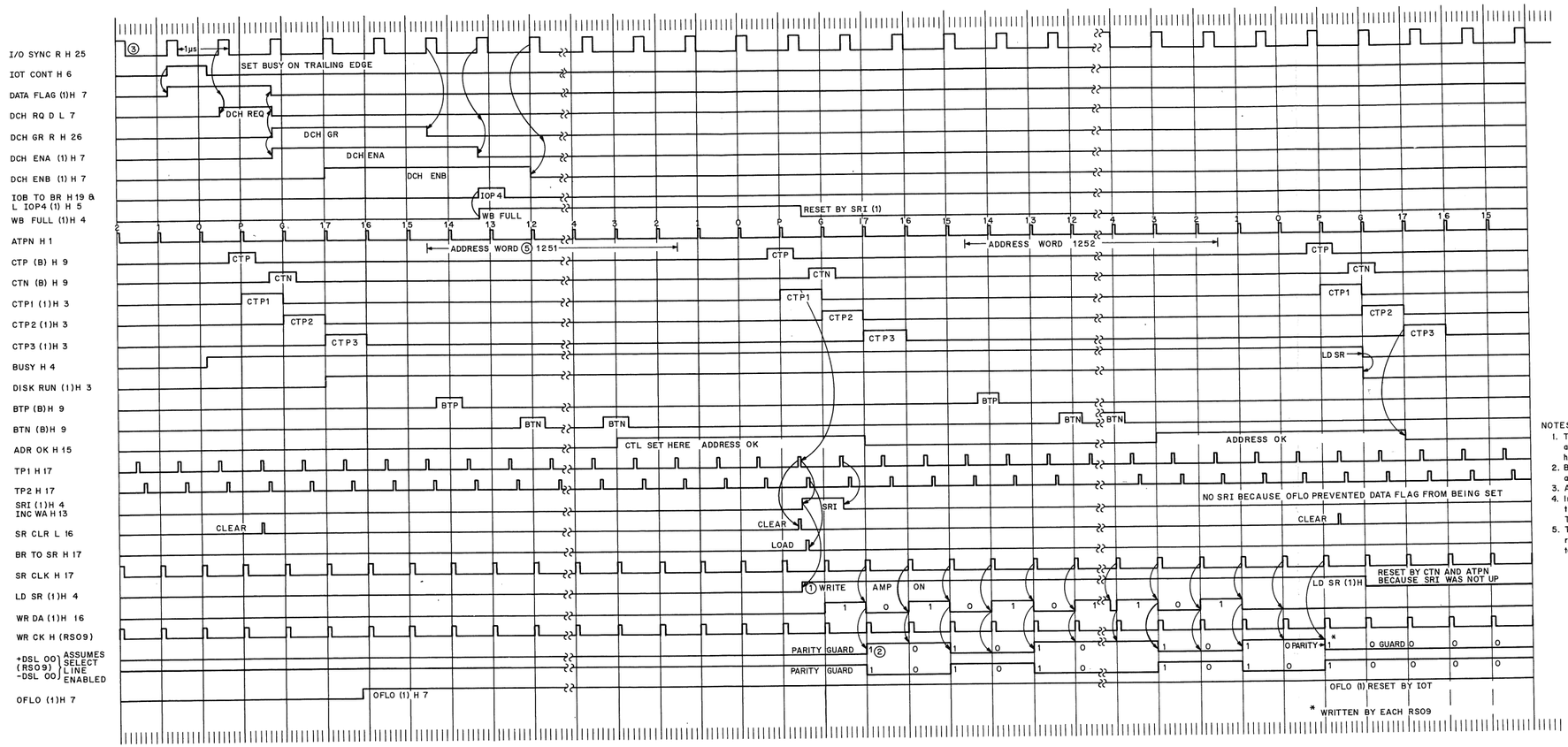


Figure 4-23 READ Timing Diagram for One Word in Address 1251



NOTES

1. The write amps are turned on early to wipe out a possible garbage area where sneak bits may have been written due to disk jitter.
2. Because of logic and head delays the track is actually written 400ns later than each ATT.
3. ATPN & I/O SYNC are asynchronous.
4. In this write operation, one word was transferred to address 1251 with the disk at high speed. The word transferred was 252525.
5. The address word comes one word before its related data word to allow time for the address to be shifted into its register and acted upon.

Figure 4-25 WRITE CHECK Timing Diagram for One Word in Address 1251

At CTP1 time, the SR0 flag (Figure 4-22) is enabled (provided ADR OK H5 is present, indicating that this word is the word needed) and sets with TP1. SR0 generates SR T0 BR H 19, and the contents of the Shift Register are jammed into the Buffer Register. At the same time, SR0 sets the DATA flag, and a three-cycle request is started. CTP1 and TP1 clear the Shift Register for the next transfer. SR0 sets RB FULL, which will stay set until the computer takes the word in the Buffer Register, and releases it to the Shift Register for the next word. During the data break, DCH ENB of the M104 module clears RB FULL when IOP-2 disappears. At this time, the I/O processor has just taken the data, and the next word can be transferred.

The flag RD SR is assumed to be set in this discussion. It sets on the first CTP (1) H 3 after the READ function is selected, provided that the level RD DIS L 3 is present (i.e., the READ operation has not been disabled); and ADR OK has been generated by the comparison logic. (RDSR remembers that a valid word is being assembled.) RD DIS L 3 is explained in Paragraph 4.3.7 with the Start Up circuits.

4.3.4 The WRITE CHECK Operation and its Associated Logic

WRITE CHECK combines the logic and timing of both the READ and the WRITE functions. The purpose of WRITE CHECK is to compare the data in memory to corresponding data in the disk. Each word in memory is transferred into the Buffer Register as though a WRITE operation were in progress. The data is moved to the Shift Register under the same conditions as it is moved for a WRITE. Now, however, the logic starts to READ. (See Figure 4-21.) The disk word is shifted into DASV and the low end of the Shift Register, while the memory word is shifted out of the high end. SR17 and DASV always have related bits; that is, the words are compared bit by bit between DASV and SR 17 as they are shifted into and out of the Shift Register. Figure 4-24 shows the comparison logic. If the two do not compare favorably, the error flag WR CHER is set. The effects of this flag are discussed in Paragraph 4.3.5. Figure 4-25 shows the timing for the WRITE CHECK operation.

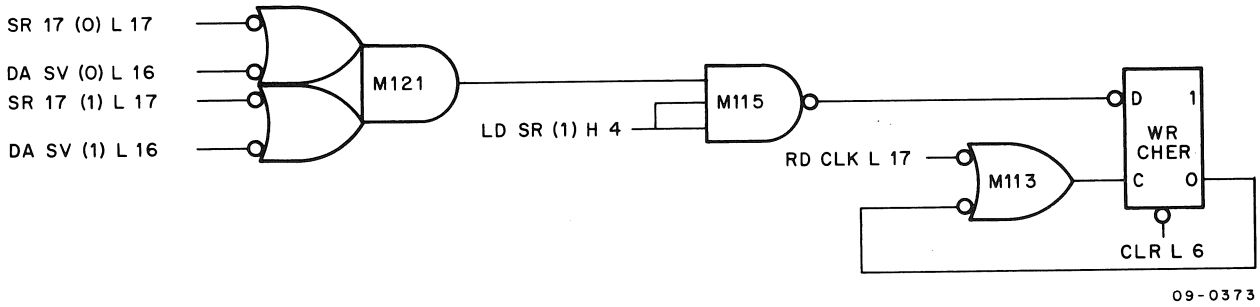


Figure 4-24 WRITE CHECK Error

4.3.5 Error Flags

The following paragraphs describe the logic that sets the various error flags.

4.3.5.1 **WRITE CHECK Error** – The WRITE CHECK error (WR CHER) is closely associated with the WRITE CHECK operation described in Paragraph 4.3.4 (see Figure 4-24). The WR CHER flip-flop is set if SR17 and DA17 logic levels differ at LDSR time. Because WR CHER (1) L is fed back, WR CHER remains set until cleared by CLRL.

4.3.5.2 **Error and FReeZe** – A FReeZe (FRZ) condition occurs if an A, B, or C track error is detected, or if the address track indicates a parity error (see Figure 4-26). The ERROR flag that causes an interrupt, either PI or API, is the OR of the flags shown in Figure 4-26.

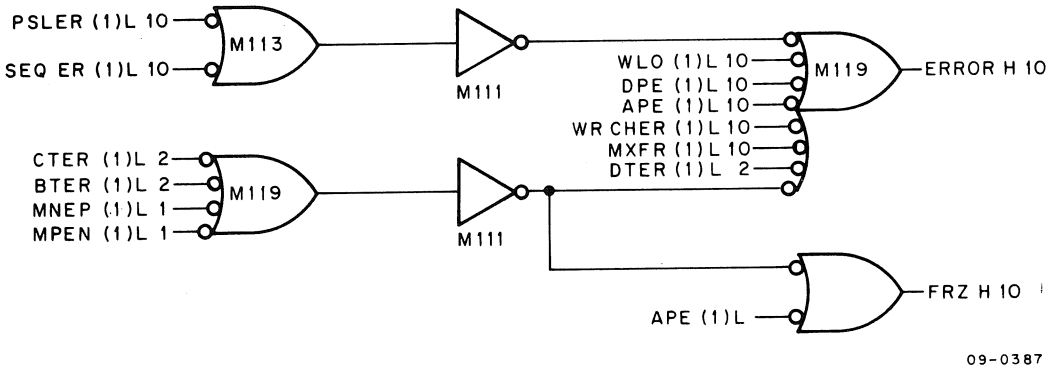


Figure 4-26 Error and Freeze

4.3.5.3 **Address Parity Error** – The APAR (Address Parity) flip-flop continually examines the address bits (see Figure 4-27). Parity must be even; if on the last address bit, APAR is set, a parity error has occurred. As a result, the APE (Address Parity Error) flop is set at CTP2 time. The APAR flop remains set until cleared by CTP3 or DISK RUN.

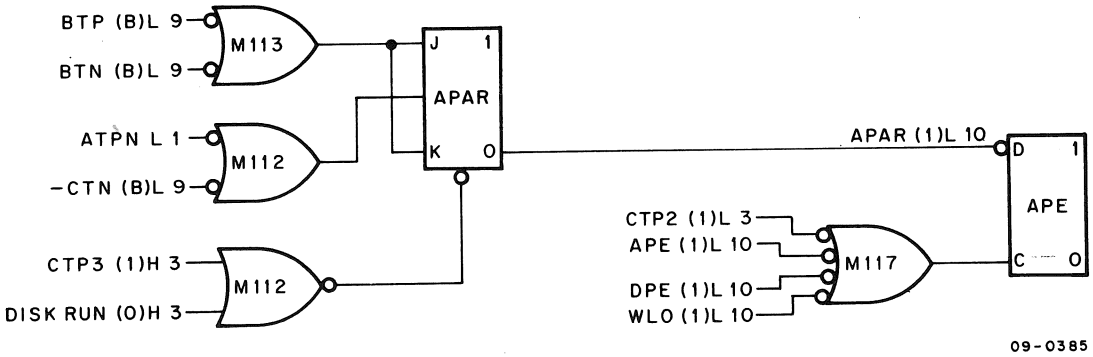


Figure 4-27 Address Parity Error

4.3.5.4 **Missed Transfer Error** – The MXFR (Missed TransFeR error) flag is set if there is no DCH ENB (1) L 7 signal (see Figure 4-28). (For example, no data transfer through the three-cycle data break after BUSY has been on for 130 ms, or two or three revolutions.)

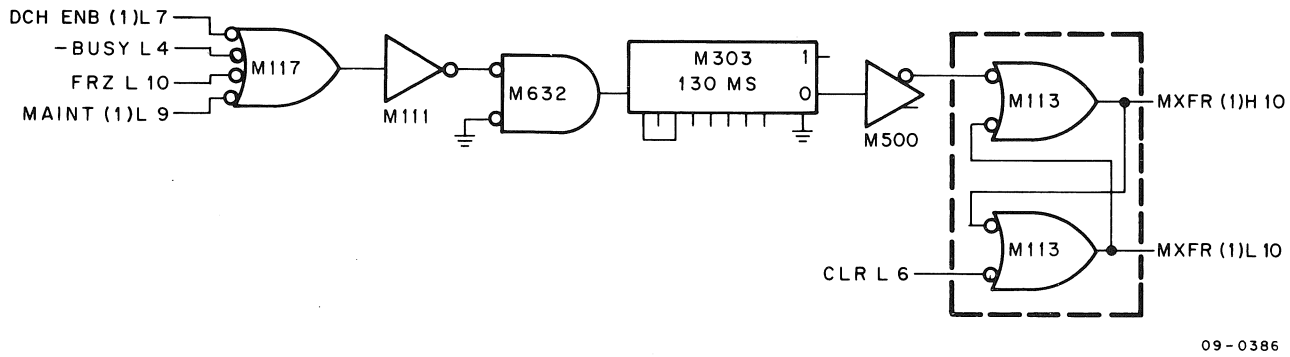


Figure 4-28 Missed Transfer Error

4.3.5.5 Data Parity Error – The DPAR (Data PARity) flag should be reset when the data word has been completely assembled (even parity) (see Figure 4-29). If the word is not completely assembled, DPAR remains set, indicating a data parity error. As a result, the DPE (Data Parity Error) flip-flop is set at CTP2 time, if a READ operation has been specified and either RD SR is asserted (indicating valid data has been transferred) or LD LY is set (indicating a WRITE CHECK operation has been performed).

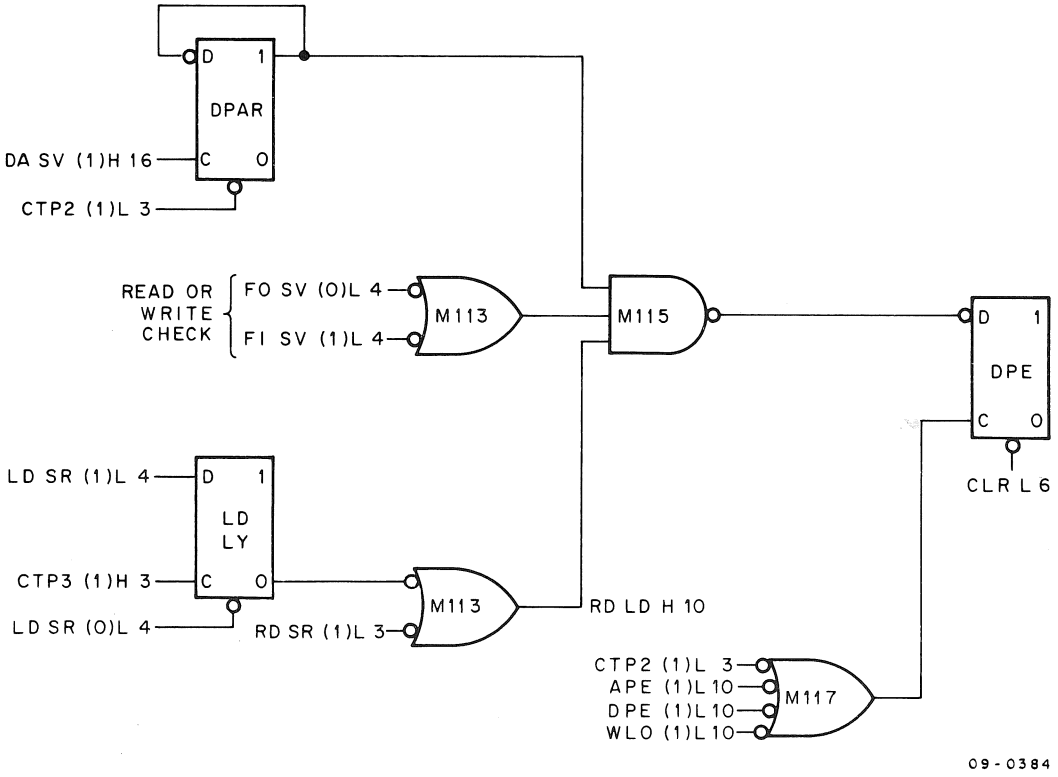


Figure 4-29 Data Parity Error

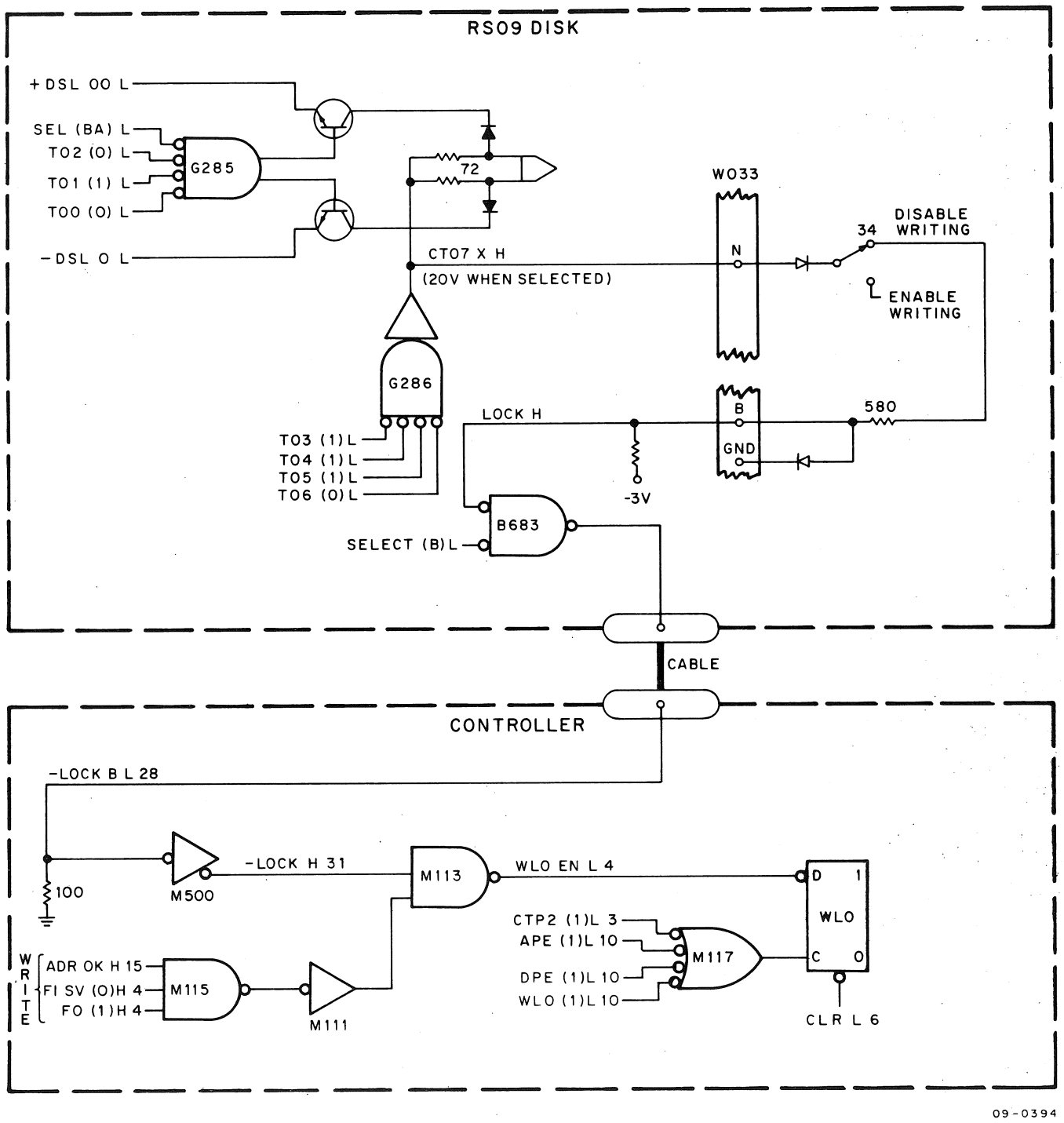


Figure 4-30 Write LockOut Error

4.3.5.6 NonExistent Disk Error (PSLER) – The PSLER (Program Select Error) flip-flop sets if there is a SEL ERR (nonexistent disk selected) after a program-controlled disk selection (IOB TO AP1) (see Figure 4-30). The difference between PSLER and SEQER is that PSLER is the result of a program error rather than an error caused by stepping over bounds during a transfer. The 1.5 μs delay allows the selection logic (SEL ERR) to settle. The PSLER flag causes an NE DSK (NonExistent DiSK) error signal.

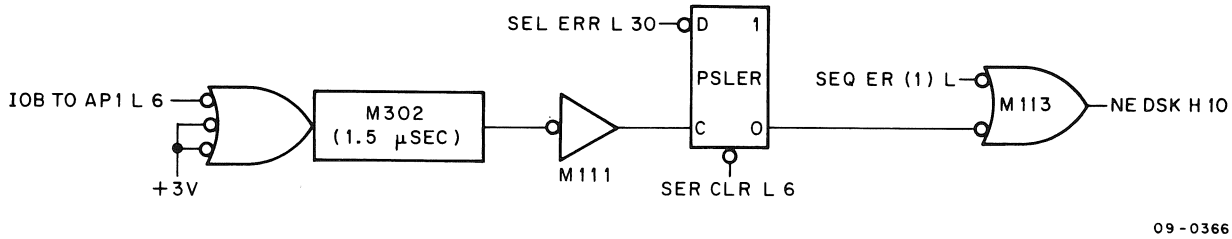


Figure 4-31 NonExistent Disk by Program Selector Error

4.3.5.7 Write LockOut Error – The CT07 xH output of the G286 is +20 dc when selected (see Figure 4-31). The +20V signal is applied to the B683 driver when switch 34 is set to DISABLE WRITING. If the disk has been selected, a negative level is applied to the controller, converted, and gated to the WL0 (Write LockOut) flip-flop. The gating signals are generated before a valid WRITE operation.

At CTP2 time, WL0 is set (if no data or address parity errors have been detected). Simultaneously, the WRITE operation is interrupted by LOCK H 31, as shown in Figure 4-18, and the SRI flip-flop cannot be set.

4.3.5.8 NonExistent Disk (SEQ ER) – The NE DSK error signal can also be produced by the SEQ ER (Sequence Error) flag (see Figure 4-32). The Sequence Error flag is set under the following conditions:

a. If SEL ERR is enabled, indicating that a nonexistent disk has been selected.

b. If DA15 overflows, indicating that the system capacity has been exceeded and the 9th disk was selected.

The flag is set by INC DA, which is delayed to wait for the settling time of the Disk Select logic. It is then gated with BUSY and RB FULL (0) to the SEQ ER flip-flop. RB FULL (0) is only asserted if OFLO has not occurred indicating that this was not the last word and an error condition actually exists. The SEQ ER flag causes an NE DSK error signal.

NOTE

The SEQ ER flag is set only during a job transfer and not by an error in program control transfer.

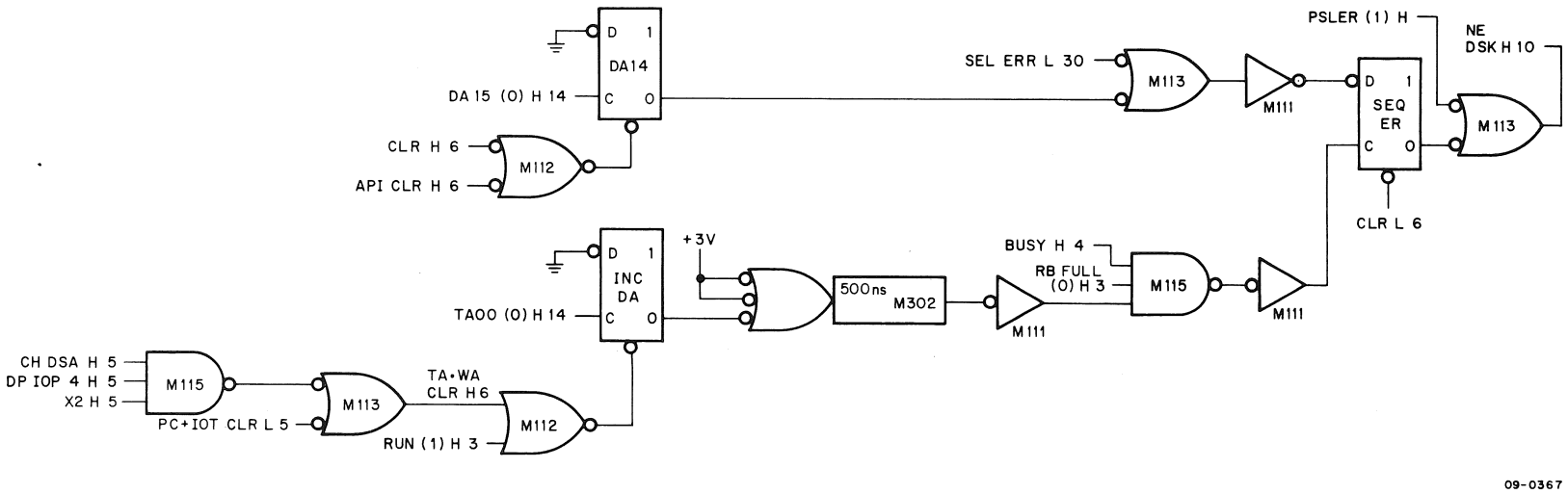


Figure 4-32 NonExistent Disk by Sequence Error

4.3.5.9 Data Channel Timing Error – (See Figure 4-33.) The DCH TE (Data Channel Timing Error) flag sets under the following conditions:

a. During READ, if RSTE does not get reset by SR0 after CTP1 and before CTP3. This indicates that the data was not read by the data channel before SR was ready with the next word.

b. During WRITE or WRITE CHECK, if LSTE does not get reset by SRI after CTP1 and before CTP3. This indicates that the data channel did not load the BR in time to transfer the SR to be written on the disk.

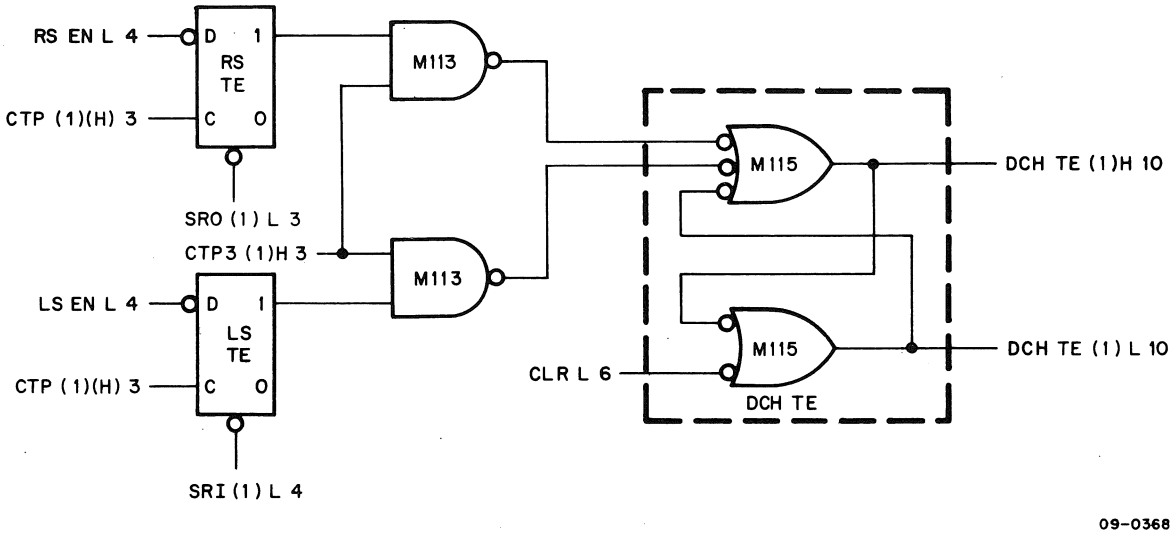


Figure 4-33 Data Channel Timing Error

4.3.5.10 Program Error – The PE (Program Error) flag is set if the computer issues an illegal IOT while the machine is doing a preset operation (see Figure 4-34). The STOP flag is set on these IOTS when BUSY is on. Under these conditions, PE is set directly by STOP.

4.3.6 Automatic Priority and Program Interrupt Logic

When an operation has been completed, the computer word count overflows and the OVERFLOW flag is posted (Figure 4-35). This flag generates the XFER CPLT L 17 signal, which is gated with INT EN (1) L to cause an API or PI break. A break can also occur if the ERROR L 10 signal, which is the logical OR of a number of errors that may occur during an operation, occurs. These errors are covered in Paragraph 4.3.5. Note that the BUSY signal is gated with OFLO to post the interrupt, which ensures during a WRITE operation that the function is finished before the interrupt is posted. (Note that during a WRITE operation OFLO happens after the word is transferred but before it has been written.

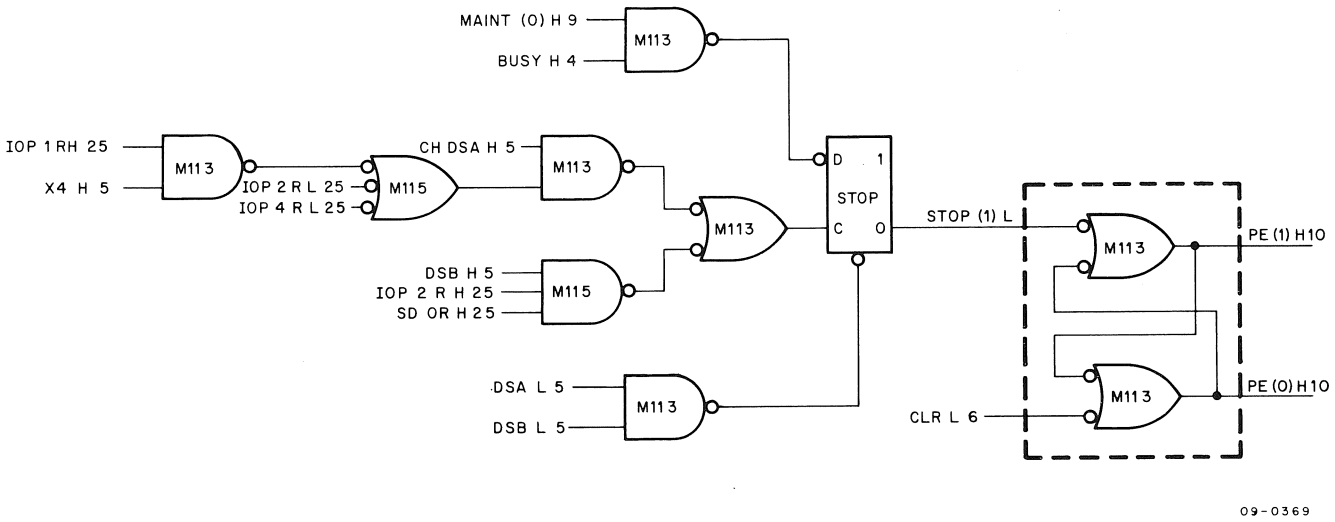


Figure 4-34 Program Error

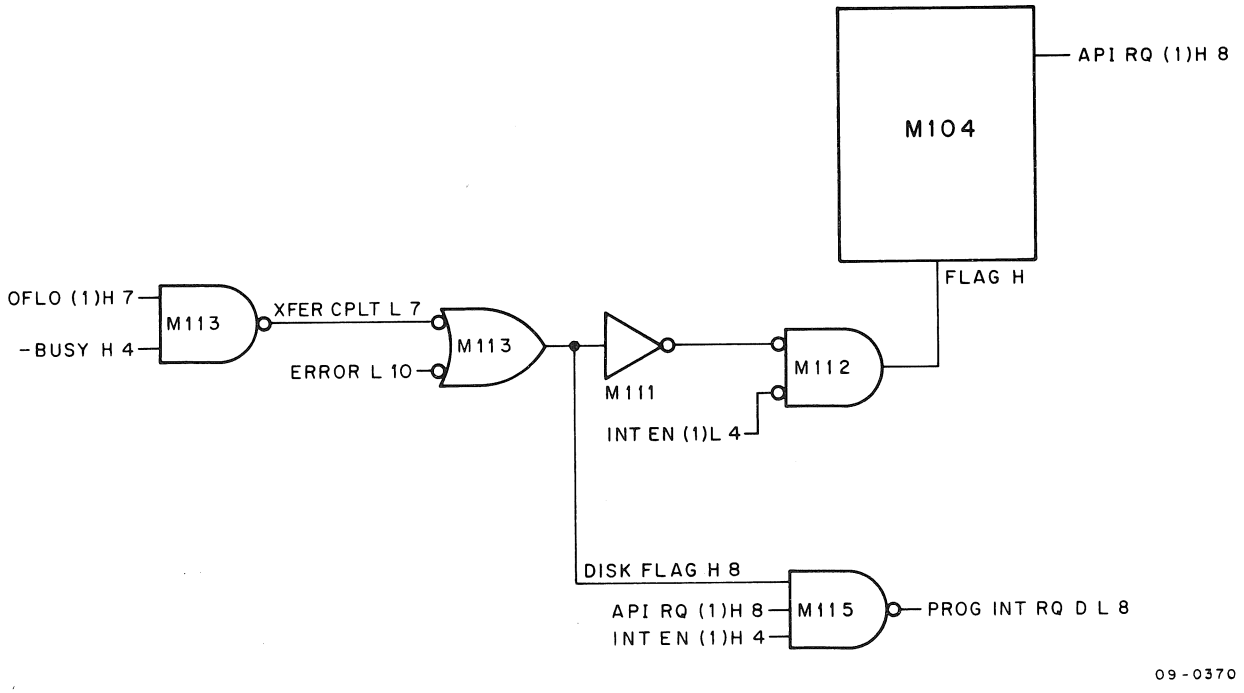


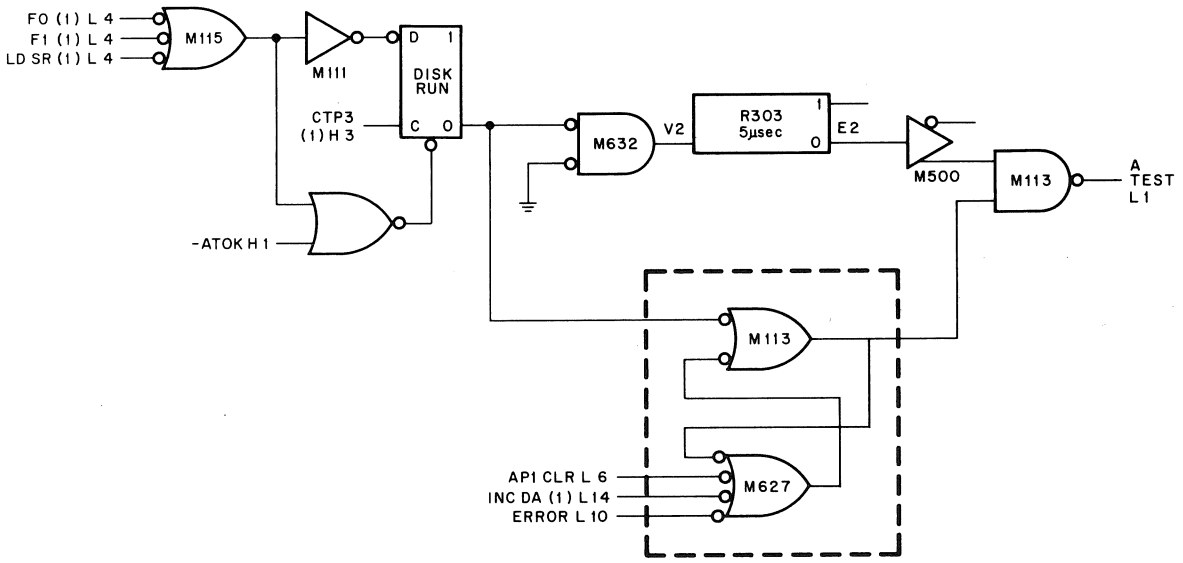
Figure 4-35 Automatic Priority Interrupt and Program Interrupt Logic

4.3.7 The A TEST and Read Disable Signal

Several flags in the controller sense when the system is in a position to perform. The most critical of these flags is the DISK RUN flag (see Figure 4-36). This flag sets if there is a valid operation specified in the Function Register, the A track timing pulses are arriving on time, and a CTP3 (L) H3 level has asserted itself. Only if DISK RUN is set will ADR OK be allowed to happen (thereby allowing a READ, WRITE or WRITE CHECK operation). Note that DISK RUN resets as soon as ATOK goes away. This happens only if one of the A track pulses is dropped because of an error or because of the gap, as described in Paragraph 4.1. One of two error flip-flops also sets to indicate where the error occurred. The R303 delay, which is held high by DISK RUN, times out and resets, disabling A TEST L 1 and stopping all timing track signals. The time it takes for the delay to reset gives the A track error detection logic a chance to set the appropriate error flag.

The R303 is triggered when DISK RUN is set. It does not reset until 5 μs after DISK RUN is reset, allowing A TEST L an extra 5 μs to function and the MNEP and MPEN flip-flops to set on the error condition.

Note that if ATOK was used (in place of A Test), no A timing error could ever exist.



NOTE:
The R303 is triggered when DISK RUN is set. It does not reset until 5µsec after DISK RUN is reset, allowing A TEST L an extra 5µsec to function, and the MNEP and MPEN flip-flops to set on the error condition.
If ATOK was used (in place of A TEST), no A timing error can exist.

09-0371

Figure 4-36 Disk Run Logic

The Read Disable signal is developed in Figure 4-37.

NOTE

A READ operation is inhibited from starting for 200 μs when the controller is not in Maintenance mode after any of the following conditions:

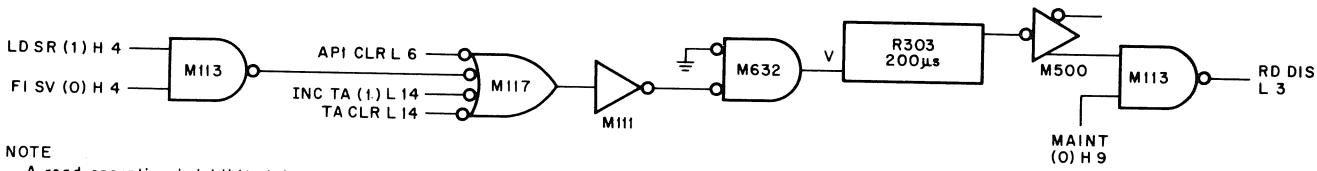
a. **The Track Address Register is incremented (INC TA (1) H 14).**

b. **The Track Address Register is cleared by an IOT.**

c. **A WRITE operation is performed.**

d. **The Disk Register is cleared.**

The 200 μs is necessary to give the Disk Data Amplifiers time to settle for a READ. In all cases, they are either reselected or going from WRITE to READ mode.



NOTE
A read operation is inhibited from starting for 200μs when the controller is not in maintenance mode after any of the following conditions :

a. The Track Address Register is incremented (INC TA (1) H14).
b. The Track Address Register is cleared by an IOT.
c. A WRITE operation is performed.
d. The Disk Register is cleared.

The 200μs is necessary to give the disk data amplifiers time to settle for a READ. In all cases, they are either reselected or going from WRITE to READ mode.

09-0372

Figure 4-37 Read Disable Logic

4.3.8 The Gap

Before and after the gap, there is an area where the A track timing pulses are present, but no address or C track data is present. In these dormant areas, the controller does nothing because no valid address is decoded. In the gap proper, however, the A timing track stops. This causes DISK RUN to clear and the TA Register to increment. The Disk Address Register increments when the TA Register overflows and sets INC DA. When the A track returns, either because the present disk reached the end of the gap or a new disk is selected, DISK RUN sets, provided the disk control is still BUSY. DISK RUN resets INC DA in preparation for the next TA Register overflow.

4.3.9 The Maintenance Logic

Engineering Drawing D-BS-RF09-0-09 shows the logic that has been designed into the controller specifically for maintenance purposes. There are two distinct sections shown; the first section, which is made up of the four flip-flops MAT, MBT, MCT, and MDT, is used to simulate the signals coming from the heads of the disk surface. Three of the flip-flops are complemented (when the AC bit is a 1) under IOT command, and the MAT is toggled by the IOT. Their outputs are cabled to the input cable of the disk head. (The special cable used is a head simulator

cable. For more details on how to perform this operation, refer to the maintenance section description in Chapter 7.) The second maintenance logic section is used to simulate the complete RS09 unit. Under IOT command, the output pulses from the RS09 can be generated from the accumulator using the AND gates of this logic. The flip-flop MAINT is set each time a maintenance IOT is issued, and it is reset by a clear IOT. MAINT disables the error-detecting signal circuitry and ATOK (which would ordinarily prevent the controller from functioning because, under IOT command, the A track signals cannot be generated quickly enough). Chapter 1 lists the maintenance IOT instructions.

Chapter 5
Field Installation

5.1 INSTALLATION LOCATION

Limitations on the length of the I/O bus generally require that the DECdisk system be located in the same room as the computer. Engineering Drawing D-AR-RF09-0-37 illustrates various DECdisk system configurations. Weights, dimensions, and service clearances are listed in Table 5-1 and Figure 5-1. Special attention should be paid to access routes (such as the size of doors, elevators, and passage ways) to be used when the system is delivered. Any special packaging requirements should be communicated to the DEC Special Systems Group when the system is ordered.

Cables should be as short as possible and protected from damage. Low frequency vibration (such as that caused by a hand forklift truck operating on a wooden floor) can cause data errors. The DECdisk system is not designed to operate in aircraft, trucks, or ships.

5.2 ENVIRONMENTAL CONSIDERATIONS

The DECdisk system is designed to operate in a temperature range from 65°F (18°C) to 90°F (35°C) at a relative humidity of 10 percent to 55 percent with no condensation. The air should be free of dust and corrosive pollutants, and the air pressure should be kept higher than that of adjacent areas to prevent dust infiltration. If air-conditioning is required, the size of the unit requirement can be calculated from the heat dissipation figures listed in Table 5-1. Computer room air-conditioning should conform to the requirements of the "Standard for the Installation of Air-Conditioning and Ventilation Systems (nonresidential) N.F.P.A. No. 90A"; as well as to the requirements of the "Standard for Electronic Computer Systems N.F.P.A. No. 75."

5.3 PRIMARY POWER REQUIREMENTS

The DECdisk system can be operated from either 115 or 230 Vac single-phase, 50 or 60 Hz power. Line voltages must be maintained to within ±10 Vac, and the line frequency should not drift more than .1 Hz/sec. A constant frequency should be provided for installations with unstable power supplies.

Table 5-1 shows the power required for various configurations. The primary power line must terminate in Hubbell wall receptacles (shown in Figure 5-2), or their equivalent, to be compatible with the DECdisk power line Hubbell connector.

The PDP-9 cabinet should be grounded to the building power transformer ground or the building ground point.

Duplex ac-outlets should be provided to power test equipment. The outlets should be close to the equipment, separately fused, switch-controlled, and rated at 115 or 230 Vac, 15 or 20A.

Table 5-1
Statistics for DECdisk Installations

Configuration (Number of Disks)	Number of Cabinets	Current (115 Vac)		Dissipation		Total Weight (lb)	
		Start (Amperes)	Run (Amperes)	Heat (BTU/HR)	Power (KW)	Crated	Uncrated
1	1	14.0	6.5	2550	.75	590	500
2	1	23.0	8.0	3140	.92	690	600
3	2	33.5	11.0	4310	1.27	1090	1000
4	2	42.5	12.5	4900	1.44	1190	1100
5	2	52.0	14.5	5690	1.75	1290	1200
6	3	62.5	17.5	6860	1.01	1690	1600
7	3	71.5	19.0	7450	2.18	1790	1700
8	3	81.0	21.0	8230	2.42	1890	1800

NOTES:
1. Cabinets are 30 in. x 21-11/16 in. x 71-7/16 in. All cabinets of the DECdisk system are shipped singly or bolted together in pairs (unless otherwise specified). These cabinets cannot be bolted to the PDP-9.
2. Disks should not be turned on simultaneously, or the circuit breaker may trip. Approximately 20 sec should be allowed before each successive disk is turned on.
3. Floor Loading = weight of cabinet/1 in.^{2}, since each caster covers approximately 1/4 in.^{2} of floor space.

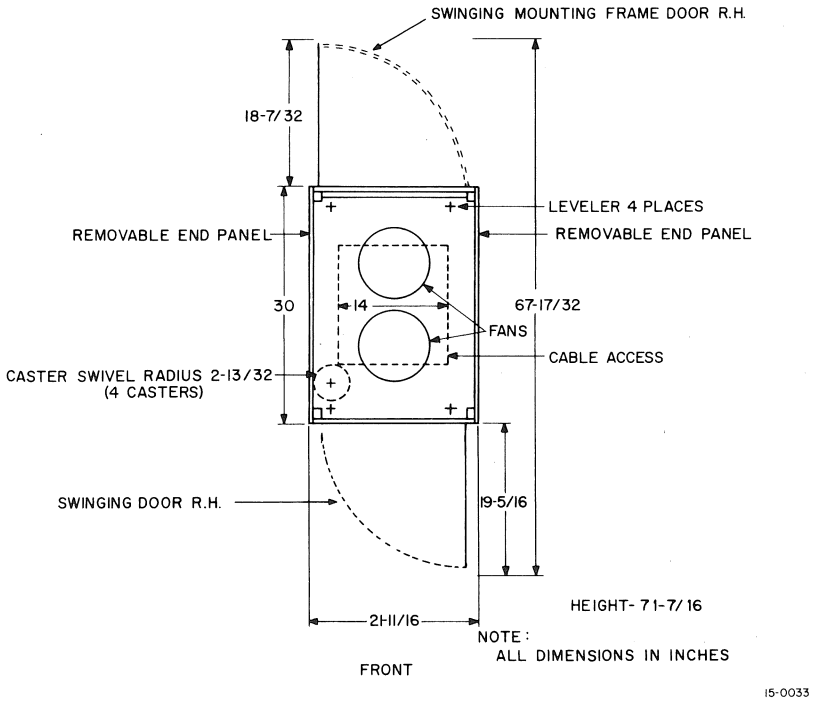
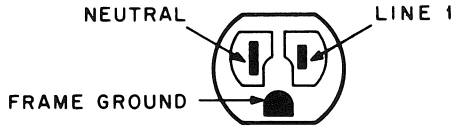


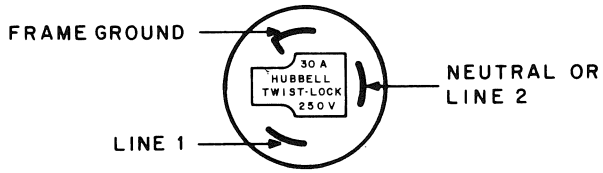
Figure 5-1 The RF09 Cabinet

SERVICE OUTLET
120V 60Hz SINGLE PHASE
15A/U GND

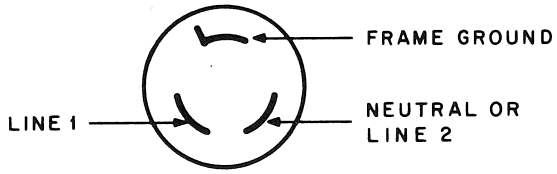


CAUTION

When neutral is not available for the above service, a receptacle of the above design shall be used, but both parallel slots shall be short to prevent polarized parallel blade plugs (caps) from fitting.



RECEPTACLE No. 3330-G
CAP No. 3331-G
115V 60Hz SINGLE PHASE
30A TWIST-LOCK



RECEPTACLE No. 7310-G
CAP No. 3321-G
230V 50Hz SINGLE PHASE
20A TWIST-LOCK

09-0414

Figure 5-2 Hubbell Wall Receptacle Connector Diagram

5.4 ACCESSORIES

If carpeting is installed in the computer room, it should be designed to minimize static electricity and resist fire.

5.5 UNPACKING AND INSTALLATION

The equipment may arrive either as a complete system (with controller, disks and power supplies mounted in their appropriate cabinet), or as an add on (with disk drives to be mounted in cabinets already available at the site).

5.5.1 Cabinet Unpacking

If the equipment arrives in cabinets, the following procedure should be followed to unpack and position them.

Step	Procedure
1	Remove the outer shipping container, which may be either heavy corrugated cardboard or plywood. Remove all straps first, and then any fasteners and cleats securing the container to the skid. Remove any wood framing and supports.
2	Remove the Polyethylene covers from all cabinets.
3	Remove the tape or plastic shipping pins from the rear access doors.
4	Unbolt the cabinets from their shipping skids. The bolts can be reached through the rear doors.
5	Raise the leveling feet so that they are above the level of the roll-around casters.
6	Form a ramp with wooden blocks and planks from each cabinet skid to the floor, and roll each cabinet down this ramp.
7	Roll the system to its proper location.

5.5.2 Cabinet Installation

The DECdisk cabinets are equipped with roll-around casters and adjustable leveling feet. They do not have to be bolted to the floor. In multiple cabinet installations, cabinets are shipped either individually or in pairs. DECdisk cabinets should be connected together at the site, but they cannot be bolted to any PDP-9 cabinets because the two cabinet types are not compatible. To install the cabinets, the following procedure should be used.

Step	Procedure
1	Cabinets are joined by filler strips (see Figure 5-3). After the cabinets are positioned, put the cabinets together and bolt both filler strips and cabinets together. Do not tighten the bolts securely.
2	Lower the leveling feet until they support the cabinet. Using a spirit level, check that all cabinets are level and that the feet are firmly against the floor.
3	Tighten the bolts that hold the cabinets together and again check the leveling.
4	Remove the shipping bolts and tape from the slide runners of each disk drive.
5	Run a ground strap from the DECdisk cabinets to the PDP-9 cabinet.

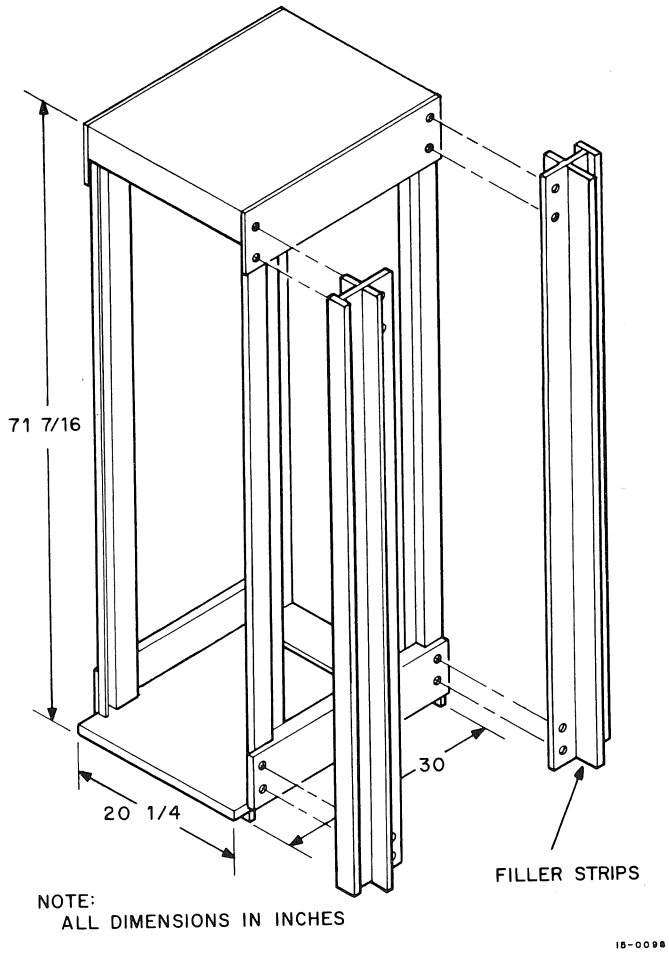


Figure 5-3 Cabinet Bolting Diagram

5.5.3 RF09 Controller Installation

The controller shown in Figure 5-4 comes mounted in a cabinet (No. 1) with at least one disk. Three steps must be followed to install it.

Step	Procedure
1	Remove any tape from the modules and check that existing wiring is not damaged, that hold down bars are in place, and that no modules have fallen out.
2	Install the I/O bus cables in accordance with Figure 5-5.
3	Connect the ac remote turn-on cable between the computer and the 855 power control unit at the back of the cabinet (see Figure 5-6). Check that the line voltage is correct and that the transformer has been properly wired. (Refer to Engineering Drawing D-IC-RF09-0-35.) Note that on 220V systems only the 705B and the optional transformer must be wired for 220V. All other accessories are already wired for 115V. Make sure that the circuit breaker is OFF on the power control, and then plug the primary power cable into the line voltage receptacle.

5.5.4 RS09 Unpacking

When the RS09 is shipped as an addition to an already installed system, it must be unpacked at the site and installed in its prelocated cabinet. The procedure for RS09 unpacking is as follows:

Step	Procedure
1	Turn off the system and the 855 circuit breaker.
2	Remove the disks from their shipping containers and identify each according to its tag number.
3	Carefully install each disk into its proper position in the cabinet according to Engineering Drawing D-AR-RF09-0-37. Cables should be placed toward the front of the cabinet.
4	Install the disk cable bus according to Figure 5-5.

5.5.5 RS09 Installation

It is assumed at this point that the disks have been installed into their cabinets either at the site or in the factory. For each new disk, perform the following procedures (see Figures 5-6 and 5-7):

Step	Procedure
1	Remove the silver cloth tape from the pan containing desiccant (Drierite) and remove the pan from the motor.
2	Unwrap the blue, green, yellow, red, and black motor leads from the motor.
3	Connect these wires to the proper color-coded connections on the back of the RS09 motor control chassis.
4	Remove the motor lock and hold down the bracket.

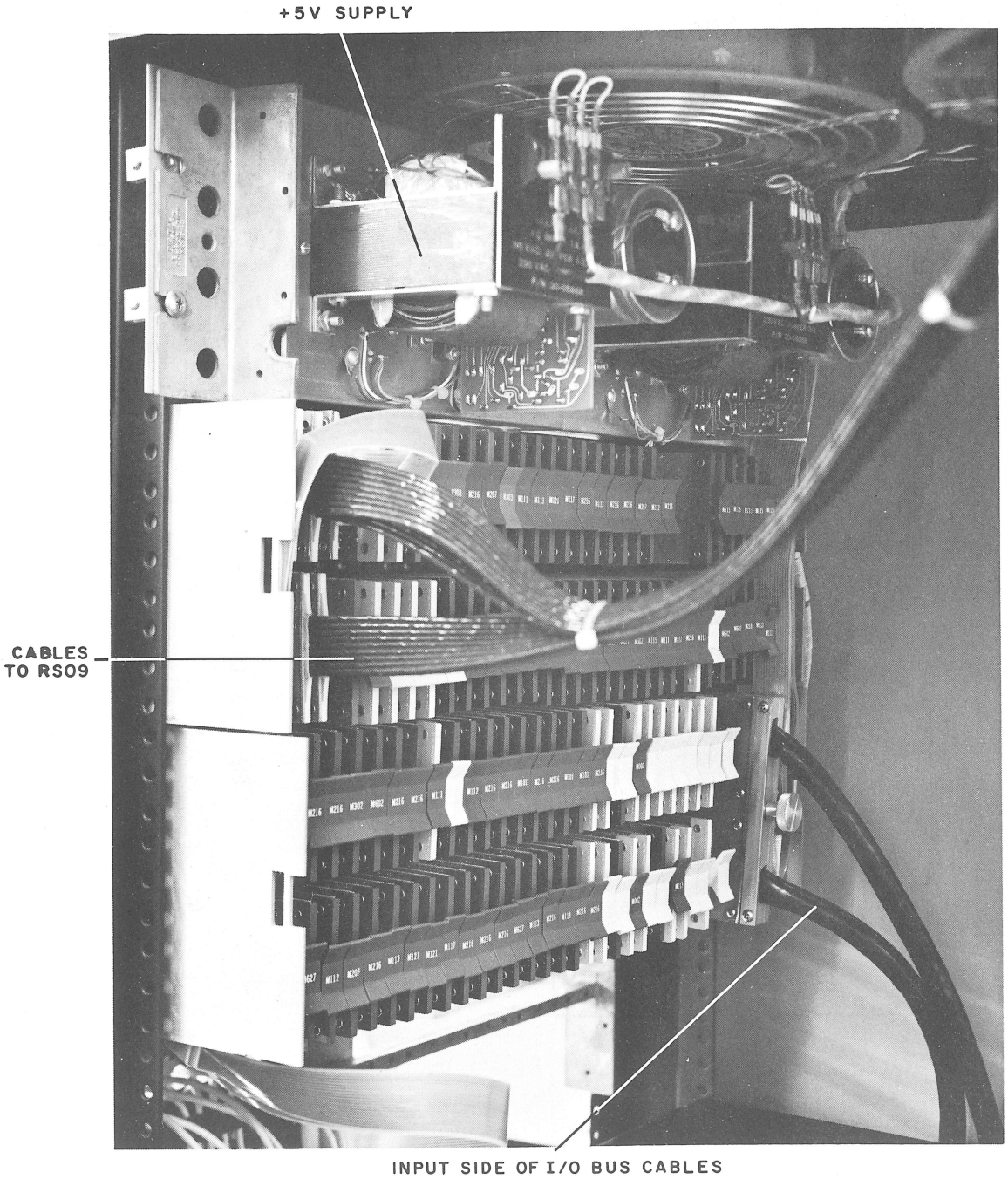


Figure 5-4 The RS09 Electronics

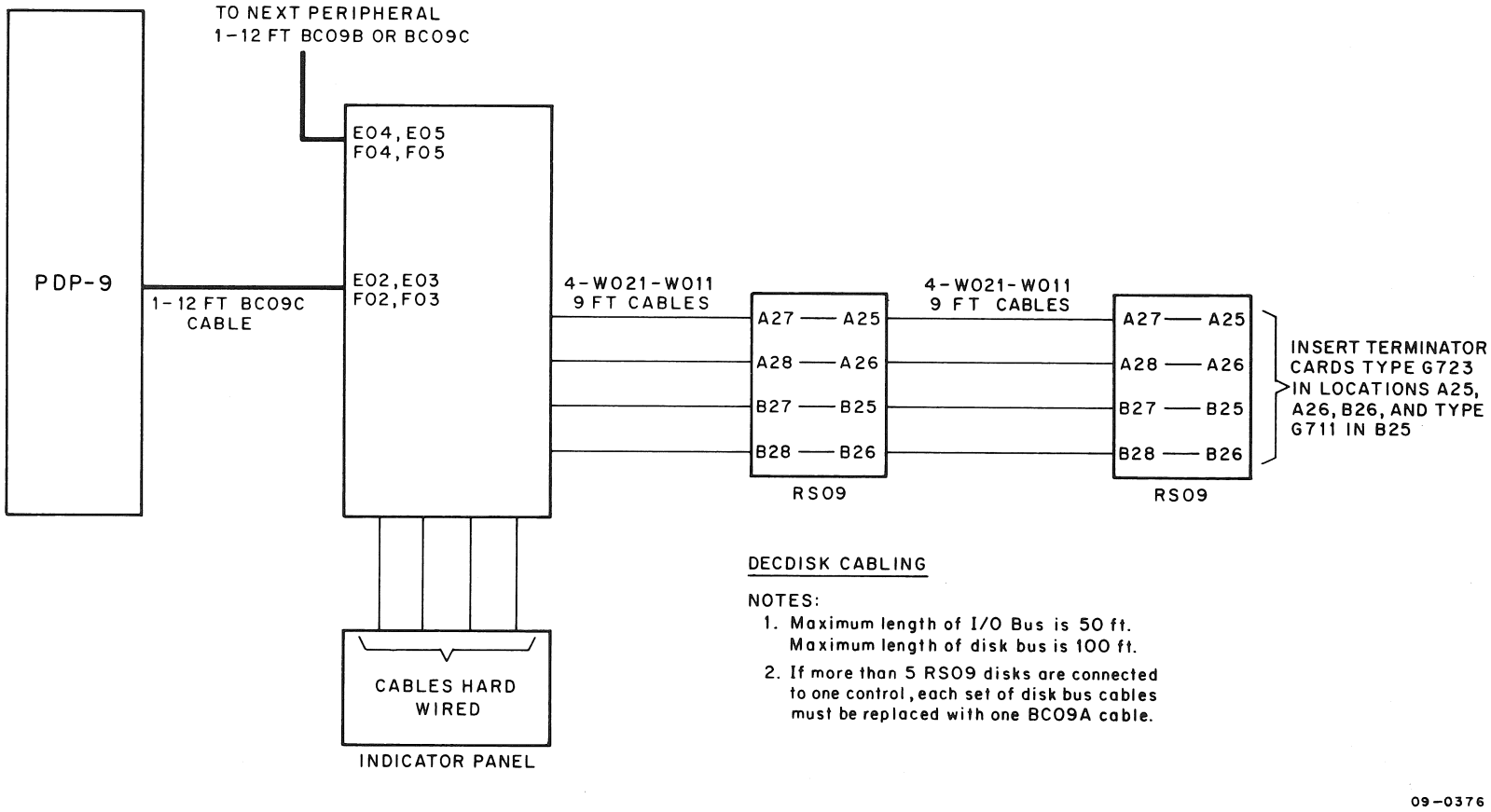


Figure 5-5 DECdisk Cabling

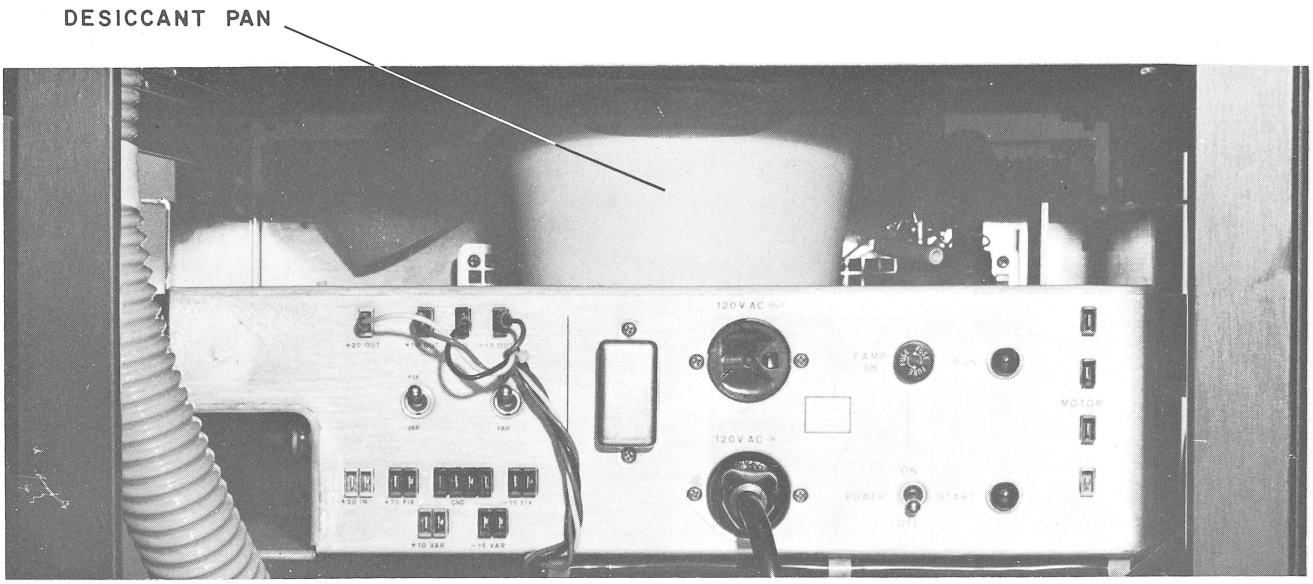


Figure 5-6 The Disk Assembly with Desiccant Pan

Step	Procedure
5	Turn the motor switches on the back of the RS09 motor control chassis to the OFF position.
6	Ensure that the circuit breaker on the 855 Power Control is OFF and that the LOCAL, OFF, REMOTE switch is in the OFF position.
7	Connect the ac- and dc-power wiring in accordance with Engineering Drawing D-IC-RF09-0-35.
8	Switch the 855 Power Control circuit breaker to On. (At this point, the hose on the purge unit has not been connected.) Thus, the purge unit itself is purged, and should continue to be purged for at least 30 min. The disk motor must be off at this time.
9	After the 30 min. purge period, remove the cap from the disk unit and connect the purge unit's hose in the cap's place.

5.6 POWER-UP SEQUENCE

Before starting the power-up sequence, all wiring should be double checked, the primary ac-power source should be tested for the correct voltage, and the positions of all relevant controls verified. The sequence to be followed to power-up the DECdisk system is as follows:

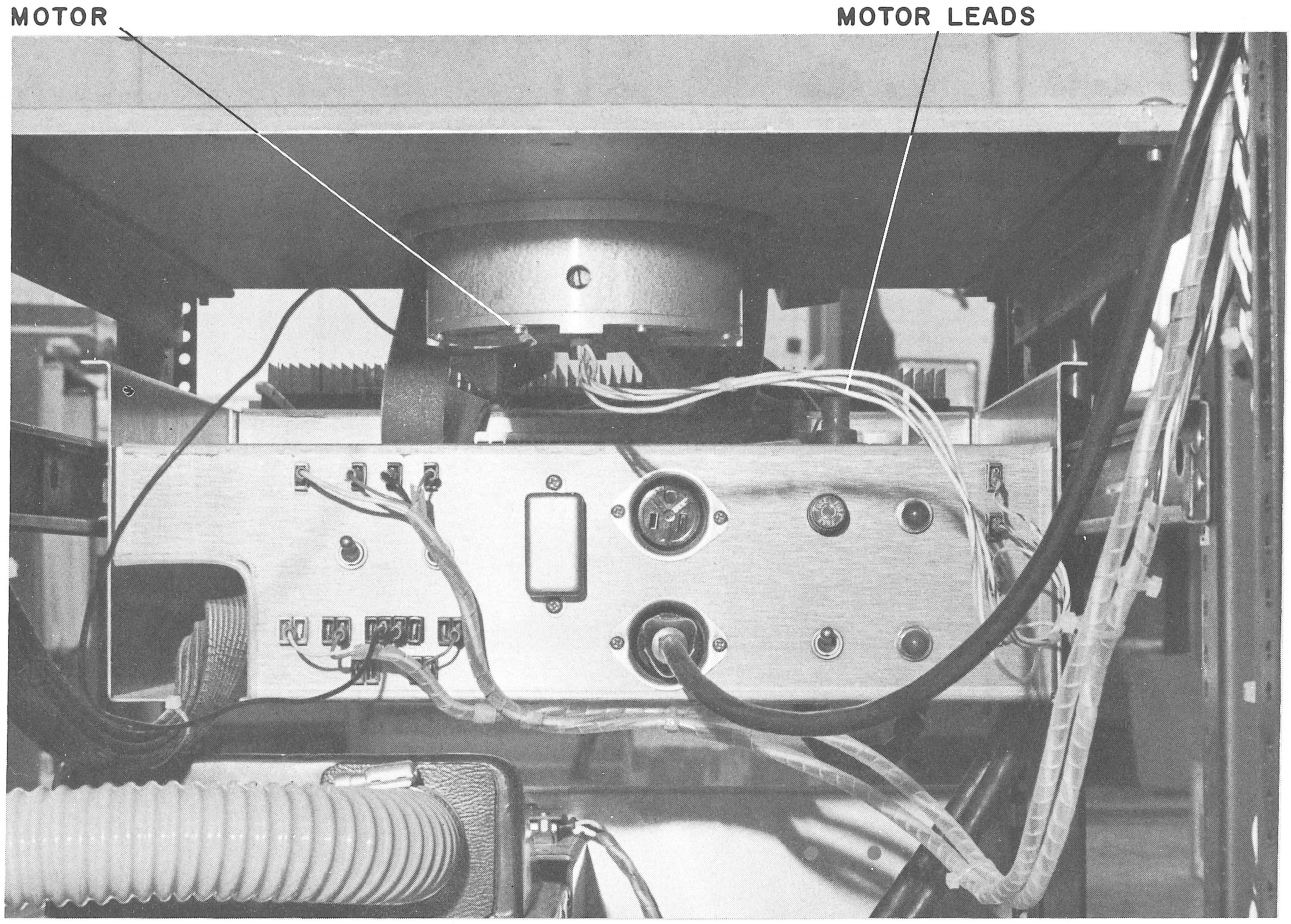


Figure 5-7 Disk Assembly with Pan Removed and Motor Leads Connected

Step	Procedure
1	Turn off the 855 circuit breaker and all power switches on the Disk Control chassis. Turn the REMOTE switch to OFF. Plug in the 855 power cord and turn on the circuit breaker.
2	Turn the DISK POWER switch of the first disk ON. The START and OPERATE lights should illuminate. The START light should extinguish in approximately 20 sec; until it does, the disk is inoperable.
3	Check that the disk is running and the blower is operating. If any unusual noises are heard, turn off the disk immediately and notify the local DEC office that depot repair is necessary.
4	Repeat this sequence for each disk. Do not turn on all disks simultaneously, or the surge current may trigger the circuit breaker. Do not attempt to use one disk while turning on another; noise transients can cause interference between disks during turn on.
5	Turn the REMOTE switch to REMOTE.

5.7 ACCEPTANCE PROCEDURE

The following paragraphs describe customer acceptance procedures after the DECdisk system is installed and operating properly.

5.7.1 Acceptance Forms

After the system is properly installed, successful operation is demonstrated to the customer by running diagnostics and the system software. Three forms contained in the accessory kit are used during the customer acceptance procedure. These forms are:

a. The Customer Acceptance Form, in which is recorded any exceptions to normal operation found in the system during the acceptance procedure. Such items should include missing parts, manuals, or engineering drawings.

b. The Software Checklist, which catalogues all software that is normally supplied with the system. Each item should be checked off by the customer and the DEC Field Representative.

c. The Accessory Checklist, which catalogues all of the hardware items normally supplied with the system. Each item should be checked off by the customer and the DEC Field Representative.

d. RS09 Data Sheets, which supply further information for the DEC Field Service Engineer.

5.7.2 Diagnostics

Three diagnostics are run. They are:

a. Disk Data (MAINDEC-09-D5AA), which is a series of address and data reliability routines that verify to the user correct operation of the control and disk.

b. Multi Disk (MAINDEC-09-D5BA), which is a high speed confidence test that operates in two modes. In the first mode (SAVE MODE), the disk tested is restored to its original state after it is exercised with random data. In the second mode, the original data on the disk is destroyed.

c. Diskless (MAINDEC-09-D5CA), Part I; which checks-out the RF09 logic in detail. The diagnostic requires several minor hardware changes that are described in the diagnostic writeup.

5.7.3 System Software

The system is operated using the checkout procedure in the Advanced Software System Checkout Package for Bulk Storage Systems. If the computer system has DECtape, this package includes a complete set of advanced software manuals, a DECtape monitor for RF09 bulk storage, and peripheral routines for bulk storage on DECtape. If the computer system does not have DECtape, the package then consists of a complete papertape advanced software system and a complete set of advanced software manuals.

The successful demonstration of both the diagnostics and the system software constitutes the acceptance procedure. Any discrepancies found must be listed in the Customer Acceptance Form.

5.8 SHIPPING

If a DECdisk System is to be shipped from one point to another (as a complete unit or in parts), it should be prepared and packed according to the packing instructions of Engineering Drawings PI 3700006 and PI 3700014.

Chapter 6
Organizational Maintenance

Organizational or first level maintenance refers to maintenance that can be performed on the equipment at the site without using special test equipment. Organizational maintenance is subdivided into three areas: preventive maintenance; adjustment procedures; and diagnostics.

6.1 PREVENTIVE MAINTENANCE

Preventive maintenance includes visual inspection of the DECdisk system according to the list in Table 6-1, and performance of the maintenance tasks listed below.

a. The prefilter of the purge unit must be removed and cleaned once each month. The prefilter part number is 7407181 (see Figure 6-1).

b. The absolute filter of the purge unit must be replaced every six months. The absolute-filter part number is 12-09388 (see Figure 6-1).

Table 6-1
Visual Inspection Checklist

Item	Check
Mechanical Connections	*a.* Check that all screws are tight and that all mechanical assemblies are secure. *b.* Check that all crimped lugs are secure and that all lugs are properly inserted in their mating connectors.
Wiring and Cables	*a.* Check all wiring and cables for breaks, cuts, frayed leads, or missing lugs. Check wire wraps for broken or missing pins. *b.* Check that no wire or cables are strained in their normal positions or have severe kinks. Check that cables do not interfere with doors, and that they do not chafe when doors are opened and closed.
Air Filters	Check all air filters for cleanliness and for normal air movement through cabinets. Check the purge unit and purge hose for cracks.

Table 6-1 (Cont)
Visual Inspection Checklist

Item	Check
Modules and Components	Check that all modules are properly seated. Look for areas of discoloration on all exposed surfaces. Check all exposed capacitors for signs of discoloration, leakage, or corrosion. Check power supply capacitors for bulges.
Indicators and Switches	Check all indicators and switches for tightness. Check for cracks, discoloration, or other visual defects.

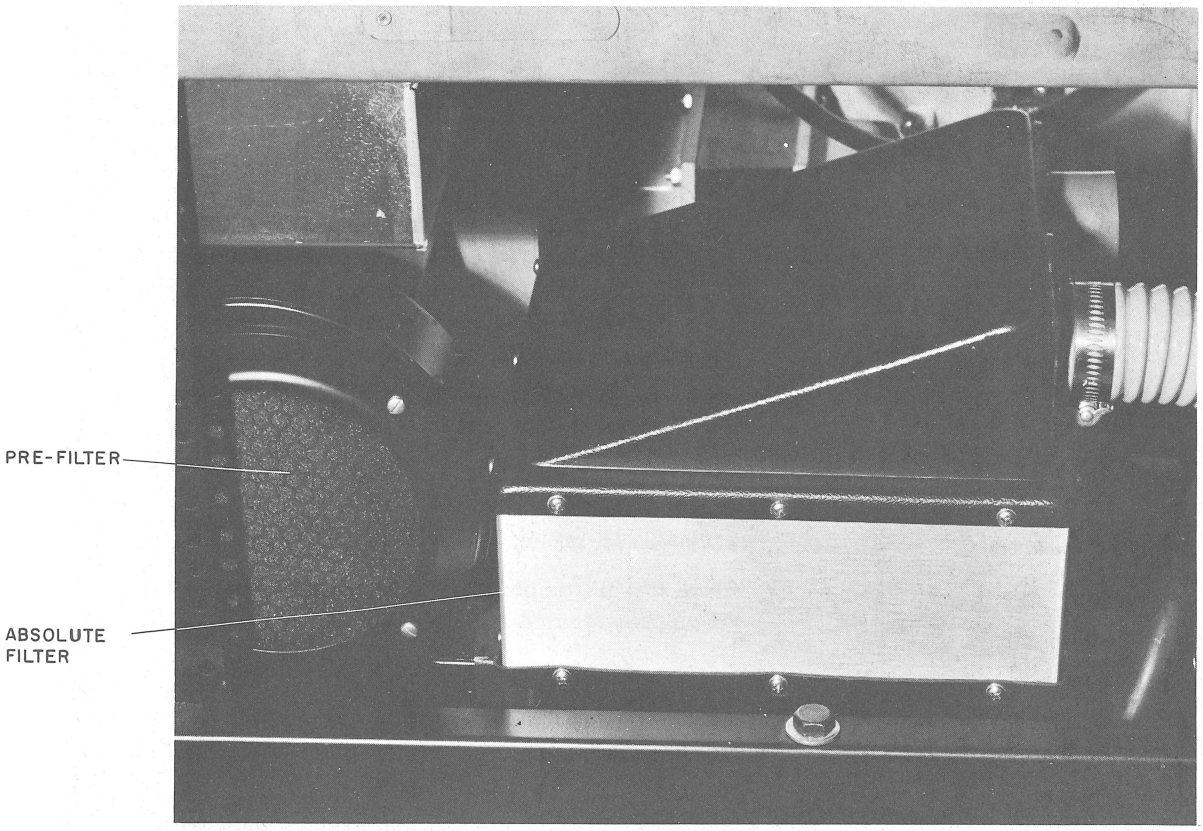


Figure 6-1 Purge Unit and Filters

6.2 RS09 ADJUSTMENTS

Organizational level adjustment procedures on the RS09 include calibrating the five G085 read amplifiers for gain and slice. (The output voltage of each G085 for the three timing tracks should be an average of 6V peak-to-peak, and the slice level for all readers should be 1.1V.)

6.2.1 Measuring the Gain

The output of a properly calibrated reader varies around the track because of variations in the surface. Figure 6-2 shows the output for a complete revolution from an A track. The gain is calculated by estimating the average voltage around the track. This is done by measuring the peak-to-peak voltage at the lowest point and the highest point, adding the measurements together, and dividing by two.

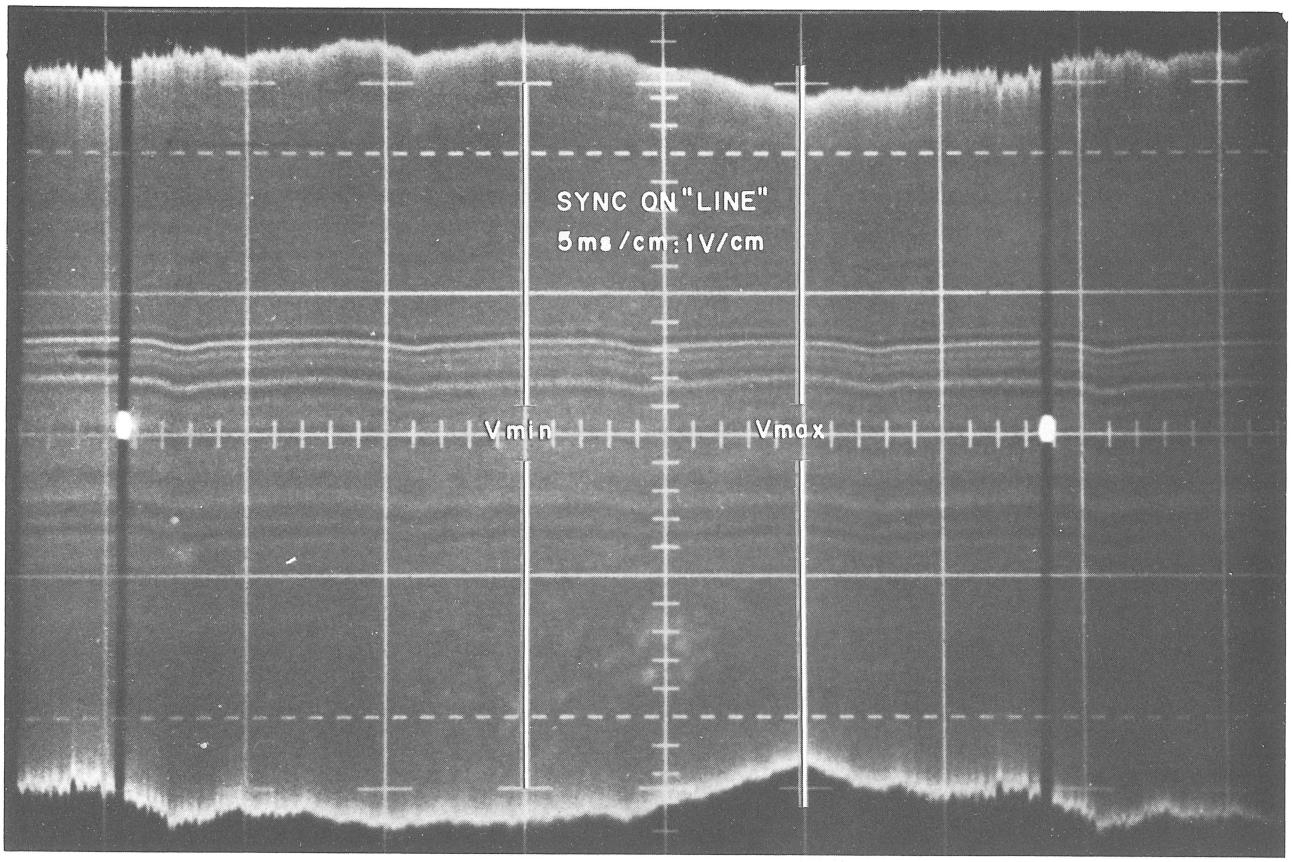


Figure 6-2 Measuring Gain, The A Track Over One Revolution

6.2.2 Measuring the Slice

The slice level for all readers should be set at 1.1V. To measure slice, set up the oscilloscope as shown in Figure 6-3. The output of the amplifier is added to the output of the slice. The two peaks of the resultant waveform are averaged after the slice overshoot is subtracted, and the reuslt is the slice level.

The equation to calculate slice is

$$\frac{A + B - \text{Overshoot}}{2}$$, which must be = 1.1V.

To establish the zero crossing, locate the gap and set the zero line on the trace as it passes through the gap as shown in Figure 6-2. Increase the trace frequency until the waveform of Figure 6-3 is displayed.

6-2.3 Calibrating the Read Amplifiers

This procedure uses a dual trace oscilloscope (such as the Tektronix 453). Pull the RS09 electronics out on its rack and remove the protective plate which covers the pins, as shown in Figure 6-6.

To calibrate the A Track, perform the following steps:

Step	Procedure
1	Place the first probe on location B02E and place the probe's ground strap on B02C.
2	Place the second probe on location A02T and place the probe's ground strap on B02C.
3	Set the average voltage to 6V peak-to-peak.
4	Set the slice to 1.1V. Waveforms are shown in Figure 6-3.

To calibrate the B Track, perform the following steps:

Step	Procedure
1	Place the first probe on location B03E and place the probe's ground strap on B03C.
2	Place the second probe on location A02T and place the probe's ground strap on B03C.
3	Set the average voltage to 6V peak-to-peak.
4	Set the slice to 1.1V. Waveforms are shown in Figure 6-4.

To calibrate the C Track, perform the following steps:

Step	Procedure
1	Place the first probe on location B04E and place the probe's ground strap on B04C.
2	Place the second probe on location A04T and place the probe's ground strap on B04C.
3	Set the average voltage to 6V peak-to-peak.
4	Set the slice to 1.1V. Waveforms are shown in Figure 6-5

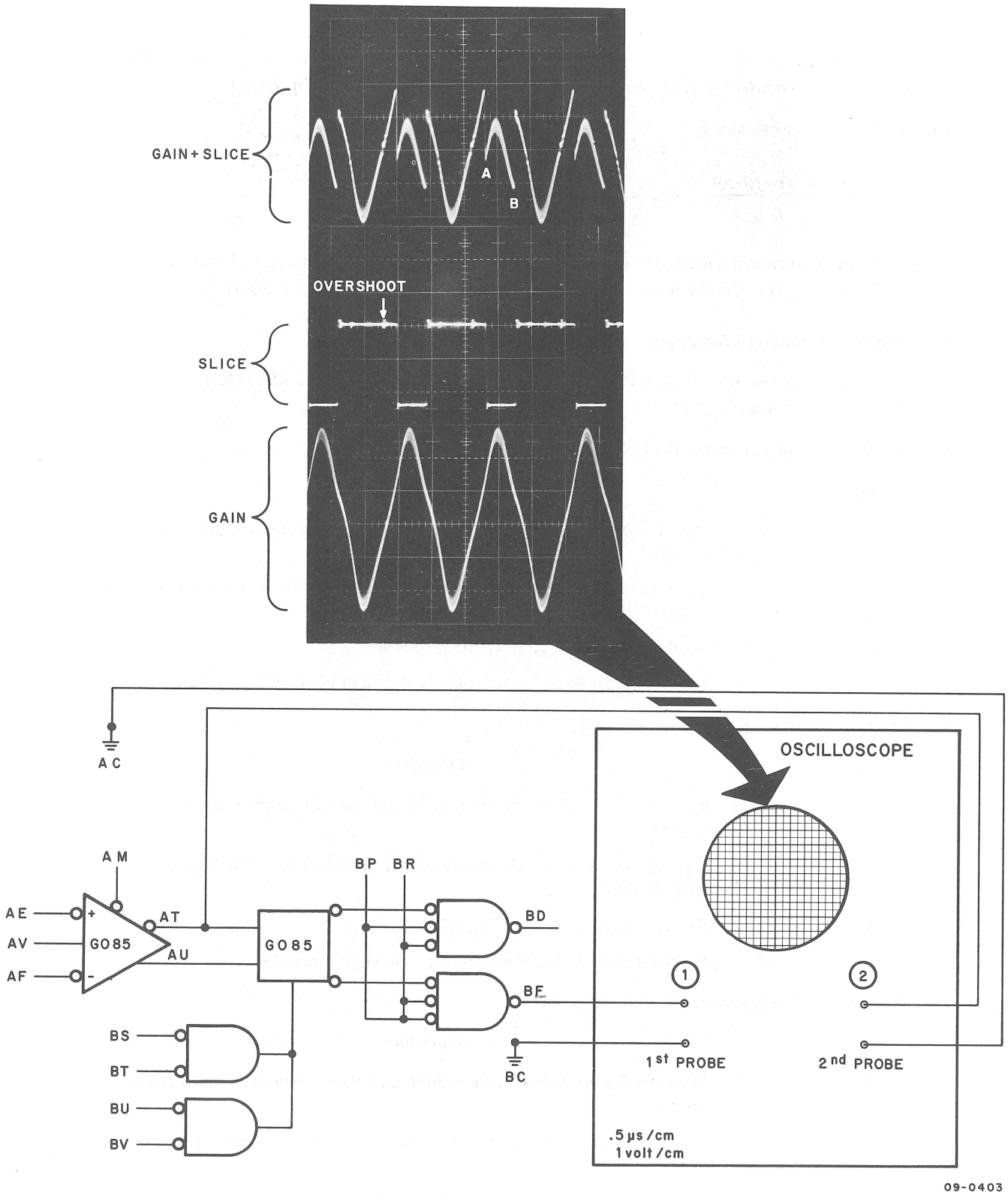


Figure 6-3 Measuring the Slice of the A Track

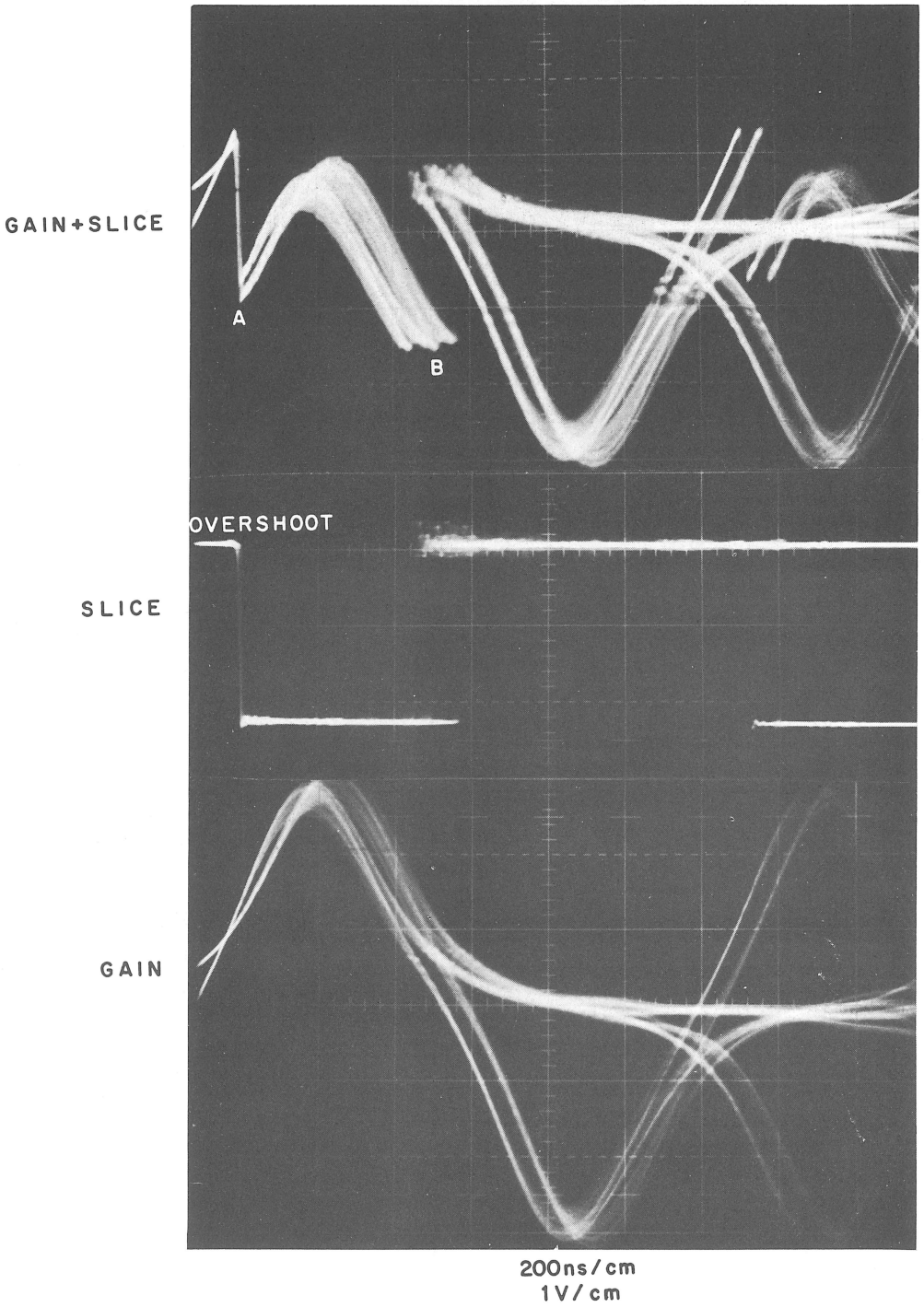


Figure 6-4 Measuring the Slice of the B Track

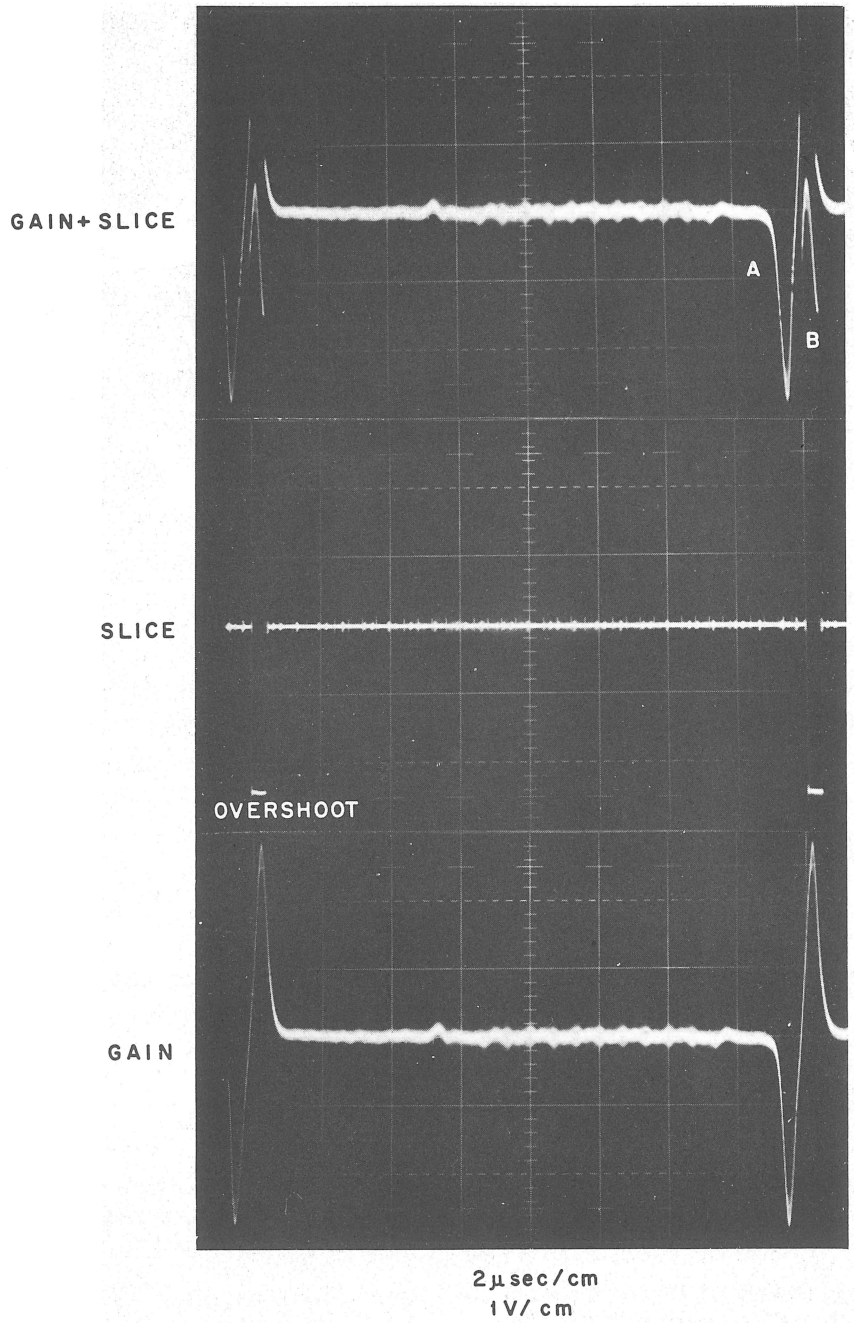


Figure 6-5 Measuring the Slice of the C Track

The Data Track Reader is calibrated from the average track of each matrix. The average output voltages per matrix and their gain are posted on the disk itself for these two tracks. (This information is also listed on the disk data sheets.) These tracks were selected at the factory, and their outputs were recorded when all 1s were written on the disk. The first step is to load the Disk Data program and write all 1s. The average track is then locked into, using the STAMP portion of Disk Data (starting address 171, push continue).

To calibrate the Data Tracks, use the following procedure:

Step	Procedure
1	Place the first probe on location B05E and place the probe's ground strap on B05C.
2	Place the second probe on location A05T and place the probe's ground strap on B05C.
3	Set the average voltage to the value indicated on the front of the disk.
4	Set the slice to 1.1V.
5	Repeat this process for the matrix 1 amplifier located at AB07.

6.2.4 Changing the Timing Tracks

An extra set of timing tracks is always recorded on the disk. This set is to be used if the first set is accidentally erased in the field. To bring the second set into operation, reverse the timing track head cable connector at the RS09 electronics, slot A01. (The gain settings on the A, B, and C Tracks should be recalibrated.) This procedure disconnects the damaged tracks and connects the spares. If the spares are also damaged, the timing tracks must both be rewritten, using the Timing Track Writer explained in Chapter 3 and used in Chapter 7.

A view of the RS09 electronics with posted data is shown in Figure 6-6.

6.3 DIAGNOSTICS

There are three programs that are run to verify that the system is operating properly or to locate faults. These programs are available from the program library, along with complete descriptions of how they are used. The programs are:

a. Disk Data (MAINDEC-09-05AA), which is a series of address tests and data reliability routines that verify for the user correct operation of the control and the disks.

b. Multi Disk (MAINDEC-09-05BA), which is a high-speed confidence test that exercises each disk with random data. It can operate in one of two modes: in SAVE MODE the original contents of the disk are restored after the exercise, and in the normal mode the original contents are destroyed.

c. DISKLESS Part I (MAINDEC-09-D5CA), which checks out the RF09 controller. The set-up instructions are given in the DISKLESS description with the procedure. Note that Part 2 is to be run by a qualified Field Service Engineer only.

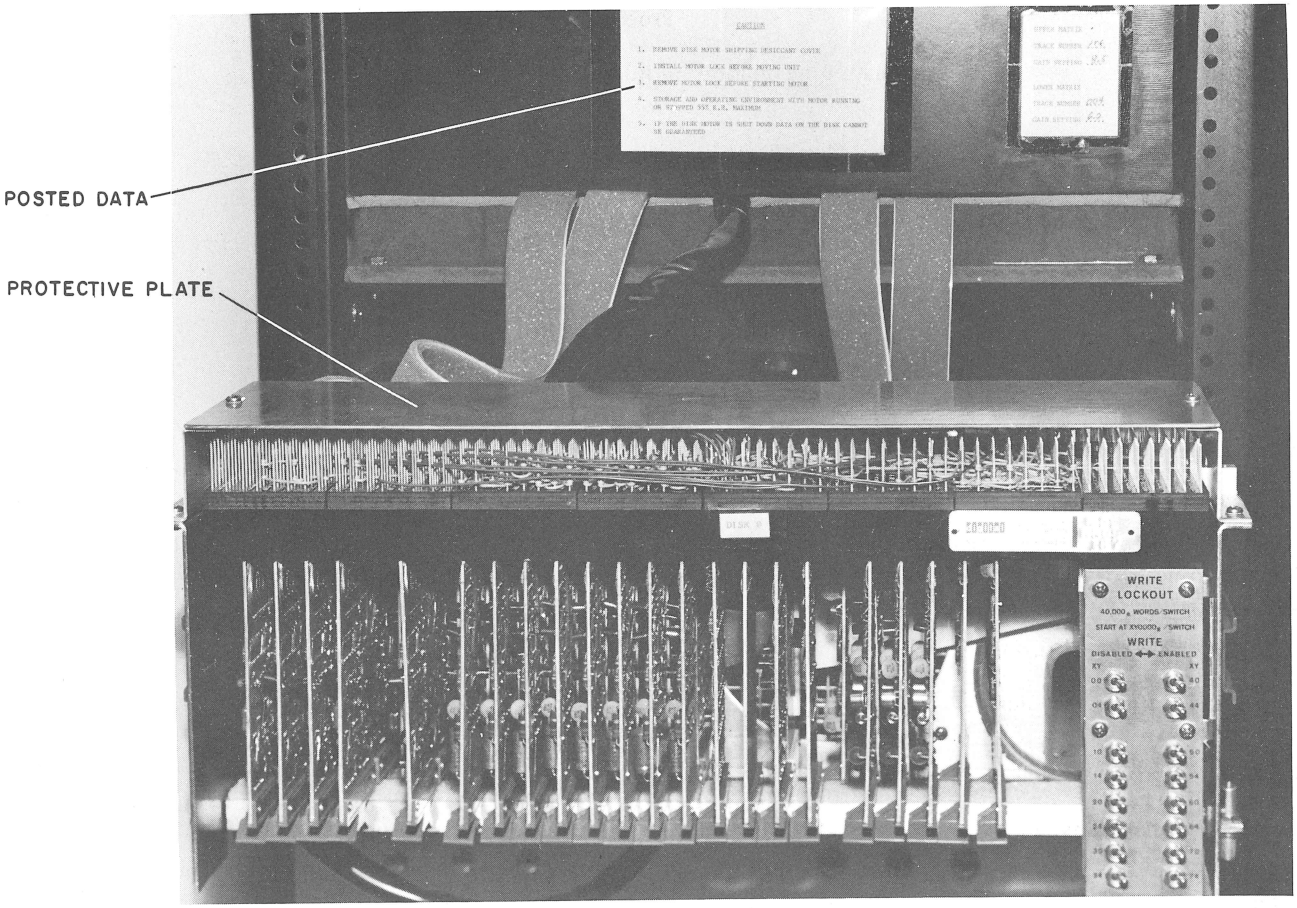


Figure 6-6 RS09 Electronics Showing Posted Data

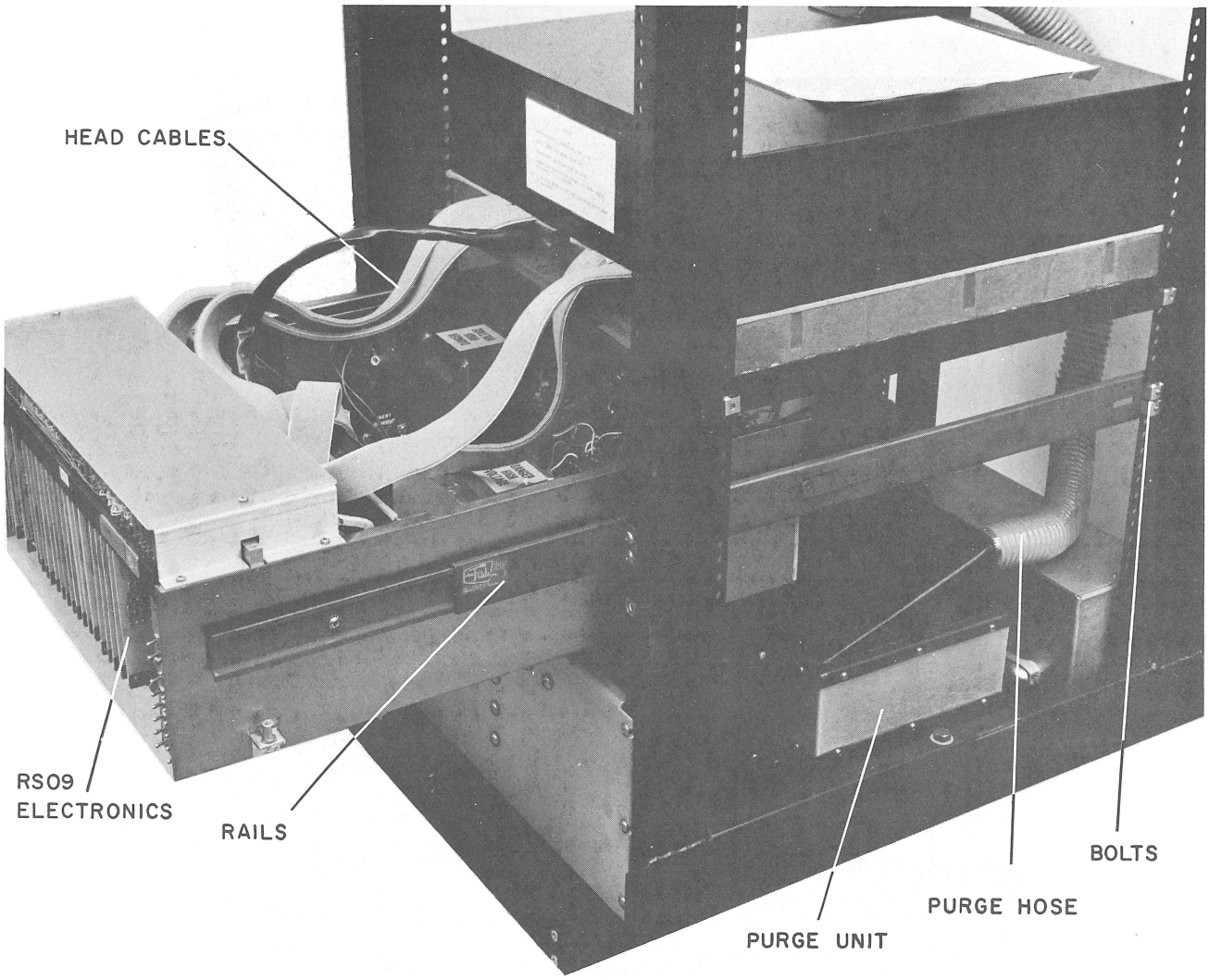


Figure 7-2 Removing the Disk Assembly from the Cabinet

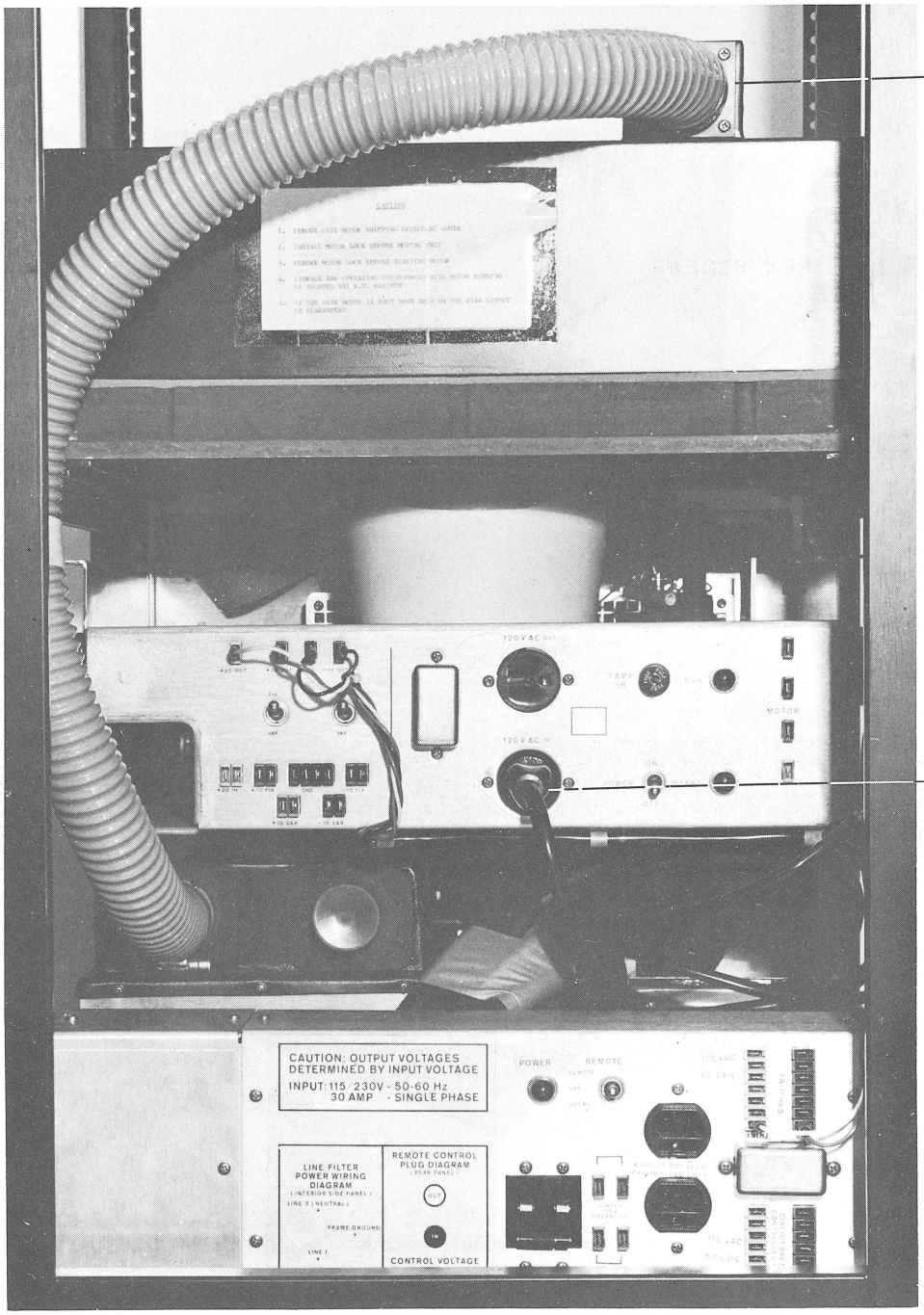


Figure 7-3 Disconnecting Motor Leads and Purge Hose

Chapter 7
Field Level Maintenance

Field or second level maintenance includes complex work performed on the equipment using special repair kits and diagnostics. This chapter is to be used by DEC Field Engineers. Only qualified DEC Field Engineers with the necessary special service equipment should attempt to perform the following procedures.

7.1 FIELD LEVEL RS09 AND RF09 MAINTENANCE

If problems occur in the RF09 or RS09 that cannot be solved using the methods of Chapter 6, the following checkout procedures should be followed. The primary tool for this checkout is the DISKLESS (MAINDEC-09-D5CA) diagnostic, which allows the Field Engineer to first test the RF09 alone, and then to test the RF09/RS09 combination. In both cases, the disk assembly itself is not used.

7.1.1 RF09 Off-Line Checkout Without the RS09

The following equipment is needed for this checkout:

a. 1 PDP-9 or PDP-9/L

b. 1 Tektronix 453 oscilloscope or equivalent.

c. 1 DISKLESS program complete with listings and writeup

d. 1 RF09

Perform the following steps:

Step	Procedure
1	Load the DISKLESS program, and then follow the set-up instructions.
2	Verify the delays in the controller by running the appropriate section of DISKLESS listed in Table 7-1, and observing on the oscilloscope the points indicated. Note that these delays are fixed. If they are outside the specification, the external component should then be checked.
3	Run Part 1 of DISKLESS. When the RF09 allows the program to sequence through all tests, the controller is ready to accept an RS09.

Table 7-1
Setting Up RF09 Delays

Delay	Program	Scope Points		Limits
		Sync Channel A	Check Channel B	
MXFR	Part 1 Test #23	C18B1	D20F2	130 ms ±20%
SEQ ERR	Part 1 Test #22	D13H2	D13F2	500 ns ±20%
A Test	Part 1 Test #22	C27N1	F28K1	5 μs ±20%
ATP Noise Suppressor	Part 1 Test #15	E30H2	E30F2	1.2 μs ±20%
ATN Noise Suppressor	Part 1 Test #15	E30M2	E30T2	1.2 μs ±20%
INh RD	I/O Reset Test	C18R2	D25C1	200 μs ±20%
INh RD	Part 1 Test #15	C18S2	D25C1	200 μs ±20%
INh RD	Part 1 Test #22	C18T2	D25C1	200 μs ±20%
INh RD	I/O Reset Test	C18U2	D25C1	200 μs ±20%
PSLER	Part 1 Test #7	D13M2	D13T2	1.5 ms ±20%

7.1.2 RF09 Off-Line Checkout with the RS09

A complete description of this procedure is given in Part 2 of the DISKLESS program. The equipment needed is:

a. 1 PDP-9 or PDP-9/L
b. 1 Tektronix 453 oscilloscope or equivalent
c. 1 DISKLESS program with listings and writeup
d. 1 RF09
e. 1 RS09
f. 1 Head Simulator cable
g. 1 M908 YA module

After the DISKLESS program sequences through Part 2 of the test, the RF09/RS09 combination is ready to accept the disk assembly.

7.2 FIELD LEVEL DISK ASSEMBLY REPAIRS

The RS08-M disk assembly is the most sensitive of the DECdisk units. The parts of the disk assembly usually requiring replacement are the shoes and the surface itself. A shoe can be damaged electrically (by a burned out diode or resistor on the G681B card) or mechanically (if the shoe crashes into the surface or breaks a lead from the head to its card). In either case, the assembly must be removed from its cabinet and disassembled.

The disk surface itself may be damaged electromagnetically (by stray fields or accidental currents through the heads from a multimeter, for example) or mechanically (by a crashing head). In the first case, the two sets of timing tracks may have to be rewritten with a portable timing track writer designed for this purpose. The assembly does not have to be disassembled for this procedure. The procedure is outlined in Paragraph 7.2.4. If the disk surface is damaged mechanically, the surface must be replaced. The assembly must be removed from its cabinet and taken apart. When a new disk is mounted (or even if the old disk is removed and remounted), the timing tracks must be rewritten with the timing track writer.

Each time a shoe or a surface is replaced, the system should be recalibrated following the procedures of Paragraph 7.3.

7.2.1 Removing the Disk Assembly

In order to gain access to the shoes or the disk surface, the disk assembly must be removed from its cabinet and dismantled on its mounting square. The kit shown in Figure 7-1 is provided for this purpose.

Turn off all power to the system and proceed as follows:

Step	Procedure
1	Pull the disk electronics out on its rack as shown in Figure 7-2.
2	Unplug the head cables from the RS09 electronics.
3	Unplug the purge hose and the motor power leads shown in Figure 7-3.
4	Remove the four bolts that hold the assembly to its rails.
5	Pull the disk out of its cabinet and mount it on the mounting square found in the kit.
6	Remove the twelve mounting screws that hold the cover on. Note that these screws are found along the sides of the assembly. On some disk-assembly versions there are four more screws in each corner that holds the shock mounts in place. Do not remove these screws.
7	Remove the cover (see Figure 7-4). The cards which hold the shoes are now accessable as shown in Figure 7-5. Be careful not to contaminate the heads or the disk surface itself.

7.2.2 Removing the Disk Surface

To remove the disk surface, perform the following steps:

Step	Procedure
1	Dismantle the assembly, following the instructions of Paragraph 7.2.1.
	CAUTION **Do not turn the disk clockwise while it is in contact with the heads.**
2	Remove the four hex screws on the disk hub (see Figure 7-4).

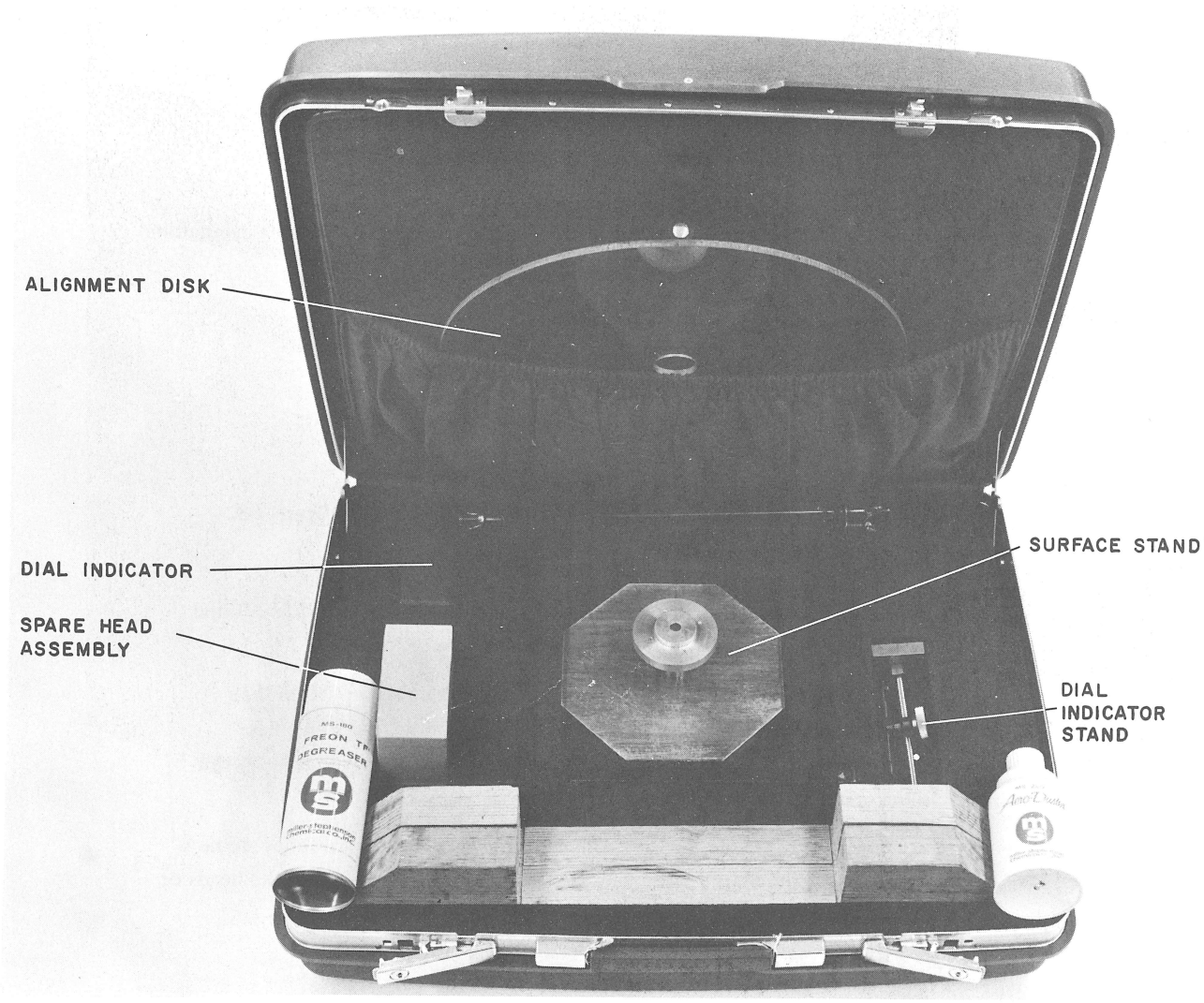


Figure 7-1 Disk Assembly Dismantling Kit

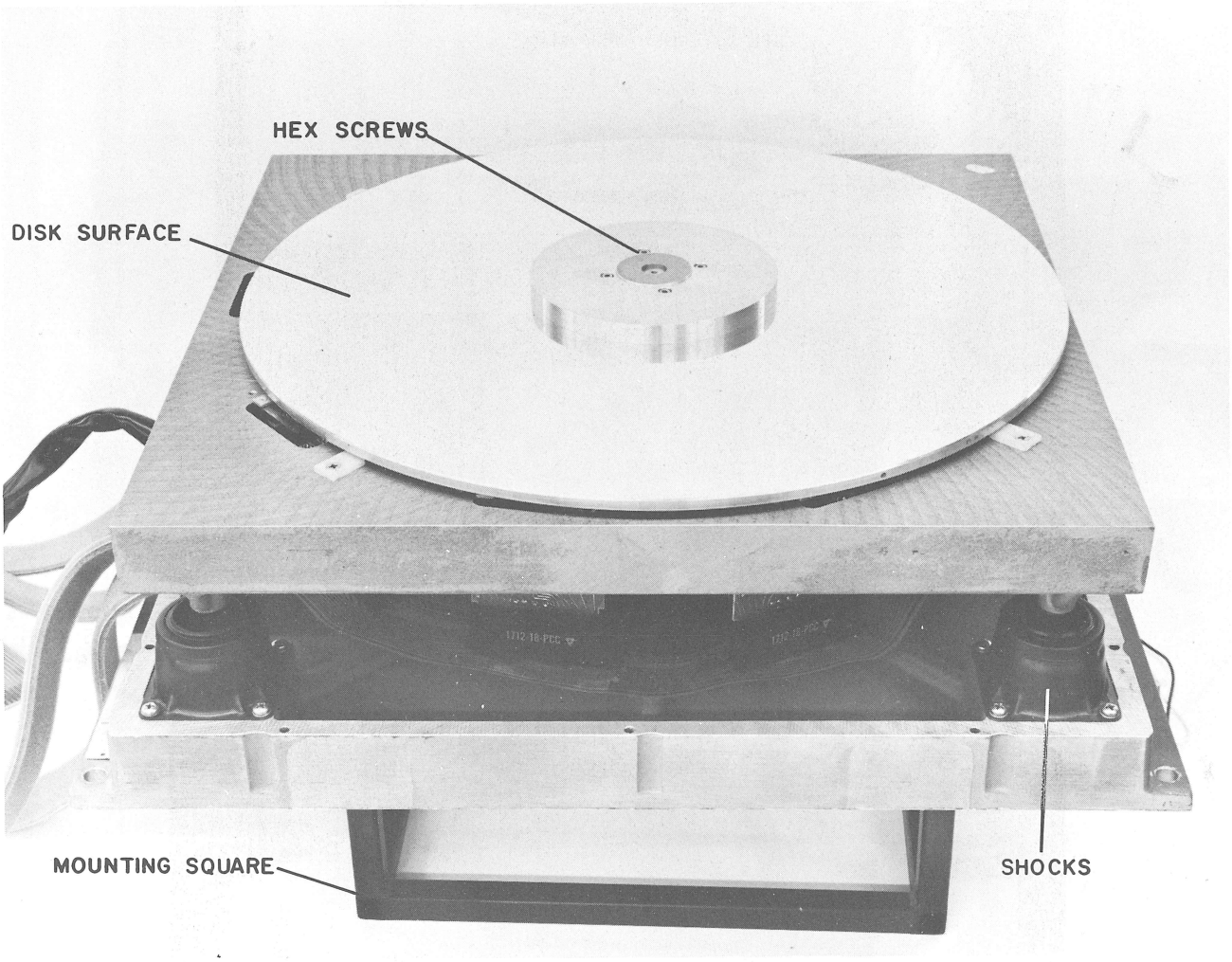


Figure 7-4 Disk Assembly With Cover Removed

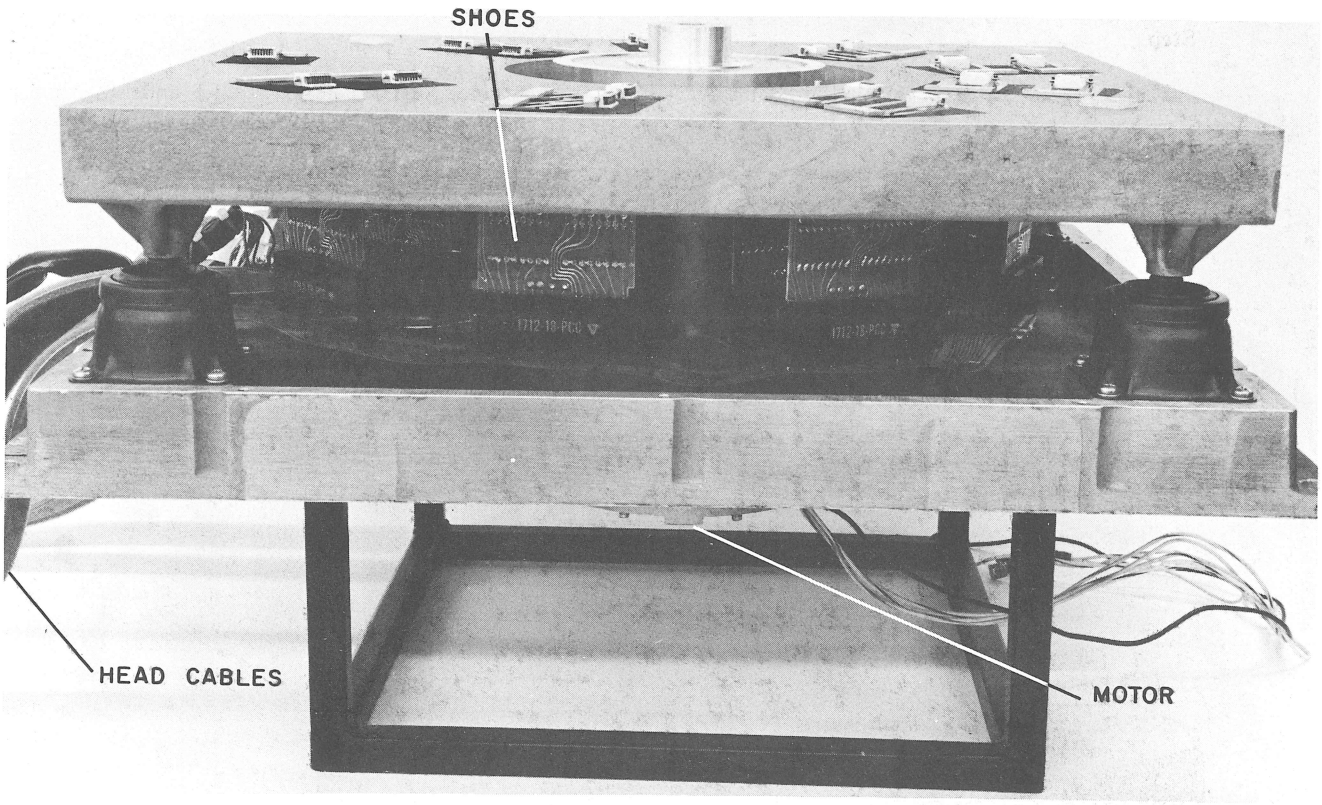


Figure 7-5 Disk Assembly With Cover and Surface Removed

Step	Procedure
3	Remove the disk surface by lifting it straight up while giving it a slight counter-clockwise twist in order to clear the heads.
4	Note which surface was used. Place the disk on its stand. Be careful that it is not contaminated with dirt.

7.2.3 Replacing the Shoes

To replace the shoes, perform the following steps:

Step	Procedure
1	Dismantle the assembly according to the instructions of Paragraph 7.2.1, and then remove the surface using the procedures outlined in Paragraph 7.2.2.
2	Locate the damaged shoe (see Figure 7-6). If it is an inside shoe, the outside shoe must then be removed first. Remove the damaged shoe.
3	Examine the new shoe. If it must be cleaned, flush it with Methanol spray and blow it dry. If any contaminants remain, saturate a cotton swab with Methanol and carefully wipe the head. Insert the new head.
4	To align the heads, cut out a single layer of Kimwipe approximately 4 in. x 4 in., and lay the Kimwipe over the motor hub to ensure a tight fit for the alignment disk.

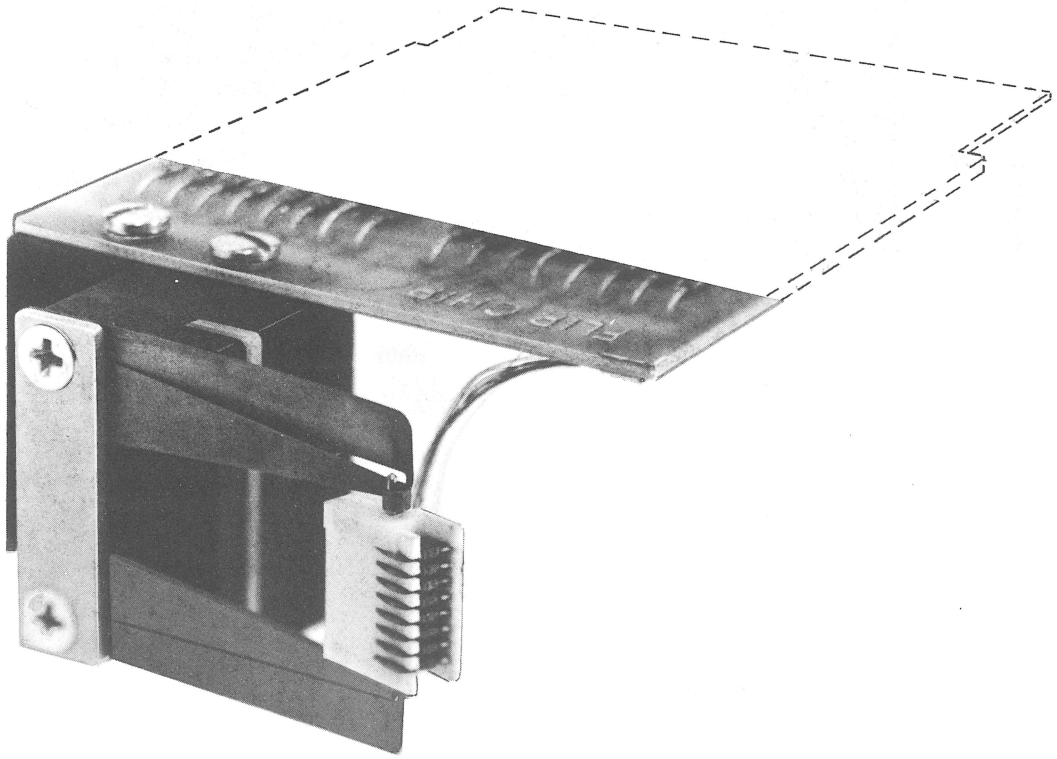


Figure 7-6 Shoe Assembly Removed

Step	Procedure
5	Gently fit the alignment disk over the tissue and hub until it is well seated. Ensure that the heads are seated firmly against the disk.
6	The outermost track on every pad must be in line with its scribe line on the disk, as shown in Figure 7-7.
7	Start with the outermost track on pad 0 (see Figure 7-8) and set it so that its inner edge is just touching the inside edge of the outside scribe line. Rotate the motor so that the radial line is over the next pad. Check that its outside track is lined up with the next track on the disk.
8	If any track is off center, loosen the three mounting screws on the bottom of the block and position it properly.

7.2.4 Replacing the Disk Surface

To replace the disk surface, perform the following steps.

Step	Procedure
1	Clean the disk surface that is to be replaced with a mild soap and Kimwipes. Do not forget which side is to be used.
2	Place the platter down on the hub and rotate it slightly counterclockwise.
3	Check the disk surface with the dial gauge. The disk surface must be flat to within 1 mil through 360°.
4	Tighten the four hex nuts just enough to lock the washers.
5	Recheck Step 3. Adjust the hex nut pressure to compensate for any TIR (Total Indicated Runout), that does not meet specifications.
6	Replace the cover.

7.2.5 Rewriting the Timing Tracks

When a new surface is installed or an old surface removed and replaced, the timing tracks must be rewritten. This is done with the Timing Track Writer (shown in Figure 7-9) as follows:

Step	Procedure
1	Install the disk into its rack, following the instructions of Chapter 5.
2	Remove the dc voltage from the RS09 logic. This can be accomplished by turning the power off at the main console of the computer. The ac power to the disk unit and the purge unit must remain on.
3	Remove the timing track cable from the RS09 unit. The cable is located in SLOT A1 of each RS09.
4	Remove the cover from the RS09 Timing Track Writer and remove the dc-wiring cable from the box. The dc-wiring cable contains four wires with Heco Tab connectors on the ends. The wire color coding is: *a.* Yellow +20V *b.* Red +10V *c.* Blue -15V *d.* Black GND

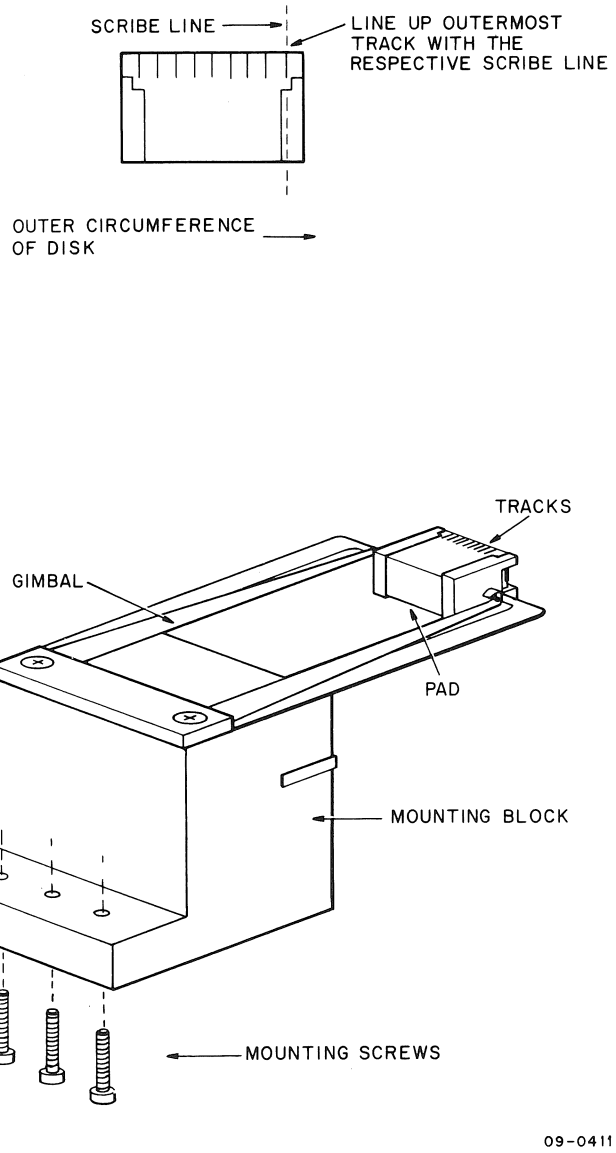


Figure 7-7 Aligning the Heads

Step	Procedure
5	Mount the Timing Track Writer box in the cabinet via the holding pins on the rear of the tester box. These pins should slide into the prepunched holes in the cabinet frame directly above the RS09 logic.
6	Insert the dc-power cable for the Timing Track Writer between the disk unit and the disk logic. The cable plugs into the dc power bus on the rear of the RS09's disk chassis. Insert the individual wires into the proper voltages as indicated on the rear of the RS09 chassis. (All wires and tabs are color coded for easy identification.)
7	Insert the timing track cable from the disk into the slot provided in the front of the tester.

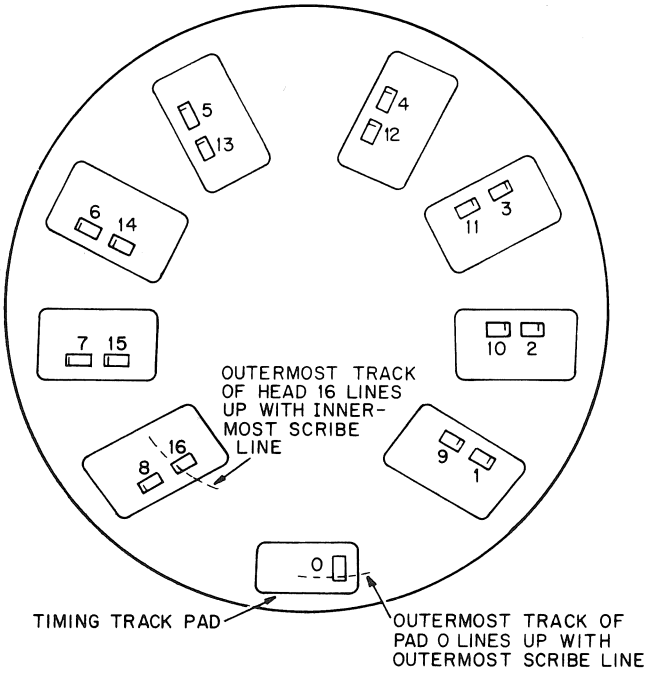
NOTE

This cable is a dual connector and may be plugged in on either side.

8	Turn power on. Power (dc) should be applied to the RS09 logic as well as the tester.

NOTE

Complete steps 9 and 10 as quickly as possible after turning the WRITE VOLTAGE switch ON. Failure to do so will damage the head center tap resistors that are inside the disk enclosure.



NOTE:
The numbering system used to designate pads is only for representation. It is not necessarily the way the pads are actually numbered.

09-0412

Figure 7-8 Aligning the Heads

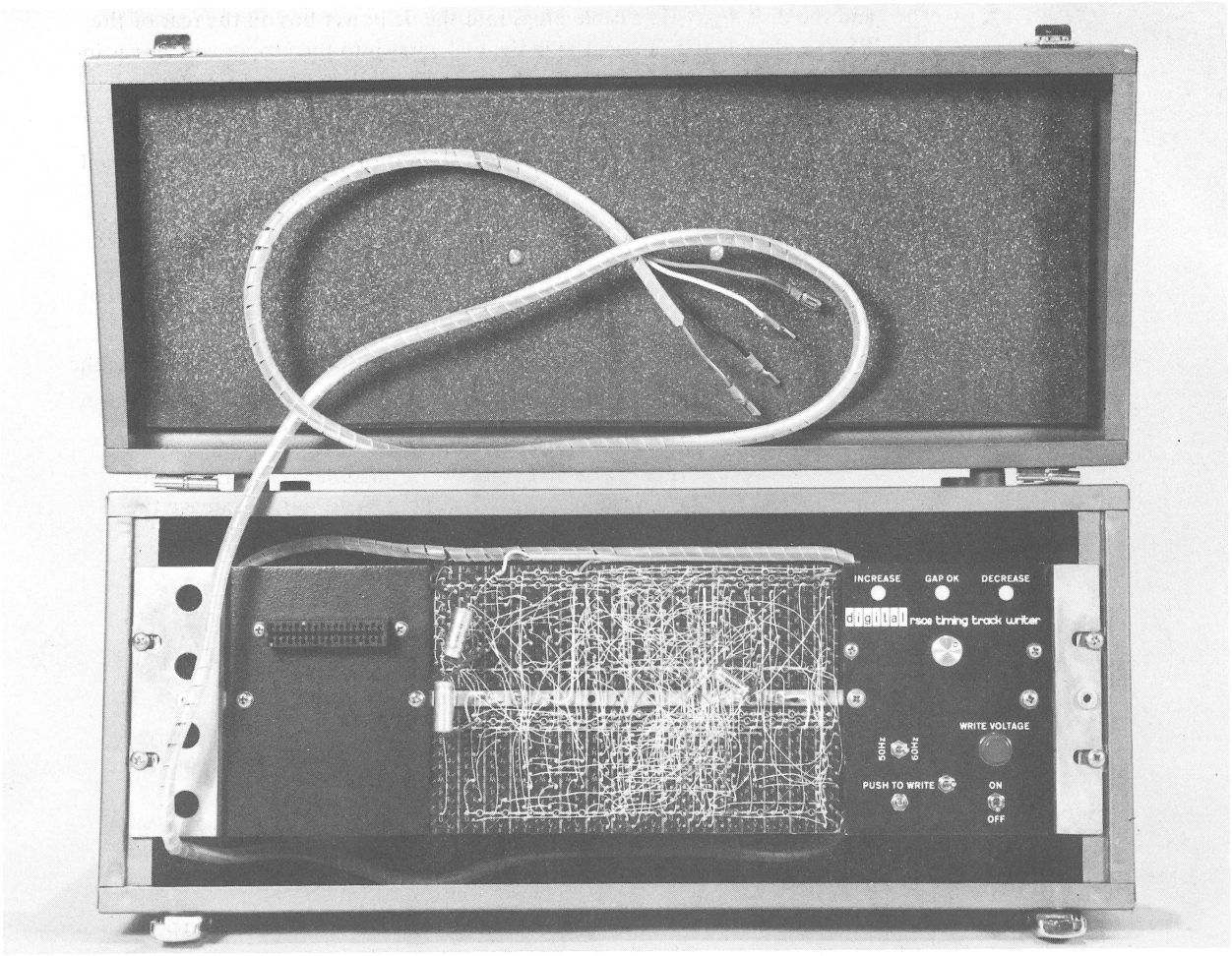


Figure 7-9 Timing Track Writer

Step	Procedure
9	Select the proper disk Control (PDP-9/PDP-15) and motor speed; i.e., 50 or 60 cycles via the switch on the front of the tester. (Note that the PDP-9/PDP-15 switch is not shown on the model of Figure 7-9. This switch is included in later models.)
10	Set the WRITE VOLTAGE enable switch on the front panel to the ON position. The red indicator light should illuminate.
11	Press the WRITE button under the frequency selector to begin the actual writing. The Timing Track Writer automatically recycles if the gap is not correct and indicates this via a flashing INC (increase) or DEC (decrease) light. To correct the gap, turn the knob clockwise if INC is flashing, and counterclockwise if DEC is flashing. When the gap is correct, OK lights and the writer stops. To ensure that writing has been successful, push the WRITE button once more without adjusting the knob. The OK light should come on without flashing either the INC or DEC lights.
12	Set the WRITE VOLTAGE switch to OFF. Turn the power off and remove the dc power lines from the RS09 and tester. The Timing Tracks should now be properly recorded.
	NOTE **Use the Timing Track Writer as little as possible. The Timing Track Writer drives 1W through 1/8-W head resistors. If it is used for too long a period, these resistors burn out. Writing stops when the OK light illuminates.**
13	Plug the Timing Track cable from the RS08-M into slot A01 of the RS09 Logic Panel.
14	Turn system power ON. Adjust the three Timing Track read amplifiers (G085) for 6V peak-to-peak and 1.1V slice, using the methods outlined in Chapter 6, Paragraph 6.2. Be sure to test both sets of tracks. By reversing the Timing Track cable at location A01, the second set of tracks is available to the RS09.

After writing new timing tracks, the unit should be thoroughly tested with its diagnostics. This is done by writing data using one set of timing tracks, then swapping this set for the other and reading the same data back. Before this is done, the Timing Track Readers should be adjusted for gain and slice following the procedures of Chapter 6, and the surface modulation of the disk should be checked according to the procedure of Paragraph 7.3.1. The procedure to calibrate the data heads should be carried out, as outlined in Paragraph 7.3.2 and 7.3.3.

7.3 FIELD LEVEL RS09 CALIBRATION

If a new surface or new shoes have been installed, calibration should be carried out and recorded on the sheets illustrated in Figure 7-13. The tests include one test to measure surface modulation and several tests to measure the mean voltage of each matrix and establish an optimum gain for the readers.

7.3.1 Measuring Surface Modulation

This test is done on the A track only. Surface modulation is the result of variations in the properties of the surface around the disk. It is measured using the following procedure.

Step	Procedure
1	Connect a calibrated oscilloscope probe to pin A02T of the RS09 (A Timing Track read amp).
2	Connect the oscilloscope ground strap to A02C.
3	Place the oscilloscope setting on dc.
4	Trigger the oscilloscope on LINE.
5	Set the time base to 5 ms/CM.
6	Measure Vmax pp and Vmin pp, as shown in Figure 7-10. Surface modulation = $\frac{\text{Vmax pp - Vmin pp}}{\text{Vmax pp + Vmin pp}}$ x 100 (Surface modulation should be less than 20%.)

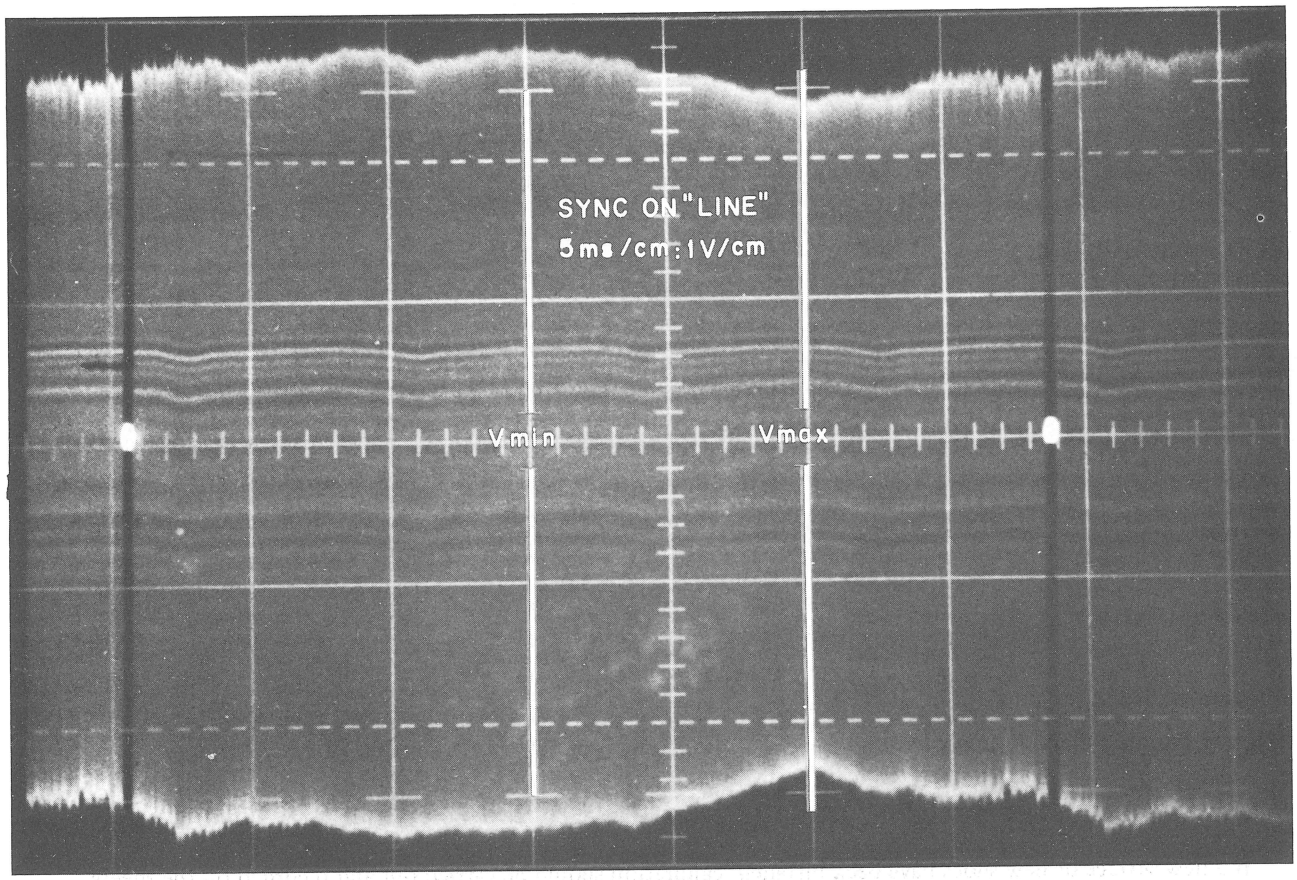


Figure 7-10 Measuring Surface Modulation on the A Track

7.3.2 Analyzing the Gain of the Data Tracks

When a new disk surface is installed or heads are replaced, the data tracks should be recalibrated. This process involves measuring the mean voltage from each head, the mean value for each shoe, and the percentage deviation for each matrix. Percent deviation is a measure of the difference in the readings. The smaller this value is, the more consistent the readings are in the matrix. In order to reduce this deviation, the shoe with the lowest reading is given a 20 percent boost in gain; and the deviation is recalculated. If the result is a reduction, a jumper is then installed in the RS09 to affect the increase in gain when that shoe is selected. The next lowest shoe is tried to see if a 20 percent increase in gain for it reduces the percentage of deviation further. If the percentage of deviation is reduced another jumper is installed. This process continues until adding more gain to the next shoe does not decrease the percentage of deviation.

The readings taken during this calibration are recorded on the Head Data Sheet. When all of the readings have been taken, the average shoe for each matrix is located; and its readings posted on the disk as a calibration standard to set the G085 readers in the future. The procedure to carry this out is as follows:

Step	Procedure
1	Obtain the following equipment: *a.* 1 PDP-9 or PDP-9/L *b.* 1 DECdisk system *c.* 1 Tetronix 453 oscilloscope or equivalent *d.* 1 Disk Data diagnostic (MAINDEC-09-D5AA)
2	Load the Disk Data diagnostic and write all 1s on all tracks.
3	Go to the STAMP test of Disk Data. This test allows the operator to select any track he wishes to examine by loading its number into the Switch register. (The relationship between the selection lines at the RS09 and the Switch register bits 11 to 17 are transferred by STAMP into bits 0 to 6 of the AC, and from there into bits 0 to 6 for the Track Address register. Bits 0 to 6 of the Track Address register are in turn translated into T06 to T00 at the RS09 selection matrix. The sequence is summarized below.)

	Matrix	Head	Shoe
Switch Register	11	12, 13, 14	15, 16, 17
Track Address Register	0	1, 2, 3	4, 5, 6
RS09 Track Select Lines	T06	T05, T04, T03	T02, T01, T00

4	Calibrate the oscilloscope and compensate the oscilloscope probes.
5	Take arithmetic mean peak-to-peak readings on each head of matrix, according to the techniques outlined in Chapter 6. Probe 1 should go on A05T and probe 2 on B05E. (Refer to Engineering Drawing D-BS-RS09-0-5.)
6	Repeat Step 5 for matrix 1. Probe 1 goes on A07T and probe 2 on B07E. Record the reading on the Head Data Sheet.

Step	Procedure

7 From the previous readings, find the percentage of deviation for each shoe, using the formula:

$$\frac{Vmax - Vmin}{Vmax + Vmin} \times 100 = \%\ deviation$$

where: Vmax is the largest mean peak-to-peak voltage taken on that shoe, and
Vmin is the smallest mean peak-to-peak voltage taken on that shoe.

This value should be less than 20 for any shoe. If it is more than 20, the shoe should be replaced.

8 Find the mean peak-to-peak voltage for each shoe with the formula:

$$\frac{Vmax + Vmin}{2} = A\ mean$$

9 From the mean for each shoe, calculate the percentage of deviation for each matrix with the formula:

$$\frac{Amax - Amin}{Amax + Amin} \times 100 = \%\ deviation$$

where: Amax = the maximum mean of all shoes
Amin = the minimum mean of all shoes

Attempt to reduce the percentage of deviation by adding 20 percent of the lowest reading to itself. Repeat this for the next lowest reading and check to see if it reduces the result. Continue this procedure until 7 shoes have been added to, or the percentage of deviation starts to increase. If the percentage of deviation decreases further when an eighth jumper is added, the computation has been done incorrectly. An average of four jumpers are used. This process is illustrated in the following example:

Example:

	A Mean	A Mean	A Mean
0	6.35 (Min) + 20% =	7.62	7.62
1	7.21	7.21 (Min) + 20% =	8.65 (Max)
2	7.46	7.46	7.47
3	8.00	8.00 (Max)	8.00
4	7.65	7.65	7.65
5	7.40	7.40	7.40 (Min)
6	7.65	7.65	7.65
7	7.46	7.46	7.46
%	Dev		
=			
	11.5 %	5.2 %	7.8 %
	(a)	*(b)*	*(c)*

Look for minimum % deviation.

a. $$\frac{8.00 - 6.35}{8.00 + 6.35} \times 100 = \frac{1.65}{14.35} \times 100 = 11.5\%$$

Step	Procedure

9 (Cont)

b. $$\% \text{ Dev} = \frac{0.79}{15.21} = 5.2\%$$

c. $$\% \text{ Dev} = \frac{1.25}{16.05} \times 100 = 7.8\ \%$$

By increasing shoe 0 by 20 percent, the deviation was reduced to a minimum. In order to effect this increase in gain on this shoe, a jumper must be installed in the logic of Engineering Drawing D-BS-RS09-0-1. Table 7-1 indicates the proper jumper for each shoe. In this case, assuming matrix 0 was under test, pin B17M would be jumpered to pin B20D.

10 Example b in step 9 is now the true set of means for the shoes in that matrix. Using these means, calculate the average track from the formula:

$$\frac{\text{Amax} + \text{Amin}}{2} = \text{Average track}$$

Find a track that is within 10 percent of the mean peak-to-peak voltage, but that is not in a shoe that has a gain jumper, and identify it as the average of that matrix. Repeat the procedure for the other matrix. From the example:

$$\frac{8.00 + 7.21}{2} = 7.655$$

Since the track's means are not part of this example, the actual average track cannot be shown. (It is most likely to be in shoe #4, however.)

If a track without a gain jumper within 10 percent of the average track cannot be found, multiply the average track value times 5/6 and look for a track in a shoe with a gain jumper that comes within 10 percent of this number. Once a track has been selected, multiply that track value by 6/5 to take oscilloscope readings.

Table 7-2
Jumpers to Increase Gain

Shoe #	Pin		Matrix 0 Gain	Matrix 1 Gain
XX0	B17M		B20D	B20K
XX1	B17N		B20E	B20L
XX2	B17P		B18D	B18L
XX3	B17R	To Matrix 0 gain	B18E	B18M
XX4	B17S	OR Matrix 1 gain	B18H	B18P
XX5	B17T		B18J	B18R
XX6	B17U			
XX7	B17V			

If 7 shoes require gain, run the matrix wire B18V to B18K (Matrix 0) or to B18S (Matrix 1); and add a jumper B18T or B18U. No matrix should ever need more than 7 jumpers.

11 *1.* Using the RS08-M test data sheet that accompanies the RS08-M, list the Arithmetic Mean (A mean) on the next column after each shoe.

Step	Procedure
11 (Cont)	*2.* Star those shoes requiring gain jumpers.
	3. Circle the track in each matrix used as the reference for the G085 gain adjustment.
	4. Record each reference track and its respective peak-to-peak voltage setting (computed on the RS09 Test Data Sheet) on both the RS08-M Test Data Sheet and the cover of the disk.

7.3.3 Calibrating the Gain of the Data Readers

In the previous paragraph, the optimum configuration for minimum percentage of deviation was established among the shoes. In this paragraph, the optimum gain for each reader is determined. This is done by determining the operating range of the slice-to-gain ratio. The highest operating gain with the smallest operating slice is found; and, conversely, the lowest possible gain with the highest possible slice. When these two ratios are found, the gain is set to the point that lies midway between the two at a normalized slice of 1.1V.

The Disk Data program is used to run optional test patterns. Proceed as follows:

Step	Procedure
1	Run the optional pattern on the entire disk. first word 525252 second word 000001
2	Go to READ mode. Set the slice of the first matrix reader to 1.1V from the average track. Raise the gain of that reader until one failing point occurs. If no failure occurs, leave the gain on maximum and start to lower the slice below 1.1V. When a failure occurs, scope these points and determine the reason for the failure. Figure 7-11 illustrates the waveforms.
3	Repeat Step 2 for the other matrix.
4	Run the optional pattern on the entire disk first word 000001 second word 525252
5	Repeat Steps 2 and 3.
6	Go to READ mode. Set the slice of the first matrix reader to 1.1V from the average track. Lower the gain of the reader until a failure occurs. If there is no failure at the lowest gain, start to raise the slice level above 1.1V until a failure does occur. Scope these points and determine the reason for the failure. Record these readings. Figure 7-12 illustrates the waveforms.
7	Repeat Step 6 for the other matrix.
8	Run the optional pattern on the entire disk. first word 525252 second word 000001
9	Repeat Steps 6 and 7.

Step	Procedure
10	Calculate the optimum gain for each reader from these readings. This is done by taking the lowest maximum gain and the highest minimum gain from the two tests, normalizing to 1.1V and finding the center point between the two gains.

Example:

High gain = 14 failed at slice .8V.

Low gain = 4.8 slice at 4.6V.

$$\text{Normalized gain} = \frac{14 \times 1.1}{8} = 19 \text{ for high}$$

$$= \frac{4.8 \times 1.1}{4.6} = 1.15$$

$$\text{Gain setting should be } \frac{19 - 1.15}{2} = 8.9$$

The average track should be selected, and its mean peak-to-peak output voltage set at 8.9V. This step should be repeated for the other matrix.

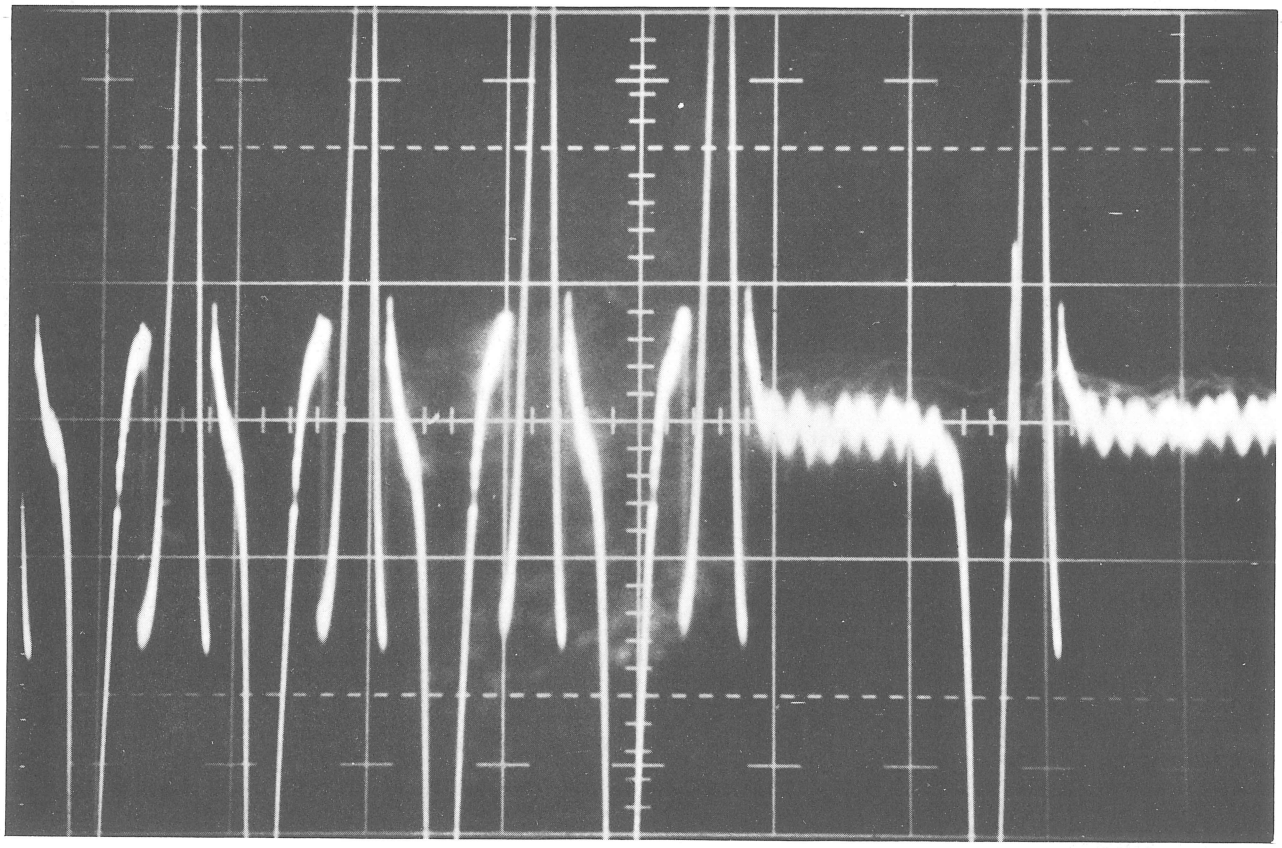
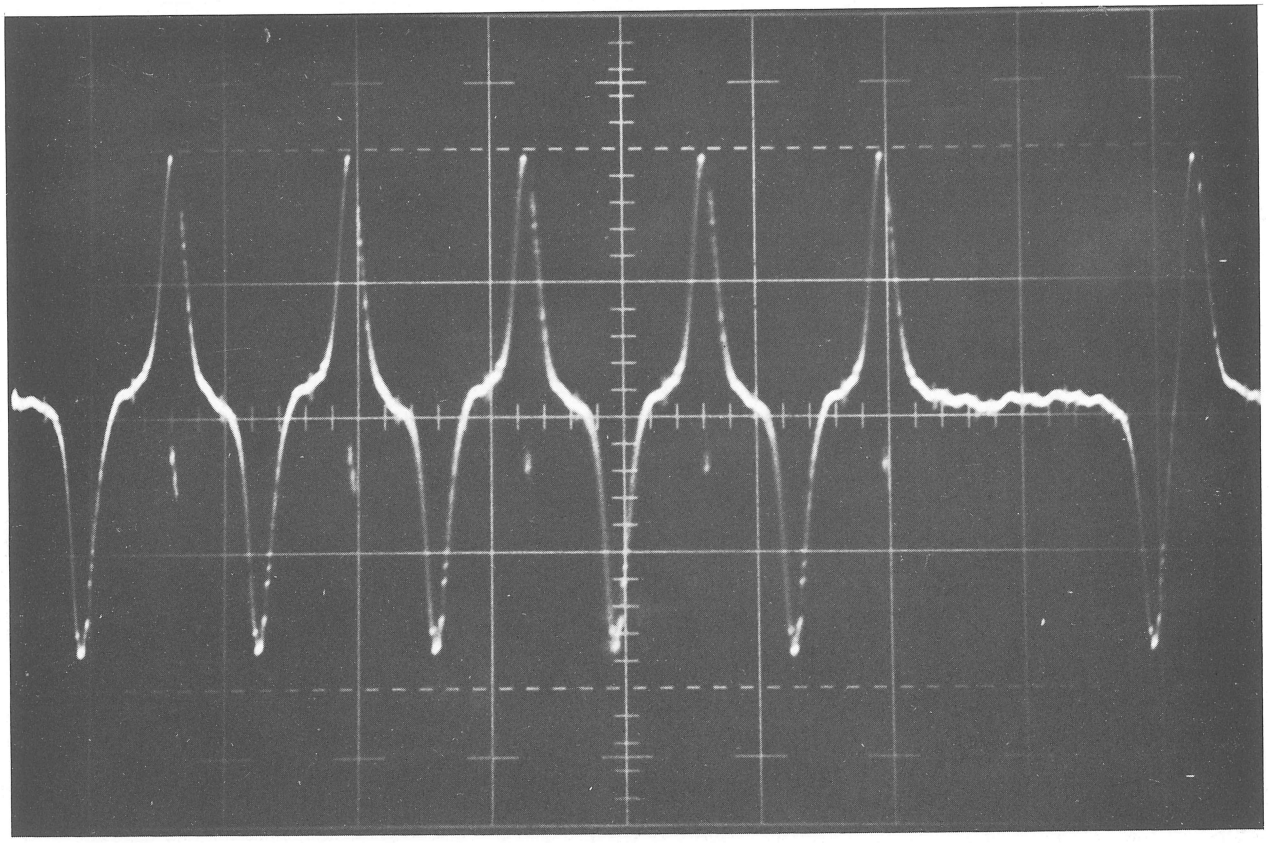


Figure 7-11 Maximum Gain, Minimum Slice



SYNC ON RD SR
10 µsec/cm 2V/cm

Figure 7-12 Minimum Gain, Maximum Slice

RSØ8M DATA SHEET

DATE: _____ BY: _____ DISK MFG.&# 432 HEAD TESTER #: None MOTOR FREQ.: 50 HTZ

SCOPE TYPE & #: 453 PREAMP TYPE & #: 038518 TYPE PROBES: B6047 X 10

	AGC	POS.	GRAMS PER SIDE	SIGNAL READING								A MEAN	AFTER GAIN	COMMENTS
				Ø	1	2	3	4	5	6	7			
1		TT												
2	✳	Ø		6.2	6.4	5.9	6.0	6.6	6.8	6.7	6.6	6.35	7.62	
3		1		7.0	7.1	7.2	7.4	7.1	7.4	7.0	7.3	7.21	7.21	
4		2		6.2	6.0	7.8	7.2	7.0	7.5	7.92	6.5	7.46	7.46	
5		3		8.0	8.5	7.5	7.0	7.2	7.6	8.8	9.0	8.0	8.0	
6		4		7.28	7.9	7.5	7.7	7.6	7.4	8.0	7.3	7.65	7.64	
7		5		6.8	6.9	7.0	6.9	6.9	7.8	7.0	7.0	7.4	7.4	
8		6		7.0	7.2	8.3	7.1	7.3	7.1	7.2	7.0	7.65	7.65	
9		7		7.4	7.9	7.0	7.5	7.1	7.92	7.8	7.3	7.46	7.46	
1Ø		1Ø		6.0	5.8	5.9	5.6	6.2	5.6	5.7	5.7	5.8	5.8	
11		11		6.0	5.8	5.5	5.5	5.7	5.8	5.8	5.8	5.75	5.75	
12		12		5.8	5.4	5.6	5.6	5.8	4.9	5.1	5.9	5.4	5.4	
13	✳	13		5.2	5.0	5.0	5.6	5.3	5.2	4.6	4.6	5.1	6.12	
14	✳	14		5.2	4.8	5.1	4.8	4.8	4.6	4.6	5.2	4.9	5.88	
15	✳	15		5.3	5.0	4.5	4.7	5.1	4.2	4.5	4.8	4.75	5.7	
16	✳	16		5.0	4.6	5.0	4.8	5.2	5.2	4.2	5.0	4.85	5.82	
17	✳	17		5.0	4.9	4.8	4.9	4.6	4.8	4.6	4.2	4.6	5.52	
				Ø	1	2	3	4	5	6	7			

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Figure 7-13 RS09 Test Data Sheet (Sheet 1)

RS09 TEST DATA SHEET

RS08M # _____ Date _____

RS09 # _____ Name _____

RF09 # _____

Surface Modulation on A Track _____ %

MAX GAIN/SLICE RATIO

	Matrix 0	Matrix 1
$\frac{\text{High Gain Setting}}{\text{Low Slice Setting}} =$	$____ = \frac{A}{B}$	$____ = \frac{C}{D}$

Matrix 0 Reason for Failure _____

Matrix 1 Reason for Failure _____

MIN GAIN/SLICE RATIO

	Matrix 0	Matrix 1
$\frac{\text{Low Gain Setting}}{\text{High Slice Setting}} =$	$____ = \frac{E}{F}$	$____ = \frac{H}{J}$

Matrix 0 Reason for Failure _____

Matrix 1 Reason for Failure _____

Using the reading obtained above – Compute:

Matrix 0 = $\frac{A}{B}$ = X0 = _____ $\frac{E}{F}$ = Y0 = _____

Matrix 1 = $\frac{C}{D}$ = X1 = _____ $\frac{H}{J}$ = Y1 = _____

$\frac{X0 + Y0}{2}$ = Z0 = _____ $\frac{X1 + Y1}{2}$ = Z1 = _____

Setting slice to 1.1V compute:

Z0 x 1.1 = _____ = Voltage setting of Ave track in each matrix respectively

Z1 x 1.1 = _____ =

Now set slice to 1.1V and set the voltage gain settings of the Ave track to the values obtained above.

Compute figure of merit.

$\frac{X0 - Y0}{X0 + Y0} \times 100 = FM$ $\frac{-}{+} \times 100 =$ _____ $\frac{X1 - Y1}{X1 + Y1} \times 100 = FM$ $\frac{-}{+} \times 100 =$ _____

Figure 7-13 RS09 Test Data Sheet (Sheet 2)

Appendix A
RF09 Signal Summary

Signal	Summary
ADROK	ADdRess OK logic signal. A true signal exists whenever the DS Register equals the WA Register, APAR is a zero, and the CTL bit has successfully shifted through all positions of the DS Register.
ADS TO IOB	Signal that places the ADS Register on the I/O Bus.
ADS	Address of Disk Segment. Bits of a register that save the D.S. shift register for real-time program control read-back.
APAR	Address PARity flip-flop. Computes parity of address read from Disk. Includes the Control (CTL) Bit.
APE	Address Parity Error
API ENA	Automatic Priority Interrupt ENable A. API Control signal indicating time for API Address to be put on the I/O Bus.
API 1 EN IN	Automatic Priority Interrupt level 1 ENable IN. True if no higher priority device on level 1 is requesting a priority break.
API 1 GR	Automatic Priority Interrupt level 1 GRant. Device requesting API break was granted service.
API 1 RQ	Automatic Priority Interrupt level 1 ReQuest to Processor.
AP1 CLR	Address Pointer #1 - CLEAR. The IOT that clears the Disk Address Register.
AP1 TO IOB	Address Pointer #1 to I/O Bus. The IOT that reads the Disk Address Register onto the I/O Bus.
ATEST	This signal allows A track pulses to enter the A track error detection circuitry.
ATF SAVE	A Timing track Flip-flop. Remembers which polarity ATT came last.
ATOK	A Timing OK. A timing pulses are occurring at their normal rate.
ATP	A Timing Pulses. Regenerated OR of the ATT's and AAT's.
ATPM	A Timing Pulse generated by the Maintenance logic.
ATPN	Logical OR of the A Timing Pulses.

Signal	Summary
ATTN	A Timing Track Negative. Level converted or buffered RS09 signal - ATT.
ATTP	A Timing Track Positive. Level converter or buffered RS09 signal + ATT.
ATT	A Timing Track. RS09 interface clocking signal. Unrectified signal pairs of this signal are designated + ATT and - ATT.
BR	Buffer Register.
BR TO IOB	Place BR on I/O Bus.
BR CLR	CLeaR the Buffer Register.
BR TO SR	Transfer the Buffer Register TO Shift Register.
BTER	B Timing track ERror. Missing or extra signal from the BTT.
BTF	B Timing track Flip-flop. Remembers which polarity BTT came last.
BTN	B Timing track Negative. Level converted or buffered RS09 signal - BTT.
BTP	B Timing track Positive. Level converted or buffered RS09 signal + BTT.
BUSY	Requested Disk transfer not completed.
BTT	B Timing Track. RS09 interface signal containing the eleven bit address of the disk segment. Unrectified signal pairs of the address track are +BTT and -BTT.
CH DSA	Data CHannel and Device Select A. IOT (code 70) OR'd with DCH ENB.
CLR	CLeaR - the OR of all clear signals.
CTER	C Timing track ERror. Missing or extra signal on the CTT lines.
CTF	C Timing track Flip-flop. Remembers which polarity of CTT was last present.
CTL	ConTrol. First bit read from the BTT. Used to control checking of the DS with the WA and shifting of the DS register.
CTN	C Timing track Negative. Level converted or buffered RS09 signal - CTT.
CTP	C Timing track Positive. Level converted or buffered RS09 signal + CTT.
CTP 1	C Timing Phase 1. First bit of a one bit 3-position ring counter used for word boundary control functions.
CTP2	C Timing Phase 2. Second bit of counter described in CTP 1.
CTP 3	C Timing Phase 3. Third bit of counter described in CTP 1.
CTT	C Timing Track. RS09 interface word boundary indicator. Unrectified signal pairs of this signal are designated +CTT and -CTT.

Signal	Summary
DA	Disk Address. Bits of a three-bit register indicating which disk of eight is selected.
DASV	DAta SaVe. Accepts each data bit to be shifted into the SR.
DATA ERROR	The OR of a data parity error and a data hardware error flag.
DATA FLAG	Flag raised by the control when DCH Break required. Effectively makes the DCH RQ.
DCH EN IN	Data CHannel ENable IN. True if no higher priority DCH device requesting a break.
DCH EN OUT	Data CHannel ENable OUT. True if no higher priority DCH devices and this device (RF09) are requesting a break.
DCH ENA	I/O Bus Data CHannel ENable A. Time to place channel address on I/O Bus for DCH break.
DCH ENB	I/O Bus Data CHannel ENable B. Time to place DCH control signals on I/O Bus (e.g., RD RQ or WR RQ).
DCH GR	I/O Bus Data CHannel GRant. Sets DCH ENA.
DCH RQ	I/O Bus Data CHannel ReQuest. I/O Bus control signal that requests DCH Break.
DCH TE	Data CHannel Timing Error. Processor had not completed DCH transfer before Disk control was ready for the next.
DIOP	Delayed IOP. Provides time for the control to determine its BUSY state.
DISK FLAG	Flag raised by either an ERROR or a XFER CPLT that may be skip tested under program control and cause an API or PI break request to the processor.
DISK RUN	Disk transfer requested (BUSY) and a word boundary has been found (CTP3).
DISK SYNC	DISK SYNChronized flip-flop. Shows a valid CTP3 pulse has occurred.
DPAR	Data PARity flip-flop. The flip-flop that calculates the data parity.
DPE	Data Parity Error. A flag set if there is a parity error in a data word.
DS CLR	Disk Segment register CLeaR.
DS TO ADS	Disk Segment TO ADdresS of the Disk Segment Transfer signal.
DS	Disk Segment. Bits of the Disk Segment address 11-bit shift register.
DSA	Disk Segment Address. Bits of a register that contain the real-time DS address readable under program control.
DSAB	Device Select A and B decoded (70 and 72).
DSB	Device Select B (code 72) decoded.

Signal	Summary
DTE	Data Timing Error. Missing or extra signal on the DTT lines detected here.
DTER	Data Timing ERror. Missing or extra signal on the DTT lines stored here.
DTN	Data Track Negative. Level converted or buffered RS09 signals - DTT.
DTP	Data Track Positive. Level converted or buffered RS09 signal + DTT.
DTT	DaTa Track. RS09 interface read data signal. Unrectified signal pairs of this signal are +DTT and -DTT.
EQ CMP EN	EQual CoMParison ENable. A signal that enables the WA and DS to compare.
ERROR	ERROR - the OR of the error flags.
FR CHNG	CHaNGe the Function Register IOT.
FR CLR	CLeaR the Function Register.
FRZ	FReeZe. Signal disables clock input to control as a result of a HDWR ERR or an APE.
F0O	Function Register bit 0 controlled by AC bit 12.
F0SV	Function Register bit 0 SaVe. Controlled by AC bit 12.
F01	Function Register bit 1 controlled by AC bit 13.
F1SV	Function Register bit 1 SaVe. Controlled by AC bit 13.
HDWR ERR	HarDWaRe ERRor. The OR of MNEP, MPEN, BTER, CTER, or DTER.
HIGH	Level indicating that the high-speed transfer rate has been selected.
INC DA	INCrement Disk Address. Occurs after the last word of each disk has been successfully transferred.
INC TA	INCrement Track Address. Occurs after the last word of each track has been successfully transferred via the DCH channel.
INC WA	INCrement Word Address register. Occurs for each successful transfer on the DCH channel.
INH RD	INHibit ReaD. Signal disables the read portion of the control logic to allow time for the RS09 read amplifiers to recover from an input overload.
INT EN	INTerrupt ENable. Control flip-flop that determines if the DISK FLAG will cause an interrupt via the API or PI facility. Prog Skip is honored independently of the state of INT EN.
INT SV	INTerrupt Enable SaVe. Second part of Function Register bit 2 controlled by AC bit 14.

Signal	Summary
IOB	I/O Bus driver inputs.
IOB TO AP0	Strobe contents of I/O Bus into Address Pointer 0.
IOB TO AP1	Strobe contents of I/O Bus into Address Pointer 1.
IOB TO BR	Strobe contents of I/O Bus into the Buffer Register.
IOD	I/O Bus Driver outputs.
IOP 1	Input/Output Pulse 1.
IOP 2	Input/Output Pulse 2.
IOP 4	Input/Output Pulse 4.
IOR	I/O Bus Receiver. Level converters and/or buffers for the I/O Bus interface.
IOT CLR	IOT CleaR. RF09 program controlled "power clear". Only control IOT recognized when a FRZ condition exists.
IOT CONT	IOT CONTinue. The execute IOT that starts the controller executing.
I/O ADDR	I/O ADDRess. I/O Bus address lines used to determine API channel address as well as DCH channel address.
I/O BUS 00-17	Computer I/O BUS data lines.
I/O OFLO ENB	OR of I/O OFLO and DCH ENB.
I/O PWR CLR	I/O PoWeR CLeaR. I/O Bus power clear line.
I/O OFLO R	I/O OverFLOw Receiver. I/O Bus signal indicating the last DCH break is in process.
I/O SYNC	The computer SYNC pulse train.
IOT CONT	IOT CONTinue. Program command that transfers the contents of the Function Register Flip-Flop (F0, F1, INT) to the Function Register Flip-Flop.
LDSR	LoaD Shift Register. Control has found the location of the word to be Written or Write Checked, has transferred the BR to SR, and is shifting the data onto the WRITE DATA line.
LDLY	Load DeLaY. A flag set during the Write Check operation to check for data parity errors.
LIOP 4	Load IOP. A delayed DIOP. Provides for a Clear/Load cycle by using DIOP to Clear and LIOP to Load.
LOCK	RS09 interface signal signifying that the Disk and Track selected is Write Protected.

Signal	Summary
LOW	A level that is asserted when the disk is set to the low transfer rates.
LS EN	Load Shift Register ENable. Control signal that allows loading of Shift Register (SR) during Write or Write Check.
LSTE	Load Shift Register Timing Error. A flag that is set and reset when the Buffer Register is filled during a Write or Write Check operation. If it resets too slowly, a DCH timing error is posted.
MAINT	MAINTenance flip-flop. Holds off RF09 delay time-outs during maintenance instructions.
MAT	Maintenance A Timing signal. Program control maintenance logic that simulates the RS09 head signal to the ATT read amplifier.
MBT	Maintenance B Timing signal. Program control maintenance logic that simulates the RS09 head signal to the BTT read amplifier.
MCT	Maintenance C Timing signal. Program control maintenance logic that simulates the RS09 head signal to the CTT read amplifier.
MCTL	Maintenance ConTroL IOT. Simulates RS09 interface signals by transferring AC bits directly into the RF09.
MDT	Maintenance DaTa signals. Program control maintenance logic that simulates the RS09 head signal to the DTT read amplifier.
MED	A level that is asserted when the disk is selected for MEDium transfer rates.
MNEP	Missing Negative or Extra Positive pulse from ATT's. Causes HDWR ERR status.
MPEN	Missing Positive or Extra Negative pulse from the ATT's. Causes HDWR ERR status.
MTO	Maintenance TOggle. Same as MTOG slightly advanced.
MTOG	Maintenance TOGgle. Maintenance IOT that uses the AC bits to produce MAT, MBT, MCT, and MDT.
MXFR	Missed X (Trans)FeR. Disk was BUSY and missed transferring data twice in succession from the same address. More than one Disk revolution occurred without a transfer.
NDT	Negative DaTa Flip-flop that stores the negative data bit.
NE DSK	NonExistent DisK. Error status indicating an attempt to use a nonexistent disk. May be caused either by sequencing into or by direct program command.
OFLO	OverFLOw flag set when the Data Channel overflows during a DECdisk transfer.

Signal	Summary
PC + IOT CLR	Power Clear and IOT CLeaR.
PDT	Positive DaTa - Flip-flop that stores the positive data bit.
PE	Program Error.
PIOP4	Pulsed IOP-4. The IOP-4 pulse slightly delayed through a pulse amplifier.
PROG INT RQ	PROGram INTerrupt ReQuest. I/O Bus signal for PI break request.
PSLER	Program SeLect ERror. A nonexistent disk was selected by the program. One of the inputs to the NE DISK status.
RB FULL	Read Buffer FULL. Control has loaded the BR from the SR and the processor has not as yet taken the data.
RD CLK	ReaD CLocK. Pulse used to shift the SR during Read or Write Check. Occurs at ATPD time.
RD DIS	ReaD DISable. OR of INH RD and MAINT. Allows maintenance control to nullify effect of INH RD.
RD LD	ReaD LoaD. During READ or WRITE CHECK this signal is one of the elements that enables data parity error detection.
RD RQ	ReaD ReQuest. Signal to processor requesting a read operation during a data channel transfer.
RD SR	ReaD (into the) Shift Register. Control has found word to be read from RS09 and is shifting the data into the SR.
RD STATUS	ReaD STATUS. IOT that causes the RF09 Status Register to be read into the AC.
RD TEST	ReaD TEST. A pulse that clocks the data error flag.
READ	Signal from controller to RS09 enabling the read amplifiers.
RS EN	Read Shift register ENable. Signal used at the word boundary being read. AND of RDSR and OFLO.
RSTE	Read Shift register Timing Error. A flag that is set and reset when the Shift Register is filled and loaded into the Buffer Register. If a timing error occurs, this DCH timing error flags.
SD	SubDevice levels.
SEL ERR	SELect ERRor. Signal return from jumper panel that allocates available disks to specific SEL lines. Unavailable disks return the SEL ER.
SEL	SELect. Unary decoded signals from the DA register for selecting one disk of eight.
SELECT	SELECT line from each disk.

Signal	Summary
SEQ ER	SEQuence ERror. A nonexistent disk was selected during a job transfer.
SER CLR	Shift Register CLeaR.
SKIP RQ	SKIP ReQuest to C.P.U.
SR CLK	Shift Register CLocK Pulse.
SR CLR	Shift Register CLeaR Pulse.
SR to BR	Shift Register to Buffer Register transfer pulse.
SR	Shift Register. Serial/parallel disk data converter.
SRI	Shift Register In. Command to transfer data from BR to SR during Write or Write Check.
SRIF	Shift Register In flag ANDed with the reset Overflow flag to enable the Data Flag.
SRO	Shift Register Out. True whenever the SR has assembled the data word to be read and the BR is ready to receive it.
STATUS CLR	CLeaR the STATUS register.
STATUS TO IOB	STATUS onTO I/O Bus data lines.
STOP	Prohibits execution of IOTs while RF09 is BUSY.
SYNC	Scope SYNC point when running Diskless.
TA	Track Address Register.
TA CLR	Track Address CLeaR.
TA WA CLR	Track Address and Word Address CLeaR pulse.
TP1	Timing Pulse #1.
TP2	Timing Pulse #2.
T00 - T06	Track address lines to RS09.
WA CLR	Word Address CLeaR.
WA	Word Address Register. An eleven-bit register containing the address desired on the disk. The WA is compared with the DS to give ADROK.
WB	Write Buffer FULL. Processor has loaded the BR with data requested during Write or Write Check and the control has not transferred the data from the BR to SR.
WLO EN	ENable Write LockOut. If any tracks are locked out, this signal effects the lockout.
WLO	Write LockOut. Error Status bit that occurs whenever an attempt is made to Write in an address that is Write Protected.

Signal	Summary
WR CKER	WRite CheckK ERror. Indicates a comparison error exists between the word from core memory and the word read from the disk during Write Check.
WR DA	WRite DAta flip-flop that receives the Shift Register output to be written on the disk.
WRITE	WRITE function decoded from Function Register.
WRITE DATA	RS09 interface signal line over which the RF09 sends the serial data to be written.
XFER CPLT	X (Trans)FER ComPLeTe. The last word has been transferred to/from the disk.
XLOW	LOW speed transfer rate selected.
XMED	MEDium speed transfer rate selected.

Appendix B
RSO9 Signal Summary

Signal	Summary
CT 00 X - CT 17 X	Center Tap Selector output signal +20V when selected. Applies current through the coil of its head.
±ATT (B)	A Timing Track. The positive or negative side of the clocking signal, Buffered.
±BTT (B)	B Timing Track. The positive or negative side of the address track signal, Buffered.
±CTT (B)	C Timing Track. The positive or negative side of the delimitter track, Buffered.
±DATA	The positive or negative side of the data signal.
±DSL 00-01	Data Signal Lines. Bidirectional data lines (positive or negative) between matrices and Read/Write amplifiers.
LOCK	Interface signal signifying that the disk and track selected is write protected.
MTRX 0 (1) GAIN	MaTRiX 0 (1) GAIN. Signal that is applied to the G085 of the corresponding matrix to increase its gain by 20 percent when a particular shoe is selected.
READ	Signal from RF09 to condition the RS09 to read.
SEL (BA)	SELECT line, Buffered.
SELECT	Signal showing that the RS09 unit has been selected.
SELECT 00-07	SELECT lines. Eight lines used to select the disk units.
T00 (0) - T06 (1)	Track address select lines that select one of 128 tracks.
WRITE DATA	Interface line over which the controller sends the data to be written.
WRITE CLK	The OR of the two timing track signals used to clock the G290 Write flip-flop.

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