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RS03 DECdisk SERVICE MANUAL

digital equipment corporation · maynard, massachusetts

RS03 DECdisk
SERVICE MANUAL

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digital equipment corporation · maynard, massachusetts

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PREFACE

SCOPE AND PURPOSE OF THIS MANUAL

This Service Manual has been devised to meet the needs of both Field Service and user personnel in servicing the RS03 DECdisk.

The bulk of the information may be found in Sections III and IV. Detailed theory, performance, and troubleshooting data is presented in modular elements, each devoted to a particular subassembly of the device, to minimize constant cross-checking through the document during troubleshooting. The modular elements are further separated into two categories: electrical and mechanical.

Section I of this Service Manual is devoted to introductory data. It includes an overall description of the equipment and defines the purpose of the equipment in a system. Both a physical and a functional description of the equipment is given with a brief list of technical characteristics.

Section II discusses the *Theory of Operation* of the RS03. It provides an overall functional description of the equipment, and its interface within a typical system. Only block diagrams are given here to describe series of events; timing diagrams are included whenever they are necessary to further delineate a concept.

Section III contains *Electrical Servicing* information. This section is headed by a diagnostic discussion for operation with the PDP-11 computer system. A table is included that describes each diagnostic test, its purpose, the probable malfunction indicated, and the probable mechanical and/or electrical area of the machine containing the fault. When an error is encountered in the testing of the RS03, this table should be used first to locate the particular area of trouble, directing the serviceman to a particular subsection for more detailed information concerning the operation and troubleshooting procedures for the module at fault. Each subsequent subsection includes a brief reminder of the location of the module in the overall system, followed by a detailed theory discussion of the operation of that module. This is then followed in each subsection by performance checks and troubleshooting information that applies to the individual module described.

Section IV contains *Servicing Information* for the mechanical portions of the RS03. This section describes, by subassemblies, the removal, replacement, inspection, and alignment of these subassemblies and cleaning procedures for critical items.

Section V is devoted to *Installation* of the RS03, with procedures for initially setting up the device in a system.

ORGANIZATION OF THE PRINT SET

The following conventions have been used on all RS03 logic module prints. Each module has a two or three alphabetic character code name as listed in the Prefatory Table.

Each sheet of the module circuit schematic has a code name, composed of the module code name followed by the sheet number of the drawing. For example, the G092 module (Timing Amp Logic) contains five circuit schematic drawings, labelled TM1, TM2, TM3, TM4, and TM5.

All signal names contain a prefix which is the drawing sheet code name for the sheet which shows the source of the signal. Example: TM3 SEC PULSE L is sourced on sheet 3 of the Timing Amp Logic module print.

On all modules, each signal pin (finger connection) has its pin number written *each time* its signal name appears on any sheet. Each time the pin number appears, it is placed in parentheses and has a solid arrow (into) on the sheet if it is connected *only* to inputs (destination). If it is connected to *any* logical output or source, it is not in parentheses and has a solid arrow (out of) on the sheet.

Multiple source signals (wired ORs) have many sources with different source sheet names and are documented as being connected on the wire list. They are also denoted as wire ORed signals by a "WO" in the signal name.

Prefatory Table
RS03 Signal/Drawing Number Prefixes

Prefix	Module Name	Module Designation	Logic Slot
TRA	MASSBUS TRansceiver A	M5903	AB04
TRB	MASSBUS TRansceiver B	M5903	AB05
TRC	MASSBUS TRansceiver C	M5903	AB06
CN	CoNtrol	M7755	AB07
ST	STatus	M7770	AB08
CD	Command Decode	M7759	AB09
AD	ADdress Register	M7754	AB10
FT	FormaT	M7771	AB11
DA	DAta Register	M7753	AB12
ED	Encode/Decode	M7751	AB14
TM	TiMing Amp Logic	G092	AB16
RW	Read/Write & Det.	G182	AB17
ATO	Alternate Track Option	M7756	AB20
HM	Head Matrix	M7758	AB18, 19

It is hoped that this new Service Manual format will more fully meet the needs of our customers and it is anticipated that it will more easily meet the needs of Training. Comments and suggestions from the field will be welcomed. A postage-paid form has been included at the back of the manual. Please use this tear-out page when communicating with the *DEC Technical Documentation Department.*

REFERENCE DOCUMENTS

In the preparation of this Service Manual, the following documents have been referred to in whole, or in part, as a guide to its preparation:

RS03 DECdisk Illustrated Parts Breakdown	DEC-RS03-IPB
RJS04/RJS03 Fixed-Head Disk System Maintenance Manual	DEC-11-HRJSA-A-D
RH10/RS03-04 Disk Controller Maintenance Manual	DEC-10-HRHMA-A-D
Digital Logic Handbook	058.00173.2505
PDP-11 Peripherals and Interfacing Handbook	112.01071.1854

RS03 DECdisk SERVICE MANUAL

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SECTION 1
INTRODUCTION

1.1 GENERAL

This section contains the information necessary to familiarize the reader with the overall characteristics and purpose of the RS03 DECdisk. It contains a description of a typical system in which the RS03 is used. In addition, it delineates the various subassemblies of the equipment and describes them from a functional standpoint. The controls and indicators are shown with a tabular listing of their purposes and a table of drive specifications is included.

1.1.1 Characteristics

The RS03 DECdisk (frontispiece) is a MASSBUS fixed-head disk subsystem that functions as a random-access mass storage device, possessing characteristics that are particularly applicable to swapping operations. The unit is designed to interface with any MASSBUS Controller. Maximum storage capacity is 262,144 18-bit words. The average transfer rate is 4 μs per word. The device is completely self-contained, requires 15-3/4 in. of panel space in a standard 19 in. rack, and slides forward for servicing.

Data is stored in the RS03, on one surface of a single, nickel-cobalt plated disk that is driven by a unitized ac induction motor/spindle.

Internal drive timing and addressing information is derived from a single prerecorded timing track. This includes index (once per revolution) and sector marks, as well as individual bit cell boundaries (when writing).

Recording on the disk is by the Three Frequency or Modified Frequency Modulation method, commonly referred to as the *Miller Encoded Recording Technique.* When writing, the data is synchronized to the timing track; when reading back however, the data is self-clocking and therefore need not be synchronized to the timing track.

Spare data tracks, which are jumper-selectable, are provided to replace any tracks which may fail over the life of the drive. In addition, one spare pre-recorded timing track is provided.

Write Protect logic is included in the RS03. When enabled, complete tracks starting with track 00 up to and including any switch-selectable track, are write protected (i.e., read-only).

1.1.2 Typical System Configuration

Figure 1-1 illustrates a typical RS03 multi-drive system configuration. Drive selection logic, located within each RS03, allows each MASSBUS Controller to service up to eight fixed-head disk files. For information concerning the Controller itself, refer to the Controller maintenance manual.

1.1.3 RS03 Recording Technique

The RS03 utilizes the Miller Encoded Recording Technique to magnetically record data on the disk surface. In the Miller encoding method, each logical one produces a flux reversal in the center of its bit cell. Two successive logical zeros produce a flux reversal at the bit cell boundary between them. There is no flux reversal in a bit cell containing a logical zero following a logical one. This method of recording has the advantage of putting at least one flux reversal on the disk for every two bit cells, thereby making it feasible to use phase-locked loop techniques to form a self-clocking data recovery system. This method has a maximum flux reversal density of one reversal per bit cell.

In this method, clock pulses from the prerecorded timing track are used to establish the bit cell time interval during writing. When reading, the phase-locked loop is synchronized to the data stream and is used as a data recovery clock.

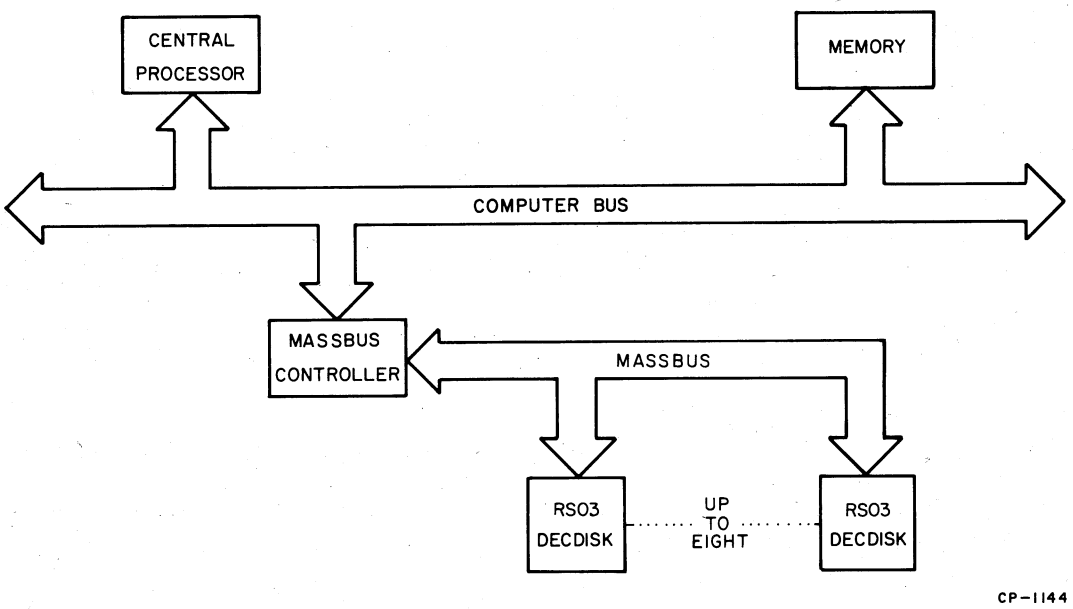

Figure 1-1 RS03 Typical System Configuration

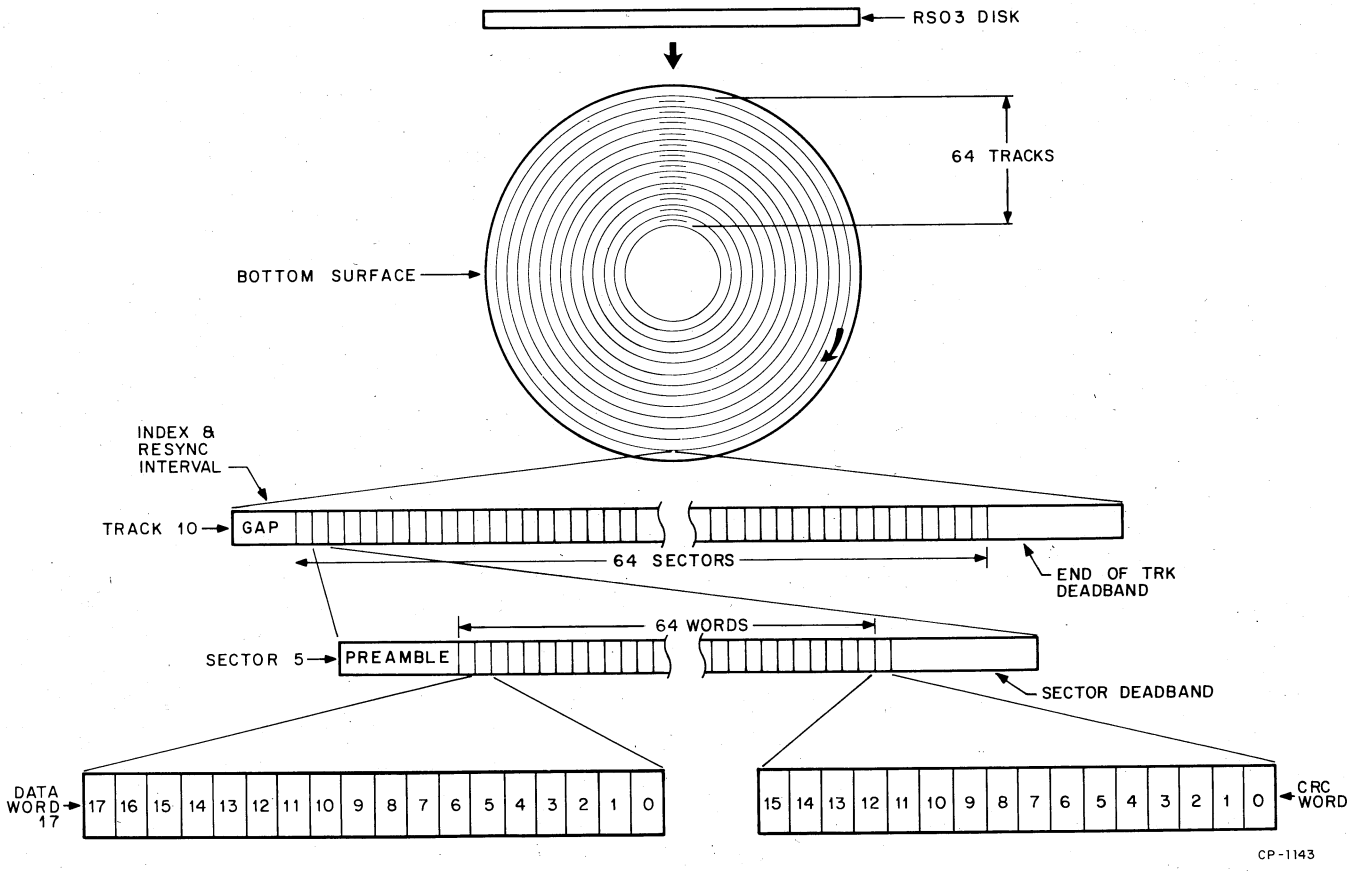

Figure 1-2 RS03 Data Track Format Schematic Diagram

1.1.4 Data Format

The bottom surface of the disk is utilized in the RS03. Ten head block assemblies (shoes) of 8 ferrites (heads) per assembly are fixed in position across the bottom surface. As the disk rotates, these ferrites describe 80 tracks. Only 64 are utilized for data. One head block assembly is used as data track spares; the last one is used for the timing tracks. The actual physical track locations on the disk are illustrated in Figure 2-27 in Section 2.3, Mechanical Principles of Operation.

The lowest level of addressing in the RS03 is the sector. Complete sectors are always transferred between Controller and drive. The detailed format of an RS03 disk is illustrated and described in later sections of this manual. Figure 1-2 is a schematic representation of format organization.

The data track consists of a $250 \pm 50\,\mu s$ index gap, followed by a resync interval, during which the phase-locked loop resynchronizes to the timing track. The remaining data area is then sub-divided into 64 sectors with each sector containing a 64-word data block plus a 16-bit Cyclic Redundancy Check (CRC) word for error detection. At the beginning of each sector, a preamble is recorded, containing 67 – 70 zero bits and concluded by a Sync "1" bit. This is followed by 64 words of data. (If the number of data words to be written in any sector is less than 64, the remaining word positions of that sector are zero-filled by the Controller.) The CRC word is then written immediately after the data block of each sector. Finally, there are 95 to 98 bits of sector deadband.

1.2 SPECIFICATIONS

A list of RS03 characteristics is given in Table 1-1.

1.3 MAJOR SUBASSEMBLIES

The RS03 can be subdivided into three major subassemblies: The Head/Disk Subassembly contains the heads, the disk, the spindle/motor, and the air filter system; the Logic Subassembly comprises all the analog and digital electronics necessary for drive control and data processing; and the Power Supply/Control Subassembly controls ac power to the disk and blower motors and supplies the dc voltages necessary to run the disk file (Figure 1-3).

1.3.1 Head/Disk Subassembly

The Head/Disk Subassembly is composed of the disk cover and lower head casting, a 16-in. NiCo-plated recording disk, a blower motor, the spindle/motor, an Absolute® filter, and 10 head block assemblies (shoes). Each head block assembly contains 8 individual read/write heads (ferrites). All head blocks have been pre-adjusted such that when the disk is rotating, the heads will fly 55 microinches from the surface of the disk. When the disk is not rotating, the heads rest on the surfaces of the disk.

The disk is driven by a 50/60 Hz integral ac induction motor/spindle.

1.3.2 Logic Subassembly

The Logic Subassembly contains 17 printed circuit modules, located in the front of the drive cabinet. This subassembly is attached to slides which pull out from the drive cabinet as shown in Figure 1-3.

1.3.3 Power Supply/Control Subassembly

The Power Supply/Control Subassembly is mounted in the lower-rear portion of the RS03 cabinet (Figure 1-3) and is removable as a unit. It contains all of the electronic components necessary for generation of the operational voltages for the drive.

The linear type dc power supply regulator operates from a ferroresonant transformer to supply +5 Vdc @ 9 A, +20 Vdc @ 1 A, and −20 Vdc @ 1.5 A. All three of these output voltages are over-current protected; in addition, the +5 Vdc output is over-voltage protected.

The power control system distributes and controls all ac power within the drive. This system is controlled by the mode switch and can be operated in either REMOTE, LOCAL, or OFF mode.

In REMOTE mode, logic signals from two power buses are used to control individual drive power, as well as power sequencing along the daisy chain that connects all drives. In LOCAL mode, the individual drive power system is removed from power bus control and is operated directly by the MODE switch. In OFF mode, only the dc power supply is shut down. If the disk drive motor, blower motor, and fan are operating when this mode is selected, they will continue to operate and can only be stopped by manually tripping the main circuit breaker or by unplugging the ac line cord. If the disk drive motor, blower motor, and fan are not operating when this mode is selected, they cannot be started with logic signals on the power bus.

®Absolute is registered trademark of Cambridge Filter Corporation.

Table 1-1
RS03 Performance Specifications

Characteristic	Parameter
Model Designation	
RS03-AA	90–132 Vac @ 60 Hz
RS03-AB	180–264 Vac @ 60 Hz
RS03-AC	90–132 Vac @ 50 Hz
RS03-AD	180–264 Vac @ 50 Hz
Power Requirements (ac)	
Input Voltage	90–132 Vac @ 50/60 Hz 180–264 Vac @ 50/60 Hz
Starting Current	13 A @ 90–132 Vac 6 A @ 180–264 Vac
Operating Current	6 A @ 90–132 Vac 3 A @ 180–264 Vac
Dimensions and Weight	
Height	15-3/4 in. (400 mm)
Width	19 in. (482.6 mm)
Depth	26-1/4 in. (665 mm)
Weight	120 lbs (54.4 kg) (uncrated)
Operating Environment	
Temperature	50° to 104° F (10° to 40° C)
Humidity	RH 10% to 90%; max wet bulb 82° F (22° C); min dewpoint 36° F (2° C).
Vibration	5–50 Hz 0.004 in. DA 50–500 Hz .5 g vertical.
Shock	5 g, half sine, 10 ms duration, any plane.
Altitude	8000 ft (2438 m)
Storage Environment	
Temperature	150° F max
Humidity	85° F max wet bulb, 80% R.H.
Vibration	*Vertical* – 1.4 g, 10–300 Hz. Acceleration spectral density .029 g^2/Hz from 10–50 Hz with 8 db/oct rolloff from 50–300 Hz *Horizontal* – 0.68 g, 10–200 Hz. Acceleration spectral density .007 g^2/Hz from 10–50 Hz with 8 db/oct rolloff from 50–200 Hz. *Shock* – 20 g, half sine, 30 ± 10 ms duration, vertical. *Altitude* – 30,000 ft (9144 m)

Table 1-1 (Cont)
RS03 Performance Specifications

Characteristic	Parameter	
Storage Medium		
Type	16 in., NiCo-plated, magnetic disk	
Method	One surface, fixed head, sector interleaving optional	
Recording Technique	Miller Encoded (MFM)	
Capacity (each disk)	262,144 words max.	
Format	18 bits/word 64 words/sector 64 sectors/track 64 tracks/disk	
Words/Logical Track	4092	
Spare Tracks	8 data spares 4 guaranteed to customer 1 timing spare	
Error Detection	16-bit CRC per sector	
Bit Error Rate		
Recoverable Data Errors	< 1 in 10^{11} bits transferred	
Unrecoverable Data Errors	< 1 in 10^{12} bits transferred	
Access Times	**60 Hz**	**50 Hz**
Minimum	6.4 μs	7.7 μs
Typical	8.5 ms	10.2 ms
Maximum	17.0 ms	20.4 ms
Transfer Rates (average)		
Non-interleaved	4 μs/18-bit word	
Interleaved	8 μs/18-bit word (jumper removed)	
Interface Signals		
Logic Levels		
Input to MASSBUS transmitters	True = 0 V, False = +3 V	
Output from MASSBUS receivers	True = +3 V, False = 0 V	
Write Lock Out	Selectable from track "0" to selected track.	
MTBF (calculated)	4700 hours	

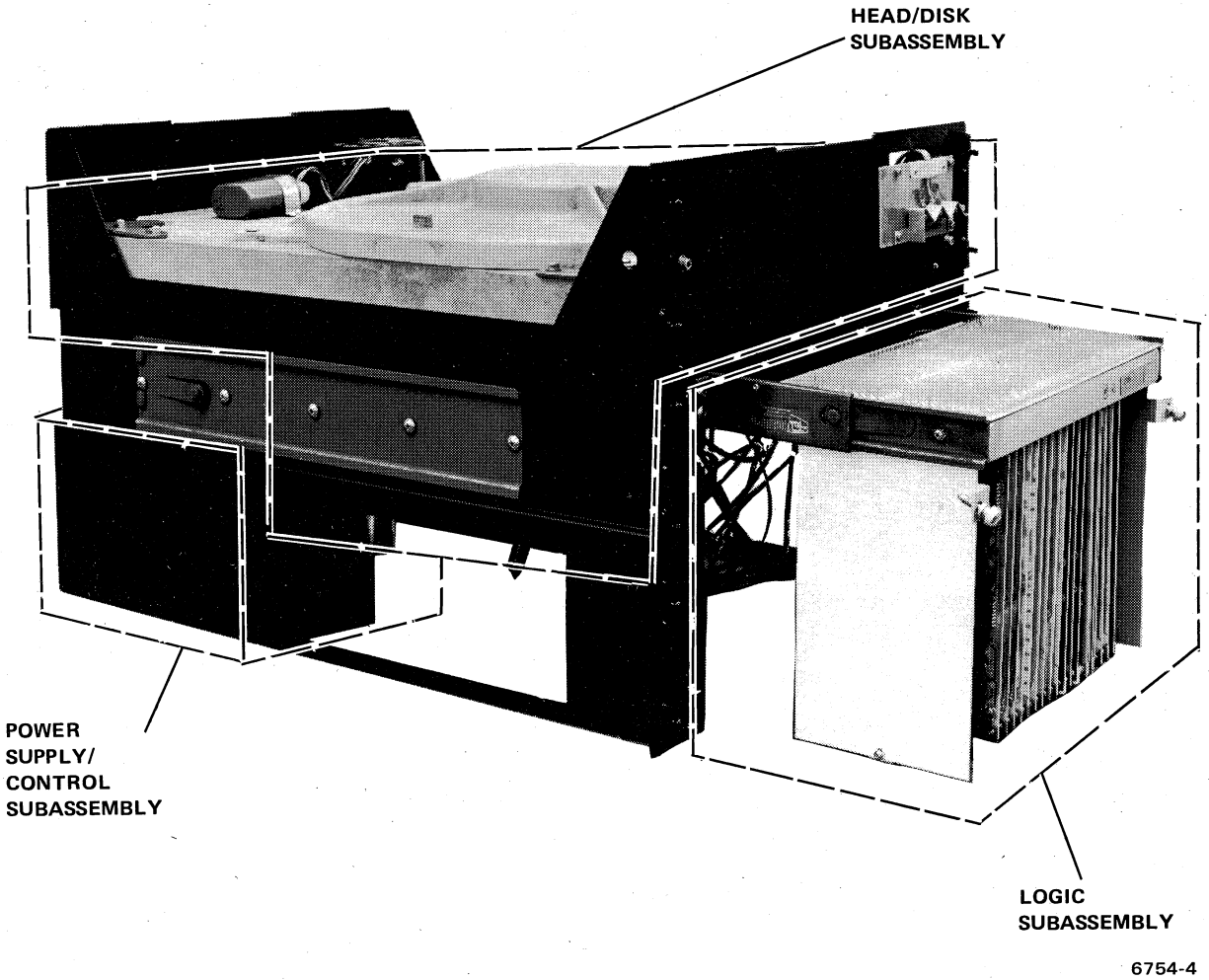

Figure 1-3 Major Subassembly Locations

1.4 RS03 CONTROLS AND INDICATORS

The RS03 controls and indicators are divided into five areas on the equipment.

Figure 1-4 illustrates the power supply/control section controls and indicators located on the rear of the unit; Table 1-2 lists their functions.

Figure 1-5 shows the front panel indicators that are described in Table 1-3.

The error indicators are shown in Figure 1-6 and correspond to each of the bits in the Error register. Table 1-4 defines the 3-letter mnemonic associated with each LED indicator. These indicators are located on Module M7770 in slot AB8 of the logic subassembly. Access to these indicators is gained by removing the lower-front panel from the unit; the LEDs are mounted on the front-edge of the module. The front panel ERROR indicator is the OR of all the error indicators.

Figure 1-7 illustrates the Write Lock Address switches, located on Module M7754 in slot AB10 of the logic subassembly. One switch enables this feature; the others are set to the highest octal track address which will be locked out. All tracks, from zero up to and including the switch-set address, are write-protected.

Figure 1-8 illustrates the Unit Number select switches, located on Module M7755 in slot AB07 of the logic subassembly. Numbers 1, 2, and 4 designate the binary weight of each switch in determining the desired unit number.

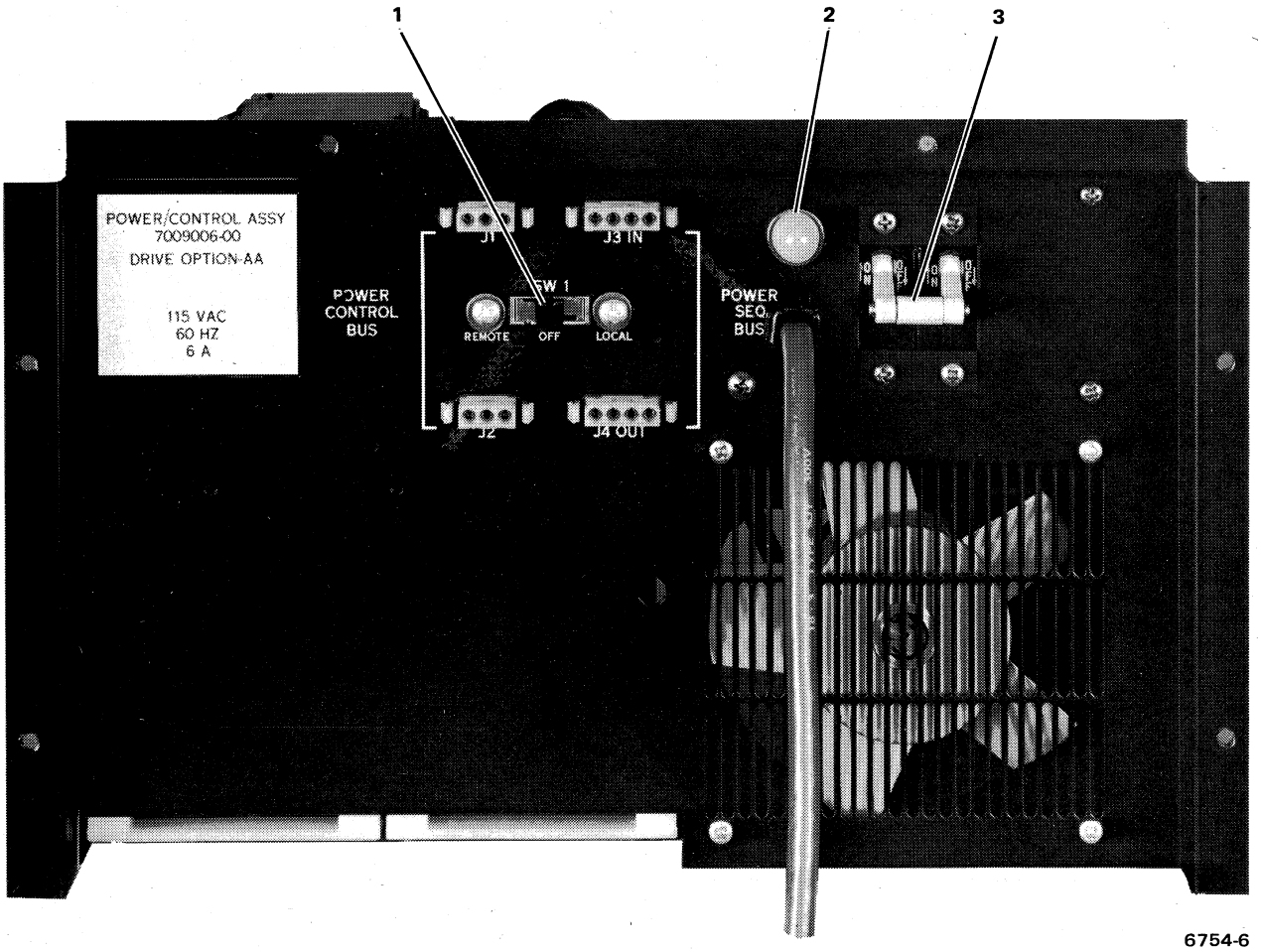

Figure 1-4 Power Controls and Indicators

Table 1-2
Power Controls and Indicators

Index No.	Panel Marking	Function
1	SW1	Power Control System Mode switch. In REMOTE position, allows the drive to be powered in accordance with the Power Sequence Bus and Power Control Bus requirements. In LOCAL position, allows the drive to be run independent of the Power Sequence and Control Buses. In OFF position, shuts off dc and inhibits starting of the drive.
2	(none)	Power indicator. Lights whenever ac voltage is present anywhere in the drive.
3	(none)	Main breaker. Controls all ac power in the drive and breaks both sides of the line in the event of malfunction.

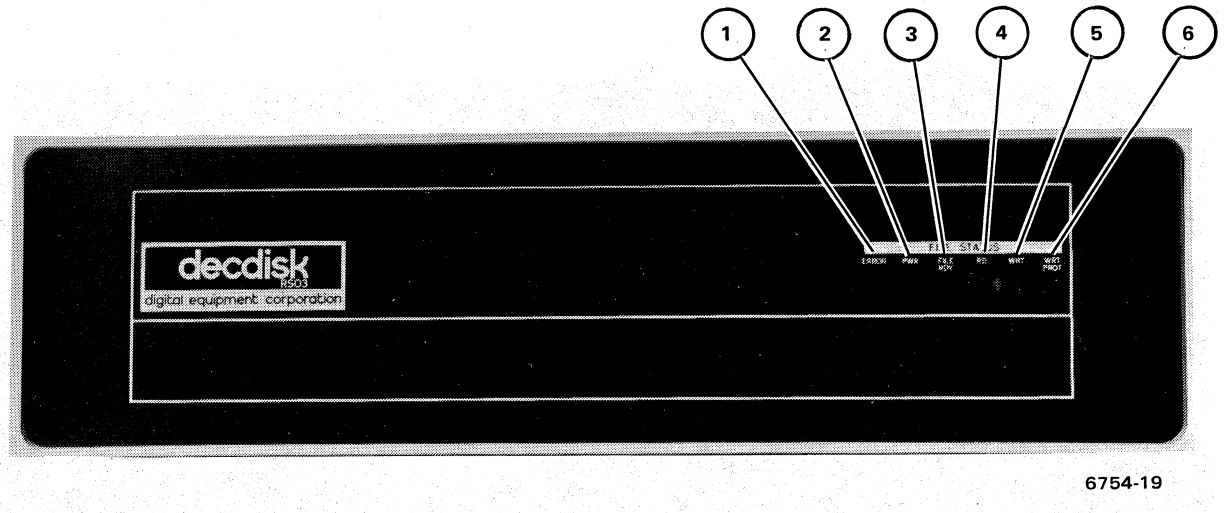

Figure 1-5 Front Panel Indicators

Table 1-3
Front Panel File Status Indicators

Index No.	Panel Marking	Function
1	ERROR	Lights when any drive error is detected; specific error is indicated in Table 1-4. Remains lit until the Controller issues a Drive Clear or Initialize command, or writes all 0s into the Error register.
2	PWR	Lights when operating power (ac and dc) is present; extinguishes when any operating power is not present.
3	FILE RDY	Lights when the disk is rotating at the correct speed and the drive is ready to perform a program-controlled operation; extinguishes while the drive is performing a program-controlled operation.
4	RD	Lights only when a Read or Write-Check command is being executed.
5	WRT	Lights only when a Write command is being executed.
6	WRT PROT	Lights whenever the address in the Desired Address register is write-protected, regardless of the drive operation.

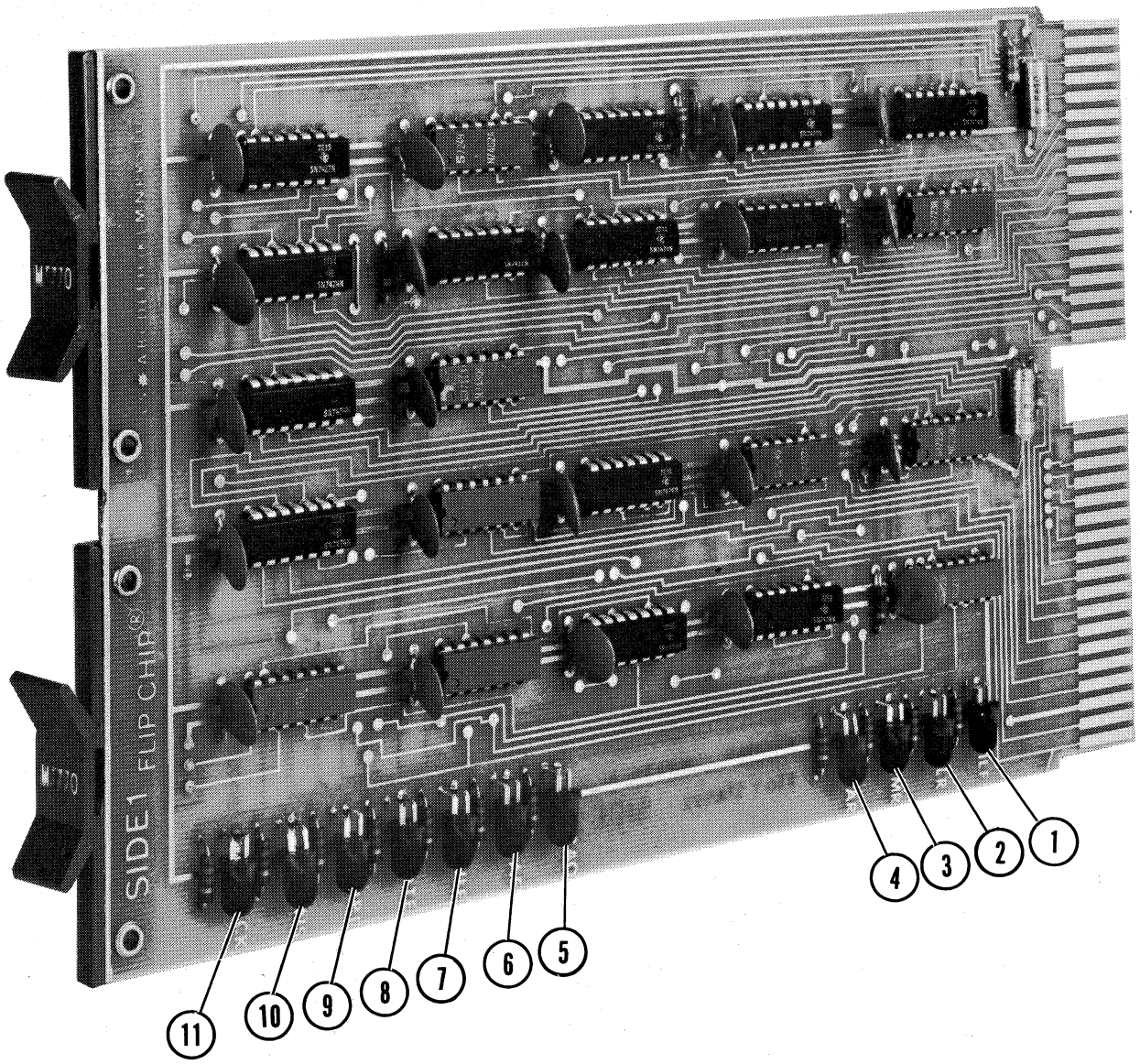

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Figure 1-6 Error Indicators

1.5 OPTIONS

There is one jumper-selectable option on the RS03, the Sector Address Interleave option. By removing jumper W1 on the G092 module, sectors are addressed in an interleaved sequence, i.e., physically sequential sectors do *not* have numerically consecutive addresses. Instead, *alternate* physical sectors have consecutive addresses (Figure 1-9). When this option is installed, a 250 μs gap is provided between any two numerically consecutive sectors, effectively doubling the time available to transfer one sector. For example, two disk revolutions (33.3 ms) are required to consecutively transfer a complete data track (4096 words) resulting in an 8 μs *average* word transfer rate.

Table 1-4
Error Indicators

Index No.	Module Label	Function
1	ILF	ILlegal Function Error
2	ILR	ILlegal Register Error
3	RMR	Register Modification Refused Error
4	PAR	MASSBUS PARity Error
5	AOE	Address Overflow Error
6	IAE	Invalid Address Error
7	WLE	Write Lock Error
8	DTE	Drive Timing Error
9	OPI	OPeration Incomplete Error
10	UNS	UNSafe Error
11	DCK	Data ChecK Error

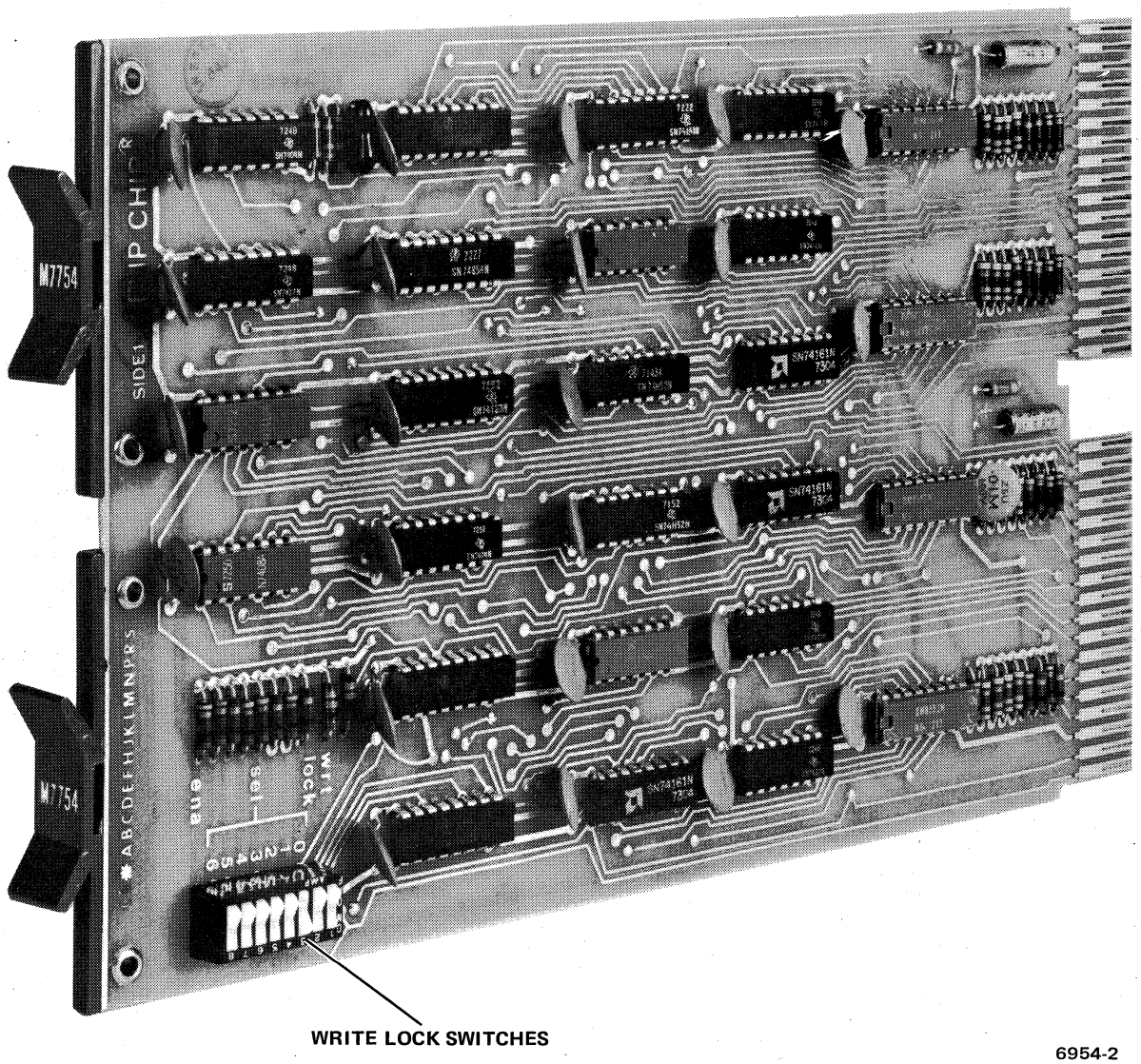

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Figure 1-7 RS03 Write Lock Protect Address Switches

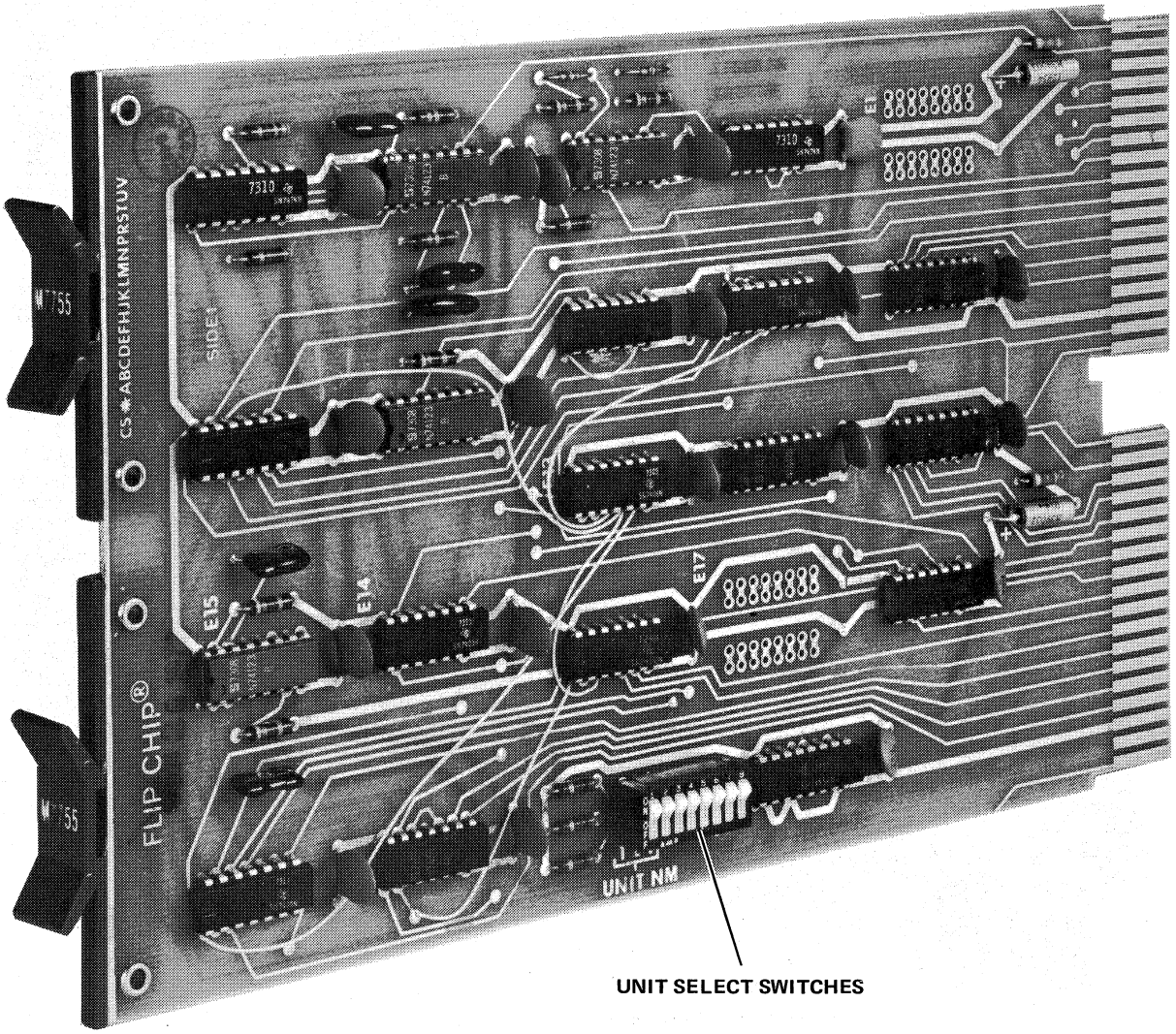

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Figure 1-8 RS03 Unit Select Switches

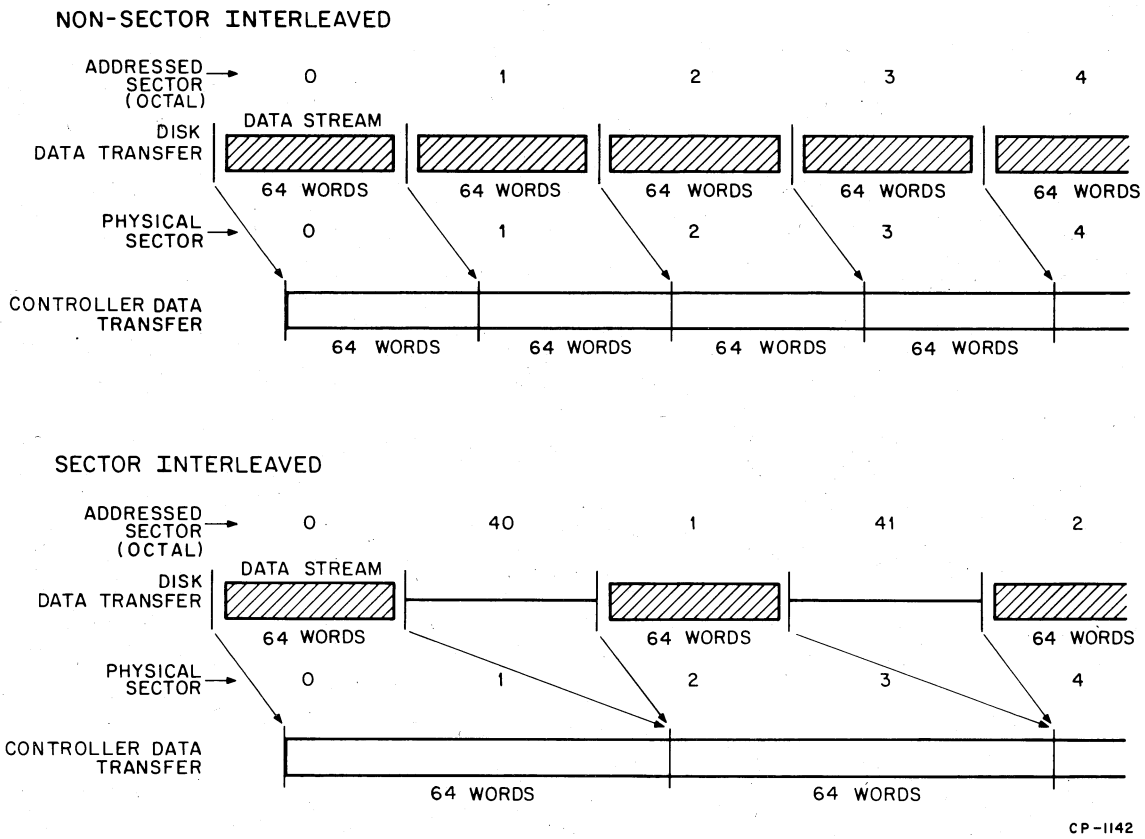

Figure 1-9 Effect of Sector Interleaving On RS03 Transfer Rate

SECTION 2
THEORY OF OPERATION

2.1 GENERAL

This section contains a theoretical discussion of the RS03. It describes the three major areas of the disk drive, electrical, mechanical, and magnetic, on a functional block diagram level. Detailed logic descriptions of modules are found in Section III – Electrical Servicing; detailed mechanical servicing and maintenance discussions are found in Section IV – Mechanical Servicing.

2.2 ELECTRICAL PRINCIPLES OF OPERATION

Subsection 2.2 discusses the electrical and electronic principles involved in the operation of the RS03.

2.2.1 MASSBUS Interface

The RS03 is a MASSBUS peripheral and communicates with the MASSBUS Controller via the MASSBUS. The MASSBUS is composed of two separate, independent buses, capable of conducting two different types of communication simultaneously: the asynchronous Control Bus and the synchronous Data Bus (Figure 2-1).

The *Control Bus* communicates with the drive registers. Its signals are defined as follows:

Control and Status (C(00:15)) – These bidirectional lines transmit 16 parallel control or status bits to or from the drive.

Control Bus Parity (CPA) – This bidirectional line transmits an odd Control Bus parity bit to or from the drive. Control parity is simultaneously transmitted with the data on the Control Bus.

Drive Select (DS(0:2)) – These three lines transmit a 3-bit binary code from the Controller to select one drive from up to eight drives.

Register Select (RS(0:4)) – These five lines transmit a 5-bit binary code from the Controller to select one of the following eight drive registers:

00_8 – Control Register
01_8 – Status Register
02_8 – Error Register
03_8 – Maintenance Register
04_8 – Attention Summary Register
05_8 – Desired Address Register
06_8 – Drive Type Register
07_8 – Look-Ahead Register

NOTE

The two most significant bits (RS 3 and 4) are not used in the RS03. If either of these lines is asserted, an Illegal Register Error occurs.

Controller To Drive (CTOD) – This line transmits the signal from the Controller to indicate in which direction information is to be transferred on the Control Bus. For a Controller-to-drive transfer, the Controller asserts CTOD; for a drive-to-Controller transfer, the Controller negates CTOD.

Demand (DEM) – This line transmits the signal from the Controller to initiate a Control Bus transfer.

Transfer (TRA) – This line transmits the signal TRA from the drive in response to DEM. For a Controller-to-drive transfer, TRA is asserted after the data is strobed; for a drive-to-Controller transfer, TRA is asserted after the data is asserted on the Control Bus. TRA is negated when the Controller negates DEM.

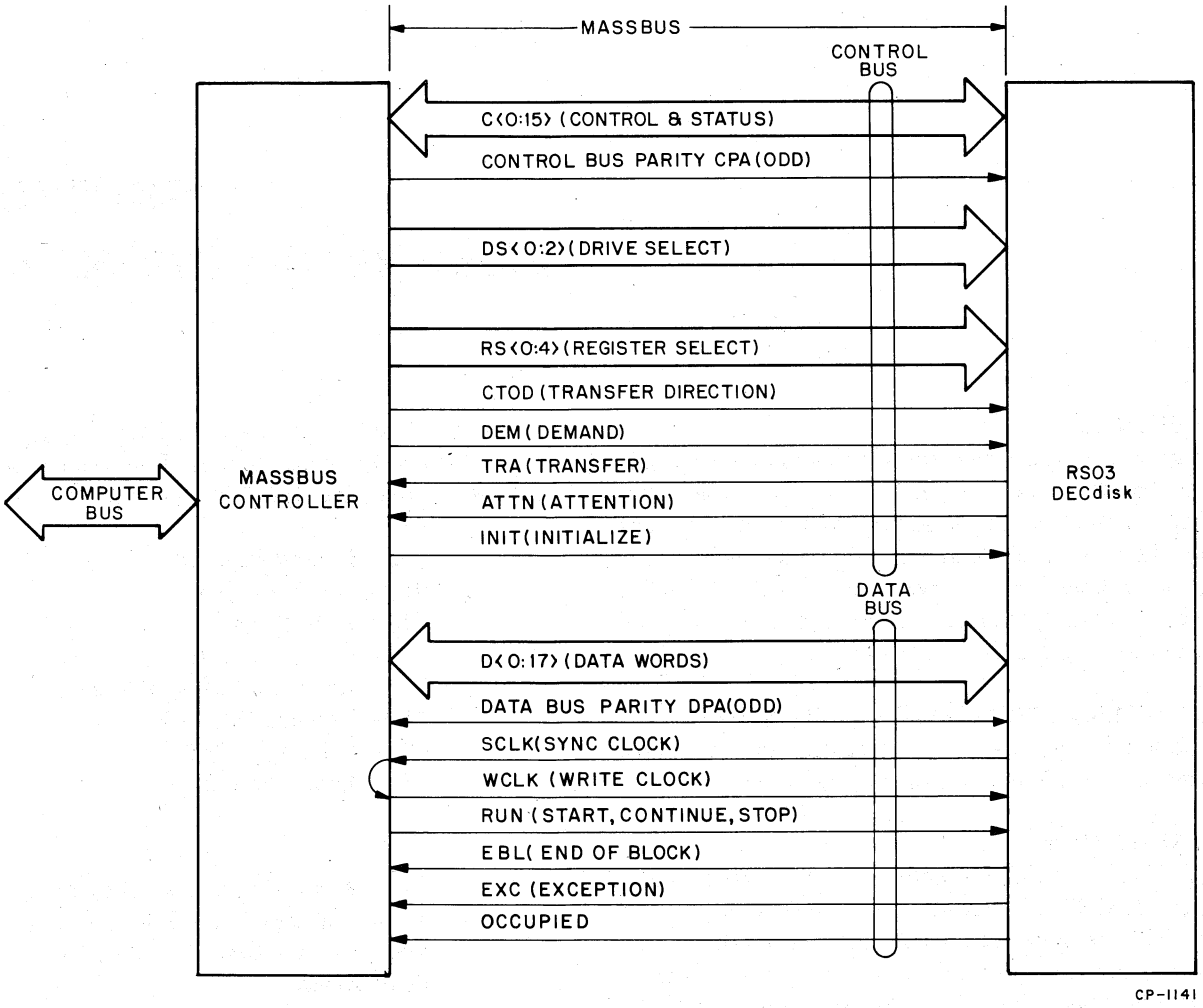

Figure 2-1 MASSBUS Configuration

Attention (ATTN) – The drive asserts this line to signal the Controller of any change in drive status. It is asserted any time a drive's ATA status bit is set. ATTN is common to all drives on the MASSBUS and may be asserted by more than one drive at a time.

Initialize (INIT) – This line transmits the signal INIT from the Controller to initialize all drives on the MASSBUS. This signal is transmitted at system start-up or whenever the Controller issues an Initialize command.

Mass Fail – This line transmits the signal MASS FAIL from the Controller whenever power fails in the Controller.

A typical Control Bus transmission is illustrated in Figure 2-2. In a Controller write operation into the RS03 registers, the Controller asserts the C lines with the register data to be transferred. The Controller also asserts the DS lines (to specify one drive), the RS lines (to specify the register to which the data must be transferred), and the CTOD line (to indicate that the direction of transfer is to the drive). After these signals have settled on the bus, the Controller asserts DEM to cause the drive to load the data on the C lines into the register addressed. When this is accomplished, the drive asserts TRA, informing the Controller that the register has been loaded. This causes the Controller to negate DEM. At the same time, the Controller negates the C, DS, RS, and CTOD lines. This is a typical transfer and illustrates what is referred to as a "handshake sequence" on the asynchronous Control Bus.

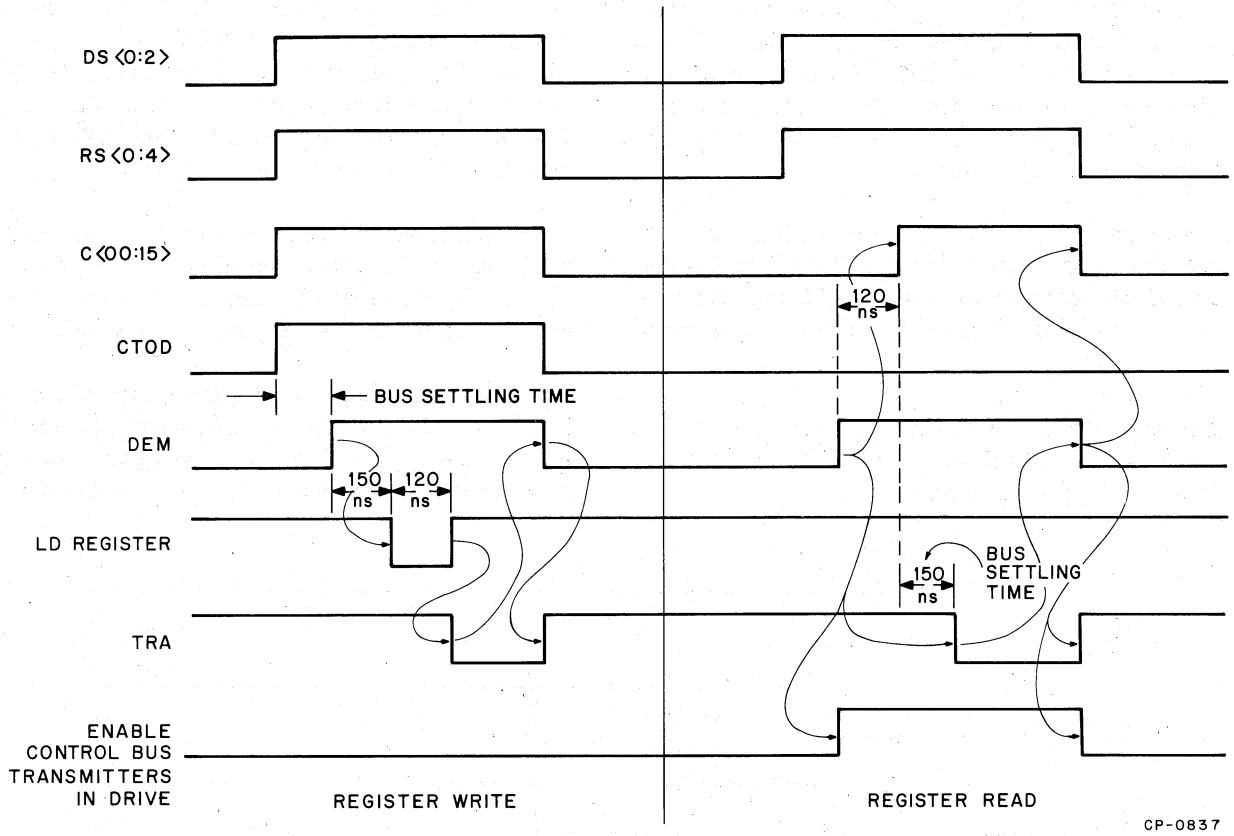

Figure 2-2 Typical RS03 Control Bus Transfer Timing

In a Controller read operation from the RS03 registers, the sequence is similar. The DS and RS lines are asserted by the Controller while the CTOD line is negated to indicate that the direction of transfer is from the drive. The Controller then asserts DEM, causing the drive to place the register data on the C lines. When the C lines have settled, the drive will assert TRA, causing the Controller to take the data from the C lines. The Controller then negates DEM, causing the RS03 to negate TRA and the C lines. This concludes the transfer operation.

The *Data Bus* lines are defined as follows:

Data Words (D(00:17)) – These bidirectional lines transmit 18 parallel data bits to or from the drive.

Data Bus Parity (DPA) – This bidirectional line transmits an odd Data Bus parity bit to or from the drive. Data parity is simultaneously transmitted with the bits on the Data Bus.

Sync Clock (SCLK) – During a read operation, this line transmits the signal SCLK from the drive to indicate when data on the Data Bus is to be strobed by the Controller. During a write operation, this line transmits SCLK to the Controller to indicate the rate at which data should be presented on the Data Bus.

Write Clock (WCLK) – This line transmits the signal WCLK from the Controller indicating when data to be written is to be strobed.

Run (RUN) – This line transmits the signal RUN from the Controller to initiate data transfer command execution. During a data transfer, the drive samples RUN at the end of each sector. If RUN is still asserted, the drive continues the data transfer into the next sector; if RUN is negated at this time, the drive terminates the data transfer.

End of Block (EBL) – This line normally transmits the signal EBL from the drive at the end of each sector during a data transfer. However, for certain abnormal conditions where it is necessary to terminate the data transfer immediately, EBL is asserted prior to the end of the sector.

Exception (EXC) – This bidirectional line transmits the signal EXC from the drive during a data transfer to indicate that an error has occurred. EXC can also be asserted by the Controller to abort an in-progress data transfer.

Occupied (OCC) – This line indicates to the Controller that the drive has accepted and recognized a valid data transfer command.

Figure 2-3 shows the typical timing of the Data Bus signals. To execute a Read command, the Controller first sets the address on the disk from which it wishes to read, and sets a read function. It then asserts the RUN line which causes the drive to search for the specified address. When the drive finds that address, transfer of data begins.

Synchronization of data transfer over the Data Bus originates in the drive, regardless of the direction of transfer. In this particular case, the drive places the first word on the D lines with the assertion of Sync Clock.

The Controller interprets the leading edge of the clock to signify that data has been put on D(00:17) and uses the trailing edge of that same clock to sample the data and place it into its data buffer. On the next leading edge of

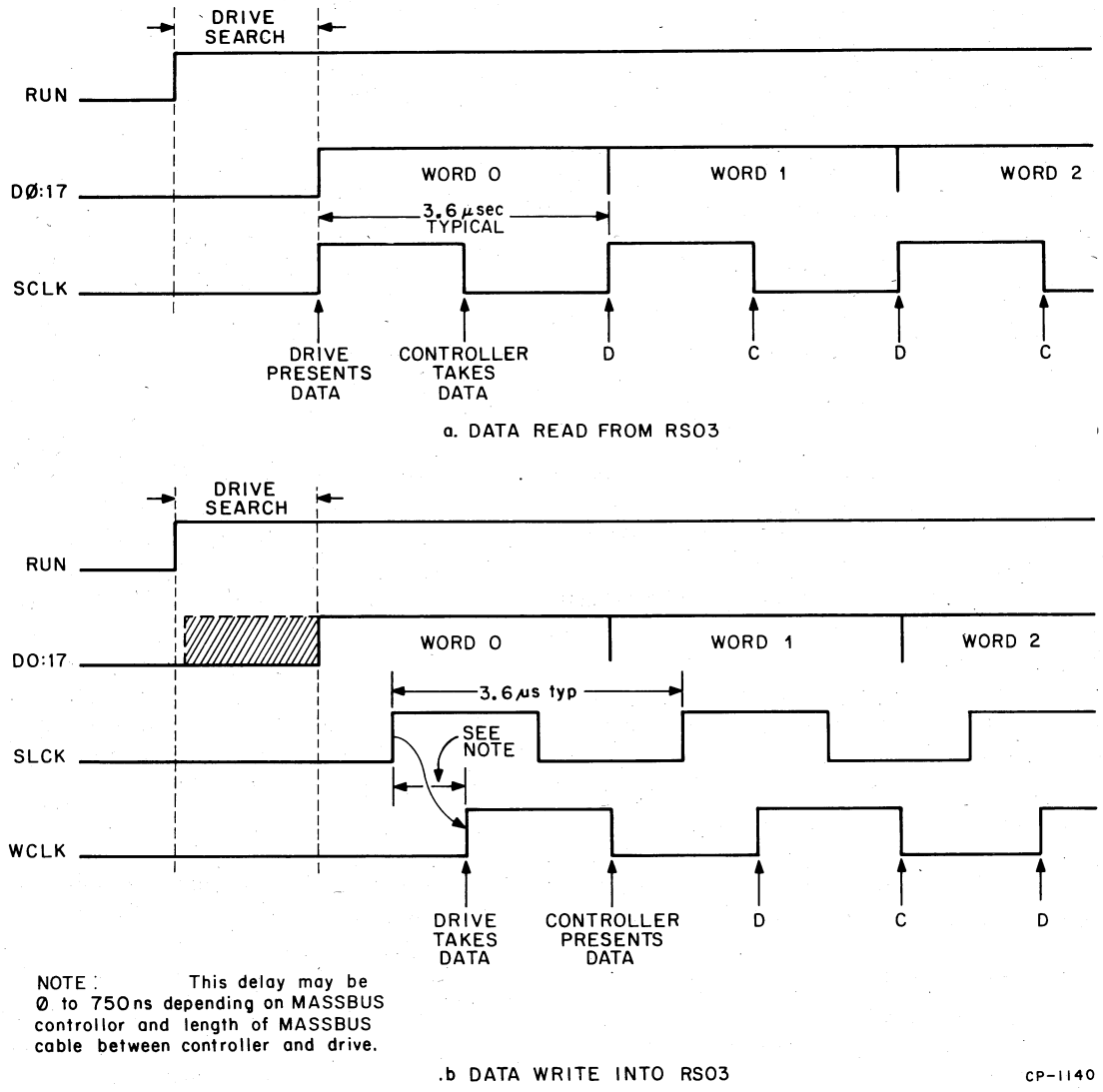

Figure 2-3 Data Bus Transfer Timing

Sync Clock, the drive places the next data word on the bus, and on that trailing edge, the Controller takes it off. This continues for complete sectors as long as RUN is asserted. The drive samples the state of RUN at the end of each sector and continues transferring complete sectors until the negation of RUN is detected.

To execute a Write command, the sequence is similar. The desired address is set in the drive and then a write function is set. The assertion of RUN initiates an address search operation, and when the desired sector is found, the drive begins issuing SCLKs. These SCLKs are "echoed" back to the drive by the Controller as WCLKs. On the leading edge of WCLK, the drive strobes D(00:17) into its data buffer. On the trailing edge, the Controller will present another word on D(00:17). At the end of each sector the drive samples RUN, and if it is negated, terminates the data transfer.

EBL is normally asserted by the drive at the end of each sector transferred, for both reads and writes. It is asserted immediately after the last word of the sector is transferred and is typically one word-time or 3.6 μs in duration. In this case, EBL indicates that a decision point has been reached – whether to continue or to terminate the current data transfer. The decision is based on the state of RUN at the trailing edge of EBL. Under certain conditions, EBL may be asserted prior to the end of a sector; these conditions will be discussed in the next paragraph and in the discussion of the Error register.

Under certain unusual circumstances, the Controller may need to terminate a data transfer prior to the end of the current sector. In such a case, the Controller asserts EXC, which is recognized only by the drive transferring data, causing that drive to assert EBL immediately and to terminate the data transfer.

EXC is asserted by the drive to indicate to the Controller that an error condition has occurred during a data transfer.

2.2.2 RS03 Logical Block Diagram

Figure 2-4 is a functional block diagram of the RS03. The drawing can be divided in half, with the top half representing all the logic associated with the Control Bus, and the bottom half showing all the logic associated with the Data Bus. Note that the dashed blocks represent individual modules and that each individual module contains complete functional elements.

The *MASSBUS Transceiver* modules are represented by the block on the left-hand edge of Figure 2-4. All of the MASSBUS signals are distributed among the three M5903 modules, located in slots AB04, AB05, and AB06 of the logic subassembly. The purpose of the transceivers is to interface between the differential signal levels present on the MASSBUS and the TTL logic signal levels utilized within the RS03.

MASSBUS Control Bus lines (Figure 2-4, top-left) are brought into an M7755 Control module, located in slot AB07 of the Logic Subassembly. Here the Drive Select lines are compared to the locally-set Drive Select switches to yield the signal SELECTED. This signal is then used to enable the Control Bus Handshake and Register Control section of this logic. The Register Control section then enables the Register Select logic to decode the MASSBUS Register Select lines for the register to be addressed and uses CTOD to determine whether the register is to be written or read. Note that an error signal can be produced from the Register Select block (1) if a register write is decoded while the drive is performing a Search or data transfer function or (2) if a non-existent register is addressed.

As can be seen from the block diagram, the inputs to the Control, Attention Summary, Maintenance, Error, and Desired Address registers (as well as the Control Bus Parity Check logic), are the Control Bus lines (C(00:15)). Inside the drive, these signals are designated WO DCB(00:15) (Wired-OR Drive Control Bus). The Drive Control Bus is driven by either the MASSBUS transceivers or by the Output Buffer.

The purpose of the Output Buffer is to freeze the contents of a readable register while it is being read by the Controller.

The input to the Output Buffer is a wired-OR bus of all drive registers, designated WO BO(00:15) (Wired-OR Bus Out).

Figure 2-5 shows a functional representation of the register data paths. The MASSBUS transceivers, shown as a single block, are represented at the top of Figure 2-5, where they tie to the MASSBUS C lines. The transmitters have a TTL input and a differential output, while the receivers are differential in and TTL out. Either transmitters *or* receivers on the Control Bus are enabled at any one time, never both.

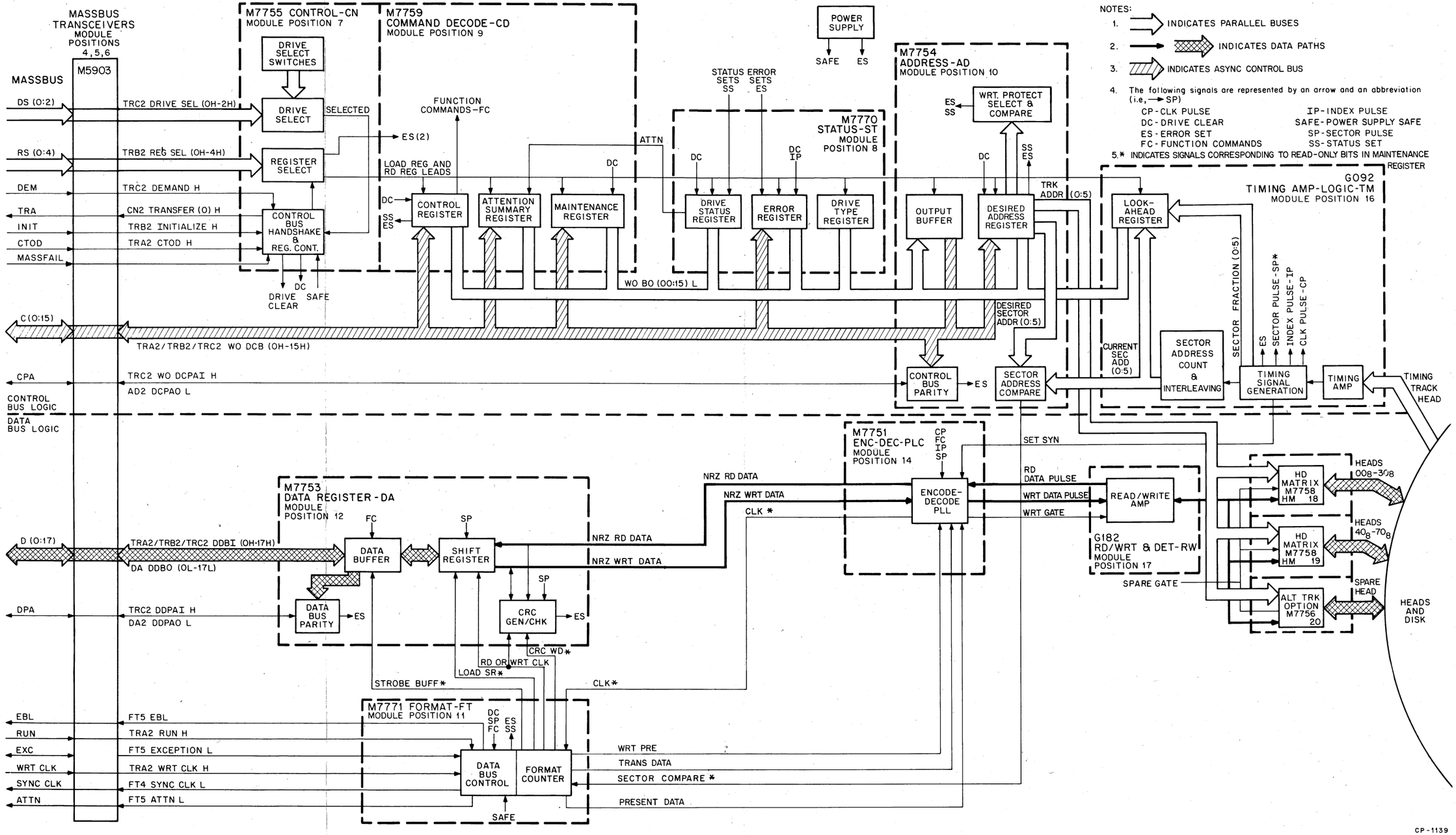

Figure 2-4 RS03 Logical Block Diagram

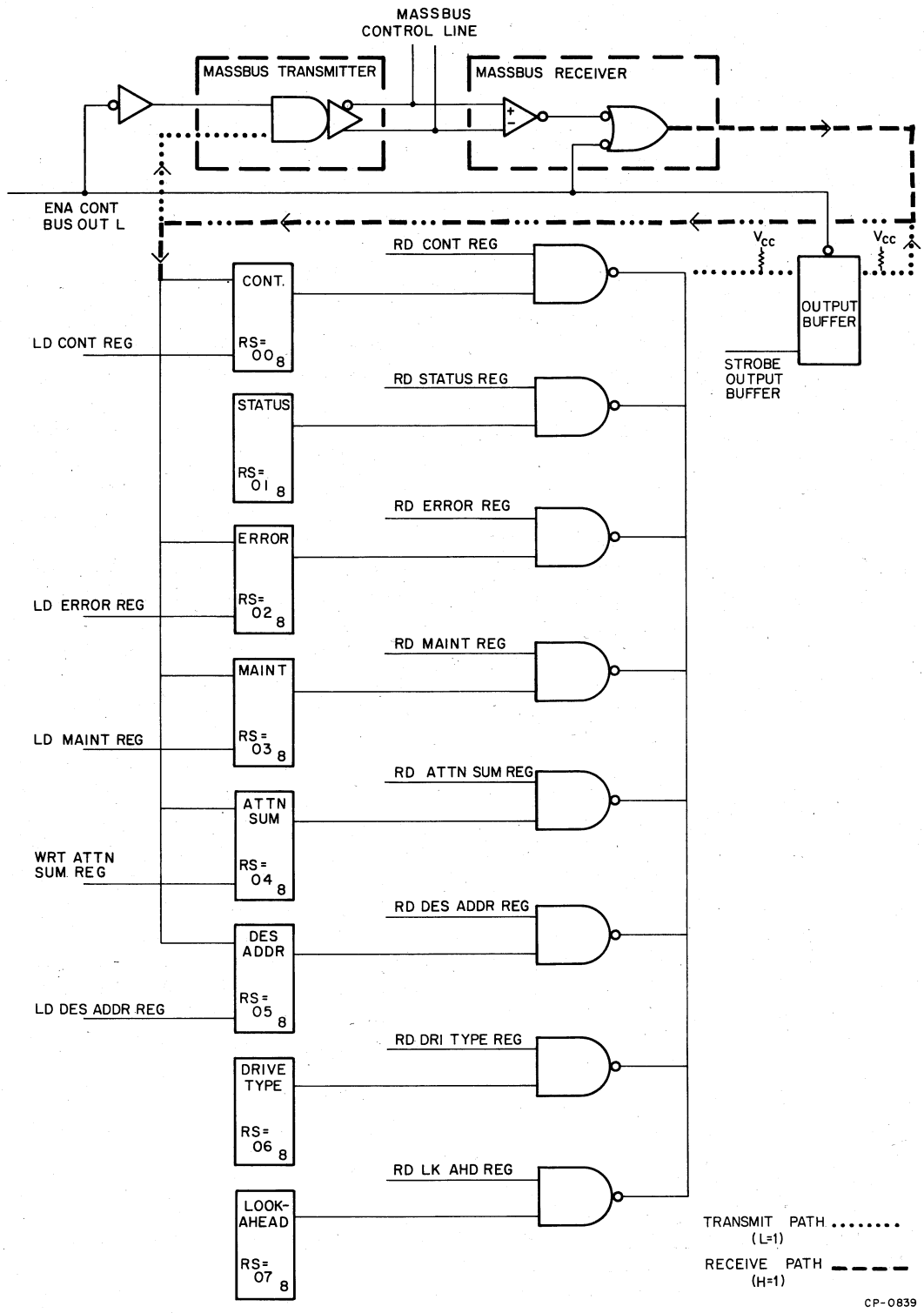

Figure 2-5 Functional Representation of Register Data Paths. (One Bit)

Normally, the receivers are enabled and data is received continuously, loading or writing any register that is selected; but when it is desired to read from some register, the ENA CONT BUS OUT signal is used to disable the receivers, and to enable both the transmitters and the Output Buffer. The contents of the selected register are gated to the input of the Output Buffer by the appropriate Register read control signal and transmitted to the MASSBUS C lines via the Output Buffer.

To perform any program-controlled drive operation, a drive must first be selected and then an operational command must be written into that drive's Control register. To accomplish this, the Controller places a 3-bit drive unit number code on the Drive Select lines, places the 5-bit Control register select code (00_8) on the Register Select lines, places the operational command on the Control Bus, and asserts CTOD.

After these signals have settled on the interface lines, the Controller asserts DEM to initiate the "handshake" operation. If the configuration of the drive's unit number switches corresponds to the Drive Select code received from the Controller, the drive control logic is enabled and the Control Bus is checked for correct parity.

At this point, a check is also made to ensure that the drive is not already performing a Search or a data transfer function. If one of these operations is in progress, a Register Modification Refused (RMR) error is generated and the command is not written into the Control register. If none of these operations is in progress, the command is written into the Control register. In any case, the signal TRA is always transmitted from the drive to complete the "handshake". When the Controller receives this signal, it negates DEM; when the drive receives DEM negation, it negates TRA.

To determine which operation a particular drive is currently performing, it is possible to read from that drive's Control register without interrupting an in-progress drive operation. To accomplish this, the Controller performs a Control register "handshake" with signal CTOD negated. Negation of CTOD inhibits the RMR and Control Bus Parity checks, while allowing a non-destructive readout from the Control register (current operational command) to the drive Output Buffer. The Output Buffer is then transferred to the Controller via the Control Bus. Thus, while the Controller is sampling the bus, the C lines remain stable.

Writing into and reading out of the rest of the drive registers is similar; the same handshake sequence must be performed. If a non-existent register is selected, an Illegal Register (ILR) error is generated. As with the Control register, when a write is attempted into the Error or Desired Address register when a Search or data transfer function is underway, an RMR error is generated and the register is not modified. If this is not the case, the data on the Control Bus is checked for correct parity and then written into the selected register.

If a *Control Bus Parity Error* is detected by the drive during a register write, the Parity Error bit in the Error register is set. With one exception, the contents of WO DCB(00:15) are strobed into the selected register as usual. The *exception* is when writing into the Control register and a Control Bus Parity Error is detected, *bit 0 of the Control register* (GO bit) *is prevented from setting.* This prevents performing a potentially invalid or erroneous command.

The *Drive registers* that store the drive status information, simulate various signals from the disk during maintenance mode operation, and control the logical operation of the drive, are listed in Table 2-1 with their Register Select addresses, type, and function. A composite diagram of all drive registers is shown in Figure 2-6.

The *Control register* is part of the Command Decode module (M7759) located in slot AB09. It receives command function codes from the Controller via the Control Bus. When a non data-transfer code with a one in the GO bit position (bit 0) is written into this register, command execution is automatically initiated within the drive. For example, if the command 31_8 is written into the Control register, a Search function is initiated. However, if a data transfer code (either 51_8, 61_8, or 71_8) is written, the drive must first receive the assertion of RUN from the Controller before command execution can occur.

Figure 2-7 illustrates the Control register format and Table 2-2 lists the valid command function codes. If a command (with a function code and GO bit set) other than those indicated in this table is transmitted to the drive, the command is loaded into the Control register in the normal fashion, but an Illegal Function (ILF) error is generated.

Note that functionally the GO bit is a part of the Function Code and that bit 11 is always read as a 1. The remaining bits (0s) are either spares or reserved for Controller use. In other words, these bits (6–10), (12–15) are always 0 at the drive.

Table 2-1
Drive Registers

RS (0:4) Register Select Code (octal)	Name	Type	Function
00	Control	Read/Write	Contains the function code and GO bit.
01	Status	Read only	Contains all non-error status information plus the Error Summary bit.
02	Error	Read/Write	Contains error indications.
03	Maintenance	Read/Write	Controls diagnostic functions.
04	Attention Summary	Read/Write	Indicates the Attention Active status of each drive (one bit/drive).
05	Desired Address	Read/Write	Contains the address of the desired track and sector.
06	Drive Type	Read only	Indicates the type of drive (i.e., fixed-head, sector addressed, single port, RS03).
07	Look Ahead	Read only	Specifies the head position within the current sector.

The *Status register* is part of the Status module (M7770) located in slot AB08. This is a read-only register that contains all the drive non-error status indicators. Figure 2-8 illustrates the Status register format and Table 2-3 defines the bit positions.

The *Error register* is part of the Status module (M7770) located in slot AB08. This read/write register stores all of the 11 drive error conditions that can be detected in the drive. Although its output can be read by the Controller at any time, the Controller can only write into this register when the drive is not performing a Search or data transfer function, i.e., when GO is negated.

In the RS03 drive, there are two classifications of error: Class A and Class B. Class A errors, such as a Register Modification Refused error, do not destroy any previously-recorded data. Class B errors, such as power failure, are more significant errors because they could destroy previously-recorded data if they were not handled properly. By immediately terminating any data transfer, loss of data is prevented if a Class B error occurs.

When any error occurs, the drive determines the class of error (Class A or Class B) and the following events occur:

a. The appropriate bit in the Error register is set.
b. The appropriate LED on the Status module lights.
c. The ERROR lamp on the drive front panel lights.

If an error of either class occurs when a data transfer is *not* in progress, ATTN is immediately asserted.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RS03 CONTROL	0	0	0	0	1	0	0	0	0	0	F4	F3	F2	F1	F0	GO	00
											FUNCTION CODE						
STATUS REG. DS	ATA	ERR	PIP	MOL	WRL	LBT	0	DPR	DRY	0	0	0	0	0	0	0	01
ERROR REG. ER	DCK	UNS	OPI	DTE	WLE	IAE	AOE	0	0	0	0	0	PAR	RMR	ILR	ILF	02
MAINT. REG. MR	SDCLK	Ø	CRCW	MWD B	SB	LSR	AC	SP	WRT	RD	Ø	MIND	MCLK	MRD B	0	DMD	03
ATTN. SUMMARY REG. AS	0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0	04
DES. ADDR. REG. DA	SP 3	SP 2	SP 1	SP 0	TA 5	TA 4	TA 3	TA 2	TA 1	TA 0	SA 5	SA 4	SA 3	SA 2	SA 1	SA 0	05
	SPARES				TRACK ADDRESS						SECTOR ADDRESS						
DRIVE TYPE REG. DT	NBA	TAP	MOH	0	DRQ	0	0	0	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0	06
									DRIVE TYPE								
LOOK AHEAD REG. LA	0	0	0	0	CS 5	CS 4	CS 3	CS 2	CS 1	CS 0	SF 5	SF 4	SF 3	SF 2	SF 1	SF 0	07
					CURRENT SECTOR						SECTOR FRACTION						

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Figure 2-6 RS03 Drive Register Summary

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RS03 CONTROL	0	0	0	0	1	0	0	0	0	0	F4	F3	F2	F1	F0	GO
											FUNCTION CODE					

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Figure 2-7 RS03 Control Register Format

Table 2-2
Command Function Codes

Function Code +GO (octal)	Name	Description
01	No-Op	Performs no operation. Clears GO bit.
11	Drive Clear	Clears GO bit and all registers except Control and Maintenance registers in the *selected drive only.*
21	Read-In Preset	Same as No-Op.
31	Search	1. Sets the Positioning In Progress (PIP) bit in the Status register. 2. Searches for address contained in Desired Address register. 3. When desired address is found, clears PIP, asserts ATTN, and clears GO.
51*	Write Check	Same as Read Data.
61*	Write	Causes drive to accept information on the Data Bus and perform a write data operation.
71*	Read	Causes drive to perform a read data operation and place the information on the Data Bus.

*Function codes 51, 61, and 71 are *data transfer commands.*

Note: In the execution of any data transfer command, the drive must find the desired sector before the transfer can begin. Because this searching is similar to execution of a Search command, it is not necessary to execute a Search command prior to the execution of a Data Transfer command. Also, the assertion of PIP in the Status register occurs *only* during execution of a Search command, not during execution of a Data Transfer command.

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS REG.	DS	ATA	ERR	PIP	MOL	WRL	LBT	0	DPR	DRY	0	0	0	0	0	0	0

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Figure 2-8 Status Register Format

If a data transfer is in progress, the following sequence takes place. For Class A errors, EXC is immediately asserted to inform the Controller that an error has occurred, but the in-progress data transfer is not terminated. The transfer continues to the end of the current sector. At this point, if the Controller has negated RUN, a normal data transfer termination occurs. If it has not, complete sectors are transferred until RUN is negated. Following transfer termination, EXC is negated and ATTN is asserted.

For Class B errors, EXC and EBL are both immediately asserted and the data transfer is terminated by the drive, regardless of the state of RUN, even though the end of sector has not been reached. Following termination, EXC is negated and ATTN is asserted.

Once interrupted, the Controller can determine which of the 11 errors has occurred by reading the drive's Error register. The ERROR lamp and the appropriate LED

Table 2-3
Status Register Bit Assignments

Bit Position	Name	Function
07	DRY (Drive ReadY)	Indicates that the drive is ready to accept a command.
08	DPR (Drive PResent)	Indicates that the drive exists and power is applied.
10	LBT (Last Block Transferred)	Indicates that the last logical sector of the drive has been transferred. This bit is reset when a new address is loaded into the Desired Address register or when a Drive Clear function or Initialize is performed.
11	WRL (WRite Locked)	Indicates that the address in the Desired Address register is write-protected.
12	MOL (Medium On Line)	Same as DPR
13	PIP (Positioning In Progress)	Indicates that the drive is performing a Search function (i.e., Control register = 31_8).
14	ERR (Composite ERRor)	Indicates that an error condition has occurred. (Sets whenever any bit in the Error register is set.)
15	ATA (ATtention Active)	Indicates a drive abnormal condition or status change. Sets when: a. The ERR bit is set and a data transfer is not in progress. b. A Search function is completed. c. Drive power is first applied. Resets when the Controller: a. Issues a Drive Clear command. b. Asserts INIT. c. Writes a (1) into the appropriate Attention Summary Register bit position. d. Sets the GO bit and ERR=0. **NOTE** **The logical expression for the MASSBUS signal ATTN is:** $ATTN=ATA_0+ATA_1+.....+ATA_6+ATA_7$ **where ATA_0 is the ATA Status bit from Drive #0** **ATA_1 is the ATA Status bit from Drive #1, etc.**

remain lit until the Controller either issues an Initialize or Drive Clear command, or writes (0)s into the Error register.

Figure 2-9 illustrates the Error register format and Table 2-4 lists the error bit assignments with their functions.

The *Maintenance register* is a 16-bit register composed of four read-write bits, nine read-only bits, and three spares. The bits that constitute this register are located on several different modules but appear as a single register when read. This register is used for diagnostic testing of the drive logic circuits by logically replacing the analog signals coming from the disk with digital signals under processor control.

During diagnostic testing of the drive, the clock, index, and data signals from the disk are removed from both the drive timing logic and the data recovery logic. Maintenance register bits are then substituted in place of these disk signals.

Figure 2-10 illustrates the Maintenance register format and Table 2-5 describes each bit position.

The *Attention Summary register* logic is contained in the Command Decode module (M7759) located in slot AB06. This is a read/write "pseudo-register" (Figure 2-11) which consists of from one to eight bits, depending upon the number of drives connected to the MASSBUS. The term "pseudo-register" refers to the fact that only one register bit position is physically contained in each drive. Each drive is assigned a bit position, corresponding to its own unit number. This bit position reflects the state of the ATA status bit of that drive. Hence, bit position 0 of the Attention Summary register is generated by the ATA bit of drive 0, bit position 1 by that bit in drive 1, etc. Bits 8 through 15 are not used and are always read as (0)s.

Unlike the other drive registers, the Attention Summary register is directly-selected by the Controller without first addressing a particular drive. Thus, for a single Attention Summary register read operation, every drive in the system responds by placing the state of its ATA bit in the appropriate bit position on the Control Bus and disabling its remaining 15 Control Bus transmitters. This Control Bus configuration appears as a single register output which collectively informs the Controller of all drives that require attention (i.e., ATA=1).

The Controller can then selectively examine the Error or Status registers of each of the drives indicating an Attention, to determine the cause of the Attention condition.

The Controller can also write into the Attention Summary register, however, the significance of the bits being written is unusual. Writing a (1) into a bit position clears the ATA bit in the drive assigned to that bit position, however, writing a (0) has no effect. This writing scheme allows the Controller to clear, after inspection, any or all ATA bits that were set, without accidentally clearing those bits that may have become set in the meantime. The following list illustrates the effects of writing into an Attention Summary bit position:

ATA Bit Before	Bit Written Into Attention Summary Register	ATA Bit After
0	0	0
1	0	1
0	1	0
1	1	0

The *Desired Address register* part of the Address module (M7754) is located in slot AB10. This is a 16-bit, read/write register which contains the address of the track and sector, to or from which a data transfer is to be made. This register is illustrated in Figure 2-12. Bits 0–5 select the sector to be transferred while bits 6–11 select the track.

NOTE

The Desired Address register is the *only* register in the RS03 which implements all 16 bits of the Control Bus as read/write bits. When verifying proper operation of the Control Bus, transfers to and from the Desired Address register should be used.

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR REG.	ER	DCK	UNS	OPI	DTE	WLE	IAE	AOE	0	0	0	0	0	PAR	RMR	ILR	ILF

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Figure 2-9 Error Register Format

Table 2-4
Error Register Bit Assignments

Bit Position	Name	Function	Error Class
00	ILF (ILlegal Function)	Indicates that an illegal function code was transmitted (with GO set) (Table 2-2).	B
01	ILR (ILlegal Register)	Indicates that a read or write to a non-existent register was attempted.	A
02	RMR (Register Modification Refused)	Indicates that during a drive operation, a write into either the Control, Error, or Desired Address register was attempted	A
03	PAR (PARity)	Indicates that incorrect MASSBUS Data Bus or Control Bus parity was detected.	A
09	AOE (Address Overflow Error)	Indicates that RUN was still asserted after the last logical sector had been transferred to or from the drive.	B
10	IAE (Invalid Address Error)	Indicates that GO was set when the address in the Desired Address register exceeded the maximum allowable address ($> 7777_8$).	B
11	WLE (Write Lock Error)	Indicates that a write operation on a write protected track was attempted.	B
12	DTE (Drive Timing Error)	Indicates that GO was set when drive clocking and synchronization was erratic or missing.	B
13	OPI (OPeration Incomplete)	Indicates that a drive operation did not complete before 3 index pulses.	B
14	UNS (UNSafe)	Indicates a loss of drive power (ac or dc).	B
15	DCK (Data CheckK)	Indicates that a CRC read error was detected.	A

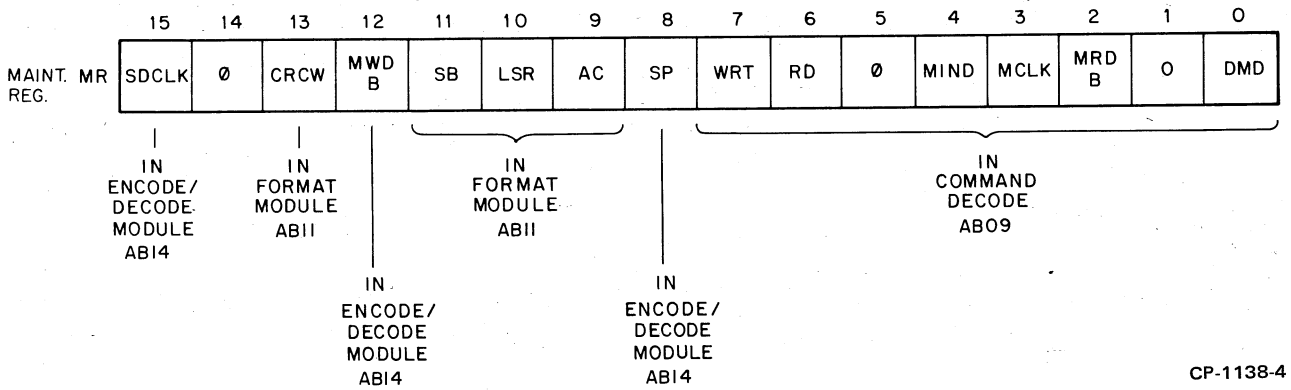

Figure 2-10 Maintenance Register Format

Table 2-5
Maintenance Register Bit Assignments

Bit Position	Name	Function	Type
00	DMD (Diagnostic MoDe)	Places the drive in the maintenance mode.	R/W
02	MRDB (Maintenance Read Data Bottom)	Replaces the read data from the read amplifier when in maintenance mode.	R/W
03	MCLK (Maintenance CLocK)	Replaces the disk timing clock when in maintenance mode.	R/W
04	MIND (Maintenance INDex)	Replaces the disk Index pulse when in maintenance mode.	R/W
06	RD (ReaD)	Indicates that the drive is performing a read operation.	RO
07	WRT (WRiTe)	Indicates that the drive is performing a write operation.	RO
08	SP (Sector Pulse)	Generated at the start of each sector.	RO
09	AC (Address Confirmed)	Indicates that the current sector and the sector portion of the desired address are the same.	RO
10	LSR (Load Shift Register)	Enables the parallel inputs of the Shift register during a write function.	RO
11	SB (Strobe Buffer)	Strobes data from the Data Bus into the drive's data buffer during a write operation, or loads read data from the Shift register into the drive's data buffer during a read operation.	RO
12	MWDB (Maintenance Write Data Bottom)	Miller encoded data to the bottom surface of the disk.	RO
13	CRCW (CRC Word)	Indicates that the CRC word is being written or read.	RO
15	SDCLK (Serial Data CLocK)	Clocks serial-read data out of the data decoding logic during a read operation; or clocks serial-write data into the data encoding logic during a write operation.	RO

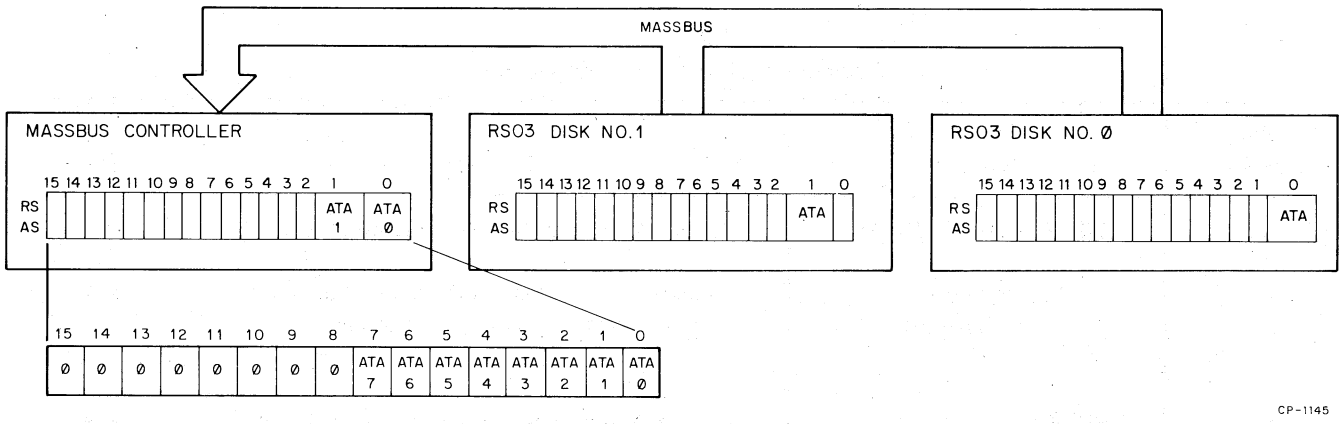

Figure 2-11 Attention Summary Register Format and Sources

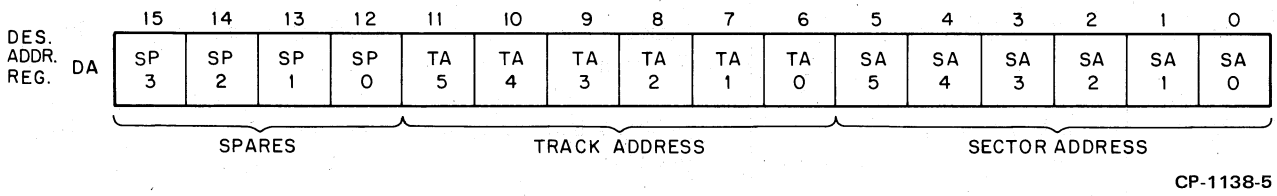

Figure 2-12 Desired Address Register Format

The register output may be read by the Controller at any time, but the Controller can only write into this register when the drive is not performing a Search or data transfer function (GO negated). If the Controller selects a non-existent track and sector address ($>7777_8$) and the GO bit is subsequently set, a gating circuit, connected to the output of this register, detects the erroneous address and an Invalid Address Error (IAE) occurs.

During a data transfer, this register is automatically incremented at the end of each sector. During normal operation, if RUN remains asserted at the end of a sector transfer, the next sector transfer is automatically initiated. However, if the Controller attempts to continue a data transfer from one sector greater than the last logical sector in the drive (address 10000_8), a gating circuit connected to the output of this register detects this fact and thereby causes an Address Overflow Error (AOE). *At the end of any data transfer operation, this register contains the address of the next sequential sector on the disk.*

The *Drive Type register* is part of the Status module, located in slot AB08. This is a read-only register, the contents of which designate a specific drive type. The data in this register specifies major differences between the same basic drive, but does not distinguish between minor options (e.g., 50 or 60 Hz power option). In the RS03, bit position 00 of this register indicates whether the sector interleave option is installed and bit position 01 is cleared to designate that the drive is an RS03. Bit positions 02 through 15 are read as (0)s.

Figure 2-13 illustrates the Drive Type register format and Table 2-6 briefly describes each bit position.

The *Look Ahead register* is part of the Timing Amp Logic module, (G092) located in slot AB16. This is a read-only register which contains the six bits of the current sector plus a 6-bit sector fraction. The information in this register specifies the angular position of the head in 64ths of a sector. This precise method of determining the head position relative to disk rotation, allows the programmer to optimize the disk access time by minimizing rotational delays.

Figure 2-14 illustrates the Look Ahead register format.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRIVE TYPE REG. DT	NBA	TAP	MOH	0	DRQ	0	0	0	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0

DRIVE TYPE

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Figure 2-13 Drive Type Register Format

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOOK AHEAD REG. LA	0	0	0	0	CS 5	CS 4	CS 3	CS 2	CS 1	CS 0	SF 5	SF 4	SF 3	SF 2	SF 1	SF 0

CURRENT SECTOR SECTOR FRACTION

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Figure 2-14 Look Ahead Register Format

Table 2-6
Drive Type Register Bit Assignments

Bit Position	Name	Function
00–07	DT (Drive Type)	Indicates the type of drive as follows: 000_8 = non-interleaved RS03 at 4 μs/word transfer rate. 001_8 = interleaved RS03 at 8 μs/word transfer rate.
11	DRQ (Drive ReQuest Required)	Reset to indicate that device is a single-port drive.
13	MOH (MOving Head)	Reset to indicate that device has fixed read/write heads.
14	TAP (TAPe Drive)	Reset to indicate that device is not a tape drive.
15	NBA (Not Block Addressed)	Reset to indicate that device is block-addressable.

The *Drive Timing Logic* is shown on the right-hand side of the logic block diagram (Figure 2-4) as part of Timing Amp Logic module (G092) located in slot AB16.

Timing originates on the disk as a prerecorded track of pulses which are amplified and fed to Timing Signal Generation logic. This logic is used to create Sector Pulses, Index Pulses, Clock Pulses, and a Set Syn signal to the Encode/Decode module, all as a function of the basic timing track. An additional output from this block increments the Sector Counter at the beginning of each sector. The Sector Counter locates the angular position of the heads relative to disk rotation. This counter is used as one input to both the Look Ahead register and the Sector Address Comparator.

The Look Ahead register comprises a set of open-collector gates, which gate the contents of the Sector Counter, plus sector fraction information from the Timing Signal Generation logic to the wired-OR register bus (WO BO(00:15)). The signal SECTOR COMPARE from the Sector Address Compare logic is fed to the Format Counter logic where it is used to initiate all data transfer operations.

The Timing Signal Generation logic outputs are also used to initialize and synchronize the Encode/Decode logic.

The timing track comprises a gap area, followed by the main portion of the track (Figure 2-15). The gap is 250 ± 50 μs long and is used to generate an Index pulse. During the gap, the frequency of the recorded signal is half the main track rate, or nominally 1.2 MHz (in 60 Hz drives). The main portion of the track is recorded to contain exactly 86,014 flux reversals, corresponding to 86,014 bit cell intervals. The frequency of the recorded signal is nominally 2.4 MHz (in 60 Hz drives).

As mentioned, the gap is used to generate an Index mark, which resets all the timing counters and identifies the location of sector 0. A Resync area, immediately following the gap, is 512 bits long and is used to allow the phase-locked loop to resynchronize to the higher frequency of the main portion of the timing track.

As shown on Figure 2-15, a spare timing track is provided, should the normal track or associated head become defective.

NOTE

The spare timing track may be selected by removing the timing track head connector, rotating it 180°, and replacing the connector on the timing track head.

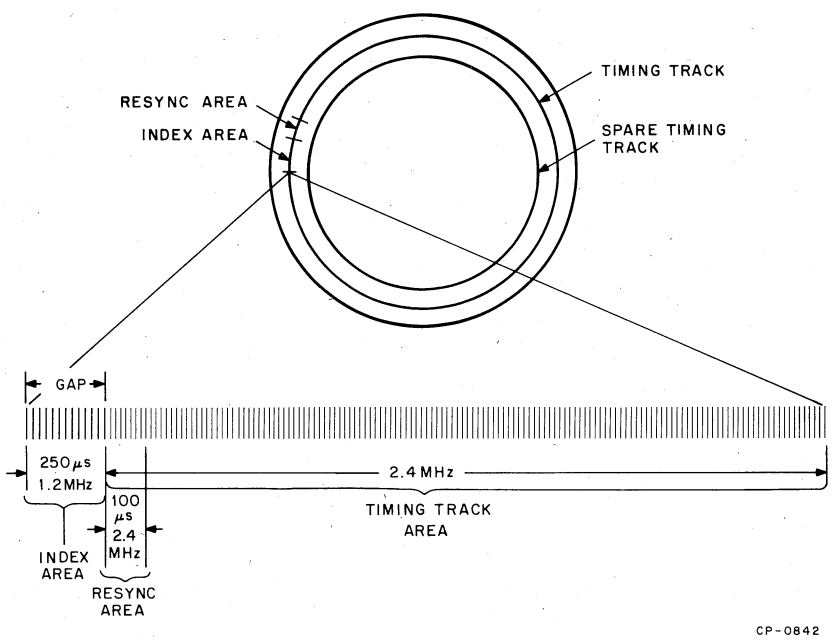

Figure 2-15 RS03 Timing Track Format

The *Timing Track Writer* module (M7757) can be used to rerecord in the field both timing tracks that are recorded on the disk at the factory.

NOTE

The two prerecorded timing tracks are *not* synchronous with one another; consequently, data recorded using one timing track cannot be recovered by using the second timing track. Similarly, if the timing track(s) are rewritten, previously recorded data is unrecoverable.

The Timing Track Writer module plugs into the logic subassembly in location AB16 (after removing the G092 module in that slot); a cable connects to the timing track head. Taking only power from the logic subassembly, the module generates the timing track signals that are recorded on the track. The Timing Track Writer generates the fixed number of flux reversals around the track, filling out the track with the half-frequency signal during the Index or gap area. An adjustment is provided to control the duration of the gap. The procedure for writing timing tracks is contained in Appendix F.

The *Data Bus Logic* is diagrammed on the bottom-half of Figure 2-4. The following discussion illustrates the interrelation of all of these blocks, first during execution of a Write function and then during execution of a Read function.

In a *Write function* (Figure 2-16), no data is written until first the Sector Address Compare logic (M7754 in the Control Bus portion of the diagram) determines that the sector portion of the Desired Address register compares with the current sector. This is indicated by assertion of SECTOR COMPARE. This assertion causes the Format Counter logic (M7771) to assert TRANS DATA which enables the Encode/Decode module (M7751). While enabling the write amp with WRT GATE, this module (M7751) encodes 0s in Miller format for the preamble and transmits these encoded zero pulses to the write amplifier (G182). The write amplifier converts the pulses to currents which drive the selected head through the Head Matrix modules (M7758).

When the Timing Signal Generation logic (G092, top-half of Figure 2-4) has determined that sufficient zeros have been recorded in the preamble, SET SYN is asserted.

NOTE

The length of the preamble is between 67 and 70 "0" bits. The exact length is dependent upon cable delays, which occur between the assertion of SCLK and reception of WCLK by the drive; therefore, the shorter the cable between the drive and Controller, the shorter the preamble in that drive.

The M7751 responds by asserting RD SYNC which enables its CLK signal, which is nominally 4.8 MHz. When this CLK begins, the Format Counter and Data Bus Control (M7771) combine to generate the first SCLK signal to the Controller. When WCLK is received from the Controller, the Data Buffer (M7753) is strobed with the data word on D(00:17). After being checked for correct parity by the Data Bus Parity logic, the word in the Data Buffer is parallel-loaded into the Shift register (M7753). At the same time, the signal WRT PREamble is negated, causing the M7751 to Miller encode and record the sync "1", terminating the preamble.

Once the data word has been loaded into the Shift register, it is clocked out serially *Most Significant Bit first (bit 17)* at 4.8M bits/sec to both the CRC Generator/Checker to generate the CRC word for that sector, and the Encode/Decode module (M7751). The Encode/Decode module converts the serial NRZ data to Miller encoded pulses just as when writing the preamble.

While this is in progress, the Format logic generates the next SCLK signal. When WCLK is returned, the second data word is strobed into the Data Buffer. This word is not transferred to the Shift register until the Format Counter logic determines that the last bit of the first word has been shifted to the Encode/Decode module. This transfer from the Data Buffer to the Shift register takes place in such a manner that *no break or gap occurs between words*, i.e., the data appears as a single, continuous serial data stream.

This entire cycle continues until 64_{10} words have been strobed into the Data Buffer, transferred to the Shift register and have been serially-shifted to the CRC logic and the Encode/Decode module. At this time, the Format Counter asserts CRC WD, which causes the CRC Generator/Checker to shift its contents as serial data to the Encode/Decode module, immediately following the last bit of the last word from the Shift register. The CRC word is recorded simply as the "65th data word" in the sector.

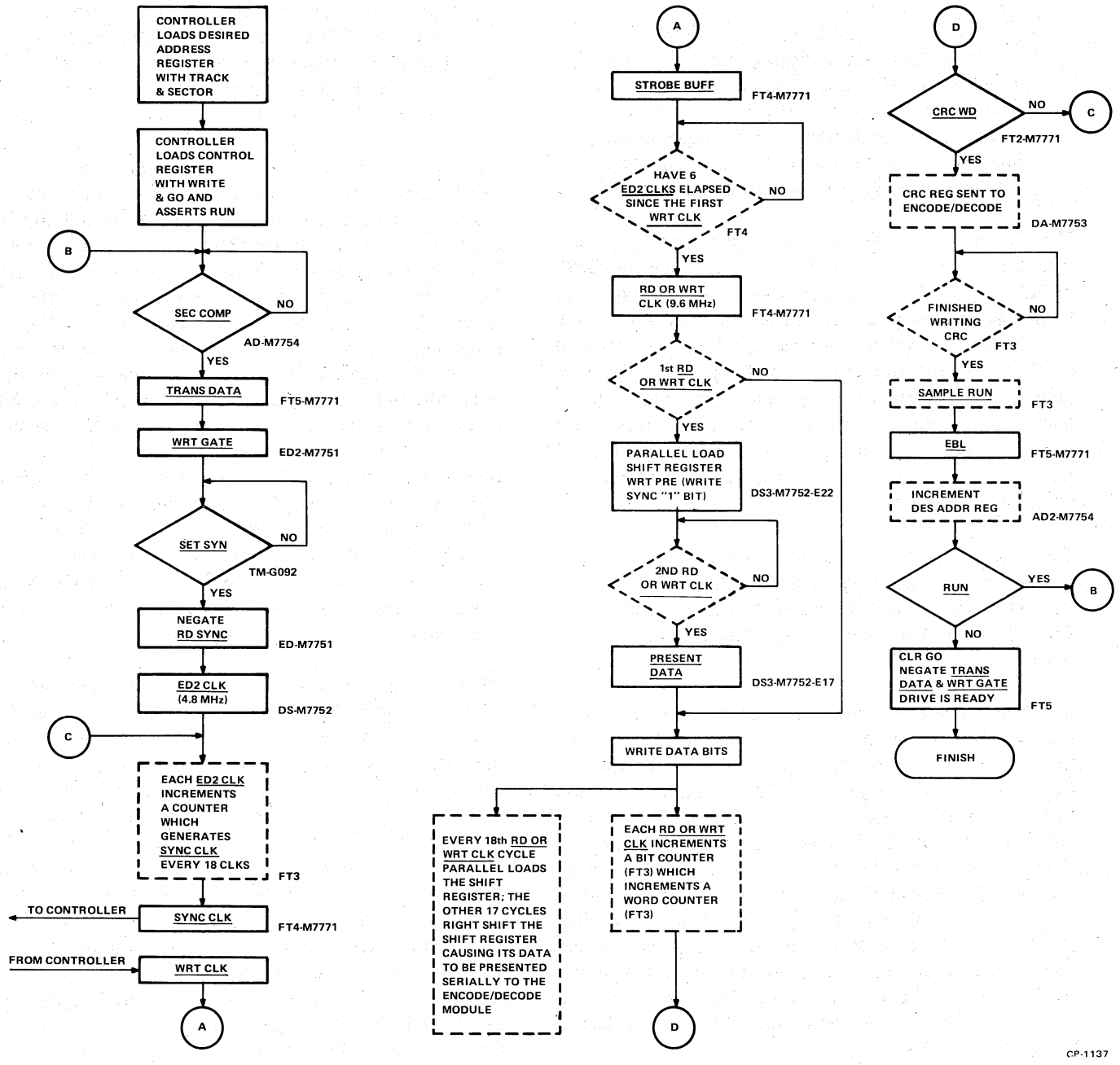

Figure 2-16 Write Data System Flow

After the CRC word is recorded, the Data Bus Control logic (M7771) asserts EBL, to indicate to the Controller that the end of the sector has been reached. Then, depending on the state of RUN, the Data Bus Control either terminates the transfer or waits to repeat the entire process during the next consecutive sector.

In a *Read (or Write Check) function* (Figure 2-17), as with a Write function, no data is recovered until first the Sector Address Compare logic (M7754 in the Control Bus portion of Figure 2-4) determines that the sector portion of the Desired Address register compares with the current sector. This is indicated by assertion of SECTOR COMPARE. This assertion causes the Format Counter logic (M7771) to assert TRANS DATA which enables the Encode/Decode module (M7751). The assertion of TRANS DATA also switches the input to the phase-locked loop (M7751) from CLK PULSE (from the Timing Signal Generation logic, G092) to the RD DATA PULSE signal, generated by the read amp (G182).

The magnetic flux reversals, recorded on the disk, generate a low amplitude (10–20 mV, peak-to-peak) signal in the heads. The signal from the selected head is switched by the Head Matrix modules (M7758) to the inputs of the read amp (G182) where the signal peaks (corresponding to the flux reversals) are converted to TTL level pulses. This RD DATA PULSE signal is still a Miller encoded pulse and must be decoded by the Encode/Decode module to NRZ data.

Initially, the M7751 is conditioned to decode only the constant all-zero pattern of the preamble. This gives the phase-locked loop the time necessary to correct for any instantaneous step phase error, resulting from switching inputs from CLK PULSE to RD DATA PULSE. After 62 CLK PULSEs, the Timing Signal Generation logic (G092) asserts SET SYN. *This switches the M7751 to decode any pattern of RD DATA PULSEs (instead of all zeros)* even though there are still 5 to 8 zeros remaining in the preamble. When *the M7751 decodes the sync "1"* at the end of the preamble, the NRZ RD DATA and CLK signals from that module are enabled and remain enabled until the end of the sector. The decoded data appears as NRZ RD DATA and CLK defines the bit intervals. The CLK signal from the M7751 is nominally 4.8 MHz.

The single 4.8M bits/sec serial NRZ RD DATA signal is clocked simultaneously into the Shift register and the CRC Generator/Checker (M7753). When the Format Counter logic (M7771) has counted 18 CLK pulses, it generates a STROBE BUFF pulse which parallel-transfers the contents of the Shift register to the Data Buffer (M7753). The Data Bus Parity logic (M7753) then generates the appropriate DPA bit, corresponding to the contents of the Data Buffer. The Data Bus Control logic (M7771) then asserts SCLK, indicating to the Controller that a data word is present on D(00:17). SCLK is negated nine CLK pulses later.

The Shift register and the CRC logic are continuously clocked with the NRZ RD DATA signal because *no break or gap occurs between words in the serial data.* Every eighteen bits, the Shift register contents are transferred to the Data Buffer and SCLK is sent to the Controller.

This entire cycle continues until 64_{10} words have been shifted into the Shift register and CRC logic, strobed into the Data Buffer, and transferred to the Controller. If the 64 data words have been read correctly, the CRC register will now contain the same CRC word that is about to be read from the disk. At this time, the Format Counter asserts CRC WD, which indicates that the CRC word from the disk is being clocked into the CRC Generator/Checker. If the entire sector (64 data words plus the CRC word) has been read correctly, the CRC register will contain all zeros after the serial CRC word has been clocked into it. The contents of the CRC register are checked to be zero, 18 CLK pulses after the last data word has been strobed into the Data Buffer.

After the CRC register is checked for zero, the Data Bus Control logic asserts EBL, to indicate to the Controller that the end of the sector has been reached. Then, depending on the state of RUN, the Data Bus Control either terminates the transfer or waits to repeat the entire process during the next consecutive sector.

The *Head Selection* logic electrically switches, to the Read/Write Amplifier, the head corresponding to the data track specified in the Desired Address register. The Head Selection logic is composed of two types of modules: there are two M7758 Head Matrix modules, and one M7756 Alternate Track Option module.

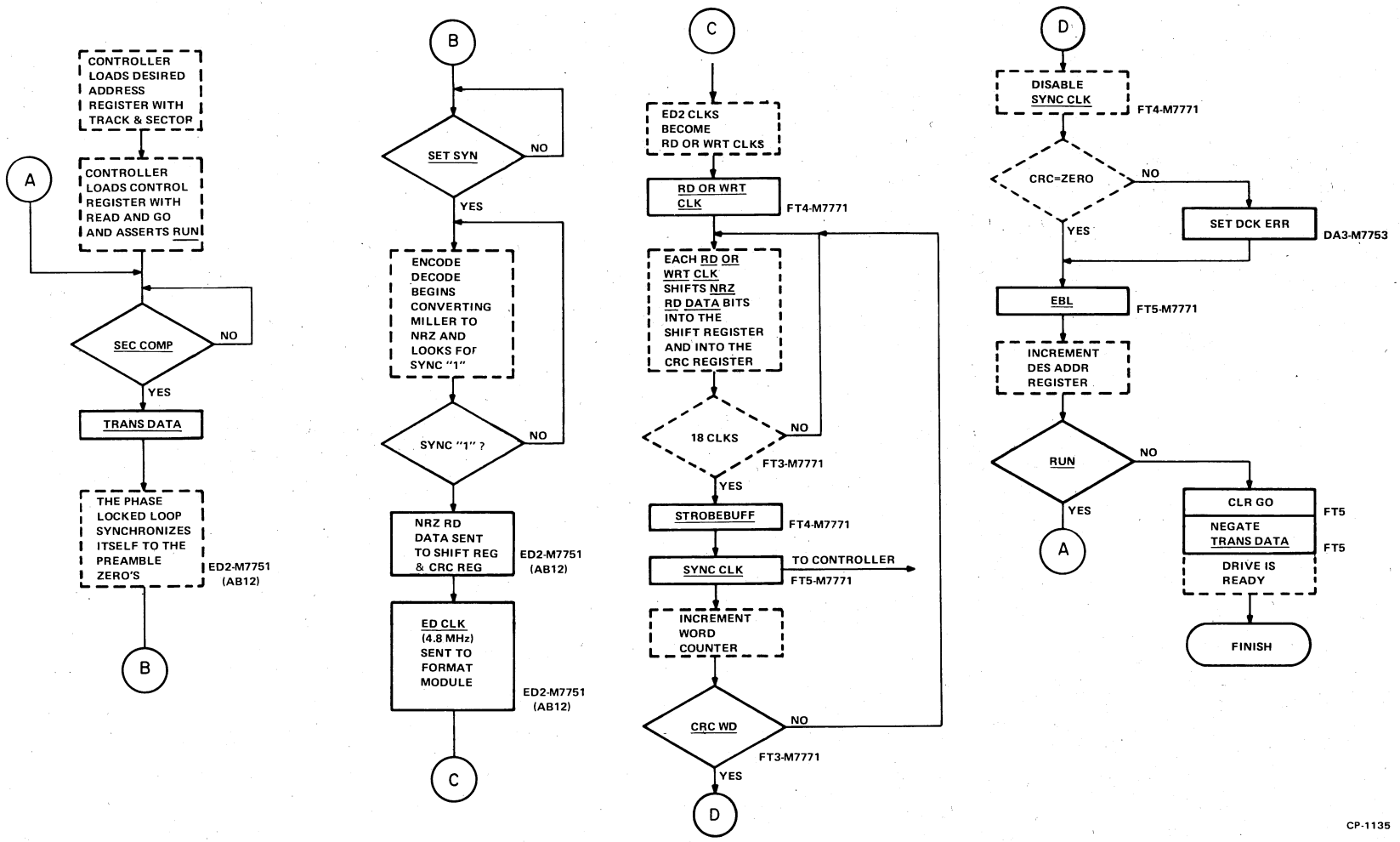

Figure 2-17 Read Function Flow

The *Head Matrix* module is capable of selecting one head out of 32 or, in other words, one head from any of four head block assemblies. This is shown in the block diagram, Figure 2-18. The column decode logic activates one of four transistor switches which selects one of four head block assemblies. The row decode logic activates one of eight transistor switches which selects one of the eight heads within the selected head block assembly.

Since there are a total of 64_{10} data tracks, two Head Matrix modules are required to select any one of the tracks. By a minor difference in the backplane wiring to the two modules, one is configured to select tracks 00_8-37_8 (AB18) and the other to select tracks 40_8-77_8(AB19).

The Head Matrix modules may be disabled by a signal from the Alternate Track Option module if the currently-addressed track has been jumpered to one of the spare data tracks. This prevents the selection of a known-faulty head.

The *Alternate Track Option* module (M7756) electrically replaces any known-defective head with one of the heads in the spare head block assembly. There is one Alternate Track Option module in the RS03.

The Alternate Track Option module receives the same track selection signals from the Desired Address register as the Head Matrix modules. Whenever the currently-addressed track corresponds to a track address which has been jumpered into the Alternate Track Option module, the module disables both Head Matrix modules associated with that disk surface and switches the selected spare track to the Read/Write Amplifier.

Instructions for connecting spare tracks are contained in Section III.

Four spare tracks are reserved for use by Manufacturing. However, any and all spares not used by Manufacturing may be used by Field Service personnel.

2.2.3 Drive Operations

There are seven valid commands that the Controller can issue to the RS03. These commands and their function codes are:

01_8	No Op	
11_8	Drive Clear	
21_8	Read In Preset	
31_8	Search	
51_8	Write Check	Data Transfer Functions
61_8	Write	Data Transfer Functions
71_8	Read	Data Transfer Functions

Each of these commands has been defined previously in the discussion of the Control register in Paragraph 2.2.2. The Data Transfer functions were discussed in conjunction with the Data Bus Logic. The following discussion is a flow chart representation of each of the remaining commands.

The *No Op* and *Read In Preset* functions (Figures 2-19 and 2-20) are identical in the RS03. The Control register is loaded with either function code (01_8 or 21_8) by a Control Bus handshake sequence. As soon as either function is decoded, the GO bit is cleared, terminating the function. The Control register will then contain either 00_8 or 20_8.

The *Drive Clear* function is shown in Figure 2-21. The Control register is loaded with the Drive Clear function code (11_8) by a Control Bus handshake sequence. When the function is decoded, the Desired Address register, the Error register, and the ATA, ERR, and LBT bits in the Drive Status register are cleared. When this is accomplished, GO is cleared and the operation is terminated.

The *Search* function (Figure 2-22) is a programming convenience.

NOTE

Any data transfer command (Read, Write, or Write Check) automatically initiates the same hardware function as a Search command, making the execution of an individual Search command unnecessary in performing a data transfer function.

Prior to initiating the Search function, the Controller loads the Desired Address register with a Control Bus transfer.

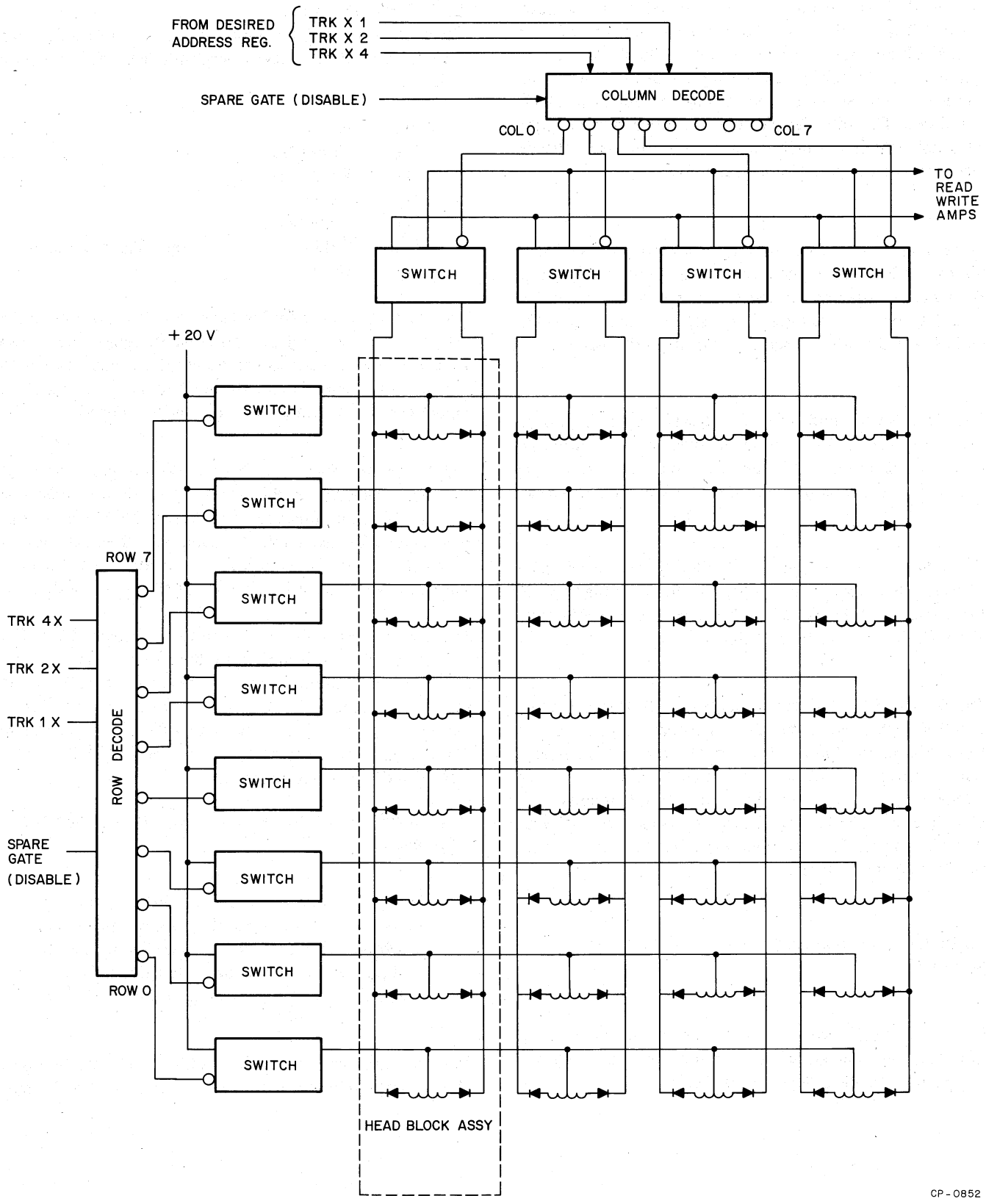

Figure 2-18 Head Matrix Module (M7758) Simplified Diagram

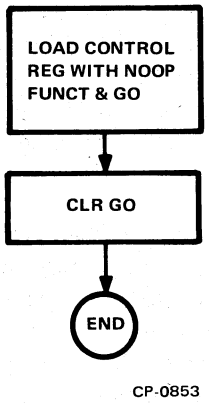

Figure 2-19 No-op Flow Chart

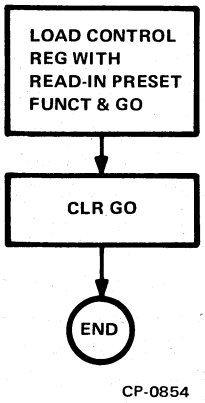

Figure 2-20 Read-in Preset Flow Chart

The Controller then performs a second Control Bus transfer to load the Search command (31_8) into the drive's Control register. This resets the Drive Ready (DRY) bit in the Drive Status register. Whenever GO is asserted, the drive becomes busy and will not accept any more commands from the Controller. The command decoding logic decodes the Search function code and generates the signal SEARCH.

NOTE

Since the Search command is not a data transfer command, it is not necessary for the Controller to issue RUN to begin command execution. All non-data transfer commands are automatically executed.

The signal SEARCH sets the Positioning In Progress (PIP) bit in the Status register and causes the drive to search for the desired sector. When the desired sector is found, the

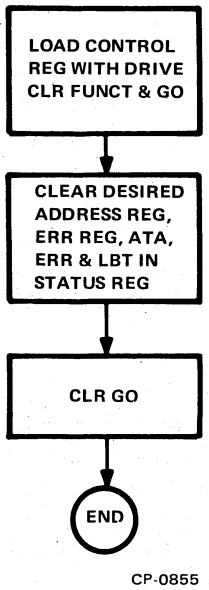

Figure 2-21 Drive Clear Flow Chart

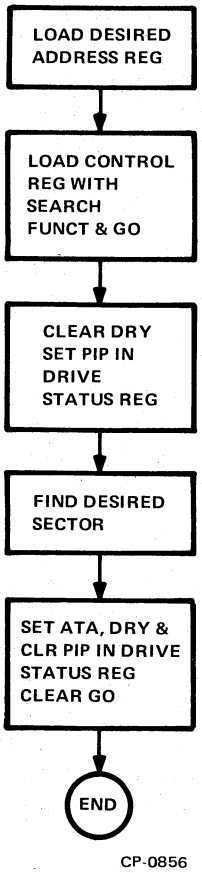

Figure 2-22 Search Flow Chart

signal SECTOR COMPARE is asserted, the PIP bit is reset, GO is negated, and ATTN is transmitted from the drive to indicate to the Controller that the Search function has been completed. In addition, the negation of GO sets the DRY bit, allowing the drive to accept another command from the Controller.

If the Search function is not completed before 3 Index Pulses have occurred, an Operation Incomplete (OPI) error occurs and the Search function is aborted.

2.2.4 Maintenance Mode

The RS03 has been designed with built-in test capability. This "Maintenance Mode" test capability isolates the digital electronics from the analog and allows independent testing of the digital logic. Therefore, failures located entirely in the logic can be separated from failures occurring in the analog electronics or the head/disk subassembly.

By setting bit 00 in the Maintenance register, the Maintenance Mode logic is enabled, and the remaining read/write bits in the Maintenance register are substituted for the corresponding signals, normally originating from the head/disk subassembly. The read-only bits in the Maintenance register reflect the states of major signals during drive operation. By setting and clearing the read/write bits in predetermined sequences and simultaneously monitoring the read-only bits, it is possible to verify the operation of all of the drive's logic. This includes all drive timing as well as the logic associated with reading and writing data.

Several characteristics of the Maintenance Mode logic are worth mentioning to avoid any confusion or misunderstandings by service personnel:

a. Before proceeding with any Maintenance Mode exercise (but after setting bit 00 in the Maintenance register), it is necessary to set and then clear the Maintenance Index bit (bit 04) to initialize the drive timing logic.

b. The Maintenance Clock bit (bit 03) is used to simulate the highest frequency clock used within the drive. This frequency is the same as the frequency at which data is recorded on the disk (TM5 CLK PULSE L). For this reason, Maintenance Clock is used by the Timing Amp logic module to generate TM5 CLK PULSE L. This is shown in the following example:

   A complete sector (leading edge of one sector pulse to the leading edge of the next sector pulse) consists of 1,334 bit intervals or TM5 CLK PULSE L cycles. To simulate a complete sector in Maintenance Mode requires 1,334 cycles of Maintenance Clock.

c. After concluding any Maintenance Mode testing, it is necessary to guarantee at least one complete disk revolution (at least 25 ms) before resuming any real-time drive operations. This allows the drive's timing logic to be re-synchronized to the timing track before attempting any drive operation, and prevents the occurrence of Drive Timing Errors.

A discussion of available Maintenance Mode diagnostics is included at the beginning of Section III of this manual.

2.2.5 Power Distribution and Control

RS03s are available in four standard voltage/frequency versions: 115 V (50 or 60 Hz), and 230 V (50 or 60 Hz). Differences in the four versions are confined to the Power Supply/Control assembly and field power conversions should be accomplished by changing the whole assembly.

All ac voltage-dependent devices in the drive have nominal 115-V windings. The windings and/or devices are connected in-parallel for 115-V operation and in-series for 230-V operation. The only frequency-dependent device is the ferroresonant power supply transformer; different transformers are used for 50 or 60 Hz operation.

Power in the drive can be controlled in three modes, selected by SW1 on the rear of the drive.

1. With the switch in the OFF position, the dc power supply is off and the disk motor will not *start*. However, if the motor was running before the switch was moved to the OFF position, it will stay running until the main breaker is thrown or ac is lost.

2. With SW1 in the LOCAL position, the disk motor will start, or it will continue running. In either case, when the motor is up to speed, the dc power supply is turned on.

3. In REMOTE mode, the drive is under control of two system buses; the Power Sequencing Bus for disk motor control, and the Power Control Bus for dc power supply control.

The *Power Sequencing Bus* sequences the disk motors of drives in REMOTE mode in a multi-drive system. Only one drive will start at a time, preventing excessive peak drain on the ac line. Connections to this bus are made in the rear of the drive to J3 IN and J4 OUT; the first drive in the sequence has a jumper on J3 IN to initiate the starting sequence. On all other drives, J3 IN is connected to J4 OUT of the preceding drive, leaving J4 OUT unused on the last drive. The three signals on the Sequencing Bus are Ground, Start In Progress L (SIP L), and Bus Grant L. Each drive monitors SIP L and will not start if this signal is asserted. Each drive also asserts SIP L if it is starting. Bus Grant In L (J3) is sensed inside the drive as Start Motor L, the assertion of which will start the drive's motor if no other drive is starting. Bus Grant Out L is driven by the drive signal Motor Started L and is asserted after the drive is up to speed. In a multi-drive system, each drive sees the previous drive's Motor Started signal as its own Start Motor signal and all disk motors sequentially power up (Figure 2-23).

The *Power Control Bus*, plugged into J1 and J2, controls the drive when it is in the REMOTE mode. The three signals on this bus are Ground, Remote Power L, and Emergency Off L. If the drive is up to speed, it starts the dc supply when it senses an assertion of Remote Power On L and anytime Emergency Off L is asserted, the dc supply is shut off.

NOTE

This is a simultaneous bus and all drives controlled by it turn on and off together, providing all motors are up to speed. Any drive in a multi-drive system that is not in Remote, passes on the Power Sequencing and Power Control bus signals to maintain bus continuity for all remaining drives.

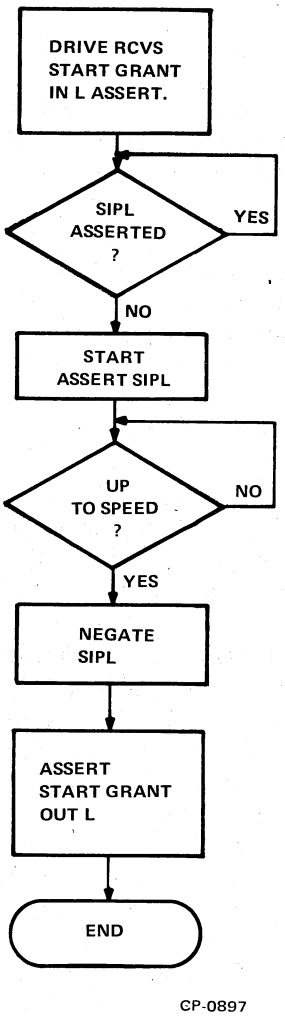

Figure 2-23 Flow Chart for RS03 Power Sequencing Bus with Drive (SW1) in REMOTE

2.2.6 Power Fail

There are two power failure conditions which must be sensed by the drive to prevent the loss of previously-recorded data. The first is a power failure within the Controller; the second is a power loss within the drive itself.

When a MASSBUS Controller detects, within itself, a power-fail condition, it asserts the signal MASS FAIL on the MASSBUS. The drive delays response to this signal for approximately 200 ns to prevent transients from causing erroneous shutdowns. After this time, the drive generates a clear signal, which functions like MASSBUS INIT, and then disables the MASSBUS signals INIT and DEM. The drive will continue to disable DEM and INIT until power returns in the Controller and MASS FAIL is negated.

The reason for this action is that when the Controller loses power, it can no longer maintain the proper differential levels on those MASSBUS signals which it asserts. These undriven differential lines may then produce oscillations in the MASSBUS receivers at the drive, and in turn, the drive could interpret this as a Control Bus transfer to initiate a Write function. By disabling DEM, no Control Bus transfer can occur and data stored in the drive is protected.

NOTE

If the Controller asserts MASS FAIL during execution of a Write function, the drive may abort the Write before completely writing a sector. Therefore, when reading that sector, a DCK (CRC) error may result.

If a drive loses power, it is not only necessary to preserve data previously recorded on that drive, but it is also necessary to maintain the integrity of the MASSBUS, to prevent the disruption of any other drive during and after the power failure in one drive. This is accomplished by disabling both the write amplifiers and the MASSBUS transmitters in the failed drive.

Loss of power (ac or dc) within the drive is indicated by negation of the signal SAFE from the drive's power supply. This sets the UNS (Unsafe) error, which is handled like any other Class B error (see Paragraph 2.2.2, Error Register).

The negation of SAFE also activates the power fail logic, located on the Control module (M7755), which consists primarily of a normally-closed relay contact in parallel with a transistor switch. The transistor-relay contact combination is used to generate an initializing signal and the disabling signals for the write amplifier and the MASSBUS transmitters. Due to the relatively long switching time of the relay, the transistor generates the initializing and disabling signals until the relay contact closes. However, generation of these signals is delayed approximately 20 μs after the negation of SAFE to provide the drive time to inform the Controller of the power failure.

The power fail logic on the Control module keeps the drive cleared and the write amplifiers and MASSBUS transmitters disabled until power returns. As soon as power is within acceptable limits, the power supply asserts SAFE. Approximately 13 seconds after assertion of SAFE, the power fail logic energizes the relay coil to open the contacts and turns off the transistor in parallel with the contacts. This removes the initializing signal, the signals disabling the write amplifier, and the MASSBUS transmitters. This drive then asserts ATTN, indicating a drive status change to the Controller.

2.3 MECHANICAL PRINCIPLES OF OPERATION

Subsection 2.3 discusses the mechanical principles involved in the operation of the RS03 (Figure 2-24).

2.3.1 Motor

The RS03 DECdisk is driven by an integral ac induction motor/spindle. The motor is mounted to the head casting vertically and rotates in a CCW direction as viewed from the top of the drive.

CAUTION

This motor and hub assembly is a precision device and must be treated with care so as not to damage any mounting surfaces, bearings, or to change any of the assembly's tightly-controlled balance and runout properties.

The motor hub assembly is balanced by adding self-sticking metallic tape to a recess in the motor hub.

NOTE

This process is performed at the factory under controlled conditions. Under no circumstances should this tape ever be removed or relocated on the hub.

The disk is clamped to the motor hub by a flexible diaphragm, which distributes the clamping force evenly around the disk, introducing no unnecessary stresses in the disk which could result in runout.

NOTE

Some early models use a Belleville washer and cap arrangement to clamp the disk.

The motor is air cooled with air intake at the mounting flange end and exhaust at the opposite end. The capacitor start motor has a high starting torque (to get the high inertial load up to speed) and a lower run torque (necessary to maintain speed).

All windings in the motor are nominally 115 V (50 or 60 Hz) and enough points are brought out to the motor's 9-pin Mate-N-Lok® connector to permit the power supply control unit, which controls the motor, to connect these windings in series or in parallel for 230 V or 115 V operation. A thermal protector is self-contained in the motor, which shuts off the motor if temperatures reach a dangerous level. It then restarts the motor as the motor temperature returns to normal.

®Mate-N-Lok is registered trademark of AMP, Incorporated.

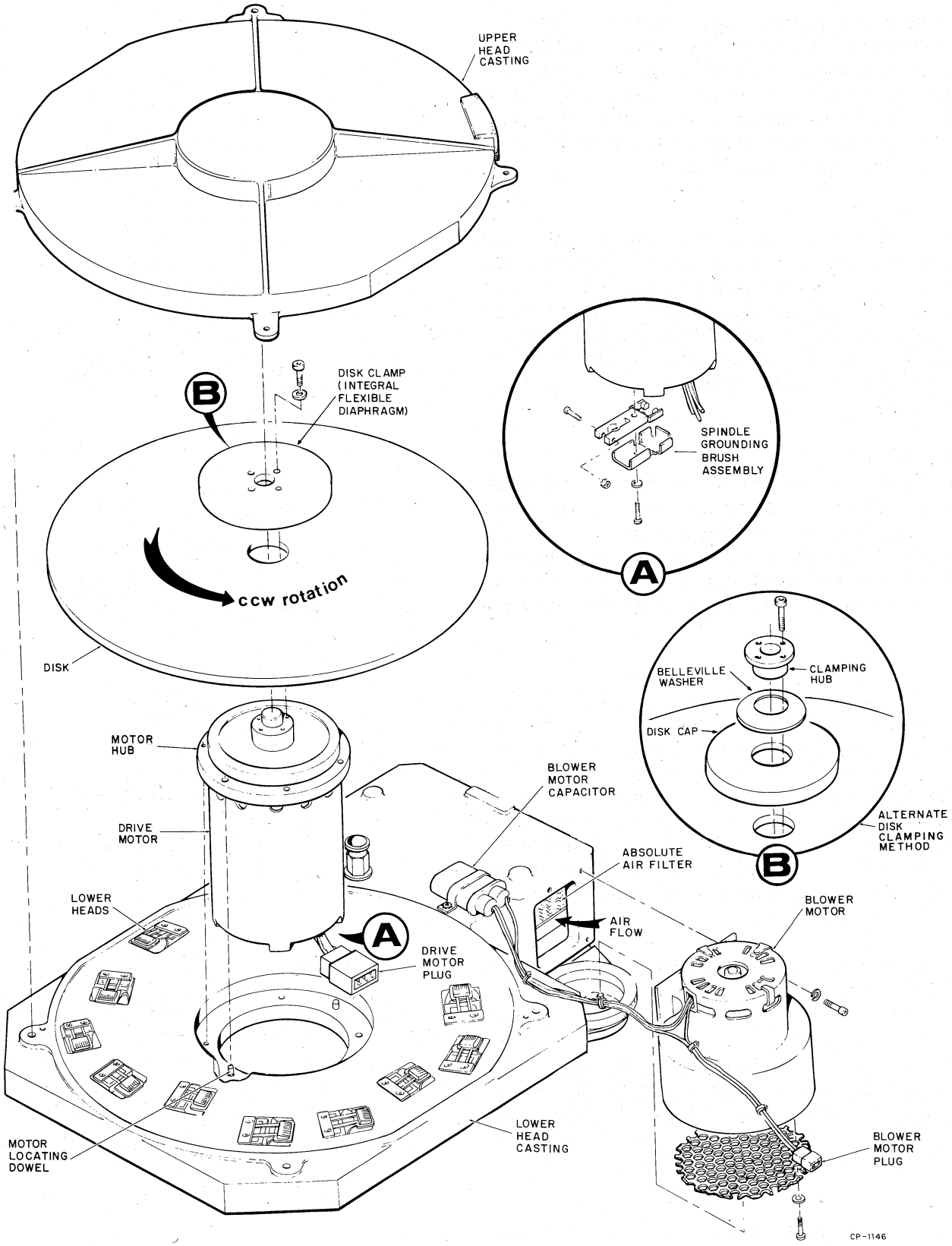

Figure 2-24 RS03 Mechanical Components

Spindle grounding brushes are mounted on the bottom of the motor in a special mounting bracket (Figure 2-24). The bracket holds the silver carbon brushes against the motor shaft and grounds it to the motor frame. This prevents static charges from building up on the surface of the disk. The brush holder, when reversed, acts as a spindle lock to prevent disk rotation during shipment.

2.3.2 Disk

The RS03 recording disk is a 16-in. diameter, aluminum platter that has been plated with nickel-cobalt as the recording medium, and specially-treated to create a hard surface. The disks are very smoothly finished and are completely tested to be free of any mechanical or magnetic flaws. In the device, the disk must be absolutely free of dirt and cleaned/lubricated following the recommended procedures exactly.

2.3.3 Heads

The RS03 has 10 head block assemblies mounted on the lower-head casting, flying on the bottom surface of the disk. Each head block assembly contains 8 ferrites which are individually selectable. The 10 head block assemblies are mounted such that their 80 ferrites describe 80 non-overlapping concentric tracks on the lower surface of the disk.

The ferrites on each head block are 0.050 in. from center-to-center; each head block assembly is located on the casting by a round and diamond-shaped dowel pin pair. One of the two dowel holes in each head block assembly is "dimpled" to prevent head block assemblies from being installed backwards. The location of dowel pin pairs on the castings interlace ferrites, radially on the disk, such that physical tracks on the disk are 0.025 in. from center-to-center. Figure 2-25 shows physical track location as a function of track number.

In the drive, 64 tracks (8 head blocks) on the bottom surface are data tracks.

Of the two remaining head block assemblies, one is dedicated to timing information. Two prerecorded, non-synchronous timing tracks (one Main and one Spare) have been recorded under two ferrites of this head block assembly; the other 6 ferrites are not used.

The tenth and final head block assembly is a spare data head block, whose ferrites may be individually selected via jumpers on the M7756 module in AB20, to replace any one

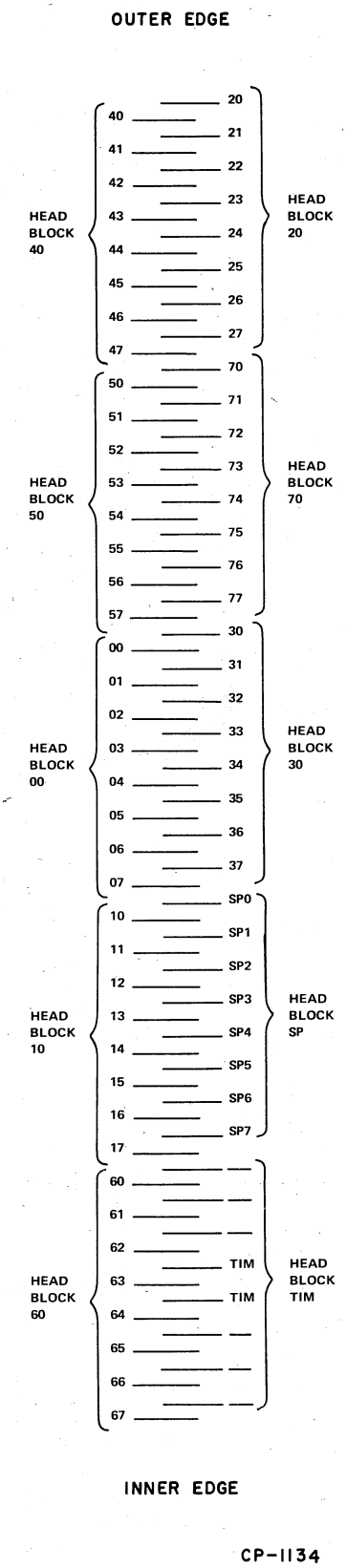

Figure 2-25 Physical Track Locations on Disk

of the normal 64 data ferrites. Although all of these 8 ferrites may be available as spares, only 4 are guaranteed available to the field.

All head block assemblies are factory-loaded to a single precise value and all casting head mounting surfaces are factory-shimmed. As the head radius increases, each head block mounting surface is shimmed closer to the disk so that as the surface velocity increases with increasing radius, the heads all fly at a nominal 55 microinches.

CAUTION

The shims are bonded to the casting and none must be lost or removed if it is necessary to replace a head.

2.3.4 Air Filter System

The RS03 air filter system consists of three elements.

1. A foam Prefilter, which is fitted to the front cover, against the logic rack, and is used to collect airborne lint and dust.

2. A Blower Prefilter, which is fitted to the blower inlet, and is intended to remove major particles from the incoming air.

3. An Absolute filter, which is fitted in a cavity within the lower head casting, and is intended to reduce the particle count to a level which will guarantee extremely clean air inside the disk cavity.

A Squirrel-Cage Blower Motor is used to force air through the Absolute filter to the middle of the top and bottom surfaces of the disk and to keep the disk cavity positively pressurized. Excess air and any particles that may have entered the disk cavity, are allowed to exit through a foam filter on the upper casting.

2.4 MAGNETIC PRINCIPLES OF OPERATION

In the RS03, information is stored in the form of flux reversals in a thin layer of magnetic material (nickel-cobalt) on the disk surface. The flux reversals are both written and read by a ferrite core and coil assembly, eight of which are mounted in one alumina slider. Each 8-track slider is mounted in one head block assembly (Figure 2-26).

When writing on the disk, the RS03 electronics switches the center tap of the selected ferrite to +20 V and the Read/Write amplifier (G182) sinks 96 mA of write current through one side of the coil *or* the other. When the 96 mA is switched from one side of the coil to the other, the direction of flux in the ferrite and the gap changes. The resulting change of direction of the fringing flux causes a reversal of flux in the nickel-cobalt on the disk where the information is stored.

When the same ferrite is reading information (flux reversals) that it has previously written, it is once again selected by switching its center tap to +20 V. In a read mode, a flux change in the ferrite is caused by a recorded flux reversal passing the gap, generating a differential voltage between the ends of the coil. Disk flux reversals appear as voltage pulses, the peaks of which are detected by the G182 Read/Write Amplifier to reproduce the sequence of pulses which was previously written.

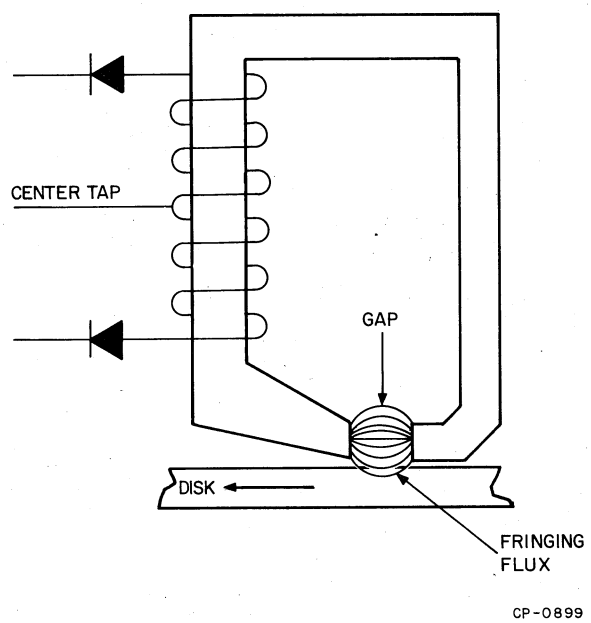

Figure 2-26 Ferrite and Coil Assembly

SECTION 3
ELECTRICAL SERVICING

3.1 GENERAL

This section is devoted to servicing the electrical portions of the RS03 DECdisk; for Mechanical Servicing, refer to Section IV. This section discusses the role played by diagnostics in trouble isolation. The diagnostic section serves to isolate the problem to a module.

Once the faulty module is determined, troubleshooting can progress to the remaining subsections of this section, where each module in the RS03 is described in detail. These subsections contain more detailed procedures, with a detailed logic discussion of each module, a troubleshooting flow chart, and timing diagrams (where necessary).

These detailed discussions are separated as to hardware (module number), not by function. Section II of this manual ignored the hardware boundaries; in this section, several functional elements may be discussed under one hardware entity.

There are several tasks considered to be a part of servicing the RS03 – diagnostic testing of the logic in a working but malfunctioning system, performance checks of the various modules, and troubleshooting procedures to be performed after a given malfunction has been isolated to a particular subsection of the logic. Performance checks and troubleshooting procedures are included in a table, listing each diagnostic and the portion of the logic that it tests.

Generally, the procedure is to run the Basic (Static) routine to isolate the malfunction to a particular area of the device. A failing test will indicate a problem, either in the logic being checked by that test, or in the intervening logic. These diagnostics are provided with subtests that may further isolate the problem within the suspected area.

The failing test is then run either during troubleshooting procedures or after troubleshooting has been accomplished. When drive repairs are completed, the checkout and exerciser routines are again run to ensure proper drive operation.

3.2 DIAGNOSTIC TESTING

There are various diagnostic programs provided by DEC to exercise the RS03 when in operation with an RH11 Controller in a PDP-11 system. These programs have been devised to test the logic on an ascending dependency basis; first checking out basic blocks of logic and as each block is proven good, utilizing that proven logic to check out logic blocks that depend on the blocks just proven.

Full instructions are given in the diagnostic printouts as to their loading and use. In the paragraphs that follow, each test and its purpose is described, as an aid to troubleshooting. Each test is listed in tabular form with its test name and function. Following each listing, the halt location is shown for a failure on that test, with a listing of probable electrical and/or mechanical faults that could produce that error. When a mechanical fault is suspected, refer to Section IV for procedures.

Within most tests, provision is made to loop on certain functions for scoping purposes. Although these diagnostics are quite comprehensive, they should not be considered as a complete maintenance tool. They must be used judiciously by the technician with the circuit schematics, the various detailed theory discussions, the indications provided by the indicator lights, and by ancillary test equipment. Diagnostics are capable of isolating trouble to a specific module but cannot indicate faults below that level.

3.2.1 PDP-11 Diagnostics

Table 3-1 and Figure 3-1 show the PDP-11 Static Tests; in the table, the Test Name is given, followed by its Function. Following this, the Scope Location is given. (Scope Location corresponds to the starting address of each test.) Note that these locations can differ from those contained in the diagnostic listing due to future changes in the diagnostic. In this event, use the location listed in the printout. The same holds true for the HLT Locations. The HLT Location corresponds to an error detected within a specific test. These locations may differ from the actual printout, but are relative to the test locations. This is followed by a listing of problems and probable malfunctions. These malfunctions are not exclusive and are not based on extensive field experience with the RS03.

Loading instructions are found in the diagnostic listing. A scoping subroutine call is placed between each test; it records the starting address of each test as it is entered in location "LAD". If a scope loop is requested, the current test will be looped upon. Switch 11 set on a 1 inhibits iterations of tests.

3.2.2 Troubleshooting in PDP-11 Systems

In the PDP-11 System, there are two diagnostics provided: the Static Test (MAINDEC-11-DZRSB) and the Data Reliability Test (MAINDEC-11-DZRSC). The arrangement of tests in the Static Diagnostic is such that basic functions are tested first, and for the most part, are stand-alone tests. The later tests are based upon the functions of earlier tests. If errors are detected with this diagnostic, it is advisable to get a complete error typeout from the failing test(s) to facilitate analysis of the failure.

The PDP-11 Reliability Diagnostic is a full exerciser that uses the surface of the disk to fulfill its function; any data that was on the disk prior to testing is destroyed. These are dynamic tests that check many functions simultaneously. This diagnostic should be run long enough to allow a statistical analysis of errors to be made. These errors can be analyzed for correlative indications, e.g., same address.

A complete set of flow diagrams is given as a special part of the Reliability Diagnostic.

3.2.3 Problem Identification (Head/Disk Assembly)

Data errors indicated by either OPI or DCK, which occur at random addresses, are usually caused by faulty read/write electronics or phase-locked loop. Heads and disk should not be replaced for this type problem.

Timing errors indicated by DTE, may be either timing amp or timing head problems.

Data errors indicated by either OPI or DCK, which occur consistently in one or more address locations, may be caused by Head Matrix, Head Cable, Head, or Disk.

Data Head Problems – When data errors occur consistently at a particular disk address (i.e., track and sector), first determine the data head associated with this location. Tracks 20 through 27, for example, are located on head block 20; for lower head locations see Figure 3-2.

Once the faulty location is determined, detach the head cable on that head block assembly and swap it with the cable on a head block assembly which has no problems. For example, if errors occur on track 63, head block 60 is indicated. Since no errors occur on any of the tracks 70 through 77, the head cables to head blocks 60 and 70 should be swapped and the diagnostics rerun. If the error remains on track 63, the head cable or the Head Matrix module is at fault; if the error moves to track 73, a head or the disk is at fault.

Return the proper cable to the head block making errors and disconnect the cables from all other head blocks associated with that Head Matrix module (M7758) (i.e., if head block is 00, 10, 20, or 30, remove all in that set but the one making errors; if 40, 50, 60, or 70, remove all in that set except the one making errors.) Then, in Conversation Mode, write and read the data pattern making the error on only the track making the error.

For example, the errors may occur on track 63. Reconnect the 60 cable to the 60 head block. Remove the cables from the 40, 50, and 70 head blocks. Using the Conversation Mode, write and then read the data pattern making errors on track 63.

If the error still exists and spare tracks are available, install a spare, as described in Paragraph 3.4.3. If no spare heads are available, first replace the head block assembly as described in Paragraph 4.8; if errors still persist, replace the disk as described in Paragraph 4.9.

When running with only the head connected that is making errors, and the other heads disconnected, and no errors occur, replace the disconnected head cables, one at a time, writing and reading the track which had made errors, between each cable replacement, until replacing a cable causes the problem to return. Then replace the head block which causes the problem to return, using the procedure described in Paragraph 4.8.

Table 3-1
PDP-11 Static Diagnostic Tests Troubleshooting Chart

Test Title	Function	Scope Location*	HLT Location*	Problem	Probable Malfunction Electrical
On-line Drives Test	Sets Error bits in RSER, causing Attention Summary bits to set in RSAS; does this for all drives. If no bits set in RSAS, tests Drive 0.	1312	1760	No Drive found; will test Drive 0.	1. RH11 MASSBUS transceiver. 2. RS03 MASSBUS transceiver. 3. Control Bus Handshake logic (M7755). 4. Attention Summary register Read logic (M7759). 5. TRC2 MASS FAIL H asserted.
RS Register Reset Test	Sets all R/W bits in the RS registers, then clears them with Reset; checks to see if they have cleared.	2020	2114	CS2 bits not cleared.	1. RH11 test.
			2134	DPR and MOL not set.	1. MASSBUS transceiver. 2. Control Bus logic (M7755). 3. Status Register Multiplexer (M7770). 4. Output Buffer (M7754).
			2146	RDY not set.	1. Output Buffer 2. Bit 1-6 set, no clear reaching drive.
			2156	BA register not set.	1. RH11 test.
			2166	DA not cleared.	1. MASSBUS transceiver. 2. Control Bus logic. 3. Output Buffer.
			2176	RSER not cleared.	1. MASSBUS transceiver. 2. Control Bus logic. 3. Output Buffer. 4. Error Register Multiplexer (M7770).
			2210	RSMR bits not cleared.	1. MASSBUS transceiver. 2. Control Bus logic. 3. Output Buffer. 4. Maintenance Register Multiplexer (M7759).
			2222	WC changed.	1. RH11 problem.
			2232	RSAS not cleared.	1. MASSBUS transceiver. 2. Control Bus logic. 3. Output Buffer 4. Attention Summary Register Read logic (M7759).

*NOTE: The addresses contained in these columns apply to DZRSB Rev B.

Table 3-1 (Cont)
PDP-11 Static Diagnostic Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
RSCS Clear Test	Sets all R/W bits in the RS registers, then clears them by MOVing #40→CS2; checks to see if they have cleared.	2234	2342	RSCS2 not cleared.	1. RH11 problem.
			2362	RSCS1 not cleared.	1. MASSBUS transceiver 2. Control Bus logic 3. Output Buffer.
			2372	RSBA not cleared.	1. RH11 problem.
			2402	RSDA not cleared.	1. MASSBUS transceiver. 2. Control Bus logic 3. Output Buffer
			2412	RSER not cleared.	1. MASSBUS transceiver. 2. Control Bus logic. 3. Output Buffer. 4. Error Register Multiplexer.
			2424	RSMR bits not clear.	1. MASSBUS transceiver. 2. Control Bus logic 3. Output Buffer. 4. Maintenance Register Multiplexer.
			2436	WC changed.	1. RH11 problem.
All register set and clear Tests	Tests to see if the function bits (7:1) in RSCS1 can be set.	2440	2470 2510 2530	RSCS1 Function bits did not set.	1. MASSBUS transceivers. 2. Control Module (M7755) 3. Control Register (M7759). 4. Output Buffer (M7754)
	Tests to see if the function bits in RSCS1 can be cleared.	2532	2556	RSCS1 Function bit did not clear.	(same as above)
	Tests all writeable bits in RSCS2 by setting all writeable bits, setting alternate writeable bits, setting complement alternate bits, and finally clearing all writeable bits.	2560	2574 2624 2644 2664 2710	RSCS2 R/W bits did not clear.	(RH11 Test)

Table 3-1 (Cont)
PDP-11 Static Diagnostic Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
All register set and clear tests (Continued)	Tests to see if all RSBA bits can be set. (patterns: all ones, alternate ones and zeros, complement alternate ones and zeros.)	2720	2740 2760 3000	All RSBA bits did not set.	(RH11 Test)
	Floats a (1) through RSBA	3002	3026	All RSBA bits did not set.	(RH11 Test)
	Clears the RSBA bits	3034	3056	All RSBA bits did not clear.	(RH11 Test)
	Sets all RSWC bits (all ones, alternate ones and zeros, complement alternate ones and zeros.)	3060	3100 3120 3140	All RSWC bits did not set.	(RH11 Test)
	Floats a (1) through RSWC	3142	3166	All RSWC bits did not set.	(RH11 Test)
	Clears the RSWC	3174	3216	All RSWC bits did not clear.	(RH11 Test)
	Sets all RSDA bits (all ones, alternate ones and zeros, complement alternate ones and zeros.)	3220	3240 3260 3300	All RSDA bits did not set and/or clear.	1. MASSBUS transceivers 2. Control module (M7755) 3. Address register (M7754) 4. Output Buffer (M7754)
	Floats a (1) through RSDA	3302	3326		
	Sets all RSDA bits and then clears them	3334	3356		
	Sets selected RSER bits	3360	3400 3420	All RSER bits did not set and/or clear.	1. Control module (M7755) 2. Error register (M7770)
	Sets selected RSER bits	3422	3442		
	Sets selected RSER bits	3444	3464		
	Sets selected RSER bits and clears them	3466	3510		
	Sets selected RSMR bits	3512	3546	All RSMR bits did not set and/or clear.	1. Control module (M7755) 2. Maintenance register (M7759) 3. Maintenance register Multiplexer (M7759)
	Sets selected RSMR bits and clears them	3550	3574		
	Sets selected RSMR bits	3576	3632		
	Sets selected RSMR bits and clears them	3634	3670		
RSWC & RSDA & RSBA Random Number Test	Generates random numbers and loads them into RSWC, RSDA, and RSBA.	3672	3754	RSWC bad.	RSWC→RH11 Test
			4024	RSDA bad.	RSDA→Control module (M7755) Address register module (M7754)
			4100	RSBA bad.	RSBA→RH11 Test

Table 3-1 (Cont)
PDP-11 Static Diagnostic Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
Odd Byte Instruction Tests	Tests odd byte instruction on RSCS1	4112	4142 4162	Did not load. Did not load.	1. RH11 problem 2. Control module (M7755) 3. Control register (M7759) 4. Control Register Multiplexer (M7759)
	Tests odd byte instruction on RSCS2	4164	4226	Load byte did not work.	(RH11 Test)
	Tests odd byte instruction on RSWC	4230	4256 4276	Did not load. Did not load.	(RH11 Test) (RH11 Test)
	Tests odd byte instruction on RSBA	4300	4326 4346	Did not load. Did not load.	(RH11 Test) (RH11 Test)
RSCS2 Data Late Test	Does a read from empty silo to cause DLT and TRE error. Clears DLT and TRE by setting TRE in RSCS1.	4352	4402 4414 4434 4452	No DLT. No DLT and/or TRE. TRE and/or SC not clear. DLT not clear.	(RH11 Test) (RH11 Test) (RH11 Test) (RH11 Test)
RSDB all 0s and all 1s Test	Loads RSDB with a word of 0s and a word of 1s. Waits for OR to set and then checks silo output. Error indicates OR did not set or that silo is not functioning.	4454	4526 4542 4560	OR did not set. Can't float 0s thru DB. DB bad.	(RH11 Test) (RH11 Test) (RH11 Test)
Silo locations Test	Puts a binary count in each silo location and checks output for 66 words, then tests DLT error by loading 67 words. Checks for no silo change on 67th word.	4562	4624 4650 4662 4714 4732	OR not a (1). Cannot match 66 locations. OR not (0). DLT did not set on 67 words. Silo moved.	(RH11 Test) (RH11 Test) (RH11 Test) (RH11 Test) (RH11 Test)
Silo Floating (1) and (0) Test	Loads the silo with a word of zeros and floats a 1 through the word. Loads the silo with an all (1) word and floats a zero through. Checks the silo output.	4734	5014 5040	DB did not bubble correctly. DB wrong.	(RH11 Test)

Table 3-1 (Cont)
PDP-11 Static Diagnostic Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
No Op Function Test	The No Op function (Code 01_8) is tested without error bits set. All the registers are checked to see if they were altered.	5050	5114 5124 5136 5146 5160 5172	GO bit not cleared. Error bits not all (0). WC incorrect. DA not zero. BA moved. AS set, shouldn't have.	1. RH11 problem 2. Control module (M7755) 3. Control register and/or function decoding (M7759)
	The No Op function is tested with error bits set. All registers are checked to see if they were altered.	5174	5216 5260 5272 5304 5314 5326 5340 5352	AS bit not set. GO bit not cleared. ERR bit not zero. WC wrong. DA not zero. BA moved. AS not set. ER changed.	1. RH11 problem 2. Control module (M7755) 3. Control register and/or function decoding (M7759)
Read In Preset Function Test	The Read In Preset function (Code 21_8) is tested without error bits set. All registers are checked to see if they were altered.	5354	5420 5430 5442 5452 5464 5476 5510	GO not cleared. Error bits not all (0). WC wrong. DA not zero. BA moved. AS set, shouldn't have. CS1 incorrect	1. RH11 problem 2. Control module (M7755) 3. Control register and/or function decoding (M7759)
	The Read In Preset function is tested with error bits set. All registers are checked to see if they were altered.	5512	5534 5576 5610 5622 5632 5644 5656 5670 5702	AS bit not set. GO not cleared. ERR bit not zero. WC wrong. DA not zero. BA moved. AS did not set. ER changed. CS1 Incorrect	1. RH11 problem 2. Control module (M7755) 3. Control register and/or function decoding (M7759)

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
Drive Clear Function Test	Sets all R/W bits in RSDA, RSWC, RSER, and RSMR and then does a Drive Clear Function. Checks all registers for correct data.	5704	5772 6002 6012 6040 6052 6064 6076	Unit # in CS2 modified. DA not zero. ER not cleared. MR bits did clear. CS1 incorrect. AS set, shouldn't have. WC incorrect.	1. RH11 problem 2. Control module (M7755) 3. Control register and/or function decoding (M7759) 4. Maintenance register (M7759) 5. Address register (M7754) 6. Error register (M7770) 7. Attention Summary register (M7759)
A Port One Word Write Function Test	Clears all registers, sets RSWC to -1, moves -1 into OUTBUF. Loads RSBA with address of OUTBUF. Does a write; tests RDY bit for 0 then waits for it to set. RDY doesn't set, times out to error and checks for error conditions. Tests RSDA for correct address, tests W/C for 0.	6100	6144 6154 6174 6202 6214 6226 6236 6250 6272 6314 6324	WC moved. BA moved. RDY not zero. RDY never came up. RSDA not ok. Error during transfer. WC failed to increment. RSDS not ok. CS2 bad. BA failed to increment. Errors set	Any errors in this test (not attributable to the RH11) are most likely associated with the Data Bus logic. Refer to detailed descriptions of Timing Amp Logic module (G092), Format module (M7771), Data Register module (M7753), and Encode/Decode module (M7751).
A Port One Word Read Function Test	Sets up RSDA, RSBA, RSWC and OUTBUF for a Read Function. Does a read and test RDY for 0, and waits for RDY to set. If not set, times out for error and checks. Tests RSDA, RSCS1, RSCS2, RSWC, RSBA, and OUTBUF for correct data.	6326	6366 6374 6406 6420 6430 6452 6474 6512	BUSY not set. TIMEOUT: RDY did not set. RSDA not ok. RSCS1 not ok. WC overflow. CS2 incorrect. RSBA failed to increment. OUTBUF incorrect.	Any errors in this test (not attributable to the RH11) are most likely associated with the Data Bus Logic. However, before troubleshooting Read problems, it is recommended that correct performance of a Write function be verified. This can be done by looping on the previous test. Check the Miller encoded output of both Encode/Decode modules (ED2 WRT DATA PULSE L) (M7751) and also check that the drive is writing at the proper time and only during sector 00 (ED2 WRT GATE L). (Continued)

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
(Continued)					After verifying the Write function, loop on this test. By checking the signal RW2 RD DATA PULSE L for correct Miller encoded data from each surface, the problem can be localized to the analog portion for incorrect Miller data (Read/Write Detection module, G182; Head Matrix module, M7758; Alternate Track Option module M7756; head-disk assembly) or the digital/phase locked loop portion for correct Miller data (Encode/Decode module, M7751; Data Register module, M7753; Format module, M7771). Refer to the detailed description of the appropriate module for further troubleshooting information.
A Port Write Check Test	Sets up RSDA, RSBA, RSWC and OUTBUF as in Read Function. Does a Write Check Function and tests RDY for 0, & then for RDY to set. Times out if not set and checks for error. Tests RSCS2, RSCS1, RSDA, RSWC, and RSBA for correct data.	6514	6556 6564 6606 6620 6632 6642 6664	BUSY did not set. BUSY did not clear. CS2 incorrect. Error during transfer. DA not incremented. WC overflow. RSBA did not increment.	Since a write check function is identical to a read function in the **RS03,** any errors occurring in this test that do not occur in the previous test are likely due to a malfunction of the RH11.
B Port One Word Write Function Test	Same as the One Word Write Function Test for the A Port. **NOTE** If a one word transfer continues to set NEM, the program will update address by 4K until it reaches 28K. If no transfer, it will skip Write, Read, and Write Check.	6666			Testing B Port is RH11 Test

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
B Port One Word Read Function Test	Same as the One Word Read Function Test for the A Port	7104			Testing B Port is RH11 Test
B Port Write Check Test	Same as Write Check Test for the A Port	7300			Testing B Port is RH11 Test
RSCS2 Unit No. Timing Test	Deselects then selects Unit # in RSCS2. Checks timing.	7474	7570 7602 7614 7624 7636 7660 7702	RDY never came up. Error during transfer. RSDA not ok. WC overflow. RSDS not ok. CS2 incorrect. BA failed to increment.	(RH11 Test)
BAI in RSCS2 Test	Tests current address inhibit in RSCS2. Sets BAI, then does a one word write and checks to see that RSBA did not increment after transfer.	7704	7740 7762 7772 10006	RDY did not set. RSBA not ok. Errors indicated. BAI did not set.	(RH11 Test)
NEM in RSCS2 Test	Tests the non-existent memory error bit in RSCS2.	10010	10050 10072 10104 10134	RDY never came up. CS2 incorrect. TRE did not set on NEM. CS2 incorrect.	(RH11 Test)
Block Search Function Test	Tests the Block Search Function, PIP and DRY bits and ADDR CONF bit.	10136	10206 10232 10246 10300 10312 10356 10372 10404 10416 10430 10434	Could not find sector 32. DRY not cleared. PIP not set. PIP did not clear. SC did not set. RSAS incorrect. RSAS did not clear. ATA did not clear. BA moved, shouldn't. WC moved, shouldn't. DRY never came up.	1. Control register and/or function decoding (M7759) 2. Status register (M7770) 3. Status register Multiplexer (M7770) 4. ATA flip-flop (M7770)

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
Illegal Function Code 3 to 51 Test	Sets RSBA, RSWC and RSDA to do a legal function. Illegal function is then executed. Tests for errors, and for correct data in RSBA, RSWC, and RSDA. Repeated for illegal functions 3 to 51. **NOTE** To loop on the function, put function into ILLTAB and zero the following location. Set switch 14.	10436	10536 10550 10562 10604 10626 10640 10652 10662 10674 10706	CS1 incorrect. ILF did not set. ERR did not set. CS2 incorrect. Wrong drive answered. BA moved on an illegal function. WC moved. DA moved. ILF did not clear. CS1 errors did not clear.	1. Control register and/or function decoding (M7759) 2. Error register (M7770) 3. RH11 problem
Illegal Function Code 53 to 77 Test	Same as previous test except illegal functions 53 to 77 are executed. **NOTE** To loop on the function, put function into ILFTB2 and zero the following location. Set switch 14.	10714	11034 11046 11060 11070 11120 11132 11144 11172 11220 11232 11246 11256	CS1 incorrect. ILF did not set. ERR did not set. DA moved. CS2 incorrect. BA moved on illegal function. WC moved. CS2 incorrect. BA moved on illegal function. WC moved. Errors did not clear. ER did not clear.	1. Control register and/or function decoding (M7759) 2. Error register (M7770) 3. RH11 problem.
Illegal Function Code 67 Test	Same as previous test except that illegal function 67 is executed.	11264	11350 11372 11404 11416 11520 11542 11554 11574 11604 11614	RSBA incorrect. CS2 incorrect. RSER is incorrect. ER did not clear. RSBA incorrect. CS2 incorrect. RSER incorrect. CS1 errors did not clear. RSER did not clear. RSAS did not clear.	1. Control register and/or function decoding (M7759) 2. Error register (M7770) 3. RH11 problem

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
PAR in RSER Test	Sets PAR in RSER and checks. Tests for ERR, ATA, and DRY set in RSDS. Clears all RS registers and checks.	11616	11646 11660 11672	ERR did not set on PAR. PAR did not clear. Error bits did not clear.	1. Control module (M7755) 2. Error register (M7770) 3. Status register (M7770)
Look Ahead Test	Checks for RSLA (12:15) bits to be clear.	11674	11706	Bits 12:15 did not clear.	1. Timing Amp Logic Module (G092) 2. Control module (M7755)
	Checks to see if sector fraction bits are moving.	11710	12016	SF bits moving.	1. Timing Amp Logic module (G092) 2. Control module (M7755)
	Sets RSDA to 0, waits for ADDRS CONF bit in RSMR to set, then compares the sector portions of RSDA & RSLA. Increments RSDA and repeats until RSDA = 10000. If the address confirm bit does not set within timeout, error occurs.	12020	12070 12202 12206	Add Conf bit always (1). Good=DA, Bad=LA. Add Conf bit never set.	1. Control module (M7755) 2. Look-Ahead register (G092) 3. Sector Address Compare logic (M7754) 4. Maintenance register (M7771)
Parity Test	Tests parity logic (if there is parity memory on the system). In less than 28K, writes bad parity in a memory location then attempts a write to the drive from that location. This causes a PE.	12210	12360 12372	CS2 incorrect. CS1 incorrect.	(RH11 Test)
A Port Write Check Error Test	Writes a word of (0)s, floats a (1) thru the word in the bus address location, and performs a write check. The WCE bit in RSCS2 should set and should result in a set of TRE in RSCS1. Clears these bits, writes a word of all ones on the disk, and repeats the operation by floating a (0) thru a word of (1)s in OUTBUF.	12432	12612 12636 12650 12672 12716 12730	CS2 incorrect. WCE did not catch bad word. TRE did not set. RSBA did not increment. CS2 incorrect. TRE did not clear.	(RH11 Test)

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
B Port Write Check Error Test	Same as A Port Write Check Error Test but on Port B.	12774	13176 13222 13234 13256 13302 13314	CS2 incorrect. WCE did not catch bad word. TRE did not set on WCE. RSBA did not increment. CS2 incorrect. TRE did not clear.	(RH11 Test)
RSCS2 Program Error Bit Test	Attempts a data transfer while control is already performing one. Checks PGE to set and that TRE sets as a result. Word count is checked for nonzero (current operation should have been aborted by PGE).	13366	13442 13454 13464 13506 13516 13526 13552 13564	RDY never came up. TRE did not set on PGE. RSAS not ok. CS2 incorrect. WC = (0) ? RMR not set. PGE did not clear. SC did not clear.	(RH11 Test)
RSDA Modification test of RMR in RSER	Attempts modification of RSDA during execution of a write command and checks for RMR and ERR to set; clears these bits.	13566	13646 13660 13672 13704 13716 13730 13742	RDY never came up. ER should = 4. DA not modified. ERR did not set. CS1 incorrect. RMR did not clear. CS1 incorrect.	1. Control module (M7755) 2. Error register (M7770) 3. Status register (M7770) 4. Data Bus Initiation/Termination logic (M7771)
RSER Modification test of RMR in RSER	Attempts modification of RSER during execution of a write command and checks for RMR and ERR to set; clears these bits.	13744	14012 14024 14036 14050	RDY never came up. ER should = 4. ERR did not set. CS1 incorrect.	1. Control module (M7755) 2. Error register (M7770) 3. Status register (M7770)

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
RSCS1 Modification test of RMR in RSER	Attempts modification of RSCS1 during execution of a write command and checks for RMR and ERR to set; clears these bits.	14054	14122 14134 14146 14160	RDY never came up. ER should = 4. ERR did not set. CS1 incorrect.	1. Control module (M7755) 2. Error register (M7770) 3. Status register (M7770) 4. Data Bus Initiation/Termination logic (M7771)
RSAS Modification test of RMR in RSER	Attempts modification of RSAS during execution of a search command and checks for RMR and ERR to remain clear; clears these bits.	14164	14262 14272 14304 14316 14332	RDY never came up. ER should = 0. DS should = 110600. CS1 incorrect. CS1 incorrect.	1. Control module (M7755) 2. Attention Summary register (M7759) 3. Control register (M7759) 4. Status register (M7770)
DCK in RSER Test	Fills one sector with all ones, then performs a MASSBUS INIT while writing zeros in the same sector. Reads that sector and checks for DCK to set and that ERR sets as a result; clears these bits.	14334	14536 14600 14612 14624 14646 14664 14722 14734	RDY never came up. DCK did not set. ERR did not set by DCK. CS1 incorrect. CS2 incorrect. Transfer did not stop at end of sector. BA incorrect. DCK did not clear.	1. RH11 problem 2. CRC register (M7753) 3. Error register (M7770) 4. Control module (M7755)
Disk Address Register Test	Tests ability of the RSDA to increment. Loads 7777 in RSDA, does a one word write; checks RSDA = 10000.	14766	15026 15040	RDY did not come up. DA did not increment.	1. Address register (M7754)
Invalid Address Error Test	Sets RSDA to 17777 and does a one word write; checks for IAE to set in RSER and that this results in setting ERR, ATA, and SC. Checks that all bits clear.	15042	15116 15130 15142 15154	IAE did not set. ERR did not set in DS. SC did not set. ER did not clear.	1. Address register (M7754) 2. Error register (M7770)
Non-Existent Disk Error Test	Attempts a one word write to a drive known to be off line or not in the system. Checks for NED to set and for that to set TRE. Clears bits by loading a (1) into TRE.	15156	15232 15250 15263 15272 15312 15332	RSER changed. CS2 incorrect. TRE not set by NED. RSAS changed. NED did not clear. NED did not set.	1. RH11 problem 2. Control module (M7755) (drive responding when not addressed).

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
AOE in RSER & LBT in RSDS Test (With Overflow)	Sets RSDA to its last address and writes one sector +1 word; checks for a set of AOE and LBT. Checks the resultant set of ERR, ATA, TRE, and SC. Checks that all bits clear.	15426	15502 15514 15526 15536 15552 15562	RDY did not set. AOE did not set. LBT did not set. SC did not set. ATA did not clear. AOE did not clear.	1. Address register (M7754) 2. AOE error logic (M7771) 3. Error register (M7770) 4. Status register (M7770)
AOE in RSER & LBT in RSDS Test (Without Overflow)	Sets RSDA to its last address and writes one sector. Checks for a set of LBT but no set of AOE. Checks the resultant errors and does a clear. Checks for clear.	15564	15640 15650 15662 15672 15706	RDY did not set. Errors indicated. LBT did not set. Error flag set. ATA did not clear.	1. Address register (M7754) 2. AOE error logic (M7771) 3. Error register (M7770) 4. Status register (M7770)
Execute Function with Error bit set Test	Sets error bits in RSER. Checks that SC sets in RSCS1 and that the proper Attention Summary register bit sets. Clears ATA by loading a (1) into Attention Summary register which results in clearing SC. Does a one word read and checks for GO to be clear. Checks for correct values in other registers.	15710	15742 15754 15772 16004 16046 16066 16110 16122 16134 16144 16156 16170 16202	AS bit not set. CS1 incorrect. AS did not clear. SC did not clear. GO not cleared. Errors did not clear on GO. CS2 incorrect. ERR did not set. WC incorrect. DA did not clear. BA moved. AS did not set. ER changed.	1. Command/Decode module (M7759) 2. Error register (M7770) 3. ATA flip-flop (M7770) 4. Control module (M7755)
PAT and MCPE Test	Sets Parity Test bit (PAT) in RSCS2. Reads drive register and checks RSCS2 (RH11 generates even parity with PAT set). Writes drive register and looks for PAR error in RSER. Checks RSAS, then clears drive.	16204	16242 16262 16304 16316 16332 16354	CS2 incorrect. PAR did not set. AS did not set. CS1 errors did not set. CS1 incorrect. PAT did not clear.	1. RH11 problem 2. Address Register module (M7754) (Control Bus Parity logic)

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
Set PAT and then load Function Test	Attempts to perform a Read function with Pat set. Checks that function was loaded into RSCS1 and was not performed. (Control register in RS03 loads, but GO is not set).	16356	16444 16456 16470	CS1 was loaded. BA moved. WC moved.	1. Control register (M7759)
Do Read and then set PAT Test	Attempts to perform a Read function, then sets PAT bit to produce a Data Bus parity error in the RH11. Checks for no drive errors, then clears.	16472	16562 16604 16616 16626 16642	MCPE did not set. CS2 incorrect. ERR did not set. Errors were set. MCPE did not clear.	1. Data Register module (M7753)
Test PAR by setting PAT	Attempts to perform a Write function, then sets PAT bit to produce a Data Bus parity error in the RS03.	16644	16740 16762 16774 17006 17022 17032	MCPE did not set. CS2 incorrect. ERR did not set. PAR did not set. MCPE did not clear. PAR did not clear.	1. Data Register module (M7753)
Ability to fill last Sector Test	Writes the last sector on the disk and checks RSDS for LBT to be set.	17034	17110 17120 17132 17142 17156	RDY did not set. Error indicated. LBT did not set. SC did not set. ATA did not clear.	1. Status register (M7770)
Test for (0)s in a partially filled sector.	Writes a complete sector with all (1)s then does a one word write. Does a Write Check to see that the remaining 63 words were written as zeros.	17160	17462	WCE indicated.	1. RH11 Test
Extended Memory Address Test	Note: If memory management is available; if not, this test traps and transfers to end of test.	17464	17664 17700 17750 17764 20004	Status error after 2 word write. CS2 did not compare. Error after reading 2 words. CS1 did not compare. Data compare error.	1. RH11 Test

(Continued)

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
(Continued)			20066	Error after reading 2 words.	
			20100	CS1 did not compare.	
			20146	Error while reading 2 words.	
			20162	CS1 did not compare.	
			20200	Data compare error.	
Program Interrupt Test	The program enables the interrupt and does a one word write. Program should not trap until the processor is dropped to priority 4. Moves 300 into RSCS1.	20230	20302	No interrupt.	1. RH11 Test
			20322	IE did not clear.	
	Checks for no disk interrupt at PS5	20324	20416	RDY never came up.	1. RH11 Test
			20426	PS incorrect.	
	Checks for no disk interrupt at PS4	20430	20526	PS incorrect.	
			20530		
			20544	IE did not clear.	
	Tests interrupt on error	20546	20634	Program didn't interrupt.	1. RH11 Test
			20650	CS1 incorrect.	
Dynamic Function Test	While one drive is reading, the unit number in RSCS2 is modified. If there is another drive on the system, a Search function is done on it. This is all done while the first drive is still reading. **NOTE** Search function will be done only if there are 2 drives. If this test fails, check second drive before trying to debug test.	20654	21154	CS1 incorrect.	System Test
			21156		
			21166	WC overflow.	
			21210	CS2 incorrect.	
			21232	RSBA failed to increment.	
			21252	DA not correct.	
			21264	RSDA not ok.	

Table 3-1 (Cont)
PDP-11 Static Diagnostics Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
Write Lock Test	Tests the ability of the RS03 logic to prevent a write operation occurring at all addresses from zero up to the address set into the lock out switches. This test requires operator intervention to set this lockout boundary address to various addresses during the test.	23744	24012	Enter unit #	1. Address Register module (M7754)
			24140	Set Wrt lock enable.	2. Error register (M7770)
			24160	DS incorrect.	3. Data Bus Initiation/Termination logic (M7771)
			24200	DS incorrect.	
			24242	Set Wrt Lk Sw 0.	
			24254	DS incorrect.	
			24274	DS incorrect.	
			24336	Set Wrt Lk Sw 1.	
			24350	DS incorrect.	
			24370	DS incorrect.	
			24432	Set Wrt Lk Sw 2.	
			24444	DS incorrect.	
			24464	DS incorrect.	
			24526	Set Wrt Lk Sw 3.	
			24540	DS incorrect.	
			24560	DS incorrect.	
			24622	Set Wrt Lk Sw 4.	
			24634	DS incorrect.	
			24654	DS incorrect.	
			24716	Set Wrt Lk Sw 5.	
			24730	DS incorrect.	
			24750	DS incorrect.	
			25034	DS incorrect.	
			25046	ER incorrect.	
			25062	WLE cleared.	
			25134	Disk written on with WLE set.	
			25174	Reset all Wrt Lk Sws.	
			25206	WLE did not clear.	

Table 3-1 (Cont)
PDP-11 Static Diagnostic Tests Troubleshooting Chart

Test Title	Function	Scope Location	HLT Location	Problem	Probable Malfunction Electrical
TKSEL	This routine allows the operator to select the unit number, word count, and data pattern via the Teletype, and to select the desired address and function to be performed (Write or Read) via the processor switch register. Switch register bits 0–11 are transferred to the RSDA and bit 12 determines the function. If Bit 12=1=Read. If Bit 12=0=Write. The program loops continuously, using the specified inputs and performs no error typeouts. This is basically a simplified version of the conversation mode routine found in DZRSC. This routine is very useful in checking several particular tracks and/or sectors.				

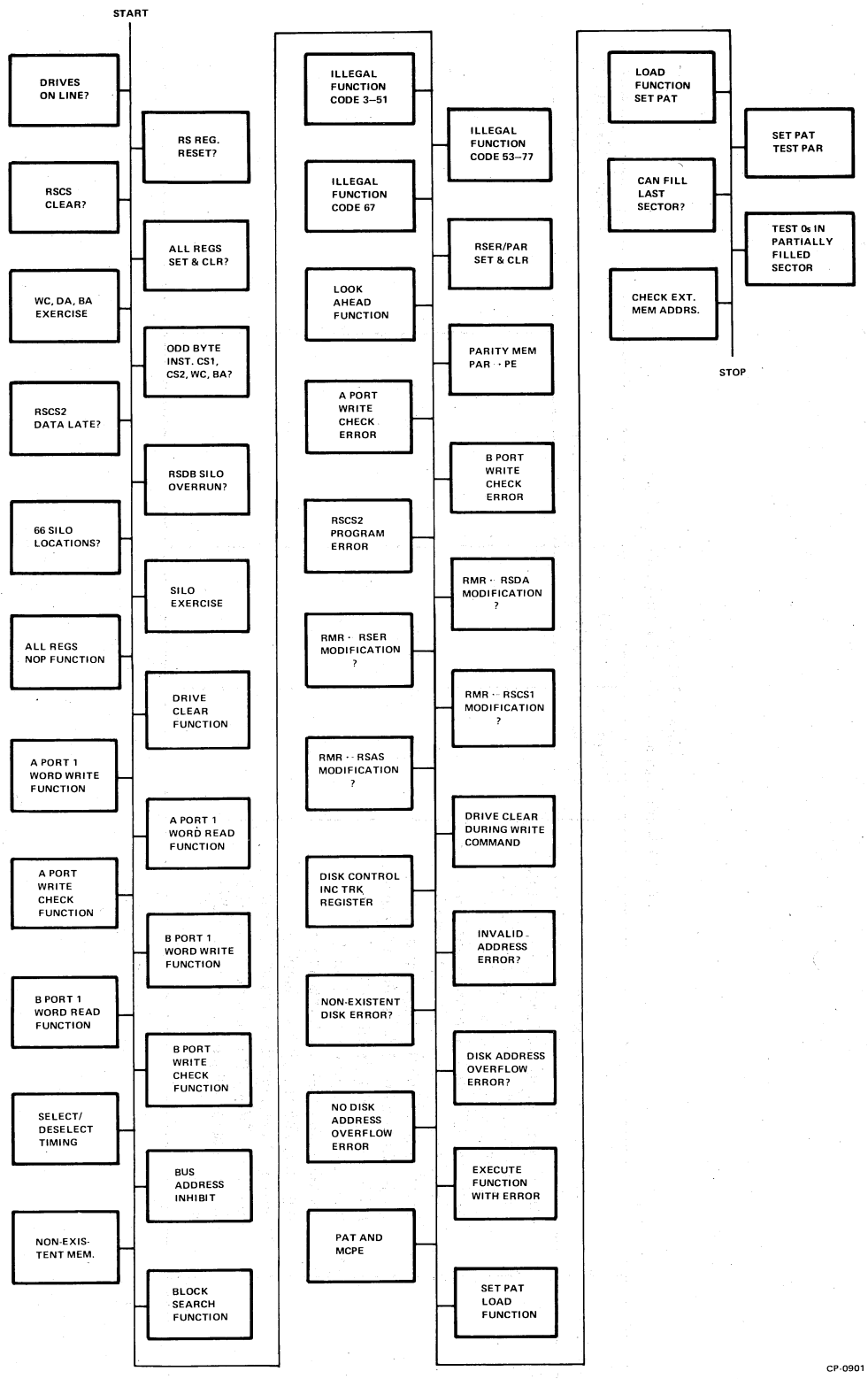

Figure 3-1 PDP-11 Diagnostic Tree

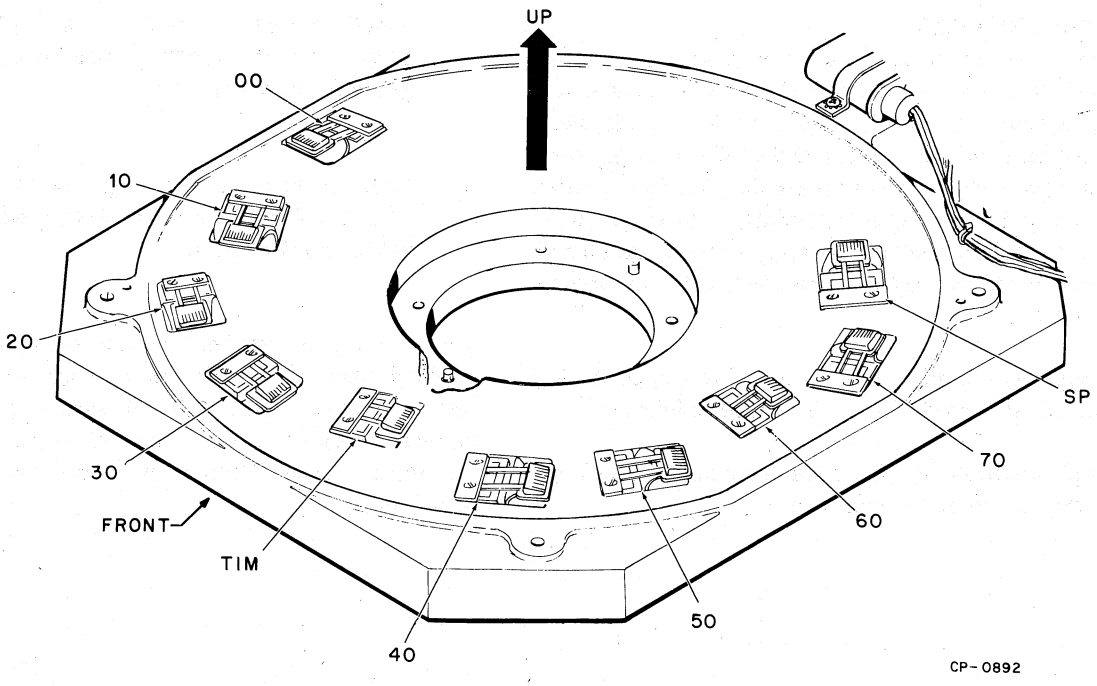

Figure 3-2 Top View of Lower Casting
Showing Head Locations

Example – errors were on track 63, cables to head blocks 40, 50, and 70 were removed, and writing and reading the data pattern on track 63 yielded no errors. If the cable to head block 40 is replaced and track 63 is written and read with no errors, the cable to head block 50 is replaced, and now the error returns when track 63 is written and read, replacement of head block 50 is indicated.

Timing Head Problems – When timing errors occur consistently, first try the spare timing track or rewrite the timing tracks, following the procedure in Appendix F.

If errors still persist after a number of rewrite attempts, write timing tracks on head block 30. Connect the TIM cable from the Timing Amp (G092) to head block 30 and the 30 head cable to the timing head block (TIM); rerun the diagnostics. If timing errors persist, the fault is in the timing head cable or the Timing Amp (G092). If data errors now occur on tracks 33 or 34, the timing head block or the disk is at fault.

First, replace the head block as described in Paragraph 4.8. If the problem persists, replace the disk as described in Paragraph 4.9.

3.3 LOGIC MODULES

This subsection contains information pertaining to the individual modules in the RS03. Each subparagraph contains detailed theory discussions of the module, with timing diagrams (where needed) and troubleshooting flow diagrams. Discussions are not arranged in functional order as they are in Section II; all information pertaining to an individual module is contained in a single subparagraph and can be considered as a separate pamphlet within the overall Service Manual.

Each pamphlet is headed by a set of references pertaining to the module discussed. These are defined as follows:

Logic Assembly Slot Location – the physical location of the module in the logic rack.

Signal Mnemonic Prefix – the alphabetical code assigned to the module, used to prefix all signals generated by that module.

Logic Elements – a list of the main functional blocks of logic contained in the module, used as headings for the theory discussions.

These theory discussions are not system-oriented. It is assumed that the reader is familiar with the system operation of the RS03. If the system orientation of a particular module is not familiar, it is recommended that the reader review Section II before using a particular pamphlet.

3.3.1 Address Module M7754

Logic Assembly Slot Location – AB10

Signal Mnemonic Prefix – AD

Logic Elements – **Control Bus Parity Checker/Generator**
Desired Address Register & Sector Compare Logic
Write Protect Logic
Control Bus Output Buffer

The numbers of the descriptive text under the paragraph titles, correspond to the numbered boxes of the flowchart. Wherever possible, the text sequence represents the logical sequence of events for a particular operation, however, the text sequence does not indicate simultaneous events. This fact is represented by parallel paths on the flowchart.

LOGIC ELEMENT THEORY OF OPERATION

Control Bus Parity Checker/Generator
The Control Bus Parity Checker/Generator is connected to the Control Bus lines (C(00:15)) and examines the parity of all Control Bus input/output data.

During a *register write* operation, Control Bus data is simultaneously applied to the checker/generator and to the selected register. If the total number of ones on the 17 Control Bus lines (C(00:15) plus CPA) is odd, the parity checking logic negates the signal AD2 ASYNC PAR ERR L. If, however, the number of ones on these lines is even, AD2 ASYNC PAR ERR L is asserted.

During a *register read* operation, TRC2 WO DCPAI H is forced high, enabling the parity checker/generator to generate the appropriate parity bit. Whenever a register which contains an even number of ones is read, parity bit AD2 DCPAO L is asserted. If the register contains an odd number of ones, AD2 DCPAO L is negated.

Desired Address Register & Sector Compare Logic
The Desired Address register consists of a synchronous-load binary counter. The Sector Compare logic compares the current sector with the desired sector address and indicates when they are the same. These logic elements function in the following manner (Figure 3-3):

1. If drive is not performing a Search or data transfer, FT5 ADDRS SEARCH H is negated, enabling Address register inputs.

2. Controller places binary address of the desired track and sector on the Control Bus (TR2 WO DCB (15:00) H).

3&4. On the trailing edge of CN2 LD DES ADDR REG L, the binary address is strobed into the Desired Address register and AD3 LAST BLK H is negated (if it had been asserted from a previous operation).

5. The address is tested. If the address is invalid, enable INV ADD gate E17–8 to assert AD2 INV ADDR H.

6&7. If, however, the address is valid, AD2 INV ADDR H is not asserted and the six read/write head selection signals (Address register bits 6–11) are applied to the Write Protect logic.

8. A check is made to see if the Write Protect logic is enabled (E9–4). If it is, a check is made to see if the desired track is protected (E5–3). Refer to the Write Protect Logic discussion, following. If the desired track is protected, the result of this comparison asserts AD3 PROTECTED L (E9–6).

9. If the desired track is *not* protected, AD3 PROTECTED L is negated.

10. A check is made to see if the desired address is the last track and sector on the disk (E12–8). If the address is 7777_8, AD2 MAX ADDR H is asserted.

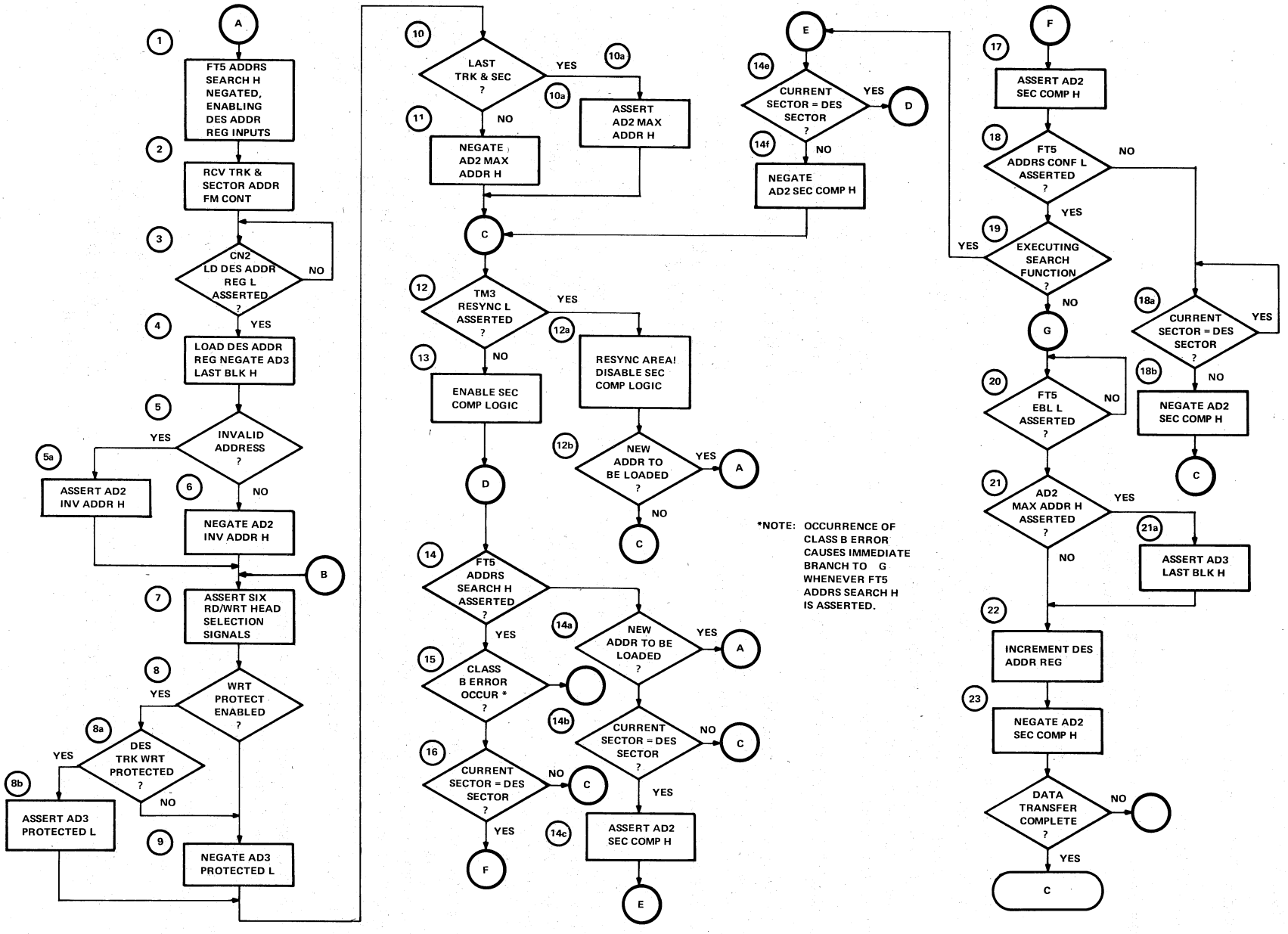

Figure 3-3 Address Register Troubleshooting Flow Chart

11&12. If the desired address is not the largest possible, AD2 MAX ADDR H is negated and a check is made to see if TM3 RESYNC L is asserted. If it is, the Resync Area is indicated and the Sector Compare logic is disabled (E4–3). If the Desired Address register is loaded during the Resync period, all of the previous steps are repeated. If it is not, the flow loops to point C until TM3 RESYNC L is negated.

13&14. When TM3 RESYNC L is negated, the Sector Compare logic is enabled, and if the drive is not performing a Search or data transfer (FT5 ADDRS SEARCH H is not asserted), a check is made to see if a new address is to be loaded (14a). If a new address is to be loaded, the flow returns to point A. If it is not, Desired Address register bits 0–5 are compared by the Sector Comparator to the current sector (14b). If the desired sector does not match the current sector, the flow loops back to point C. If the desired sector does match the current disk sector (TM4 SEC ADD 0H–4H), AD2 SEC COMP H is asserted (14c). AD2 SEC COMP H remains asserted until the desired sector no longer matches the current sector (because the disk has moved), at which time it is negated (14e,f).

15. If at the time that the Sector Compare logic was enabled (13), FT5 ADDRS SEARCH H *was* asserted (14), a check is made to see if any Class B errors exist. If one exists, the flow branches to point G to generate EBL.

NOTE

A Class B error will cause an immediate branch to point G whenever FT5 ADDRS SEARCH H is asserted.

16–19. If a Class B error does not exist, when the current disk sector matches the desired sector, AD2 SEC COMP H is asserted (17). A check is made to see if FT5 ADDRS CONF L is asserted (18). If it is not asserted at this time, it indicates that FT5 ADDRS SEARCH H became asserted *during* the desired sector and another complete disk revolution is required to reach the *beginning* of the desired sector. If the drive is executing a Search (19), the flow is to point E. The Search function is completed when FT5 ADDRS CONF L is asserted. This results in the negation of FT5 ADDRS SEARCH H and returns the flow to the loop of steps 12–14.

20–22. At the end of every sector transferred, FT5 EBL L is asserted. If the signal AD2 MAX ADDR H (E9–13) is asserted (indicating the last logical sector on the disk) the drive asserts AD3 LAST BLK H (E9–8). FT5 EBL L is used to increment the Desired Address register.

23. When the Desired Address register is incremented, at this point it is one greater than the current sector, so AD2 SEC COMP H is negated (E8–6).

24. If the data transfer *is* complete, the flow returns to point C and continues to loop. If it is *not* complete, it returns to point B and continues.

To summarize this flow chart, AD2 SEC COMP H is asserted *any time* the desired sector compares with the current sector. If the desired sector is changed by modifying the Desired Address register, all of the checks are repeated and the Sector Compare Logic simply compares the new desired sector to the current sector. During Resync, no comparisons are made.

Write Protect Logic

The Write Protect Logic consists of comparator E22, E26, and a set of eight switches in a dual-in-line package. To write protect a group of tracks, starting from track 00_8, the binary address of the highest track in the group is set into the switches and the Write Protect Logic is enabled.

NOTE

An open switch = logic 1 for that bit in the address. A switch is open (logic 1) when it is depressed toward the labelling in etch on the module.

Thus, whenever the track address from the Desired Address register is equal to, or lower than, the switch setting, AD3 PROTECTED L is asserted.

NOTE

Switch 1 is an enable switch for the Write Protect Logic; in order to enable, switch must be opened.

Figure 3-4 shows the Write Protect Logic enabled and the switches set to protect all tracks from 00_8 up to and including 31_8.

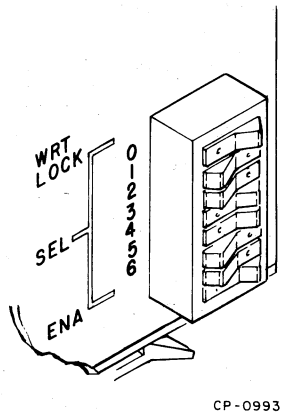

Figure 3-4 Write Protect Switches Showing Write Protect Logic Enabled and Set to Protect Tracks 00_8–31_8

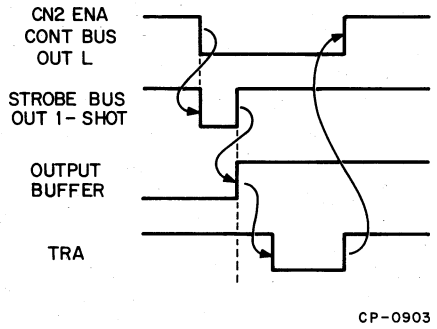

Figure 3-5 Control Bus Output Buffer Timing Diagram

Control Bus Output Buffer

The Output Buffer consists of four quad-D flip-flops with tri-state outputs (E1, E10, E15, and E23). (A tri-state output can be a logic 1, a logic 0, or a high impedance "off" state.) During a *register read*, CN2 ENA CONT BUS OUT L fires 120-ns Strobe Bus Out one-shot (E13) and simultaneously enables the outputs of the Output Buffer (Figure 3-5). When the Strobe Bus Out one-shot times out, data from a selected register has settled on the wired-OR register bus (WO BOXX L) and is then strobed into the Output Buffer. Although the selected register may change during the Control Bus read operation, the Control Bus data is frozen at the time the one-shot times out.

NOTE

The input to the Output Buffer is a Wired-OR bus, which is low asserted or low = logic 1. The Output Buffer is non-inverting, so its output is also low asserted.

PERFORMANCE CHECKS

See Table 3-1.

TROUBLESHOOTING

See Table 3-1.

3.3.2 Command Decode Module M7759

Logic Assembly Slot Location – AB09

Signal Mnemonic Prefix – CD

Logic Elements – **Control Register & GO Flip-Flop**
Illegal Function (ILF) Detection Circuitry
Command Decoder
Clear GO Circuitry
Attention Summary Register Logic
Maintenance Register

The numbers of the descriptive text under the paragraph titles, correspond to the numbered boxes of the flowchart. Wherever possible, the text sequence represents the logical sequence of events for a particular operation, however, the text sequence does not indicate simultaneous events. This fact is represented by parallel paths on the flowchart.

LOGIC ELEMENT THEORY OF OPERATION

Control Register & GO Flip-Flop (Figure 3-6)

1. The drive receives 5-bit command function plus GO bit (TRA 2 WO DCB (05:00)H) from the Controller.

2&3. The leading edge of CN2 LD CONT REG L loads the function code into the drive Control register.

4&5. If ST4 COMP ERR L is asserted, CD2 SET ATA H is asserted. If not, CD3 CLR ATTN H is asserted.

6&7. If ST4 COMP ERR L is asserted on the trailing edge of CN2 LD CONT REG L, the GO flip-flop is not set, CD2 SET ATA H is negated, and the operation is terminated.

8&9. If, however, ST4 COMP ERR L is not asserted, the GO flip-flop is set and CD3 CLR ATTN H is negated on the trailing edge of CN2 LD CONT REG L.

ILF Error Detection

10–13a. If the Control register contains a function code ending in 3, 5, or 7, the flow branches to point C, where CD2 SET ILL FUNCT ERR L is asserted. This signal sets the ILF flip-flop in the Error register. In this event, GO is cleared (14), the function decode signals and CD2 SET ILL FUNCT ERR L are negated (15), and the operation terminates.

Command Decoding

11&12. If the function code does not end in 3, 5, or 7, the Control register output is decoded and the function decode signals are asserted.

13. If the function code = 41_8, CD2 SET ILL FUNCT ERR L is asserted, setting the ILF flip-flop in the Error register. When CN2 CLK DRIVE ACTIVE H is asserted, the Drive Active flip-flop is clocked set.

14. After the command has been executed, the GO and Drive Active flip-flops are cleared; the function decode signals are negated (along with CD2 SET ILL FUNCT ERR L if it was asserted), and the operation is terminated.

NOTE

Function codes 51_8, 61_8, or 71_8 produce CD2 TRANS L.

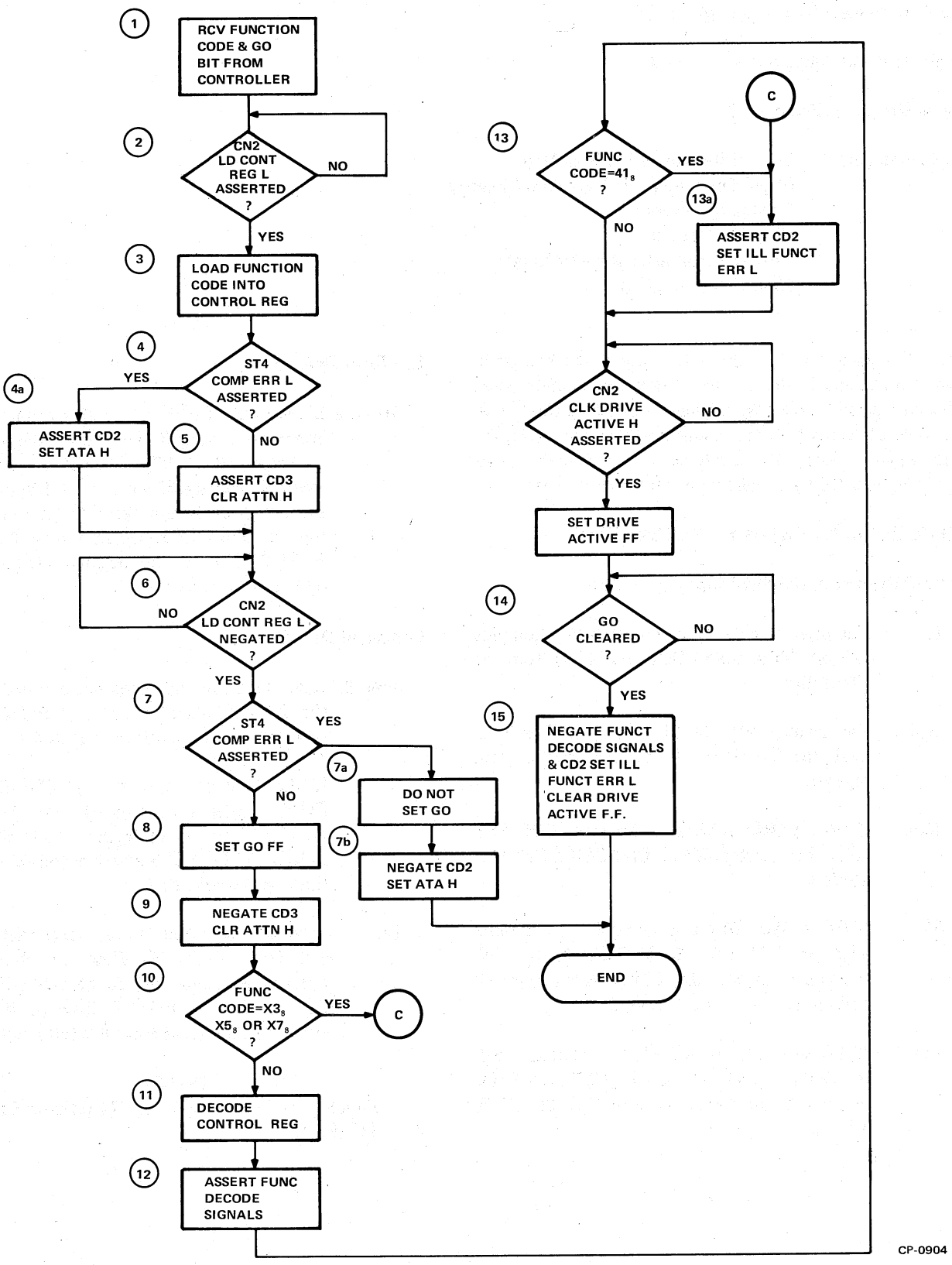

Figure 3-6 Command Decode Troubleshooting Flow Chart

Clear GO Circuitry
Consists of two 50-ns one-shots plus the necessary gating components. This circuit produces an output signal which resets the GO flip-flop (E14–1) and the Drive Active flip-flop (E14–13) at the following times:

- at data transfer termination by trailing edge of FT5 CLR GO L
- at completion of Search function by assertion of FT5 ATTN L
- whenever the Controller issues a Drive Clear, Read-In Preset, or No Op command
- whenever the Controller asserts MASSBUS INIT.

Attention Summary Register Logic
The Attention Summary register logic can be divided into two parts: one for reading this register, the other for writing into it.

Attention Summary Register Read
When the Controller reads the Attention Summary register, the drive asserts one bit in the register, which corresponds to that drive's unit number, if that drive's ATA status bit is set. The Attention Summary register (Read) decoder (E4) is enabled by FT5 ATTN L•CN2 RD ATTN SUM REG L. When enabled, this decoder (with open-collector outputs) asserts one of eight lines on the wired-OR register bus, corresponding to the drive's unit number.

Attention Summary Register Write
When the Controller writes into the Attention Summary register, the drive clears its ATA status bit, if the bit being written, corresponding to the drive's unit number, is a (1). The Attention Summary register (Write) multiplexer selects the one line on the Drive Control Bus that corresponds to the drive's unit number. The multiplexer output is enabled by CN2 WRT ATTN SUM REG L. If the Drive Control Bus signal, corresponding to the drive's unit number, is a (1), the signal CD3 CLR ATTN H is asserted when the multiplexer output is enabled.

Maintenance Register
The read/write bits of the Maintenance register are on this module. On the leading edge of CN2 LD MAINT REG L, the Drive Control Bus lines are strobed into the Maintenance register (E12).

The register multiplexers (E5 and E6) enable either the Control register or Maintenance register (00:07) onto the wired-OR register bus whenever either one is read by the Controller. These multiplexers also have open-collector outputs.

PERFORMANCE CHECKS
See Table 3-1.

TROUBLESHOOTING
See Table 3-1.

3.3.3 Control Module M7755

Logic Assembly Slot Location – AB07

Signal Mnemonic Prefix – CN

Logic Elements – **Drive Selection Circuitry**
Register Selection Decoders
RMR and ILR Detection Circuitry
Transfer Timing Circuitry
Power Fail Logic
Unit Number Selection Switches

The numbers of the descriptive text under the paragraph titles, correspond to the numbered boxes of the flowchart. Wherever possible, the text sequence represents the logical sequence of events for a particular operation, however, the text sequence does not indicate simultaneous events. This fact is represented by parallel paths on the flowchart.

LOGIC ELEMENT THEORY OF OPERATION

Drive Selection Circuitry (Figure 3-7)

1. The Controller asserts the Drive Select, the Register Select, the C TO D, and C(00:15)+ CPA lines.

2. The drive compares the Drive Select lines DS(0:2) with the unit select switches. If they do not match, a check is made of the Register Select lines to see if the Attention Summary register is addressed (04_8). If not, the operation is ignored (by this drive).

3. If either the Drive Select comparison is true, or if the Attention Summary register is addressed, the Selected flip-flop is enabled.

4. If TRC2 MASS FAIL is asserted, the operation ends (no Control Bus transfers occur if TRC2 MASS FAIL H is asserted).

Register Select Decoder (Figure 3-7)

5&6. If TRC2 MASS FAIL is not asserted, the Selected flip-flop is set upon assertion of TRC2 DEMAND H from the Controller.

7&8. TRC2 DEMAND H strobes the C TO D flip-flop with the state of TRA2 C TO D H and enables the Control Bus Active flip-flop (E14-1, -2, -3, -8, -9, -10).

Register Write (Figure 3-7)

9. CN2 C TO D (1) H assertion permits RMR checking.

10–12. Setting the Selected flip-flop triggers the 150-ns one-shot (E15–10). This asserts CN2 CHK BUS PARITY L and CN2 CONT BUS ACTIVE L.

13&14. If either of the two most significant bits of the register select code (TRA2 REG SEL 3 or 4 H) are asserted, an Illegal Register error is generated. If they are *not* asserted, CN2 SET ILL REG ERR L is negated.

15&16. If a write into the Control, Error, or Desired Address register is attempted while a Search or data transfer is occurring, a Register Modification Refused (RMR) error is generated. If CD2 DRIVE ACTIVE (1) H is not asserted, CN2 SET RMR ERR L is not asserted.

17–19. When E15–5 times out (set in Step 10), CN2 CHK BUS PARITY L and CN2 SET ILL REG ERR L are both negated and 120-ns one-shot (E15–1) is triggered.

20. Once again, the RS lines are checked for an Attention Summary register code (04_8). If true, CN2 WRT ATTN SUM REG L is asserted and the flow progresses to point (B).

21. If RS=(04_8) is not decoded, and if CN2 SET RMR ERR L is asserted, the load register signal is not produced.

22. If either of the two most significant bits of the register select code (TRA2 REG SEL 3 or 4 H) is asserted, the "load register" signal is likewise not produced.

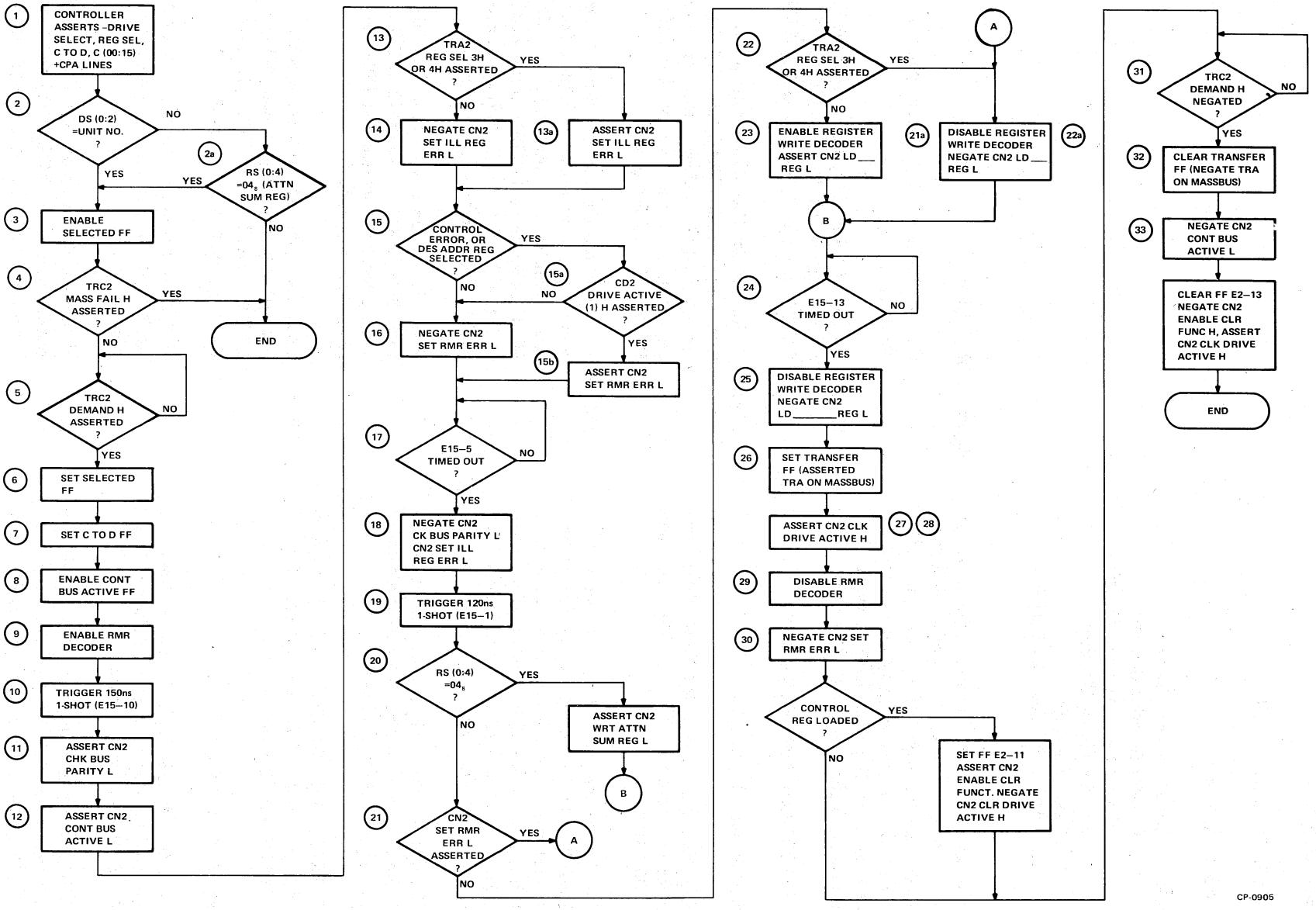

Figure 3-7 Control Module Register Write Troubleshooting Flow Chart

23. If neither TRA2 REG SEL 3 or 4 H is asserted, the address of the desired register is decoded and the appropriate load register signal (CN2 LD XXX REG L) is asserted.

24&25. When E15–13 times out, the Register Write Decoder is disabled and CN2 LD XXX REG L is negated.

26. This sets the Transfer flip-flop that asserts TRA on the MASSBUS.

27–30. The Selected flip-flop is then cleared, the RMR Decoder is disabled, and CN2 SET RMR ERR L is negated (if it was asserted). If the Control register is the register just written, flip-flop E2–11 is clocked set. This asserts the signal CN2 ENABLE CLR FUNC H and negates the signal CN2 CLK DRIVE ACTIVE H.

31–33. When TRC2 DEMAND H is negated, the Transfer flip-flop is cleared, negating TRA on the MASSBUS. This negates CN2 CONT BUS ACTIVE L, clears flip-flop E2–13, negates CN2 ENABLE CLR FUNC H, asserts CN2 CLK DRIVE ACTIVE H, and the operation ends.

Register Read (Figure 3-8) – (Drive Selection Circuitry)

1. The Controller asserts the Drive Select and the Register Select lines, and negates the C TO D line.

2. The Register Read Decoder asserts CN2 RD XXX REG L.

3. The drive compares the Drive Select lines DS(0:2) with the unit select switches. If they do not match, a check is made of the Register Select lines to see if the Attention Summary register is addressed (04_8). If not, the operation is ignored (by this drive).

4. If either the Drive Select comparison is true, or if the Attention Summary register is addressed, the Selected flip-flop is enabled.

5. If TRC2 MASS FAIL H is asserted, the operation ends.

Register Select Decoder (Figure 3-8) – (During Read)

6&7. If TRC2 MASS FAIL H is not asserted, the Selected flip-flop is set upon assertion of TRC2 DEMAND H from the Controller.

8. TRC2 DEMAND H strobes the C TO D flip-flop with the state of TRA2 C TO D H.

Register Read (Figure 3-8)

9. TRC2 DEMAND H assertion enables the Control Bus Active flip-flop.

10. Setting the Selected flip-flop triggers the 150-ns one-shot (E15–10).

11&12. If either of the two most significant bits of the Register Select Code (TRA2 REG SEL 3 or 4 H) are asserted, an Illegal Register error is generated. If they are *not* asserted, CN2 SET ILL REG ERR L is not asserted.

13&14. At this point, CN2 CONT BUS ACTIVE L is asserted, resulting in the assertion of CN2 ENA CONT BUS OUT (L & H).

15. This combination enables the MASSBUS transmitters and disables the MASSBUS receivers.

16–18. When E15–5 times out, CN2 SET ILL REG ERR L is negated (if it was asserted), and the 120-ns one-shot (E15–1) is triggered.

19. When E15–13 times out, the Transfer flip-flop is set, thereby asserting TRA on the MASSBUS.

21–23. The Selected flip-flop is then cleared and when TRC2 DEMAND H is negated, the TRANSFER flip-flop is cleared, negating TRA on the MASSBUS.

24&25. This negates CN2 CONT BUS ACTIVE L, resulting in CN2 ENA CONT BUS OUT (L & H) being negated.

26. This combination causes the MASSBUS transmitters to be disabled, and the MASSBUS receivers to be enabled, thereby ending the operation.

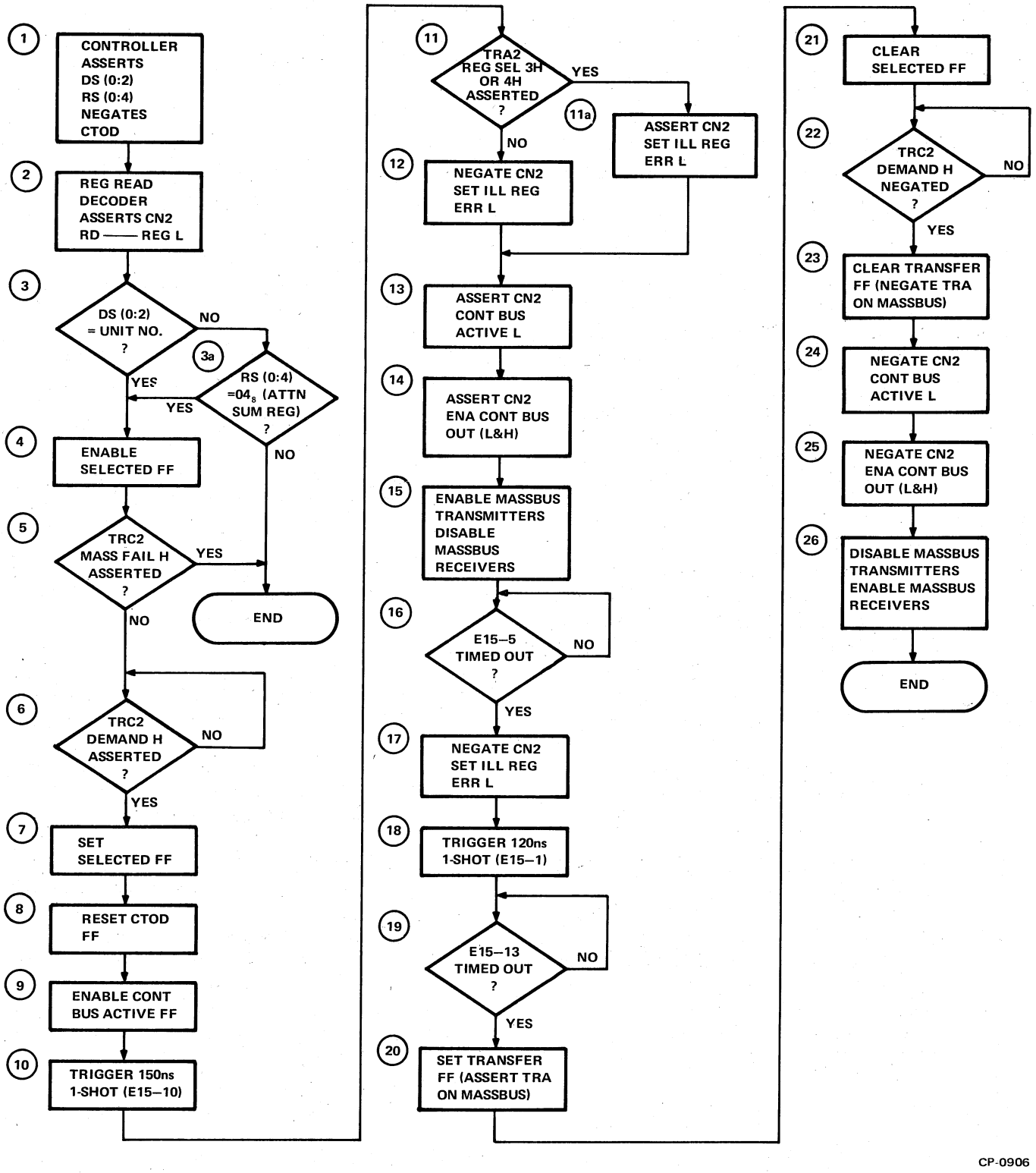

Figure 3-8 Control Module Register Read Troubleshooting Flow Chart

RMR Error Detection
An RMR error occurs if a write into the Control, Error, or Desired Address register is attempted while CD2 DRIVE ACTIVE (1) H is asserted. The Drive Active flip-flop (Command Decode module E14) is set at the end of a "handshake" sequence, when the Control register is loaded, and is cleared by the same signals that clear GO.

Transfer Timing (Figure 3-9)
This circuit contains a 150-ns one-shot (E15), a 120-ns one-shot (E15) and a TRANSFER flip-flop (E21).

During a register write, this circuit allows an RMR check and a Control Bus parity check to be performed prior to loading the selected register.

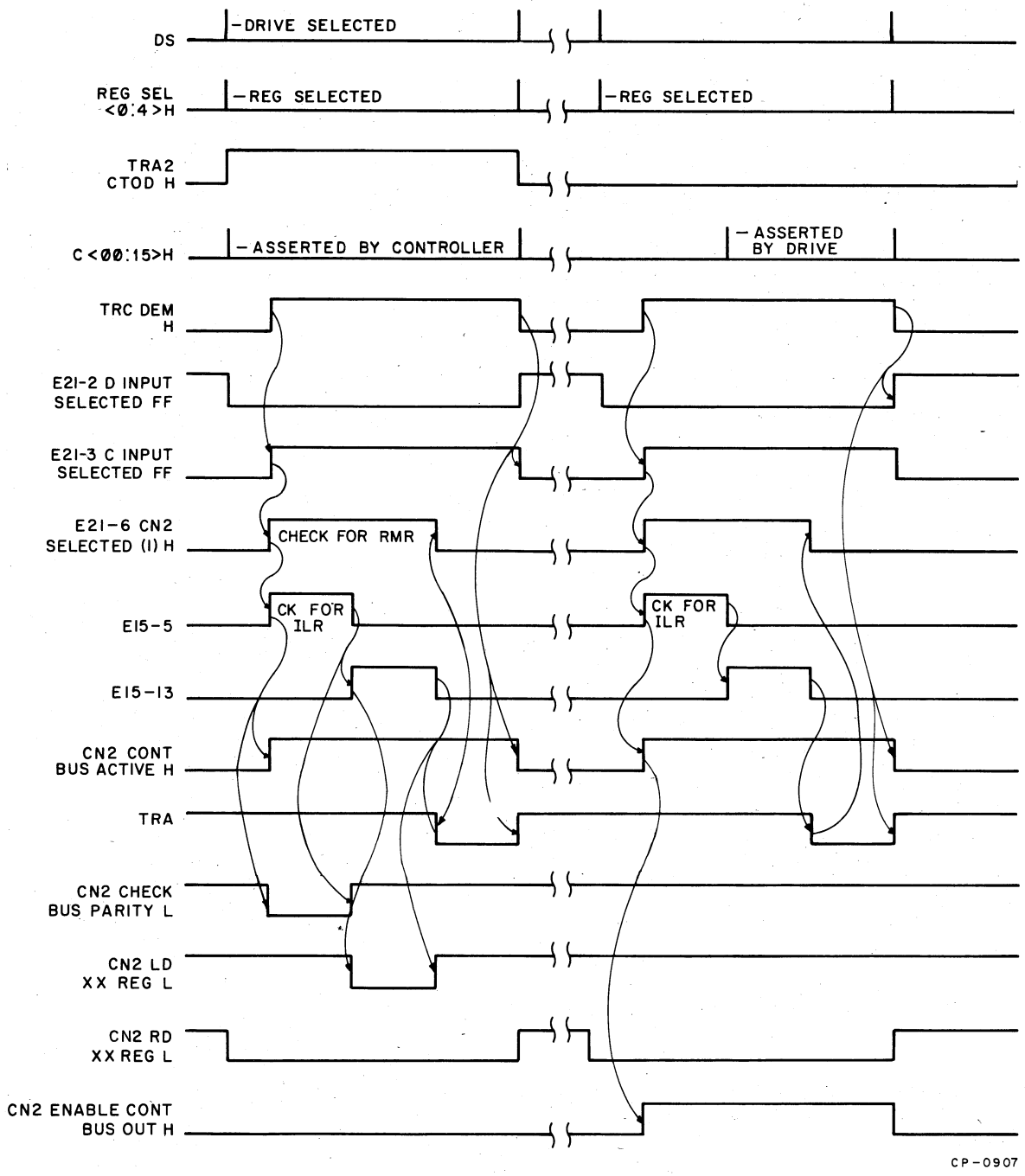

Figure 3-9 Control Bus Transfer Timing

During a register read, this circuit allows data to be clocked from the selected register into the Output Buffer, prior to assertion of Transfer.

Power Fail Logic

Power fail logic that maintains protection for the RS03 is contained on this module. Its operation during a "power up" and a "power down" sequence is described as follows:

Power Up (Figure 3-10)

1–3. Relay K1 is normally-closed. When the power supply is turned on, the MASSBUS drivers are disabled (CN2 DSBL MBUS DRVRS L) to prevent erroneous signals from being sent to the Controller or any other on-line drives. The Write Amps are disabled (CN2 DSBL WRITE AMP L) to prevent any erroneous data from being written on the disk, and the two signals CN2 C AND M REG CLR L (E8–13) and CN2 DRI CLR L (E13–8) are asserted.

4. These conditions prevail until power has come up to a safe value (PS2 SAFE L) (E10–1).

5. When PS2 SAFE L is asserted, the 13 second one-shot (E3–10) is triggered. This guarantees that the motor is fully up to speed if it had been previously off.

6–8. When E3–12 times out, the K1 coil driver, E17–3, is turned on and transistor switch E17–5, is turned off.

9–11. When K1 contacts open, the signals asserted in Step 3 are negated and the 100-ns one-shot (E3–1) is triggered.

12–13. This clears the Selected flip-flop and pulses CN2 PWR UP ATTN L. The drive is now "Ready".

Power Down (Figure 3-11)

1. In the event of a power failure, PS2 SAFE L is negated.

2–4. This triggers 20-μs one-shot (E9–10) and when E9–12 times out, K1 coil driver, E17–3, is turned off.

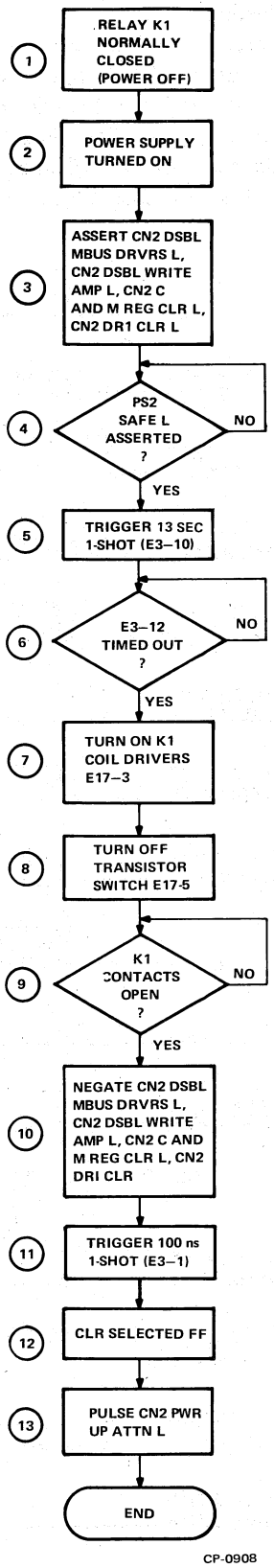

Figure 3-10 Power Up Flow Chart

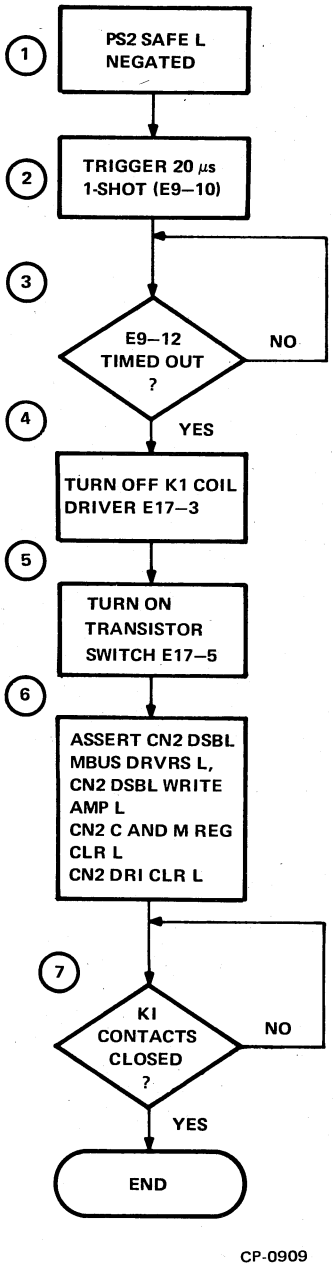

Figure 3-11 Power Down Flow Chart

5&6. When E17–3 turns off, transistor switch, E17–5, is turned on to assert CN2 DSBL MBUS DRVRS L, CN2 DSBL WRITE AMP L, CN2 C AND M CLR L, and CN2 DRI CLR L.

7. Finally, the K1 contacts close until the next power up sequence.

Unit Number Selection Switches (Figure 3-12)
The Control module contains a set of rocker switches in a dual-in-line package, mounted in location E20. Three of the switches are labelled in etch on the module with the numbers *1, 2,* and *4.* The numbers correspond to the weight of each switch in determining that drive's unit number. When the switch is depressed *toward* the weighting number, that number is added to the unit number. For example, to select unit number 5, depress the switches toward the numbers *1* and *4.*

PERFORMANCE CHECKS
See Table 3-1.

TROUBLESHOOTING
See Table 3-1.

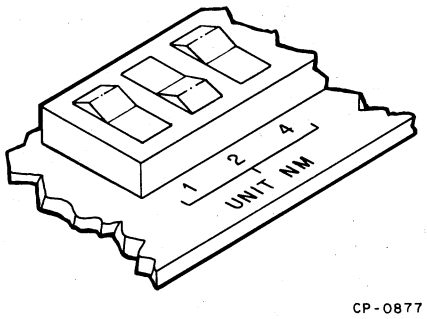

Figure 3-12 Unit Number 5 Switch Setting

3.3.4 Data Register Module M7753

Logic Assembly Slot Location – AB12

Signal Mnemonic Prefix – DA

Logic Elements – **Data Buffer**
Data Bus Parity Checker/Generator
Shift Register
CRC Logic

The numbers of the descriptive text under the paragraph titles, correspond to the numbered boxes of the flowchart. Wherever possible, the text sequence represents the logical sequence of events for a particular operation, however, the text sequence does not indicate simultaneous events. This fact is represented by parallel paths on the flowchart.

LOGIC ELEMENT THEORY OF OPERATION

Data Buffer
The Data Buffer is a two-to-one multiplexer plus storage element. During a write operation, CD2 WRT L enables the Data Bus inputs (TR2 DDBI (00:17) H) to the Data Buffer and FT4 STROBE BUFF L strobes parallel data from the Data Bus into the Data Buffer. In a read operation, CD2 WRT L negation enables the Shift register inputs (DA3 SHIFT REG (00:17) H) to the Data Buffer and FT4 STROBE BUFF L clocks parallel data from the Shift register into the Data Buffer.

Data Bus Parity Checker/Generator (Figure 3-13)
Consists of a parity checker/generator (E9, E15, and E26), a Parity Check flip-flop (E7) plus the necessary gating components. The parity checker is connected to the output of the Data Buffer (18 data bits plus DPA) and examines each data word for odd parity during a write operation, as follows:

1&2. CD2 WRT L assertion removes the direct clear input to Parity Check flip-flop E7–13.

3–5. The assertion of FT4 STROBE BUFF L strobes write data from the Data Bus into the Data Buffer; the negation of that signal clocks the Parity Check flip-flop set (E7–11).

6. The Parity Checker checks the Data Buffer contents for odd parity. If even parity (parity error), the Parity Checker asserts high output from E26–6.

7. FT4 STROBE BUFF L negation produces DA2 SYNC PAR ERR H is parity error exists.

8&12. If the transfer is complete, Parity Check flip-flop (E7–13) is cleared and the operation is terminated.

7–9. If not, the next word on the bus is processed in similar fashion until the transfer is completed.

During a read operation, the Parity Generator determines the correct state of DA2 DDPAO L, corresponding to the 18 data bits in the word just read from the disk.

Shift Register
The Shift register converts a data word from parallel to serial during a write operation, or from serial to parallel for a read operation.

During a write operation, FT4 LOAD SR L enables the parallel inputs to the Shift register and the first FT4 RD OR WRT CLK L clocks the entire 18-bit data word from the Data Buffer into the Shift register. FT4 LOAD SR L is then negated and each successive FT4 RD OR WRT CLK L shifts a single data bit out of the last stage of the Shift register and simultaneously applies it to the CRC logic and the encoding logic on the Encode/Decode module.

During a read operation, ED2 NRZ RD DATA H bits from the Encode/Decode module are applied to the first stage of the Shift register. Each FT4 RD OR WRT CLK L serially shifts a data bit into the Shift register. When the entire 18-bit data word is loaded into the Shift register, FT4 STROBE BUFF L clocks the Shift register output into the Data Buffer.

CRC Logic
The Cyclic Redundancy Check (CRC) character is a 16-bit, mathematically-derived word, which is computed during the Shift register clocking of a write operation. During a

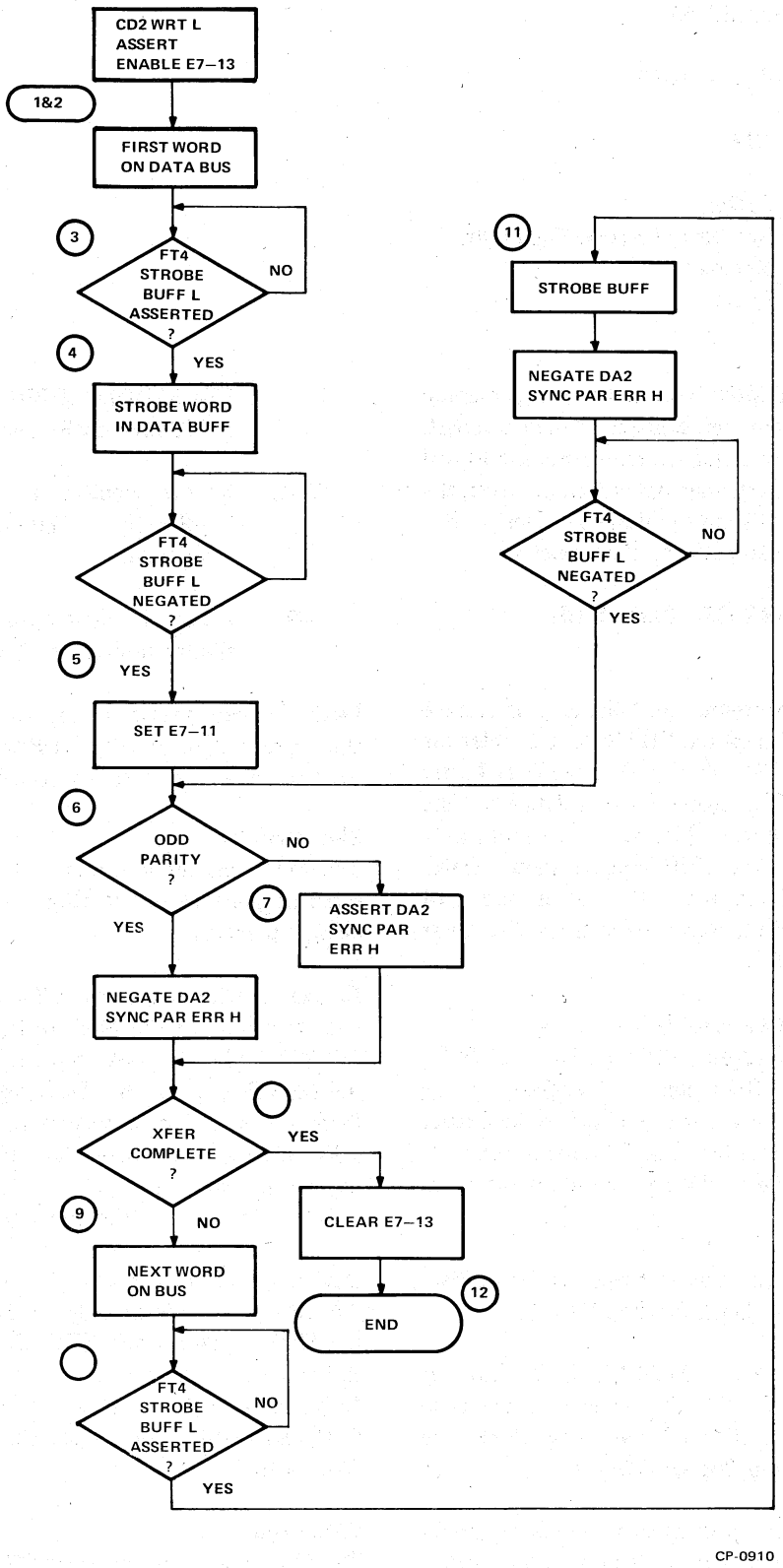

Figure 3-13 Parity Check Troubleshooting Flow Chart

write operation, as each data bit is shifted out of the Shift register, it is also simultaneously shifted into the CRC register in a manner such that the entire data block is divided by a pre-selected CRC polynominal ($x^{16}+x^{15}+x^{2}+1$).

The division remainder from this CRC computation is then recorded at the end of the data block as the CRC character.

During a read operation, as each data bit is shifted into the Shift register, it is shifted into the CRC register in exactly the same manner as it was during a Write. At the end of the data field, the CRC register should contain a pattern identical to the CRC character which follows. The CRC character read from the disk is then shifted into the CRC register. If all the data and CRC bits have been retrieved correctly, the CRC register should now equal zero. In other words, the division of the data, plus the CRC character by the CRC polynominal, yields a zero remainder.

The 16 outputs from the CRC register are wire-ORed to provide a simple zero-detect circuit. If any bit in the CRC register is a one, the output of the wired-OR is low. The assertion of FT4 STROBE BUFF L and FT3 CRC WD L checks the state of the wired-OR after the CRC word has been read. If the wired-OR is high at this time, there was no error in data or CRC; if the wired-OR is low at this time, DA3 SET DATA ERR L is asserted. For the following discussions, refer to Figure 3-14.

Write CRC

1. TM3 SEC PULSE L clears CRC register (E19, E24, and E30) and resets the last stage of Shift register (E28–1).

2. CD2 WRT L enables E13–2.

3–5. First FT4 RD OR WRT CLK L loads data word into Shift register and the most significant bit of the Shift register (DA3 SHIFT REG 17 H) is applied to the CRC logic. DA3 CRC INPUT H is recirculated and XORed with DA3 CRC FEEDBACK 0 H.

6&7. Successive FT4 RD OR WRT CLK L pulses shift serial data bits into CRC register.

8. FT3 CRC WD L assertion forces DA3 CRC INPUT H low.

9. Shift out contents of CRC register to Encode/Decode module.

Read CRC

1. TM3 SEC PULSE L clears CRC register and resets last stage of Shift register (E28–1).

10&11. DA3 NRZ RD DATA H is applied to E13-3, -4. DA3 CRC INPUT H is recirculated and XORed with DA3 CRC FEEDBACK 0 H.

12&13. Successive FT4 RD OR WRT CLK L pulses shift serial data bits into CRC register.

14&15. FT3 CRC WD L assertion enables Zero Detect gate E5–6.

16–18. If CRC register does not equal zero, enable CRC Check gate E6–4 and at FT4 STROBE BUFF L assertion, assert DA3 SET DATA ERR L. If the CRC register equals zero, DA3 SET DATA ERR L remains negated.

PERFORMANCE CHECKS

See Table 3-1.

TROUBLESHOOTING

See Table 3-1.

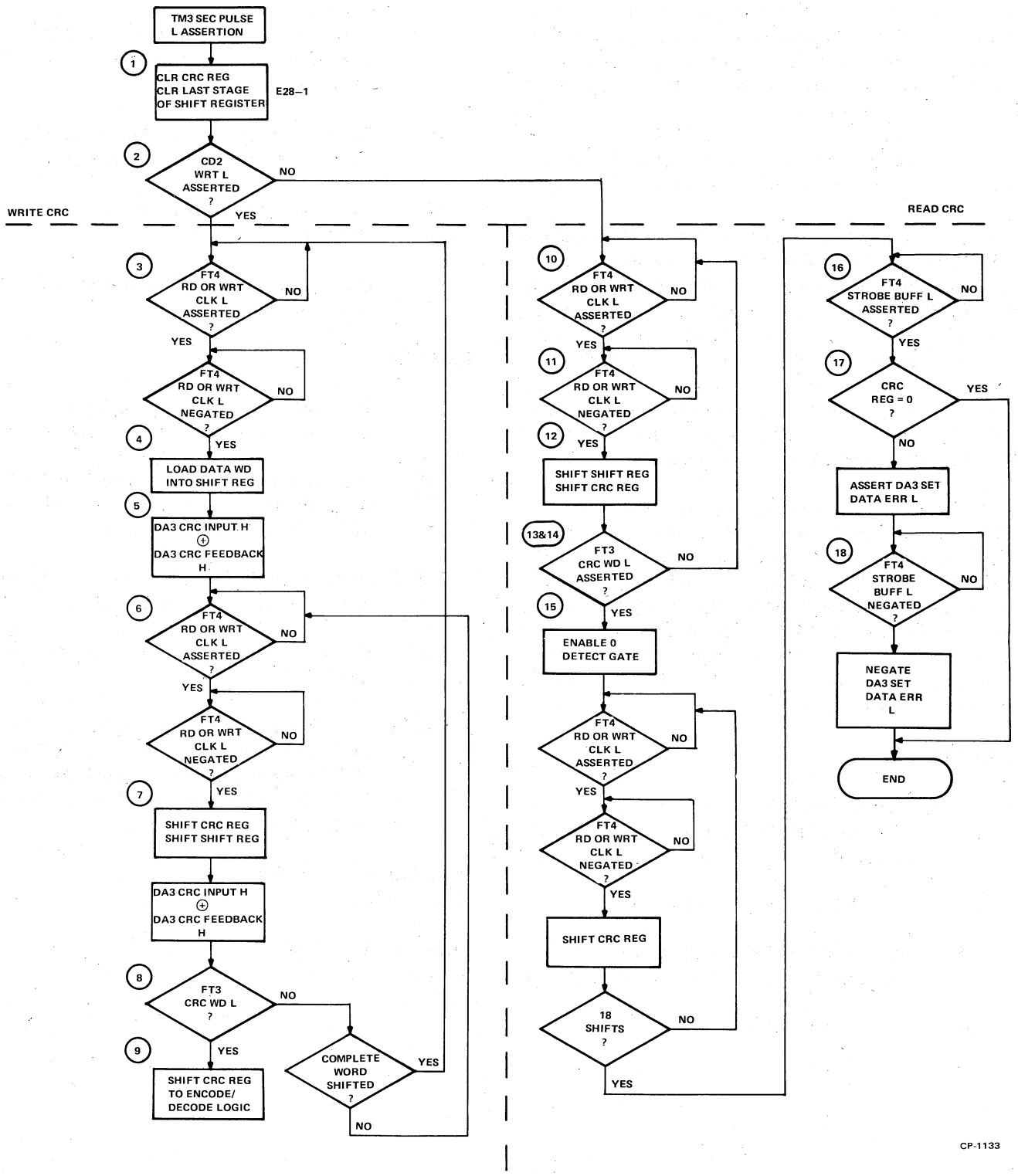

Figure 3-14 CRC Troubleshooting Flow Chart

3.3.5 Encode/Decode Module M7751

Logic Assembly Slot Locations – AB14

Signal Mnemonic Prefix – ED

Logic Elements – **Phase Locked Loop**
Encode Logic
Decode Logic

The numbers of the descriptive text under the paragraph titles correspond to the numbered boxes of the flowchart. Wherever possible, the text sequence represents the logical sequence of events for a particular operation, however, the text sequence does not indicate simultaneous events. This fact is represented by parallel paths on the flowchart.

LOGIC ELEMENT THEORY OF OPERATION

Phase Locked Loop

The phase locked loop is a closed loop circuit which provides an output that is in phase and frequency lock with the input signal, and which occurs at twice the bit rate. A block diagram is shown in Figure 3-15.

When the drive is Ready (i.e., neither reading nor writing) and during a write operation, TM5 CLK PULSE L is applied to the phase locked loop through the input select. This input is delayed through DL2, then compared to the feedback signal by the phase detector (E–13).

The Phase Detector outputs an Up or Down signal, which is equal in duration to the time between the falling edges of the two inputs. An Up signal occurs if the input edge precedes feedback; a Down signal occurs if the feedback edge precedes the input (Figure 3-16).

The charge pump circuit (Q1, R10, 11, 12, 13, 15, D2, D3, D4, C28) then provides signals of almost constant current to the integrator. These signals are of the Up/Down signal's duration – negative current (out of the integrator) for Up signals and positive current for Down signals.

The integrator (R6, R8, R9, C29, C33) integrates these inputs. The amplifier (Q2, Q3, R1, R2) provides level shift, inversion, and dc amplification of the integrator output to give a proper control voltage to the VCO.

The VCO (E–6) provides an output frequency proportional to its control voltage. When the drive is Ready or writing, the VCO output is divided by two and delayed to become the feedback signal.

During a read operation, RW2 RD DATA PULSE L signals from the Read Amplifier (G182) are applied to the phase locked loop through the input select. During the first 62 bits of a sector, which are recorded as an all "zero" preamble, the loop performs exactly as in the Ready or Write mode.

After 62 bits, TM3 SET SYN H is asserted, causing ED2 RD SYNC L to be set. At this time, the divide-by-two circuit is disabled and the "Digital Control" of feedback gate is enabled.

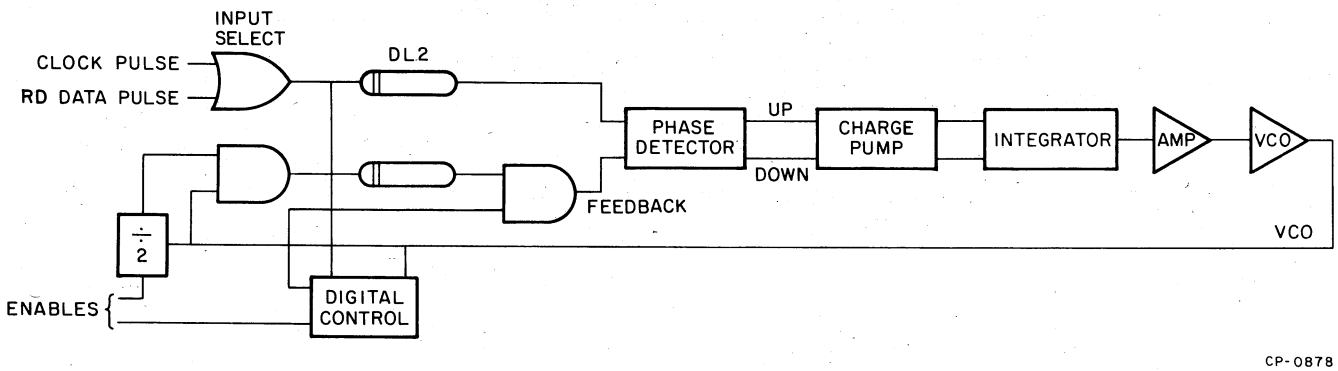

Figure 3-15 Phase Locked Loop Block Diagram

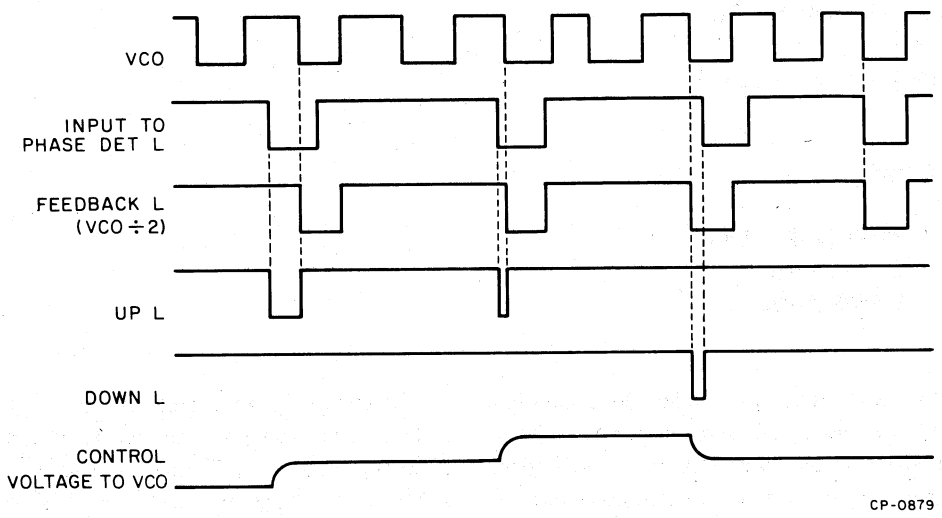

Figure 3-16 Loop Signals (Ready or Write)

Since the location of transition of the RD DATA PULSE signal (i.e., negative edge at bit cell center, boundary, or non-existent) in Miller encoding is determined only by the data sequence recorded, the "Digital Control" circuitry (E17, E3, E10) recognizes an input pulse and allows only those VCO pulses which have corresponding data input pulses to reach the feedback input to the phase comparator (Figure 3-17). In this way, loop lock is maintained on the data.

Encode Logic

The Encode Logic receives serial NRZ data and converts it to Miller encoded serial pulse data during write operations. It also provides the CLK H signal to the logic providing the serial data, to allow it to shift the NRZ data at the proper rate. In addition, the "Zero" preamble is inserted by the Encode Logic when WRT PRE (0) H is low, and the "Sync 1" bit is inserted by the Encode Logic when WRT PRE (0) H is high and PRESENT DATA (1) H is low.

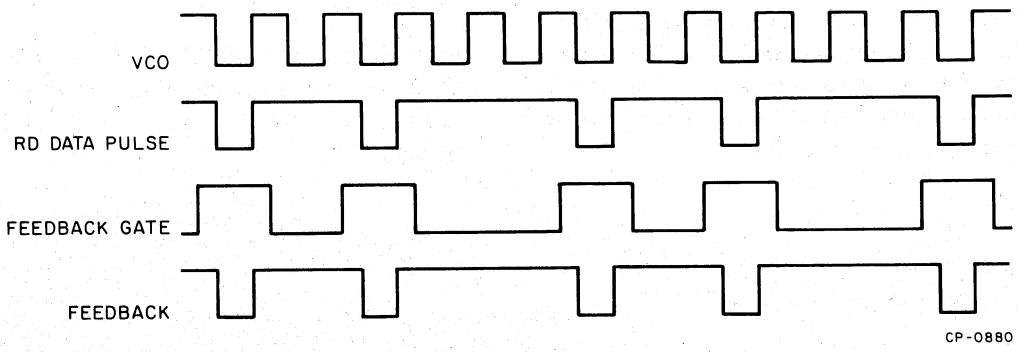

Figure 3-17 Loop Lock on Data Timing Diagram

Each cycle through the flowchart (Figure 3-18) represents one bit cell time and is shown on the timing diagram, Figure 3-19. Detailed operation follows.

1. TM3 SEC PULSE L initializes WRTQ (E15–6), WRTQ+1 (E15–8), and ED2 RD SYNC L (E16–9) at the start of every sector to ensure that the encoder starts in an initialized state.

2. Gate E8–1 ensures that FT5 TRANS DATA L and CD2 WRT L are asserted (i.e., this is a sector to be written).

3. ED2 WRT GATE L is then asserted, turning on the Write Amp (G182).

4. The state of WRT PRE (0) H is then checked by E18–6 (i.e., is this the preamble period or the data field?). If WRT PRE is low, the preamble is being written; otherwise, skip to Step 6.

5. Since the all zeros preamble is being written, the contents of WRTQ is shifted to WRTQ+1 and a "zero" is forced into WRTQ at the rising edge of ED2 Window L. Skip to Step 9.

6. The state of Present Data (1) H is then checked by E18–3. If Present Data is low, the "Sync 1" bit, indicating the end of the preamble, is to be written and Step 7 is next. If Present Data is high, data is to be written and Step 8 is next.

7. Since the "Sync 1" is to be written, the contents of WRTQ is shifted to WRTQ+1 and a "one" is forced into WRTQ at the rising edge of ED2 Window L. Skip to Step 9.

8. Since data is to be written, the contents of WRTQ is shifted into WRTQ+1 and NRZ WRT DATA is shifted into WRTQ at the rising edge of ED2 Window L.

9. The data bit to be written is now stored in WRTQ and the preceding bit written is in WRTQ+1. If the bit to be written is a "one" (WRTQ+1), it is recognized by E18–8 and Step 10 is next; otherwise skip to Step 11.

10. Since the bit to be recorded is a "one", ED2 Window H enables E18–8 during the last half of the bit cell, enabling E2–11 to pass the VCO pulse during the last half of the bit cell as ED2 WRT DATA PULSE L (i.e., a Miller encoded "one").

11. If the bit to be written is a "zero" following a zero (WRTQ=1 and WRTQ+1=0), E19–12 recognizes this and Step 12 is next; otherwise, no pulse is to be passed and Step 13 is next.

12. Since the bit to be recorded is a "zero", ED2 Window L enables E19–12 during the first half of the bit cell, enabling E2–11 to pass the VCO pulse during the first half of the bit cell as ED2 WRT DATA PULSE L.

13. TM3 SET SYN H is strobed by the trailing edge of ED2 Window H.

14. If TM3 SET SYN H is asserted, sufficient preamble has been written and ED2 RD SYNC L flip-flop is cleared; otherwise, it is left set.

15&16. If ED2 RD SYNC L is asserted, E19–6 and E21–6 pass Window L out as ED2 CLK H. Presence of CLK H signifies to the Format Logic that sufficient preamble has been written and that data should be received from the Controller. Once Present Data (1) H is asserted, signifying that data has been written, CLK H is also used to shift the NRZ WRT DATA signal at the proper rate.

Step 2 is next and the cycle is repeated for the next bit. When the end of the sector's data area is reached, FT5 TRANS DATA L will be negated, WRT GATE is negated, and the procedure skips to Step 1 to await the next sector.

Decode Logic

The Decode Logic receives Miller encoded serial pulse data and converts it to serial NRZ data during a read operation. It also provides the CLK H signal to the logic receiving the NRZ data for proper strobing. In addition, by controlling the start of the CLK H signal, the Decode Logic removes the "zeros" preamble and "sync 1" bit from the data.

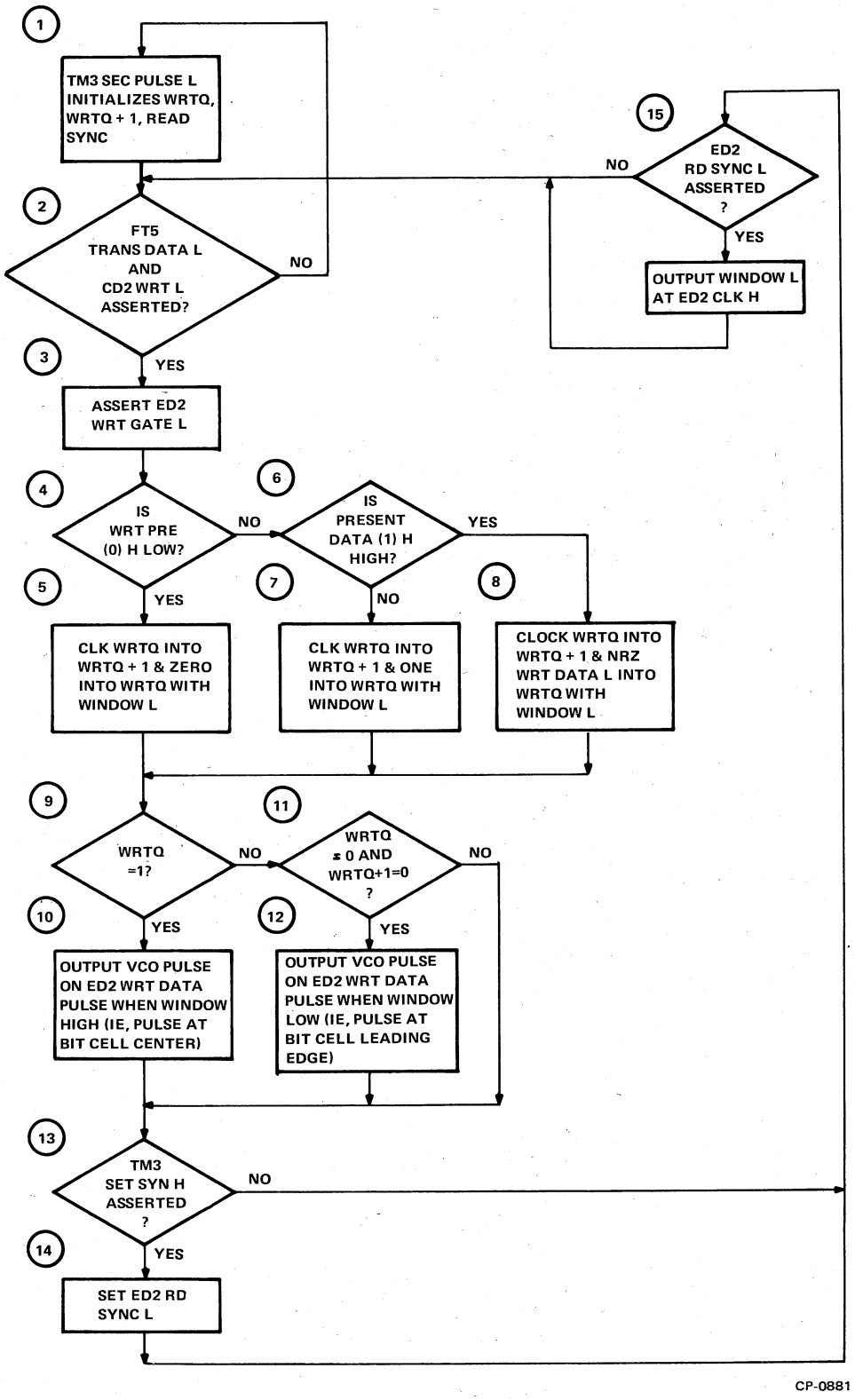

Figure 3-18 Encode Logic Flow Chart

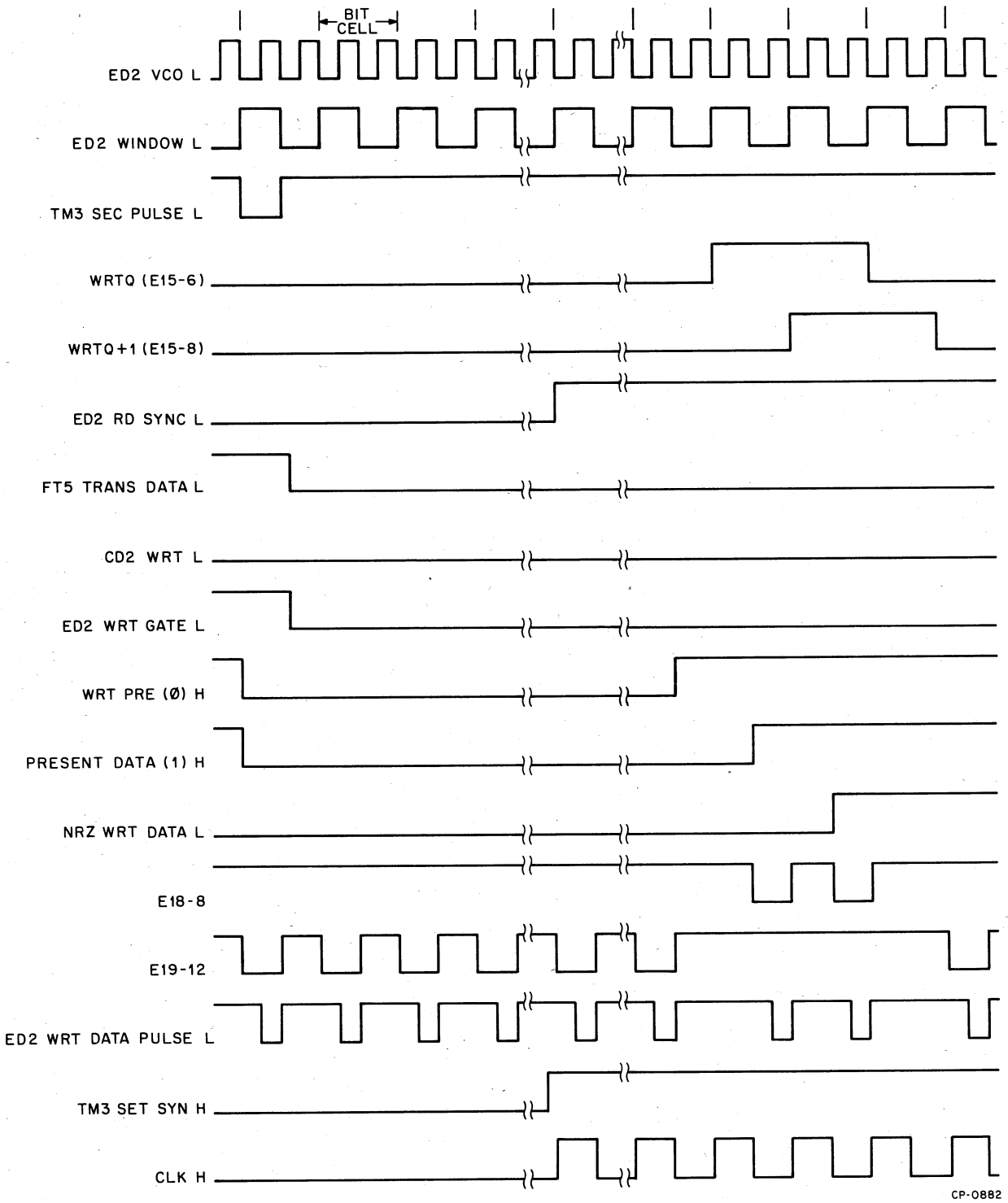

Figure 3-19 Encode Timing

Clocking and data inputs to the Decode Logic actually come from the phase locked loop. During the first 62 bits of a sector, ED2 RD SYNC L prevents operation of the Decode Logic while the loop is establishing synchronization. Once the 62 bits have passed, the loop is assumed to be synchronized and decoding begins. Flowchart (Figure 3-20) and timing diagram (Figure 3-21) serve to outline the operation. Detailed operation follows.

1. TM3 SEC PULSE L initializes ED2 RD SYNC L (E16–9) to ensure that the decoder starts in an initialized state. During the first 62 bits, ED2 RD SYNC L being negated holds all flip-flops in the decoder (E17–9, E16–5, E11–5, E11–9, and E10–9) initialized through gates E2–3, E2–6, E21–11, E1–11, and E4–13, disabling the decoder.

2. FT5 TRANS DATA L must be asserted and CD2 WRT L unasserted to indicate that a read is to take place and that this is the correct sector to read. This is recognized by gates E8–10 and E8–4, allowing gate E1–8 to permit the RW2 RD DATA PULSE L signal to become the phase locked loop input.

3. When 62 bits of the sector have passed, TM3 SET SYN H becomes asserted, to signify that the loop should now be locked on the data pulses.

4. ED2 RD SYNC L (E16–7) is now set by the trailing edge of ED2 WINDOW H.

5. Assertion of ED2 RD SYNC L causes ED2 2 TO 1 H to go high through gates E2–3 and E2–6, releasing the direct clear on the "synchronize flip-flop" (E17–9).

6. The "Synchronize flip-flop" (E17–9) is then set by a signal from the phase locked loop, which ensures that the "read window flip-flop" (E16–5) is in phase with the data, i.e., the "read window" must be opened during the center of the bit cell when Miller encoded "1" pulses occur, and closed at the end and at the beginning of the bit cell when Miller encoded "0" pulses occur.

7. The "read window" (E16–5) is now "opened" (set) by ED2 STROBE DATA 1 L.

8. Flip-flop E11–5 can now be set by the clock input if a pulse exists, i.e., if a "1" is recorded.

9&10. If ED2 SYNC 1 H is set, "read window" (E16–5) is gated out as ED2 CLK H. Skip to Step 13.

11. If ED2 SYNC 1 H is not set and DE2 RD DATA H (E11–9) is set, E11–9 now contains the "Sync 1" bit; otherwise, skip to Step 13.

12. The "read window" (E16–5) is now "closed" (cleared). This transition of "read window" sets ED2 SYNC 1 H and clocks E11–5 into ED2 NRZ RD DATA H (E11–9). Further transitions of "read window" will be gated out as ED2 CLK H, telling the logic receiving the NRZ DATA, when to strobe ED2 NRZ RD DATA H.

13. The "read window" (E16–5) is not "closed" (cleared). This transition of "read window" clocks E11–5 into ED2 NRZ RD DATA H (E11–9).

14. The end of the sector is indicated by the negation of FT5 TRANS DATA L. When this happens, operation ceases until the next sector pulse (Step 1). Until this happens, the cycle for Step 7 is repeated for each bit of data.

Maintenance Mode Operation

When the drive is placed in Maintenance Mode, the CD3 MAINT H signal is asserted.

During a write operation, ED2 WINDOW L is controlled by the direct set and clear inputs of E9–9 and directly follows MCLK H; all other circuitry operates in the normal mode.

During a read operation, the "read window flip-flop" (E16–5) is controlled by MCLK H, by means of the direct set and clear inputs, and ED2 NRZ RD DATA H is controlled by CD3 MRD H, by means of the direct set and clear inputs. Hence, the "Synchronize flip-flop" (E17–9) is not used, but all other logic operates normally.

PERFORMANCE CHECKS

See Table 3-1.

TROUBLESHOOTING

See Table 3-1.

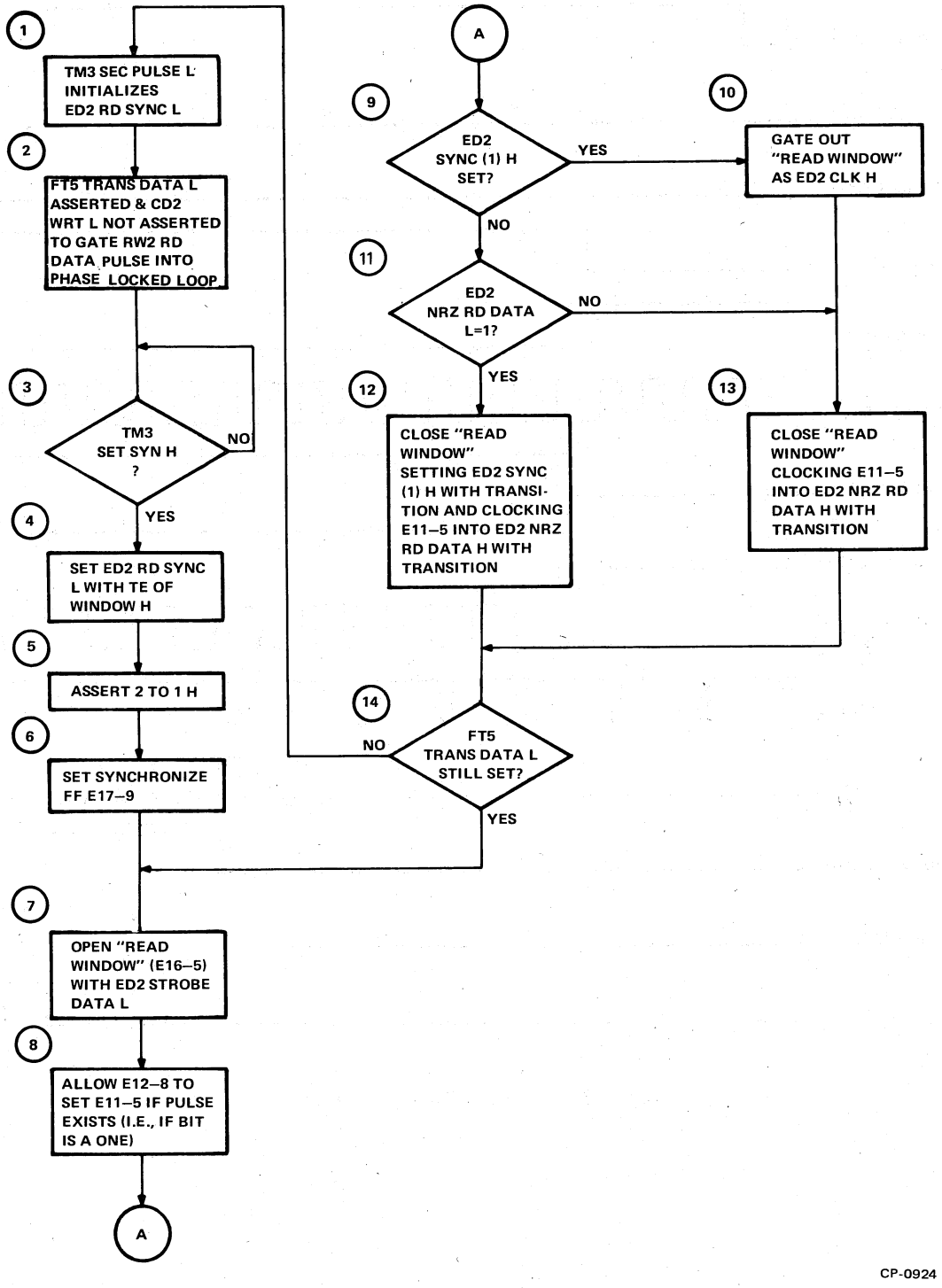

Figure 3-20 Decode Logic Flow Chart

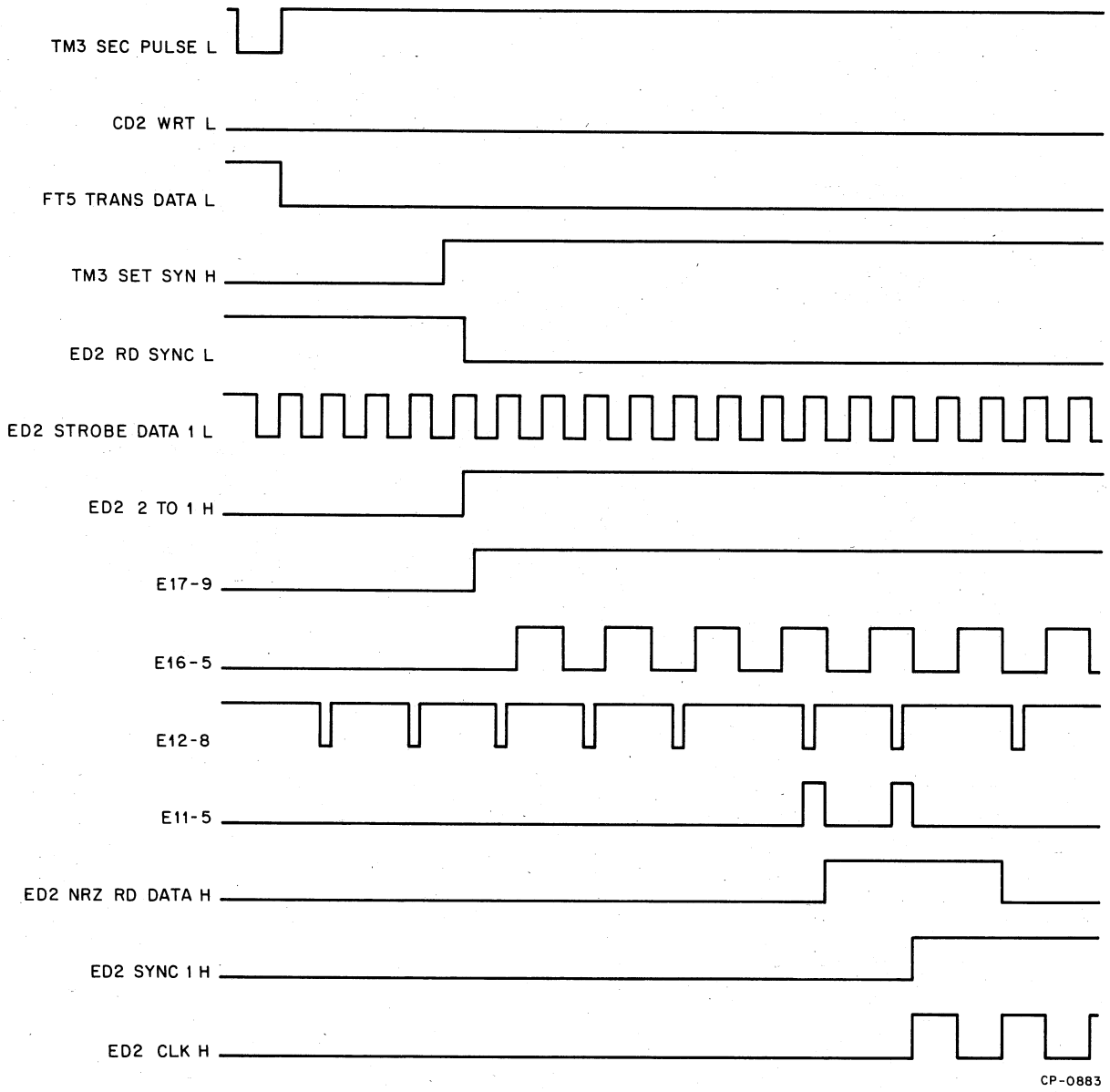

Figure 3-21 Decode Timing Diagram

3.3.6 Format Module M7771

Logic Assembly Slot Location – AB11

Signal Mnemonic Prefix – FT

Logic Elements –

Format Control Section:
- **Modulo-9 Sync Counter & Sync Clk Wrt Flip-Flop**
- **Modulo-9 Bit Counter & Sync Clk Rd Flip-Flop**
- **Words/Sector Counter**
- **Shift Register**
- **Preamble Extension Enable Flip-Flop and Preamble Extension Counter**

Initiation/ Termination Section (Data Bus Control):
- **Sector Start Flip-Flop**
- **Do It Flip-Flop**
- **EBL One-Shot**
- **Exception Latch**

The numbers of the descriptive text under the paragraph titles correspond to the numbered boxes of the flowchart. Wherever possible, the text sequence represents the logical sequence of events for a particular operation, however, the text sequence does not indicate simultaneous events. This fact is represented by parallel paths on the flowchart.

LOGIC ELEMENT THEORY OF OPERATION

General

During a data transfer operation (write, read, or write check), the Format module supplies various control and synchronizing signals to the drive logic and to the Controller. The following paragraphs describe the Format module operation.

The operation of the two modulo-9 counters is identical; this is important to understand. The first counter consists of binary counter E5 and comparator E6, the second consists of counter E17 and comparator E18. The comparator detects whenever the binary counter equals zero. The zero condition is indicated when the comparator's A < B output (pin 7) is low, which enables the binary counter's synchronous load input. The next clock pulse to the counter parallel-loads it to binary state 1000. Since the binary counter is no longer zero, the comparator's A < B output goes high, enabling the binary counter to count up on successive clock pulses. The binary counter counts up to 1111, ripples over to 0000, and on the next clock pulse is preset to 1000. The states of the counter are shown as follows:

State No.	Binary Counter State	A < B Output
1	0000	L
2	1000	H
3	1001	H
4	1010	H
5	1011	H
6	1100	H
7	1101	H
8	1110	H
9	1111	H
1	0000	L
2	1000	H

NOTE

The Sync Counter is enabled only during write functions and is used to generate SCLK during writes. The Bit Counter is enabled during *all* data transfers and counts bits as they come out of or go into the Shift register. The Bit Counter generates SCLK during read and write check functions.

The signal BW TRK PAR L is a backplane wire which is not used in the RS03 allowing the signal to go high. This signal defines the length of the sector as 64_{10} words by allowing FT3 DATA FIELD DONE L to be asserted only after the Words/Sector Counter reaches $0100\ 0000_2$ or 64_{10}.

Refer to the system timing diagrams in Appendix A and the following flow charts to understand the timing relationships described in this subsection.

Since each data transfer is initiated at the beginning of a sector, the description that follows assumes that the signal TM3 SEC PULSE L has already initialized all Format Logic elements.

Data Write (Figure 3-22)

1–3. FT4 WRT H enables Sync Counter E17-6/10; CD2 TRANS L enables S CLK Generation Logic. TRA2 RUN H and recognition of a data transfer command (CD2 TRANS L assertion) sets Do It flip-flop (E28–1) to initiate an Address Search. This enables Sector Start flip-flop (E13-1,2) to guarantee that FT5 ADDRS CONF L becomes asserted only at the beginning of the desired sector. (Note that it is possible for TRA2 RUN H to be asserted *during* the desired sector. If this occurs, an entire disk revolution must occur before beginning the data transfer, because a data transfer may be initiated only from the beginning of the desired sector.) FT5 ADDRS CONF L assertion indicates that the read/write head is located over the desired sector and the write sequence begins by writing the preamble.

4&5. After 62 preamble zeros have been recorded on the disk, FT4 CLK L pulses begin and increment Sync Counter (E17–2).

6–8. The first negation of FT4 CLK L sets Sync CLK WRT flip-flop (E2–3) to assert FT4 SYNC CLK L. This signal is transmitted to the Controller to indicate that the drive is ready to receive a data word.

9&10. TRA2 WRT CLK H enables the D input of the PREAMBLE EXTENSION ENABLE flip-flop E13–12. In addition, TRA2 WRT CLK H ANDs at gate E16–9 to generate FT4 STROBE BUFF L.

11. FT4 STROBE BUFF L loads the data word from the Controller into the Data Buffer.

12&13. After the first assertion of TRA2 WRT CLK H, ED2 VCO L clocks the PREAMBLE EXTENSION ENABLE flip-flop set. This allows Preamble Extension (decade) Counter E29-6/7 to increment (it was held preset to state 1001 before it was enabled). (Zeros are still being written in the preamble.)

14&15. When the Preamble Extension Counter reaches count 0110, the D input of WRT PRE flip-flop E7–2 is disabled; this allows the next CLK H to reset this flip-flop.

16. With the WRT PRE flip-flop reset, FT4 FORMAT CLK L is produced, which in turn produces FT4 RD OR WRT CLK L. The first assertion of FT4 RD OR WRT CLK L causes a logical one (Sync 1) to be written on both surfaces, indicating the end of the preamble for that sector.

17–19. FT4 FORMAT CLK L ANDs at gate E15–1 to produce FT4 WD COUNT CLK L.

20&21. The first negation of FT4 RD OR WRT CLK L parallel-transfers the data word from the Data Buffer into the Shift register and also negates FT4 LOAD SR L.

22–30. Successive positive edges of FT4 CLK L increment the Bit Counter such that every ninth count complements the SYNC CLK RD flip-flop. Every 18th count of the Bit Counter asserts the signal FT3 LAST BIT H. This ANDs with FT4 FORMAT CLK H at E15-1,2 to produce FT4 WD COUNT CLK L, which increments the Words/Sector Counter immediately before writing each data word.

31–33. When the Words/Sector Counter reaches binary state 0100 0000, 64_{10} words have been written and FT3 DATA FIELD DONE L is asserted, disabling Sync Counter E17–7, to prevent further assertions of SCLK.

34&35. Next, FT4 WD COUNT CLK L clocks a zero into Shift register E23 to assert FT3 CRC WD L. This signal allows successive FT4 RD OR WRT CLK L signals to now shift the CRC word out of the CRC register.

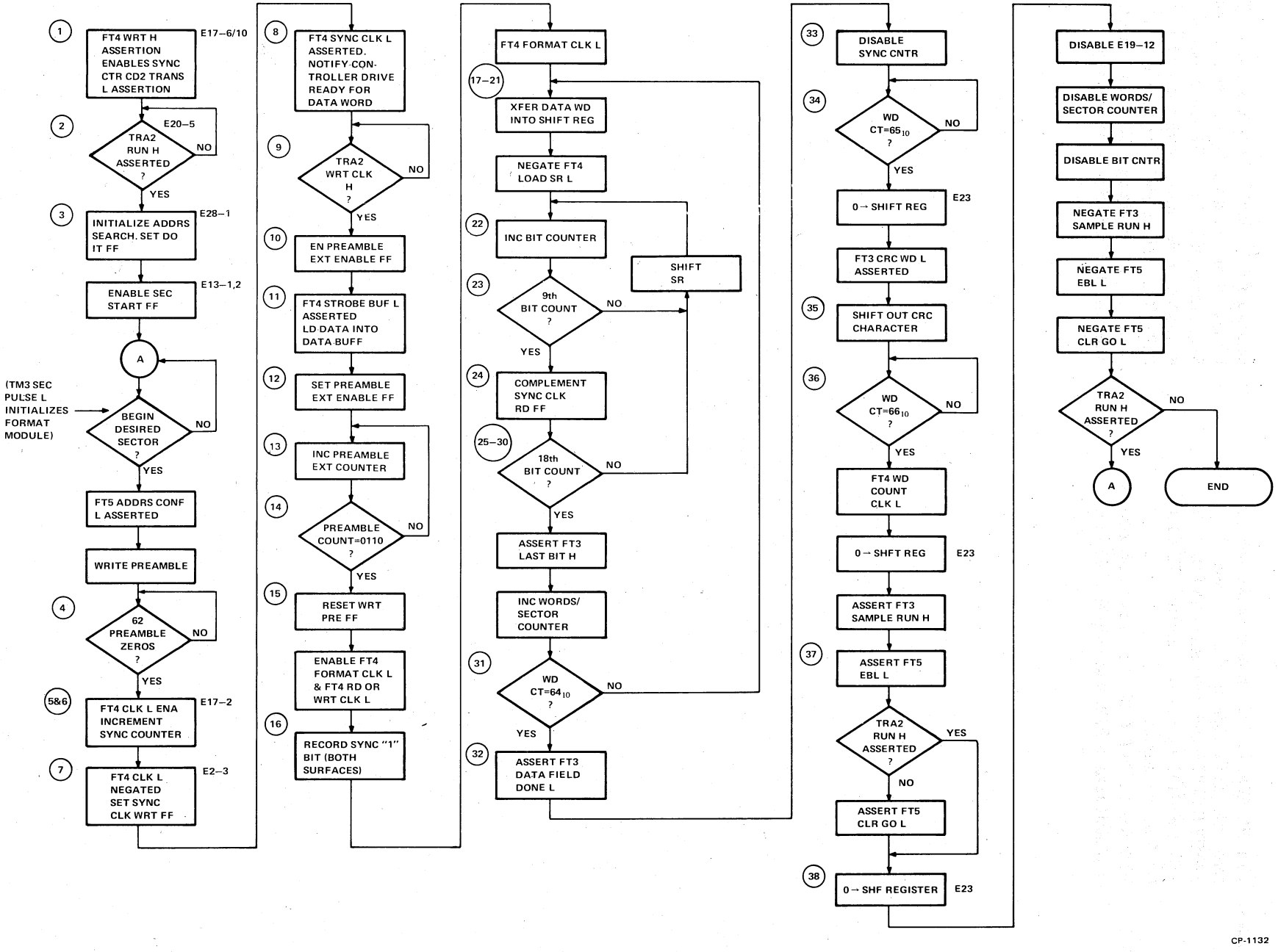

Figure 3-22 Format Logic Data Write Troubleshooting Flow Chart

36&37. FT4 WD COUNT CLK L now clocks another zero into Shift register E23 to assert FT3 SAMPLE RUN H and thus assert FT5 EBL L. If TRA2 RUN H is no longer asserted, FT5 CLR GO L is now asserted.

38. FT4 WD COUNT CLK L clocks a third zero into Shift register E20, which disables E19–12, negating FT3 SAMPLE RUN H and thus FT5 EBL L; it also disables the Words/Sector and Bit Counters. If FT5 CLR GO L was asserted, it is negated at this time, clearing GO. If TRA2 RUN H is still asserted, the flow returns to point A to continue the data transfer; otherwise, the transfer is now terminated.

Data Read (Figure 3-23)

1. CD2 WRT L negation:

   - enables D input of START SCLK RD flip-flop (E4–12)
   - disables Sync Counter (E17-6/10)
   - disables Preamble Extension Counter (E29-2/3)
   - enables gate (E30–4)

2&3. TRA2 RUN H AND CD2 TRANS L set Do It flip-flop (E28–1) to initiate an Address Search. This enables Sector Start flip-flop (E13-1,2), which guarantees that FT5 ADDRS CONF L becomes asserted only at the beginning of the desired sector. (It is possible for TRA2 RUN H to become asserted *during* the desired sector. If this does happen, an entire disk revolution must occur before beginning the data transfer, because a data transfer may be initiated only from the beginning of the desired sector.)

3a. FT5 ADDRS CONF L assertion indicates that the read/write head is located over the desired sector. This asserts FT5 TRANS DATA L, which switches the input of the phase locked loop from the timing track to the data.

4–6. After the end of the preamble and the first data bit has been decoded, ED2 CLK H is enabled and applied through gate E30–1, to produce FT4 FORMAT CLK L. This signal:

   - increments Bit Counter (E5–2)
   - ANDs at gate E15–1 to produce FT4 WD COUNT CLK L after every 18-bit data word has been shifted into the Shift register.
   - ANDs at gate E16–1 to produce FT4 RD OR WRT CLK L.

7. FT4 RD OR WRT CLK L shifts serial data bits from the decoding logic into the Shift register.

8&9. The first negation of FT4 FORMAT CLK L sets SYNC CLK RD flip-flop (E4–3).

10–12. The ninth bit count resets SYNC CLK RD flip-flop, clocking START SCLK RD flip-flop (E4–11) set.

13&14. FT4 FORMAT CLK H enables gate E9–13 to produce FT4 STROBE BUFF L after every 18 bit counts. This signal parallel-transfers a data word from the Shift register into the Data Buffer. At the same time, the Words/Sector counter is incremented.

15–17. The next bit count (second word) again sets SYNC CLK RD flip-flop, thus asserting FT4 SYNC CLK L. This signal is transmitted to the Controller to indicate that a data word is present and is stable on the Data Bus. This process is repeated until 64_{10} words have been transferred.

18&19. When the Words/Sector counter reaches binary state 0100 0000, 64_{10} data words have been read and FT3 DATA FIELD DONE L is asserted.

20. Next, FT4 WD COUNT CLK L clocks a zero into Shift register E23 to assert FT3 CRC WD L. FT3 LAST BIT H assertion now clocks DSBL SCLK RD flip-flop set to prevent further FT4 SYNC CLK L assertions. The 65th FT4 STROBE BUFF L enables CRC Check gate (E6–5) thus checking for an all-zero CRC register.

21&22. Next, FT4 WD COUNT CLK L clocks another zero into Shift register E23 to assert FT3 SAMPLE RUN H and thus assert FT5 EBL L. If TRA2 RUN H is no longer asserted, FT5 CLR GO L is now asserted.

23. FT4 WD COUNT CLK L clocks a third zero into Shift register E23, which disables E19–2, negating FT3 SAMPLE RUN H and thus FT5 EBL L; it also disables the Words/Sector and Bit Counters. If FT5 CLR GO L was asserted, it is negated at this time, clearing GO. If TRA2 RUN H is still asserted, the flow returns to point A to continue the data transfer; otherwise, the transfer is now terminated.

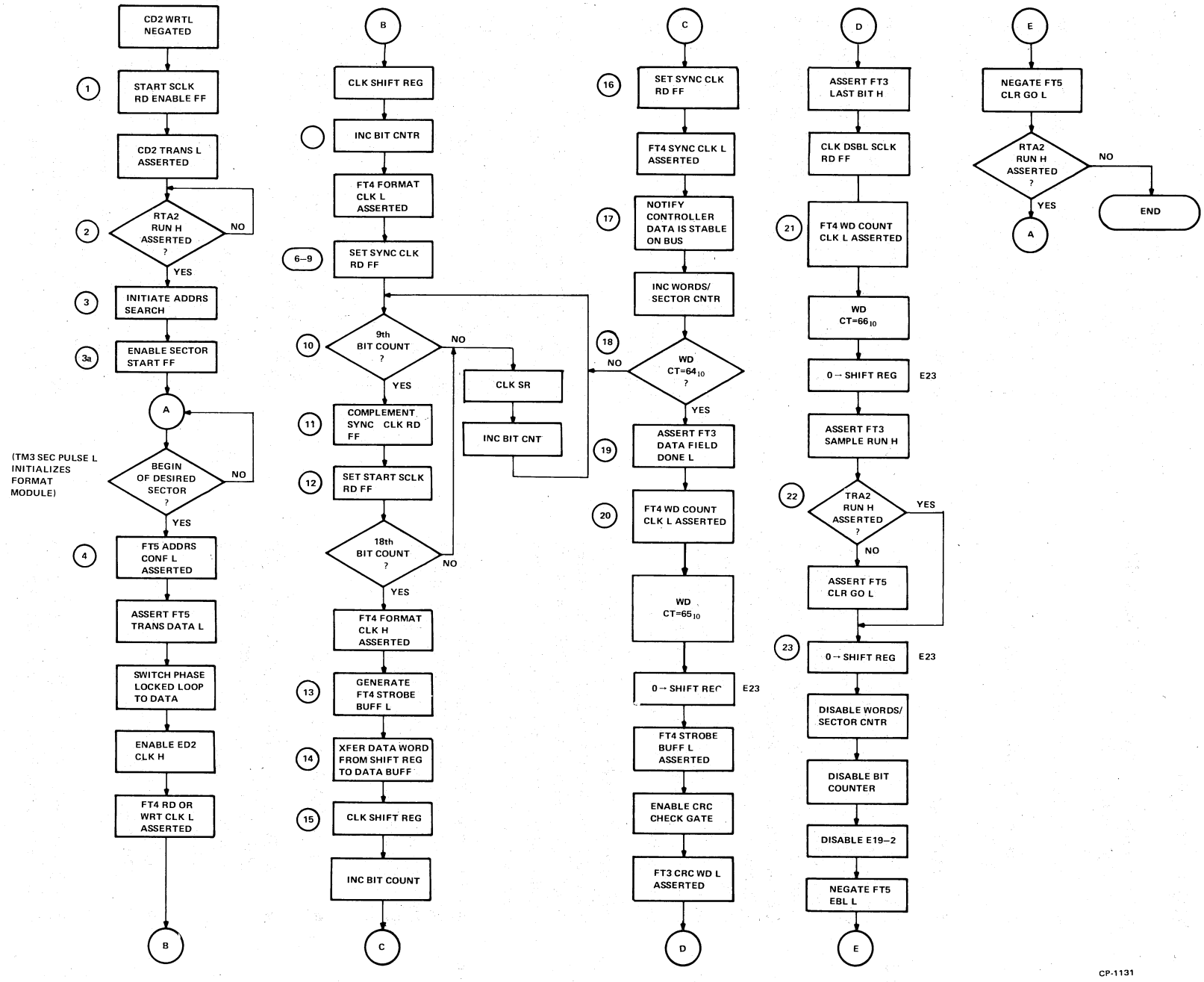

Figure 3-23 Format Logic Data Read Troubleshooting Flow Chart

Search Function (Initiation/Termination) (Figure 3-24)

1. CD2 SEARCH L, applied through E27–4, enables D input of SECTOR START flip-flop (E13–2).

2&3. The next FT3 SEC PULSE L clocks E13 set.

4–6. Address logic searches for desired sector; when located, AD2 SEC COMP H is asserted.

7–9. AD2 SEC COMP H ANDs at E14–5 to generate FT5 ADDRS CONF L. This signal sets the ATA flip-flop on the Status module. Assertion of ST4 ATA H produces assertion of FT5 ATTN L.

10. FT5 ATTN L assertion clears GO flip-flop to terminate Search function.

NOTE

If the desired sector is not located prior to the third TM5 INDEX L assertion after CD2 GO (1) H assertion, OPI flip-flop (E8–4) on Status module sets to generate an OPI (Operation Incomplete) error.

Data Transfer (Initiation/Termination) (Figure 3-25)

1. CD2 TRANS L clocks flip-flop E24–11 reset.

2&3. TRA2 RUN H sets Do It flip-flop (E28–1). (If TRA2 RUN H is not asserted within two complete disk revolutions after GO is set, OPI results.)

4–6. Address logic searches for desired sector; when located, generates AD2 SEC COMP H. (If third TM5 INDEX L occurs before an FT5 EBL L pulse occurs, set OPI flip-flop in Status module).

7&8. FT5 ADDRS CONF L ANDs at E21–9 to generate FT5 TRANS DATA L. For a read operation, FT5 TRANS DATA L enables the Data Bus output gates. For a write or a read operation, FT5 TRANS DATA L enables the encode/decode logic.

9–11. At word count 66, the leading edge from gate E19–1 produces FT5 EBL L. (If a third TM5 INDEX L occurs prior to FT5 EBL L, set OPI flip-flop (E8–4) in status logic).

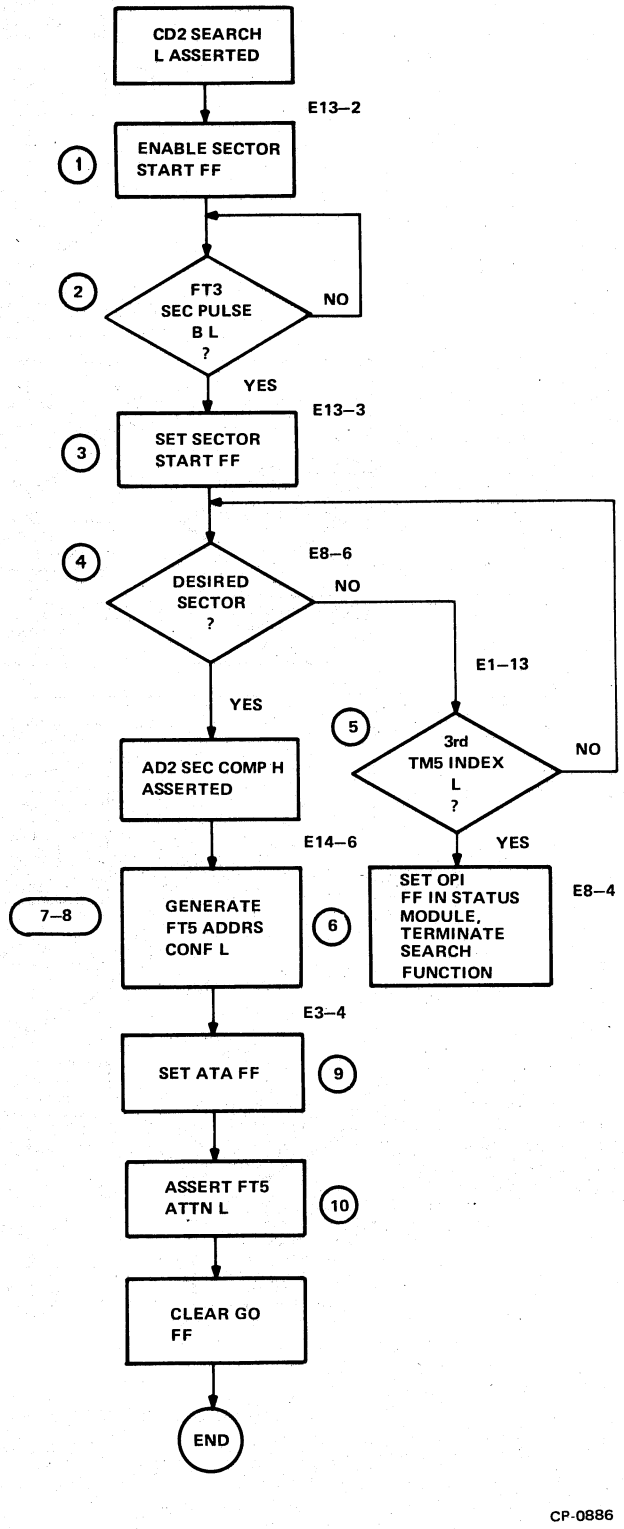

Figure 3-24 Search (Initiation/Termination) Troubleshooting Flow Chart

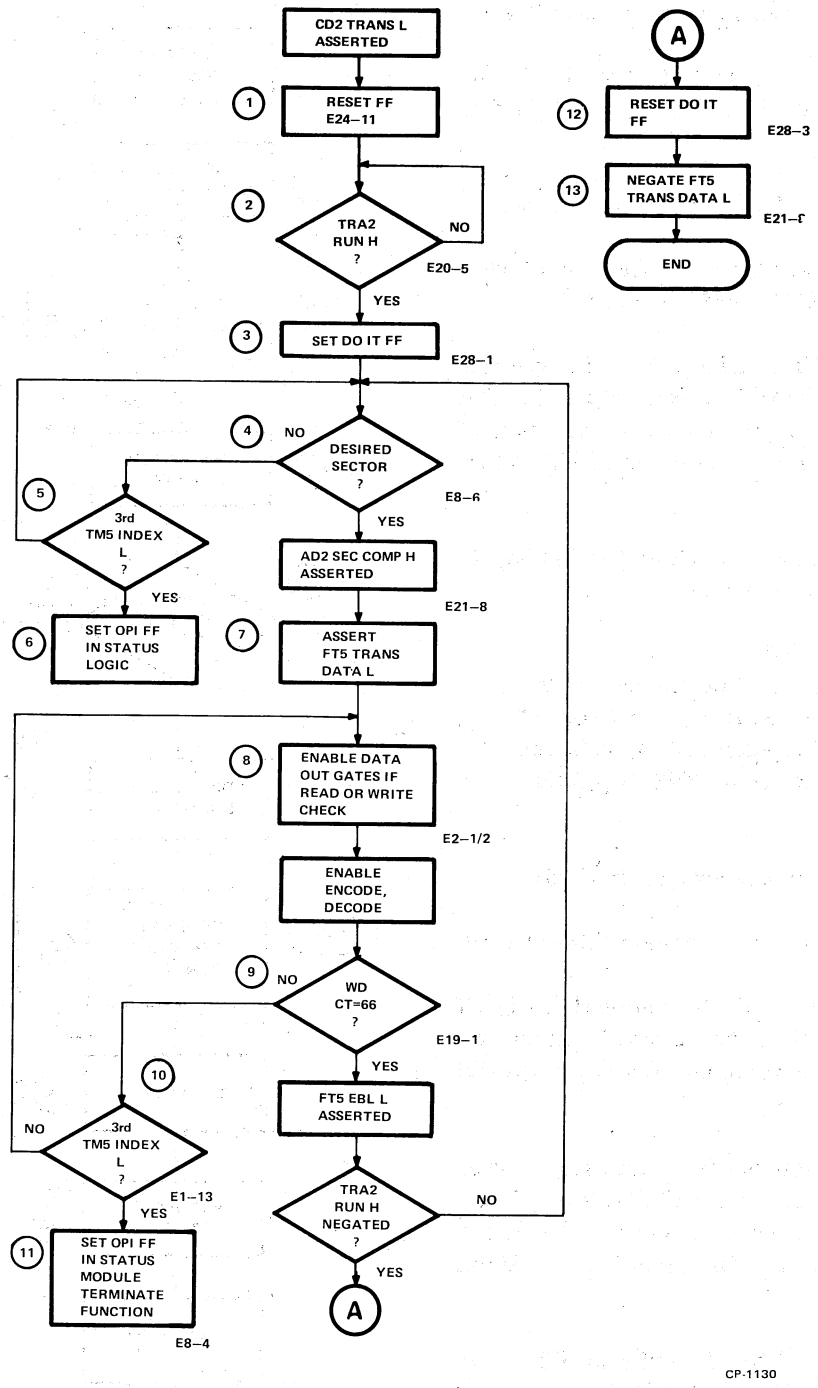

Figure 3-25 Data Transfer (Initiation/Termination) Troubleshooting Flow Chart

12&13. The trailing edge from E19–1 clocks Do It flip-flop (E28–3) reset if TRA2 RUN H has been negated by the Controller. This action removes FT5 TRANS DATA L, terminating the data transfer. Negation of FT5 EBL L also increments the Desired Address register.

14. If TRA2 RUN H is not negated by the trailing edge of E19–1, return to Step 4.

NOTE

If a drive error occurs during a data transfer, the transfer operation is terminated as described in Paragraph 3.3.7.

The Controller may assert TRB2 EXT EXCEPTION to terminate an in-progress data transfer. This is detected by gate E26–12, which produces a termination sequence identical to that following detection of a Class B error.

The operation of the ERR EBL flip-flop (E24) and of the SET AOE flip-flop (E28) is of special significance and is discussed here separately.

Whenever EBL is asserted prior to the end of a sector (due to the occurrence of a Class B error during a data transfer, or to the assertion of EXC by the Controller during a data transfer), it is generated by the ERROR EBL 1-Shot (E25). When this 1-Shot is triggered, it direct-sets ERR EBL flip-flop (E24–10). When this flip-flop is set, it disables E26–11, allowing the Do It flip-flop (E23) to be reset by the trailing edge of EBL, and asserting FT5 CLR GO L. Therefore, even if the Controller leaves RUN asserted, the drive terminates the data transfer in these two cases.

The SET AOE flip-flop detects the occurrence of a drive address overflow condition. AD3 LAST BLK H is asserted on the leading edge of FT3 SAMPLE RUN H, after address 7777_8 has been transferred. Generally, the Do It flip-flop would be reset by the trailing edge of the same FT3 SAMPLE RUN H. If for any reason the Do It flip-flop is not reset at this time, the D input of the SET AOE flip-flop is enabled. The next FT3 SEC PULSE H assertion (corresponding to sector 00 on the next disk revolution) sets the SET AOE flip-flop, producing an Address Overflow Error (AOE). *However,* if the Controller asserts EXC before the leading edge of FT3 SEC PULSE H, the Do It flip-flop is cleared, which terminates the address overflow condition and prevents the SET AOE flip-flop from being set.

If the assertion of TRA2 RUN H is not received by the RS03 after a data transfer command has been loaded into the Control register, an Operation Incomplete (OPI) Error will occur (Paragraph 3.3.7). If this happens, the drive must simulate the assertion of TRA2 RUN H to terminate its use of the Data Bus and return to the Ready state. To do this, ST3 OPI (1) H is ORed with TRA2 RUN H at E8-8,9. The assertion of ST3 OPI (1) H will set the Do It flip-flop, which in turn will trigger the ERROR EBL 1-Shot; this produces the error EBL sequence described above.

PERFORMANCE CHECKS

See Table 3-1.

TROUBLESHOOTING

See Table 3-1.

3.3.7 Status Module M7770

Logic Assembly Slot Location – AB08

Signal Mnemonic Prefix – ST

Logic Elements – **Error Flip-Flops and Associated LEDs**
Error Summary Circuit
Attention Active Circuit
Optional Parity Error Jumper
Error Register Multiplexer
Status Register Multiplexer
Drive Type Register Multiplexer

The numbers of the descriptive text under the paragraph titles correspond to the numbered boxes of the flowchart. Wherever possible, the text sequence represents the logical sequence of events for a particular operation, however, the text sequence does not indicate simultaneous events. This fact is represented by parallel paths on the flowchart.

LOGIC ELEMENT THEORY OF OPERATION

Error Flip-Flops and Associated LEDs (Figure 3-26)
There are 11 detectable error conditions in the RS03. When any of these errors occur, an error signal is asserted (e.g., CN2 SET RMR ERR L) which accomplishes the following:

1–3. Sets the associated error flip-flop in the Error register and lights a corresponding LED.

4. Two OR gates are used to define each error as either Class A or Class B.

Of the 11 error flip-flops, 6 are direct-set by signals generated on other modules: ILF, ILR, RMR, AOE, UNS, and DCK. Explanations for these errors are contained in the descriptions of those modules. For the remaining five error conditions, gating is contained on this module to detect these errors.

The MASSBUS Parity Error (PAR) is generated by incorrect parity on either the Control Bus or the Data Bus. A Control Bus parity error is detected by the assertion of AD2 ASYNC PAR ERR L and CN2 CHK BUS PARITY L. This is ORed with the signal DA2 SYNC PAR ERR H from the Data Bus parity logic to direct-set the PAR flip-flop.

The IAE flip-flop is direct-set whenever flip-flop E8–8 is clocked set. The D input of this flip-flop (E8–12) is the signal AD2 INV ADDR H, which is asserted when any of bits 12–15 of the Desired Address register is a one. The flip-flop is clocked by the assertion of CD2 GO (1) H.

The WLE flip-flop is direct-set whenever the address in the Desired Address register is write-protected (AD3 PROTECTED L asserted) and a write function is loaded into the Control register (CD2 WRT L asserted).

The DTE flip-flop is direct-set whenever a timing error is encountered (TM5 SET TIMING ERR L asserted) and the GO bit is set (CD2 GO (1) H asserted).

The OPI flip-flop is direct-set whenever the function contained in the Control register is not executed within two complete disk revolutions. Index pulses are counted to define disk revolutions; the first Index pulse after assertion of CD2 GO (1) H marks the beginning of the first disk revolution, the second Index pulse marks the beginning of the second revolution, and the third Index pulse marks the *completion* of the second revolution.

The negation of CD2 GO (1) H at E9–2 holds FIRST INDEX and 2ND INDEX flip-flops (E23–13) and (E3–13) clear. When the GO bit is set, both flip-flops E23 and E3 are enabled, along with NAND gate E2–10. The first trailing edge of Index after GO is set, sets the FIRST INDEX flip-flop; on the next revolution, the trailing edge of Index sets the 2ND INDEX flip-flop; if the 2ND INDEX flip-flop is still set by the leading edge of the next Index,

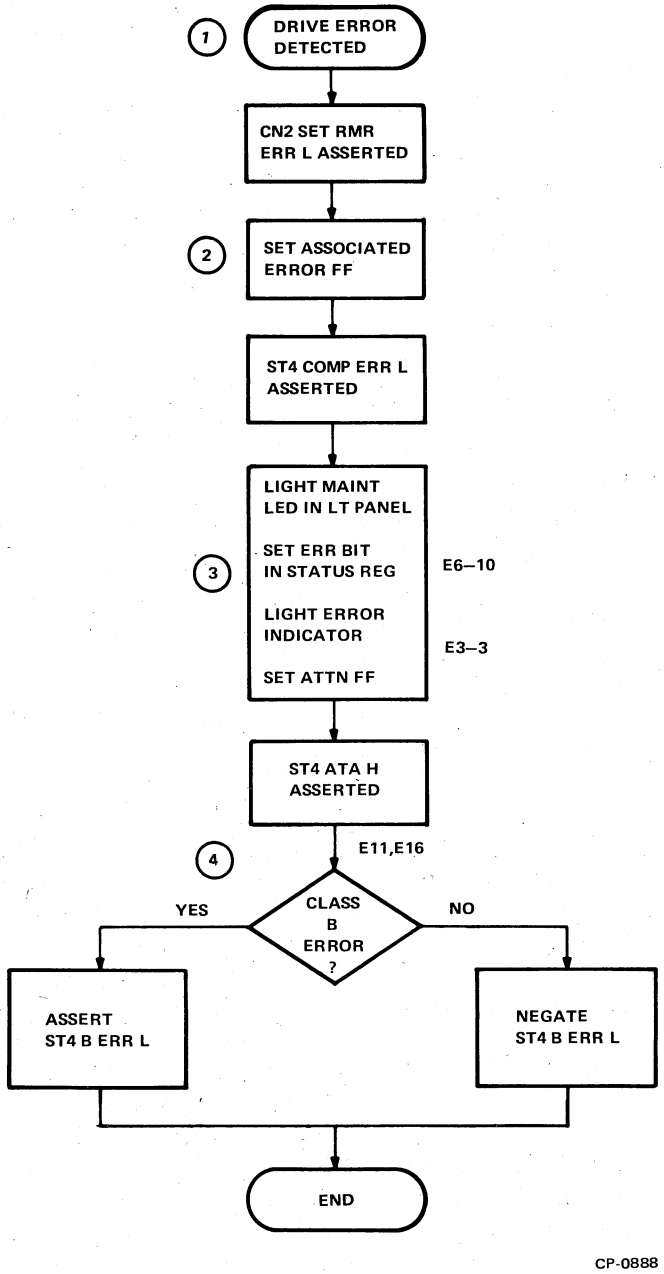

Figure 3-26 Error Troubleshooting Flow Chart

NAND gate (E2–11) direct-sets the OPI flip-flop. The OPI flip-flop will not be set if the FIRST INDEX and 2ND INDEX flip-flops are cleared before the third Index pulse occurs. During the execution of either a Search of a data transfer function, either ST4 SEARCH COMP H or FT5 EBL L, respectively, is asserted. The assertion of either of these signals clears both FIRST and 2ND INDEX flip-flops, preventing the OPI flip-flop from being set.

NOTE

OPI is a difficult error to troubleshoot because it can be caused by any number of malfunctions. Some possible causes (by no means the only causes) are: if OPI occurs during both Search and data transfer functions, addressing logic may be at fault (M7754, G092); if OPI occurs only during data transfer functions, the fault may be in the Data Bus Initiation/Termination Logic (M7771) or, TRA2 RUN H assertion may not be received from the Controller.

If the drive is not performing a data transfer or Search function (CD2 GO (1) H negated), the Controller can also set the error flip-flops. This is done by performing a register write operation with the appropriate bits (TR2 WO DCB (00:15) H) asserted on the Control Bus.

Error Summary Circuit

Consists of a Class A gate (E16), a Class B gate (E11), and the necessary gating components.

Class B Error – If a Class B error occurs, ST4 B ERR L, ST4 ATA H, and ST4 COMP ERR L are asserted.

Class A Error – If a Class A error occurs, ST4 ATA H and ST4 COMP ERR L are asserted.

Attention Active Circuit

Consists of the Attention flip-flop (E3) plus the necessary components. The Attention flip-flop is set at the following times:

- at Search completion by ST4 SEARCH COMP H
- upon detection of any error by ST4 COMP ERR H
- during initial power-up sequencing by CN2 PWR UP ATTN L
- by attempting to set GO with ST4 COMP ERR L asserted.

NOTE

These latter two conditions are ORed together as CD2 SET ATA H.

PERFORMANCE CHECKS

See Table 3-1.

TROUBLESHOOTING

See Table 3-1.

3.3.8 Timing Amp Module G092

Logic Assembly Slot Location – AB16

Signal Mnemonic Prefix – TM

Logic Elements – **Timing Amplifier**
Timing Error Detection Logic
Sector Boundary Counter
Sector Counter
Look-Ahead Register

The numbers of the descriptive text under the paragraph titles correspond to the numbered boxes of the flowchart. Wherever possible, the text sequence represents the logical sequence of events for a particular operation, however, the text sequence does not indicate simultaneous events. This fact is represented by parallel paths on the flowchart.

LOGIC ELEMENT THEORY OF OPERATION

Timing Amplifier Circuit

The timing amplifier circuit detects flux reversals from a prerecorded timing track to generate clock, sector, and index pulses. The timing track is prerecorded at the factory and consists of 86,014 clock reversals at a nominal frequency of 2.4 MHz, separated by a 250 ± 50 μs index gap. The flux reversals in the index gap are recorded at half the clock frequency (1.2 MHz).

As long as the recording disk is rotating, flux reversals from the timing track are continuously detected, regardless of the drive operational mode. These flux reversals are applied across pins 3 and 4 of the differential timing amplifier, across protection diodes D1–D4, to amplifier E5 (Figure 3-27). The amplified output is then transmitted through a differential low-pass filter network to zero crossover detectors E20. Detector E20–1 detects positive-going zero crossings, producing a corresponding square-wave output. Positive transitions of this square-wave signal trigger 40-ns one-shot (E25–1). Similarly, detector E20–8 detects negative-going zero crossings to trigger 40-ns one-shot (E19–5). The two one-shot outputs (which are 180° out of phase with each other) are combined at E14-4,5 to produce the signal TM5 CLK PULSE L.

During the main portion of the timing track, the period of the signal TM5 CLK PULSE L is nominally 208 ns. During Index, the period of this signal is increased to nominally 416 ns. The GAP DETECT and INDEX ASSERT retriggerable one-shots detect when the period of TM5 CLK PULSE L is greater than 300 ns. This is accomplished in the following manner:

The negative edge of TM5 CLK PULSE L triggers retriggerable GAP DETECT one-shot (E24–5). During the Index gap, E24–5 times out between successive negative edges of TM5 CLK PULSE L, triggering retriggerable INDEX ASSERT one-shot (E24–13). The INDEX ASSERT one-shot is continuously retriggered prior to its time-out during the gap. This action produces the assertion of TM5 INDEX L. When the period of TM5 CLK PULSE L is reduced to 208 ns (higher frequency) GAP DETECT one-shot is retriggered and does not time out, thus allowing INDEX ASSERT one-shot to time out and negate TM5 INDEX L.

Timing Error Detection Logic

The timing error detection logic monitors the clock and index pulse intervals from the timing amplifier circuit. If the clock or index signals from the amplifier circuit fail intermittently or are lost entirely, a timing error is generated in the following manner:

TM5 CLK PULSE L Error (Figure 3-28) – During normal clock generation, positive edges from zero crossover detectors E20–1 and E20–8 fire corresponding 40-ns one-shots. The positive edge of TM5 CLK PULSE L clocks CLOCK PULSE FAULT flip-flop E4 at the TM5 CLK PULSE L rate. If, for example, one of the zero crossover outputs is missing, the CLOCK PULSE FAULT flip-flop is not complemented, hence, the respective 40-ns pulse enables the Timing Error gate to produce the signal TM5 SET TIMING ERR L. This signal sets DTE whenever CD2 GO (1) H is asserted. The next Index following the missed clock will reset the timing error latch and if CD2 GO (1) H was not asserted during that disk revolution, DTE is not produced.

NOTE

When the drive is in Maintenance Mode, the Timing Error gate is disabled.

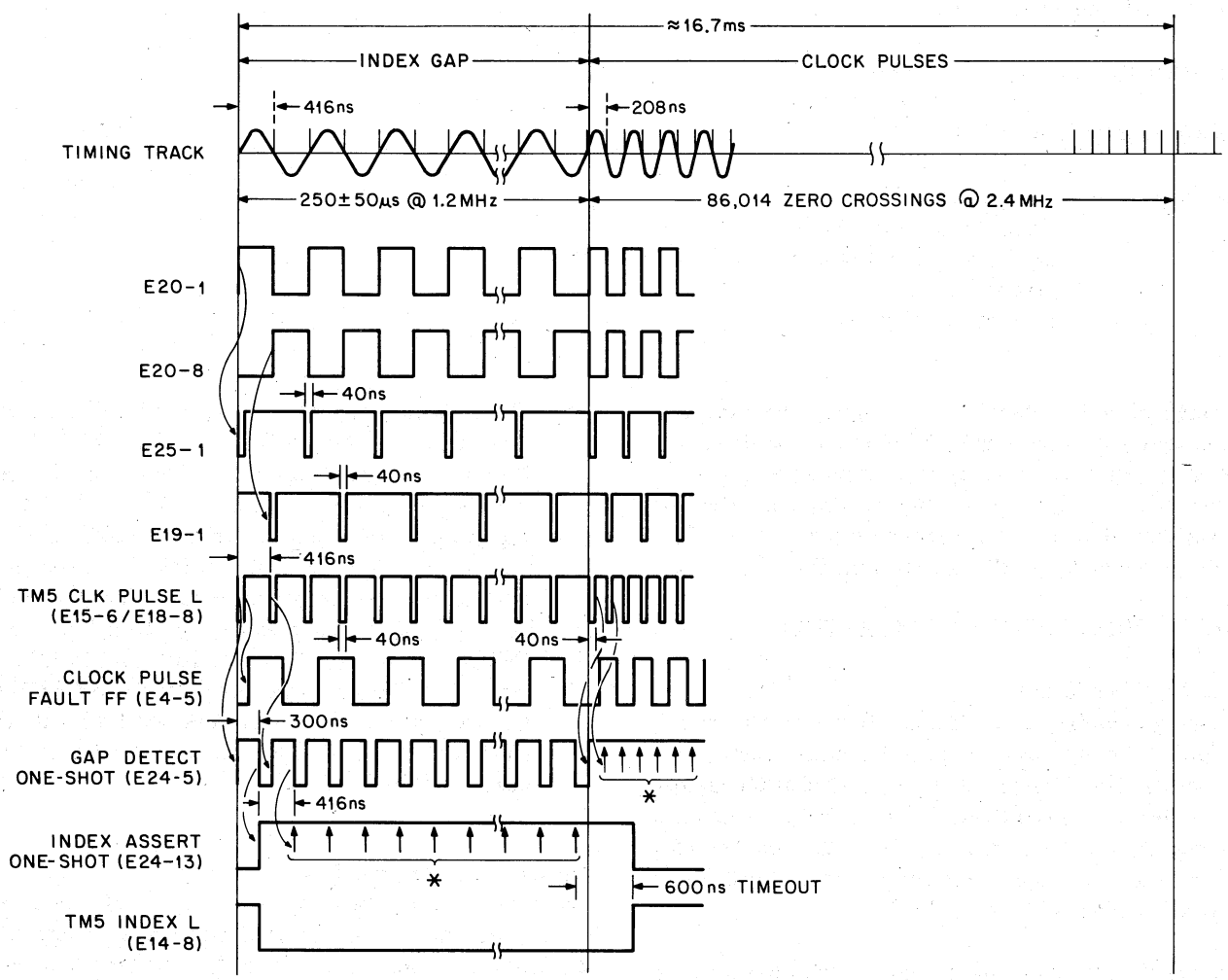

Figure 3-27 Index and Clock Pulse Timing

TM5 INDEX L Error – During normal operation, TM5 INDEX L triggers retriggerable MISSING INDEX one-shot (E9–1). Since the time interval between Index gaps is approximately 16.7 ms for 60-Hz drives and 20 ms for 50-Hz drives, and the one-shot time period is 28 ms, successive TM5 INDEX L signals retrigger this one-shot prior to its time-out period. If TM5 INDEX L is not asserted within 28 ms, the MISSING INDEX one-shot times out. This action enables the Timing Error gate to produce the signal TM5 SET TIMING ERR L. This signal sets DTE whenever CD2 GO (1) H is asserted. If an Index is generated on the next disk revolution, it will reset the timing error latch; if CD2 GO (1) H was not asserted at any time during the previous revolution, no DTE is produced.

Sector Boundary Counter

The Sector Boundary Counter (E13,17,23) is a modulo-1334 counter. *IC E23* of this counter *is a decimal counter chip,* which produces one CLK output to the next counter circuit for every ten TM5 CLK PULSE L cycles. ICs E13 and E27 are binary counter chips. The Sector Boundary Counter is held preset to binary 0111 1001 1000 by the assertion of either TM5 INDEX L or TM3 SEC PULSE L.

The function of this counter is to generate a signal, TM3 SEC PULSE L, consisting of one pulse per sector, to mark the beginning of each sector. The first sector begins 512 clock pulses after negation of TM5 INDEX L; this is

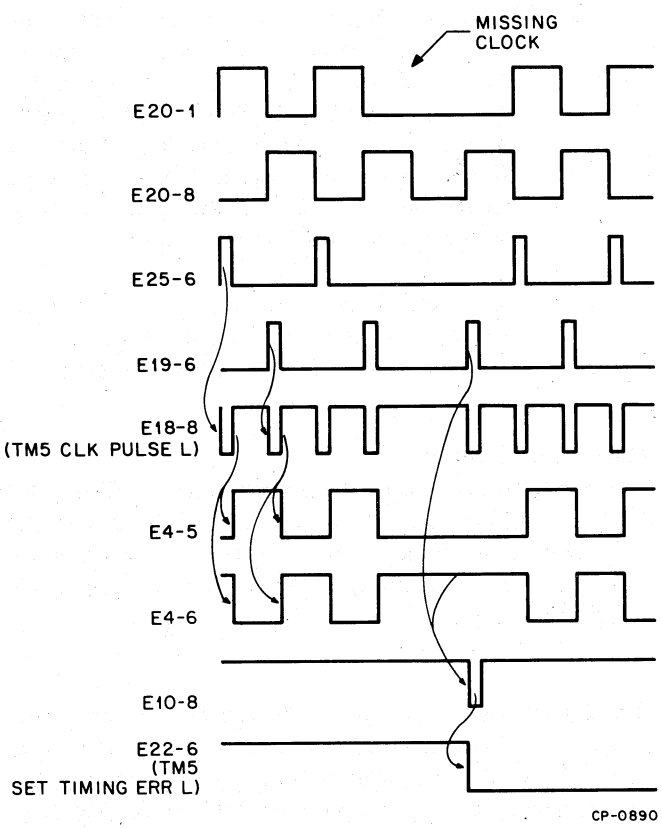

Figure 3-28 Clock Pulse Error Timing Example

detected by gate E12 to produce a sector pulse. Thereafter, for the rest of the disk revolution, every sector pulse is generated when gate E16–6 detects a maximum count of binary 1111 1111 0000 in the counter. This corresponds to 1,334 TM5 CLK PULSE L cycles.

Resync and Sector Pulse Generation (Figures 3-29 and 3-30)

A step phase error may be introduced into the phase locked loops at the transition from one frequency to another, at the end of the Index gap; therefore, an initial loop resynchronization interval is required after each complete revolution of the recording disk. The resync and sector pulse generation is accomplished as follows:

1-3. TM5 INDEX L

- Resets Resync flip-flop (E21–13) to assert TM3 RESYNC L
- Presets Sector Boundary Counter to binary

0111	1001	1000
E13	E17	E23

- Presets Sector Counter to binary

1100	0000
E3	E8

4. TM5 INDEX L negation allows TM5 CLK PULSE L to increment Sector Boundary Counter.

5&6. When the Sector Boundary Counter reaches the binary state 1010 1101 0000, 512 TM5 CLK PULSE L cycles, following Index negation, have been counted. This is detected by gate E12, which enables the D input of Sector Boundary flip-flop (E21–2). The next TM5 CLK PULSE L negation clocks this flip-flop set to assert TM3 SEC PULSE L and to reset the Sector Boundary Counter. The next TM5 CLK PULSE L negation resets the Sector Boundary flip-flop, since the Sector Boundary Counter is now back to binary state 0111 1001 1000. This clocks the RESYNC flip-flop set and removes the preset signal from the Sector Boundary Counter, enabling it to resume counting.

7&8. When Sector Boundary Counter reaches binary state 1000 0000 0000, after negation of TM3 RESYNC L, 62 TM5 CLK PULSE L cycles have occurred; this assertes the signal TM3 SET SYN H, which indicates that the preamble for each sector is nearly complete.

9&10. TM5 CLK PULSE L continues to increment the Sector Boundary Counter until the counter reaches binary state 1111 1111 0000. This is detected by E16–6 which enables the D input of Sector Boundary flip-flop (E21–2). The next TM5 CLK PULSE L negation clocks this flip-flop set to assert TM3 SEC PULSE L and to reset the Sector Boundary Counter. The next TM5 CLK PULSE L negation resets the Sector Boundary flip-flop, enabling the Sector Boundary Counter to resume counting. This also enables gate E15–11 to increment the Sector Counter. A total of 1334 TM5 CLK PULSE L cycles occur from leading edge to leading edge of TM3 SEC PULSE L.

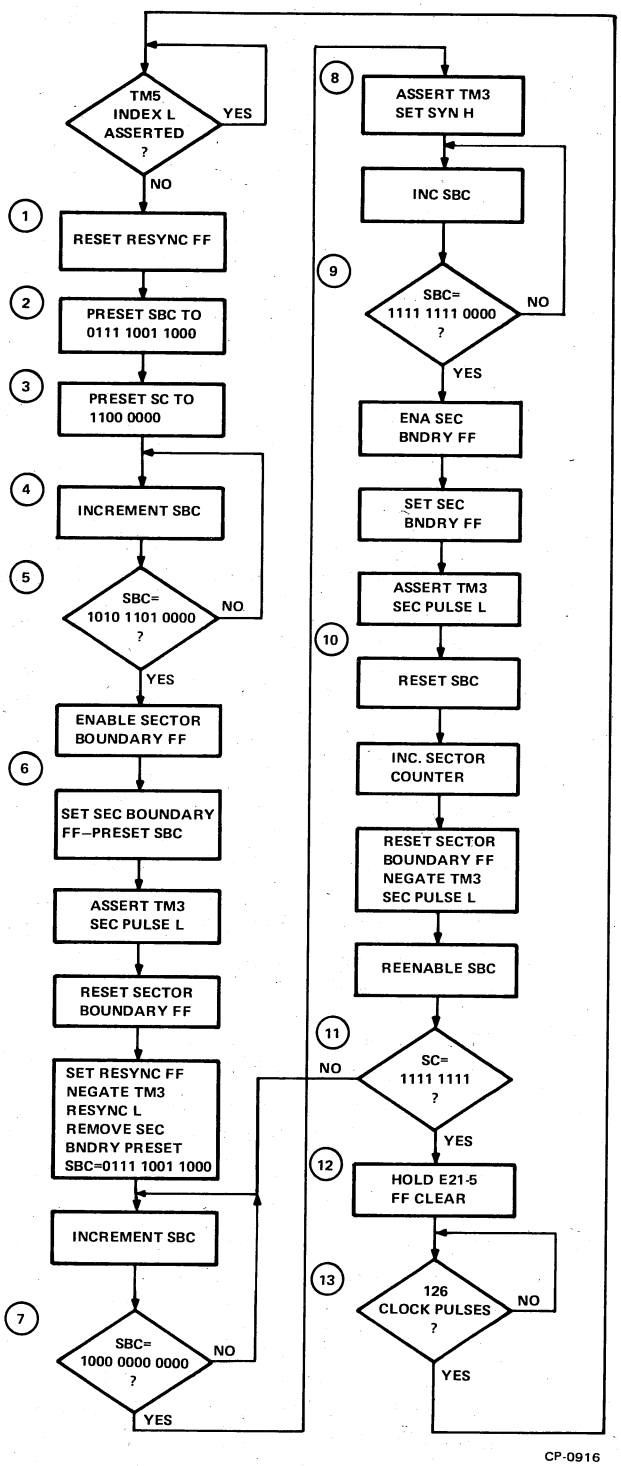

Figure 3-29 Resync & Sector Pulse Generation Troubleshooting Flow Chart

11&12. When the Sector Counter reaches binary state 1111 1111, 64 sector pulses have occurred. This is detected by E16–8 to hold the SECTOR BOUNDARY flip-flop (E21–5) clear. In this way, the Sector Boundary Counter is allowed to increment through the dead band, beyond the end of the last sector, without producing any additional sector pulses.

13. 126 clock pulses remain beyond the end of the last sector. Once past this, the Index area is encountered and the entire cycle is repeated.

Look-Ahead Register

The Look-Ahead register consists of a set of 7401 gates (E1, E6, & E11) which, when enabled by CN2 RD LK AHD REG L, gate out the appropriate bits of the Sector Counter and the Sector Boundary Counter onto the wired-OR register bus.

Bits 00–05 of the Look-Ahead register are the sector fraction. Although these bits increment through the entire range, from 00_8–77_8, the fraction is held at 00_8 through the preamble, by the negation of TM3 SET SYN H at E15–10. At the time TM3 SET SYN H is asserted, TM3 LOOK AHEAD (0:5) H contains all zeros, so the fraction still does not change until another 20 bits have occurred. Once the fraction starts to increment, it continues to increment, through the remainder of the sector, at approximately 4 μs per count. Also, since TM3 SET SYN H is not asserted during Index or the Resync period, the sector fraction is held at zero during both Index and Resync.

Sector Interleaving Option

The Sector Interleave option is implemented by two quad 2:1 multiplexers (E2 & E7) and jumper W1. With the jumper in, the "A" multiplexer inputs are enabled to the outputs and the bits in the Sector Counter correspond directly to the Sector Address bits; i.e., TM3 SEC COUNT 0 H corresponds to TM4 SEC ADD 0 H, TM3 SEC COUNT 1 H corresponds to TM4 SEC ADD 1 H, TM3 SEC COUNT 2 H corresponds to TM4 SEC ADD 2 H, etc. When the jumper is removed, a logic 1 is applied to the select input to the multiplexers and the "B" inputs are enabled to the outputs. In this mode, the least-significant bit of the Sector

Counter becomes the most-significant bit of the Sector Address and the remaining Sector Count bits are decreased in significance, one bit position before being gated out as Sector Address bits. For example:

TM3 SEC COUNT 0 H corresponds to TM4 SEC ADD 5 H

TM3 SEC COUNT 1 H corresponds to TM4 SEC ADD 0 H,

TM3 SEC COUNT 2 H corresponds to TM4 SEC ADD 1 H,

etc.

Table 3-2 illustrates the principle involved.

Maintenance Mode

When the drive is placed in Maintenance Mode, by setting bit 00 in the Maintenance register, TM5 CLK PULSE L and TM5 INDEX L are no longer derived from the timing track. To do this, the assertion of CD3 MAINT H disables E14–2 and E14–13 and enables E14–4 and E14–10. TM5 CLK PULSE L is now derived from the MCLK H input at E14–3, which is driven by the signal CD3 M CLK H. TM5 INDEX L is derived from the CD3 M IND H input at E14–9.

Although the Timing Error gate (E10) is disabled by the assertion of CD3 MAINT H, the remainder of the Timing logic functions in exactly the same manner as when *not* in Maintenance Mode. In this way, timing of all drive functions is under control of the processor when the drive is in Maintenance Mode.

PERFORMANCE CHECKS

See Table 3-1.

TROUBLESHOOTING

See Table 3-1.

Table 3-2
Sector Count/Sector Address in Interleaved and Non-Interleaved Systems

TM3 Sector Count						(Jumper In) Non Interleaved TM4 Sector ADDR							(Jumper Out) Interleaved TM4 Sector ADDR						
5H	4H	3H	2H	1H	0H	5H	4H	3H	2H	1H	0H	Addressed Sector	5H	4H	3H	2H	1H	0H	Addressed Sector
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	32
0	0	0	0	1	0	0	0	0	0	1	0	2	0	0	0	0	0	1	1
0	0	0	0	1	1	0	0	0	0	1	1	3	1	0	0	0	0	1	33
0	0	0	1	0	0	0	0	0	1	0	0	4	0	0	0	0	1	0	2
0	0	0	1	0	1	0	0	0	1	0	1	5	1	0	0	0	1	0	34
0	0	0	1	1	0	0	0	0	1	1	0	6	0	0	0	0	1	1	3
0	0	0	1	1	1	0	0	0	1	1	1	7	1	0	0	0	1	1	35
0	0	1	0	0	0	0	0	1	0	0	0	8	0	0	0	1	0	0	4
0	0	1	0	0	1	0	0	1	0	0	1	9	1	0	0	1	0	0	36
									Etc.										

3.4.1 Read/Write and Detection Module G182

Logic Assembly Slot Locations – AB17

Signal Mnemonic Prefix – RW

Circuit Elements – Write Amplifier
Read Amplifier and Detection Circuits

CIRCUIT ELEMENT THEORY OF OPERATION

Write Amplifier

The Write Amplifier consists of a constant current source, a Write flip-flop (E4), and two write current switches; Figure 3-31 is a simplified diagram of these elements. The constant current source produces a fixed write current of nominally 96 mA, which is switched through either half of the selected read/write head. The current source consists of D3, D4, R13, R14, R39, R40, Q5, and Q6.

The Write flip-flop is a JK flip-flop; its J and K inputs are both enabled by the assertion of ED2 WRT GATE L, allowing each negative edge of ED2 WRT DATA PULSE L to complement the flip-flop. The signal TM3 SEC PULSE L is used to initialize this flip-flop so that each sector starts with this flip-flop in the same state.

The write current switches are both off until the beginning of the sector to be written. The level shifters which drive the switches are enabled by the assertion of ED2 WRT GATE L at E6-2.

NOTE

If the drive is executing a write function in Maintenance Mode (CD3 MAINT L asserted), both switches are turned off to prevent destruction of previously-recorded data.

Once enabled, only one switch is on at any time; this switch is determined by the state of the Write flip-flop. A low output from the flip-flop turns the switch on, a high output turns the switch off. One switch (including the level shift circuit) consists of R5, R7, R9, Q1, and Q3; the other consists of R6, R8, R10, Q2, and Q4. At the conclusion of the sector, both switches are disabled by the negation of ED2 WRT GATE L.

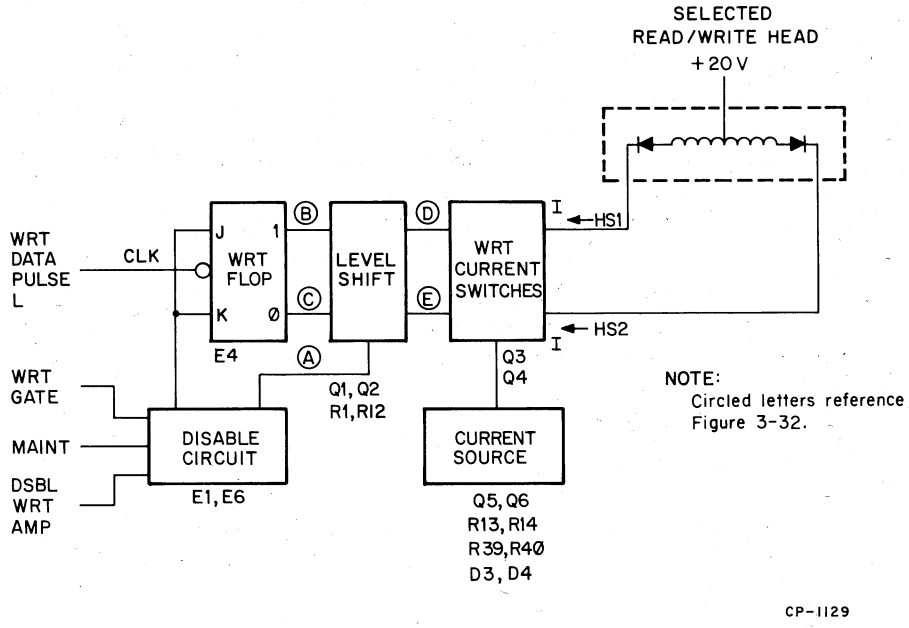

Figure 3-31 Write Amplifier (G182) Elements, Simplified Block Diagram

Any time a power fail condition exists (Paragraph 2.2.6) the write current switches are disabled by the assertion of CN2 DSBL WRITE AMP L which pulls the emitters of Q1 and Q2 low so neither transistor can turn on.

Figure 3-32 is a timing diagram of a typical write sequence.

Read Amplifier and Detection Circuits

When reading, magnetic flux reversals on the disk generate a small differential voltage between the ends of the head coil. The read amplifier and detection circuits must amplify this signal and detect the peaks, which correspond to the flux reversals, to reproduce the sequence of pulses originally written.

The read signal from the selected head is ac-coupled to the first amplifier by the input biasing network (Figure 3-33). The first amplifier (E7) has a gain of approximately 20. The output of this amplifier can be observed differentially with an oscilloscope between test points TP1 and TP2. This amplified signal is then phase-shifted 90°. The 90° Phase Shift network converts the peaks of the input signal to zero-crossings. The phase-shifted signal is amplified by amplifier E8, which has a gain of 10. The signal is then low-pass filtered to remove any high-frequency noise. The filter has an attenuation of approximately 50 percent. The output of the low-pass filter can be observed differentially with an oscilloscope between test points TP4 and TP5. The zero-crossing detection circuit consists of two comparators (E5): one to detect positive-going zero-crossings, the other to detect negative-going zero-crossings. A positive transition from a comparator output triggers the one-shot (E2 or E3) associated with that comparator. The outputs of the two one-shots are ORed together to produce the signal RW2 RD DATA PULSE L.

Figure 3-34 is a timing diagram of a typical read sequence.

PERFORMANCE CHECKS

See Table 3-1.

TROUBLESHOOTING

See Table 3-1.

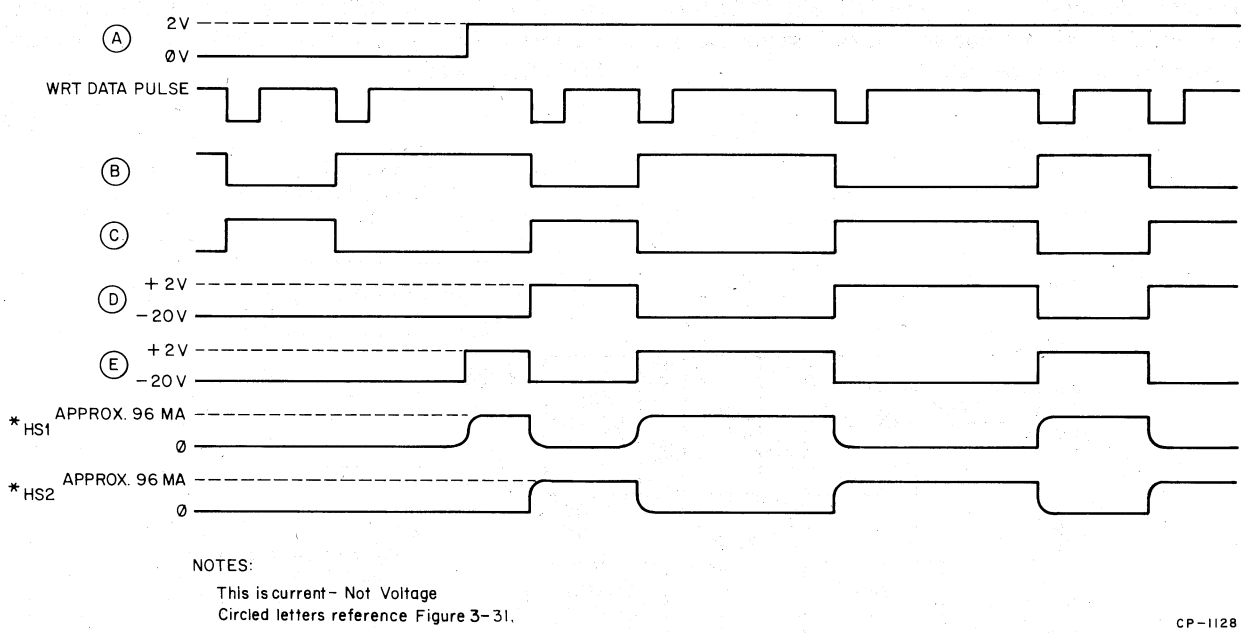

Figure 3-32 Write Sequence Timing Diagram

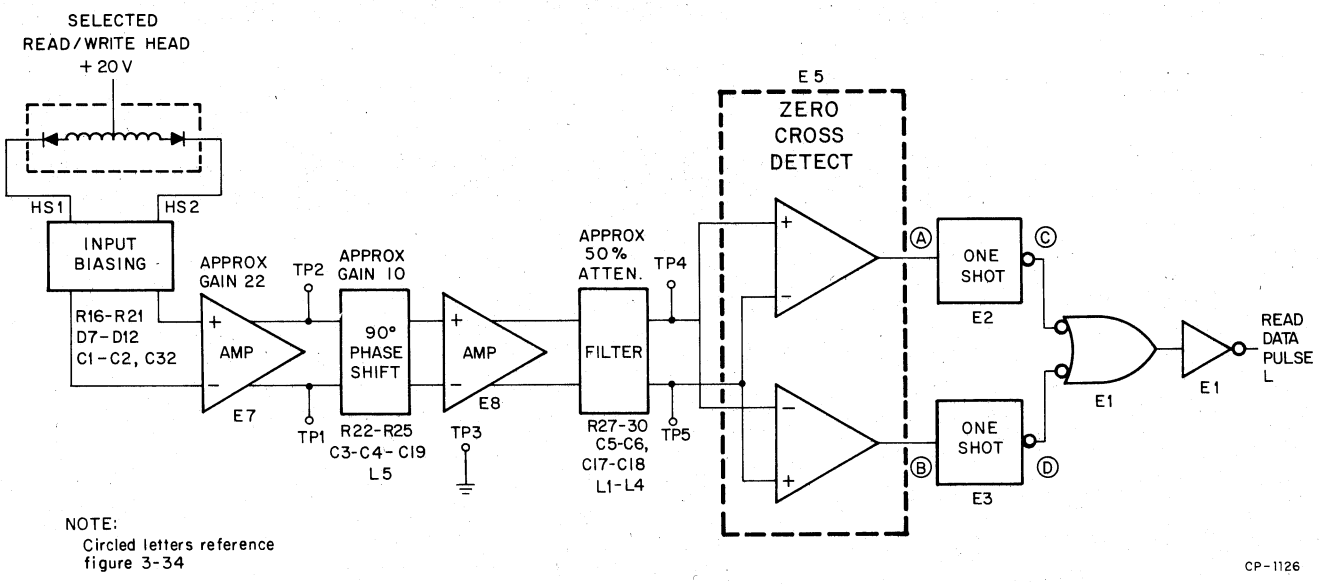

Figure 3-33 Read Amplifier (G182) Peak Detection, Simplified Diagram

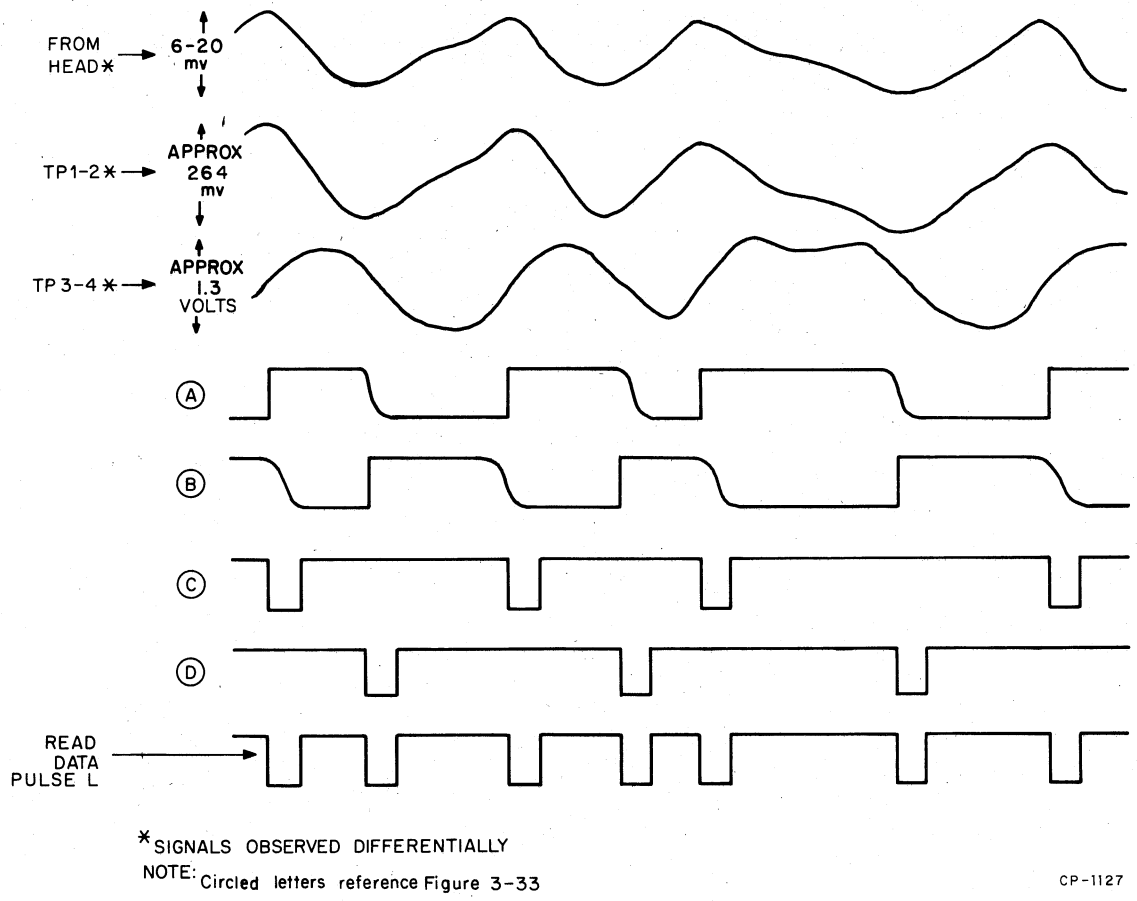

Figure 3-34 Read Sequence Timing Diagram

3.4.2 Head Matrix Module M7758

Logic Slot Locations – AB18, AB19

Signal Mnemonic Prefix – HM

Circuit Elements – Binary Decoders
Head Drivers

CIRCUIT ELEMENT THEORY OF OPERATION
Head selection is accomplished using a row-column matrix technique; the column refers to a head block, while the row refers to 1 of the 8 heads contained in that head block. A Head Matrix module can select 1 head (ferrite or track) from any of 4 head blocks, or 1 track out of 32 (Figure 3-35).

Since there are 64 physical data tracks in the RS03, 2 Head Matrix modules are required.

One Head Matrix module (AB18) selects tracks $00_8 - 37_8$ while the other (AB19) selects tracks $40_8 - 77_8$. The most-significant bit of the six track address bits (AD2 TRK X4 H) is used to determine which Head Matrix module is active at any one time. AD2 TRK X4 H is wired on the logic backplane to pin B18 M2, which enables the Column Decoder (E1-13) on this module whenever the signal is low. AD2 TRK X4 H is wired to pin B14P2, which is an inverter input. The inverter output, B19N2, is then wired to B19M2, which enables Column Decoder (E1-13) on this module whenever AD2 TRK X4 H is high.

The next two most-significant track address bits, AD2 TRK X2 H and AD2 TRK X1 H are decoded by the Column Decoder (E1-14, 15) to select one of four head blocks associated with that Head Matrix module. Decoder outputs f_0–f_3 drive level-shifting transistors, which in turn drive the column-selection transistors.

The other three track address bits, AD2 TRK 4X H, AD2 TRK 2X H, and AD2 TRK 1X H are decoded by Row Decoder (E3–13, 14, 15). Row decoder outputs f_0–f_7 select one row out of eight head center taps. Level shifting from logic levels to +20 V is accomplished by the 75451 drivers (E4–E7). The selected row is switched to +20 V by one of the transistors (Q17–Q24).

Both the Row and Column Decoders are disabled by the assertion of the signal AT02 SP GATE L. This signal is asserted by the Alternate Track Option module (M7756) whenever the track address contained in the Desired Address register is wired to one of the spare data tracks.

Each Head Matrix module has four head cables attached to it; each cable has a male connector on one end which mates with a connector on each head block assembly. The cable connectors are held in place, on each head block, by a knurled thumbscrew. The labelling of the cables and their routing within the drive is discussed in Paragraph 3.4.4.

PERFORMANCE CHECKS
See Table 3-1.

TROUBLESHOOTING
If data errors are occurring on up to half the tracks (either 00_8–37_8 or 40_8–77_8), this module may be at fault. Depending on the exact nature of the failure, *several* courses may be followed.

If the failing track(s) are located on only one head block (e.g., tracks 40_8–47_8), interchange that head cable with another head cable from the same Head Matrix module (e.g., interchange the 30 and 40 head cables). If the problem remains on the original track address, this module is probably at fault. If not, the original track/head may be at fault. If the failing tracks contain a common row address (e.g., 03_8, 13_8, 23_8, 33_8), interchange the two head Matrix modules *and cables.* If the failures now occur on another group of tracks (e.g., 43_8, 53_8, 63_8, 73_8), the Head Matrix module is at fault. If the problem remains with the original addresses, the problem is not in the Head Matrix, but is more likely in one or more of the heads. See Paragraph 3.2.3 for procedures to verify a head failure.

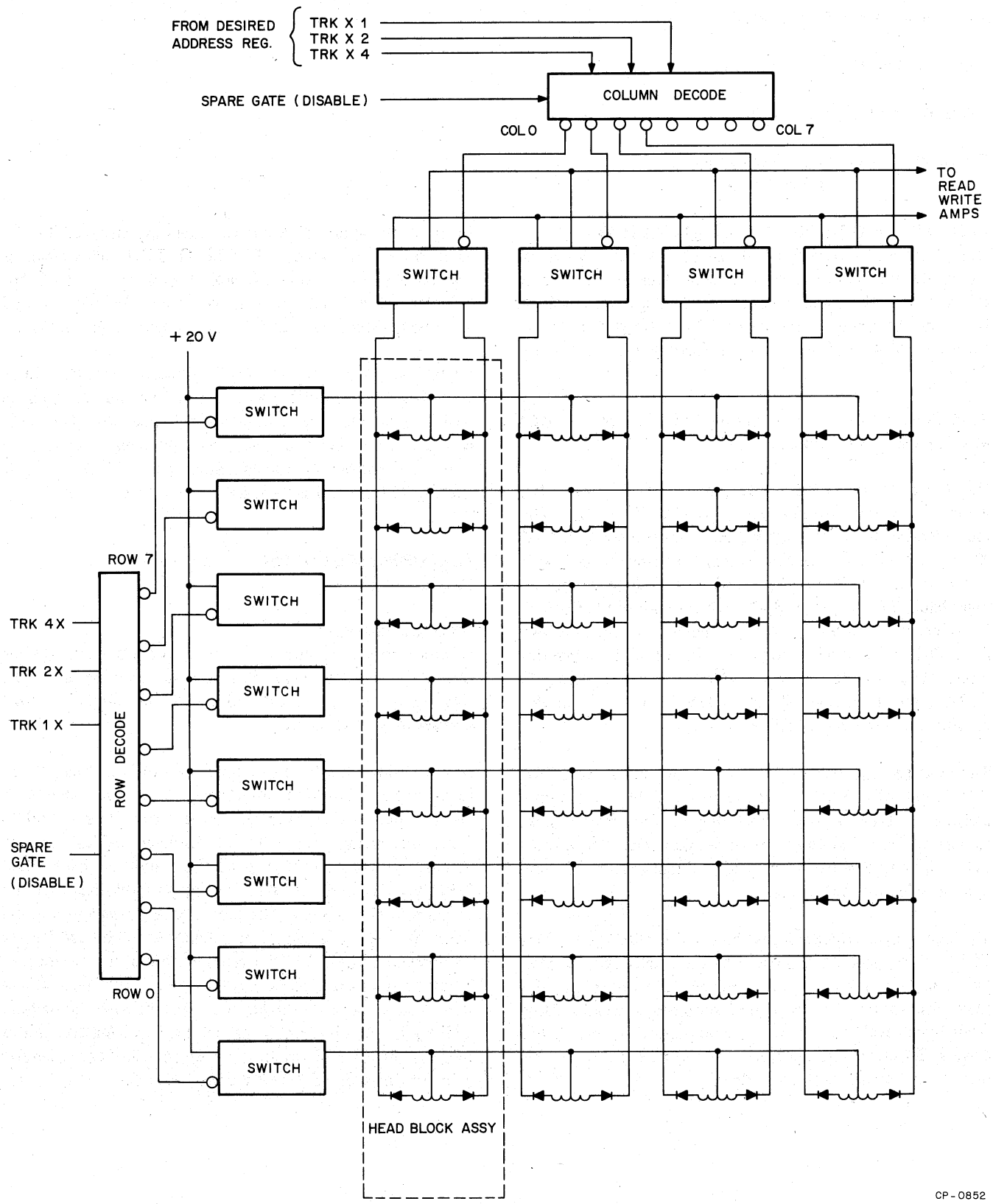

Figure 3-35 Head Matrix Module (M7758) Simplified Diagram

3.4.3 Alternate Track Option M7756

Logic Slot Locations – AB20

Signal Mnemonic Prefix – AT

Logic Elements – **Binary Decoders**
Head Drivers
Track Selection Jumpers
Alternate Track Gating

The Alternate Track Option module receives the six track address bits directly from the Desired Address register. There are two decoders, a Column Decoder and a Row Decoder, which are enabled *at all times.* The Column Decoder decodes the three most-significant track address bits (AD2 TRK X4 H, AD2 TRK X2 H, and AD2 TRK X1 H); the Row Decoder decodes the remaining three track address bits (AD2 TRK 4X H, AD2 TRK 2X H, and AD2 TRK 1X H). However, the outputs of the two decoders are ignored unless jumpers have been installed to select the spare track(s).

The spare track selection jumpers are always installed in pairs. One of the two jumpers connects one output from the Row Decoder to an input of one of the eight AND gates (E3, 5). The other jumper connects one output from the Column Decoder to the other input of the same AND gate. The outputs of the two decoders, which are ANDed together, determine the address of the track being replaced by the spare track associated with that AND gate.

The outputs of an AND gate do two things when high. First, through one of the level-shifting transistors (Q1–Q8), it switches the center tap of the selected spare head to +20 V (through one of transistors Q9–Q16). Second, through OR gate E1 and E6–12, 13, it asserts AT02 SP GATE L and switches on transistors Q19, 20 (through level-shifting transistors Q17, 18) which connect the selected spare read/write head to the read/write amplifier.

The Alternate Track Option module has one head cable attached to it, similar to those on the Head Matrix module. Cable routing and labelling is discussed later in subsection 3.4.4.

Installing Spare Track Selection Jumpers

NOTE

Alternate Track Option modules with Etch Rev E or later contain two dual-in-line sockets between the lines of split lug terminals. These sockets are intended to facilitate testing of this module by Manufacturing and must *NOT* be used by Field Service Personnel.

Proceed as follows:

1. Using the diagnostic programs, determine which track address is failing.

   NOTE

   Generally, if more than one track is failing, the problem is not due to a defective head. Attempt to locate a problem elsewhere first.

2. Turn off the dc power supply. From the logic rack, remove the Alternate Track Option module. Disconnect the head cable from the spare head to work on the module conveniently.

3. As shown in Figure 3-36, there are two groups of split lugs (column and row) on the module, each group consisting of two lines of eight lugs. In each group, the line (labelled "C" and "R") nearest the module handle is associated with the spare track, while the other line (labelled "CL" and "RW") is associated with the track address to be replaced. Examine the spare track line of split lugs on the module and select any unused pair of lugs *of the same number,* one from the "C" line and one from the "R" line.

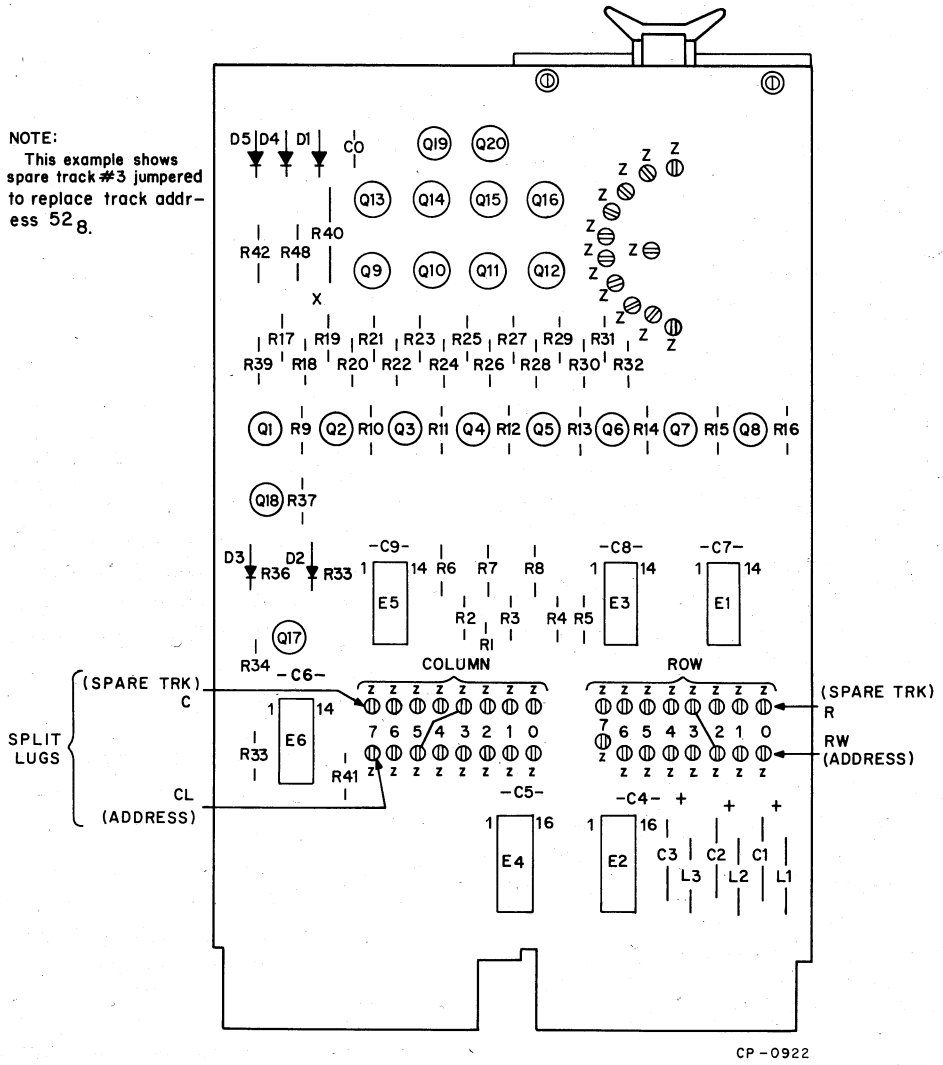

Figure 3-36 Alternate Track Wiring Example (Showing Spare Track No. 3 Jumpered to Replace Track Address 52_8)

In the example shown in Figure 3-36, 3R and 3C were selected.

NOTE

The logic rack end plate contains a decal, listing which spare tracks have been used and which track addresses have been replaced by those spares.

4. Solder one jumper from the selected lug in the C line to the lug in the CL line, corresponding to the column of the track address to be replaced. In the example shown in Figure 3-36, the jumper is connected between 3C and CL5, because 5 is the column in track address 52_8.

NOTE

Always use insulated wire for these jumpers to prevent jumpers that cross from shorting together.

5. Solder a second jumper from the selected lug in the R line to the lug in the RW line, corresponding to the track address to be replaced. In the example shown in Figure 3-36, this jumper is connected between 3R and RW2, because 2 is the row in track address 52_8.

6. Ensure that both jumpers were installed correctly.

7. Replace the module in the logic rack and reconnect the head cable to the spare head.

NOTE

The head connector contains two rectangular inserts in one end, which allow the connector to be connected to the head in one direction only. DO NOT REMOVE THESE INSERTS.

8. Turn on the dc power supply.

9. Run diagnostics to verify that installation of the spare track corrected the problem.

10. After verifying that the problem has been corrected, update the decal on the logic rack end plate; specify the spare track to which the address was jumpered.

3.4.4 Cabling

Cabling from the heads to the logic rack has been arranged in an orderly fashion, with connector labels, to facilitate proper installation should it become necessary to disconnect the cables from the heads, or to change one of the associated modules. Each Head Matrix module (M7758) contains four head cables that terminate in head block connectors. Each of these connectors has been labelled with a dual address for proper head block connection. The connectors are labelled "00/40", "10/50", "20/60", or "30/70". The connectors labelled "00/40" can connect to either head block 00 or 40, depending upon which logic slot the Head Matrix module is plugged into.

The Alternate Track Option module (M7756) contains one head cable which terminates in a head block connector labelled "SP". The cable from this module plugs into the SP head block.

The timing track head cable is labelled "TIM". It originates at the Timing Amp module (G092) in slot AB16 and plugs into the timing track head. Figure 3-37 illustrates this relationship.

No special routing is observed for the 10 head cables, however, do not pinch these cables between the bottom cover and the chassis when replacing the bottom cover.

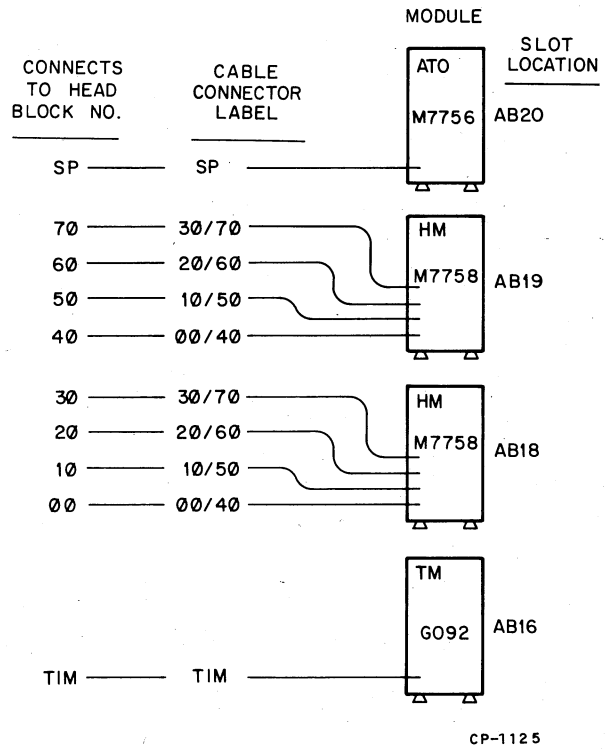

Figure 3-37 Module to Connector Relationship

The timing track head connector is keyed by two rectangular inserts, in diagonally-opposite corners, so that it can be plugged into the timing head in either of two ways. This allows use of the alternate timing track by simply unplugging the connector, rotating it 180°, and replacing it on the timing head.

The remaining 9 head connectors are each keyed by two rectangular inserts, in one end of the connector, so that each connector can be plugged into a head in only one way.

CAUTION

DO NOT REMOVE THESE INSERTS FROM ANY HEAD CONNECTOR. All head connectors must be secured to the head blocks by finger-tightening the knurled thumbscrews.

3.5 POWER SUPPLY

The RS03 power supply can be divided into 5 areas: the ferroresonant transformer, the +20 V, −20 V, and +5 Vdc regulators, and the voltage-sensing circuit. Except for the ferroresonant transformer, the other four parts of the power supply are mounted on the Power Supply Regulator module (5410188). The transformer is mounted separately on the power control assembly chassis.

The primary of the *ferroresonant transformer* and the resonant capacitor form a parallel-resonant circuit at the frequency of the ac line (50 or 60 Hz). The resonant frequency is determined by the transformer, so different transformers are required, depending on the drive operation line frequency. The ferroresonant transformer provides constant secondary voltages over a very wide range of primary input voltage.

The *+20 Vdc regulator* provides an output of +20 V ± 7%. It has a current rating of 1 Amp with a maximum ripple of 200 mV peak-to-peak and is overcurrent-protected.

The regulator is a class A feedback amplifier. The output voltage is divided by resistor network R5, R7. The resistor network output is compared to the reference voltage provided by Zener diode D1 (13 V ± 5%) by transistor Q4. Q4, which operates in the linear region, controls the base drive to pass transistor Q1 in the following way. The emitter of Q4 is held at a nominal 13 V by D1. The base of Q4 (and the R5, R7 output) is one diode drop (0.7 V) higher. If the +20 V tries to go high, more current will flow through R5. This current must go to the base of Q4, since the voltage drop across R7 is fixed. This extra base current causes Q4 to draw more collector current, thus diverting base current from Q1, which forces the +20 V down. Conversely, if the +20 V tries to go low, Q4 will receive less base current, making more base current available to Q1, which forces the +20 V up.

Q5 provides overcurrent protection; it is normally off. If the voltage across R3 becomes greater than 0.7 V, Q5 conducts, shunting base current from Q1, thereby limiting the current that Q1 provides.

The *−20 Vdc regulator* provides an output of −20 V ± 7%. It has a current rating of 1.5 Amps with a maximum ripple of 200 mV peak-to-peak and is overcurrent-protected.

This regulator is the complement of the +20 V regulator and its operation and theory is similar.

The *+5 Vdc regulator* provides an adjustable output of +4.7 V – +5.4 V. *THIS IS THE ONLY ADJUSTMENT IN THE RS03.* This regulator has a current rating of 9 Amps, with a maximum ripple of 20 mV peak-to-peak. It contains protection circuitry for both overvoltage and overcurrent. The regulator output should *always* be adjusted for +5.0 V *at the logic backplane.*

IC E1 and transistors Q8 and Q2 provide the regulation and short-circuit protection. Q8 drives the pass element Q2 to provide the 9 Amp capability. Resistors R12, 14 and potentiometer R13 provide the output voltage adjustment.

CAUTION

Potentiometer R13 can be reached, with a small insulated pot adjustment tool, through an access hole in the power control assembly in the rear of the drive. Use of a metal screwdriver may damage the power supply by shorting components to the chassis.

Overcurrent protection is provided by R16, R17, and R18. As the current increases (> 9 Amps), the drop across R18 increases as does the voltage at the junction of R16 and R17. As this voltage rises, E1 reduces drive to Q8 and therefore Q2, thus limiting output current.

Q9 and Q10 provide overvoltage protection. As the output rises above the base of Q9 enough to turn Q9 on, Q9 couples Q10's gate back to its anode, turning Q10 on and pulling +5 V to ground.

The current sensing circuit (R16, R17, R18) mentioned previously senses an overcurrent caused by the "on" SCR (Q10) and shuts the +5 V supply "off".

NOTE

E1 is powered from the +20 V supply, allowing the +5 V protection circuits to remain functional even without +5 V existing properly. It is important to realize that the +20 V supply *must be operational before the +5 V regulator can operate* properly.

The *Voltage-Sensing circuit* asserts SAFE L when the ac and all three dc voltages are present. When ac power is interrupted, the SAFE L signal goes high, through the ac sensing circuit (D3, D4, R21, R22, C7, R23, and Q11). This signal is negated at least 4 ms before the +5 V regulator output falls, providing sufficient time to cycle down the drive.

+20 V, +5 V and −20 Vdc are monitored by E2, Q13, and the associated resistive network. This circuitry senses *only* voltage presence, not the magnitudes of these voltages. Q2 drives the wire carrying SAFE L to the logic backplane.

When the ac power first turns on, the SAFE L signal rises with the +5 V (rectifier charging waveform) until Q13 starts to conduct, which switches SAFE L low to signify that dc power is ready. Q13 stays off until the +5 V has reached +4.2 V or above.

Power-up and power-down sequencing of the drive, based on the state of SAFE L, is provided by the Control module (M7755) described in subsection 3.3.3.

PERFORMANCE CHECKS

See Table 3-1.

TROUBLESHOOTING

Before checking any suspected power supply problems, check the voltage at the ac outlet and at the transformer primary. If the ac line voltage is acceptable, check the unregulated, rectified voltages at the inputs to the regulators. Table 3-3 lists the checkpoints.

Table 3-3
Power Supply Checkpoints

Regulator	Input Point	Minimum (dc) Level (Measure with Oscilloscope)
+20 V	Collector of Q1 (case)	+25 V
−20 V	Collector of Q3 (case)	−25 V
+ 5 V	Fuse F1	+10.5 V

NOTE

These measurements *must* be made with an oscilloscope because the lowest point on the ripple must be greater than the numbers specified.

If the regulator input voltages are below the minimum values listed, check bridges D7, D8 or filter capacitors C1, C2, C3.

NOTE

If replacement of D7 is necessary, use plenty of heat sink compound (9008268) to ensure adequate heat sinking of new bridge.

If the regulator input voltages are acceptable, remove the load by disconnecting J2. If this corrects the problem, a short circuit in the logic rack exists. This may be due to a short on the wire-wrap backplane or a failed component on one of the modules. Remove all modules from the logic rack (do not disconnect cables), reconnect J2 to the power supply module, and turn on the power supply (move SW1 on the power control assembly to LOCAL). If dc returns, a short exists on one of the modules. Inspect each module and check with an ohmmeter until the problem is found and corrected. If dc does not return, the short is on the backplane or in the power cable between J2 and the backplane. Inspect the cable for broken wires and broken or worn insulation; inspect the backplane for any debris or solder splashes.

If removing the load does not correct the overload condition, the problem is within the power supply module.

+20 V Regulator Procedure

If the input to the +20 V regulator is correct (Table 3-3) but there is no output, check the dc voltage drop across R3. If it is greater than 0.65 V, excessive current is being drawn and the regulator is in overcurrent-protection mode. If the voltage drop across R3 is less than 0.65 V, either Q1 or Q4 may be defective. Check Q1 first.

If the +20 V output is too high or too low, D1 may be at fault; check the emitter of Q4 for a nominal voltage of +13 V ± 5%. The base of Q4 should be nominally 0.7 V higher.

If the ac ripple is excessive (> 200 mV peak-to-peak), check C8 and C4. Q4 could also produce excessive ripple.

−20 V Regulator Procedure

Troubleshooting procedures for the −20 V regulator are the same as for the +20 V regulator.

+5 V Regulator Procedure

If the input to the +5 V regulator is correct (Table 3-3) but there is no output, check the voltage on E1−12; it should be greater than 16.5 V. If it is low because of low +20 V, repair the +20 V regulator before proceeding. If the +20 V output is acceptable and the voltage on E1−12 is low, replace E1.

If the voltage on E1−12 is greater than 16.5 V, check E1−10. The nominal voltage at this pin is +8 V ± 1.5 V. If the voltage at E1−10 is outside this range, replace E1.

If the voltage at E1–10 is acceptable, check the emitter of Q8. The voltage at that point should be +7 V ± 1 V. If it is not, replace Q8.

If the voltage at the emitter of Q8 is acceptable, replace Q2.

3.6 POWER CONTROL

As shown on Drawing D-CS-7009006-0-1, a control voltage transformer receives its ac from and returns its low voltage ac to the power control module through J5. D22 full-wave rectifies the low voltage ac output, generating an unregulated +15 V for relays, and a Zener-regulated +5 V for logic power (*on this module only*). All Sequencing Bus and Power Control Bus signals are received on J1. Each signal is level-shifted by a resistive diode network and received by a 380. These signals are combined with drive-generated signals to control two relays: K1 and K2, which control the ac to the rest of the disk drive. Main relay K1, when activated, switches ac to the blower, fan, and drive motors and latches on until ac is removed. Power Supply Relay K2, when activated, switches ac to the power supply transformer.

The signal PULL MAIN RELAY L is asserted when there is not a START IN PROGRESS, and when both START MOTOR L and INITIALIZED L are asserted. The relay itself asserts MAIN RELAY ON L, which latches the relay on and asserts START IN PROGRESS L.

As the motor gets up to speed, its starting relay drops out, energizing Photo Isolator OCI, and UP TO SPEED H is asserted. This asserts MOTOR STARTED L, negates START IN PROGRESS L, and if EMERGENCY OFF is negated and START PWR SUPPLY L is asserted, allows PULL PWR SUPPLY RELAY L to be asserted. K2 pulls and switches ac to the power supply transformer.

All other components and/or hardware on this module serve to distribute ac to all ac devices in the drive and the jumpers in J2 permit series- or parallel-connection of windings for 115/230 V operation.

For a detailed ac distribution diagram, see Drawing 7009006-0-1.

SECTION 4
MECHANICAL SERVICING

4.1 GENERAL

This section contains detailed instructions for servicing the mechanical portions of the RS03. Procedures are separated by subassembly, with sequential procedures for removal, inspection, cleaning, and reassembly. Cleaning of the RS03 heads and disk is not recommended except as an integral part of disassembly of the device. Under normal circumstances, the RS03 should never be disassembled unless it is *absolutely* necessary.

NOTE

The DEC part numbers for all replacement parts in the RS03 are listed in the RS03 *Illustrated Parts Breakdown* (DEC-RS03-IPB-1).

Section 3.2.3 presents general criteria for determining whether a given problem is electrical or mechanical. These indications are not exclusive; they are guidelines for determining areas of malfunction.

Most procedures require that other procedures be performed as part of those steps. These are cross referenced by paragraph numbers within each procedure. The following Caution should be considered a part of each procedure:

CAUTION

Before beginning any procedure, carefully read all steps for that procedure and any procedures referenced.

4.2 FILTERS

Refer to Appendix G for a schedule of recommended filter maintenance.

4.2.1 Pre-Filter

Removal – Proceed as follows:

1. Remove the front bezel panel (Figure 4-1) by grasping the panel at the center of both sides and pulling it straight out from the front of the drive cabinet.

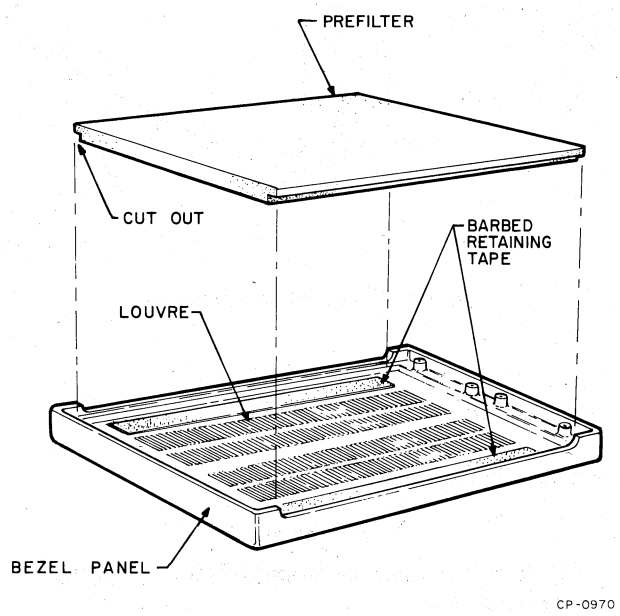

Figure 4-1 Pre-Filter Removal and Replacement

2. Pull the pre-filter away from the retaining tape barbs (Figure 4-2).

Cleaning – If a new pre-filter is not available, clean the old filter with a mild liquid detergent (e.g., Ivory) and warm water. Use a vacuum cleaner exhaust to air-dry the filter completely.

Replacement – Place the cleaned or new pre-filter, with the cut-out side down, over the tape as shown in Figure 4-2. Press the filter onto the tape barbs, ensuring that the cut-out fits within the recess in the bezel panel.

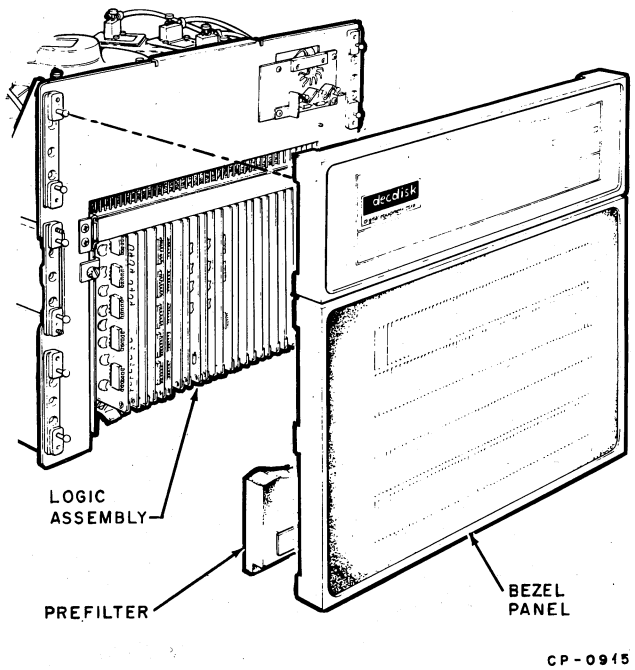

Figure 4-2 Pre-Filter Installation

4.2.2 Absolute (Disk Assembly) Filter

Removal – Proceed as follows:

CAUTION
Disk motor must be stopped before changing Absolute filter.

1. Set the mode switch SW1 (Figure 4-2) to OFF (center position); turn the main circuit breaker to OFF. Wait 5 minutes for disk to stop turning.

2. Remove the filter access plate, secured by two 6-32 X 3/8 screws, from the rear of the drive cabinet.

3. Remove the filter cover plate, secured by two 6-32 X 3/8 screws, located beneath the access plate.

4. Remove the filter loader by pulling on the outer end of the handle.

5. Remove the filter by pulling on the tape tab; discard the filter.

CAUTION
ONCE REMOVED FROM A DRIVE, A FILTER MUST NEVER BE REUSED.

Replacement – Proceed as follows:

1. Replace with new filter (12-10803-1), ensuring that the airflow arrow on the new filter agrees with the decal arrow on the rear of the drive. The arrow must point *away* from the blower motor.

2. Locate the filter loader over the edge of the filter and push in until resistance is felt – a push of several pounds force will be required to fully seat the loader against the rear end of the filter and to ensure that the filter is properly loaded.

3. Replace the cover and access plates.

4. Reset the main circuit breaker; set SW1 to LOCAL, wait 30 seconds to ensure that the disk motor is up to speed, then set SW1 to REMOTE. (A dull rattle may be heard when power is first applied. This is caused by the initial startup of the disk motor and is not cause for alarm).

4.2.3 Blower Pre-Filter

Removal – Proceed as follows:

CAUTION
The disk motor must be stopped before changing the blower pre-filter.

1. Remove the Power/Control Assembly (Paragraph 4.5).

2. Remove the three screws securing the blower pre-filter to the underside of the disk assembly.

CAUTION
ONCE REMOVED FROM A DRIVE, A FILTER MUST NEVER BE REUSED.

Replacement – Proceed as follows:

1. Locate the foam seal of the filter over the blower inlet and reassemble the hardware previously removed.

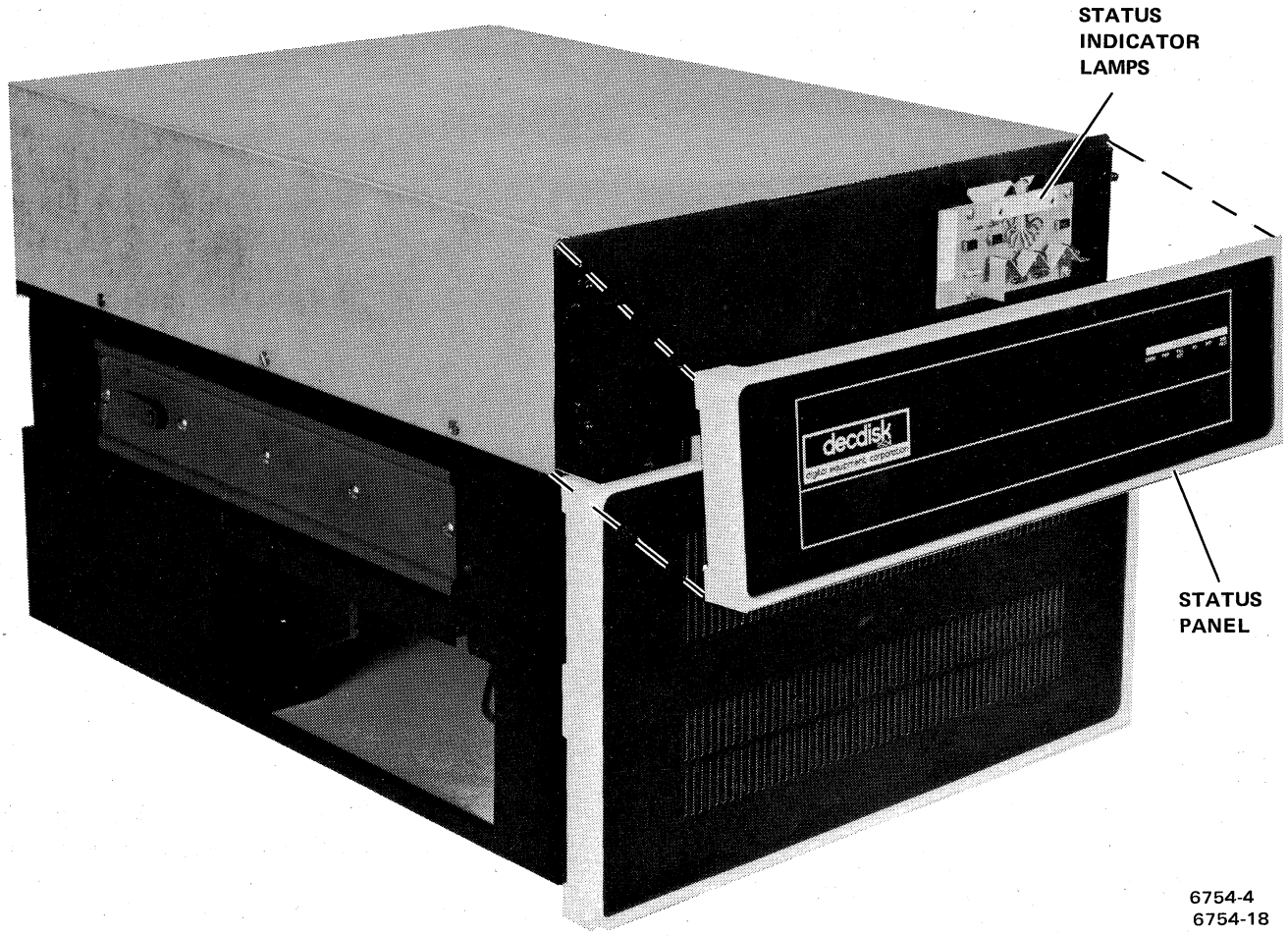

Figure 4-3 Status Indicator Lamp Access

2. Replace the Power Supply/Control Assembly (Paragraph 4.5).

4.3 STATUS INDICATOR LAMPS

Status Indicator lamps are accessed by snapping off the front status panel (Figure 4-3).

4.4 COVER (CHASSIS)

The chassis covers must be removed to gain access to the blower motor, the power supply cables, the read/write heads, the recording disk, the spindle motor, and the timing head. The cover does not need to be removed to gain access to the write lock-out switches or the drive unit select switches, to make spare track connections, to change light bulbs, or to reach test points.

Removal – (Figure 4-4)

NOTE

There are two locking plates, one for each chassis slide, located at the rear of the drive. The two screws in each plate should be removed upon receipt of the drive and the plates rotated 180°. The screws should be replaced in the clip-nuts for storage.

1. Extend the drive to its full-forward slide position.

2. Loosen the six hold-down screws on the top and bottom covers.

3. Remove the covers by outwardly flexing each cover side plate and pulling down (for bottom cover), and up (for top cover).

Replacement – To replace the covers, reverse the removal procedure. Do not pinch any head cables between the bottom cover and the chassis when replacing the bottom cover.

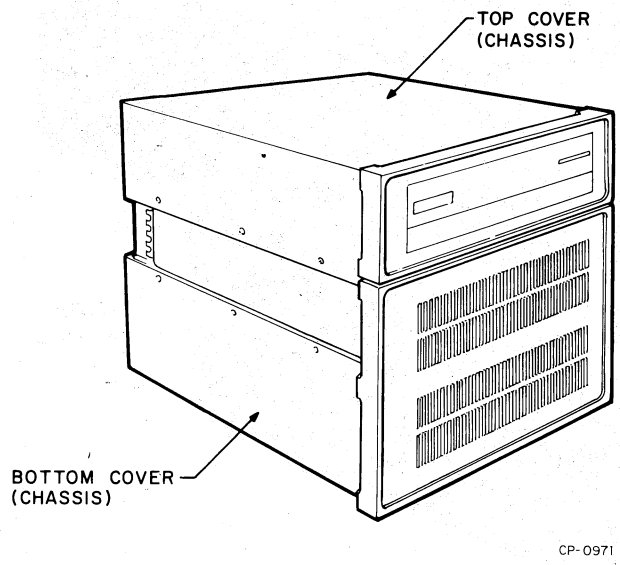

Figure 4-4 Chassis Cover Removal

4.5 POWER/CONTROL ASSEMBLY

Removal – Proceed as follows:

1. Stop the drive motor; remove all power from the drive by setting the mode switch SW1 (Figure 4-5) to OFF and turning the main circuit breaker to OFF. The drive motor should stop within 5 minutes.

2. Unplug the ac line cord from the unswitched ac.

3. Use masking tape to mark the Power Control and Power Sequence cables with their respective plug numbers (i.e., J1, J2, J3, and J4), then disconnect the cables from the Power/Control Assembly.

4. Slide the drive out of the rack until it locks in the extended position.

5. Remove the top and bottom covers (Paragraph 4.4).

6. Remove the MASSBUS cable clamps from the bottom of the Power/Control Assembly.

7. Use the access area in the side panels of the drive and remove the Mate-N-Lok connectors from the blower motor (P6), the drive motor (P7), and the logic power (P2) as shown in Figure 4-6.

8. Slide the drive back into the rack and remove the six screws that secure the Power/Control Assembly to the rear panel.

9. Pull the Power/Control Assembly straight out from the rear panel.

CAUTION
This assembly weighs 25 pounds.

Replacement – Proceed as follows:

1. Slide the Power/Control Assembly into the drive and secure it with the previously removed hardware (Figure 4-5).

2. Use the access area in the side panels of the drive to reconnect the Mate-N-Lok connectors to the blower motor (P6), the drive motor (P7), and the logic power (P2) as shown in Figure 4-6.

3. Connect the Power Control and Power Sequence cables (as previously marked) to the Power/Control Assembly.

4. Slide the logic rack out of the drive until it locks in the extended position, then clamp the MASSBUS cables to the bottom of the Power/Control Assembly.

5. Ensure that mode switch SW1 is OFF and the main circuit breaker is OFF, then apply power to the drive as follows:

   a. Plug the ac line cord into the unswitched ac.

   b. Set mode switch SW1 to LOCAL

   c. Set the main circuit breaker to ON.

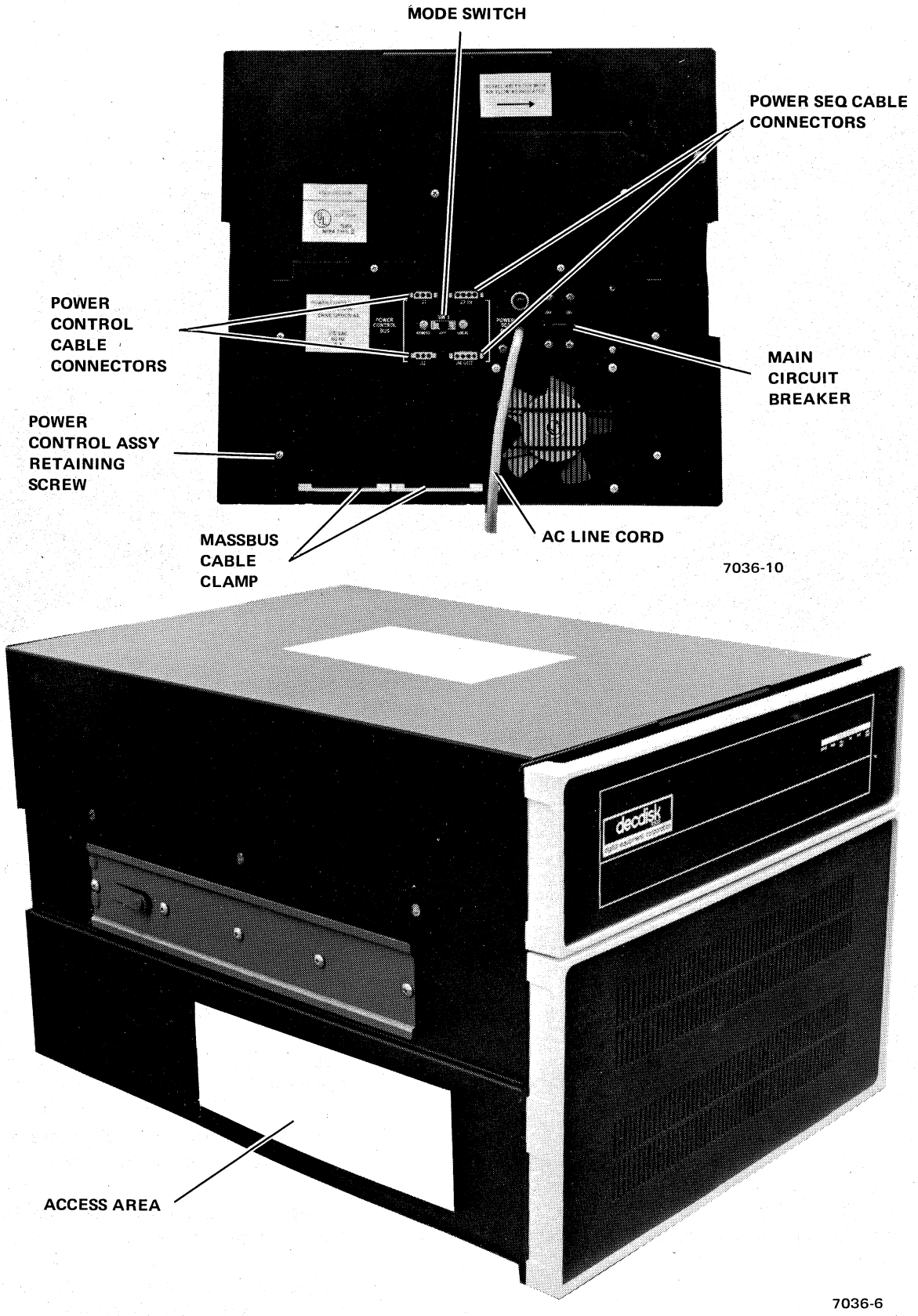

Figure 4-5 Power/Control Assembly Removal and Replacement

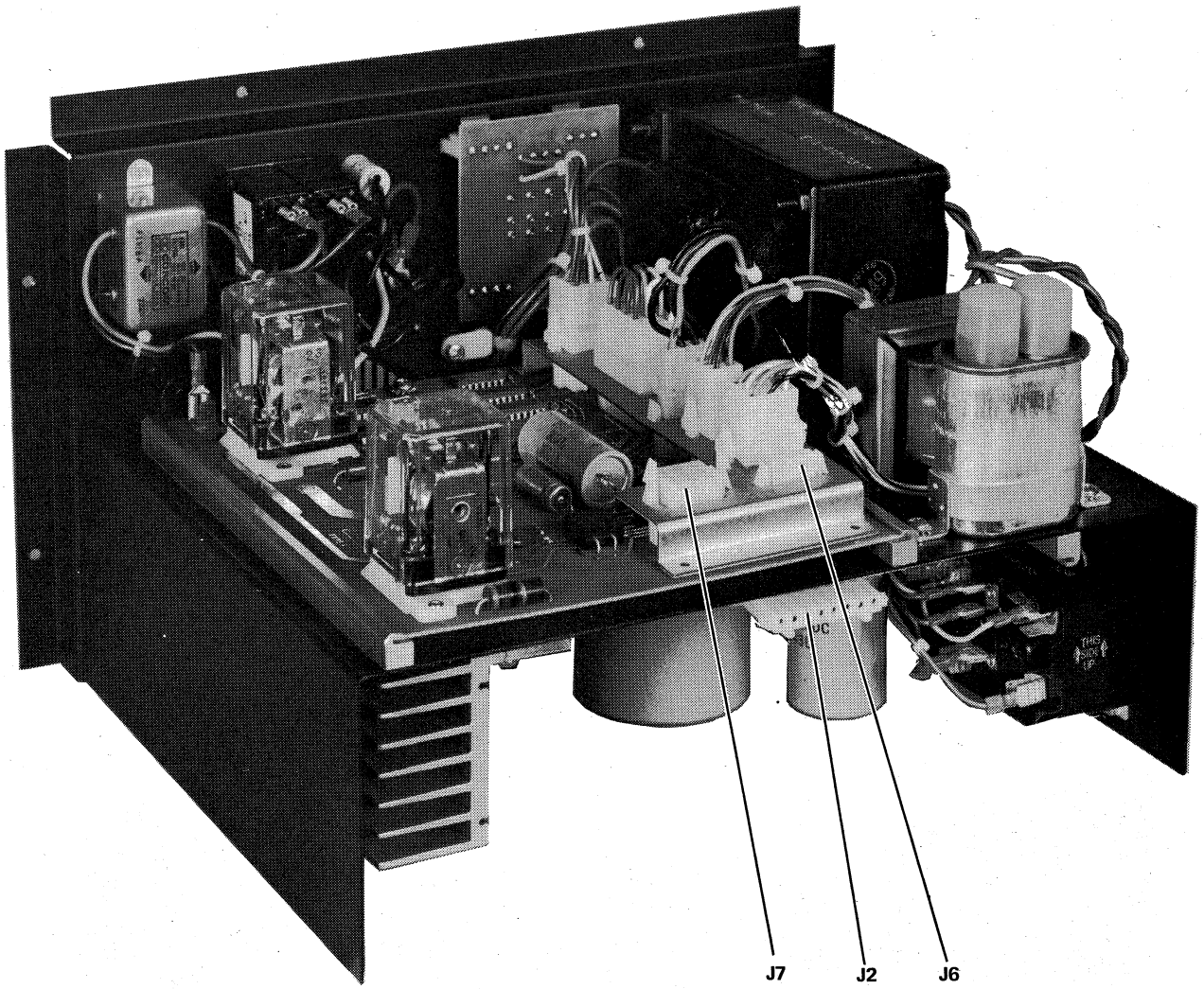

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Figure 4-6 Power/Control Assembly Connectors

NOTE

A dull rattle may be heard when power is first applied. This is caused by the initial start-up of the disk motor and is not cause for alarm (allow 30 seconds for the disk to come up to speed).

6. If the Power/Control Assembly operates satisfactorily, set SW1 to REMOTE, slide the drive out of the rack, and replace the top and bottom covers.

7. Slide the drive into the rack.

4.6 FAN

Removal – Proceed as follows:

1. Remove the Power/Control Assembly per Paragraph 4.5.

2. Unplug the female fan cable connector from the top-right portion of the fan (Figure 4-7).

3. Unscrew the transformer cable clamp from the top-right corner of the fan.

4. Remove the four 8-32 screws that secure the fan to the Power/Control Assembly and remove the fan.

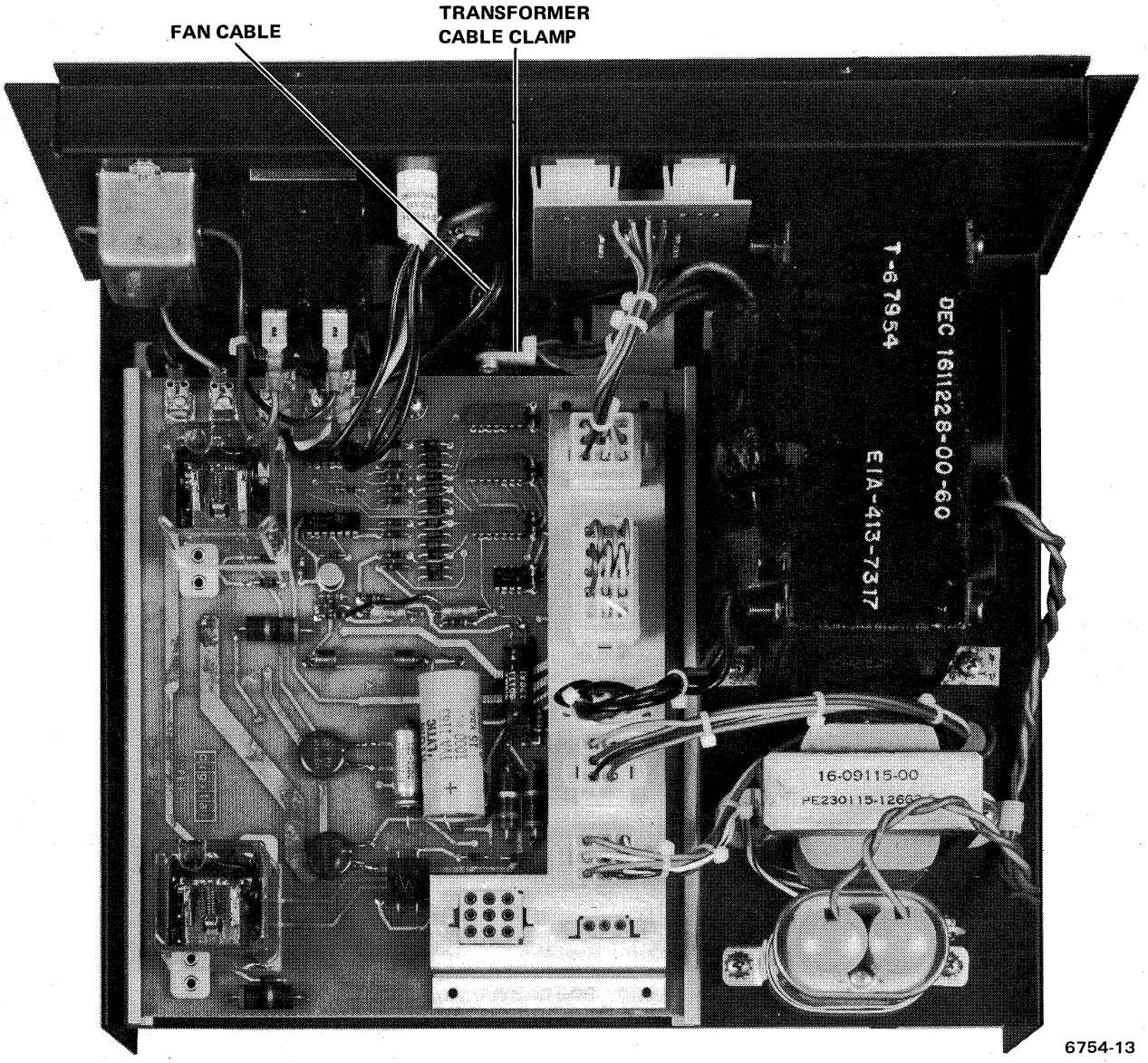

Figure 4-7 Fan Cable Removal

Replacement – Proceed as follows:

1. Insert the new fan in the Power/Control Assembly, ensuring that the label on the fan hub is inward, toward the center of the drive, and that the airflow arrow on the fan bottom points outward.

2. Attach the fan with the previously removed hardware and reconnect the fan cable connector.

3. Attach the transformer cable clamp to the top-right corner of the fan and replace the Power/Control Assembly per Paragraph 4.5.

4.7 BLOWER ASSEMBLY

Removal – Proceed as follows:

1. Remove the blower pre-filter (Paragraph 4.2) and the Power/Control Assembly (Paragraph 4.5) to gain access to the blower lower mounting screws.

2. Disconnect the blower motor leads from the starting capacitor as shown in Figure 4-8.

3. Remove the four screws attaching the motor to the lower head casting and remove the motor.

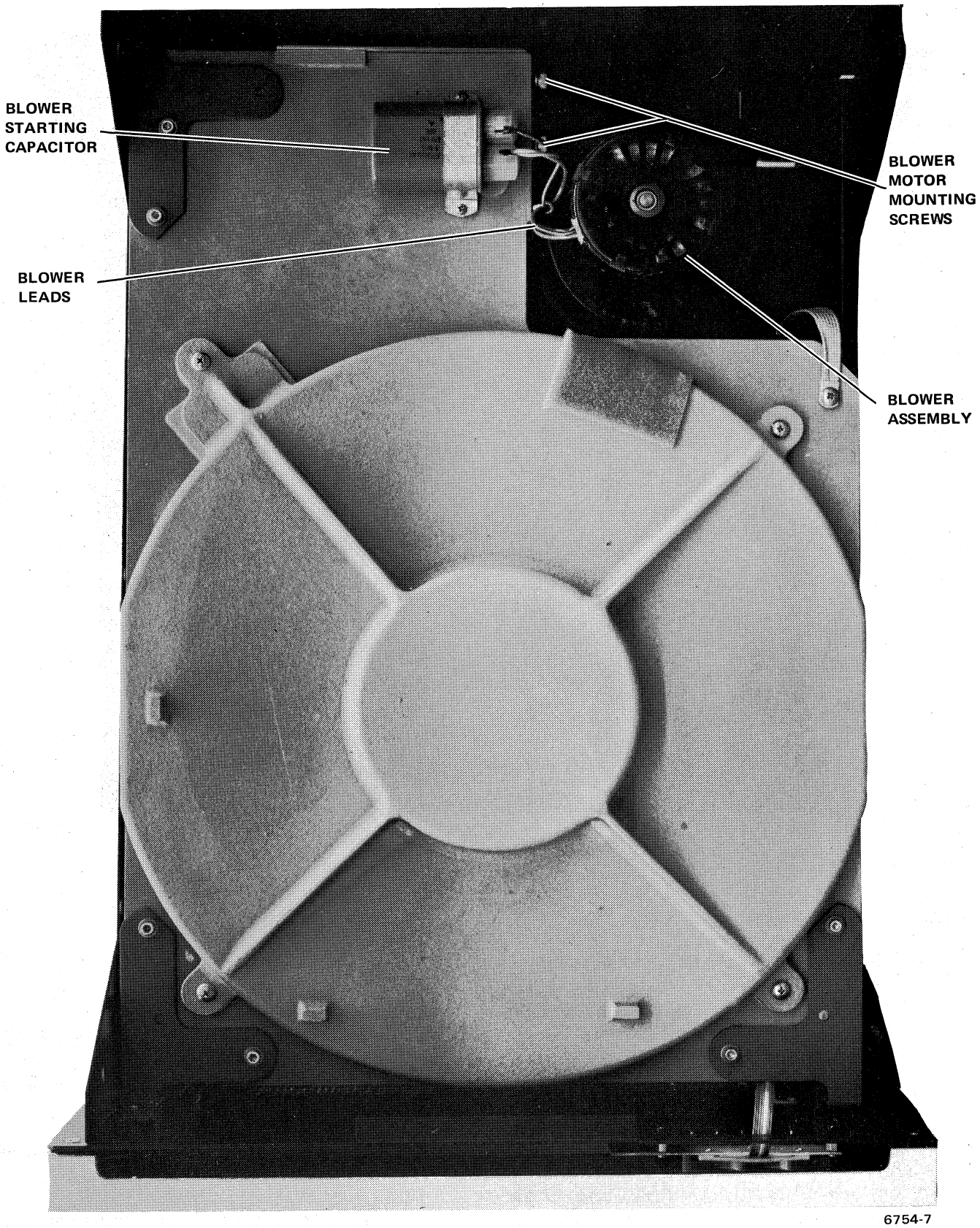

Figure 4-8 Blower Motor Removal and Replacement

Replacement – Proceed as follows:

1. Position the blower assembly on the lower head casting and secure it with the previously removed hardware (Figure 4-8).

2. Connect the motor leads to the starting capacitor and reinstall the Power/Control Assembly per Paragraph 4.5. Reinstall the blower pre-filter per Paragraph 4.2.

3. Apply power to the drive as follows:

   a. Plug the ac line cord into the unswitched ac.

   b. Set mode switch SW1 to LOCAL.

   c. Set the main circuit breaker to ON.

   NOTE

   A dull rattle may be heard when power is first applied. This is caused by the initial start-up of the disk motor and is not cause for alarm.

4. If the blower operates satisfactorily, set SW1 to REMOTE and replace the top and bottom covers.

5. Slide the drive into the rack.

4.8 READ/WRITE HEADS

Removal

CAUTION

Do not replace heads unless it has been determined as described in subsection 3.2.3 that it is necessary.

Proceed as follows:

1. Stop the drive motor and remove power from the drive by setting mode switch SW1 (Figure 4-9) to OFF and tripping the main circuit breaker. The drive motor should stop within 5 minutes.

2. Slide the drive out of the rack until it locks in the extended position.

3. Remove the bottom cover.

4. Remove the front bezel panel and extend the logic assembly to gain access to the head connectors.

5. Unscrew the captive knurled thumbscrew on the cable connector of the defective read/write head (Figure 4-10) and unplug the cable.

6. Remove the two mounting screws that attach the head block to the casting (Figure 4-11).

7. Insert a knurled thumbscrew (from the Support Kit) into the head block and carefully pull on the knurled thumbscrew *just enough to free the block from the dowel pins*, but not enough to remove it from the casting.

   CAUTION

   Do not damage or remove head block shims from the casting during this process.

8. When the head block is free of the dowel pins, slide the block in place toward the diamond-shaped pin, then lift the entire block assembly out of the casting.

Inspection – None

Cleaning

CAUTION

DO NOT USE MS200 SPRAY CLEANER. Do not spray *any* cleaner on or near the head block mounting surface on the casting, this may contaminate the disk surface.

The following equipment is required for this procedure:

One pack of 6 in. cotton-tipped applicators
One 16 oz can of MS 180 (Freon TF)
One 16 oz can of dry air

NOTE

When cleaning heads in conjunction with the disk removal procedure in Paragraph 4.9, it is not necessary to remove the heads from the casting to perform the following procedure.

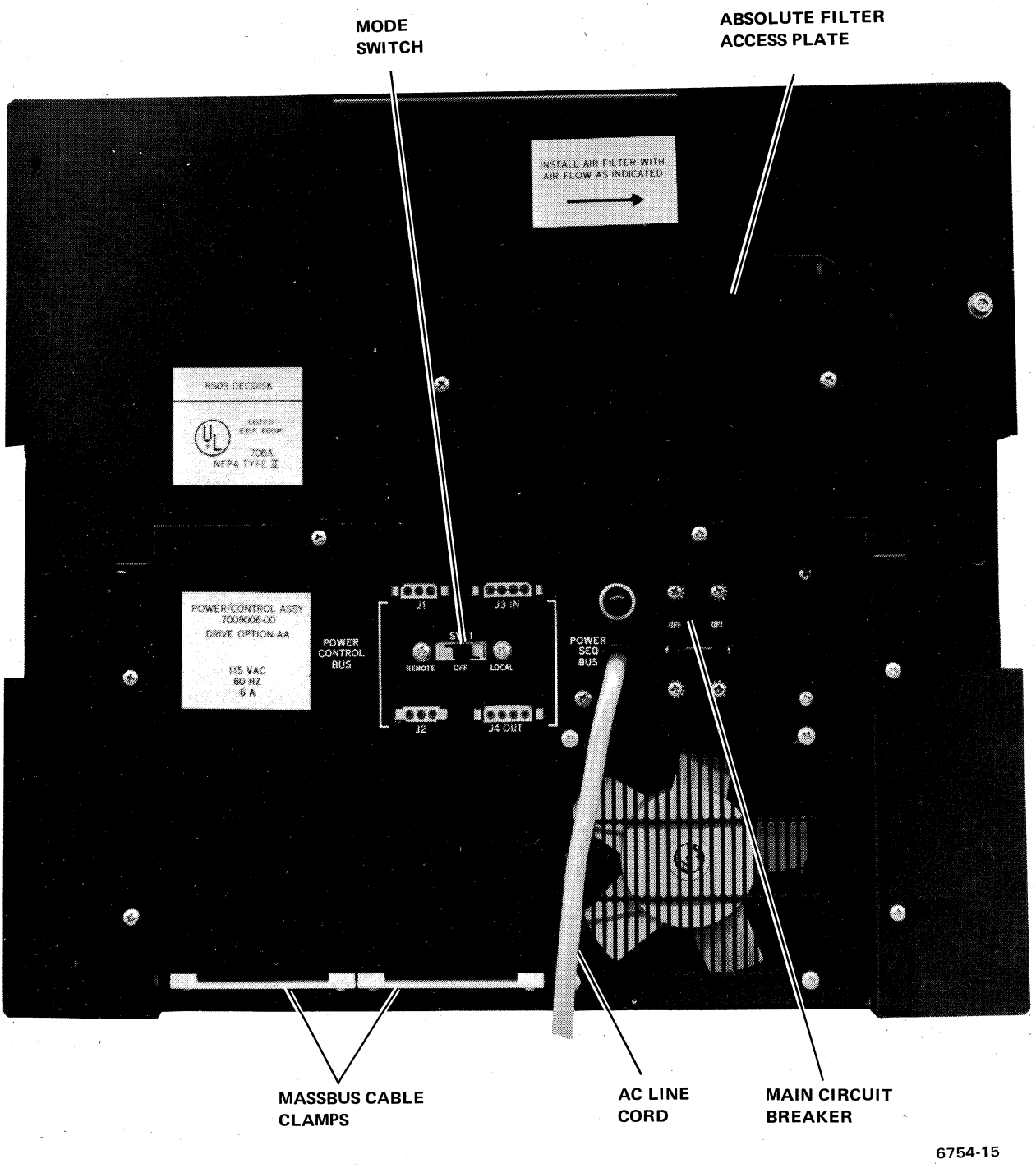

Figure 4-9 RS03 Rear Panel

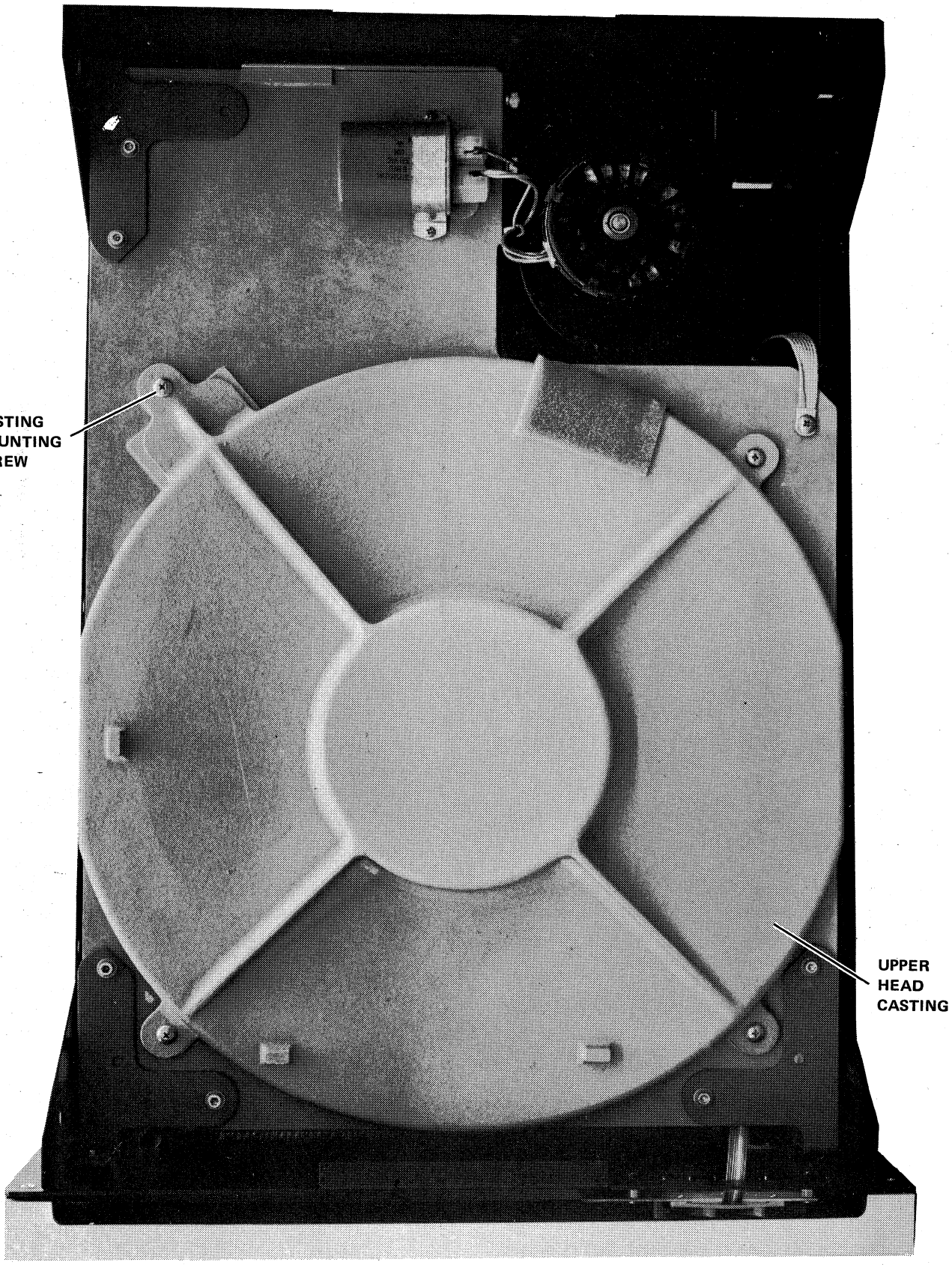

Figure 4-10 Disk Cover Casting Removal and Replacement

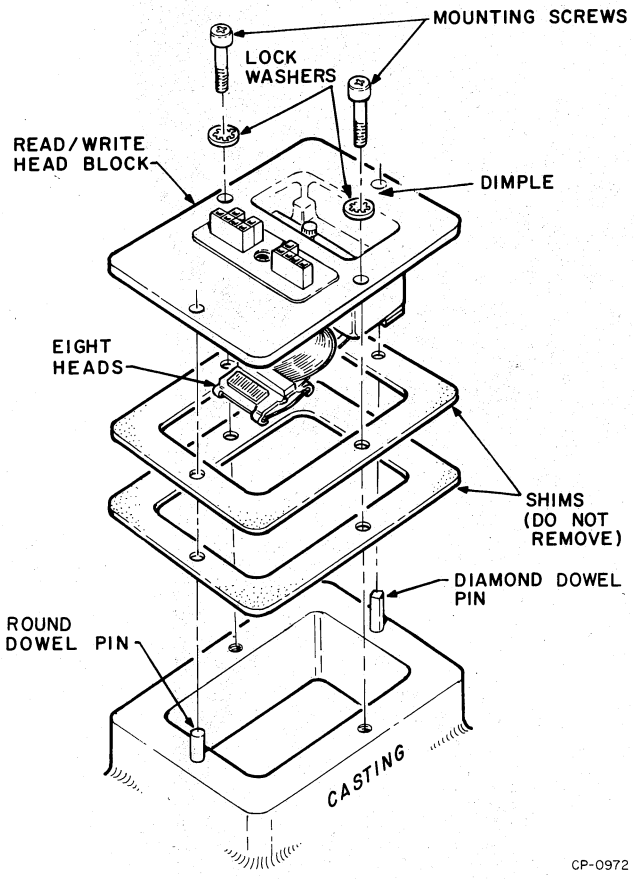

Figure 4-11 Head Block Removal

Proceed as follows:

1. Hold the head block assembly by the front flange of the head block.

2. Hold the can of MS 180 4 to 6 inches away from the assembly, and direct the spray to completely flood the slider and core assembly. Spray for about five seconds.

3. Immediately dry the assembly by using the can of dry air in the same manner.

NOTE

If the air bearing shows any sign of debris or contamination, proceed to step 4; otherwise the procedure is complete.

4. Hold the head block assembly (Figure 4-12) by grasping the side flange of the head block between the second and third fingers of one hand. The assembly should be cupped in the palm of the hand with the air bearing facing up.

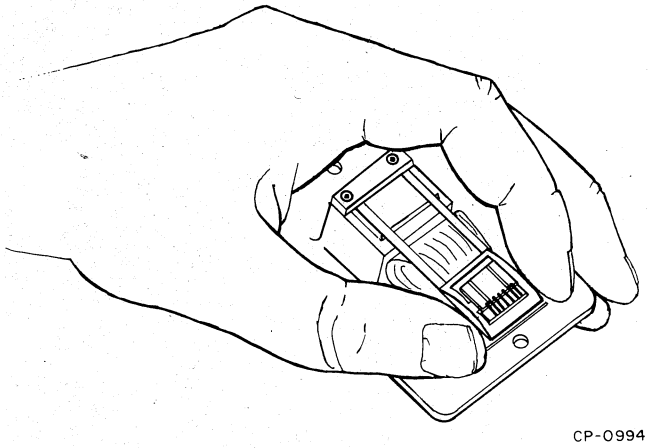

Figure 4-12 Proper Head Holding During Cleaning

5. Close the first finger and thumb of the same hand (pincer fashion) to lightly grip both edges of the gimbal and bracket. Maximum support can now be given to the gimbal to prevent distortion during the following steps.

CAUTION

When performing the following steps while the heads are in the casting, always support the gimbal and bracket with first finger and thumb as shown in Figure 4-12.

6. Spray the cotton tip of an applicator with Freon TF; shake off excess.

7. Lightly scrub the center surfaces of the air bearing (white upper surface) in the direction of the leading and trailing edges. Avoid the slider corners.

8. With a wiping action, scrub the air bearing, adjacent to the leading and trailing edges, from the slider center toward the leading or trailing edge.

9. Scrub the leading edge with the same wiping action, starting in the center and wiping laterally toward each corner.

10. Repeat steps 6 through 9 until the contamination is no longer removed from the slider.

11. To conclude the operation, repeat steps 1, 2, and 3.

Replacement (Figure 4-13) – Proceed as follows:

1. Locate a read/write head block assembly (12-11203) in the Support Kit. Two head block assemblies are supplied with the kit.

2. From the Support Kit, insert a knurled thumbscrew (74-10762) into the mounting hole and *finger*-tighten.

3. Before inserting the new head block in the casting, ensure that the block is positioned so that the dimpled hole is over the diamond dowel side of the casting and that the head block is toward the diamond dowel pin as far as possible. This ensures that the head pad does not scrape against the opposite side of the casting during insertion. The dimpled hole ensures that the head block assembly cannot be installed backward.

4. Once the block is resting on top of the dowel pins, slide it over the pins and press it down firmly on the casting, using *finger pressure* near the dowel holes.

5. Replace the two head block mounting screws and tighten them to a torque of 10 in/lb ± 1/2 in/lb.

6. Remove the knurled thumbscrew from the head block and replace the head cable connector. *Finger-tighten* the knurled thumbscrew on the connector.

7. Restore the drive to its operational configuration and apply power as follows:

   a. Set mode switch SW1 to LOCAL
   b. Set the main circuit breaker to ON.

NOTE

A dull rattle may be heard when power is first applied. This is caused by the initial start-up of the disk motor and is not cause for alarm.

8. Exercise the drive to ensure that the replacement head block operates correctly.

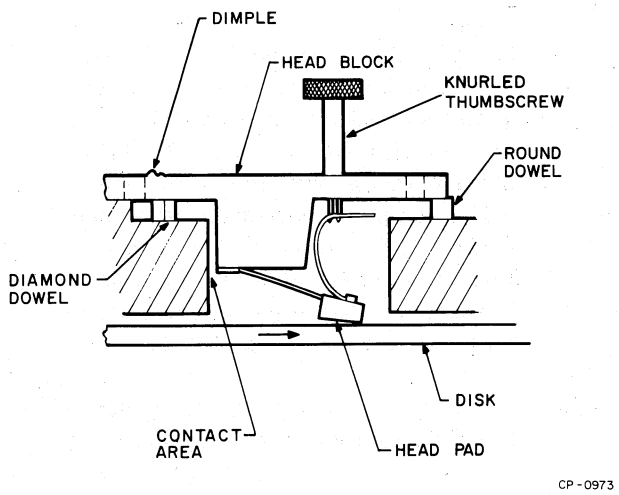

Figure 4-13 Head Block Insertion

CAUTION

Once a replacement head block assembly has been installed, verify correct operation of *all* tracks. It is possible that the replacement head block assembly may have become misaligned, which could produce errors on those tracks with which its ferrites are interleaved. Refer to Figure 2-25 for the locations and interleaving of tracks. Two examples illustrate what may happen.

Example 1:

Data errors were occurring on tracks 22_8 and 23_8 on the bottom surface, so the No. 20 head block assembly was replaced. To verify the replacement, data was written on all tracks in sequence, 00_8–77_8. When read back, data errors occurred on tracks 20_8–27_8. Because the replacement head block assembly was misaligned, its ferrites did not interleave properly with the No. 40 head block assembly. Since tracks 40_8–47_8 were written after 20_8–27_8, the data on tracks 20_8–27_8 was destroyed.

To verify this problem, next write only on tracks 40_8–47_8 and then write on tracks 20_8–27_8. If tracks 40_8–47_8 cannot now be read back, the replacement head block assembly was misaligned and must be replaced.

Example 2:
In this example, head block assembly No. 40 was replaced. When writing and then reading all tracks in sequence (00_8–77_8) data errors occur on tracks 20_8–27_8, which previously were not making errors and at first glance were in no way related to the replacement head block assembly. Verification of the problem is the same as in Example 1, and again the replacement head block assembly must be replaced.

9. If the heads operate satisfactorily, set SW1 to REMOTE and slide the drive into the rack.

4.9 DISK

A disk should be replaced if it has been determined necessary as described in subsection 3.2.3. In addition, any disk which shows copper-colored circular score marks should be replaced.

If the disk sticks to the heads and impairs starting, a thorough cleaning of both the disk and heads is needed.

An accumulation of dirt, usually most prominent on the leading edge of the alumina slider, necessitates a thorough cleaning of the disk and heads.

Any sticking, excessive dirt, or scoring of the disk indicates that the air filtering system may be faulty. In this case, the filters must be changed as in Paragraph 4.2.

Disk Cover Casting Removal (Figure 4-14) – To perform this procedure, a clean tabletop work area is required. Care and cleanliness are of the utmost importance in this procedure. To remove the disk cover casting, proceed as follows:

1. Stop the drive motor and remove all power from the drive by setting mode switch SW1 (Figure 4-9) to OFF and tripping the main circuit breaker. The drive should stop within 5 minutes.

2. Unplug the ac line cord from the unswitched ac. DO NOT REMOVE THE POWER CONTROL OR POWER SEQUENCE CABLES FROM THE REAR OF THE POWER/CONTROL ASSEMBLY.

3. Slide the drive out of the rack until it locks in the extended position.

4. Remove the top and bottom covers (Paragraph 4.4).

5. Reverse the motor grounding brush and tighten the motor lock to prevent the disk from rotating in the wrong direction during removal.

6. Remove the four mounting screws from the disk cover casting and lift the casting out of the drive.

Disk Removal and Cleaning

CAUTION
It is extremely important to follow this procedure to the letter. Deviation can cause disastrous consequences in the operation of the drive system.

Secure the following materials prior to performing this procedure. They are contained in the Disk Cleaning Kit.

1 bottle Chevron 325
1 bottle DCB lubricant
20 Kaydry disposable towels (15 X 16-7/8)
1 pair plastic gloves
2 medicine droppers

Proceed as follows:

1. Prepare two work areas, using four overlapping Kaydrys in each area. *Put on gloves.*

2. Remove the 4 screws on the mounting cap and remove the cap or Belleville Washer.

CAUTION
Observe and record the orientation of the lettering on the edge of the disk. The disk must be replaced in the same orientation, since only one surface is usable.

3. Pick up the disk, and using a Kaydry, wet with Chevron 325, swab the edge of the disk around the entire disk periphery. Dry with a fresh Kaydry.

4. Place the disk on the work area with the top face up.

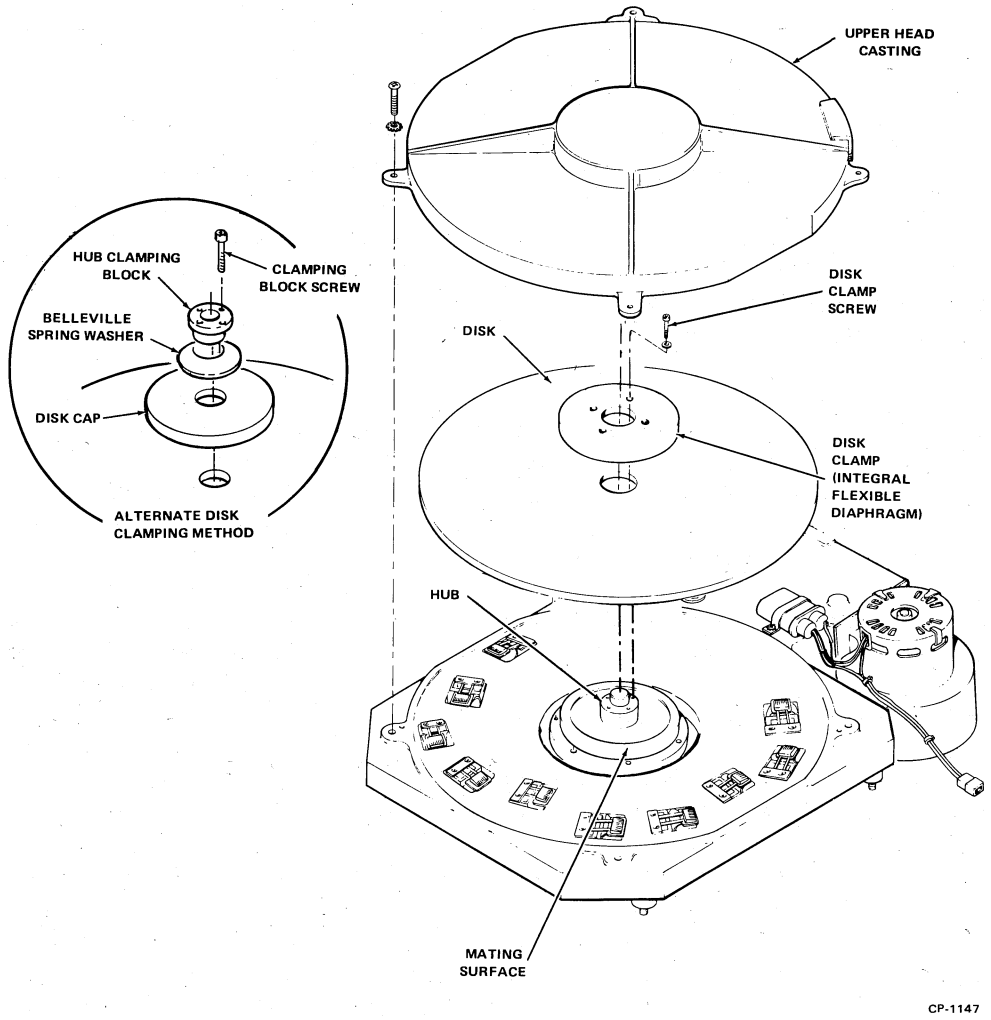

Figure 4-14 Disk Cover Casting and Recording Disk Removal and Replacement

5. Fold additional Kaydry towels into buffing pads by folding towels in half three times.

6. Apply a full dropper (1 ml) of Chevron 325 solvent to the disk at each of four locations, at a 6-inch radius, spaced 90 degrees apart, and buff to a haze-free surface.

7. Repeat Step 6 twice so that the disk surface has been cleaned three times with Chevron 325.

8. Apply a full dropper of DCB lubricant to four areas of the disk, at a 6 inch radius, spaced 90 degrees apart.

9. Using a folded Kaydry buffing pad, immediately wipe the disk lightly to distribute the cleaner over the entire disk surface.

10. Turn over the pad and buff until strong fringe patterns are observed over the entire disk surface, then let air dry.

11. Using a new buffing pad, buff entire surface.

12. Turn the disk over and move to second Kaydry work area.

13. Repeat steps 6 and 7.

14. Repeat steps 8, 9, and 10.

15. Clean the lower heads per Paragraph 4.8.

16. Mount the disk in the drive in its original orientation and replace the collar or Belleville Washer and screws.

NOTE

Tighten screws alternately and diagonally in several steps and torque to 16 in/lb ± 1/2 in/lb.

17. Using a clean Kaydry towel, buff the top disk surface to remove any lint, prior to installing the disk cover casting.

Disk Cover Casting Replacement – Proceed as follows:

1. Ensure that the mating surfaces of the disk cover and lower head castings are clean.

2. Position the disk cover over the lower casting.

3. Replace the four mounting screws in the disk cover casting and secure to the lower head casting.

4. Remove the motor lock and reverse. Make sure that *both* grounding brushes contact the motor spindle.

5. Apply power to the drive as follows:

   a. Plug the ac line cord into the unswitched ac.

   b. Set mode switch SW1 to LOCAL.

   c. Set the main circuit breaker to ON.

   d. Wait 30 seconds for disk to come up to speed.

6. Rewrite both timing tracks following the procedure in Appendix F.

7. If the drive operates satisfactorily, set SW1 to REMOTE and replace the top and bottom covers.

8. Slide the drive into the rack.

Confirmation – Once the head/disk assembly is reassembled, run the diagnostic to confirm that the problem has been corrected.

4.10 DISK DRIVE MOTOR

To perform the following procedure, the disk support kit, the disk cleaning kit, and a clean tabletop work area are required. The disk drive motor is a precision piece of equipment, handle it with care.

Drive Motor Removal – Proceed as follows:

1. Remove the recording disk from the drive (Paragraph 4.9).

2. Remove the front bezel panel (Figure 4-1) and extend the logic assembly.

3. Use the access area in the side panels of the drive (Figure 4-16) to disconnect the drive motor Mate-N-Lok connector (P7) from the top of the Power/Control Assembly (Figure 4-6).

4. Remove the grounding bracket on the bottom of the motor shaft (Figure 4-15) and retain for reinstallation. Note the way this bracket is mounted so that it can be reinstalled in the same way on the new motor.

5. Remove the four drive motor mounting screws from beneath the lower head casting (Figure 4-16), then lift the motor up through the bottom casting.

6. Place the old motor in a shipping carton; replace the red protective cap and prepare it for return to DEC.

NOTE

Drive motors should be stored in their shipping cartons at all times.

Drive Motor Replacement – This replacement should be done carefully and slowly. Proceed as follows:

1. Locate the new motor assembly (74-09804) and remove the red protective plastic cap from around the spindle hub. Ensure that all mating machined surfaces on the motor and casting are clean and free of burrs.

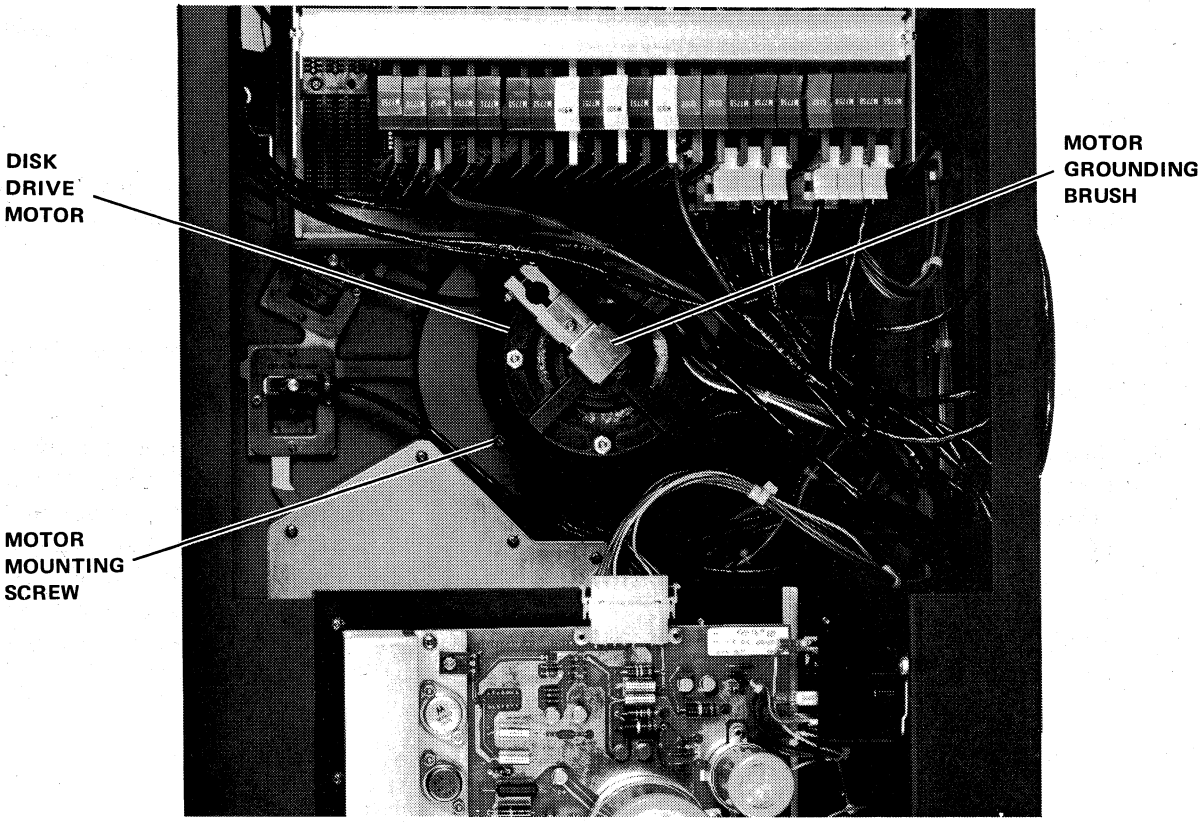

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Figure 4-15 Disk Drive Motor Bottom View

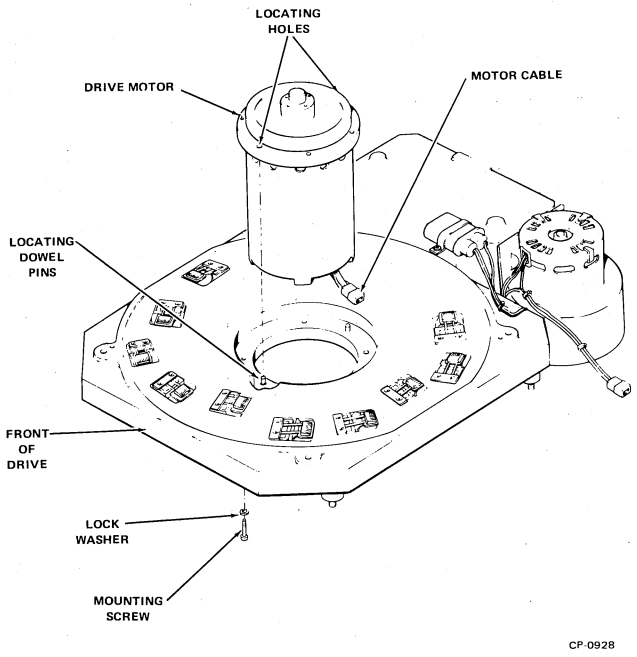


Figure 4-16 Disk Drive Motor Removal and Replacement

2. Insert the new motor, with the motor cable positioned toward the rear of the drive (toward the blower motor), through the lower casting (Figure 4-16).

CAUTION

Ensure when inserting the motor that no nicks are put in the flanges in the process.

3. Align the two dowel holes in the motor with the dowel pins in the casting and firmly seat the motor in the casting.

4. Replace the four motor mounting screws beneath the lower casting and moderately tighten them. DO NOT USE EXCESSIVE FORCE.

5. Replace the grounding brush bracket on the bottom of the motor (Figure 4-15) in the same way that it was mounted on the old motor.

6. Use the access area in the side panels of the drive (Figure 4-16) to reconnect the drive motor Mate-N-Lok connector (P7).

7. Clean and reinstall the recording disk on the drive hub and the disk cover casting per Paragraph 4.9.

8. Reinstall the chassis covers per Paragraph 4.4.

9. Set the main circuit breaker to ON. Set SW1 to REMOTE. A dull rattle may be heard when power is first applied. This is caused by the initial start-up of the disk motor and is not cause for alarm. However, if the start-up noise is accompanied by a screeching sound, remove power to the drive immediately and inspect the disk surface and the heads.

SECTION 5
INSTALLATION

5.1 GENERAL

This section contains instructions pertaining to the installation of the RS03 DECdisk. The drive can be shipped in a rack as an integral part of a system, or it can be shipped in a separate container. If the drive is shipped in a separate container, refer to Paragraph 5.2; if the drive is shipped already installed in a rack, locate the rack in its permanent location and proceed to Paragraph 5.3.

5.2 DRIVE SHIPPED SEPARATELY

If the drive is not shipped as part of a system, proceed as follows:

1. Move the carton close to the point where the drive is to be installed. Unpack and retain all packaging materials for possible return shipment. Inspect the drive for damage and report any damage to the local Field Service Representative.

   CAUTION
   Use care in unpacking the drive. This unit is heavy. DO NOT DROP.

2. If the drive is to be installed in an existing rack, install the chassis slides in the rack as shown in Figure 5-1. Install clip-in nuts (DEC part no. 9007786) in the holes noted. If further information is required, refer to RS04 Option Configuration Drawing No. D-OC-RS04-0-4 for detailed specifications of a multiple-drive installation.

3. If the drive is to be mounted in a rack without sufficient weight to prevent tipping when the drive is fully extended, install cabinet stabilizers before mounting the drive.

   CAUTION
   Before extending the drive on its slides, ensure that the cabinet stabilizer levelers are touching the floor, or that weights are installed in the rear of the cabinet.

4. Pull the chassis slides out until they lock in the extended position.

5. Slide the drive into the chassis slides until it locks.

6. Proceed to Paragraph 5.3 for the balance of the installation.

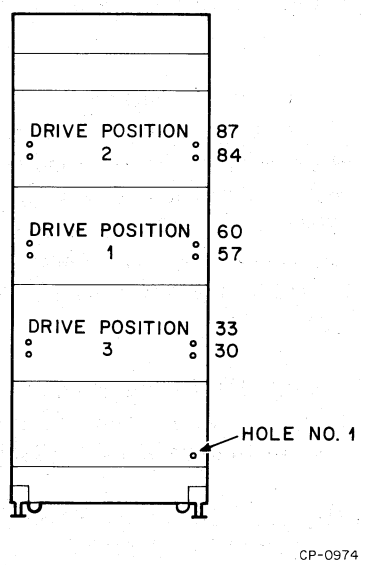


Figure 5-1 Chassis Slide Mounting Hole Locations

5.3 DRIVE MOUNTED IN A RACK

When the drive is mounted in a rack, proceed as follows:

CAUTION

Before extending the drive on its slides, ensure that the cabinet stabilizer levelers are touching the floor, or that weights are installed in the rear of cabinet.

1. Remove the two screws from the slide locking plate, one on each side, from the rear of the drive. Push the drive out approximately six inches.

2. Pull the drive out from the front until the slides lock.

3. Remove the control panel and inlet filter cover from the latch moldings on the front of drive.

4. Remove the top and bottom covers, which are identical.

5. Loosen the logic rack locking thumbscrews and extend the logic rack on its slides until the slides lock.

6. Remove the M5903 modules from slots AB04, 05, and 06 and attach the preconfigured MASSBUS cable as shown in Figures 5-2 and 5-3.

NOTE

If a drive is the only or last drive on the MASSBUS, it must have either M5903s, with H870 terminators in J2, or M5903-YAs, which incorporate the terminator resistors. These must be located in slots AB04, 05 and 06 (Figure 5-3).

7. The MASSBUS cable should be installed in the drive as shown in Figure 5-3 if the drive is the only or last drive on the MASSBUS.

8. All other drives on the MASSBUS should have the "out" labelled end of the MASSBUS cable interleaved (shown in Figure 5-4) after cutting cable tie "A". Align IN and OUT MASSBUS cable ends as shown and retie the cable bundle where shown (cable tie "A") with ties provided in the accessory kit.

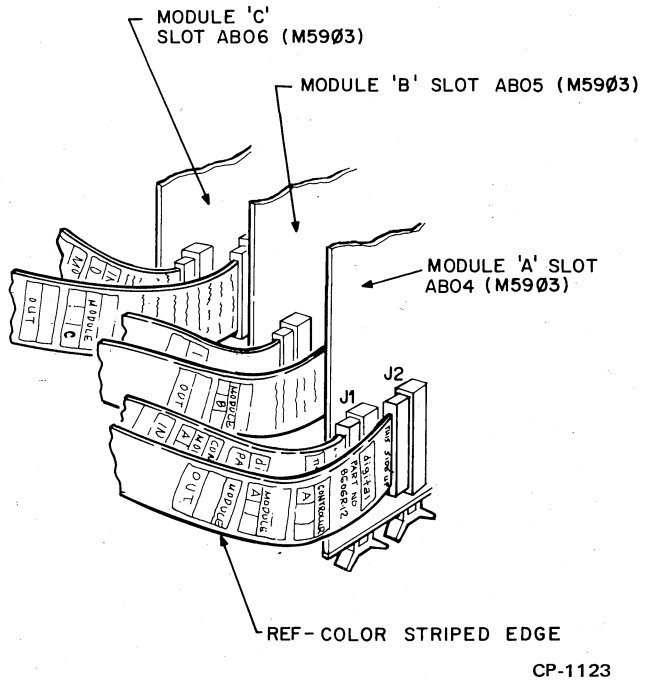


Figure 5-2 MASSBUS Cable Installation (Middle of Bus)

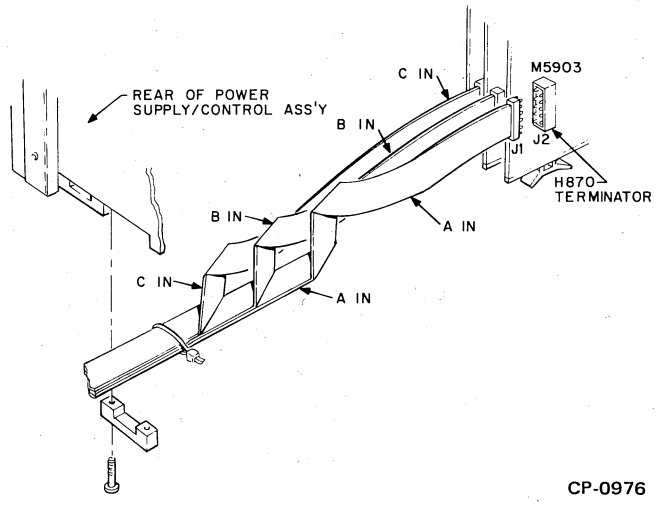


Figure 5-3 MASSBUS Cable Installation (Last or Only Drive)

9. Reassemble the M5903 modules in the logic rack as noted in Figure 5-2. When replacing cable clamps at the rear of power supply/control assembly, ensure that sufficient cable is left inside the drive so that the logic rack can be fully extended on its slides without pulling on the MASSBUS cable.

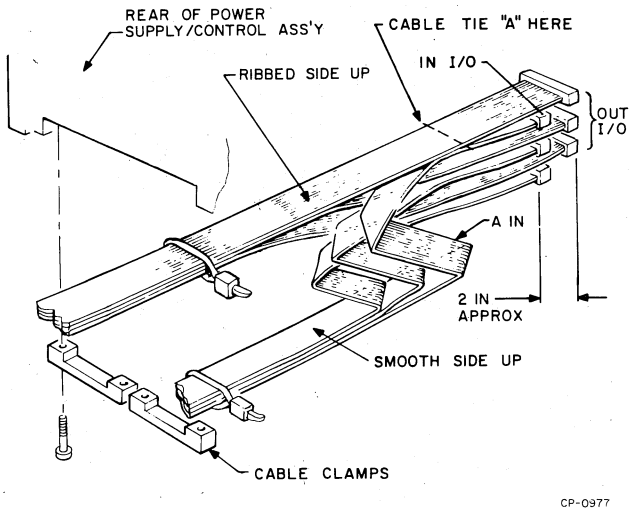


Figure 5-4 Cable Routing for Drives Located in the Middle of MASSBUS

10. Remove the shipping brackets *in the following order.*

    a. Remove the screw securing the left-rear bracket to the chassis.

    b. Remove the two screws holding the bracket to the casting.

    c. Remove the two screws securing the front-right and -left shipping brackets to the chassis.

    d. Remove the screws holding the brackets to the casting.

11. Shipping brackets should be stored as shown in Figure 5-5, using one of the shipping bracket screws. The remaining screws should be securely replaced in the casting and in the shipping brackets.

12. Remove the motor lock and reverse. (Note that the motor lock assembly contains spindle grounding brushes).

NOTE

Both grounding brushes must contact motor shaft.

13. The light panel assembly should be removed from the rear of the chassis front and re-assembled as shown in Figure 5-6.

14. Replace the top and bottom covers.

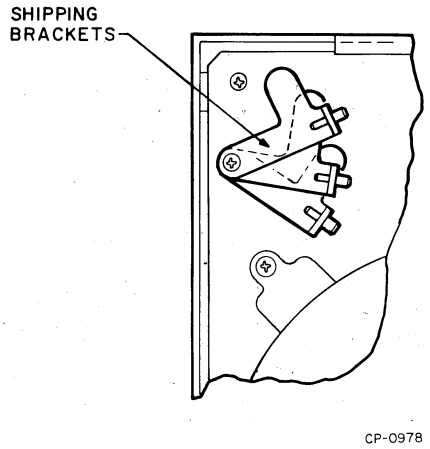


Figure 5-5 Shipping Bracket Storage Location

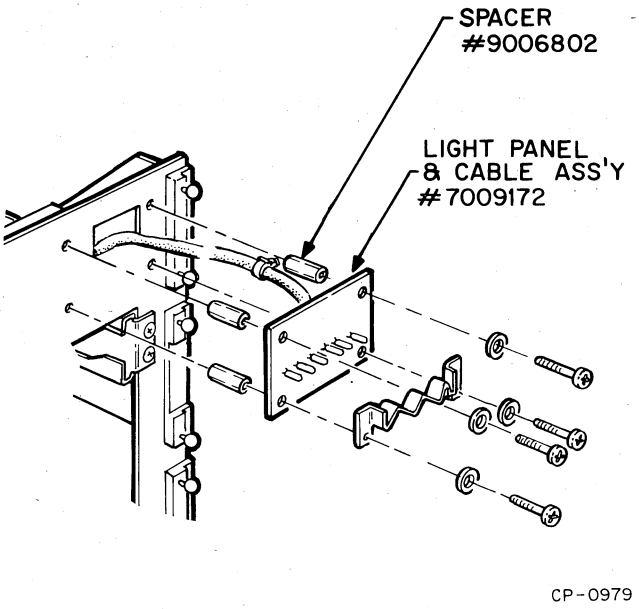


Figure 5-6 Light Panel Assembly Procedure

15. The Power Sequence Jumper (DEC part no. 7009490) should be placed in power sequence bus J3 on the rear of the power supply/control assembly on the rear of the first drive on the MASSBUS. Subsquent drives on the MASSBUS should be daisy-chained, using Power Sequence Cable Assembly (DEC part no. 7009491) between J4 of one drive and J3 of the next.

NOTE

No connection is made to J4 of the last drive on the MASSBUS.

16. The Remote Power Cable Assembly (DEC part no. 7009288-8F) should be connected to the remote power control connectors of the power controller associated with the MASSBUS controller and J1 of the power control bus on the rear of the drive. Subsequent drives on the bus should be daisy-chained, using the same type of cable between J2 of one drive and J1 of the next.

NOTE

No connection is made to J2 of the last drive on the MASSBUS.

17. Secure one end of the Ground Strap (DEC part no. 1209820) to the cabinet chassis containing the controller and the other end under the left-hand locking plate screw on the rear of the drive. Subsequent drives should be daisy-chained by securing the ends of the ground straps under the locking plate screws.

18. Set REMOTE/LOCAL switch (SW1) on power supply/control assembly to REMOTE.

NOTE

The circuit breaker for the power controller must be OFF before plugging in the drive line cord.

19. Connect the power cord to the unswitched outlet of the cabinet power controller. Cabinet fans should also be connected to the unswitched outlets.

20. Set the following switches in the disk logic:

    M7755 Module – Select switches for proper unit number (refer to subsection 3.3.3).

    M7754 Module – Select switch for write lock enable off (refer to subsection 3.3.1).

21. Check the following jumpers:

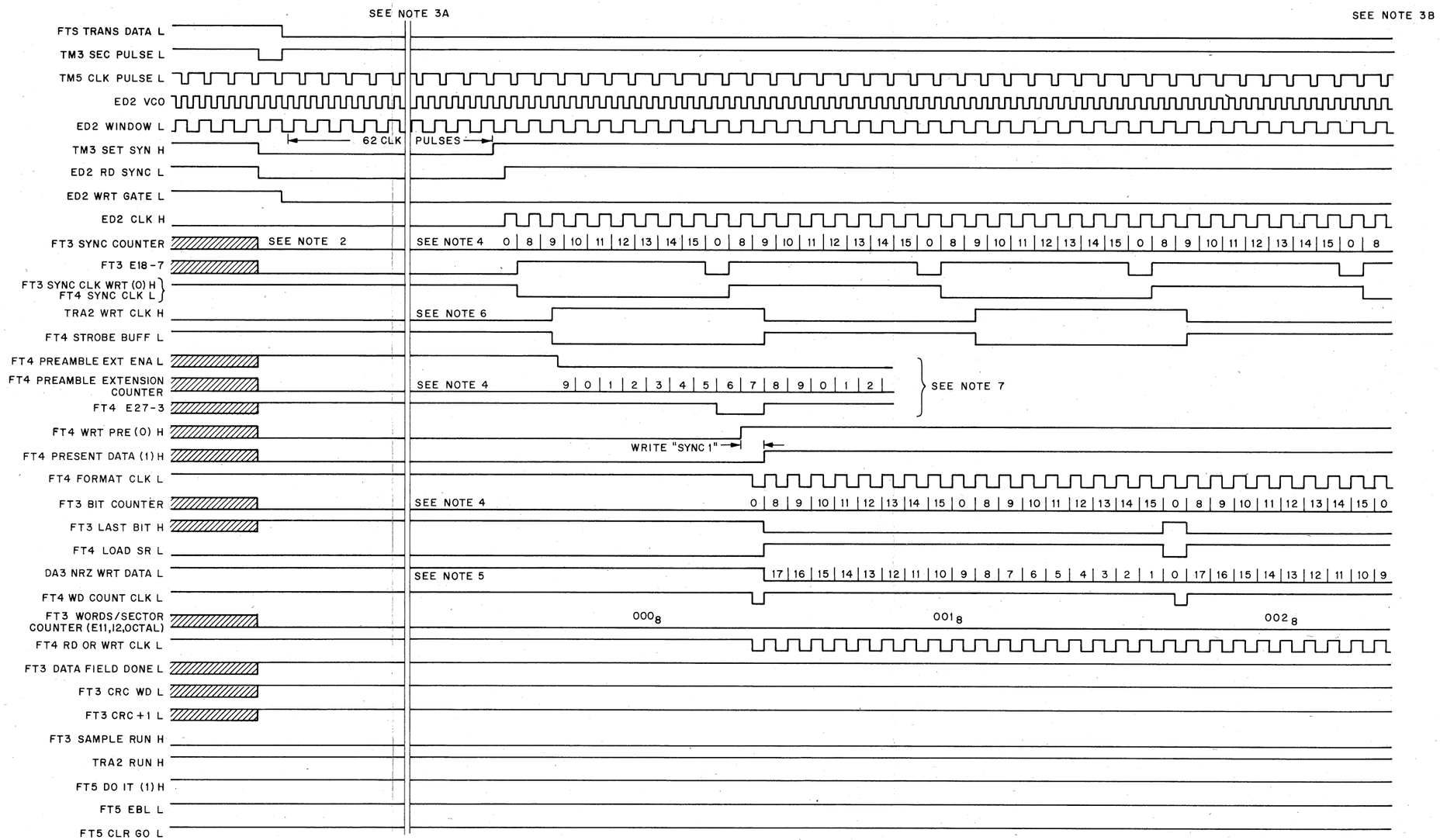
    For 4 μs/wd operation, ensure that jumper W1 on G092 is IN.

    For 8 μs/wd operation, ensure that jumper W1 on G092 is OUT.

APPENDIX A
DETAILED TIMING DIAGRAMS

A.1 GENERAL

Figures A-1 and A-2 comprise two system timing diagrams for the RS03, showing waveforms for a Write function and a Read or Write Check function, respectively.



NOTE 1:
This timing diagram assumes that the Desired Address and Control Registers have been previously loaded with an address and a Write command, respectively and that TRA2 RUN H has been asserted. It is also assumed that the Data Transfer terminates after this sector has been written.

NOTE 2:
This symbol (ZZZZZ) indicates those signals which are initialized by TM3 SEC PULSE L.

NOTE 3:
The solid vertical lines indicate time discontinuities.

NOTE 3A:
Preamble "0" 's are written during this gap. The assertion of TM3 SET SYN H indicates sufficient "0" 's have been written.

NOTE 3B:
The middle 60_{10} words in the sector are not shown for space reasons and because no timing variations occur in that interval.

NOTE 3C:
The deadband at the end of the sector is abbreviated to show those signals initialized by the next sector pulse.

NOTE 4:
The convention (|8|) is used to designate counter states. The decimal number between vertical lines correspond to the binary state of the counter.

NOTE 5:
Serial NRZ data is designated by the symbol (|15|). The decimal number between vertical lines corresponds to the bit position of that data bit in the data word.

NOTE 6:
TRA2 WRT CLK H will be asserted between 0 and 750 ns after assertion of FT4 SYNC CLK L. For this example, a typical time of 300 ns is assumed.

NOTE 7:
These signals continue throughout the balance of the sector but are of no significance once the "SYNC 1" has been written at the end of the preamble.

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Figure A-1 Write Function Timing Diagram (one sector) (Sheet 1 of 2)

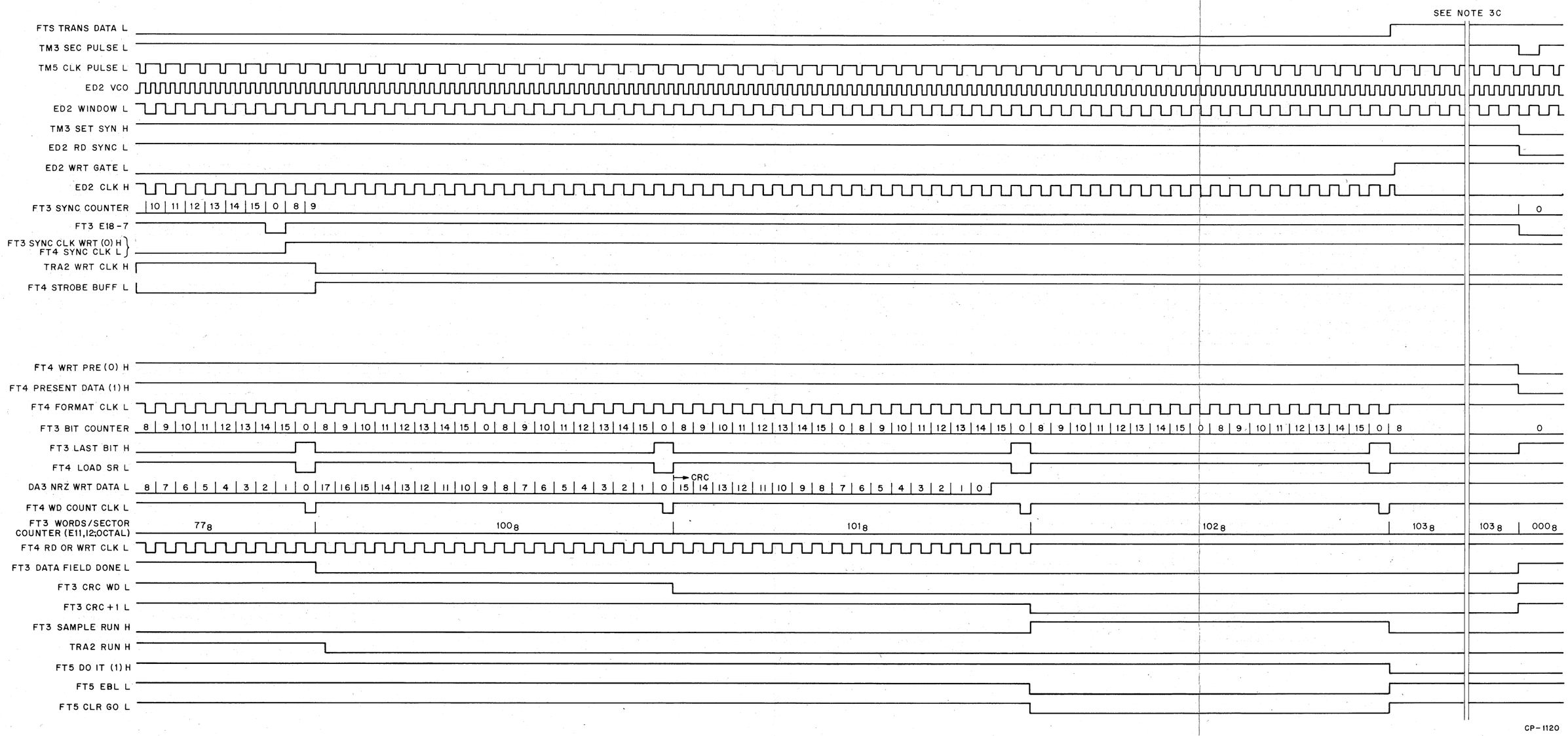
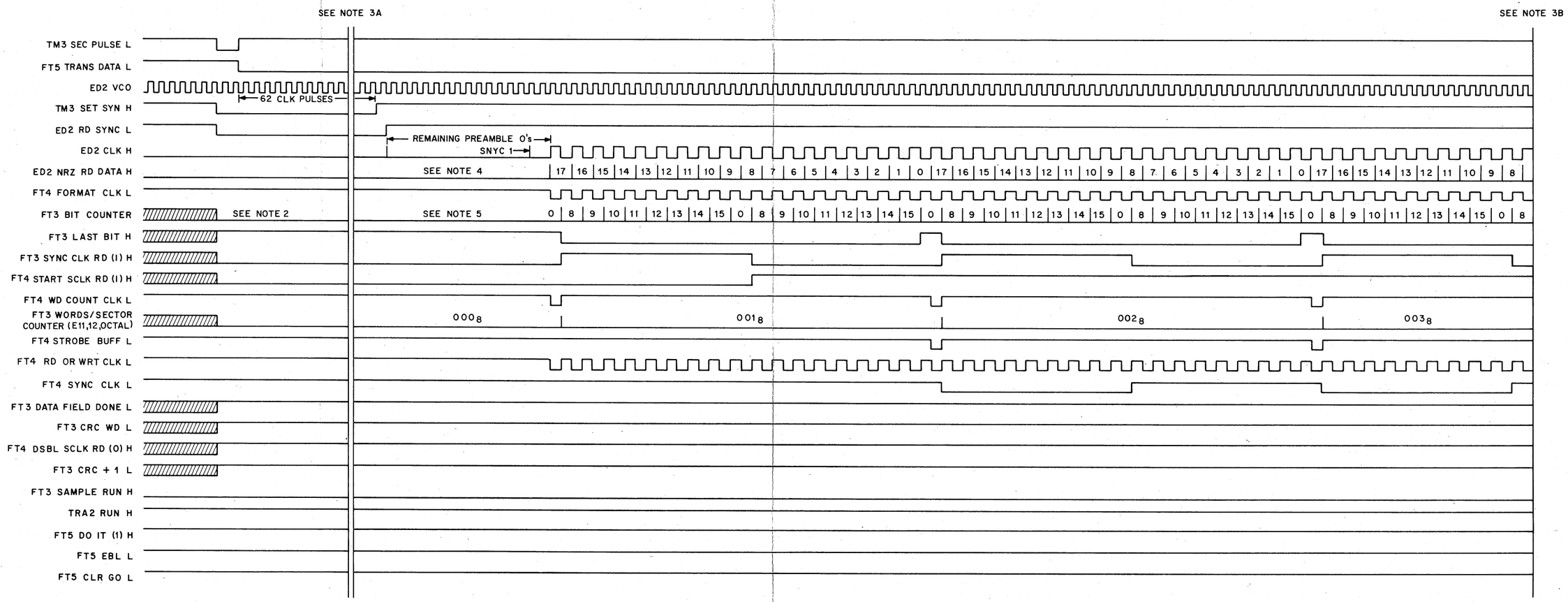


Figure A-1 Write Function Timing Diagram (one sector) (Sheet 2 of 2)



NOTE 1: This timing diagram assumes that the Desired Address and Control Registers have been previously loaded with an address and a Read (or Write Check) command, respectively and that TRA2 RUN H has been asserted. It is also assumed that the data transfer terminates after this sector has been written.

NOTE 2: This symbol (//////) indicates those signals which are initialized by TM3 SEC PULSE L.

NOTE 3: The solid vertical lines indicate time discontinuities.

3A: Preamble "0" 's are read during this interval. This allows the phase locked loop to synchronize to the readback data after having been synchronized to the timing track. The assertion of TM3 SET SYN H indicates that the phase locked loop must begin looking for the sync "1" which signifies the end of the preamble and the beginning of data.

3B: The middle 60_{10} words in the sector are not shown for space reasons and because no timing variations occur in this interval.

3C: The deadband at the end of the sector is abbreviated to show those signals initialized by the next sector pulse.

NOTE 4: Serial NRZ data is designated by the symbol (|16|). The decimal number between vertical lines corresponds to the bit position of that data bit in the data word.

NOTE 5: The convention (|7|) is used to designate counter states. The decimal number between vertical lines corresponds to the binary state of the counter.

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Figure A-2 Read or Write Check Function Timing Diagram (one sector) (Sheet 1 of 2)

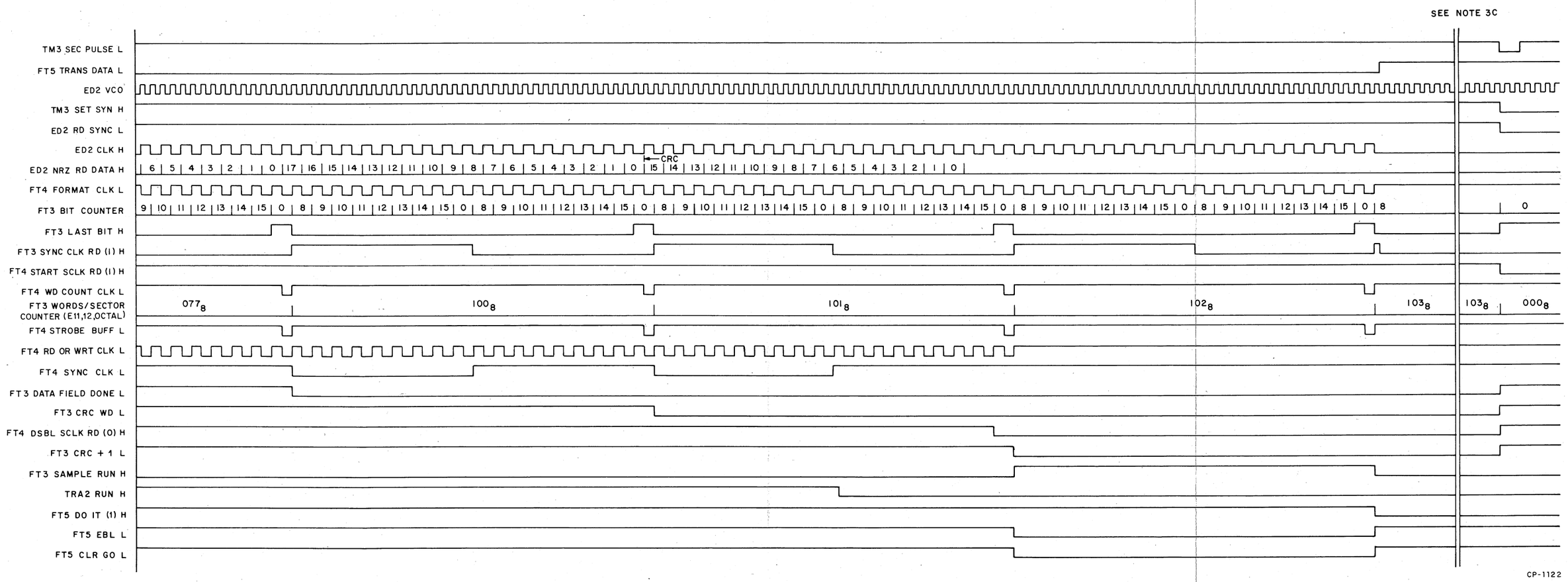


Figure A-2 Read or Write Check Function Timing Diagram (one sector) (Sheet 2 of 2)

APPENDIX B
LOGIC DICTIONARY
(Signal Glossary)

B.1 GENERAL

Table B-1 lists the basic signal mnemonics used in the RS03 and gives the literal definition for each signal. This information can be used in conjunction with the Wire List, Drawing Number K-WL-RS03-0-WL, in locating and identifying the various signals in the RS03.

Table B-1
RS03 Signal Glossary

Mnemonic	Meaning
AD2 ASYNC PAR ERR L	ASYNChronous (CONTROL) BUS PARITY ERROR
AD2 DC PAO L	DRIVE CONTROL BUS PARITY OUT
AD2 INV ADD H	INVALID ADDRESS
AD2 SEC COMP H	SECTOR COMPARE
AD2 TRK 1X H	TRACK 1X
AD2 TRK 2X H	TRACK 2X
AD2 TRK 4X H	TRACK 4X
AD2 TRK X1 H	TRACK X1
AD2 TRK X2 H	TRACK X2
AD2 TRK X4 H	TRACK X4
AD2 WO BO00 L	WIRED-OR REGISTER BUS OUT 00
AD3 LAST BLK H	LAST BLOCK (DESIRED ADDRESS REGISTER=7777_8)
AT02 SP GATE L	SPARE GATE
BW TRK PAR L	(BACKPLANE WIRE) TRACK PARALLEL (LEFT HIGH)
CD2 CLR FUNCTION L	CLEAR FUNCTION
CD2 DRIVE ACTIVE (1) H	DRIVE ACTIVE
CD2 GO (1) H	GO
CD2 SEARCH L	SEARCH FUNCTION IN PROGRESS
CD2 SET ATA H	SET ATA FLIP-FLOP
CD2 SET ILL FUNCT ERR L	SET ILLEGAL FUNCTION ERROR
CD2 TRANS L	DATA TRANSFER COMMAND
CD2 WRT L	WRITE FUNCTION
CD3 CLR ATTN H	CLEAR ATTENTION (ATA FLIP-FLOP)
CD3 M RD B H	MAINTENANCE MODE READ DATA, BOTTOM SURFACE
CD3 MAINT H	MAINTENANCE (OR DIAGNOSTIC) MODE
CD3 MCLK H	MAINTENANCE MODE CLOCK
CD3 MIND H	MAINTENANCE MODE INDEX
CD3 RD MAINT REG L	READ MAINTENANCE REGISTER
CD3 WO BO05 L	WIRED-OR REGISTER BUS OUT 05
CD3 WO BO06 L	WIRED-OR REGISTER BUS OUT 06
CN2 C AND M REG CLR L	CONTROL AND MAINTENANCE REGISTERS CLEAR
CN2 CHK BUS PARITY L	CHECK CONTROL BUS PARITY
CN2 CLK DRIVE ACTIVE H	CLOCK DRIVE ACTIVE FLIP-FLOP
CN2 CONT BUS ACTIVE L	CONTROL BUS ACTIVE
CN2 DRI CLR L	DRIVE CLEAR
CN2 DSBL MBUS DRVRS L	DISABLE MASSBUS DRIVERS
CN2 DSBL WRITE AMP L	DISABLE WRITE AMPLIFIER
CN2 ENA CONT BUS OUT L/H	ENABLE CONTROL BUS OUT

Table B-1 (Cont)
RS03 Signal Glossary

Mnemonic	Meaning
CN2 ENABLE CLR FUNC H	ENABLE CLEAR FUNCTION
CN2 LD CONT REG L	LOAD CONTROL REGISTER
CN2 LD DES ADDR REG L	LOAD DESIRED ADDRESS REGISTER
CN2 LD ERR REG L	LOAD ERROR REGISTER
CN2 LD MAINT REG L	LOAD MAINTENANCE REGISTER
CN2 PWR UP ATTN L	ON POWER UP, SET ATTENTION (SET ATA FLIP-FLOP)
CN2 RD ATTN SUM REG L	READ ATTENTION SUMMARY REGISTER
CN2 RD CONT REG L	READ CONTROL REGISTER
CN2 RD DES ADDR REG L	READ DESIRED ADDRESS REGISTER
CN2 RD DRI TYP REG L	READ DRIVE TYPE REGISTER
CN2 RD ERR REG L	READ ERROR REGISTER
CN2 RD LK AHD REG L	READ LOOK AHEAD REGISTER
CN2 RD MAINT REG L	READ MAINTENANCE REGISTER
CN2 RD STATUS REG L	READ STATUS REGISTER
CN2 SET ILL REG ERR L	SET ILLEGAL REGISTER ERROR
CN2 SET RMR ERR L	SET REGISTER MODIFICATION REFUSED ERROR
CN2 TRANSFER (0) H	TRANSFER
CN2 UNIT NUM 0 H	UNIT NUMBER 0
CN2 UNIT NUM 1 H	UNIT NUMBER 1
CN2 UNIT NUM 2 H	UNIT NUMBER 2
CN2 WRT ATTN SUM REG L	WRITE ATTENTION SUMMARY REGISTER
DA2 DDBO 00 L	DRIVE DATA BUS OUT 00
DA2 DDBO 01 L	DRIVE DATA BUS OUT 01
DA2 DDBO 02 L	DRIVE DATA BUS OUT 02
DA2 DDBO 03 L	DRIVE DATA BUS OUT 03
DA2 DDBO 04 L	DRIVE DATA BUS OUT 04
DA2 DDBO 05 L	DRIVE DATA BUS OUT 05
DA2 DDBO 06 L	DRIVE DATA BUS OUT 06
DA2 DDBO 07 L	DRIVE DATA BUS OUT 07
DA2 DDBO 08 L	DRIVE DATA BUS OUT 08
DA2 DDBO 09 L	DRIVE DATA BUS OUT 09
DA2 DDBO 10 L	DRIVE DATA BUS OUT 10
DA2 DDBO 11 L	DRIVE DATA BUS OUT 11
DA2 DDBO 12 L	DRIVE DATA BUS OUT 12
DA2 DDBO 13 L	DRIVE DATA BUS OUT 13
DA2 DDBO 14 L	DRIVE DATA BUS OUT 14
DA2 DDBO 15 L	DRIVE DATA BUS OUT 15
DA2 DDBO 16 L	DRIVE DATA BUS OUT 16
DA2 DDBO 17 L	DRIVE DATA BUS OUT 17
DA2 DDPAO L	DRIVE DATA BUS PARITY OUT

Table B-1 (Cont)
RS03 Signal Glossary

Mnemonic	Meaning
DA2 SYNC PAR ERR H	SYNCHRONOUS (DATA) BUS PARITY ERROR
DA3 NRZ WRT DATA L	NRZ WRITE DATA (4.8M bit/sec)
DA3 SET DATA ERR L	SET DATA CHECK (DCK) ERROR
ED2 CLK H	NRZ DATA CLOCK (4.8 MHz)
ED2 NRZ RD DATA H	NRZ READ DATA (4.8M bit/sec)
ED2 RD SYNC L	READ DATA SYNCHRONIZATION INTERVAL
ED2 VCO	VOLTAGE CONTROLLED OSCILLATOR
ED2 WINDOW L	WINDOW
ED2 WRT DATA PULSE L	MILLER ENCODED WRITE DATA PULSE
ED2 WRT GATE L	WRITE GATE
FT3 CRC WD L	CRC WORD
FT3 SAMPLE RUN H	SAMPLE RUN
FT4 LOAD SR L	PARALLEL LOAD SHIFT REGISTER
FT4 PRESENT DATA (1) H	PRESENT DATA
FT4 RD OR WRT CLK L	READ OR WRITE CLOCK (4.8 MHz)
FT4 STROBE BUFF L	STROBE DATA BUFFER
FT4 SYNC CLK L	MASSBUS SCLK
FT4 WD COUNT CLK L	WORD/SECTOR COUNTER CLOCK
FT4 WRT PRE (0) H	WRITE PREAMBLE (WHEN LOW)
FT5 ADDRS CONF L	ADDRESS CONFIRMED
FT5 ADDRS SEARCH H	ADDRESS SEARCH
FT5 ATTN L	MASSBUS ATTENTION
FT5 CLR GO L	CLEAR GO
FT5 EBL L	MASSBUS EBL (END OF BLOCK)
FT5 EXCEPTION L	MASSBUS EXC (TO CONTROLLER)
FT5 READ L	READ DATA FROM DISK
FT5 SET AOE (0) H	SET ADDRESS OVERFLOW ERROR
FT5 TRANS DATA L	TRANSFER DATA TO/FROM THIS SECTOR
FT5 WO BO13 L	WIRED-OR REGISTER BUS OUT 13
HM3 TRK X4 40-77 L	INVERTED AD2 TRK X4 H
PS2 SAFE L	POWER SUPPLY SAFE
RW2 HS 1	HEAD SELECTION COLUMN, 1
RW2 HS 2	HEAD SELECTION COLUMN, 2
RW2 READ DATA PULSE L	MILLER ENCODED READ DATA PULSE
ST3 OPI (1) H	OPERATION INCOMPLETE ERROR
ST3 SET CONT PAR ERR H	SET CONTROL BUS PARITY ERROR
ST4 ATA H	ATTENTION ACTIVE
ST4 B ERR L	CLASS B ERROR
STA COMP ERR L/H	COMPOSITE ERROR
ST5 WO BO12 L	WIRED-OR REGISTER BUS OUT 12
ST5 WO BO14 L	WIRED-OR REGISTER BUS OUT 14

Table B-1 (Cont)
RS03 Signal Glossary

Mnemonic	Meaning
ST5 WO BO15 L	WIRED-OR REGISTER BUS OUT 15
TM3 RESYNC L	RESYNCHRONIZE AFTER INDEX
TM3 SEC PULSE L	SECTOR PULSE
TM3 SET SYN H	SET READ SYNC FLIP-FLOP
TM4 INTERLEAVED H	SECTOR INTERLEAVED
TM4 SEC ADD 0 H	SECTOR ADDRESS 00
TM4 SEC ADD 1 H	SECTOR ADDRESS 01
TM4 SEC ADD 2 H	SECTOR ADDRESS 02
TM4 SEC ADD 3 H	SECTOR ADDRESS 03
TM4 SEC ADD 4 H	SECTOR ADDRESS 04
TM4 SEC ADD 5 H	SECTOR ADDRESS 05
TM4 WO BO02 L	WIRED-OR REGISTER BUS OUT 02
TM4 WO BO03 L	WIRED-OR REGISTER BUS OUT 03
TM4 WO BO04 L	WIRED-OR REGISTER BUS OUT 04
TM4 WO BO07 L	WIRED-OR REGISTER BUS OUT 07
TM4 WO BO08 L	WIRED-OR REGISTER BUS OUT 08
TM4 WO BO09 L	WIRED-OR REGISTER BUS OUT 09
TM4 WO BO10 L	WIRED-OR REGISTER BUS OUT 10
TM4 WO BO11 L	WIRED-OR REGISTER BUS OUT 11
TM5 CLK PULSE L	TIMING TRACK CLOCK PULSE (4.8 MHz)
TM5 INDEX	INDEX
TM5 SET TIMING ERR L	SET TIMING ERROR
TRA2 C to D H	CONTROLLER TO DRIVE (MASSBUS CTOD)
TRA2 DDBI 00 H	DRIVE DATA BUS IN 00
TRA2 DDBI 01 H	DRIVE DATA BUS IN 01
TRA2 DDBI 02 H	DRIVE DATA BUS IN 02
TRA2 DDBI 03 H	DRIVE DATA BUS IN 03
TRA2 DDBI 04 H	DRIVE DATA BUS IN 04
TRA2 DDBI 05 H	DRIVE DATA BUS IN 05
TRA2 REG SEL 3 H	REGISTER SELECT 03 (MASSBUS RS03)
TRA2 REG SEL 4 H	REGISTER SELECT 04 (MASSBUS RS04)
TRA2 RUN H	RUN
TRA2 WO DCB 00 H	WIRED-OR DRIVE CONTROL BUS 00
TRA2 WO DCB 01 H	WIRED-OR DRIVE CONTROL BUS 01
TRA2 WO DCB 02 H	WIRED-OR DRIVE CONTROL BUS 02
TRA2 WO DCB 03 H	WIRED-OR DRIVE CONTROL BUS 03
TRA2 WO DCB 04 H	WIRED-OR DRIVE CONTROL BUS 04
TRA2 WO DCB 05 H	WIRED-OR DRIVE CONTROL BUS 05
TRA2 WRT CLK H	MASSBUS WCLK
TRB2 DDBI 06 H	DRIVE DATA BUS IN 06

Table B-1 (Cont)
RS03 Signal Glossary

Mnemonic	Meaning
TRB2 DDBI 07 H	DRIVE DATA BUS IN 07
TRB2 DDBI 08 H	DRIVE DATA BUS IN 08
TRB2 DDBI 09 H	DRIVE DATA BUS IN 09
TRB2 DDBI 10 H	DRIVE DATA BUS IN 10
TRB2 DDBI 11 H	DRIVE DATA BUS IN 11
TRB2 EXT EXCEPTION H	MASSBUS EXC FROM CONTROLLER
TRB2 INITIALIZE H	MASSBUS INIT
TRB2 REG SEL 0 H	REGISTER SELECT 00 (MASSBUS RS00)
TRB2 REG SEL 1 H	REGISTER SELECT 01 (MASSBUS RS01)
TRB2 REG SEL 2 H	REGISTER SELECT 02 (MASSBUS RS02)
TRB2 WO DCB 06 H	WIRED-OR DRIVE CONTROL BUS 06
TRB2 WO DCB 07 H	WIRED-OR DRIVE CONTROL BUS 07
TRB2 WO DCB 08 H	WIRED-OR DRIVE CONTROL BUS 08
TRB2 WO DCB 09 H	WIRED-OR DRIVE CONTROL BUS 09
TRB2 WO DCB 10 H	WIRED-OR DRIVE CONTROL BUS 10
TRB2 WO DCB 11 H	WIRED-OR DRIVE CONTROL BUS 11
TRC2 DCPAI H	DRIVE CONTROL BUS PARITY IN
TRC2 DDBI 12 H	DRIVE DATA BUS IN 12
TRC2 DDBI 13 H	DRIVE DATA BUS IN 13
TRC2 DDBI 14 H	DRIVE DATA BUS IN 14
TRC2 DDBI 15 H	DRIVE DATA BUS IN 15
TRC2 DDBI 16 H	DRIVE DATA BUS IN 16
TRC2 DDBI 17 H	DRIVE DATA BUS IN 17
TRC2 DDPAI H	DRIVE DATA BUS PARITY IN
TRC2 DEMAND H	MASSBUS DEM
TRC2 DRIVE SEL 0 H	DRIVE SELECT 00 (MASSBUS DS00)
TRC2 DRIVE SEL 1 H	DRIVE SELECT 01 (MASSBUS DS01)
TRC2 DRIVE SEL 2 H	DRIVE SELECT 02 (MASSBUS DS02)
TRC2 MASS FAIL H	MASS FAIL
TRC2 WO DCB 12 H	WIRED-OR DRIVE CONTROL BUS 12
TRC2 WO DCB 13 H	WIRED-OR DRIVE CONTROL BUS 13
TRC2 WO DCB 14 H	WIRED-OR DRIVE CONTROL BUS 14
TRC2 WO DCB 15 H	WIRED-OR DRIVE CONTROL BUS 15

APPENDIX C
MASSBUS TRANSCEIVERS PIN MAP

C.1 GENERAL

Table C-1 lists the MASSBUS signals with the various pin numbers at which those signals appear.

Table C-1
M5904 Signal Table

Signal Names A	Signal Names B	Signal Names C	Driver Input Pin	RCVR Output Pin	Driver Enable Pin	RCVR Enable Pin	Header Pin –	Header Pin +
D00	D06	D12	AE1	AD1	AB1	AL1	A	B
D01	D07	D13	AC1	AA1	↓	↓	D	C
D02	D08	D14	AK1	AJ1	↓	↓	E	F
D03	D09	D15	AF1	AH1	↓	↓	J	H
D04	D10	D16	AN1	AM1	↓	↓	K	L
D05	D11	D17	AL2	AM2	↓	↓	N	M
C00	C06	DPA	BD2	AU2	AU1	AS1	P	R
C01	C07	C12	AP1	AR1	AT2	BB1	T	S
C02	C08	C13	BD1	BC1	↓	↓	U	V
C03	C09	C14	AV2	BA1	↓	↓	X	W
C04	C10	C15	BJ1	BH1	↓	↓	Y	Z
C05	C11	CPA	BE1	BF1	↓	↓	BB	AA
SCLK	EXC	OCC	BR2	BP2	BN1	BN2	CC	DD
RS3	RS0	DS0	BM1		BM2		FF	EE
RS4	RS1	DS1	BU2		↓		KK	LL
CTOD	RS2	DS2	BP1		↓		MM	NN
WCLK	INIT	DEM	BV1		BU1		RR	PP
RUN	spare	spare	BS1		BR1		TT	SS
ATTN	EBL	TRA		BK1		BL1	JJ	HH
–	–	FAIL	BV2				UU	
+3 V	+3 V	+3 V		BK2				
+5 V	+5 V	+5 V	AA2/ BA2/ AV1				–	+
−15 V	−15 V	−15 V	AB2				These are relative polarity for a logic 1 at module input pin.	
GROUND	GROUND	GROUND	AC2/ AT1/ BC2/ BT1/ AN2					

Table C-1 (Cont)
M5903 Signal Table

Signal Names			Driver Input Pin	RCVR Output Pin	Driver Enable Pin	RCVR Enable Pin	Header Pin	
A	B	C					-	+
D00	D06	D12	AE1	AD1	AB1	AJ1	A	B
D01	D07	D13	AC1	AA1			D	C
D02	D08	D14	AM2	AK1			E	F
D03	D09	D15	AL2	AF1			J	H
D04	D10	D16	AP2	AM1			K	L
D05	D11	D17	AN2	AL1			N	M
C00	C06	DPA	AU1	AS1	AU2	AR1	P	R
C01	C06	C12	AT2	AN1	BS2	AP1	T	S
C02	C08	C13	BB1	BA1			U	V
C03	C09	C14	AV2	AV1			X	W
C04	C10	C15	BJ2	BE1			Y	Z
C05	C11	CPA	BD1	BC1	BF2		BB	AA
SCLK	EXC	OCC	BP2	BL1	BM1	BK1	CC	DD
RS3	RS0	DS0		BF1		BH1	FF	EE
RS4	RS1	DS1		BU1			KK	LL
CTOD	RS2	DS2		BV2			MM	NN
WCLK	INIT	DEM		BR1		BS1	RR	PP
RUN	spare	spare		BP1		BN1	TT	SS
ATTN	EBL	TRA	BL2		BJ1		JJ	HH
–	–	FAIL		BT2			UU	
+3 V	+3 V	+3 V		BR2				
+5 V	+5 V	+5 V	AA2	BA2	AV1			
-20 V	-20 V	-20 V	AB2					
GROUND	GROUND	GROUND	AC2/ AT1/ BC2/ BT1/				VV	

APPENDIX D
IC DESCRIPTIONS

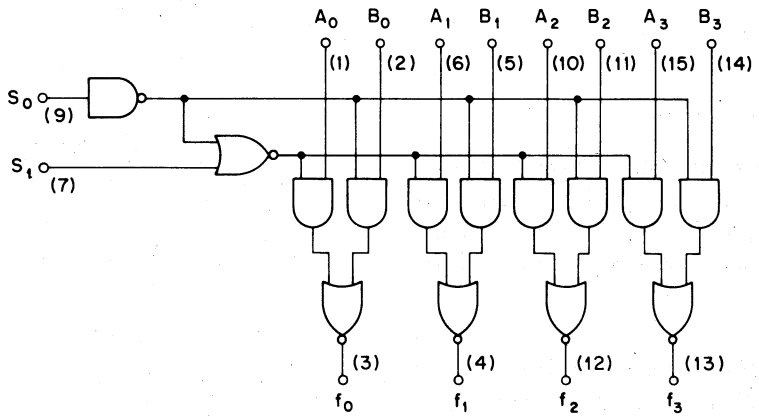
D.1 RS03 INTEGRATED CIRCUIT (IC) DESCRIPTIONS

This appendix provides diagrams, truth tables, pin assignments, and brief descriptions of the MSI integrated circuits used in the RS03 logic. The ICs covered in this section are listed as follows:

8234 2-Input 4-Bit Digital Multiplexer
8271 4-Bit Shift Register
7442 4-Line-To-10-Line Decoder
7485 4-Bit Magnitude Comparator
7490 Decade Counter
7496 5-Bit Shift Register
74145 BCD-To-Decimal Decoder/Driver
74151 Data Selector/Multiplexer
74153 Dual 4-Line-To-1-Line Data Selector/Multiplexer
74157 Quadruple 2-Line-To-1-Line Multiplexer
74161 Synchronous 4-Bit Counter
74173 4-Bit D-Type Register with Tri-State Output
74174 Hex D-Type Flip-Flops
74175 Quad D-Type Flip-Flops
74180 Parity Control Generator/Checker
74190 Synchronous Up/Down Counter with Down/Up Mode Control
74191 Synchronous Up/Down Counter with Down/Up Mode Control
74298 Quadruple 2-Input Multiplexer with Storage

D.2 8234 2-INPUT 4-BIT DIGITAL MULTIPLEXER

This device is a 2-input, 4-bit digital multiplexer designed for general purpose, data selection applications. The 8234 features inverting data paths. The 8234 design has open-collector outputs which permit direct wiring to other open-collector outputs (collector logic).



S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

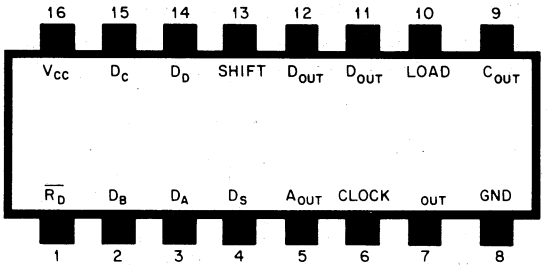
V_{CC} = (16)
GND = (8)
( ) = DENOTES PIN NUMBERS

11-2383

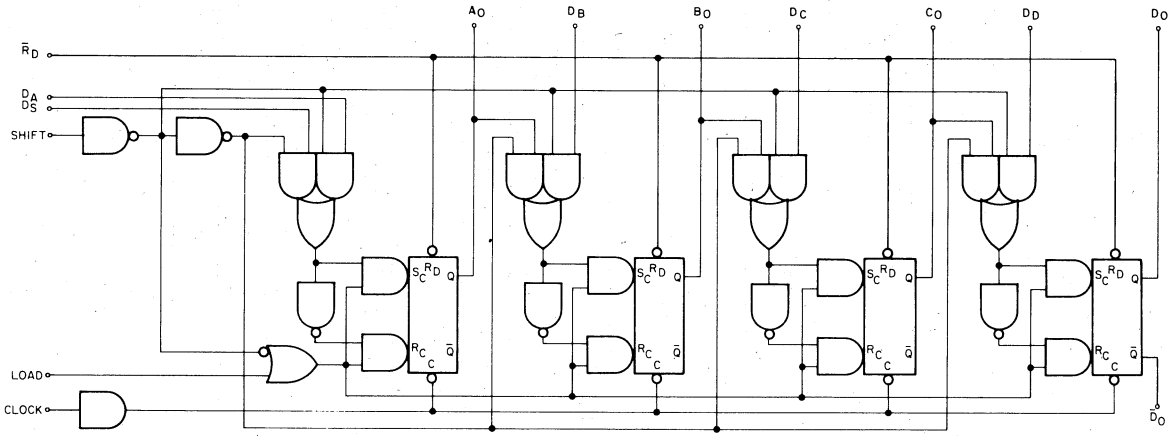
D.3 8271 4-BIT SHIFT REGISTER

Truth Table

Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1



11-0756



11-0476

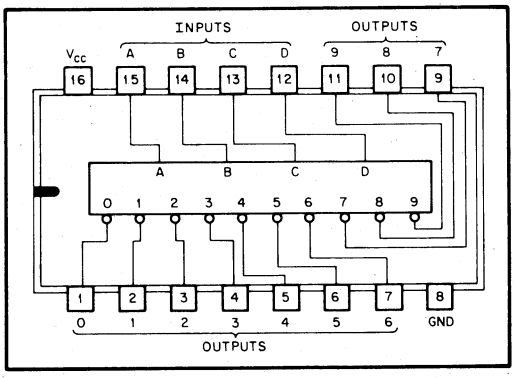
D.4 7442 4-LINE-TO-10-LINE DECODERS (1-of-10)

These monolithic decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

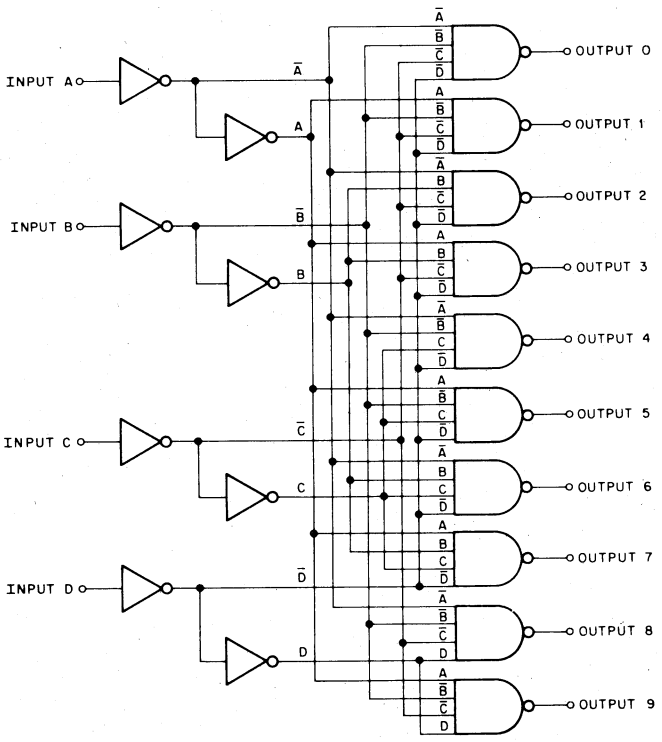
The 7442 BCD-to-decimal decoder features familiar transistor-transistor-logic (TTL) circuits with inputs and outputs that are compatible for use with other TTL and DTL circuits.

TRUTH TABLES

BCD Input				Decimal Output									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1



11-0733



11-0734

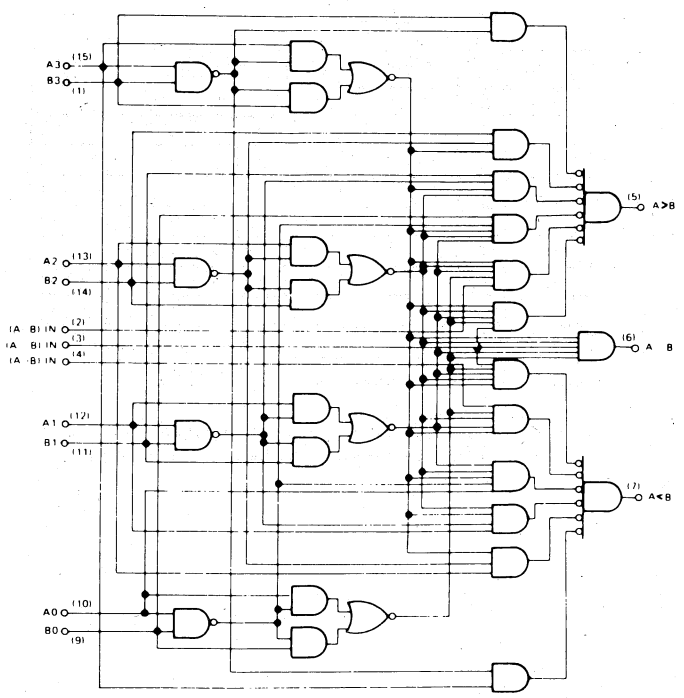
D.5 7485 4-BIT MAGNITUDE COMPARATORS

The 7485 performs magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE H = high level, L = low level, X = irrelevant

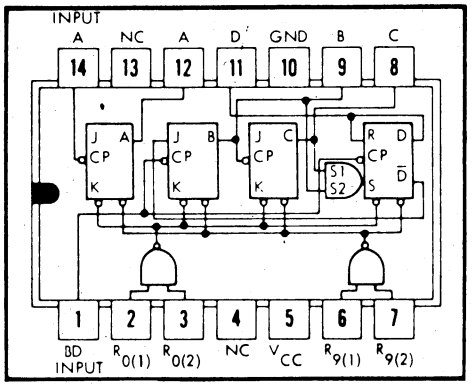


Pin (16) = V_{CC}, Pin (8) = GND

D.6 7490 DECADE COUNTERS

The 7490 consists of four master-slave flip-flops, internally connected to provide a divide-by-two counter and a divide-by-five counter. Gated direct-reset lines inhibit count inputs and return all outputs to zero or to a binary-coded-decimal count of 9.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

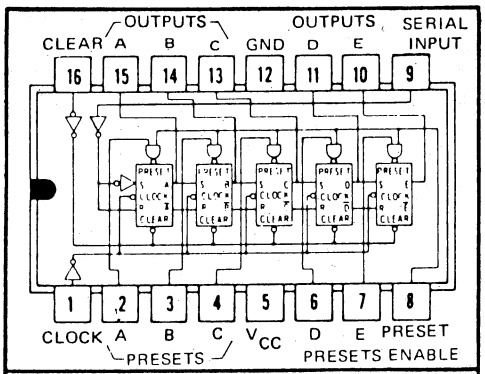
NC—No Internal Connection

NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

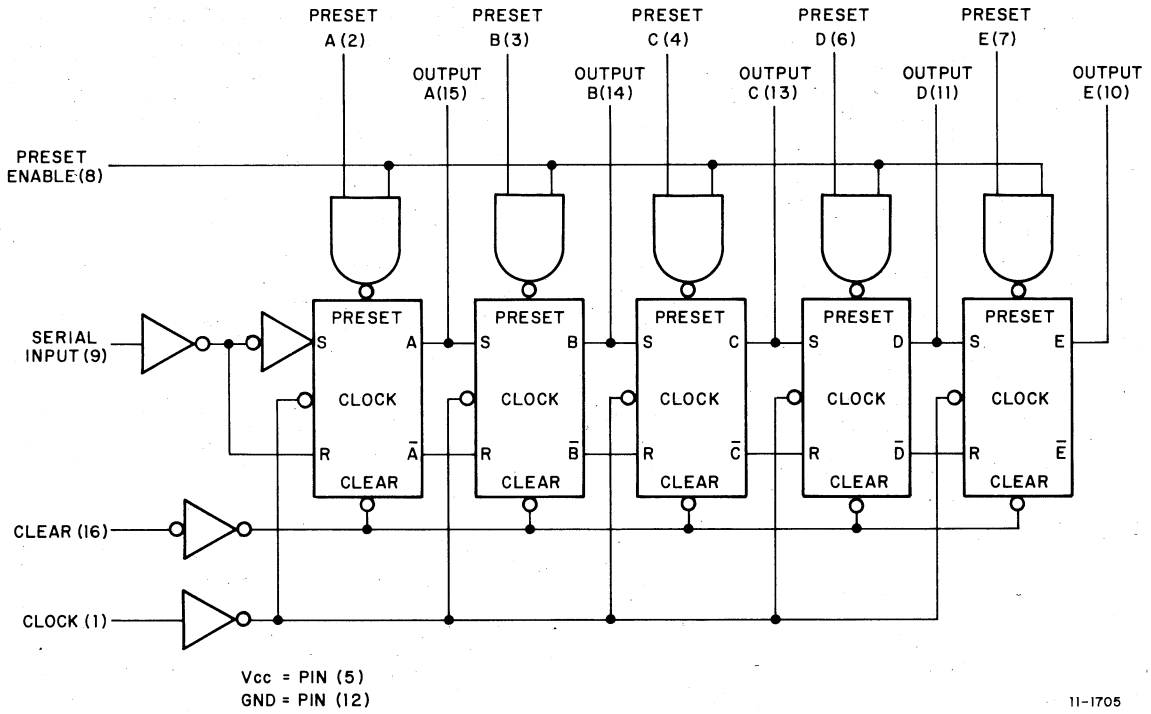
D.7 7496 5-BIT SHIFT REGISTER

The 7496 consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed. Transfer of information to the outputs occurs on the positive-going edge of the clock pulse.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input at clear sets all outputs to logical 0.



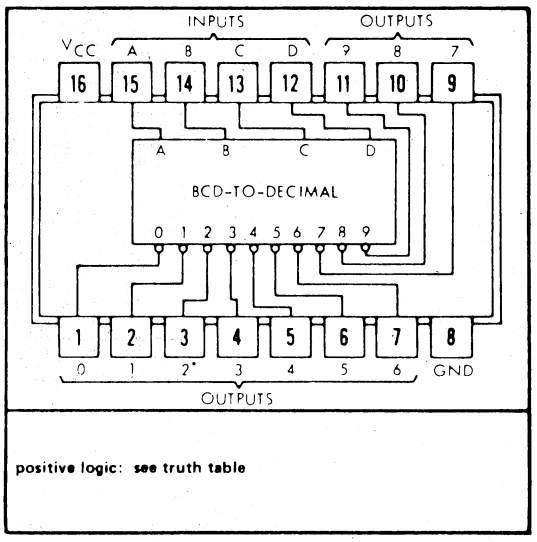
D.8 74145 BCD-TO-DECIMAL DECODER/DRIVERS

The 74145 consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. TTL inputs and NPN output transistors enable their use as indicator/relay drivers or as open-collector, logic-circuit drivers.

TRUTH TABLE

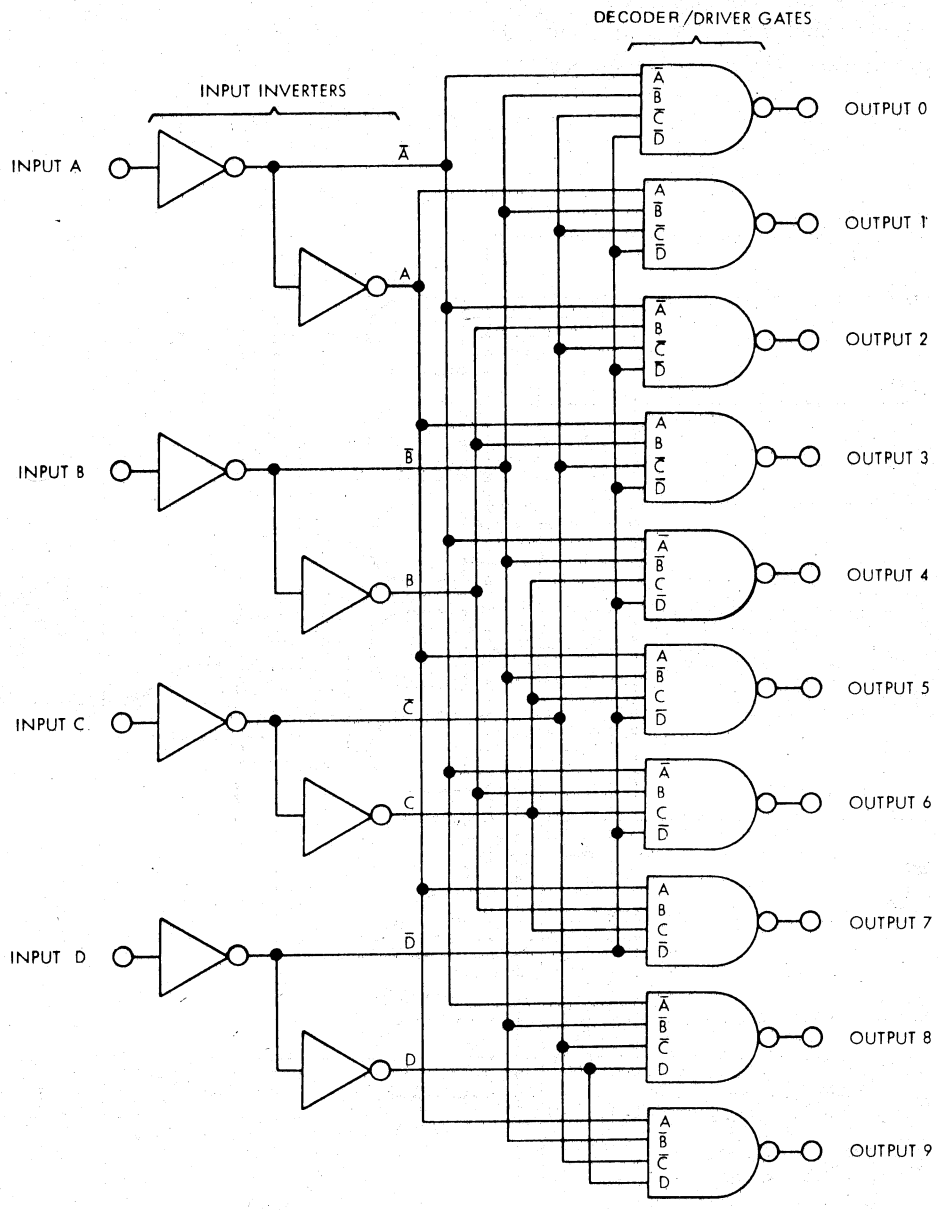
INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



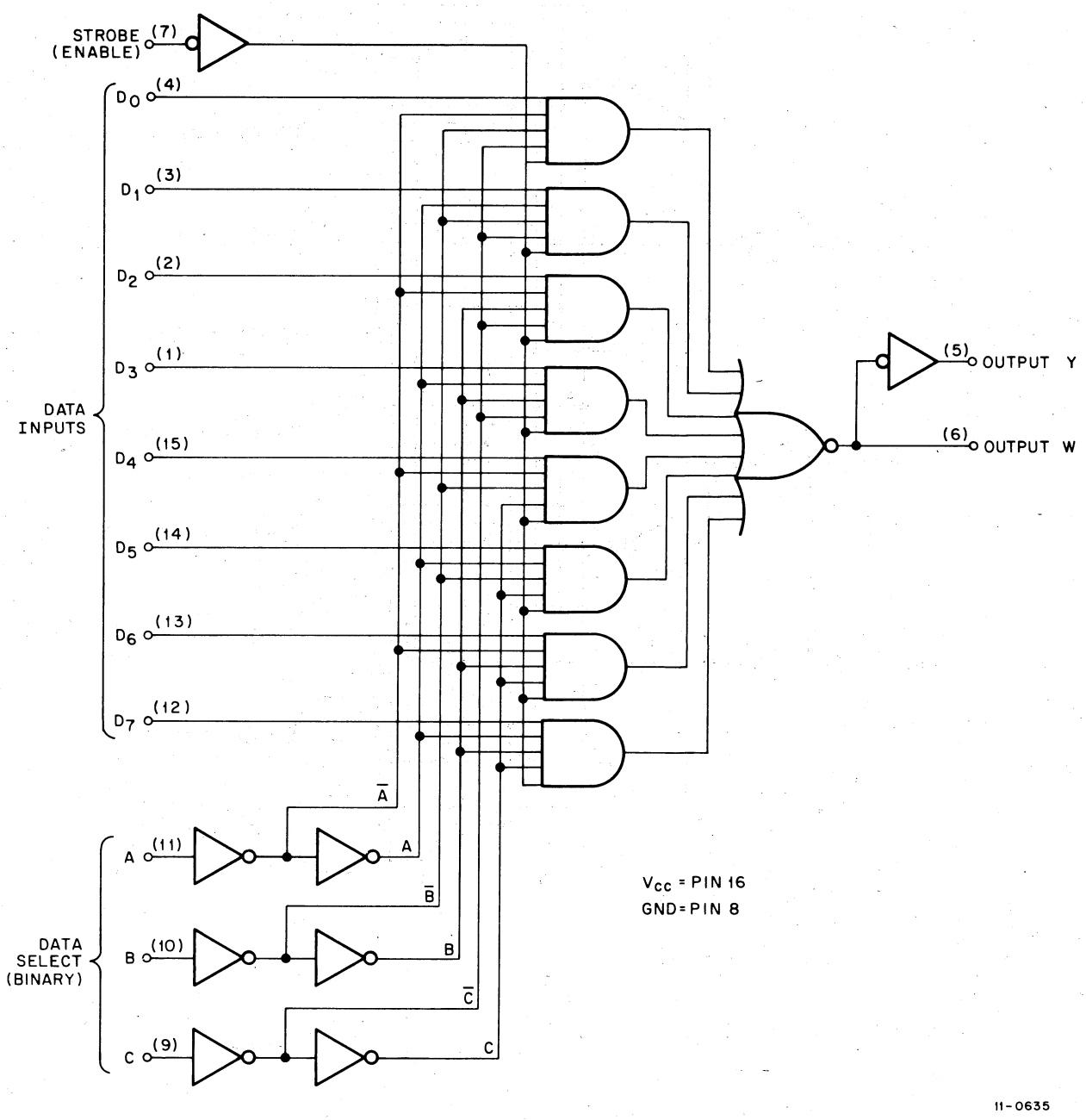
†Pin assignments for these circuits are the same for all packages.

74145 Logic Diagram



D.9 74151 DATA SELECTOR/MULTIPLEXER

The 74151 contains full on-chip binary decoding to select one of eight data sources and has complementary outputs. It includes a strobe input which when taken to a low logic level, enables the multiplexer. The logic diagram is shown below.



Truth Table

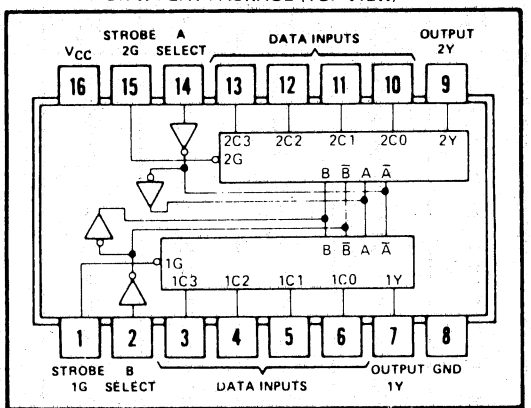
Inputs												Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input, X = irrelevant.

D.10 74153 DUAL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER

The 74153 contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



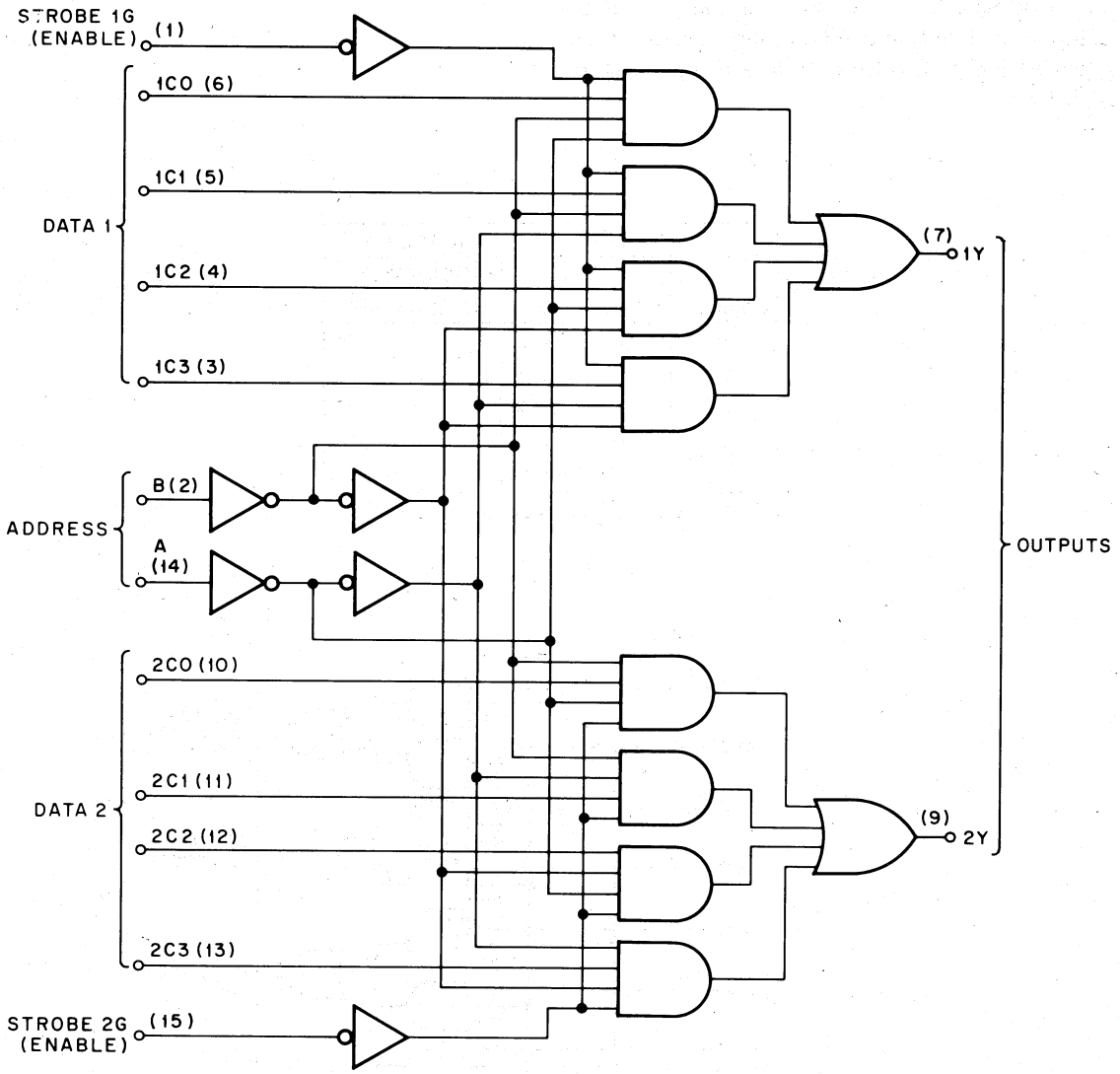
positive logic: See truth table

†Pin assigments for these circuits are the same for all packages.

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

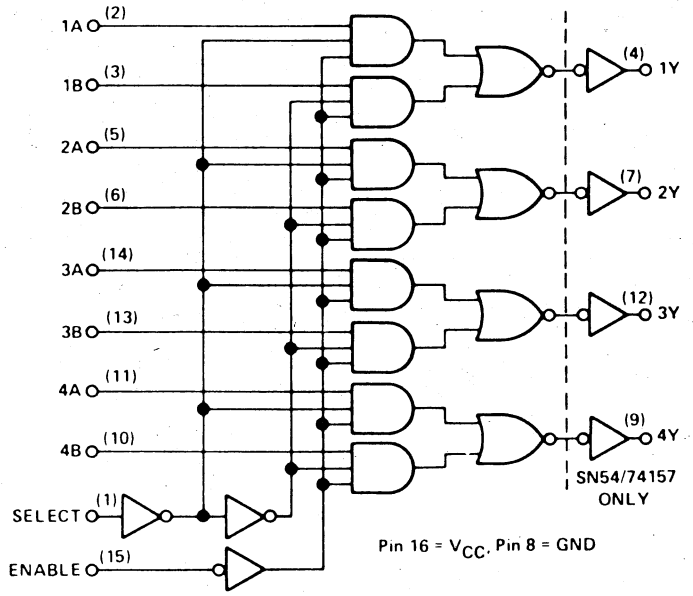

STROBE 1G
(ENABLE)
(1)
1C0 (6)
1C1 (5)
DATA 1
1C2 (4)
1C3 (3)
(7)
1Y
B(2)
ADDRESS
A
(14)
OUTPUTS
2C0 (10)
2C1 (11)
DATA 2
2C2 (12)
2C3 (13)
(9)
2Y
STROBE 2G
(ENABLE)
(15)

D.11 74157 QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER

The 74157 quadruple 2-line to 1-line multiplexer features buffered inputs and outputs. All outputs are low when disabled (enable high). The truth table and logic diagram are shown below.

INPUTS			OUTPUT Y
ENABLE	SELECT	A B	SN54/74157, SN54S/74S157
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

H = high level, L = low level, X = irrelevant

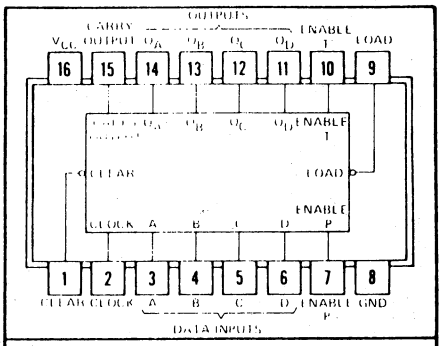


Pin (16) = V_{CC}, Pin (8) = GND

D.12 74161 SYNCHRONOUS 4-BIT COUNTER WITH DIRECT CLEAR

The 74161 features an internal carry look-ahead for high-speed counting schemes. Synchronous operation is achieved by simultaneous clocking of all flip-flops so that all outputs change coincidentally when enabled by internal count enable gates. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†

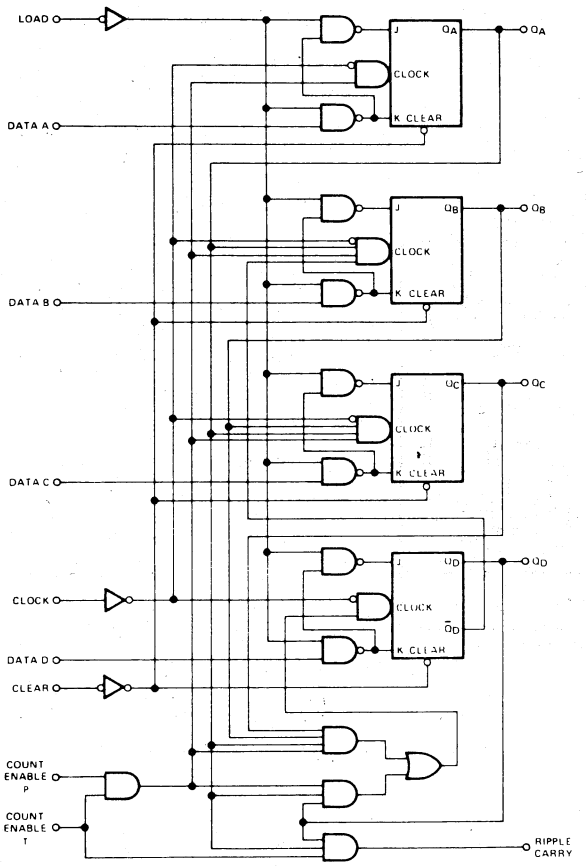


positive logic: See description

†Pin assignments for these circuits are the same for all packages.

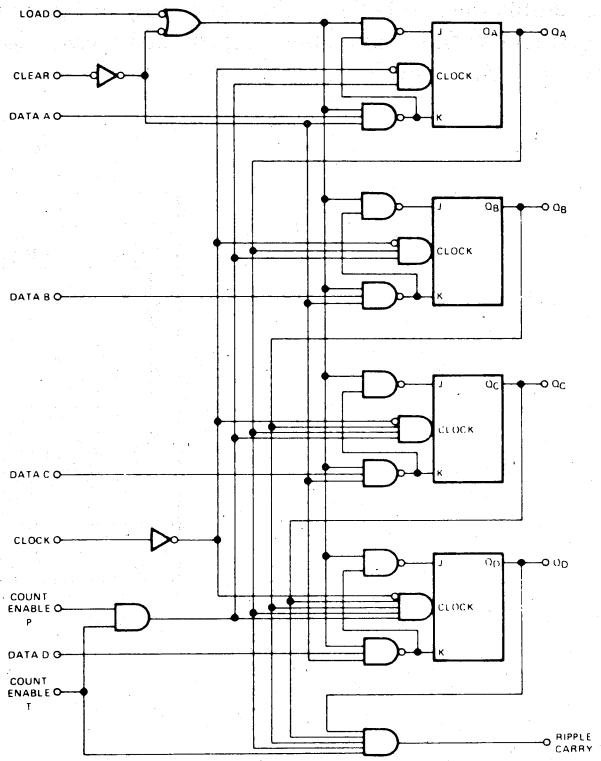
SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.



SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

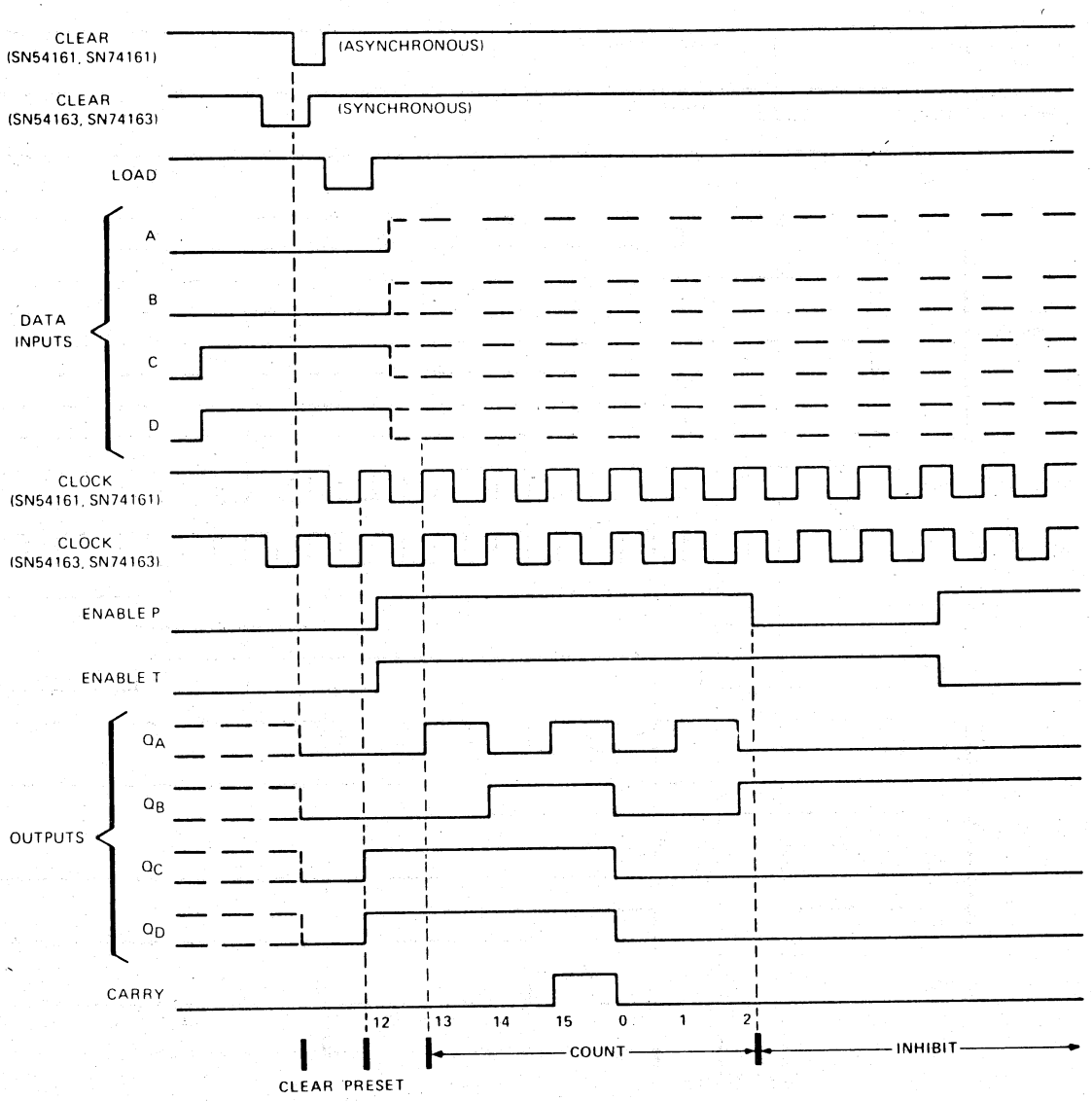
SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

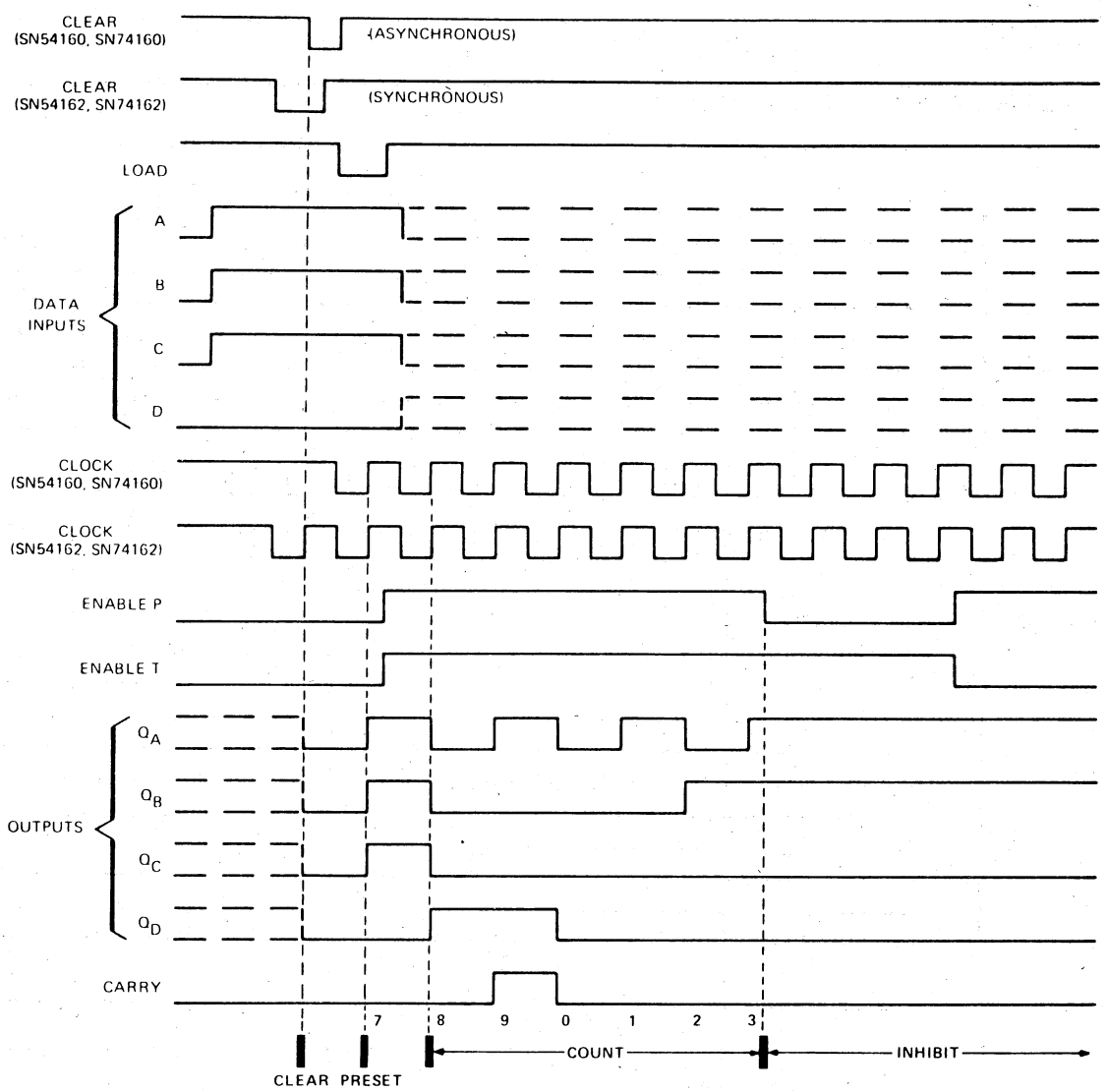
1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

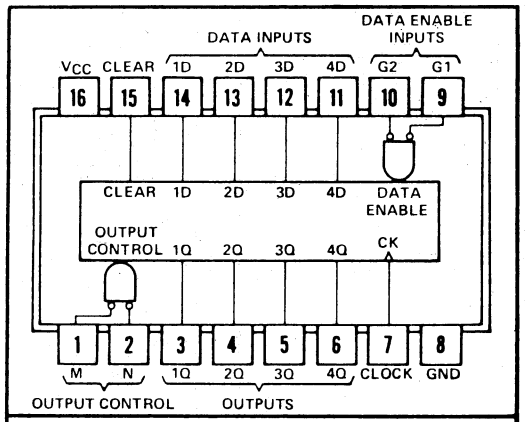
1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



D.13 74173 4-BIT D-TYPE REGISTER WITH TRI-STATE OUTPUT

The 74173 four-bit register includes D-type flip-flops, featuring totem-pole, three-state outputs, capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state, with high logic level drive, permits connection directly to and driving of the bus lines in a bus-organized system without need for interface or pull-up components.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

FUNCTION TABLE

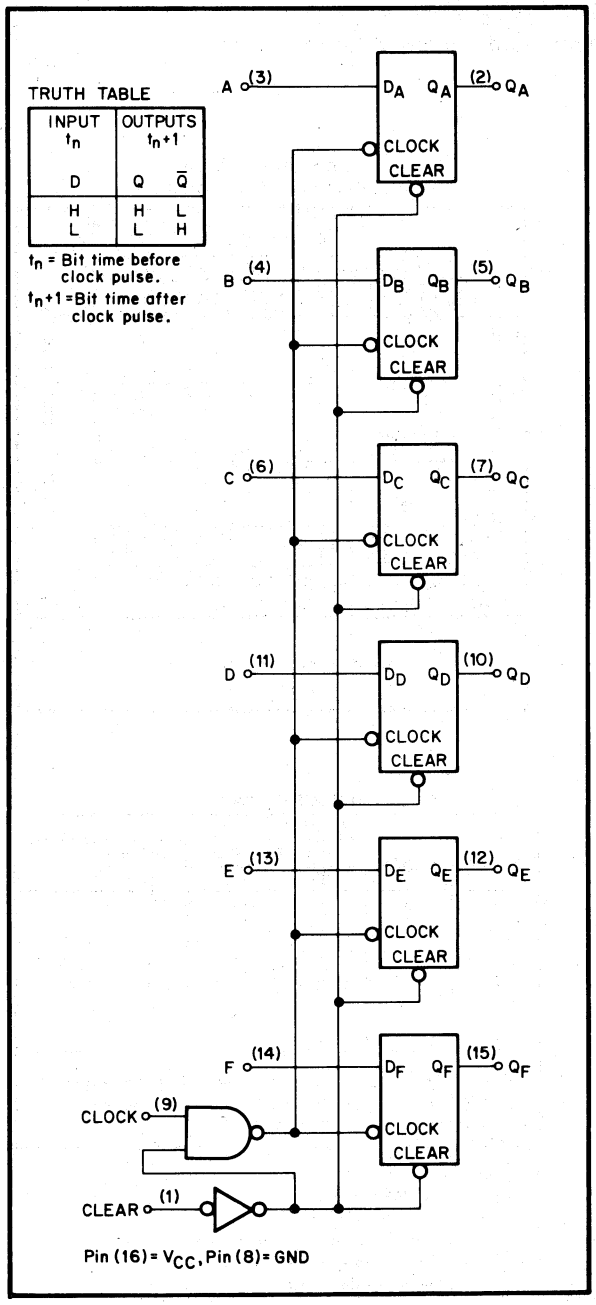
INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE		DATA	Q
		G1	G2	D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low to-high-level transition
X = irrelevant (any input including transitions)
Q_0 = the level of Q before the indicated steady-state input conditions were established.

D.14 74174 HEX D-TYPE FLIP-FLOPS

The 74174 contains six flip-flops with single outputs. The flip-flops contain direct clear inputs and buffered clock inputs.



11-1112

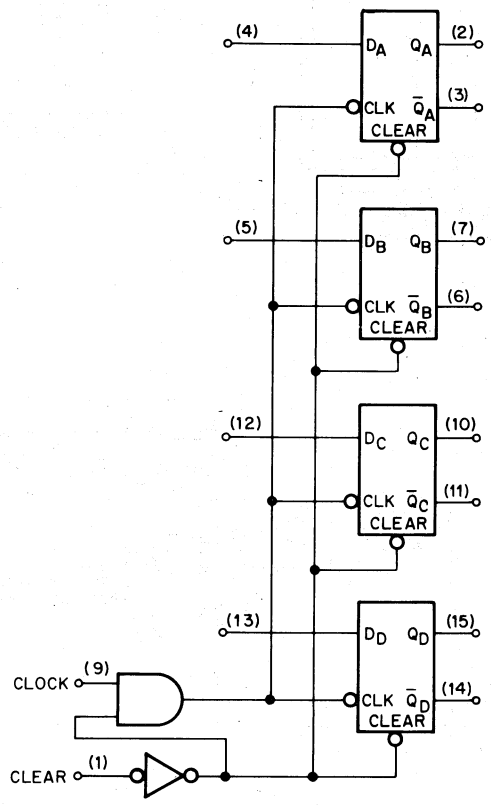
D.15 74175 QUAD D-TYPE FLIP-FLOPS

The 74175 contains four D-type flip-flops with dual outputs. Each flip-flop has direct clear and buffered clock inputs.

TRUTH TABLE

INPUT t_n	OUTPUTS t_{n+1}	
D	Q	$\bar{Q}$
H	H	L
L	L	H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

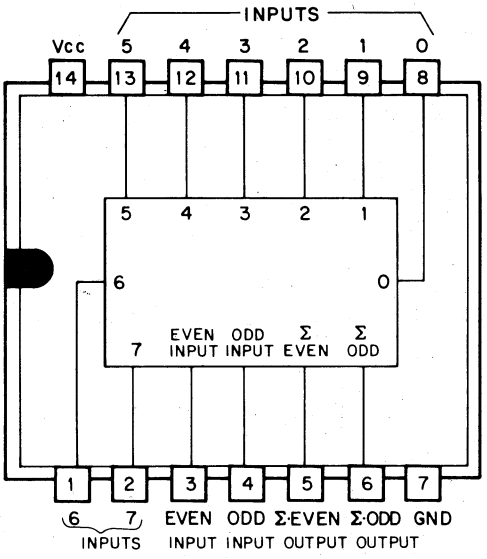


Pin (16) = V_{CC}, Pin (8) = GND

11-1113

D.16 74180 PARITY CONTROL GENERATOR/ CHECKER

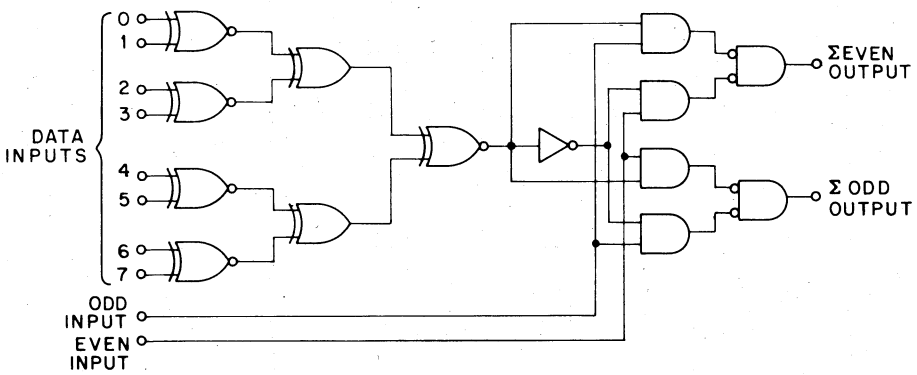
The 74180 is an 8-bit parity generator/checker featuring odd and even outputs and control inputs to provide odd or even parity operation. Word length is expandable by cascading. The truth table, pin connection diagram, and functional block diagram are shown below.



TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= IRRELEVANT

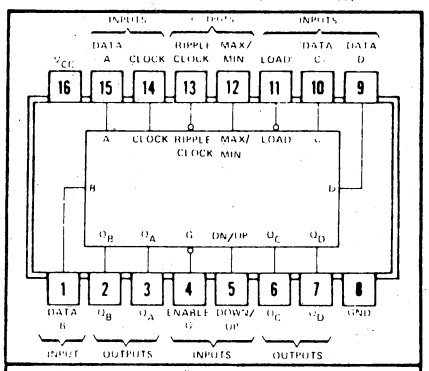


11-2384

D.17 74190 and 74191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

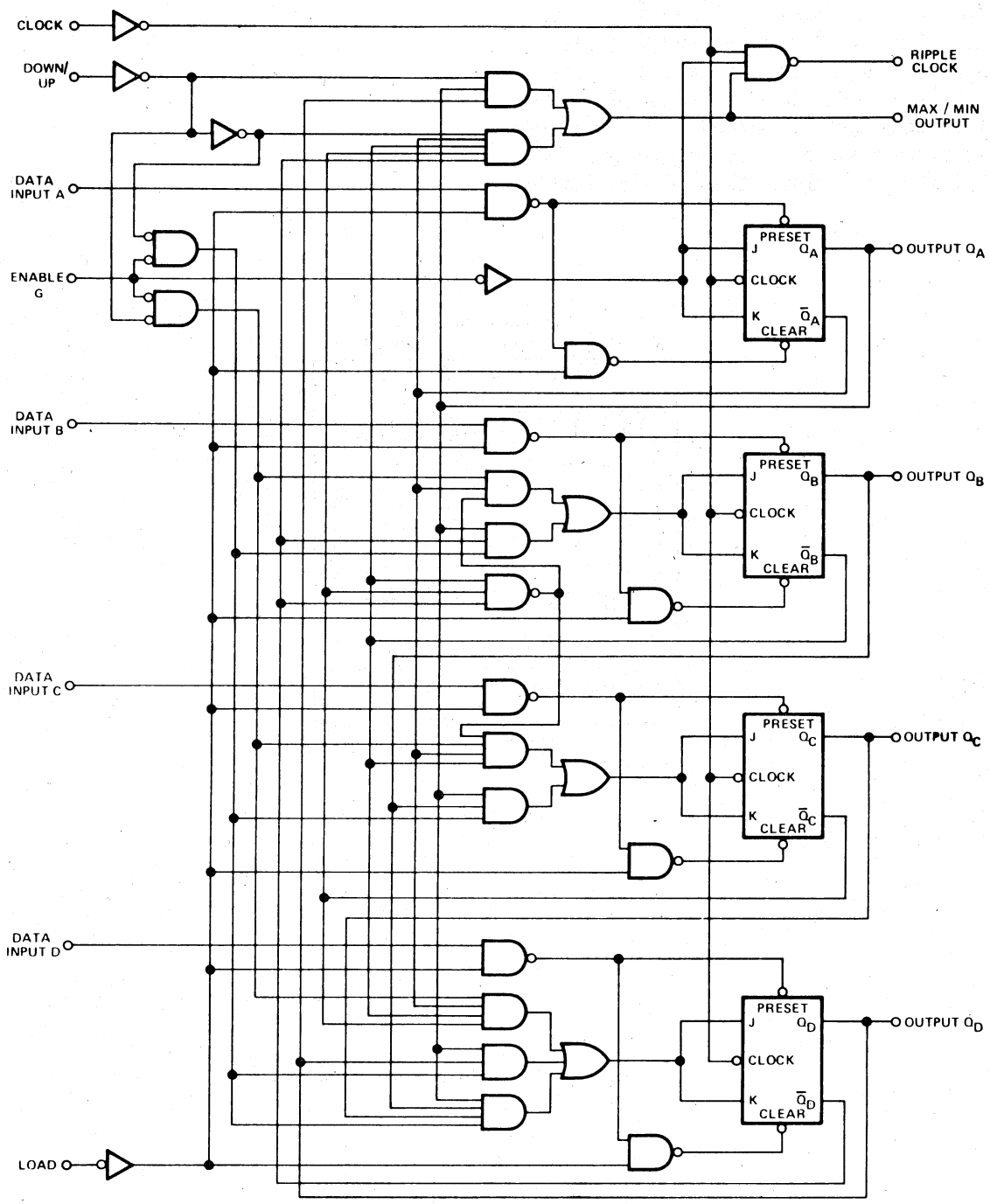
The 74190 and 74191 are synchronous, reversible up/down counters. The 74190 is a BCD counter and the 74191 is a 4-bit binary counter. Synchronous operation is achieved by simultaneous clocking of all flip-flops so that all outputs change coincidentally when so instructed by the steering logic. Flip-flops are triggered on a low-to-high-level transition of the clock input. A high at the enable input inhibits counting.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†

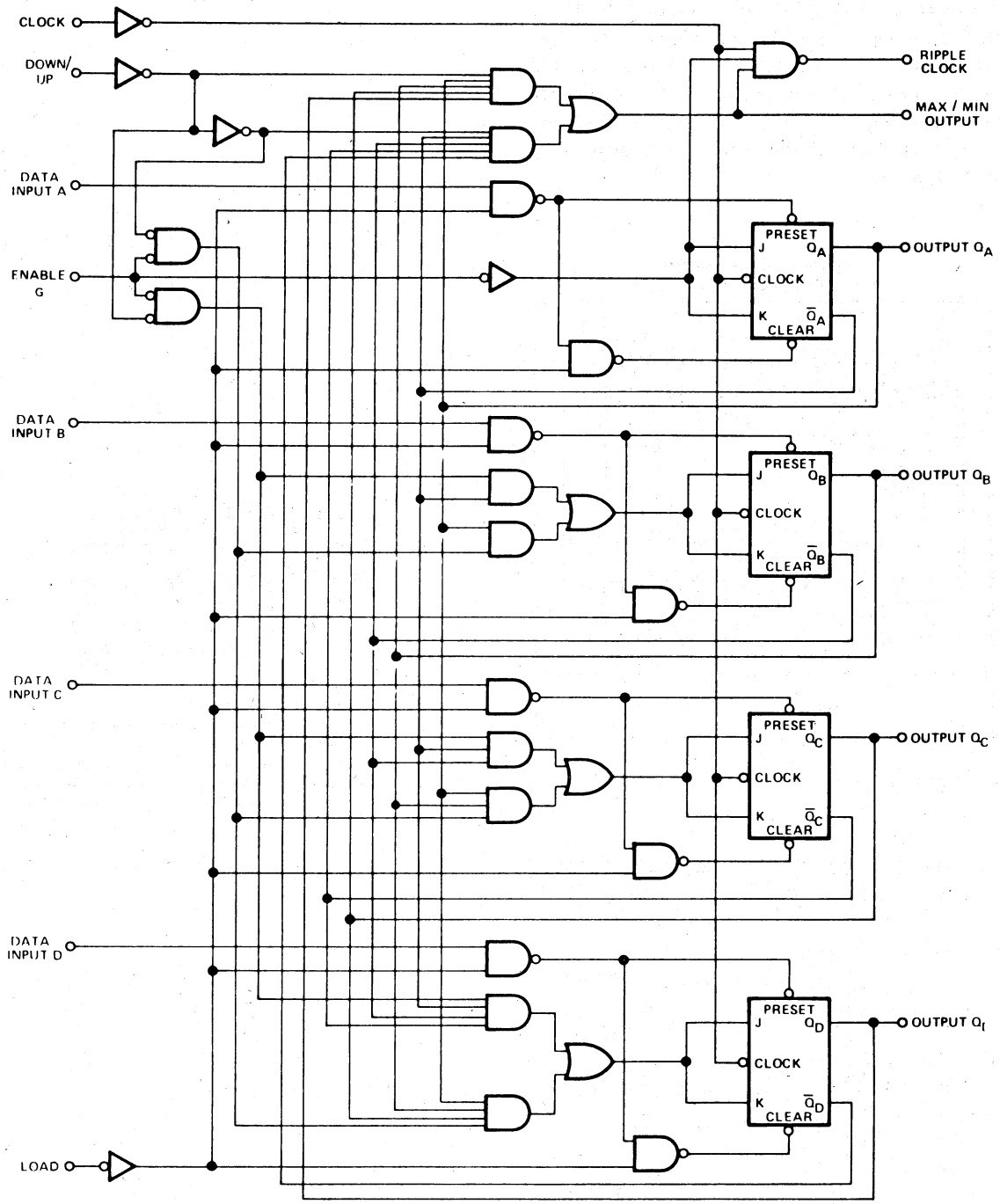


asynchronous inputs: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

†Pin assignments for these circuits are the same for all packages.


CLOCK
DOWN/ UP
DATA INPUT A
ENABLE G
DATA INPUT B
DATA INPUT C
DATA INPUT D
LOAD
RIPPLE CLOCK
MAX / MIN OUTPUT
PRESET
J
Q_A
CLOCK
K
$\overline{Q}_A$
CLEAR
OUTPUT Q_A
PRESET
J
Q_B
CLOCK
K
$\overline{Q}_B$
CLEAR
OUTPUT Q_B
PRESET
J
Q_C
CLOCK
K
$\overline{Q}_C$
CLEAR
OUTPUT Q_C
PRESET
J
Q_D
CLOCK
K
$\overline{Q}_D$
CLEAR
OUTPUT Q_D

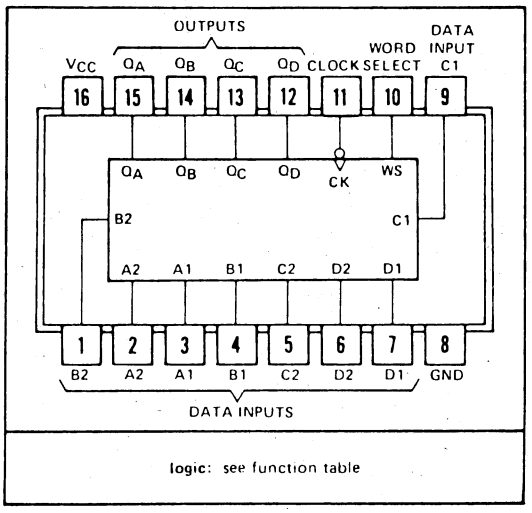
functional block diagram **SN54191, SN74191 BINARY COUNTERS**



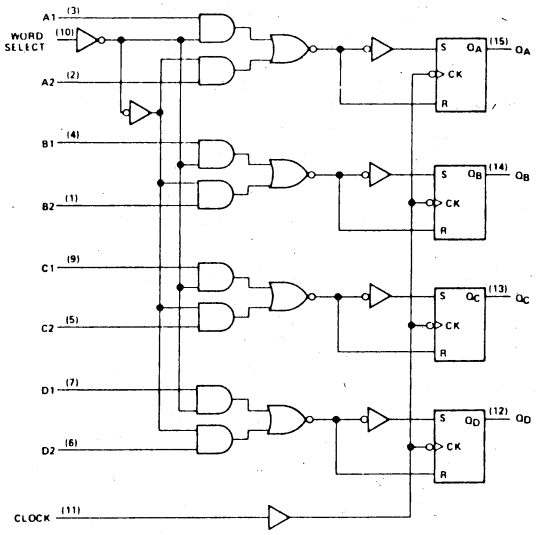
D.18 74298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

The 74298 selects one of two 4-bit data sources and stores data synchronously with the system clock. The logic arrangement is shown in the functional block diagram. When the WORD SELECT input is low the "1" inputs are selected and, when high, selects the "2" inputs. Selected word is clocked into the flip-flops on the negative-going edge of the clock pulse.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



functional block diagram



. . . Dynamic input activated by a transition from a high level to a low level

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
A1, A2, etc. = the level of steady state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the last ↓ transition of the clock input

APPENDIX E
MULTI-LAYER BOARD TECHNIQUES

E.1 GENERAL

The Encode/Decode module (M7751) is a multi-layer etched circuit board. The four layers consist of one power and one ground internal plane and two external signal layers (Figure E-1).

E.2 IC CONNECTIONS

On the M7751 module, which uses a DEC standard inner layer, three types of plated-through holes are made in the board.

1. A feed-through hole which makes no connections to V_{CC} or ground inner layers and only connects the outer signal surfaces.

2. A plated-through hole which connects both signal surfaces to the ground inner layer and does not contact the V_{CC} inner layer.

3. A plated-through hole which connects both signal surfaces to the V_{CC} inner layer and does not contact the ground inner layer.

See Figure E2(a and b) for examples.

E.3 IC AND COMPONENT REMOVAL AND REPLACEMENT

Because the etch is small and plated-through holes are delicate, extra care should be taken during the maintenance and repair of the multi-layer modules, especially when soldering and unsoldering components. Certain tools, listed in Table E-1, (or their equivalent) are recommended for use during removal and replacement of ICs on the multi-layer modules. The manufacturer and type or part number of each tool is indicated in parentheses at its first occurrence in the procedure.

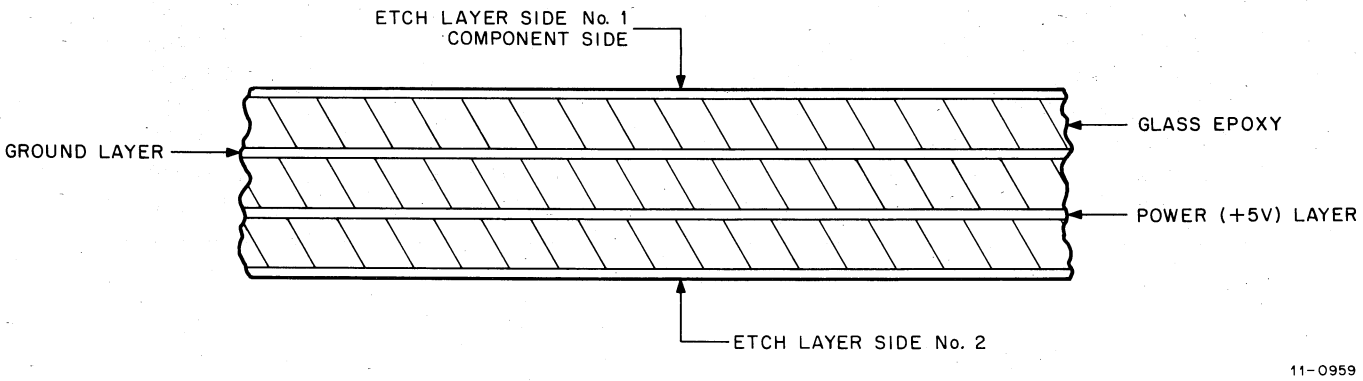


Figure E-1 Cross Section of Multilayer Board

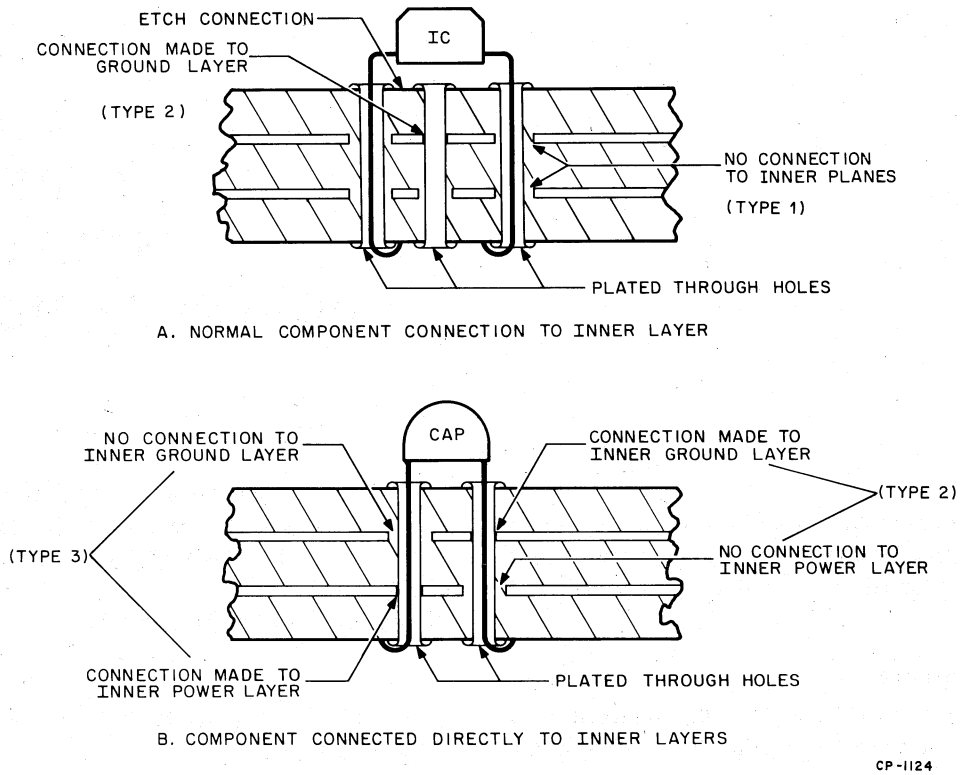


Figure E-2 Component Connections to Inner Layers

Table E-1
Repair Tools Required

Equipment or Tool	Manufacturer	Model, Type or Part No.	DEC Part No.
Diagonal Cutters	Utica	47-4	29-13460
Diagonal Cutters	Utica	466-4 (modified)	29-12551
Miniature Needle Nose Pliers	Utica	23-4-1/2	29-13462
Solder Extractor	Solder Pullit	Standard	29-13451
Soldering Iron (30 W)	Paragon	615	29-13452
Soldering Iron Tip	Paragon	605	29-19333
16-pin IC Clip	AP Incorporated	AP923700	29-10246
24-pin IC Clip	AP Incorporated	AP923714	29-19556

E.3.1 Removal and Replacement of Plastic Case ICs

To remove and replace a plastic case IC and to prevent damage to the multi-layer board, the following procedure should be strictly adhered to. Removal and replacement of ceramic ICs is covered in Paragraph E.3.2.

To remove and replace Plastic Case ICs, proceed as follows:

1. Figure E-3 shows the module to be repaired and the required tools. The sample module is a G401 MOS Memory Matrix module (not used in the RS03, but it is used here to illustrate the principles which apply to the M7751).

2. Figure E-4 shows leads of the defective IC being clipped, using small diagonal cutters (Utica, Part No. 47-4).

3. Figure E-5 shows the IC location after the IC has been removed, with the IC leads still in the board. Locate the IC leads just removed on the soldered (back) side of the board; cut all leads to avoid difficulty during their removal.

4. Figure E-6 shows the IC leads being removed from side 1 of the board. Apply heat to the lead with the soldering iron (Paragon, Part No. 615) until the lead becomes loose. Then remove the lead with pliers (Utica, Part No. 23-4).

   CAUTION

   Leads that are connected to an inner layer require more heat because much of the heat is absorbed by the inner layer. It is helpful to add solder to the lead first, which causes more heat to be conducted to the solder in the eyelet around the lead.

5. Figure E-7 shows a lead immediately after removal from the eyelet. After all of the IC leads have been removed, carefully apply a small amount of solder to each of the eyelets (Figure E-8). The extra solder distributes heat evenly and makes Step 6 (cleaning the holes) easier and more effective.

6. Once the eyelets have been refilled with solder, (Step 5), remove the solder using the soldering iron and solder extractor as shown in Figure E-9. In Figure E-9, the eyelet has no connection to the board inner layers; the solder can be extracted from the same side of the module to which the heat is applied. However, in cases where direct connections to the inner layer are made, heat must be applied to one side of the module and the solder must be extracted from the opposite side, due to the heat sinking properties of the inner layers. In this case, the module should be in a vertical position to allow access to both sides of the module simultaneously.

7. Figure E-10 shows the IC location after all of the eyelets have been cleared of solder. Inspect the eyelets to ensure that no excess solder remains. If all of the solder is not removed, refill the hole as described in Step 5 and again remove the solder as described in Step 6. *Carefully* continue this procedure, as required, until all of the eyelets are cleared of excess solder.

8. Use a cleaning solvent and a brush to clean the IC location of any excess solder flux.

9. Thoroughly inspect the IC location and the surrounding areas for solder splash and damage to etch lines and plated-through holes.

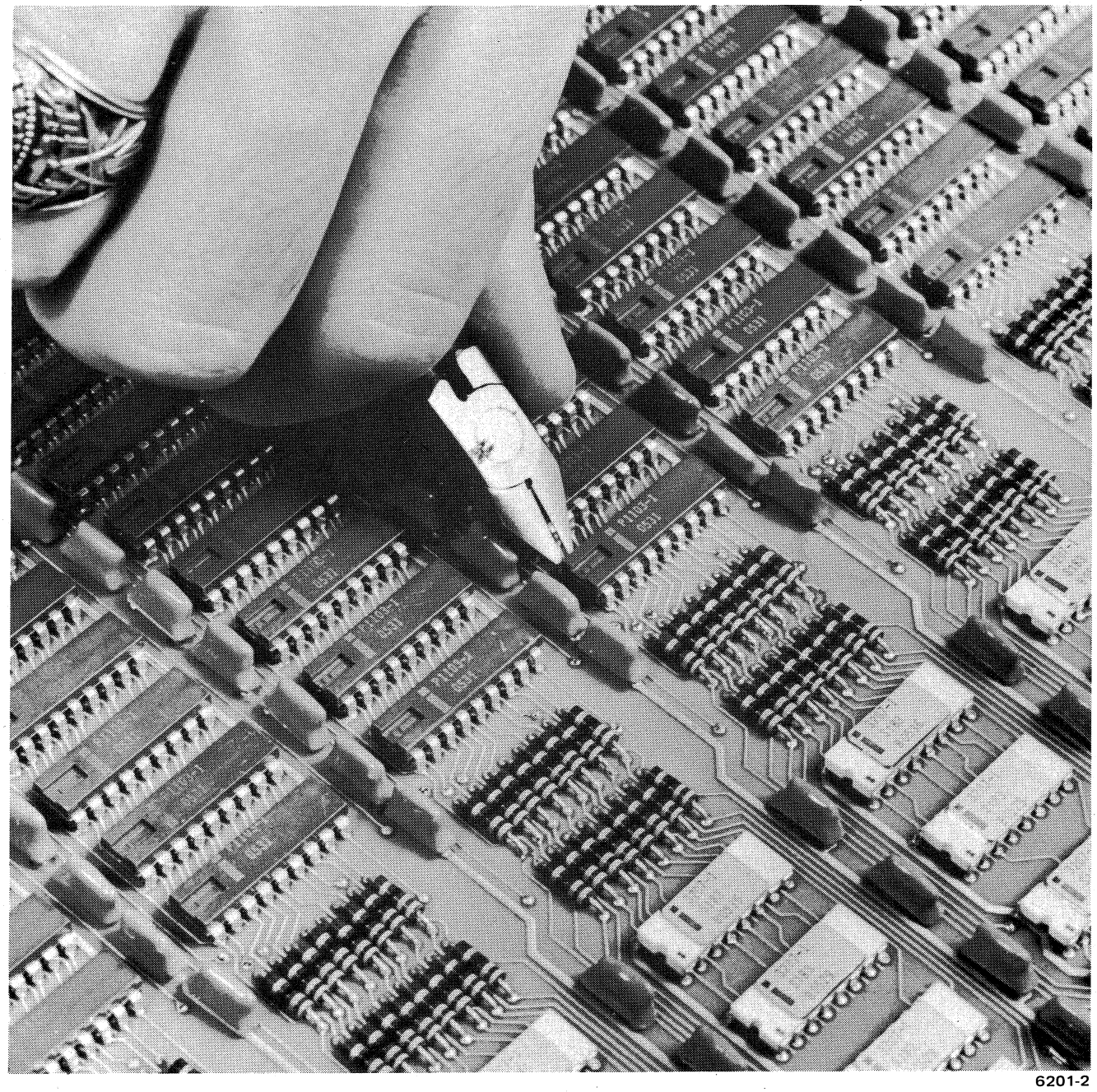
10. Ensure that none of the leads on the replacement IC are bent; insert the replacement IC in the holes. When inserting the replacement IC into place, avoid bending the leads on side 2 of the module to make any future removal of the ICs easier.

    CAUTION

    If the leads must be bent to hold the IC in position for soldering, avoid bending the leads more than 45°, using only one lead at each end and on opposite sides of the IC.

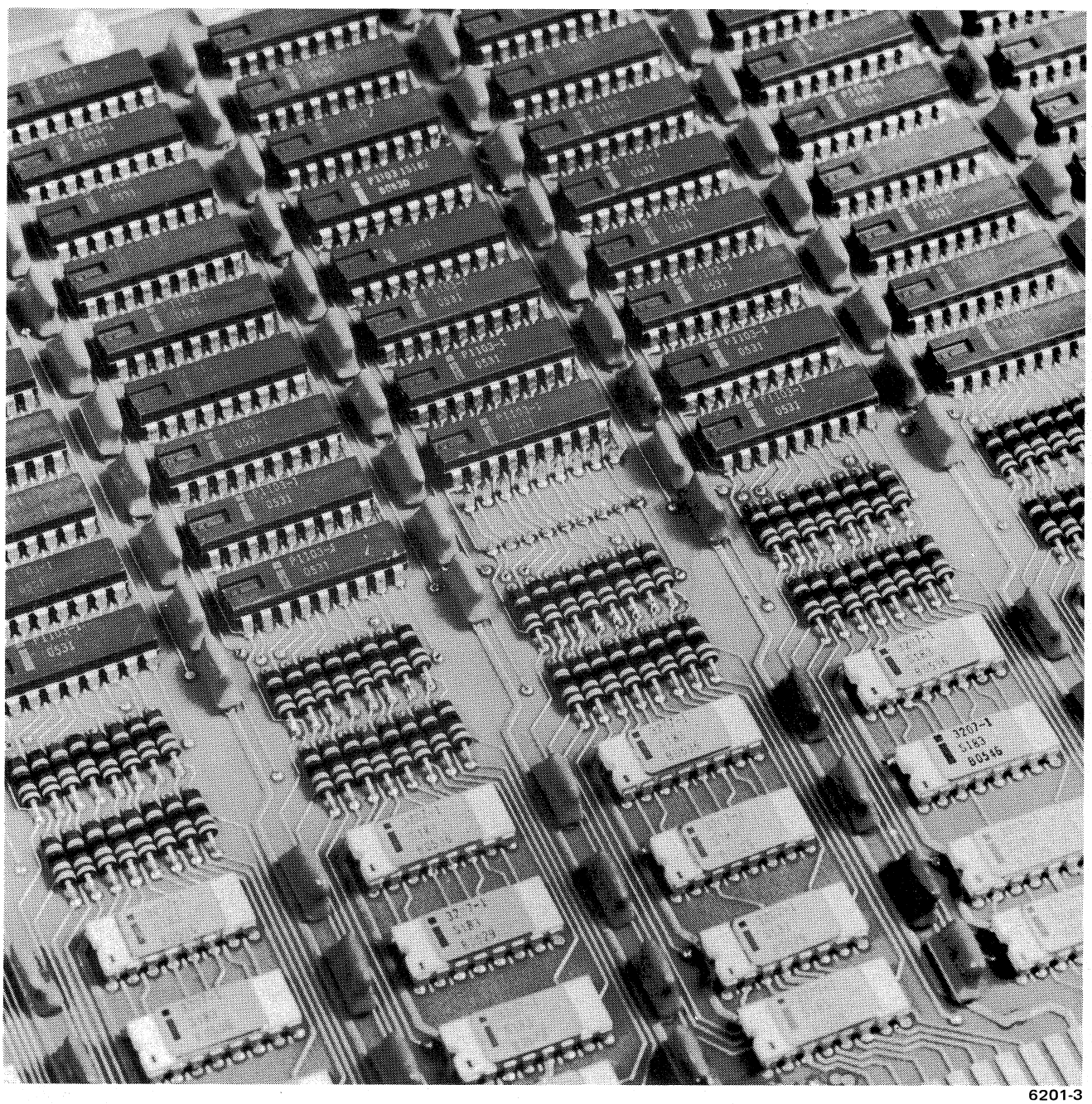
6201-1

Figure E-3 Module to be Repaired and Tools Required



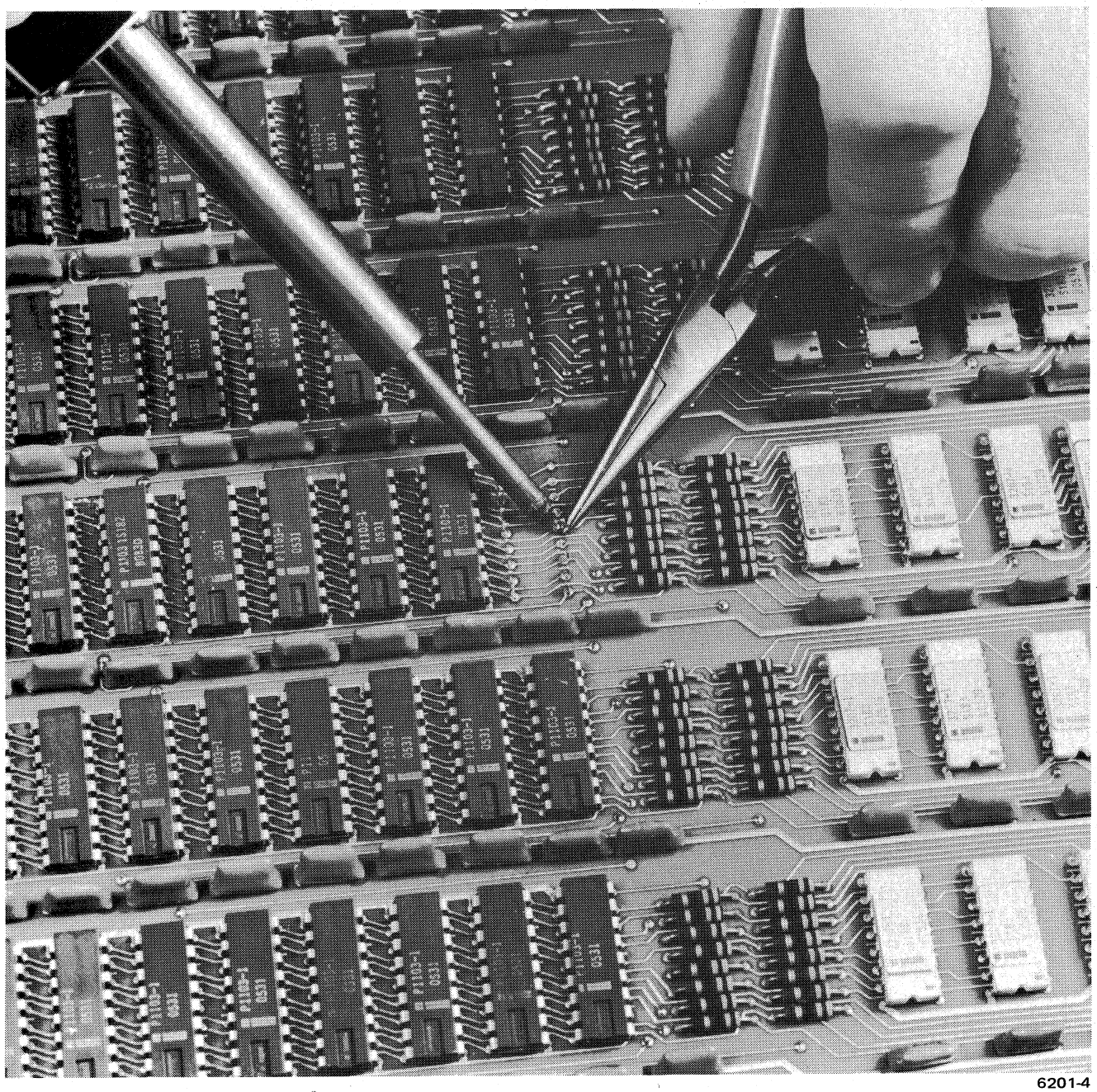
6201-2

Figure E-4 Clipping Leads of a Defective IC



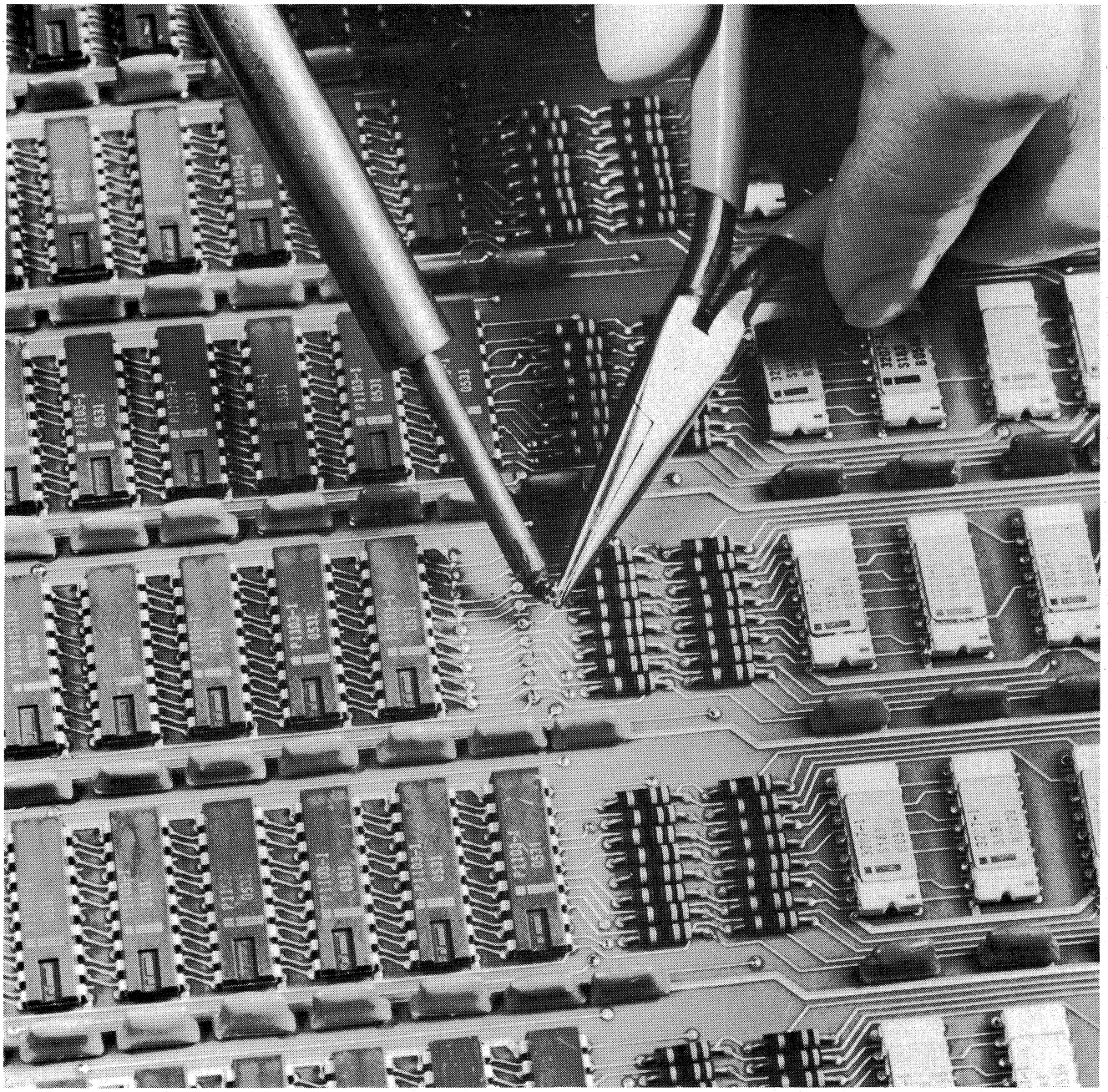
6201-3

Figure E-5 Defective IC Removed



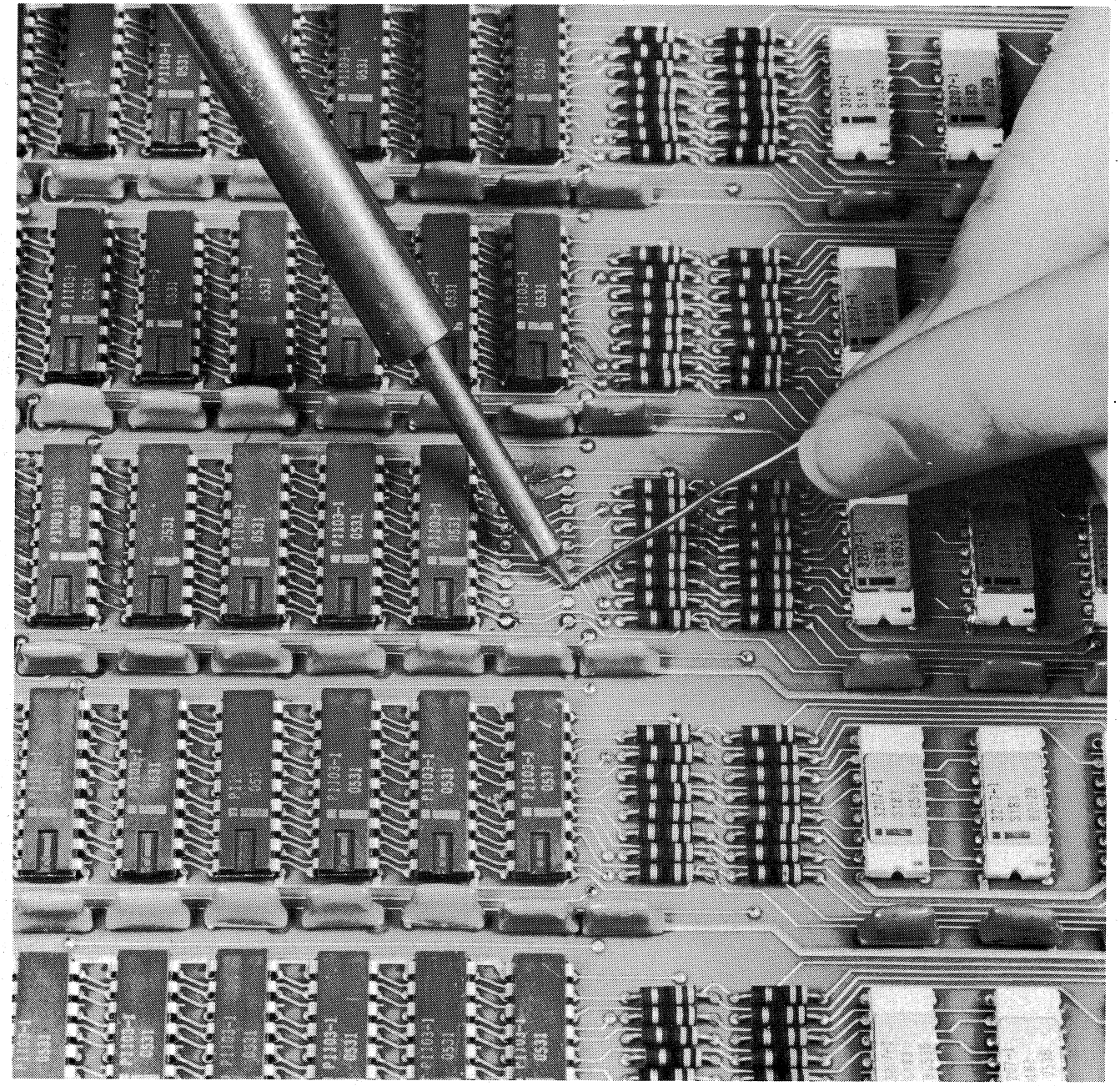
6201-4

Figure E-6 Removing IC Leads



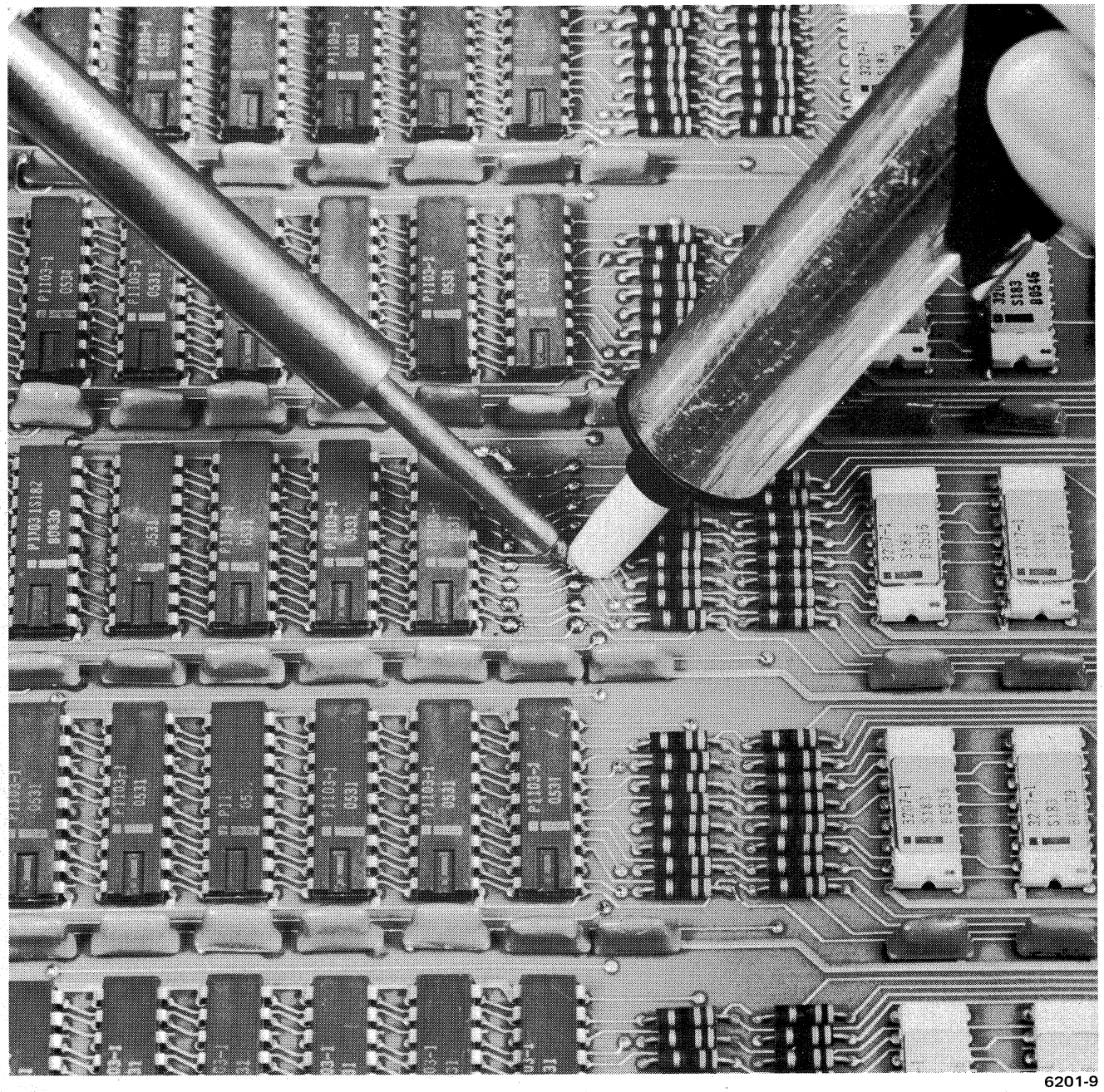
6201-5

Figure E-7 IC Lead Removed



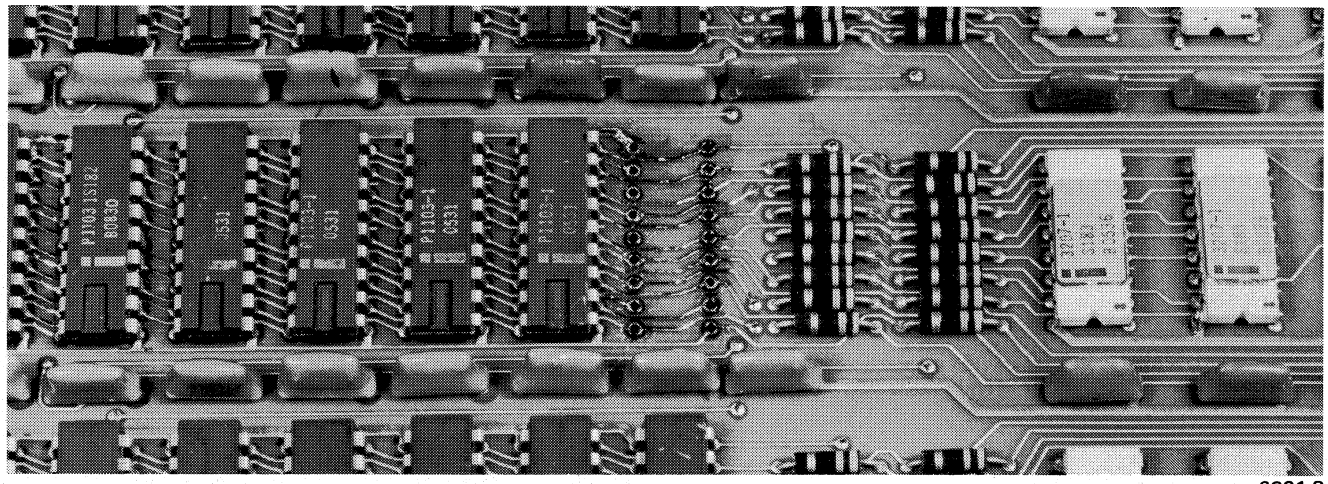
6201-6

Figure E-8 Applying Solder to Refill Eyelet



6201-9

Figure E-9 Removing Excess Solder from Eyelet



6201-8

Figure E-10 IC Location Ready for Insertion of New IC

11. Solder the new IC from side 2 of the module. Use enough solder to fill the holes and make a good connection. Avoid using an excess of solder to prevent an overflow on the top side of the board, which could cause a short under the body of the IC.

12. Once all of the solder connections are made, clean and inspect the area for any damage. Take the necessary corrective action for any defects that are found.

CAUTION

After installing an ECO or replacing a faulty IC on a module, ensure that no short circuit exists between the power and ground of the module. Do this *before* replacing the module in the equipment.

E.3.2 Removal and Replacement of Ceramic ICs

Ceramic ICs require a different removal/replacement procedure than the plastic ICs, because of their different construction. Leads of the plastic ICs extend out and down from the IC case, whereas the leads on the ceramic ICs extend straight down from the IC case, and are harder and thicker than those found on plastic ICs. Thus, certain steps of the removal/replacement procedure for the plastic ICs do not apply to removal and replacement of ceramic ICs. To remove a ceramic IC, use the following procedure:

1. Special diagonal cutters (DEC Part No. 20-12551) are required to remove ceramic ICs (Figure E-11). Cut all of the IC leads and remove the IC from the module.

2. Inspect the component side of the module for any burrs that may be present from cutting the IC lead. If any burrs are present, carefully remove them using the special diagonal cutters.

3. Perform Steps 3 through 12 of the procedure listed in Paragraph E.3.1., substituting Steps 4 and 5 below for Steps 4 and 5 in that procedure.

NOTE

Because the leads will be cut flush with the board surface, it is not possible to remove leads with pliers. Use the following procedure to remove leads:

4. Cut the leads on side 2 of the board to allow easy removal.

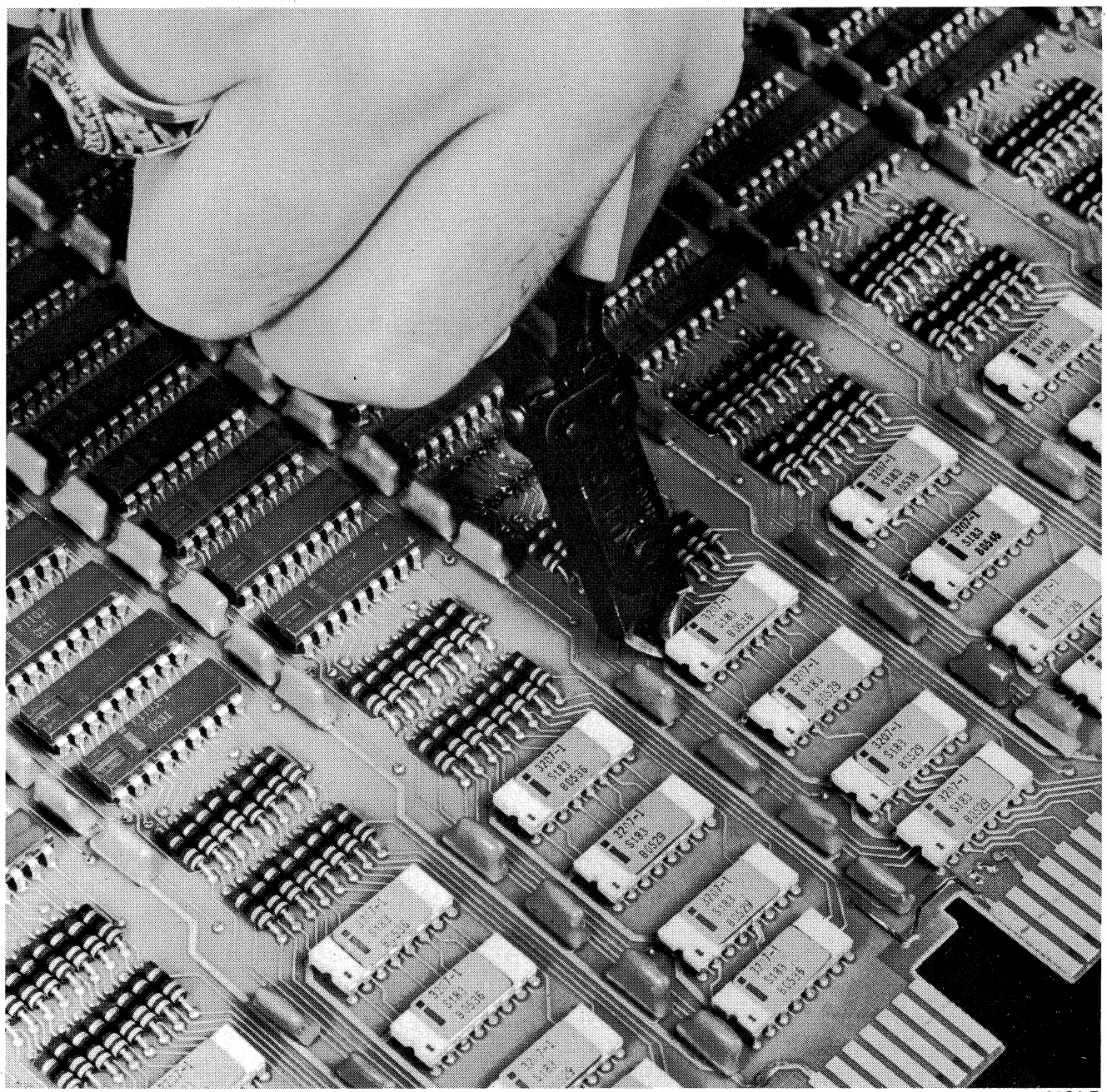
5. On side 1, heat the plated-through hole and extract the lead and the solder with the solder extractor. If the lead cannot be extracted from side 1, try to extract it from side 2.

NOTE

Do not attempt to remove melted solder or lead by banging the module on the bench.

E.4 SOLDER MASK REMOVAL

Side 2 of M7751 modules (the side opposite the component side) is coated with a solder mask to prevent short circuits between adjacent electrical connection points. To repair side 2 of these modules, scrape off the solder mask chemical. Use a knife or X-acto tool to remove the solder mask.



6201-7

Figure E-11 Special Tool and Method Used to Clip Ceramic IC Leads

APPENDIX F
TIMING TRACK WRITING PROCEDURE

F.1 GENERAL

The procedure for writing timing tracks on a RS03 disk is given in this appendix. This procedure should be followed if the timing tracks were destroyed.

PROCEDURE – To write timing tracks on the RS03, proceed as follows:

1. Move drive REMOTE/LOCAL switch to OFF.

2. Disconnect timing head connector (TIM) and remove Timing Amp module (G092).

3. Insert timing track writer (RS04-TA) into Timing Amp location in logic rack (AB16). Connect head connector to timing head (TIM). (The timing track writer head connector mates with the timing head in either of two directions. Either orientation is acceptable here because the following procedure is repeated with the connector in the other orientation.)

4. Move drive REMOTE/LOCAL switch to LOCAL.

5. On timing track writer, set OFF/ON switch to ON; ADJ/WRT switch to ADJ.

6. Adjust GAP ADJ pot to center of OK range as indicated by INC, OK, DEC lights.

NOTE

Pot, with its adjustment screw pointing towards the module handles, is a coarse adjust and once set, will probably not require further adjustment.

7. Move ADJ/WRT switch to center position, then depress to WRT position, once. Check that OK light remains lit.

8. Remove head connector and reinstall, turned 180° on the TIM head connector. Repeat steps 5 through 7 to write spare timing track.

9. Disconnect head connector.

10. Move OFF/ON switch to OFF; move drive REMOTE/LOCAL switch to OFF.

11. Remove timing track writer and reinstall Timing Amp module (G092).

APPENDIX G
RECOMMENDED FILTER MAINTENANCE

G.1 GENERAL

Table G-1 lists the various possible operating environments, the typical particle counts for those environments, and the recommended replacement frequency for each of the filters in the RS03.

Table G-1
Recommended Filter Maintenance

Typical Operating Environment	Typical Particle Count Particles/ft^3 $> .5\ \mu m$	Cabinet	Drive Filters		
		Filter	Pre-Filter	Blower Pre-Filter	Absolute Filter
Computer Room	1.0×10^5	Vacuum every 6 months	Vacuum clean every 6 months	Replace once per year	Replace every year
Business Office	4.0×10^5	Vacuum every 3 months	Vacuum clean every 3 months	Replace once per year	Replace once per year
Electronic Assy Area	1.5×10^6	Wash in detergent every 6 months	Wash in detergent every 6 months	Replace every 6 months	Replace once every 6 months
Machine Shop	5×10^5 (oily)	Wash in detergent or replace every 3 months	Wash in detergent or replace every 3 months	Replace every 3 months	Replace every 6 months
Steel Mill	25×10^6	These environments are too dirty for application of the drive without special air cleaning equipment.			
Auto Assy Plant	100×10^6				

APPENDIX H
RS03 DECdisk PREVENTIVE MAINTENANCE PROCEDURE

H.1 APPLICABLE OPTION DESIGNATIONS

RS03-AA	115 V, 60 Hz	Disk
RS03-AB	230 V, 60 Hz	Disk
RS03-AC	115 V, 50 Hz	Disk
RS03-AD	230 V, 50 Hz	Disk
RJS03-BA	115 V, 60 Hz	Disk and Control
RJS03-BB	230 V, 60 Hz	Disk and Control
RJS03-BC	115 V, 50 Hz	Disk and Control
RJS03-BD	230 V, 50 Hz	Disk and Control

H.2 PERIODIC PREVENTIVE MAINTENANCE SCHEDULES

Periodic preventive maintenance will be performed according to Table H-1. The disk assembly will not be taken apart and cleaned during a PM procedure unless an error condition indicates that a disk cleaning is in order, or the motor/spindle is being changed due to a mechanical fault.

The RS03 preventive maintenance schedule is unique, since there are no adjustments in the logic, one voltage adjustment, no head alignments to perform, no run-out adjustments on the platter, and the Absolute filter may be changed without disassembling the disk. The timing track writer is one module and the Error Status register is displayed by LEDs.

The subsystem filters will be checked on every PM period (Table H-1); however, filter maintenance is a function of the subsystem environment. Table G-1 lists six possible computer environments with recommended time intervals.

It is expected that the computer room and the business office environments will be most common. Vacuum cleaning and filter replacement is required at the indicated time intervals. Electronic assembly and machine shop areas require filter washing, due to a higher particle count and the possibility of oil film in the air.

CAUTION

Under no conditions is the RS03 to be operated in environments containing excessive particle counts, such as in a steel mill or auto part assembly area, unless special air cleaning equipment is installed.

H.3 EQUIPMENT AND PARTS REQUIRED

Table H-2 lists the equipment and parts needed for a "worst-case" PM situation. Normal PM should require no special parts, tools, or support kit, unless a filter needs to be changed (Table G-1). If an Absolute filter is to be replaced, the only tool required is a screwdriver.

H.4 DIAGNOSTICS

The following diagnostics are available for preventive maintenance of the RS03 DECdisk:

MAINDEC-11-DZRSB – RH11/RS03/RS04 Basic Function Diagnostic

MAINDEC-11-DZRSC – RH11/RS03/RS04 Data Reliability Diagnostic

NOTE

A system exerciser such as DECEX-11 or RSTS/E SYSTST must also be run, selecting the RS03 during overall system PM tasks.

Table H-1
RS03 Preventive Maintenance Schedule

Daily – Customer	Weekly – Customer	Monthly – Customer	Quarterly – Field Service	Annual – Field Service	Task	Est. Time (minutes)
		X	X	X	Inspect wiring and assembly	10
	X	X			Check lamps	2
			X	X	Check filters (Table G-2)	45
			X	X	Install F-Coded ECOs	30
			X	X	Check +5 V	10
		X	X	X	Run diagnostics	30

Table H-2
RS03 Preventive Maintenance Recommended
Test Equipment and Replacement Parts

Item	Mfg. Part/Drawing No.
Multimeter	Simpson, Micronta, (or equiv.)
Oscilloscope	Tektronix 453 (or equiv.)
Probes, Oscilloscope (X10)	Tektronix P6010
Probe, Oscilloscope (X1)	Tektronix P6011 (DEC 29-14050)
Flags, probe	DEC 29-15188
Flags, adapter	DEC 29-19363
Tool Kit, Field Service	DEC 29-18303
Pre-Filter	DEC 12-11255-00
Blower Pre-Filter	DEC 12-11733-00
Absolute Filter	DEC 12-10803-01
Brush Assembly	DEC 12-10659-00
Blower Fan Assembly	DEC 70-09671-00
Motor and Hub Assembly	DEC 74-09804-00
Lamps	DEC 12-09169-00
RS03 Support Kit	Field Service
Rack Filter	H950-SA
Torque Wrench, 1-30 lb/in.	Henry Mann, TS30 (7/64)

H.5 RELATED DOCUMENTATION

The following documents should be used in whole or in part in the performance of preventive maintenance:

RJS04/RJS03 Fixed-Head Disk System Maintenance Manual (DEC-11-HRJSA-A-D)

RH11 Print Set (B-DD-RH11-0)

RS03 Print Set (B-DD-RS03-0)

DEC-O-LOG

H.6 GENERAL INSPECTION

Proceed as follows:

1. Inspect the interface cables for proper strain relief.
2. Ensure that the 3M-Flat Cable connectors on the RS03 M5903 modules are seated and secure.
3. Ensure that all modules are fully seated in the RS03 logic assembly.
4. Ensure that the 3M-Flat Cable connectors on the RH11 M5904 modules are seated and secure.
5. Check the RH11 power wire tabs for wear or loose connections.
6. Check chassis bolts and screws holding major assemblies.
7. Check the spindle brush assembly for chattering or scraping noise.
8. Clean all areas of soil deposits.

H.7 DIAGNOSTIC CHECKS

H.7.1 MAINDEC-11-DZRSB, RH11/RS03/RS04 Basic Function Diagnostic

The Basic Function Diagnostic is used to verify that the controller and the drives are operating correctly. This program can test up to eight drives; the drives can be intermixed in any order. Proceed as follows:

1. Load the diagnostic.
2. Load address 200.
3. Set all switches down.
4. Start.
5. Run the diagnostic for one pass (each drive is tested during one pass).

H.7.2 MAINDEC-11-DZRSC, RH11/RS03/RS04 Data Reliability Diagnostic

The disk data test is a series of address and data reliability routines, which verify that the controller and the drives are operating correctly. Proceed as follows:

1. Load the diagnostic.
2. Load address 200.
3. Set all switches down.
4. Start.
5. Run for one pass.

NOTE

For memory sizes greater than 28K, select the Conversation Mode and memory above 28K and run for one pass.

H.8 LAMP CHECK

Status indicator lamps are accessed by removing the front status panel (refer to subsection 4.3).

H.9 FILTER CHECK

The frequency of which filters are changed, washed, or vacuumed is a direct function of the computer area environment. Table G-1 lists the four filter types found in the RS03 cabinet and specifies six different environments. Table G-1 should be referenced during every PM procedure to determine what action is to be taken with the subsystem filters (refer to subsection 4.2).

CAUTION

Visual inspection for dirty filters is not a recommended procedure.

H.10 F-CODED ECOs

Any F-Coded ECOs should be installed during each *quarterly* PM procedure.

H.11 DISK AND HEAD CLEANING

The disk surface and heads should only be cleaned when the spindle and blower motors are being changed due to a fault. The following subsections of this manual must be referenced for disk and head cleaning:

Procedure	Subsection
Upper Casting Removal	4.9
Disk Removal and Cleaning	4.9
Head Cleaning	4.8
Upper Casting Replacement	4.9
Confirmation	4.9

H.12 TIMING TRACKS

If the disk platter is removed for any reason (i.e., motor/spindle replacement, disk cleaning, etc.), the primary and alternate timing tracks *must* be rewritten. See Appendix F of this manual for this procedure.

RS03 DECdisk SERVICE MANUAL
DEC-00-HRS3A-A-D

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