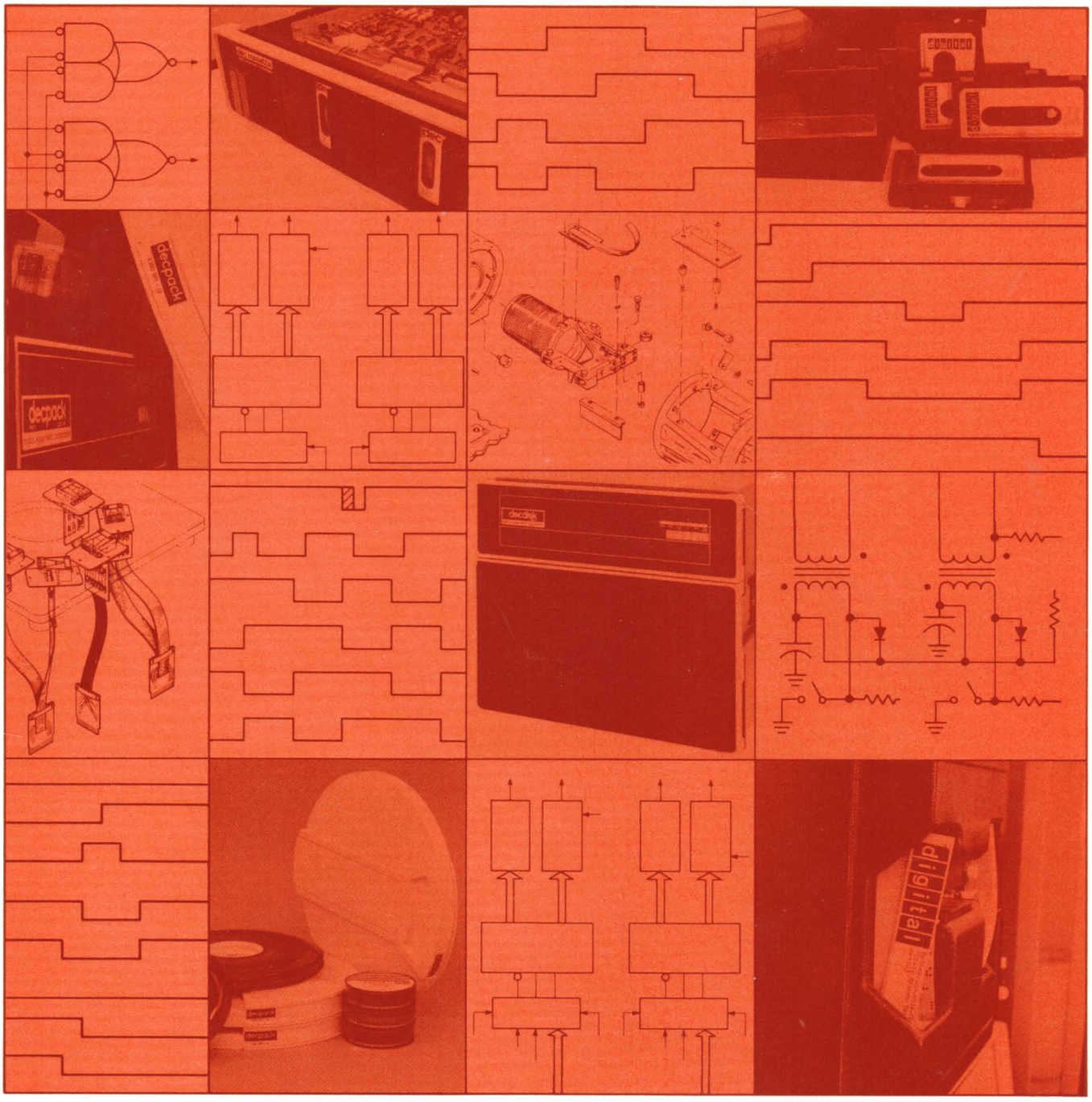
digital

2340 XOR test system maintenance manual



digital equipment corporation · maynard, massachusetts

2340 XOR test system maintenance manual

DEC-00-H2340-A-D

digital equipment corporation · maynard. massachusetts

1st Edition, June 1974

Printed in U.S.A.

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CHAPTER 1
GENERAL DESCRIPTION

1.1 SCOPE

This chapter describes the 2340 XOR Test System in general terms – its purpose and use, the unit in functional terms, and provides a brief list of general specifications.

1.2 DESCRIPTION

1.2.1 General

The 2340 XOR Test System, (Figure 1-1) is a production line automatic test system, designed to be used in both Manufacturing and Field Service applications for comparison testing of DEC FLIP-CHIP Modules. The unit utilizes the Exclusive Or (XOR) principle to compare the outputs of a "known good module" (KGM) with the identical outputs from another module of the same type that is being tested (MUT). The same input pins on both modules are simultaneously activated and their resultant outputs are then checked on a time-margined basis. The unit is intended for testing only those modules that use positive logic at standard logic levels.

6845-7

Figure 1-1 2340 XOR Test System

1.2.2 Functional

The 2340 is a stand-alone device that does not require an external computer to supply source signals. Signal generation is achieved within the tester by two modes of operation (Figure 1-2): the first is provided by pseudo-random pattern generators, the second by preprogrammed adapter cards. Timing is generated by an M405 Master Crystal Clock that controls the operation of the tester at all times.

Outputs from the two modules are strobed into the comparator by a preselected strobe. The rate and amount of delay of this strobe (or sampling period) provides a tolerance for critical timing measurements. If the output of the MUT does not coincide with the KGM during the sampling time, an error is shown on the indicator panel.

1.2.3 Mechanical

The 2340 is housed within a specially-constructed cabinet intended for bench-top use. The unit is contained within three subassemblies, each secured and hinged upon the other, providing a high degree of stability for the components while affording easy accessibility to all sections. Section accessibility is schematically illustrated in Figure 1-3. Overall cabinet dimensions are given in Figure 1-4.

Forced air cooling is supplied by two Caravelle fans, located inside the back of the unit. A separate fan is situated inside the front of the control section and supplies extra cooling for the power supplies.

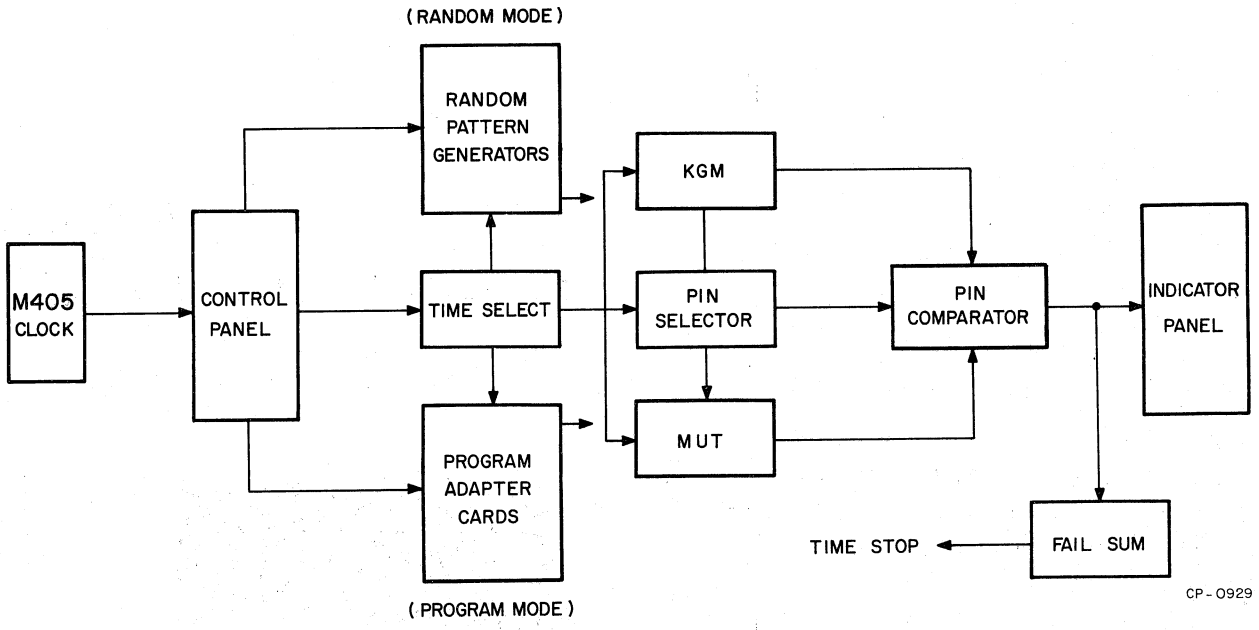

Figure 1-2 2340 Functional Block Diagram

The unit contains two power supplies: the Type H740 provides the voltages needed by the indicator lamps, the Type BKF 5-5 supplies power to the logic. A single 10-ft power cord, terminated in a NEMA Type 5-15P power plug and a DEC Power Control H400-A, connects ac power to the unit.

The test head consists of 2 H851 Module Slot Connectors, 1 for the KGM and 1 for the MUT. These are double-height connectors so that double-height modules can be accommodated. Single-height modules are tested in the left-hand side of each head. The slots on each connector are connected in parallel to allow testing in any position.

Three BNC connectors, described in Table 4-1, may be used for scoping during troubleshooting procedures on a defective module.

The unit contains the following module complement. Figure 1-5 shows the Module Utilization Chart for the 2340 Test System.

1.3 GENERAL SPECIFICATIONS

Physical

Height: 17-1/2 in.
Width: 19-3/4 in.
Length: 25-1/2 in.

Environmental

Temperature Range: +40° to +210° F
Humidity: 10 to 95% Relative (no condensation)

Power Requirements

AC

Frequency: 47 to 63 Hz Single Phase
Voltage: 95 to 130 V

DC

Indicators: Supplied by self-contained Type H740 Power Supply

Logic: Supplied by self-contained Type BKF 5-5 Power Supply

Performance

Test Cycle Time (Random Mode): 25 sec (approx.)
Range of Testing Speeds (Module): dc to 10 MHz
Testing Capacity: 100 module types are implemented
Type of Testing Fixture: 2 Type H851 Module Slot Connector Blocks

Logic Input Requirements
Logic Type: Positive
Logic Levels: Gnd = (0) +3 = (1)

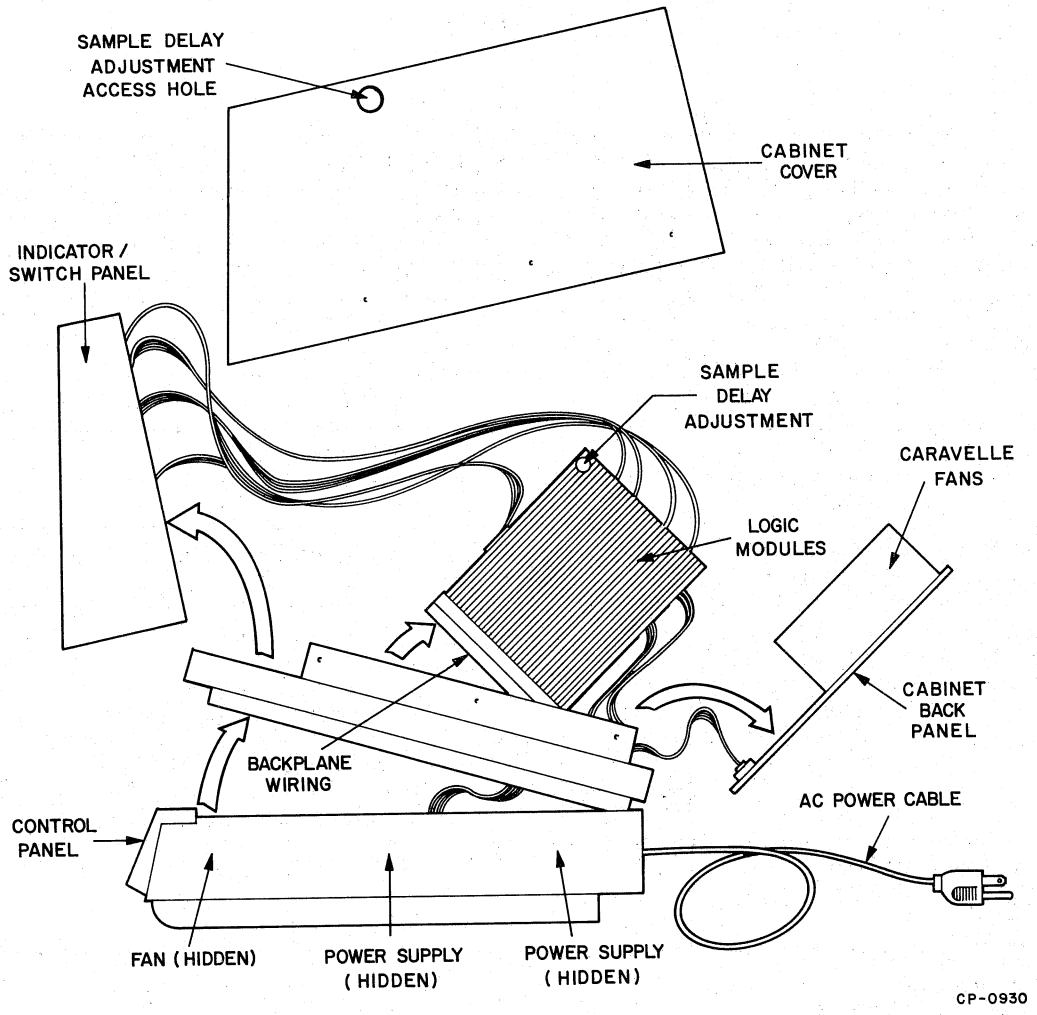

Figure 1-3 2340 Access Schematic

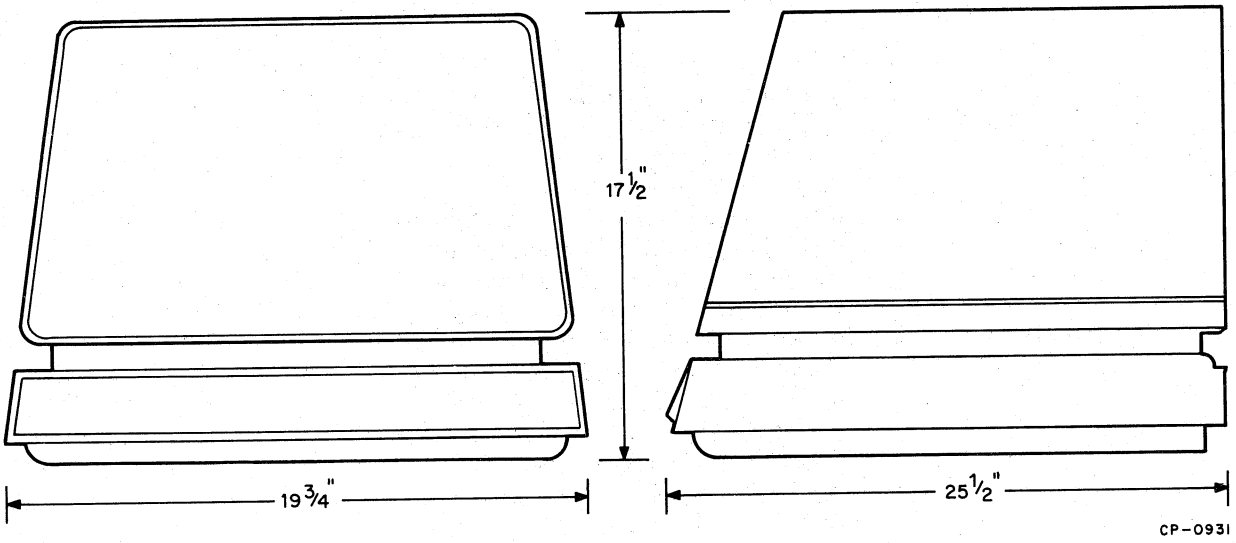

Figure 1-4 2340 Overall Dimensions

	F	E	D	C	B	A
14	M908B KGM A FROM A4 HEAD	M908B KGM B FROM C4 HEAD	G752 KGM A FROM A1 HEAD	G752 KGM B FROM B1 HEAD	G752 MUT A FROM C1 HEAD	G752 MUT B FROM D1 HEAD
13	M908B MUT A FROM B4 HEAD	M908B MUT B FROM D4 HEAD	G751 KGM A FROM A1 HEAD	G751 KGM B FROM B1 HEAD	G751 MUT A FROM C1 HEAD	G751 MUT B FROM D1 HEAD
12	M405 CLOCK	M908B MAJOR FUNC.	G5001 PIN SELECTOR			
11	M9002 TO J1 PANEL		G5002 COMPARATOR #3			
9	M9002 TO J2 PANEL		G5002 COMPARATOR #2			
8	M9002 TO J3 PANEL		G5002 COMPARATOR #1			
7	G750 KGM A TO A2&A3 HEAD	G750 KGM B TO B2&B3 HEAD	G5007 ADAPTER INTERFACE			
6	G750 MUT A TO C2&C3 HEAD	G750 MUT B TO D2&D3 HEAD	G5006 RANDOM ADAPTER			
4	M9002 TO J4 PANEL		G5005 RANDOM GENERATOR #3			
3	M9002 TO J5 PANEL		G5004 RANDOM GENERATOR #2			
2	M9002 TO J6 PANEL		G5003 RANDOM GENERATOR #1			
1	M908B & TEST ADAPTER CLOCK RATE	M908B SAMPLE RATE	G5000 SUMMATION & TIMING			

FROM PANEL
FUNCTION SWITCHES

Figure 1-5 2340 Module Utilization

1 M405 Crystal Clock Module
6 M908B Ribbon Cable Connector/Terminator
6 M9007 Bus Terminators
4 G750 Interface Connector Modules
4 G751 Interface Driver Connector Modules
4 G752 Interface Driver Connector Modules
1 G5000 Summation and Timing Module
1 G5001 Pin Selector Module
3 G5002 XOR Comparator Modules (#1, #2, #3)
1 G5003 Random Generator Module #1
1 G5004 Random Generator Module #2
1 G5005 Random Generator Module #3
1 G5006 Random Adapter Module
1 G5007 Adapter Interface Module
1 G5008 Indicator Board
6 M9002 Ribbon Connector Cable Module

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains installation procedures for the 2340 XOR Test System, including instructions on how to unpack the unit, and how to reinstall those unit components that were removed prior to shipment to ensure their safety. Included are checks that can be made once the System is reassembled to verify its proper operation, and tests that can be made to validate its acceptance by the user.

2.2 SPACE REQUIREMENTS

The 2340 should be operated in an atmosphere relatively free of dust and corrosive fumes. The frequency of maintenance schedules is determined by the ambient operating conditions.

The degree of heat radiated by the equipment is relatively low and has no effect on the air conditioning requirements at the site.

The unit should be operated on a bench, providing proper support and power source, with sufficient space for auxiliary test equipment required when troubleshooting modules. It is recommended that the system be located in the module test area.

2.3 POWER REQUIREMENTS

As listed under General Specifications (Paragraph 1.3), the 2340 is powered from a standard 3-wire, single-phase power line, properly fused to accommodate the added load it imposes. The required receptacle is a NEMA Type 5-15R, as illustrated in Figure 2-1. The unit should never be operated through a "zip-cord" type power extension, and it should never be powered from the accessory receptacle of another piece of auxiliary test equipment. Serious ground loops can be set up by this practice that could affect the accuracy of test indications.

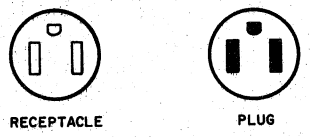

Figure 2-1 2340 Power Plug and Source Receptacle

The 2340 Test System operates on ac voltages ranging from 95 V to 130 V. When inserted into a properly wired outlet, the third prong grounds the cabinet.

WARNING

It is dangerous to operate the tester without this ground connection.

If the integrity of the ground connection is questionable, the user is advised to measure the potential between the tester cabinet and a known ground with an ac voltmeter. If a potential exists, the circuit must be corrected before operating the tester.

2.4 UNPACKING AND INSPECTION

The 2340 XOR Test System is packed in a specially designed shipping container to prevent damage during shipment. Observe any cautions printed on the container before unpacking the equipment. Proceed as follows:

1. Move the equipment, in its container, to the location in which it is to be used; then remove.

2. Save all shipping materials and the carton.

3. Remove the shipping document, affixed to the outside of the shipping carton; check it against the materials received.

NOTE
Any shortages should be noted and reported immediately to the DEC Field Service Representative.

4. Inspect the equipment for any obvious dents, scratches, or other shipping damage. Report this to the Field Service Representative.

5. Remove any polyethylene covers and/or tape from the equipment; remove any shipping hardware. Save this material.

6. Perform the checks listed in Paragraph 2.5.

2.5 CHECKOUT AND ACCEPTANCE TESTS

Once the 2340 is unpacked and installed in its operating position, the procedures listed below should be followed to checkout and assure acceptance of the equipment. The following equipment is required for these procedures:

Tektronix 454A (or equivalent) oscilloscope
Two known good modules (M115)
Simpson 260 Voltohmeter
W984A Module Extender Board

Proceed as follows:

1. Using a multimeter, perform a continuity test of the power wiring and check for shorts to ground on the +5 V line.

2. With no modules installed in any mounting frames, turn on the main power supply and check the +5 V line.

3. Remove power and install modules per the module utilization shown in Figure 1-5.

4. Reapply power and check once again for any shorts.

5. Push RESET button. All lights should extinguish.

6. Set TEST RATE switch to position 1. Set ADAPTER CLOCK switch to position 1. Set SAMPLE RATE switch to position 4. Press START; in approximately 13 seconds the INIT light should indicate.

7. Turn on the +5 Vdc.

8. Some lights may indicate. These are erroneous and should be extinguished by pushing RESET.

9. On the G5000 module, put the scope probe on E42-3 and verify the rates, listed in Table 5-2, by rotating the TEST RATE switch through its positions.

10. On the front panel, connect the scope to the CLOCK BNC connector and verify the rates, listed in Table 5-1, by rotating the ADAPTER CLOCK switch through its positions.

11. On the front panel, connect the scope to the S RATE BNC connector and verify the rates, listed in Table 5-3, by rotating the SAMPLE RATE switch through its positions.

12. Plug two modules into the KGM and MUT test heads and verify the +5 Vdc line.

13. With the modules in place, verify the ground line.

14. With the modules in place, place all 66 front panel switches in neutral position; using the scope, verify random signals on all pins, except V_{cc} and ground pins.

15. With the modules in place, check corresponding pins (pin AA1 on the MUT side and pin BA1 on the KGM side). Place switch AA1 in UP position, and in the NEUTRAL and DOWN positions. Verify that pins correspond by observing the following:

Switch Position	Signals on AA1 and BA1
UP	0 Vdc
NEUTRAL	Random Signal
DOWN	+5 Vdc

16. Repeat step 15 for all corresponding KGM and MUT pins.

17. Remove the modules, and on a W984A extender card, tie all pins together *except* V_{cc}. Plug the W984A card into the KGM test head only. *All* KGM lights should indicate. This verifies all comparators and lights.

18. Repeat step 17 by plugging the W984A card in the MUT Test Head only. This verifies all comparators and lights. Remove the W984A card and plug the module into the MUT side.

19. Set the oscilloscope on internal trigger and place the probe on pin AA1. Check that the rise and fall times appear as in Figure 2-2.

20. Place sync probe on KGM pin AA1. On G5000, place the other probe on either E43-8, E43-6, or E43-4. Adjust SAMPLE RATE DELAY to match the waveform in Figure 2-3.

21. Using the 2340 Test Procedure for M115, supplied as a separate document, set switches as indicated.

22. Press RESET. All erroneous panel lights should extinguish.

23. Press STOP. PAUSE should indicate and RUN should extinguish.

24. Insert an M115 in the KGM Test Head and an M115 in the MUT Test Head.

25. Press CONTINUE. PASS should indicate and RUN should light.

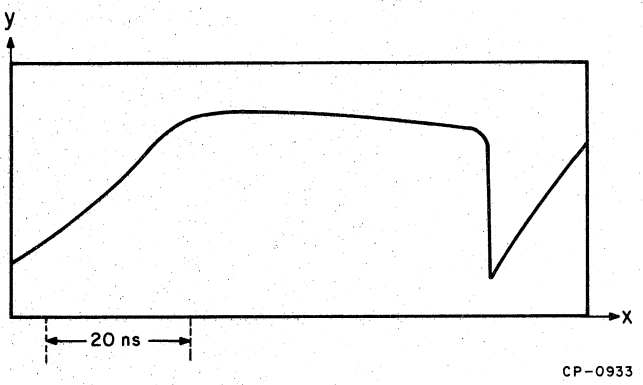

Figure 2-2 MUT pin AA1 Rise Time

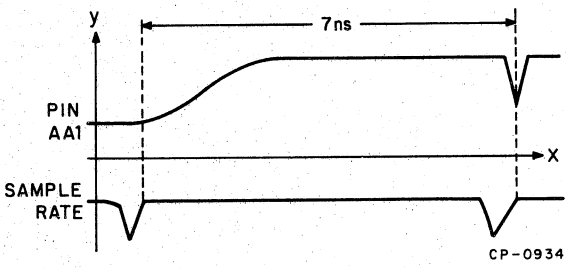

Figure 2-3 Sample Rate Adjustment

26. On the MUT module, ground pins AA1, AM1, AE2, AK2, AP2, and AU2. The FAIL light should indicate and RUN should blink. The error indicators for the grounded pins should indicate.

27. Push both RESET and STOP. Turn off POWER and remove the modules. The procedure is complete.

CHAPTER 3
PROGRAMMING

3.1 GENERAL

Although the 2340 XOR Test System requires no programming in the traditional sense, it does require the use of *Programmed Adapter Cards.* These cards must be fabricated for each type module to be tested when the unit is operated in the Program Mode. This mode is used to test those modules containing clocks or oscillators, etc. that cannot be tested in the Random Mode.

3.2 TYPICAL PROGRAM ADAPTER

Figure 3-1 is a block diagram of a typical module to be tested in Program Mode (M249 Bus Register). Figure 3-2 illustrates an adapter to be built for testing this module; Figure 3-3 shows the adapter timing signals.

Similar cards can be constructed for other modules.

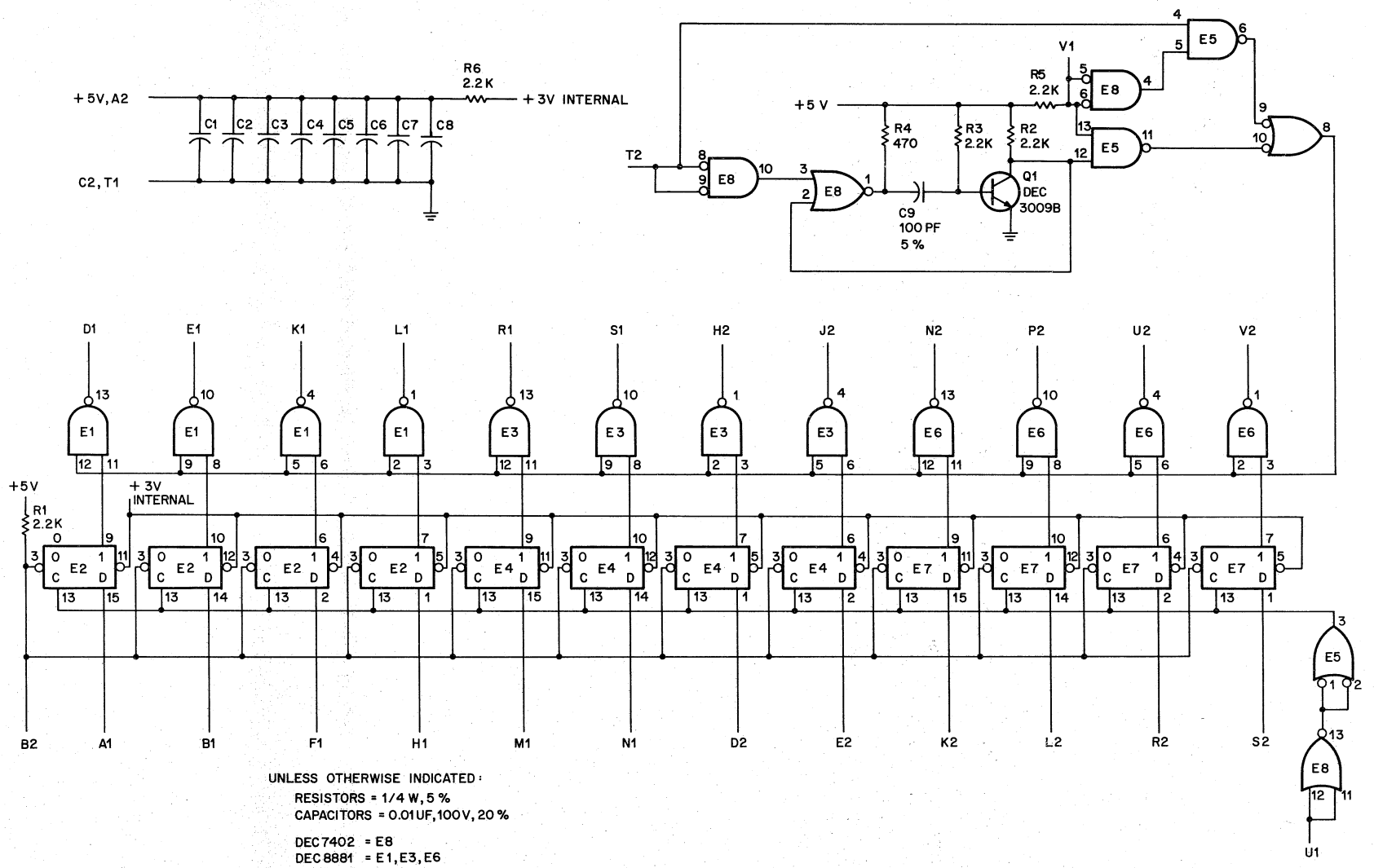

Figure 3-1 Typical Program Mode Module

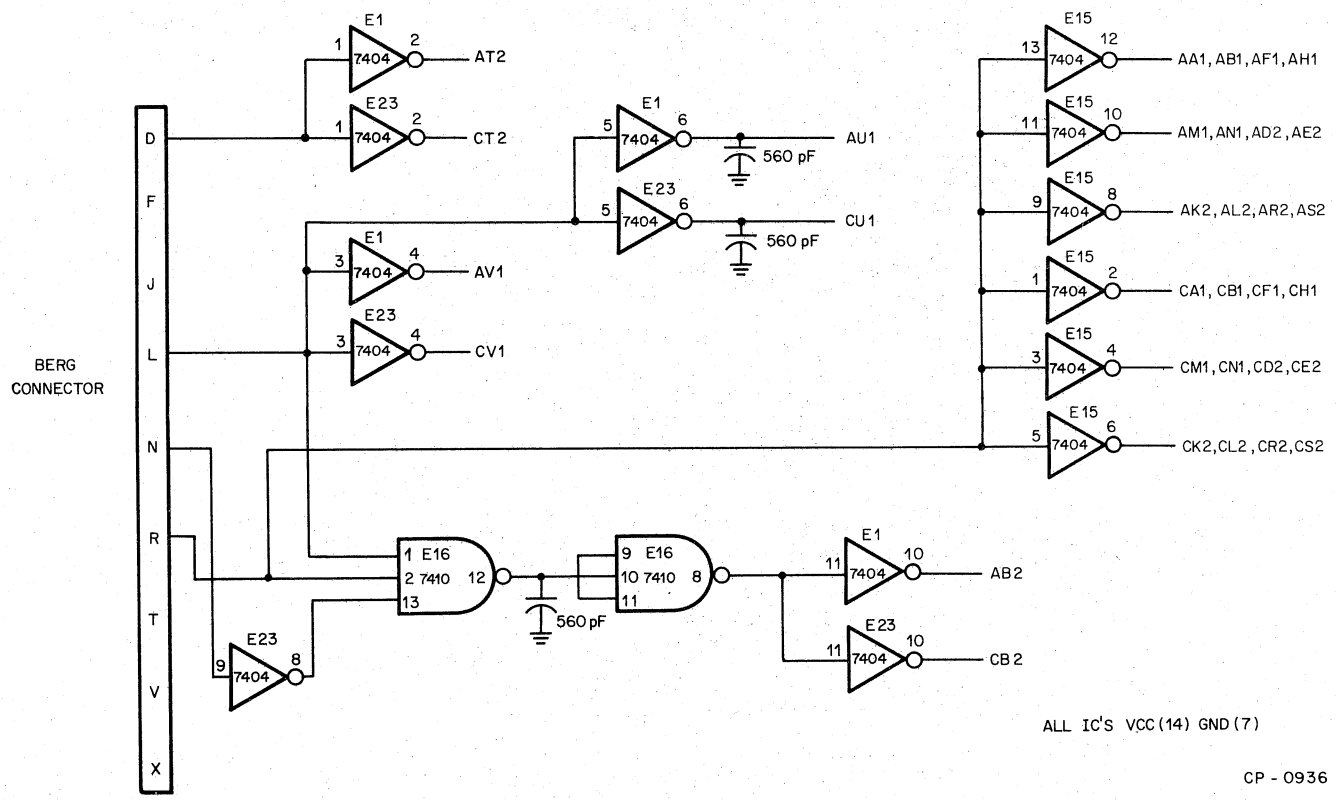

Figure 3-2 M249 Adapter

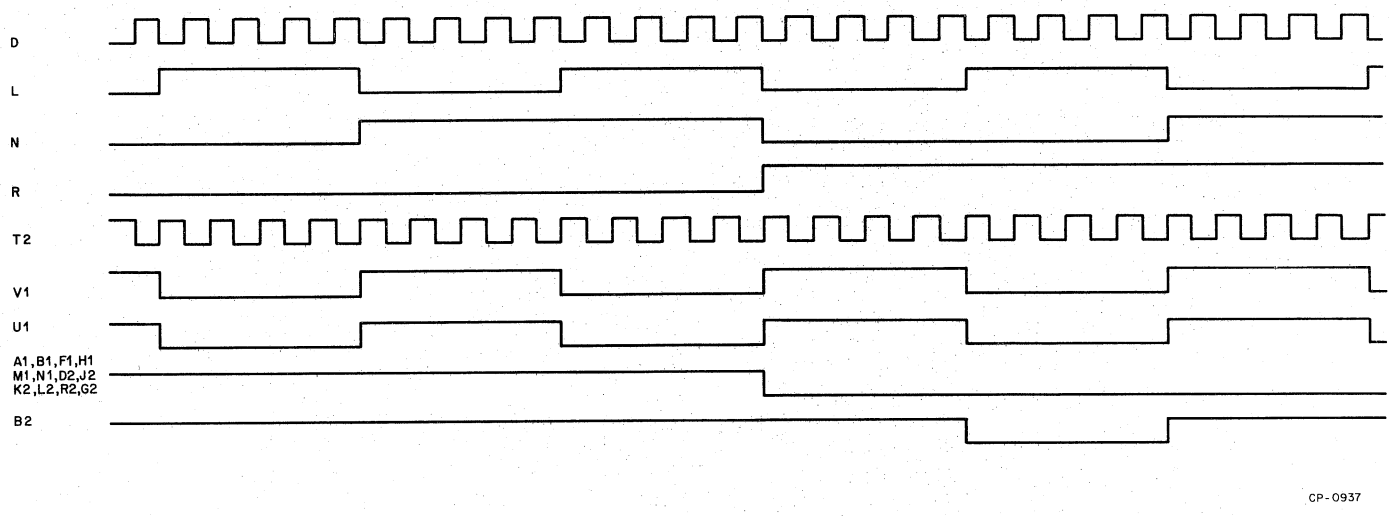

Figure 3-3 M249 Adapter Timing

CHAPTER 4
OPERATION

4.1 SCOPE

This chapter discusses the operation of the 2340 XOR Test System. It contains a description of the controls and indicators used on the equipment with a tabular listing and description of each control in functional terms. The chapter also contains operational procedures to be used with the equipment and a description of its use as a maintenance tool.

4.2 CONTROLS AND INDICATORS

The controls and indicators for the 2340 XOR Test System are all located on the front panel of the unit (Figure 4-1). The functions of each control and indicator are listed in Table 4-1 as keyed to Figure 4-1.

Table 4-1
2340 Controls and Indicators

Index No.	Function
1	HIGH/NEUTRAL/LOW – 66 3-position toggle switches, each pertaining to a pair of comparable module pins on both KGM and MUT, that apply either a high (output) or low level to that pin, or leave it open (Neutral) for pattern activation. For use with Random Mode of testing.
2	AA1 - BV2 – 66 indicators, 1 for each testable pin on the modules. Each indicator bears a one-to-one positional relationship with its associated indicator. These indicators light whenever a lack of comparison is found for any comparable set of pins on KGM and MUT.

Table 4-1 (Cont)
2340 Controls and Indicators

Index No.	Function
3	TEST RATE – An 11-position rotary switch. By rotating this switch, a specific Test Clock Rate is applied to the Pin Selector and Adapter Interface. Determines the rate at which the output pins of KGM and MUT are tested in relation to the same rate of enablement of their input pins.
4	ADPT CLOCK – A 12-position rotary switch. By rotating this switch, a specific Adapter Clock Rate is applied to the Random Pattern Generator and to the Adapter Interface. Drives shift register generators.
5	SAMPLE RATE DELAY – A potentiometer adjustment (available through side panel). In conjunction with SAMPLE RATE rotary switch, moves the testing window to conform to the speed of the data.
6	SAMPLE RATE – A 24-position rotary switch. By rotating this switch, a specific sampling window is applied to the sample delay circuit for application to the pin comparators. In conjunction with this adjustable delay, the specific window can be moved through the duration of test rate in the comparators. Determines the particular portion of the output signals from KGM and MUT that will be used for comparison and evaluation.

Table 4-1 (Cont)
2340 Controls and Indicators

Index No.	Function
	NOTE **The following 3 entries are front panel BNC connectors. They are not controls or indicators, but provide convenient scoping references in the use of the equipment for troubleshooting.**
7	SYNC – This is a return sync pulse from the Program Adapter Card, used as an oscilloscope clocking source for troubleshooting a defective module.
8	CLOCK – This is a copy of the Adapter Clock Rate as set by the front panel switch for use in troubleshooting.
9	S RATE – Same as above, only Sample Rate.
10	POWER – Momentary Close Pushbutton – Applies ac power to the 2340 power supplies, and dc power to the 2340 logic. Does not apply dc to the KGM and MUT.
11	+5 – Momentary Close Pushbutton – Applies dc power to the KGM and MUT, if POWER has been pushed.
12	RUN – Indicates that a test is running in either Program or Random Mode. Lights when initialization has been achieved and START is pushed, in Random Mode. In Program Mode, lights if START is pushed, or, if in Single Step operation, lights momentarily whenever SINGLE STEP is pushed. Will blink if a FAIL condition exists.
13	START – Momentary Close Pushbutton – Causes testing to either start after initialize or to resume after it has been interrupted.

Table 4-1 (Cont)
2340 Controls and Indicators

Index No.	Function
14	STOP – Momentary Close Pushbutton – Causes testing to stop at whatever point it is situated.
15	MODE – SPDT toggle switch – In PROGRAM position, if the Program Adapter Card is inserted into slot A-D-6, testing will be conducted in a sequential manner as controlled by the Pin Selector. In RANDOM position, if the Random Adapter Card is inserted into slot A-D-6, testing will be conducted in psuedo-random fashion, as determined by the Random Generator.
16	TRT – SPDT toggle switch – In AUTO position, testing progresses at the rate determined by the Test Clock. In SINGLE STEP position, testing is stepped by the SINGLE STEP pushbutton.
17	INIT – Momentary Close Pushbutton – When depressed, causes the synchronization of the 3 Random Generators. When accomplished, the INIT indicator will light.
18	ERROR – DPDT toggle switch – In STOP position, testing automatically stops on error. In BYPASS position, testing will not stop on error, but errors will accumulate in the error indicators. Functions in Program Mode.
19	SINGLE STEP – Momentary Close Pushbutton – Causes testing, for troubleshooting purposes, to progress one pin for each press of this button, when TRT switch is placed in SINGLE STEP position. Functions in Program Mode.
20	ERROR RESET – Momentary Close Pushbutton – Negates the error condition, causes any error indicators to extinguish. If in "Error Stop" condition, causes testing to resume, the FAIL indicator to extinguish, and the PASS indicator to light. Functions in this manner in Program Mode.

Table 4-1 (Cont)
2340 Controls and Indicators

Index No.	Function
21	ERROR STOP – Indicates that the test cycle has been halted by an error condition, if the ERROR switch is in the STOP position.
22	FAIL – Indicates at the end of a cycle of tests, in Program Mode, if an error has been sensed on any set of pins.
23	INIT – Lights whenever the 3 Random Generators have reached synchronism and are now ready to be used for testing.
24	PASS – In Program Mode, indicates at the end of a cycle of tests that has sensed no errors. In Random Mode, will light *until* an error is sensed.
25	PAUSE – Indicates that testing has been interrupted as a result of having pressed the STOP button.

4.3 OPERATING PROCEDURES

There are two procedures for using the 2340 XOR Test System: One when in Random Mode, used for most modules, and one when in Program Mode, used to test those modules that cannot be tested in Random Mode (e.g., those containing clocks).

4.3.1 In Random Mode

In this mode, the MODE switch should be positioned to RANDOM, a Random Adapter (G5006) must be installed in slot A-D-6, and the Random Generator must be initialized before testing can commence. Proceed as follows:

1. Press POWER. All pin error indicators will light.
2. Press ERROR RESET to extinguish lights.
3. Insert KGM in the left-hand test head and MUT in right-hand test head.
4. Position the HIGH/NEUTRAL/LOW switches (per the block schematic) for the type module being tested, e.g., set switches associated with output pins to their HIGH positions. Switches associated with input pins should be set to the NEUTRAL position. To disable any pin, set its switch to the LOW position. Set the TEST RATE, ADAPT CLOCK, and SAMPLE RATE switches to their desired positions.

NOTE
The ERROR and TRT switches and the SINGLE STEP button are inoperative in this mode.

5. Press the +5 button to power the modules. The button will light.
6. Press INIT. Some error lights may come up along with FAIL on the first error; these indications should be ignored.
7. In about 3 seconds, the INIT lamp should light. At this time, press ERROR RESET to extinguish the erroneous error indications generated by the initialization process. The FAIL lamp should also extinguish.
8. When ready, press START. The PASS light should come on and RUN should indicate.
9. Upon the first error indication, PASS will go out and errors will accumulate in the indicators.
10. The generator will continue to run indefinitely.
11. When the desired test period has elapsed, press STOP. The RUN lamp will extinguish, the PAUSE indicator will light, and testing will cease. The same will hold true if testing is stopped and then restarted.
12. At this point, either commence troubleshooting procedures, if errors were detected, or, if the tester is being used to test many modules, record the errors encountered and proceed with testing the next module.
13. Turn off the +5 V by depressing the +5 button. The +5 button light will extinguish.

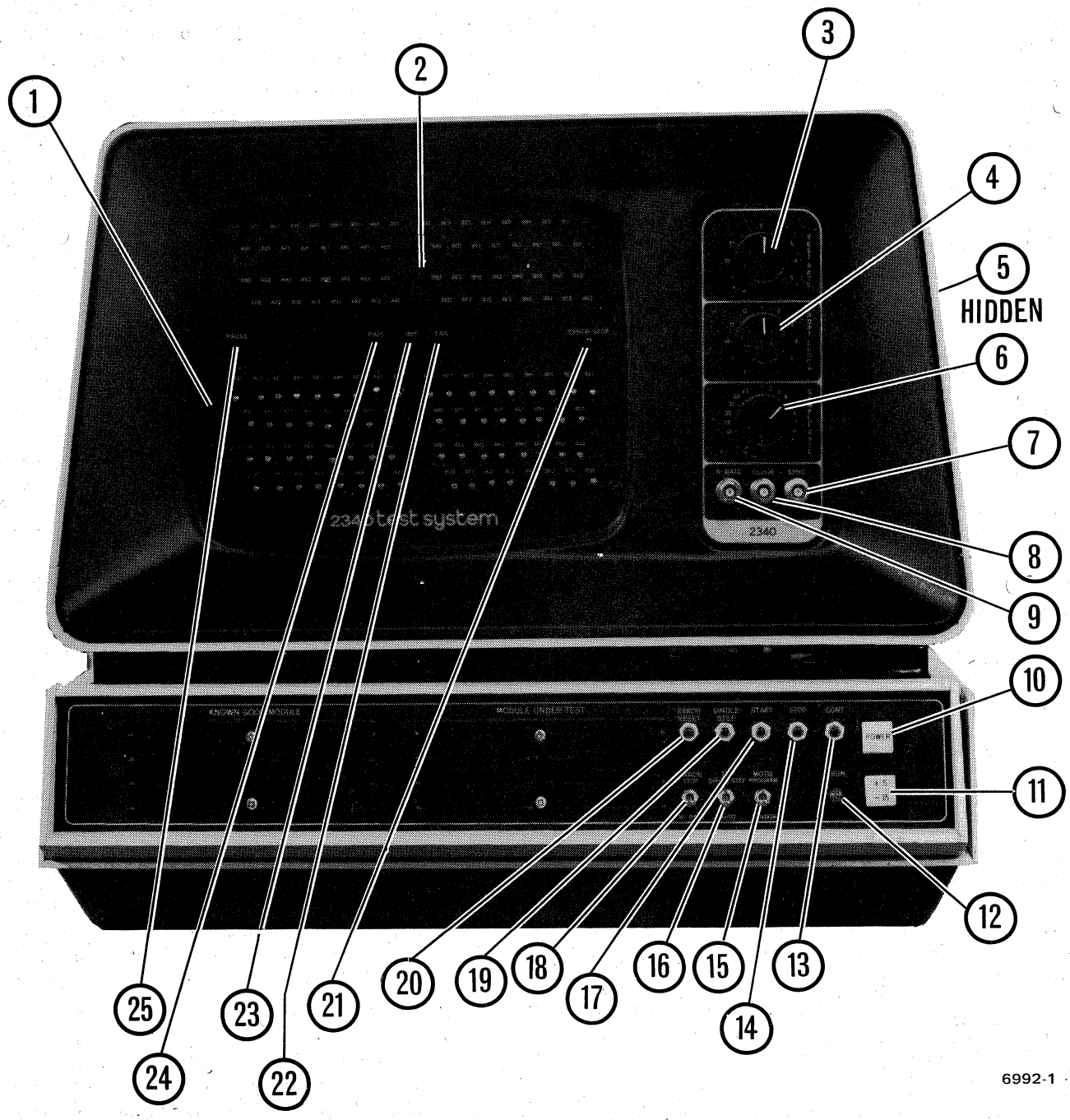

Figure 4-1 2340 XOR Test System Controls and Indicators

14. Insert the next module and press +5.

15. Repeat the procedures in steps 4 through 13.

4.3.2 In Program Mode

In this mode, the MODE switch should be positioned to PROGRAM; a specially fabricated Program Adapter Board must be installed in slot A-D-6 (Paragraph 3.3). Proceed as follows:

1. Press POWER. All pin error indicators will light.

2. Press ERROR RESET to extinguish lights.

3. Insert KGM in the left-hand test head and MUT in the right-hand test head.

4. Set the TEST RATE, ADAPTER RATE, and SAMPLE RATE switches to their desired positions. Set SAMPLE RATE DELAY adjustment to its mid-point.

5. Press +5 to power the modules. The button will light.

6. Set the ERROR switch to STOP position, if it is desired to have the tester stop on each error, and to BYPASS position if not.

7. Set the TRT switch to SINGLE STEP position, if it is desired to manually control progress of the tests, and to AUTO position if not.

NOTE

The HIGH/NEUTRAL/LOW switches are inoperative in this mode.

8. Press START. The RUN indicator will come on. Any error indications will come up in sequence during the test cycle. If TRT is in AUTO position, and if ERROR is in STOP position, the tester will stop on every error; the ERROR and PAUSE indicators will come on and the RUN lamp will extinguish. If ERROR switch is in BYPASS position, the tester will not stop on an error, but the indications will accumulate.

9a. If in ERROR STOP condition, press ERROR RESET to proceed. The pin error and ERROR indications will go out and RUN will come on. If it is desired to interrupt testing, press STOP. All indications will be the same; when ready, press START.

9b. If in ERROR BYPASS condition, the error indications will accumulate; when the last pin is tested, testing will cease. RUN will extinguish; if any errors are indicated, the ERROR indicator will be on and the FAIL lamp will light. If no errors are indicated, the PASS lamp will come on.

10. If the TRT switch is in SINGLE STEP position, all the above conditions will still be true, but testing will proceed one pin for each press of the SINGLE STEP button.

NOTE

If a second test cycle is desired, press START and the test will recycle.

11. At this point, either commence troubleshooting procedures, if errors were detected, or if the tester is being used to test many modules, record the errors encountered and proceed with testing the next module.

12. Press +5 to remove power from the modules and remove the MUT. The +5 button will extinguish.

13. Insert the next module and press +5.

14. Repeat the procedures in steps 6 through 13.

NOTE

A specific Program Adapter Card must be used for each specific type module.

4.4 USE OF THE 2340 AS A MAINTENANCE TOOL

The 3 BNC connectors on the front panel can be used separately, or in conjunction, to trigger oscilloscope traces, allowing observation within those time frames. While the board inputs are activated as slowly as by "Single Stepping", the outputs of those boards, as well as the intervening logic, can be examined.

In addition, when in Random Mode, the various pin outputs of the Random Generators are available on "Over Top Connector" boards as part of the logic assembly within the unit. These can also be used to sync testing equipment in the process of isolating problems.

NOTE

It is impossible to test modules used in the 2340 with the 2340 Test System.

Table 4-2
Auxiliary Test Equipment and Troubleshooting Aids

Equipment	Manufacturing Part/Drawing No.
Oscilloscope (dc to 150 MHz)	Tektronix Type 454
Probes (X10)	Tektronix Type P6054
Integrated Circuit Extender	DEC 29-10246
Pulse Generator	Datapulse 101
Multimeter	Triplett Model 310
Digital Voltmeter	John Fluke Model 8100

Typical module types to be tested in Program Mode include registers such as the M249, illustrated in Chapter 3. Analog modules, and modules containing clocks or oscillators should be tested in this mode also.

Typical module types to be tested in Random Mode include the M111, M113, and M115.

Standard troubleshooting techniques can be used to isolate problems in modules under test. Isolation of a point of failure can be accomplished by comparing the same pin on the KGM and MUT cards, on a 2-channel oscilloscope, with 1 channel inverted. By adding the 2 inputs, a straight line is seen for a condition of comparison (no failure); a difference signal will be seen if a problem exists.

CHAPTER 5
THEORY OF OPERATION

5.1 SCOPE

This chapter is devoted to the theory of operation of the 2340 XOR Test System. It describes the equipment from a theoretical standpoint, describing the underlying principles used in its design. The equipment is discussed from both a functional block diagram level and a detailed logic level. The discussion does not go to the gate-chasing point, but rather describes the operation of the various sections of logic to the degree necessary to afford competent maintenance of the equipment. It is assumed that the reader is familiar with basic logic operation and with the various standards of symbology and drawing practices utilized by DEC.

5.2 BASIC XOR PRINCIPLE OF TESTING

The basic logic element on which the entire system operation depends is the Exclusive OR gate, in which an output will be seen if its inputs differ, but will not be seen if its inputs are the same. One of these gates is assigned to each output pin of both modules. The gate outputs are fed to front panel lights and to a summation circuit that in turn can be utilized to control the progress of the tests.

5.3 FUNCTIONAL BLOCK DIAGRAM DISCUSSION

5.3.1 General

In the 2340 Test System, each output pin of the MUT is compared, on an XOR basis, with the same output pin of the KGM, since the same input pin on both modules is simultaneously activated. The rate at which the inputs are activated, the rate at which the outputs are observed, and the duration of the output observation are all controllable by front panel switches. The switches select discrete repetition rates, which are functions of one master system clock module (M405) and apply these rates to the proper sections of the system.

The manner in which the input pins of the modules are activated is determined by two modes of operation. Random Mode (Figure 5-1) is the mode of operation used for most testing. In this mode, the pattern of activation is controlled by Random Generators that output a pseudo-random cyclic binary sequence. Program Mode (Figure 5-2) is used to test only those modules that cannot be tested in random fashion. In this mode, input activation is performed in a straight sequential manner, on a pin-for-pin basis.

As can be seen by comparing the block diagrams in Figures 5-1 and 5-2, most of the hardware is used in both modes. The difference lies in the fact that when testing in Program Mode, the Random Adapter module must be replaced by a specially fabricated Program Adapter Card, and the front panel MODE switch must be placed in the PROGRAM position.

5.3.2 Random Mode Operation

The 2340 Test System utilizes an M405 Crystal Clock Module as a master clock that is fixed at 10 MHz (Figure 5-1). This clock is then divided by 2 28 times to provide 3 sets of pulse periods to 3 rate selectors.

The rate selector logic consists of sets of dual-input ORs whose inputs AND a particular pulse rate with a specific front panel switch position. These rates are given for each switch and switch position in Tables 5-1, 5-2, and 5-3.

The ADAPTER CLOCK SELECT provides 12 rates between 800 ns and 3.34 seconds. These are used to drive the Random Generators and effectively control the speed of activation of inputs.

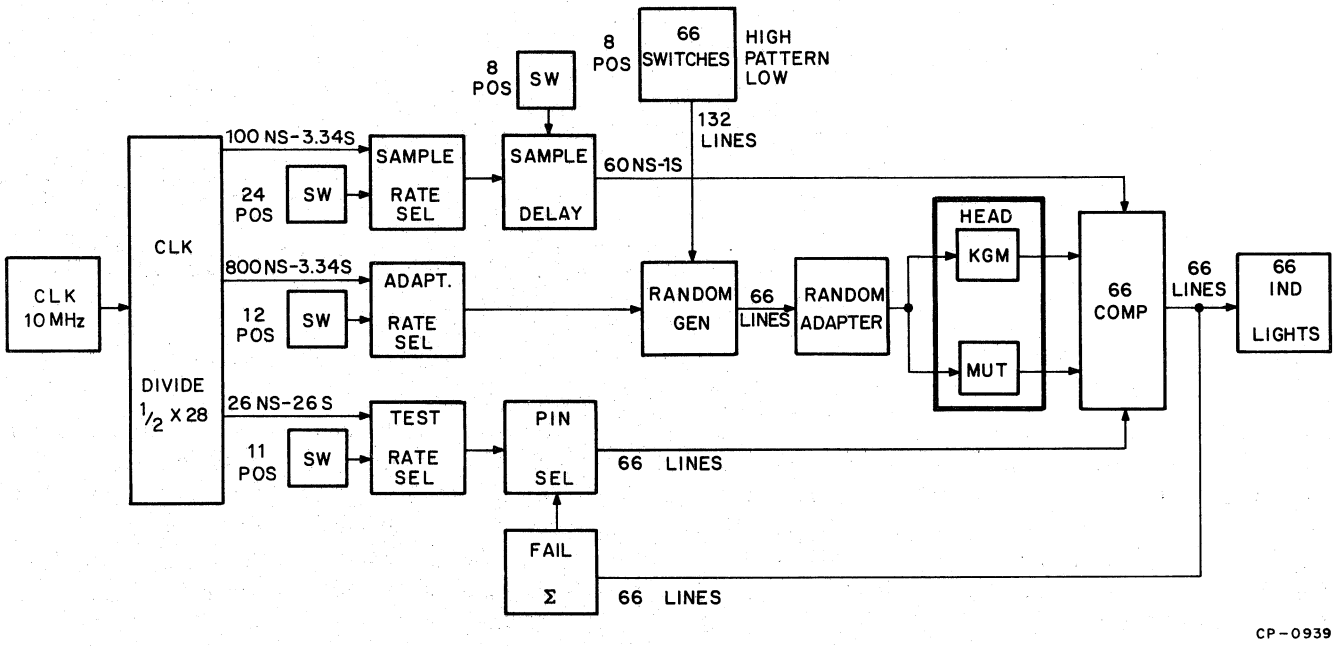

Figure 5-1 2340 Random Mode Functional Block Diagram

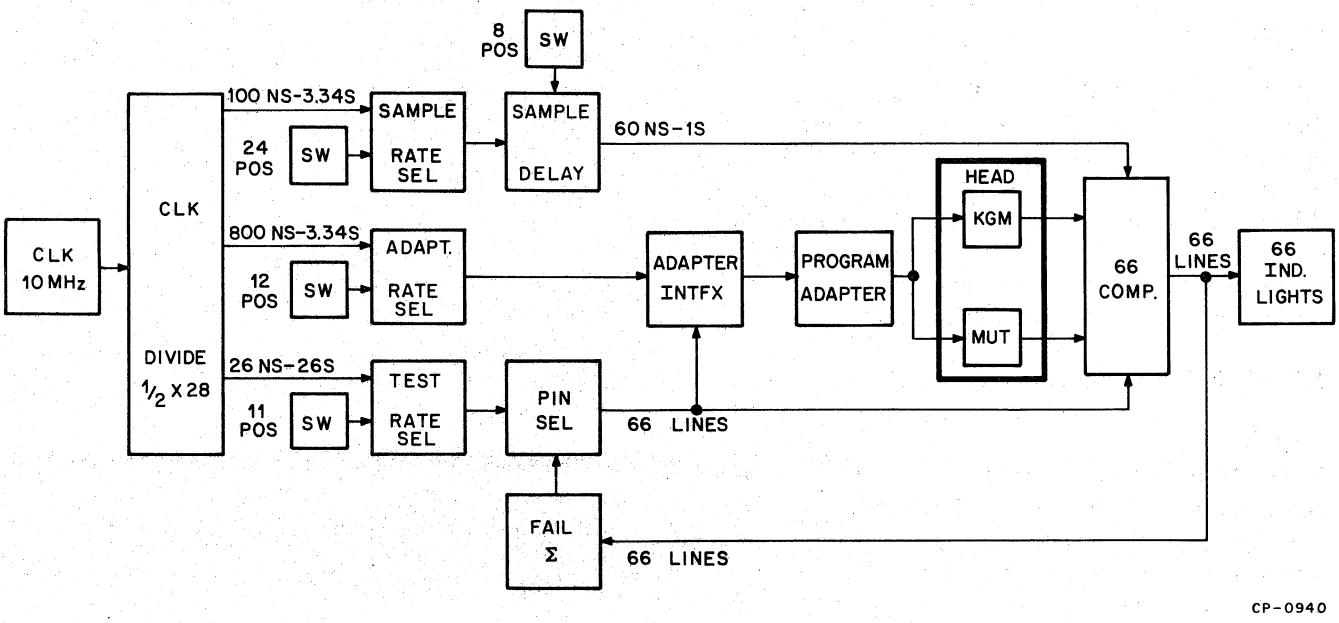

Figure 5-2 2340 Program Mode Functional Block Diagram

The TEST RATE SELECT (12 values between 26 ms and 26 seconds) is used in this mode to shift 1s into the shift register (Pin Selector) which in turn enables all the comparator gates on the output pins so that output observation can be made in accordance with the random input.

Table 5-1
Adapter Clock Select
Position/Rate

Position	Period
1	800 ns
2	3.2 μs
3	12.8 μs
4	51.2 μs
5	204 μs
6	819 μs
7	3.2 ms
8	13.04 ms
9	52 ms
10	208 ms
11	834 ms
12	3.34 sec

The SAMPLE RATE SELECT sets one of 24 rates between 100 ns and 3.34 seconds and determines the observation speed of outputs from both modules. The selected rate is fed through a SAMPLE RATE DELAY ADJUST. This is an R/C network that determines the duration of each observation. The adjustment is made by a potentiometer that controls the width of this sampling "window" and is adjusted to conform to the speed of the data (1 kHz – 10 kHz).

Table 5-2
Test Rate Select
Position/Rate

Position	Period
1	26 ms
2	52 ms
3	104 ms
4	208 ms
5	417 ms
6	834 ms
7	1.67 sec
8	3.34 sec
9	6.68 sec
10	13.3 sec
11	26.7 sec

The 2340 uses feedback shift register generators to produce a binary sequence of pseudo-random numbers. In this arrangement, the shift registers, on a clocking signal, accept an input value into their first stages. With each successive clock, this value is shifted through the individual register. The value in stage X_i moves to stage X_i+1; the value in X_i+1 moves to stage X_i+2, etc.

Table 5-3
Sample Rate Select
Position/Rate

Position	Period
1	100 ns
2	200 ns
3	400 ns
4	800 ns
5	1.6 μs
6	3.2 μs
7	6.4 μs
8	25.6 μs
9	51.2 μs
10	102 μs
11	204 μs
12	409 μs
13	819 μs
14	1.6 ms
15	(not used)
16	6.5 ms
17	26 ms
18	52 ms
19	104 ms
20	208 ms
21	417 ms
22	834 ms
23	1.67 sec
24	3.34 sec

In this type of arrangement, unless new data is loaded into stage 1, the clocking command will ultimately clear the register; therefore, to form a sequence generator, data from a selected stage, or stages, must be fed back to stage 1. If the operation in the feedback path involves only addition (Modulo 2), the sequence generator is said to be linear.

Modulo 2 arithmetic can be implemented by an Exclusive OR logic gate. When the shift register is connected with a feedback loop in this manner and is operated so that at unit time interval, the content of each stage is shifted to the next stage, the resultant content of stage 1 will be a function of the initial state of the bits in the register and of the feedback connections made.

Both the length of the register and the point(s) from which feedback connections are taken determines how long the sequence will run before it repeats. For example, if the register contained n stages, there would be 2^n possible combinations of bits; if all possible combinations were generated, the sequence would have a period of 2^n digits. If the generator was allowed to generate all of these combinations, it would reach a point at which the register would contain all 0s. At this point, the sum-digit of the modulo 2 gate would be 0 and the generator would remain in this state producing, from that point forward, a trivial all-0s sequence. Because of this, the largest possible period for a linear n-stage shift register sequence generator is 2^n-1.

A functional block diagram of one of the 2340 shift registers is shown in Figure 5-3. The state of the 23rd bit is XORed with the state of the 5th bit and on the next clock, the result is fed back into the first bit position. Figure 5-4 shows an abbreviated pattern listing that ensues if the generator begins with an all 0s pattern. This is shown for illustrative purposes only; in practice, these generators are all initialized to a particular pattern before they are started (Paragraph 5.4.5).

Refer to Figure 5-4; because of the match at the XOR between bits 4 and 22 for the first 5 clock pulses, 1s will be shifted in, until on the 6th clock pulse, a mismatch exists, shifting in a 0. This mismatch exists for the next 4 clock pulses until on the 11th clock, the match is reestablished. This pattern persists until on the 23rd clock, the state of bit 22 changes, modifying the recurrence of the pattern.

The entire Random Generator is contained on 3 modules, comprising 3 sectors of 22 outputs each. For every Adapter Clock pulse, the output data pattern shifts, causing each register to enable the testing of pseudo-random combinations of pins assigned to it.

Since there are 3 Random Generators, each operating independently to produce different patterns, a means is provided to ensure that they are generating in synchronism. This is done by an initialization process within the Test System (Figure 5-5). When the INIT button is pressed on the front panel, the Pin Selector is filled with 1s (the timing diagram is keyed to the block schematics). At the same time, the Adapter Clock is applied to all 3 Random Pattern Generators. As can be seen by the timing diagram, these generators will all begin shifting their patterns but they may not be synchronized. Each generator is wired to detect a particular pattern. When this happens in the first generator, the Adapter Clock for that sector is inhibited; when it occurs in the second sector, that sector clock is inhibited. Finally, when the pattern is reached by the third generator,

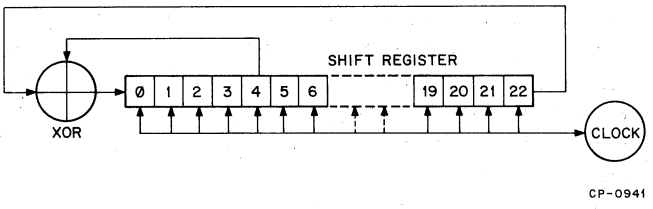

Figure 5-3 Random Generator Shift Register (Typical)

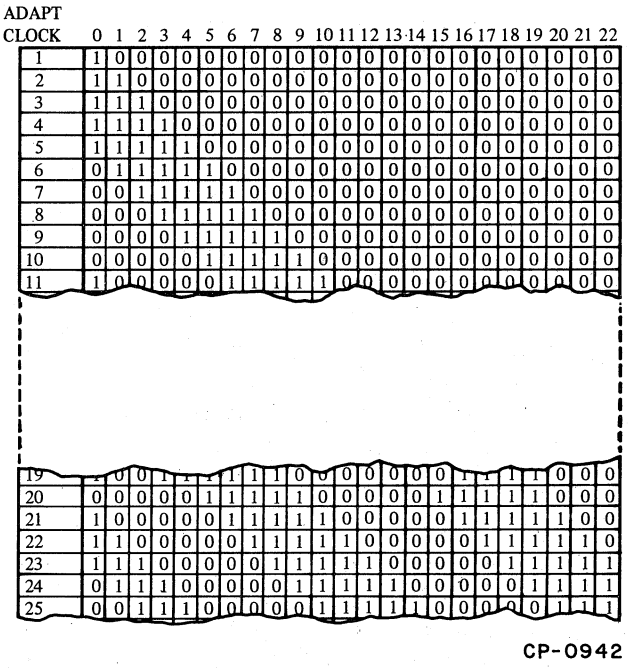

Figure 5-4 Partial Random Generator Pattern

the other 2 clocks are enabled, allowing all 3 sectors to generate in sync. Now, all 3 generators will step and when the pattern is simultaneously reached in all 3 sectors again, all 3 clocks are inhibited and the INIT indicator will glow. Any erroneous indications that might come up during this process, due to a lack of synchronization, can be reset by the ERROR RESET button on the front panel. Now, when the START button is pressed, the Random Generator will run for as long as it is desired.

The outputs of the Random Pattern Generator are controlled by 66 panel-mounted switches associated with each testable pin on the modules. These switches each select the inputs and outputs of the modules. The outputs are then sent to the Random Adapter, containing 66 7405 Open-Collector Buffers. The 66 3-position switches supply either a high signal, a low signal, or an open signal, which holds the output to pattern.

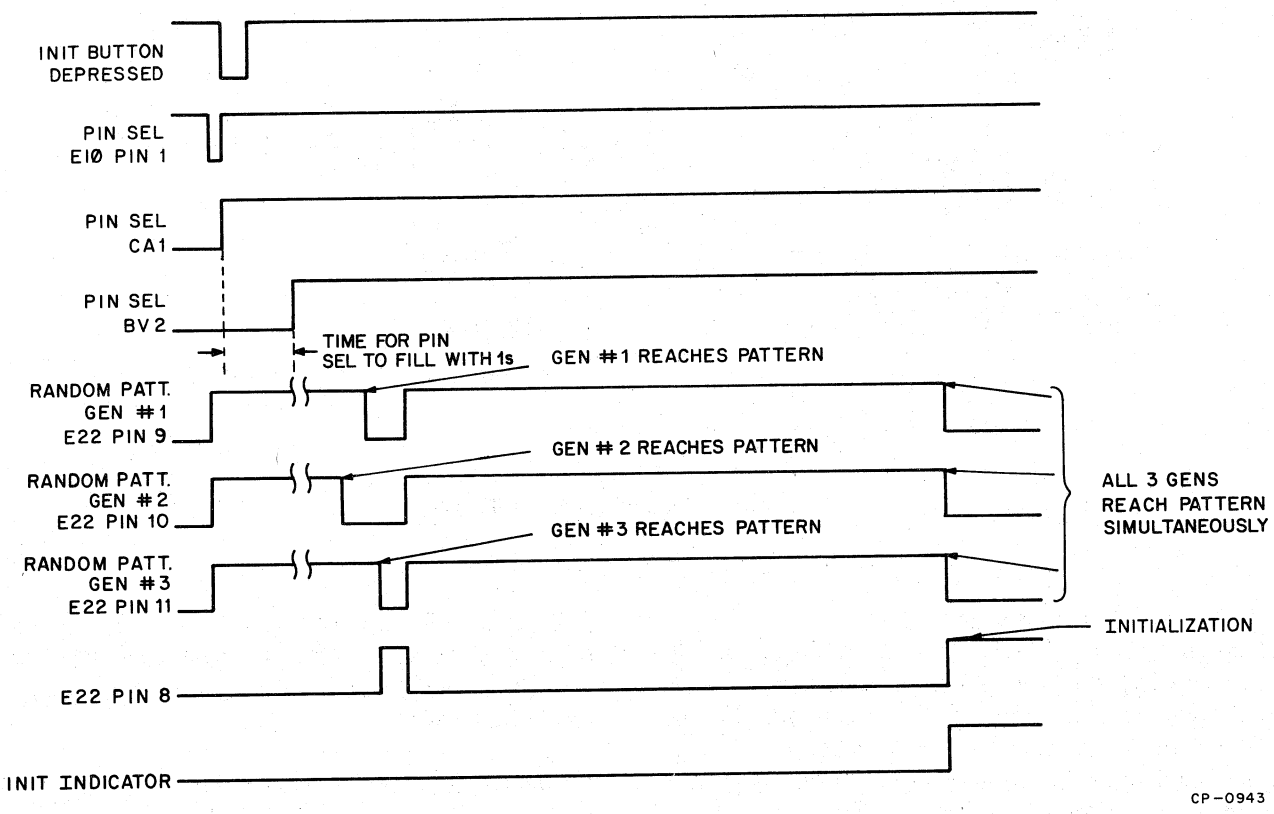

Figure 5-5 Random Generator Initialization Sequence

The outputs of the Random Adapter feed an interface cabling assembly (9305365-0-85) comprising a G750 Interface Connector module that feeds G751 and G752 Interface Driver Connector modules. Their prime function is to limit noise and cross-talk in the transfer to the head fixture. These in turn feed M908B Pull-Ups for termination and then feed the KGM and MUT, mounted in the Head Fixture on a pin-parallel basis. An identical interface cabling assembly then feeds the outputs of the KGM and MUT to the comparator modules where coincidence testing of the module outputs is made.

The 2340 contains 66 individual comparator circuits contained on 3 identical modules of 22 comparators each. The comparator logic is simplified in Figure 5-6. The 66 lines from the KGM are fed to point A while the 66 comparable lines from the MUT are fed to point B. The sample signal feeds the clock inputs of these flip-flops to strobe in the data. Point C of the comparator sees the timing input from the pin selector. These gates then feed an XOR. If the 2 pins compare favorably, the output of the XOR will remain low and will not clock its flip-flop. If a difference exists, an error will be recorded as the flip-flop sets to light its associated indicator and sends a signal to the Failure Summation Logic. This flip-flop will then lock up, retaining the indication after the strobe has been removed.

In this mode, the test will continue indefinitely until the front panel STOP button is pushed and will then continue once again if the START button is pushed. Error indications will accumulate in the indicators. The PASS light will initially come on and will remain lighted until the first error is detected, when it will extinguish. The FAIL light will light, indicating that an error has been detected. This is accomplished in the Failure Summation logic on the G5000 board, where the 66 outputs of the comparator XORs are fed to a set of gates that yield 1 error output signal (LOE) on any error input.

Error indications are carried to the indicator board by 6 M9002 Ribbon Connector Cables. The 66 lights on the board correspond to the 66 pins on the boards being compared. There is a set for A1, A2, B1, and B2, with A1A corresponding to A1A on the boards.

A Test Cycle takes approximately 60 seconds to complete.

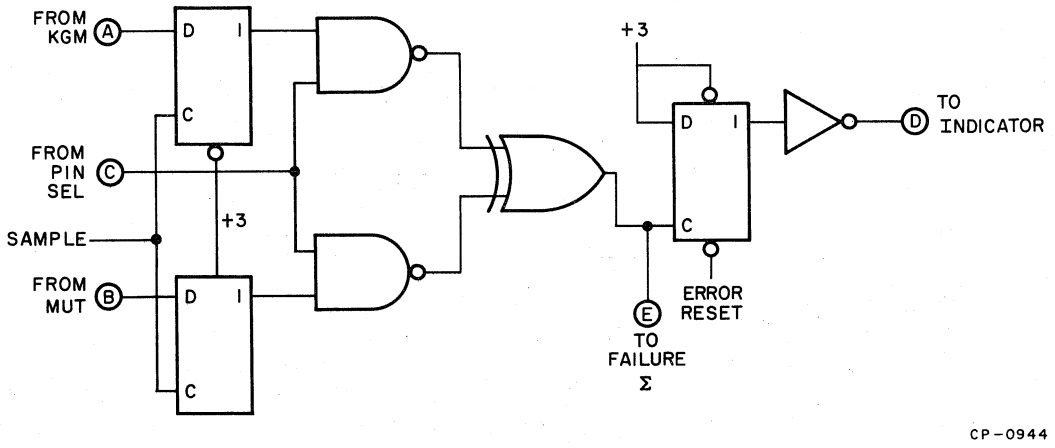

Figure 5-6 Comparator Block Diagram

5.3.3 Program Mode Operation

All hardware is identical except that the Random Generator is not used and is disabled by a front panel switch marked MODE (refer to Figure 5-2). In this mode, the Random Adapter Card is replaced by a specially fabricated Program Adapter Card, designed to function only with the specific module to be tested. In addition, when in this mode (MODE switch set to PROGRAM position), the 66 front panel switches are inoperative.

This mode is used to test only those modules that cannot be tested in Random Mode, such as modules containing clocks, oscillators, etc.

In this mode, the Adapter Rate determines the rate at which 9 test waveforms are presented to the module inputs. These are the outputs of a divider chain in which the input is the inverse of Adapter Clock. Each subsequent output is then twice the period of its predecessor and is the basis for the design of the Program Adapter Board.

Testing is conducted on a sequential basis by the Pin Selector. In Random Mode, this logic was filled with 1s to hold all comparator inputs open to comparison, but in this mode, a 1 is shifted through this 67-bit register, causing it to function as a single-level rotary switch, enabling each of the 66 comparators, in sequence. The register stops on bit 67.

The failure summation logic serves to stop the test on error if the ERROR switch is set to the STOP position. If it is set to BYPASS, it will not stop on error but indications will accumulate until all pins on the modules are sampled. When in Error Stop Condition, an error will stop the test. The LOE signal, described under Random Mode Operation, is used in the Pin Selector to interrupt the common clock input to the register.

Testing is interrupted by pressing the STOP button on the front panel, causing the Pin Selector to stop where it is, lighting the PAUSE indicator. The test will not resume until the START button is pushed.

The Test System can be made to single-step for troubleshooting purposes by placing the TRT switch on the front panel to SINGLE STEP position and then pulsing the SINGLE STEP switch.

Two pins are provided on the Interface: a return SYNC pulse from the Adapter (available on the SYNC BNC) and a return PAUSE signal from the Adapter, which stops the Pin Selector on a low command.

5.4 DETAILED LOGIC DISCUSSION

In this paragraph, the equipment is discussed in terms of the various sections of logic. The boards are described separately and not necessarily in the sequence of their operation. References are made to the block schematics included within the Engineering Drawing Set. Simplified block schematics and/or timing diagrams are included to aid in the discussion.

These discussions are intended as supplementary to the functional discussions in Paragraph 5.3 and should be related to that paragraph for an overall view of the operation.

5.4.1 Timing

The 2340 timing is derived from an M405 Crystal Controlled Clock, located in slot F-12 of the backplane. This is a standard DEC module and is described in detail in separate DEC documentation. Its output is fixed at 10 MHz and is fed via control circuits to the Time Select logic, located in slot A-D-1 of the backplane. This circuit is shown on Drawing D-CS-G5000-0-1 and is simplified in Figure 5-7.

The master clock control logic is contained on the Adapter Interface (Drawing D-CS-G5007-0-1) where its availability to the time select logic is made dependent upon what could be termed a "master" clock flip-flop (E2). Application of the clock is made whenever this flip-flop sets, by pressing START, or is direct-set when the INIT button is pressed. Resetting this flip-flop by the STOP or ERROR RESET buttons will interrupt the clock.

When applied, the 10 MHz is fed to a clock divider register, comprising 7 7493s, in tandem, that generate 28 increasing timing periods from the input of 100 ns to 26.7 seconds. These are then distributed in differing sets to the time select gating combinations.

The time select combinations, like the select combinations, consist of sets of AND/NOR/NANDs that yield one and only one rate per combination, depending upon the position of their front panel rotary switch. Each input AND gate combines a particular clock rate with a ground applied by the switch to feed that rate to that specific clock distribution line.

Note that the rates for each function are selected to afford maximum flexibility over a wide range of board response times (Figure 5-8). The test rates, which in Program Mode are applied to the comparators by the Pin Selector, are the 11 longest periods. These are the enable rates for the comparators and by definition, should be the longest periods to allow for propagation delays and settling times. This is not important in Random Mode, since once the pin selector fills with (1)s, the rate of testing is entirely under control of the Adapter and Random Generator.

The range of the Adapter Clock, used to activate the input pins of the modules, is set within the overall range of periods and excludes the 3 shortest and 3 longest periods, in addition to excluding every other rate within that span.

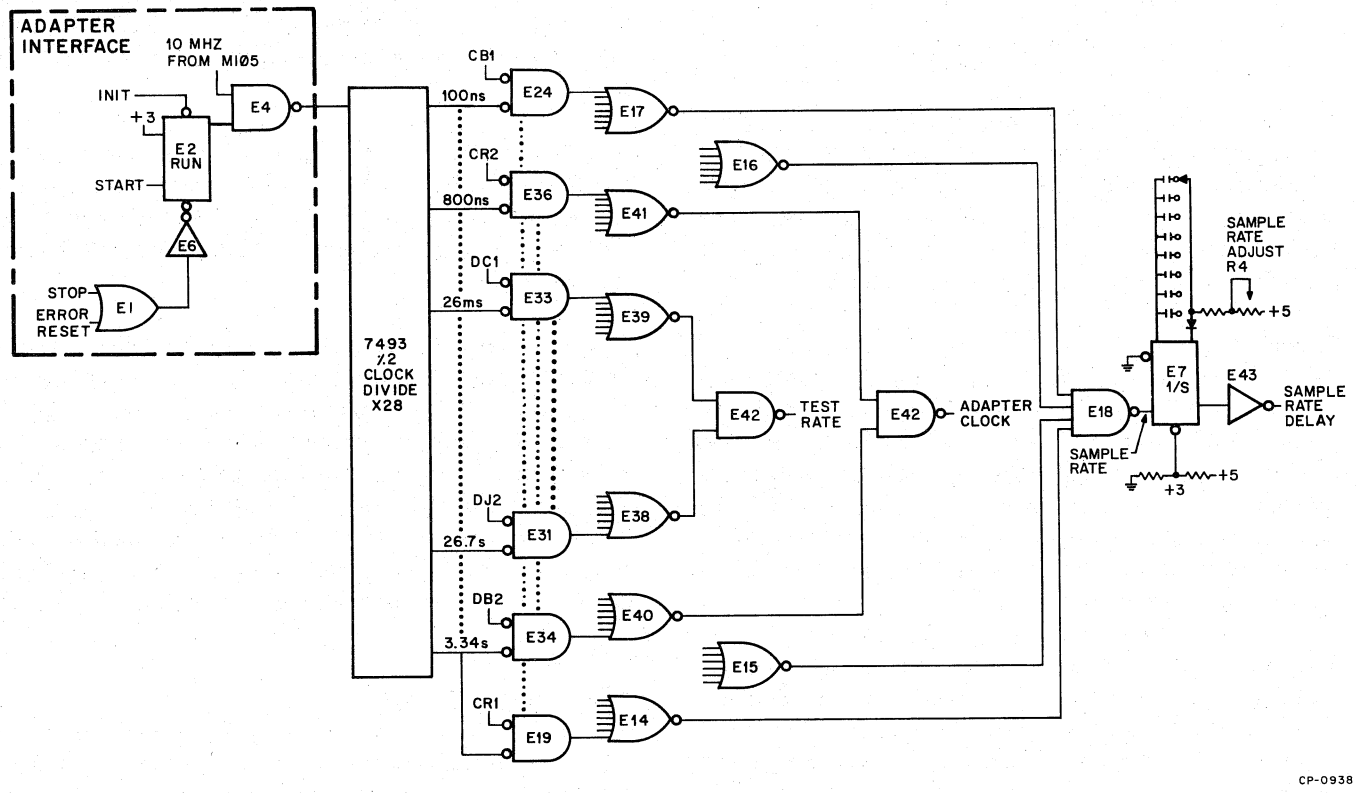

Figure 5-7 Time Select Simplified Block Diagram

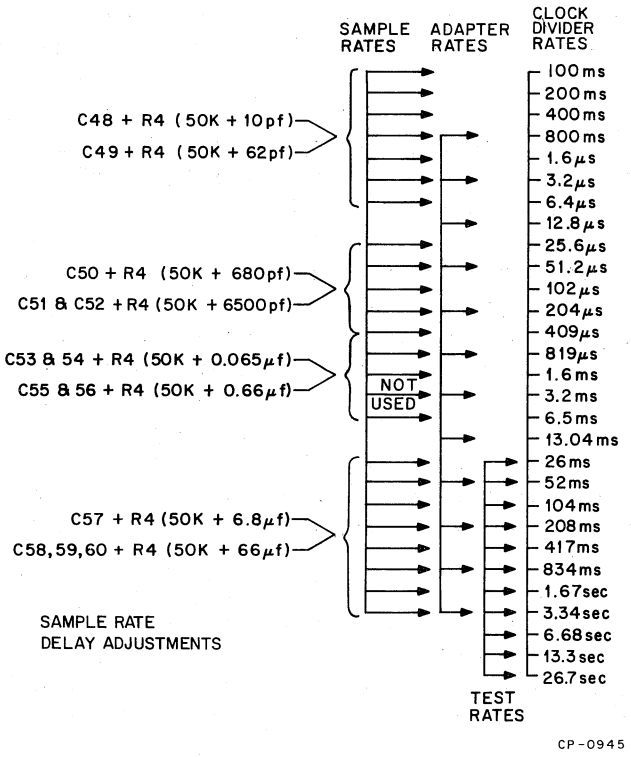

Figure 5-8 Rate Distributions

This gives ample overlap with the Test Rate, so that mid-ranges of coincidence can be checked, but does not waste gates on the high and low ends where they are not needed. It can be seen by this distribution pattern that judicious rate choices must be made by the operator while keeping cable delays and logic response in mind.

Sample Rates are set across the Adapter Rate range in 3 clumps of 7, 9, and 8 each. The 2 deleted sample rates, 12.8 μs and 13.04 ms are not critical, since the slip of Sample Rate Delay can more than amply cover these periods. Inclusion of these 2 rates would result in poor gate economy. The rates are applied as clocking signals to the comparator input flip-flops, where the greatest variety of rate is required, since it determines the actual duration of coincidence observation ("window").

The Sample Rate is then subjected to a delay circuit, comprising a 74123 at E7. There are 8 capacitor combinations provided, which in conjunction with the fine tuning of R4, can slide the start of the window anywhere within the selected rate. Figure 5-8 also relates these components to the ranges they cover.

5.4.2 Adapter Interface

The 2340 Adapter Interface (Drawing D-CS-5007-0-1) is located in slot A-D-7 and is simplified in Figure 5-9. This logic contains the master clock control logic, discussed in Paragraph 5.4.1, and the control logic for the RUN indicator.

The RUN indicator lights upon coincidence of three lows; one for the 7474 at E2 when set, one from the 7474 at E25 when set, and a third which is the inverse of the same set condition.

In Random Mode, when INIT is pressed, the "run" flop will clear and the "master clock" flop will set. This applies the 10 MHz to the select logic, but prevents the RUN indicator from lighting, by placing a high at pins 10 and 11 of E3. When the initialization process is complete, INITIALIZE (L) is generated in the Random Generators, clocking the "run" flop and enabling the RUN indicator once again. Since "master clock" is already set, the RUN lamp will light.

When in Program Mode, a ground is applied to pin AF2 by the MODE switch to enable the run condition by direct-setting the "run" flop. Now, the RUN indicator will light when the START button is pushed as the $\overline{Q}$ side of the "master clock" flop places the completing low on pin 9 of E3.

In either mode, the RUN light will extinguish whenever STOP or ERROR RESET is pushed. Whenever a failure is sensed (FAIL(H)) it ANDs with the 417 ms output of the time selection logic to cause the RUN indicator to flash at that rate.

The other logic included on this board is used, when in Program Mode, to control the operation of the Program Adapter Card. This comprises 2 clock dividers (7493), in tandem, that produce a simple 8-bit binary sequence on ADAPTER CLOCK, each individually buffered for use. In addition, the SYNC and PAUSE signal lines are routed through this interface from the Pin Selector module to the front panel BNC connectors, along with ADAPTER CLOCK, the inverse of which is brought out to a similar connector.

5.4.3 Program Adapter

As described earlier, the Program Adapter is a specially fabricated board, designed specifically to adapt the 2340 for testing a module that cannot be tested in Random Mode. Because its design will vary with the board to be

tested, this module cannot be discussed at this level of discussion.

5.4.4 Random Adapter

The 2340 Random Adapter (slot A-D-6 of the backplane) is shown on Drawing D-CS-5006-0-1, sheets 1-6, and is simplified in Figure 5-10. This module, used only in Random Mode, contains 2 identical sets of 66-each, 7405 open collector buffers. Each pair of buffers are fed, in-parallel, by a particular output of the Random Generator. One output of each set of buffers is fed to a specific input pin on the KGM, while the other output is fed to the same specific input pin of the MUT. Their purpose is to feed the same signal to comparable module pins. Their outputs are interfaced with the modules through a G751, a G752, and M908B Pull-ups. When in Program Mode, this module is removed and replaced by a Program Adapter Card.

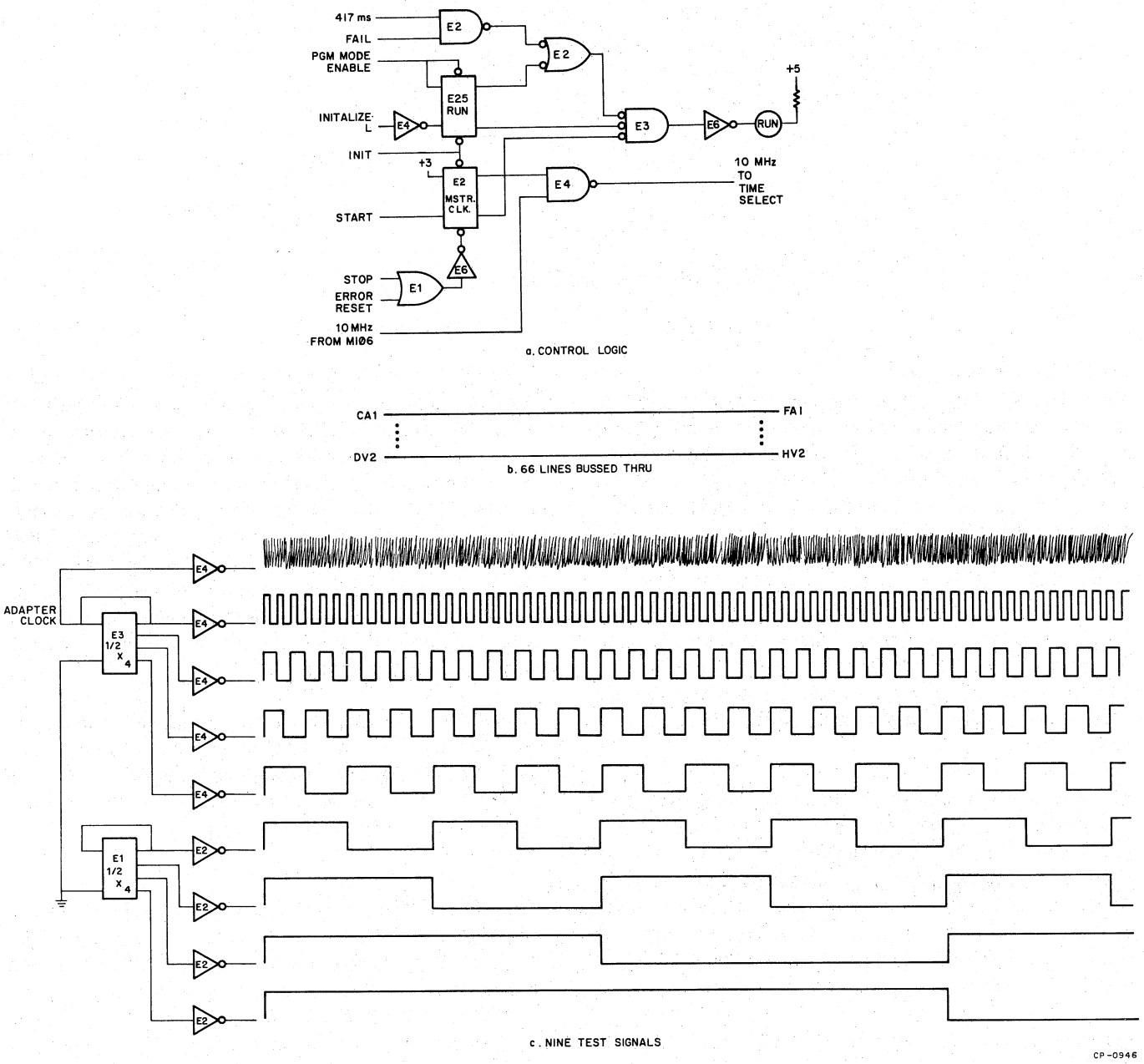

Figure 5-9 Adapter Interface Block Diagram

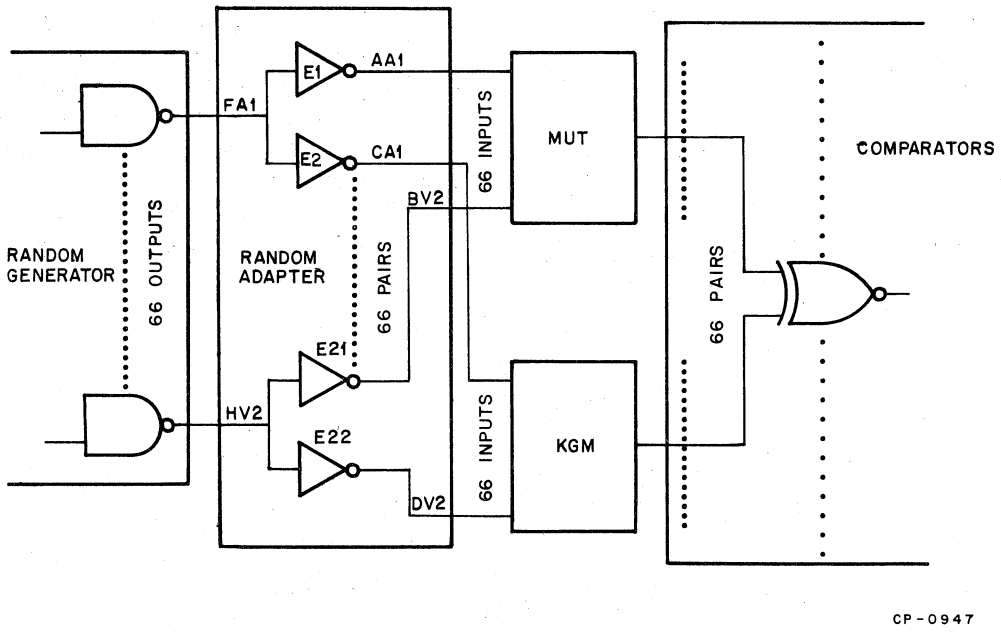

Figure 5-10 Random Adapter Block Diagram

5.4.5 Random Generators

The underlying theory of this logic was discussed in general terms in Paragraph 5.3.1 and illustrated in Figures 5-3 and 5-4. The schematic is shown on Drawings D-CS-G5003, 4-, and 5-0-1, and is simplified in Figure 5-11. Functionally, this logic is a shift register that takes inputs from the ADAPTER CLOCK and the 66 front panel switches and outputs a pattern of (1)s and (0)s that are a function of both its inputs and its feedback arrangement.

The logic on the 3 modules is similar but not identical. Generators #2 and #3 are almost identical with Generator #1, containing extra control logic for overall generator control, and for generating control signals for use elsewhere in the system.

All 3 generators contain a basic shift register, each comprising 3 74164s, connected in tandem. The 3 generators function independently on the common ADAPTER CLOCK, but the availability of the clock to Generators #2 and #3 and to Generator #1 is put under control of logic in Generator #1, as interlocked by a condition of initialization in each generator. This is described later in this paragraph.

Each bit output in all 3 generators is fed to a double set of buffers used to control the output conditions of each bit position. A typical bit control arrangement is illustrated in Figure 5-12. The bit output of the register is fed through 2 NANDs, whose other inputs are normally tied high when the associated panel switch is in PATTERN position. When in this position, the output of the second buffer will track the output of the register. When the associated panel switch is put in LOW position, the buffer output will be a steady low; it will be a steady high when the switch is put in HIGH position. In this way, selected pins can be held to the proper state for normal operation of the boards under test, or left tied high so that they will be under control of the output of the generator. The positioning of each switch is dictated by the board design.

Clocking for all 3 74174s (Adapter Clock) is fed in on pins AA1 and BA1 and then ANDed with the (0) H state of a 7474 flip-flop. These registers are not clearable; pin 9 on all chips is tied to +3 to prevent any possibility that the register will ever exist in an all-0s state.

The bit arrangements on all 3 generators are similar but not identical. In all 3 generators, the instantaneous states of bits 4 and 22 are fed back to bit 0 through an XOR. When these two bit states are the same a 0 is fed back into the register on the next clock; when they differ, a 1 is fed back. It is this characteristic that enables the register to generate a random output pattern while shifting through the sum digit outputs of the feedback logic.

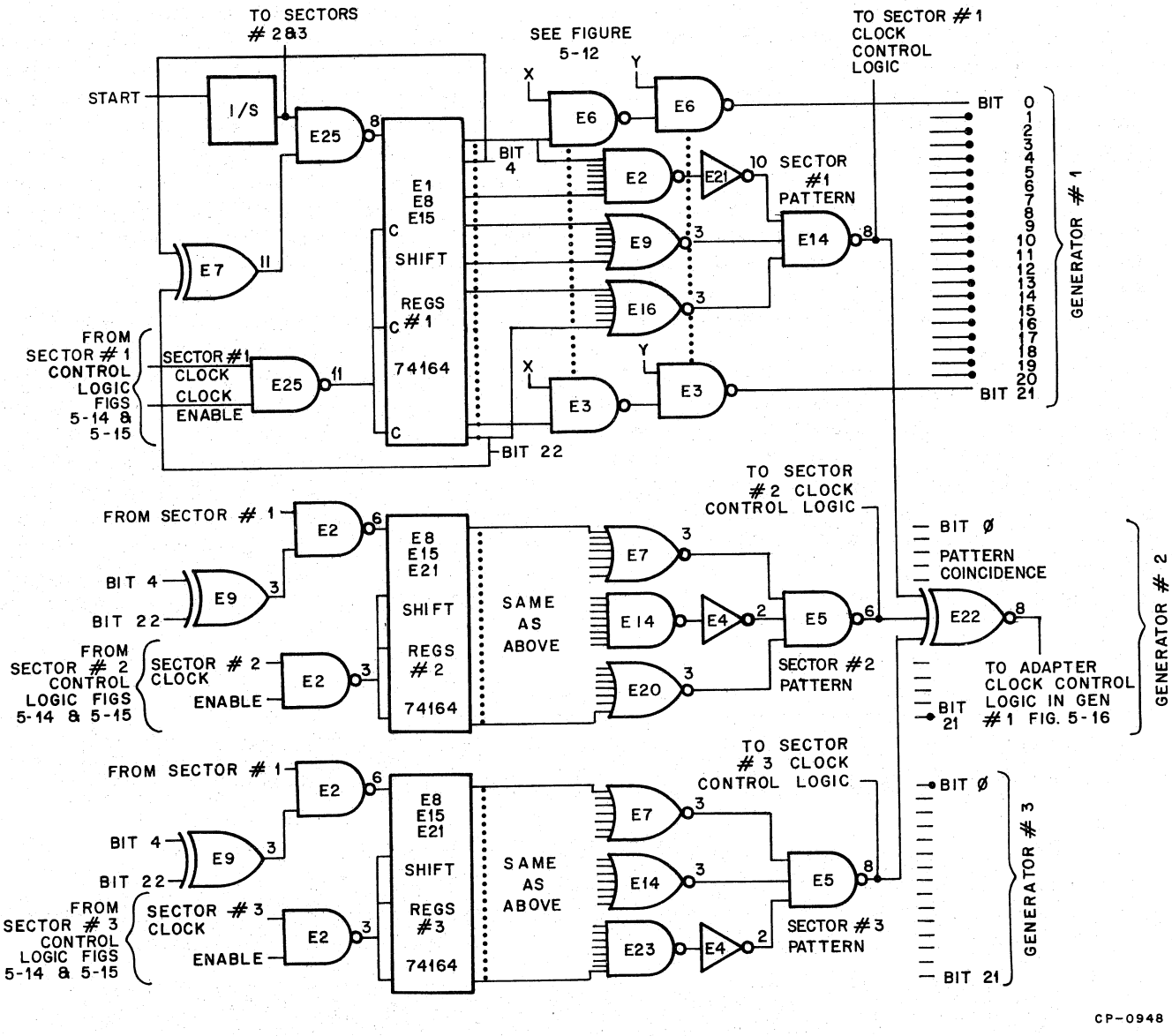

Figure 5-11 Random Generators Simplified Block Diagram

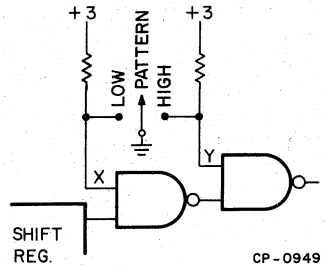

Figure 5-12 Typical Front Panel Switch Arrangement

In addition to each bit output being fed to individual output gates, they are also collected by various NAND and NOR combinations, and summed, to detect a particular output pattern. These patterns are different for each generator, but once detected by each, they are used to serve an initialization function.

Initialization is required for two reasons: 1) to prevent an all-0s pattern from happening, and 2) to ensure that all 3 generators are operating in synchronism during test. Only when all 3 generator patterns are the same, can it be assured that all pins will be checked in the same random fashion.

When the INIT button is pressed on the front panel, a ground is put on pin BE1 of Generator #1 and on AE1 of Generators #2 and #3. This clears all 7474 control flops in all 3 generators and initiates a one-shot combination at E26/E28 in Generator #1. This puts a low on a NAND in each generator, thereby placing a (1) into the data input of each input chip. At the same time, ADAPTER CLOCK is made available to all chips when ANDed with the high reset state of the individual control flops.

Note that the placing of a 1 into the first stage of each register is done to ensure that an all-0s condition does not exist in any register. If this were the case, the generators would operate but would generate all 0s because of a continuous match at the XORs. Even if an all-0s combination did not exist, it is quite possible that the random states at the outset could begin with some form of coincidence between bits 4 and 22 of some generator. This alters that condition so that the generators can be initialized to a state of synchronism.

Figure 5-13 illustrates the bit patterns at the outset of some random condition in each register. The first set of states shows a (1) placed in the first stage of each register. On the next clock, all conditions shift with the succeeding state of bit 0, determined by the XOR of the states of bits 4 and 22. The figure is broken after the 4th clock and picks up at 5 clocks prior to initialization (X-4). For purposes of this discussion, it is assumed that Generator #2 reaches its preset pattern at this point as determined by the states necessary to produce a low at pin 6 of E5 (Drawing D-CS-G5005-0-0). At this point, the pattern remains fixed

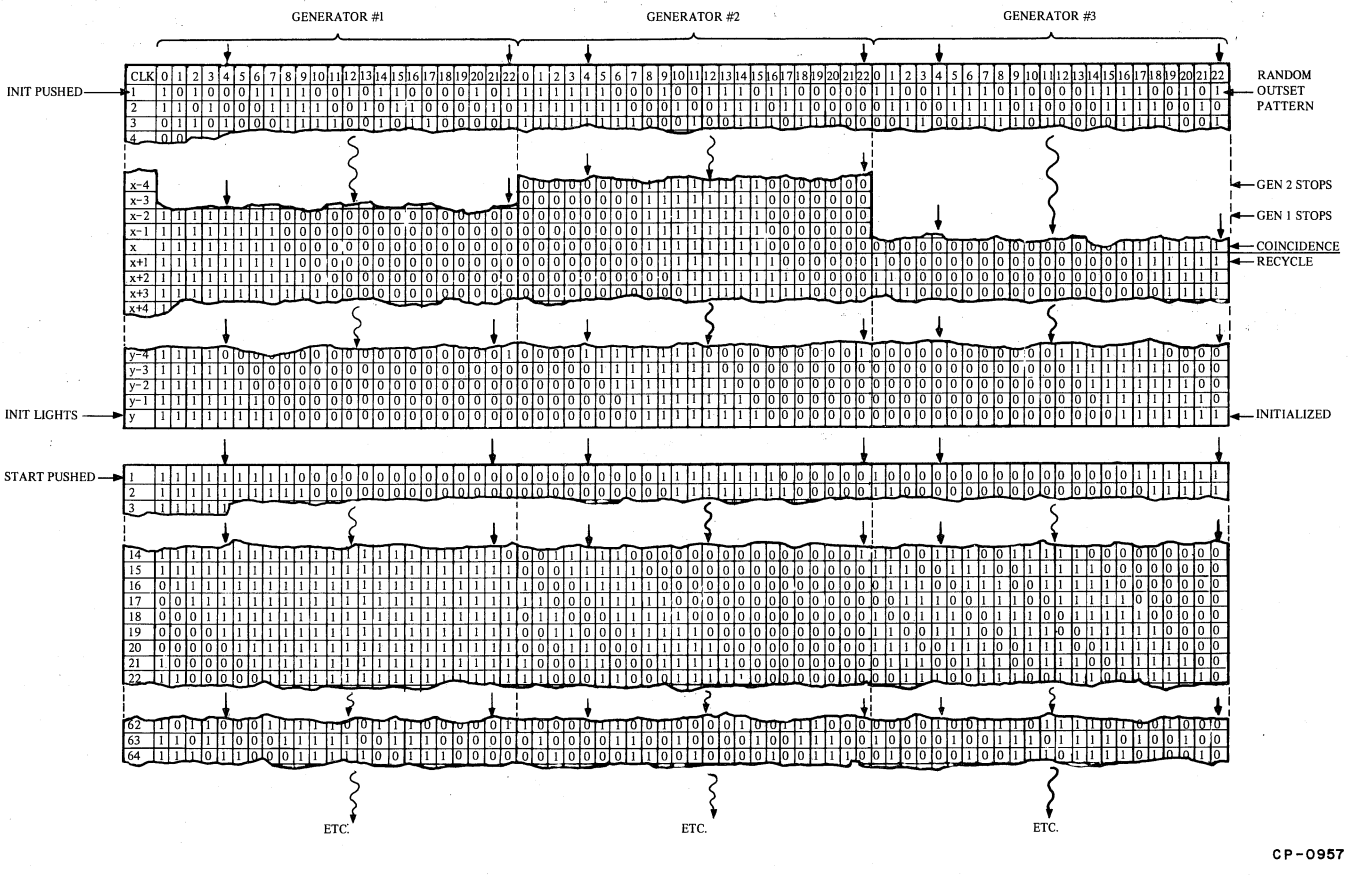

Figure 5-13 Random Generator Patterns

because as shown on the drawing, the 7474 at E1 is clocked, thereby interrupting the clock to this generator at pin 3 of E2.

The figure then assumes that Generator #1 reaches pattern at X-2 for the same reasons and waits for Generator #3 to reach pattern at X. Note that the figure calls this "coincidence".

This can be seen in the logic on the drawing for Generator #1 at pins 9, 10, and 11 of the 7427 at E22. These pins see the outputs of each pattern gate, and at coincidence, pin 8 is driven high, thereby clearing the 7474 at E23, restoring the clock to all 3 generators. There is a sequential interlock here to allow any generator (if it is the last to reach pattern) to restore the clock to all 3 generators. The operation of this interlock is discussed later in this paragraph.

At coincidence, the clock is restored and all 3 generators are recycled for 1 pass to ensure synchronism. This point in the figure is identified as clock "y"; it should be noted that the patterns at initialize are identical to those at coincidence.

At initialization, the clock is once again removed, but this time by clocking the 7474 combination at E24, and although the 7474 combination at E23 is once again cleared, the clock is removed from pin 4 of E25 which, via pin BF1 of this module, interrupts the clock on the other 2 modules by setting the latching control flip-flops on those modules.

At this point, the INIT light comes on and the 2340 waits to be started. When the START button is depressed, a ground is put on pin BE1 of Generator #1 clearing the 7474 at E24, and reapplying the clock. This is parallel to pins AE1 in the other 2 generators to restore the clock there. When this happens, the INIT light is turned off at pin BD1 of Generator #1, and the generators produce the patterns shown (in part) in the figure. Note that as early as clock 64, a high degree of randomness has been achieved by all 3 generators. Note also that because of the differences in the preset initialize patterns, the pins are all checked, but not necessarily in the same sets of sequences.

The sequential interlocking of the application of ADAPTER CLOCK is shown separately in Figures 5-14, 5-15, and 5-16. The function of this logic is: 1) to apply clock to all 3 generators when the INIT button is pressed, 2) remove clock independently from any generator when *it*

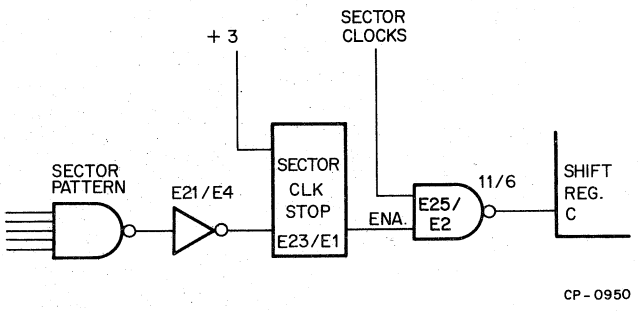

Figure 5-14 Sector Clock Removal Logic

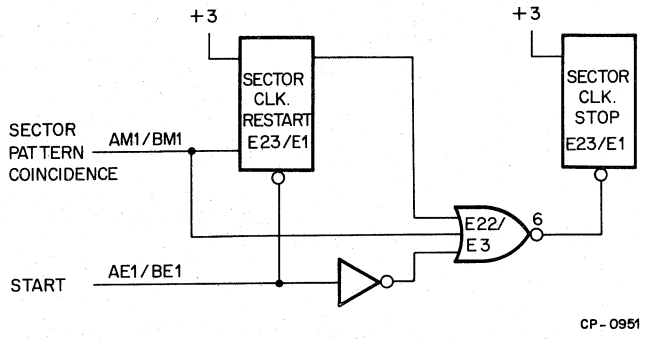

Figure 5-15 Sector Clock Restoration Logic

reaches its preset pattern, 3) reapply clock to all generators when all 3 have reached their preset patterns, 4) remove clock from all 3 generators when they then have reached pattern simultaneously, and 5) provide a means at that point to apply clock on a non-pattern-interrupt basis by the front panel START button. In addition, the logic controls the necessary indicator functions during this process.

The basic logic for removing the clock from each sector is shown in Figure 5-14. When Sector Pattern is decoded, a SECTOR CLOCK STOP flip-flop is set to remove the clock from that sector's shift register. By referring to the drawings for the generators, it can be seen that this logic is identical for all 3.

The basic logic for restoring sector clock is also identical in all 3 generators and is shown in Figure 5-15. When Sector Pattern is detected in all 3 generators, a Sector Pattern Coincidence signal is generated that clocks the SECTOR CLOCK RESTART flip-flop, which in turn resets the SECTOR CLOCK STOP flip-flop. This allows the generators to cycle through an additional pass to pattern.

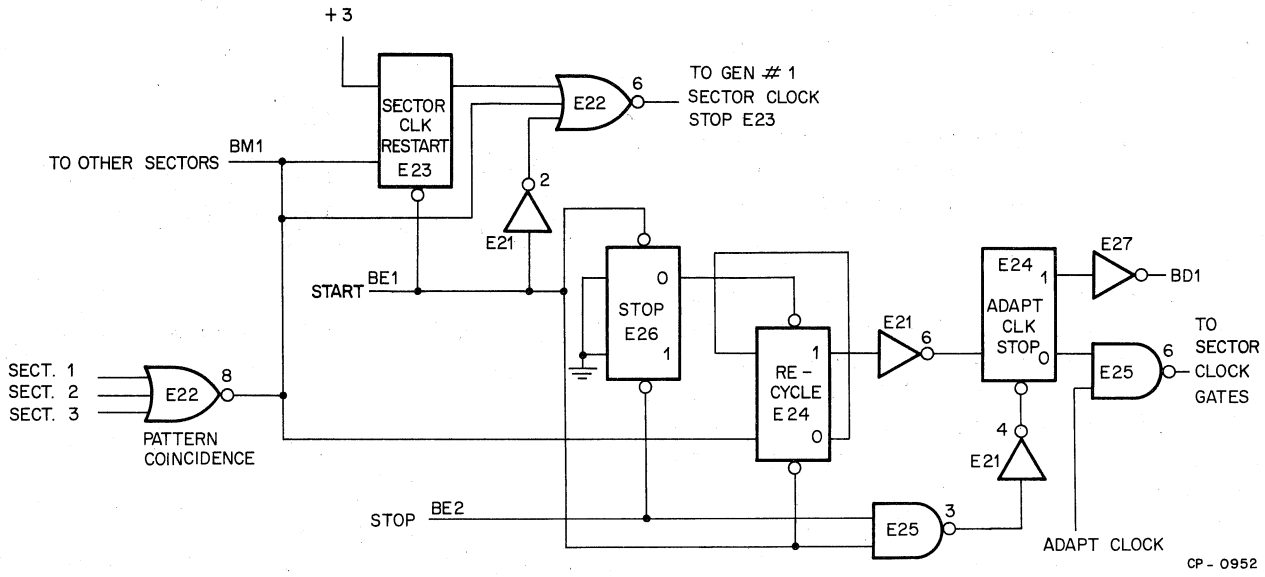

Figure 5-16 Adapter Clock Removal and Restoration Logic

At the second coincidence of pattern, all 3 generators stop to await a START from the front panel. The logic for this second stop is caused by interrupting all Sector Clock signals at their source in Generator #1, where ADAPTER CLOCK is removed by the logic shown in Figure 5-16.

When pattern coincidence is seen, E22 pin 8 goes high. This does several things: 1) it clears SECTOR CLOCK STOP, restoring Sector Clock to Generator #1, 2) it clocks SECTOR CLOCK RESTART, which holds SECTOR CLOCK STOP reset, 3) it sends the same high through pin BM1 to pin AM1 on the other generators to restore their sector clocks, and 4) it sets the RECYCLE flip-flop in Generator #1. When RECYCLE sets, its (1) side goes high, which has no effect on ADAPTER CLOCK STOP at this time, but it conditions that flip-flop for the second appearance of coincidence. The generators then recycle through to pattern once again and on simultaneous coincidence, the RECYCLE flip-flop complements. When its (1) side goes low, ADAPTER CLOCK STOP sets. This interrupts ADAPTER CLOCK from all 3 generators via BF1 and lights the INIT indicator via pin BD1. At the same time, all 3 SECTOR CLOCK STOP flops are cleared to open their sector clock sources.

Later, when the START button is pushed, pin BE1 is grounded, clearing RECYCLE, clearing ADAPTER CLOCK STOP (to restore ADAPTER CLOCK), clearing SECTOR CLOCK RESTART (restoring Sector Clock), and ensuring that the STOP flip-flop is cleared.

The generator will run indefinitely and will not stop on any subsequent coincidences because pattern in any generator will not set its SECTOR CLOCK flip-flop since the coincidence signal will occur at the same time and will therefore hold those flip-flops reset.

When STOP is pressed, a ground is placed on pin BE2, which direct-sets STOP, thereby placing a direct-set on RECYCLE. This interrupts the ADAPTER CLOCK to all 3 generators. Depressing START then clears both RECYCLE and ADAPTER CLOCK STOP, restoring clock to all 3 generators.

Note that INIT, START, and STOP are the only front panel pushbuttons that are operable while in this mode. ERROR RESET and SINGLE STEP are not operable.

5.4.6 Pin Selector

The 2340 Pin Selector logic is shown on Drawing D-CS-G5001-0-1 and is simplified in Figure 5-17. This logic functions basically as a rotary switch to control the enables on the Pin Comparator. In Random Mode, it is quickly filled up with (1)s so that the comparators are all left open for the Random Generator patterns. In Program Mode, it is operated like a Shift Register with a single (1) shifted through in sequential order. In that mode, this rotating signal is applied both to the Adapter Interface, where it activates one and only one input to the modules at a time, and to the Pin Comparator, where it enables the comparable output pin comparators in the same sequence.

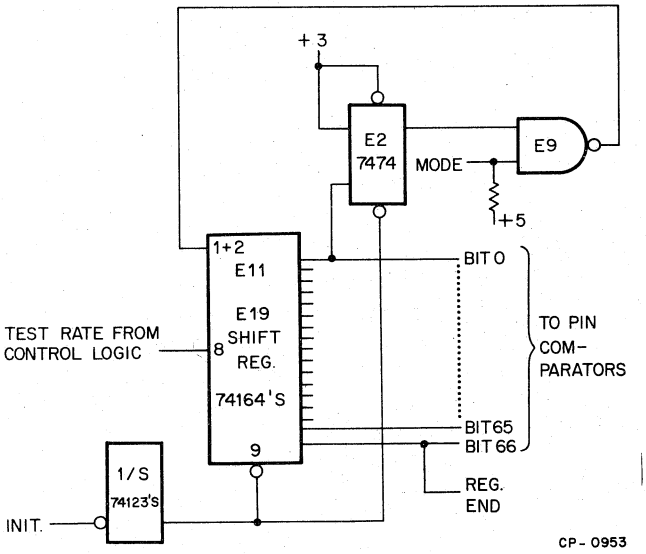

Figure 5-17 Pin Selector Shift Register Logic

The pin selector shift register consists of 9 74164s, in tandem, that are cleared by a pair of 74123 1-shots. These 1-shots also clear a 7474 flip-flop. The register is clocked by TEST RATE, made available at pin 11 of E9 as determined by the associated control logic. The 7474 at E2 is used to either feed in a single (1) that is then shifted through or to fill up the register with (1)s.

When the MODE switch on the front panel is placed in PROGRAM position, pin 2 of the NAND at E9 is tied high so that when the START button is pushed, a ground is put on pin AB1 and the 7474 at E3 is cleared. This completes the TEST RATE path through pin 6 of E9 to the clock inputs of the register. On the first subsequent clock, due to the mismatch at the input of E9, a 1 is strobed into the first position, thereby clocking E2. When E2 sets, its pin 5 goes high, returning the input to the first position of the register to 0. At each subsequent clock thereafter, the 1 is shifted through, followed by a string of 0s.

When the MODE switch is placed in RANDOM position, pin 2 of E9 is grounded, and when the INIT button is pushed, the dual 1-shot clears E2, but since pin 2 is now held low, 1s will be shifted in, regardless of the state of E2. This fills the register with 1s and maintains that condition as long as the MODE switch is in RANDOM position.

The control logic for application of TEST RATE is simplified in Figure 5-18. TEST RATE is fed through inverter E8 to pin 5 of E9, where it is fed to the shift register from pin 11 of E9 whenever a ground is placed on pin 9 of E9 by placing the TRT switch in AUTO position. Clock is then interrupted or controlled by any of the following:

1. If TRT is put in SINGLE STEP position, a ground is placed on pin 4 of E9, putting a low on pin 12 of E9. This inhibits the TEST RATE clock from being seen by the shift register. Now, pulsing SINGLE STEP transmits a timed-out high to pin 10 of E9 and a high is seen at the shift register clock input for the duration of the one-shot. At all other times, when the TRT is in AUTO position, pin 9 of E9 is low, leaving pin 13 high, placing the source of TEST RATE solely under control of what happens at pin 5 of E9.

2. When the ERROR switch is put in STOP position, BN1 is connected to MB1. Then, whenever the LOE signal signifies an error, E7 is clocked at pin 1, interrupting the clock to the register. The same thing will occur if PWR fails (or is not yet up to value) by clocking E7 at pin 10. In either case, the FAIL indicator will light. ERROR RESET clears both of these flip-flops, extinguishing the lamp and restoring clock. When this happens, pin 8 of E7 goes high to light PASS.

3. PASS remains lighted until the shift register reaches bit 66. At this time, PASS will extinguish and the clock is inhibited at pin 1 of E8.

4. If the STOP is pushed, E3 sets, causing its pin 6 to go low, thereby inhibiting clock. Pressing START clears this flip-flop, restoring clock.

5.4.7 Comparators

The comparators for the 2340 Test System are shown in Drawing D-CS-5002-0-1 and are simplified in Figure 5-19. There are 3 identical 22-pin modules used in the system to accommodate the 66 pin pairs to be compared. The operation of each individual comparator is identical; refer to Figure 5-6. Each comparator comprises 2 74174s whose data inputs are fed by a pin pair from the KGM and MUT. Their (1) outputs feed a pair of 7400 NAND gates whose outputs are XORed by a 7486. The output of the XOR feeds both an individual input of the Failure Summation logic and a 7474 latching flip-flop, which in turn is used to turn on a specific indicator.

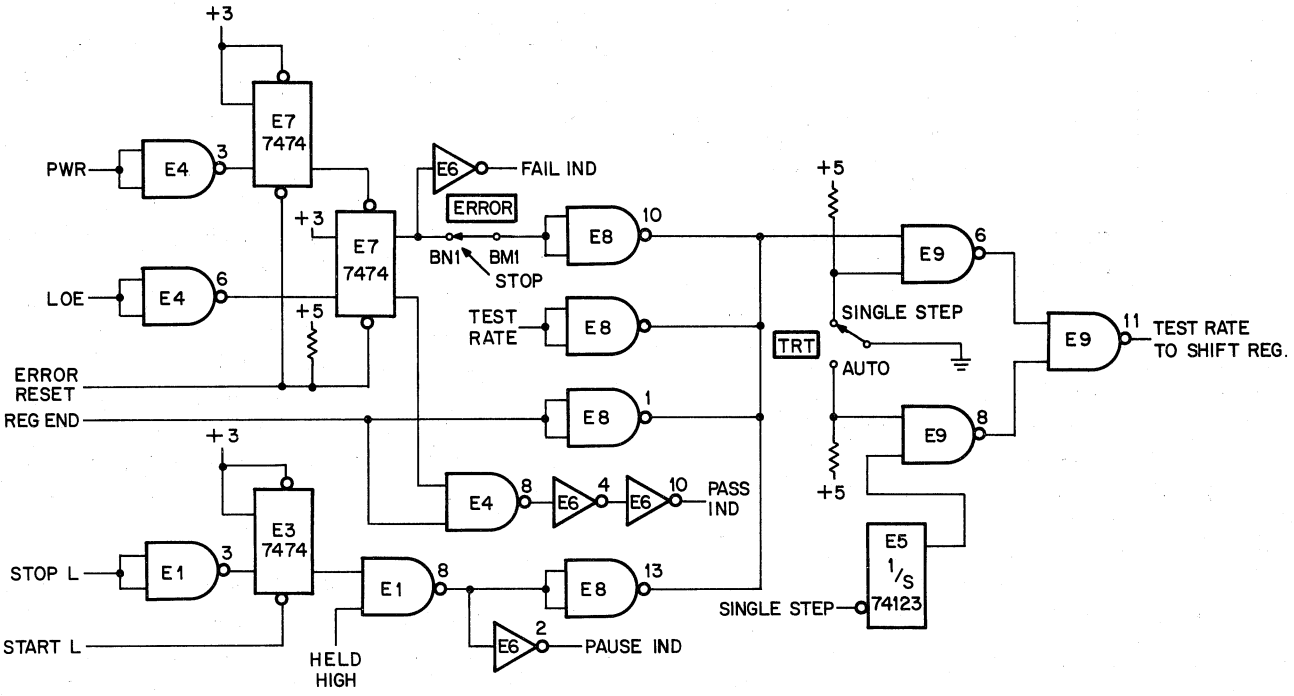

Figure 5-18 Pin Selector Control Logic

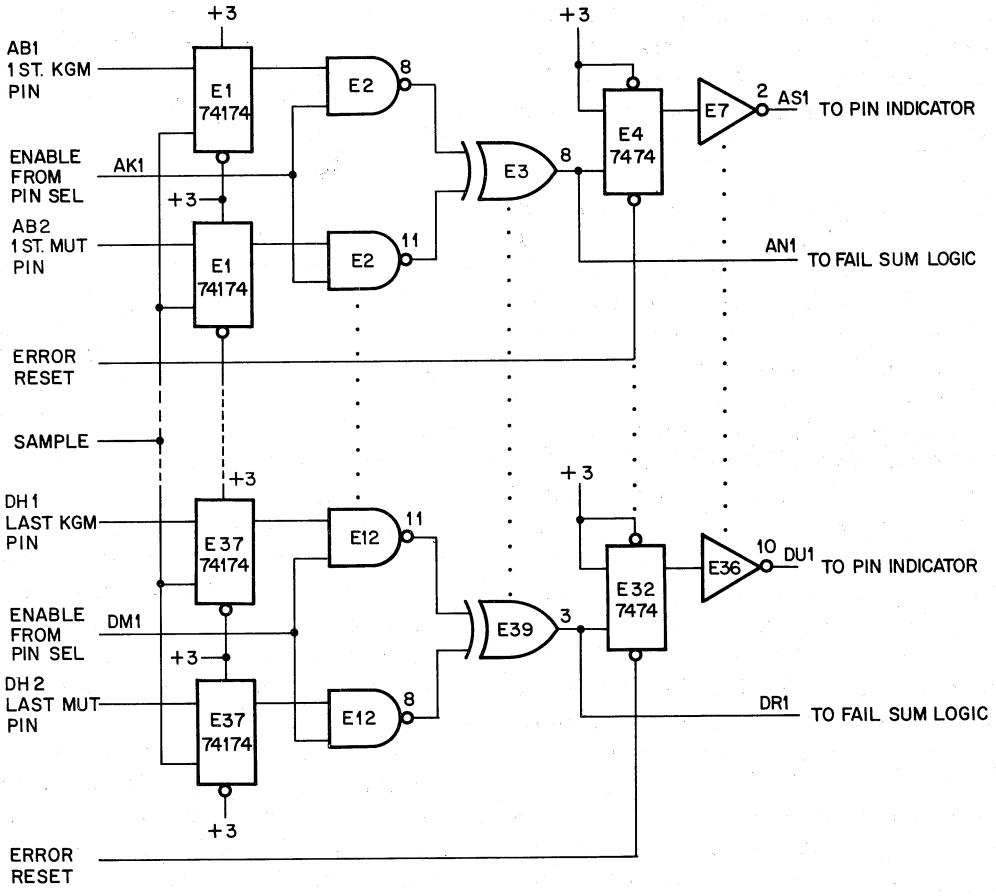

Figure 5-19 XOR Comparators Block Diagram

All input flip-flops are clocked commonly by SAMPLE RATE DELAY, and the NAND pairs are each enabled by the Pin Selector. In Random Mode, as previously explained, all gates are enabled at once; in Program Mode they are enabled one at a time, in sequence.

If at any time the output from a KGM pin does not match the output from the same pin on the MUT, when that pin is enabled by the selector, and during the period that it is being sampled, a signal will be summed in the Failure Summation logic, the 7474 will be clocked as a result of an XOR output, and the indicator will light, remaining lit as the 7474 locks up. Pressing ERROR RESET will clear the 7474, thereby extinguishing the indicator.

5.4.8 Failure Summation

The Failure Summation logic, (Drawing D-CS-G5000-0-1) is simplified in Figure 5-20. This logic functions to produce a Low Error Signal (LOE) whenever any input signal is present.

The logic comprises 10 314 NORs that feed 2 7430 NANDs. These in turn feed a single 7402 NOR. Inputs are the 66 XOR output lines from the pin comparators.

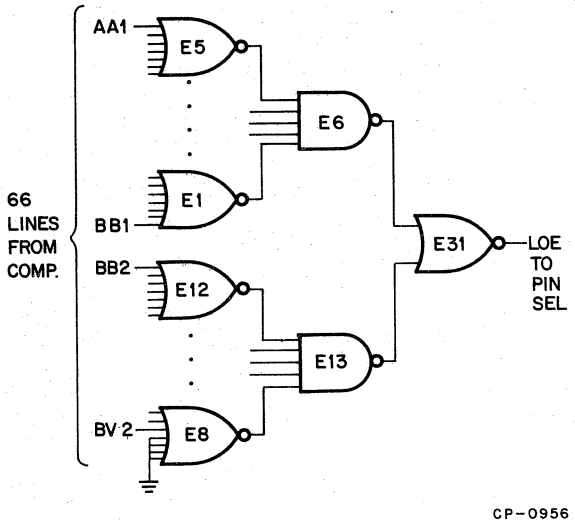

Figure 5-20 Fail Sum Block Diagram

The output signal LOE is used to stop the TEST RATE clock in the Pin Selector as described in Paragraph 5.4.6.

CHAPTER 6
MAINTENANCE

6.1 SCOPE

This chapter is concerned with maintenance of the 2340 XOR Test System. It does not discuss the use of the Tester in the maintenance of other equipment. Included is a list of test equipment required to perform these functions, procedures to be performed periodically to prevent malfunction, and steps to be taken if the equipment should fail due to component failure. It covers the maintenance philosophy assumed in the design of the unit and gives suggested methods to be used in its repair.

The procedures given in this chapter are recommended procedures, but do not encompass all possible methods that could be used in isolating trouble in the 2340 XOR Tester. Only through experience in its use and repair can an efficient repair procedure ultimately be derived.

The chapter does not include repair procedures for the power supplies or purchased subassemblies. For more information, refer to the specific repair documentation for these parts.

These procedures are based on a thorough understanding of the equipment and familiarity with the Manufacturing Drawing Set.

6.2 TEST EQUIPMENT REQUIRED

A list of basic test equipment required in the maintenance of the 2340 Test System is given in Table 6-1.

6.3 PREVENTIVE MAINTENANCE

Preventive maintenance tasks, performed regularly, will prevent premature breakdown of the equipment. These can be performed as part of the daily operating procedure (if the equipment is used on a daily basis), or prior to use (if the equipment is used infrequently). These procedures include cleaning, visual inspection, mechanical checks, and operational testing. Entries should be made in the Maintenance Log each time these procedures are performed to provide a source of troubleshooting information should repair become necessary due to a major malfunction.

6.3.1 Visual Inspection

A visual inspection of the 2340 comprises a check for broken connectors, broken or frayed insulation, improperly seated modules, worn or bent contacts in the test heads, or overheated components. For systems operating on a continual basis, these should be considered daily checks and are listed in brief in Paragraph 6.3.2.

Table 6-1
Maintenance Equipment

Equipment	Specifications	Equivalent
Oscilloscope	DC to 150 MHz	Tektronix Type 454
Probes	X10	Tektronix Type P6054
Integrated Circuit Extender	AP Inc.	DEC 29-10246
Pulse Generator		Datapulse 101
Multimeter		Triplett Model 310
Digital Voltmeter	4-1/2 digits min.	John Fluke Model 8100

6.3.2 Daily Checks

Proceed as follows:

1. With no modules in the test head, press POWER. All error lamps should light. If any do not, they need to be replaced. The POWER button should also light. If not, replace the indicator portion of the button.

2. Press POWER again to remove power from the system and check the cabinet for dirt or scratches.

3. Ensure that all modules under the cover are secure. See that modules are firmly seated in their slots.

4. Ensure that all internal connectors are secure; inspect the cables for any worn spots or fraying.

5. Inspect the contacts in the Test Heads to see that none are bent or broken.

6. Power up and see that ventilating fans are operating.

6.3.3 Maintenance Schedule (3 months or 5000 hours)

The following recommended procedures should be performed at the indicated interval. Their performance should be recorded in the Maintenance Log.

Task	Procedure
Clean	Clean the exterior and interior with a vacuum cleaner and/or clean cloth moistened in nonflammable solvent. Clean the ventilating system with a vacuum cleaner. Wipe fan blades with moistened cloth. See that their connections are secure.
Lubricate	Lubricate slide mechanisms and hinges with a light machine oil or graphite. Wipe off excess oil.
Inspect	Perform the tasks listed in the preceding subparagraph.
Check	Check power supply levels at the output of the supply and at key points on the backplane. Refer to the maintenance manual for the specific supply for values and to the 2340 drawing set for the key backplane points.

6.4 CORRECTIVE MAINTENANCE

Corrective maintenance consists of tasks performed when it has been determined that a malfunction exists within the equipment. When consistent errors show up for a series of the same module during testing, the "known good module" should be suspected, and another known good module substituted to see if the same malfunction persists. If it is determined that the XOR Tester is faulty, troubleshooting procedures should be conducted according to standard procedures used for all digital equipment. The procedure isolates the problem to a particular module in the test set and simply replaces that module with a spare. The isolated defective module should then be set aside for repair at a later time.

If replacement of the module does not clear the problem, investigate the power supply. Refer to documentation for the power supplies for proper readings.

Sporadic indications of error over several test runs when in Program Mode or in Random Mode can indicate marginal conditions in the 2340 Timing Chain. These frequencies can be checked at the front panel. The SYNC BNC supplies the basic 10 MHz frequency from the M405 Master Clock. If it is determined that this is at fault, replacement of this module will probably clear the fault. If the M405 is determined to be working properly, the frequency divider chain can be checked in a course fashion by checking at the ADAPTER RATE BNC. Note from Figure 5-8 that this will not check the 3 highest frequencies, nor will it check the 3 lowest frequencies in the chain. A finer check of the chain can be seen at the SAMPLE RATE BNC with the exception of 2 deleted frequencies from this switch.

6.4.1 Defective Components

When a specific module has been isolated as a malfunctioning module, the module should be replaced from spares and repaired at a later time.

When a module is repaired, standard troubleshooting techniques should be utilized in isolating the defective

component, using the theoretical descriptions given in Chapter 5, together with the logic block schematics supplied as part of the Manufacturing Drawing Set.

NOTE

Modules used in the 2340 cannot be XOR tested in the 2340 Test System.

The following maintenance notes are given as a general guide in these repair procedures.

Visual inspection of a module may reveal overheated or broken components or an etch. Otherwise, a multimeter can be used to check for continuity or to measure the resistance of a suspected component.

CAUTION

The X10 multimeter range is recommended for checking semiconductor devices.

Most multimeters apply a positive voltage to the common lead when adjusted for measuring resistance, therefore, the polarity of the multimeter leads should be checked before measuring the resistance of semiconductor devices.

ICs are complex integrated circuits with only the input, output, and power terminals available; thus, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is done best under dynamic conditions, using a module extender to make terminals readily accessible.

6.4.2 IC Locations

Figure 6-1 illustrates the component side of a typical DEC module. To locate a particular IC as identified in the block schematic (e.g., E7), proceed as follows:

1. Hold the module as shown in the figure, i.e., component side up.
2. ICs are numbered starting at the upper right-hand corner (connector side) counting toward the handle side of the board.
3. When a row is completed (E5 in Figure 6-1), the next IC is located in the next row at the contact end of the board.

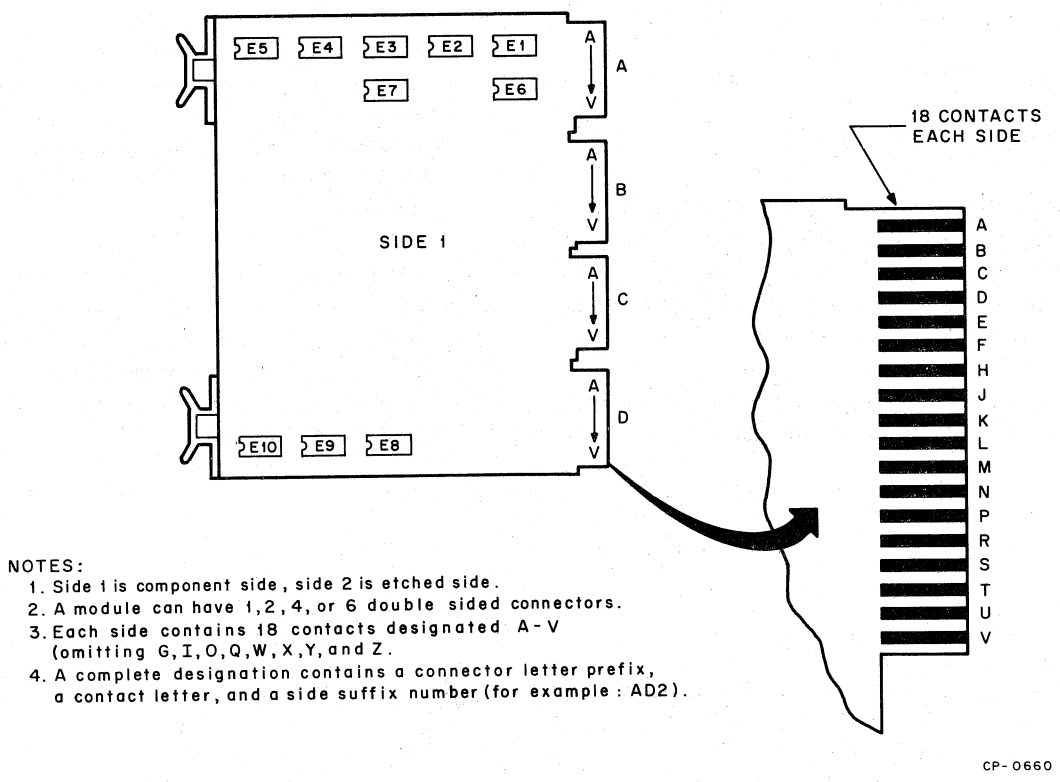

Figure 6-1 Physical Location of ICs on a Typical DEC Module

6.4.3 Repair and Replacement

When soldering semiconductor devices (transistors, diodes, rectifiers, or integrated circuits) that can be damaged by heat, physical shock, or excessive electrical current, the following precautions are recommended:

1. Use a heat sink, such as a pair of pliers, to grip the lead between the joint and the device being soldered.

2. Use a 6 V pencil-pointed tip soldering iron with an isolation transformer. The smallest iron adequate for the work should be used.

3. Perform the soldering operation in the shortest time possible to prevent damage to the component and delamination of the module etch.

4. ICs can be removed by using a solder sucker to remove all excess solder from the contacts. Then, by straightening the leads, lift the IC from its terminal points. If the defective IC is not be be saved for test purposes, perform steps 5 through 12. If the IC is to be saved, perform steps 8 through 12.

5. Clip the IC leads close to the chip.

6. Remove the chip portion of the IC.

7. Apply heat to individual leads (side 2) and remove leads from side 1, using a pair of needlenose pliers. Do not hold lead with pliers while applying heat; the pliers will act as a heat sink.

8. Heat each hole individually (side 2) removing excess solder with a desoldering tool.

9. Insert the new component, bending appropriate leads. (Only leads with tear drop lands should be bent; they should be bent in the direction of the point.)

10. Clip protruding component leads from side 2. Do not cut flush with the board. (Leads and solder joints should not exceed 1/16 inch from bottom of the board.)

11. Solder all leads on side 2.

12. Clean flux from both sides of the board with trichlorethylene, freon, or equivalent.

CAUTION

These cleaning agents will damage the plastic handles.

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excess solder or flux on adjacent parts or service lines. When repair has been completed, remove all excess flux by washing junctions with a solvent such as trichlorethylene. Do not expose paint or plastic surfaces to this solvent.

CAUTION

Never attempt to remove solder from the terminal points by heating and rapping the module against another surface. This practice can result in module or component damage. Remove solder with a solder sucking tool or solderwick.

When removing any part of the equipment for repair and replacement, all leads or wires that are unsoldered, or otherwise disconnected, should be legibly tagged or marked for identification with their respective terminals. Replace defective component only with parts of equal or better quality and of equal tolerance.

CHAPTER 7
DRAWINGS

7.1 GENERAL

This chapter contains a brief list of Manufacturing Drawing Numbers as referenced in this manual. For a complete list of drawings and actual block schematics, refer to Volume 2 of this manual.

7.2 REFERENCED ENGINEERING DRAWINGS

Table 7-1 lists those engineering drawings referenced in this manual.

Table 7-1
Referenced Engineering Drawings

Drawing No.	Title
D-CS-G5000-0-1	Failure Summation & Time Select
D-CS-G5001-0-1	Pin Selector
D-CS-G5002-0-1	22 Pin Comparator
D-CS-G5003-0-1	Random Pattern Generator #1
D-CS-G5004-0-1	Random Pattern Generator #2
D-CS-G5005-0-0	Random Pattern Generator #3
D-CS-G5006-0-1	Random Adapter
D-CS-G5007-0-1	Adapter Interface
D-CS-G5008-0-1	Indicator Module

7.3 LIST OF RECOMMENDED SPARES

A recommended list of spare parts for the 2340 Test System is given in Table 7-2.

Table 7-2
List of Recommended Spares

Description	Part Number	Qty
Compulite AC Power Switch	11-8-2-1-8	1
Compulite VDC Switch	28-6-9-2-2-8	1
Marco-Oak LED Indicator	QT/D2000	1
Alco Pushbutton Switch	MSPM 101C	2

Table 7-2
List of Recommended Spares

Description	Part Number	Qty
C&K Toggle Switch	7103-L1-Y-C-B-E	5
C&K Toggle Switch	7101-L1-Z-B-E	1
C&K Toggle Switch	7201-L1-Z-B-E	1
Power Supply Transformer	DIA-7008726-0-0	1
2 Pin Mate-N-Lok	1210822-01	1
8 Pin Mate-N-Lok	1210822-08	1
8 Pin Mate-N-Lok (Female)	1210821-08	1
Power Control	BC05 H-6	1
Pin Selector	G5001	1
Comparator	G5002	1
Adapter Interface	G5007	1
Random Adapter	G5006	1
Random Generator	G5005	1
Random Generator	G5004	1
Random Generator	G5003	1
Summation and Timing	G5000	1
Cable Connector	M908B	1
9 Pin Mate-N-Lok (Male)	129350-09	1
9 Pin Mate-N-Lok (Female)	129351-09	1
BNC Connector	1201444	1
Wired Over Top Conn. Block	H8514/MS 40102	1
Wired Over Top Conn. Block	H851	1
LEDs, LED Holders	11-10864	10
Crystal Clock	M405	1
3 Pin Mate-N-Lok	12-09350-03	1
3 Pin Mate-N-Lok	12-09351-03	1
15 Pin Mate-N-Lok	12-09350-15	1
15 Pin Mate-N-Lok	12-09351-15	1
Conn, 3M	12-11206	1
Bus Terminator Board MS 80292	M9007	2
10 MHz Crystal (Impach Sales)	HCL-19 (Clark)	1
Interface Module	G750 B YA	2
Test Head Interface Drivers	G751	2
Test Head Interface Drivers	G752	2
Rubber Feet	9008190	4

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Maynard, Massachusetts

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printed in U.S.A.