Vishay Telefunken

# 2.7 V to 5.5 V Serial Infrared Transceiver Module Family (SIR, 115.2 kbit/s)



## Description

VISHA

The TFDU4100, TFDS4500, and TFDT4500 are a family of low–power infrared transceiver modules compliant to the IrDA 1.2 standard for serial infrared (SIR) data communication, supporting IrDA speeds up to 115.2 kbit/s. Integrated within the transceiver modules are a photo PIN diode, infrared emitter (IRED), and a low–power analog control IC to provide a total front–end solution in a single package. Telefunken's SIR transceivers are available in three package options, including our BabyFace package (TFDU4100), the smallest SIR transceiver available

#### Features

- Compliant to IrDA 1.2 (Up to 115.2 kbit/s)
- 2.7 to 5.5 V Wide Operating Voltage Range
- Low–Power Consumption (1.3 mA Supply Current)
- Power Sleep Mode Through V<sub>CC1</sub>/SD Pin (5 nA Sleep Current)
- Long Range (Up to 3.0 m at 115.2 k/bit/s)
- Three Surface Mount Package Options
  - Universal (9.7  $\times$  4.7  $\times$  4.0 mm)
  - Side View  $(13.0 \times 5.95 \times 5.3 \text{ mm})$
  - Top View  $(13.0 \times 7.6 \times 5.95 \text{ mm})$

### Applications

- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors

# **Package Options**

TFDU4100 Baby Face (Universal)



on the market. This wide selection provides flexibility for a variety of applications and space constraints. The transceivers are capable of directly interfacing with a wide variety of I/O chips which perform the pulse–width modulation/demodulation function, including Telefunken's TOIM3000/TOIM3232. At a minimum, a current–limiting resistor in series with the infrared emitter and a  $V_{CC}$  bypass capacitor are the only external components required to implement a complete solution.

- BabyFace (Universal) Package Capable of Surface Mount Solderability to Side and Top View Orientation
- Directly Interfaces with Various Super I/O and Controller Devices and Telefunken's TOIM3000 and TOIM3232 I/Os
- Built–In EMI Protection No External Shielding Necessary
- Few External Components Required
- Backward Compatible to all Telefunken SIR Infrared Transceivers
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video Conferencing Systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection Devices

TFDS4500 Side View



TFDT4500 Top View



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# **Ordering Information**

Part Number	Qty / Reel	Description
TFDU4100-TR3	1000 pcs	Oriented in carrier tape for side view surface mounting
TFDU4100-TT3	1000 pcs	Oriented in carrier tape for top view surface mounting
TFDS4500-TR3	750 pcs	
TFDT4500–TR3	750 pcs	

# **Functional Block Diagram**

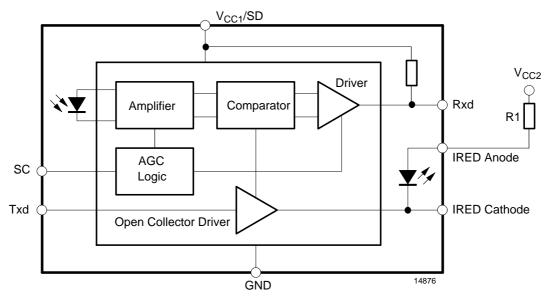


Figure 1. Functional Block Diagram

# **Pin Description**

Pin Number		Function	Description	I/O	Active
"U" and "T" Option	"S" Option				
1	8	IRED Anode	IRED anode, should be externally connected to $V_{CC2}$ through a current control resistor		
2	1	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	7	Txd	Transmit Data Input	I	HIGH
4	2	Rxd	Received Data Output, open collector. No external pull–up or pull–down resistor is required (20 k $\Omega$ resistor in- ternal to device). Pin is inactive during transmission.	0	LOW
5	6	NC	Do not connect		
6	3	V <sub>CC1</sub> / SD	Supply Voltage / Shutdown		
7	5	SC	Sensitivity control		HIGH
8	4	GND	Ground		

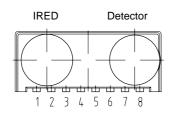


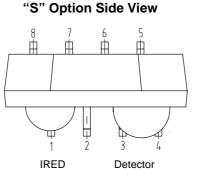
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# TFDU4100/TFDS4500/TFDT4500

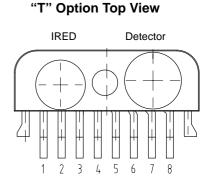
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#### "U" Option BabyFace (Universal)





#### Figure 2. Pinnings



### **Absolute Maximum Ratings**

Reference point Pin GND unless otherwise noted. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Тур.	Max.	Unit
Supply Voltage Range		V <sub>CC1</sub>	- 0.5		6	V
Input Currents	For all Pins, except IRED Anode Pin				10	mA
Output Sink Current					25	mA
Power Dissipation	See Derating Curve	PD			200	mW
Junction Temperature		TJ			125	°C
Ambient Temperature Range (Operating)		T <sub>amb</sub>	-25		+85	°C
Storage Temperature Range		T <sub>stg</sub>	-25		+85	°C
Soldering Temperature	See Recommended Solder Profile			215	240	°C
Average IRED Current		I <sub>IRED</sub> (DC)			100	mA
Repetitive Pulsed IRED Current	t < 90 μs, t <sub>on</sub> < 20%	I <sub>IRED</sub> (RP)			500	mA
IRED Anode Voltage		V <sub>IREDA</sub>	- 0.5		V <sub>CC1</sub> +0.5	V
Transmitter Data Input Voltage		V <sub>Txd</sub>	- 0.5		V <sub>CC1</sub> +0.5	V
Receiver Data Output Voltage		V <sub>Rxd</sub>	- 0.5		V <sub>CC1</sub> +0.5	V
Virtual Source Size	Method: (1–1/e) encircled energy	d	2.5	2.8		mm
Maximum Intensity for Class 1 Operation of IEC825–1 or EN60825–1 (worst case IrDA SIR pulse pattern *)	EN60825, 1997				400	mW/sr

#### \* Note:

Transmitted data: continuously transmitted "0". In normal data transfer operation "0" and "1" will be transmitted with the same probability. Therefore, for that case, about a factor of two of safety margin is included. However, for worst case thermal stress testing such data pattern are often used and for this case the 400 mW/sr value has to be taken.

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### **Electrical Characteristics**

 $T_{amb} = 25^{\circ}C$ ,  $V_{CC} = 2.7$  V to 5.5 V unless otherwise noted. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions / Pins	Symbol	Min.	Тур.	Max.	Unit
Transceiver						
Supply Voltage	Receive Mode Transmit Mode, $R2 = 47 \Omega$ (see Recommended Application Circuit)	V <sub>CC1</sub>	2.7 2.0		5.5 5.5	V V
Supply Current Pin V <sub>CC1</sub> (Receive Mode)	V <sub>CC1</sub> = 5.5 V V <sub>CC1</sub> = 2.7 V	I <sub>CC1 (Rx)</sub>		1.3 1.0	2.5 1.5	mA mA
Supply Current Pin V <sub>CC1</sub> (avg) (Transmit Mode)	$I_{IRED} = 210 \text{ mA}$ (at IRED Anode Pin) $V_{CC1} = 5.5 \text{ V}$ $V_{CC1} = 2.7 \text{ V}$	I <sub>CC1 (Tx)</sub>		5.0 3.5	5.5 4.5	mA mA
Leakage Current of IR Emitter, IRED Anode Pin	V <sub>CC1</sub> = OFF, T <sub>XD</sub> = LOW, V <sub>CC2</sub> = 6 V, T = 25 to 85°C	I <sub>L (IREDA)</sub>		0.005	0.5	μΑ
Transceiver Power On Settling Time		T <sub>PON</sub>		50		μs

# **Optoelectronic Characteristics**

 $T_{amb} = 25^{\circ}C$ ,  $V_{CC} = 2.7$  V to 5.5 V unless otherwise noted. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Тур.	Max.	Unit			
Receiver									
Minimum Detection	BER = $10^{-8}$ (IrDA Specification)								
Threshold Irradiance	$\alpha = \pm 15^{\circ}$ , SIR Mode, SC = LOW	E <sub>e</sub>		20	35	mW/m <sup>2</sup>			
	$\alpha = \pm 15^{\circ}$ , SIR Mode, SC = HIGH	E <sub>e</sub>	6	10	15	mW/m <sup>2</sup>			
Maximum Detection	$\alpha = \pm 90^{\circ}$ , SIR Mode, V <sub>CC1</sub> = 5 V	Ee	3.3	5		kW/m <sup>2</sup>			
Threshold Irradiance	$\alpha = \pm 90^{\circ}$ , SIR Mode, V <sub>CC1</sub> = 3 V	E <sub>e</sub>	8	15		kW/m <sup>2</sup>			
Logic LOW Receiver Input Irradiance	SC = HIGH or LOW	E <sub>e</sub>			4	mW/m <sup>2</sup>			
Output Voltage –	Active, C = 15 pF, R = 2.2 k $\Omega$	V <sub>OL</sub>		0.5	0.8	V			
Rxd	Non–active, C = 15 pF, R = 2.2 k $\Omega$	V <sub>OH</sub>	V <sub>CC1</sub> -0.5			V			
Output Current – Rxd	V <sub>OL</sub> < 0.8 V	I <sub>OL</sub>		4		mA			
Rise Time – Rxd	C = 15 pF, R = 2.2 k $\Omega$	t <sub>r (Rxd)</sub>	20		1400	ns			
Fall Time – Rxd	C = 15 pF, R = 2.2 k $\Omega$	t <sub>f (Rxd)</sub>	20		200	ns			
Pulse Width – Rxd Output	Input pulse width = 1.6 μs, 115.2 kbit/s	t <sub>PW</sub>	1.41		8	μs			
Jitter, Leading Edge of Output Signal	Over a Period of 10 bit, 115.2 kbit/s	ti			2	μs			
Latency		tL		100	500	μs			





# **Optoelectronic Characteristics**

 $T_{amb} = 25^{\circ}C$ ,  $V_{CC} = 2.7$  V to 5.5 V unless otherwise noted. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Тур.	Max.	Unit
Transmitter						
IRED Operating Current	IRED Operating Current can be adjusted by Variation of R1. Current Limiting Resistor is in Series to IRED: R1 = 14 $\Omega$ , V <sub>CC2</sub> = 5.0 V	I <sub>IRED</sub>		0.2	0.28	A
Logic LOW Transmitter Input Voltage		V <sub>IL</sub> (Txd)	0		0.8	V
Logic HIGH Transmitter Input Voltage		V <sub>IH</sub> (Txd)	2.4		V <sub>CC1</sub> +0.5	V
Output Radiant Intensity	In Agreement with IEC825 Eye Safety Limit, if Current Limiting Resistor is in Series to IRED: R1 = 14 $\Omega$ , V <sub>CC2</sub> = 5.0 V, $\alpha = \pm 15^{\circ}$	l <sub>e</sub>	45	140	200	mW/sr
	Txd Logic LOW Level	l <sub>e</sub>			0.04	mW/sr
Angle of Half Intensity		α		±24		0
Peak Wavelength of Emission		$\lambda_{\rm P}$	880		900	nm
Half–Width of Emis- sion Spectrum				60		nm
Optical Rise Time, Fall Time		t <sub>ropt,</sub> t <sub>fopt</sub>		200	600	ns
Optical Overshoot					25	%
Rising Edge Peak- to-Peak Jitter of Op- tical Output Pulse	Over a Period of 10 bits, Independent of Information content				0.2	μS

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### **Recommended Circuit Diagram**

The only required components for designing an IrDA 1.2 compatible design using Telefunken SIR transceivers are a current limiting resistor to the IRED. However, depending on the entire system design and board layout, additional components may be required (see figure 3).

It is recommended that the capacitors C1 and C2 are positioned as near as possible to the transceiver power supply pins. A tantalum capacitor should be used for C1, while a ceramic capacitor should be used for C2 to suppress RF noise. Also, when connecting the described circuit to the power supply, low impedance wiring should be used.

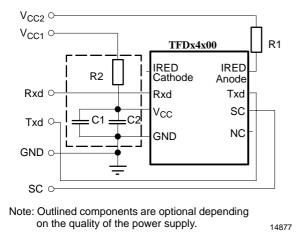


Figure 3. Recommended Application Circuit

R1 is used for controlling the current through the IR emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the resistor should be increased. For typical values of R1 (see figures 4 and 5), e.g. for IrDA compliant operation ( $V_{CC2} = 5 V \pm 5\%$ ), a current control resistor of 14  $\Omega$  is recommended. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet and the eye safety limitations given by IEC825–1.

R2, C1 and C2 are optional and dependent on the quality of the supply voltage  $V_{CC1}$  and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

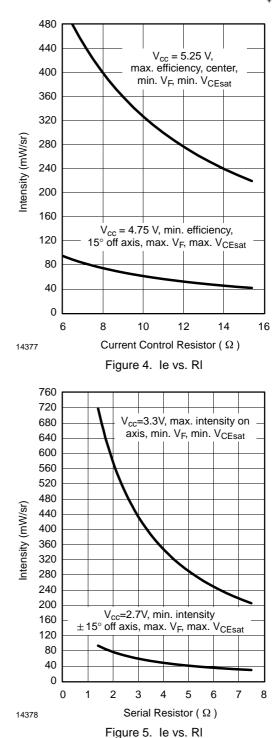


Figure 5. le vs. Ki

Table 1. Recommended Application Circuit Components

Component	Recommended Value		
C1	4.7 μF, Tantalum		
C2	0.1 μF, Ceramic		
R1	14 $\Omega$ , 0.25 W (recommend using two		
	7 $\Omega$ , 0.125 W resistors in series)		
R2	47 Ω , 0.125 W		



The sensitivity control (SC) pin allows the minimum detection irradiance threshold of the transceiver to be lowered when set to a logic HIGH. Lowering the irradiance threshold increases the sensitivity to infrared signals and increases transmission range up to 3 meters. However, setting the Pin SC to logic HIGH also makes the transceiver more susceptable to transmission errors due to an increased sensitivity to fluorescent light disturbances. It is recommended to set the Pin SC to logic LOW or left open if the increased range is not required or if the system will be operating in bright ambient light.

The guide pins on the side-view and top-view packages are internally connected to ground but should not be connected to the system ground to avoid ground loops. They should be used for mechanical purposes only and should be left floating.

#### Shutdown

The internal switch for the IRED in Telefunken SIR transceivers is designed to be operated like an open collector driver. Thus, the V<sub>cc2</sub> source can be an unregulated power supply while only a well regulated power source with a supply current of 1.3 mA connected to V<sub>CC1</sub>/SD is needed to provide power to the remainder of the transceiver circuitry in receive mode. In transmit mode, this current is slightly higher (approximately 4 mA average at 3 V supply current) and the voltage is not required to be kept as stable as in receive mode. A voltage drop of V<sub>CC1</sub> is acceptable down to about 2.0 V when buffering the voltage directly from the Pin V<sub>CC1</sub> to GND see figure 3).

This configuration minimizes the influence of high current surges from the IRED on the internal analog control circuitry of the transceiver and the application circuit. Also board space and cost savings can be achieved by eliminating the additional linear regulator normally needed for the IRED's high current requirements.

The transceiver can be very efficiently shutdown by keeping the IRED connected to the power supply  $V_{CC2}$  but switching off  $V_{CC1}$ /SD. The power source to  $V_{CC1}$ /SD can be provided directly from a microcontroller (see figure 6). In shutdown, current loss is realized only as leakage current through the current limiting resistor to the IRED (typically 5 nA). The settling time after switching  $V_{CC1}$ /SD on again is

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approximately 50  $\mu$ s. Telefunken's TOIM3232 interface circuit is designed for this shutdown feature. The V<sub>CC\_SD</sub>, S0 or S1 outputs on the TOIM3232 can be used to power the transceiver with the necessary supply current.

If the microcontroller or the microprocessor is unable to drive the supply current required by the transceiver, a low–cost SOT23 pnp transistor can be used to switch voltage on and off from the regulated power supply (see figure 7). The additional component cost is minimal and saves the system designer additional power supply costs.

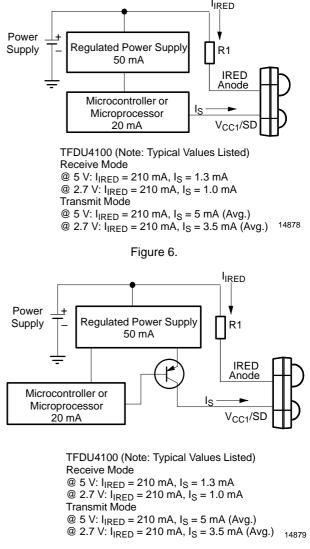


Figure 7.

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### **Recommended SMD Pad Layout**

The leads of the device should be soldered in the center position of the pads.

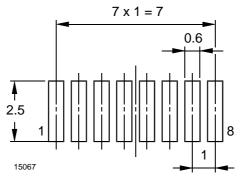


Figure 8. TFDU4100 BabyFace (Universal)

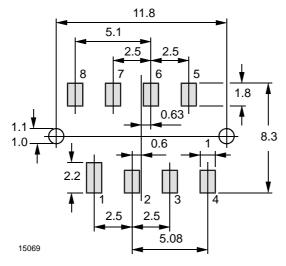


Figure 9. TFDS4500 Side View Package

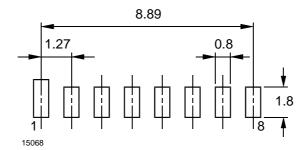


Figure 10. TFDT4500 Top View Package Note: Leads of the device should be at least 0.3 mm within the ends of the pads. Pad 1 is longer to designate Pin 1 connection to transceiver.



### **Recommended Solder Profile**

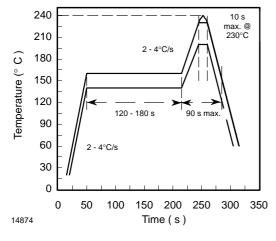


Figure 11. Recommended Solder Profile

#### **Current Derating Diagram**

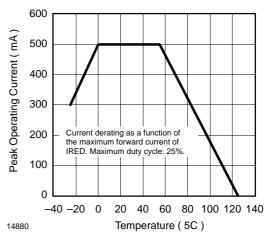
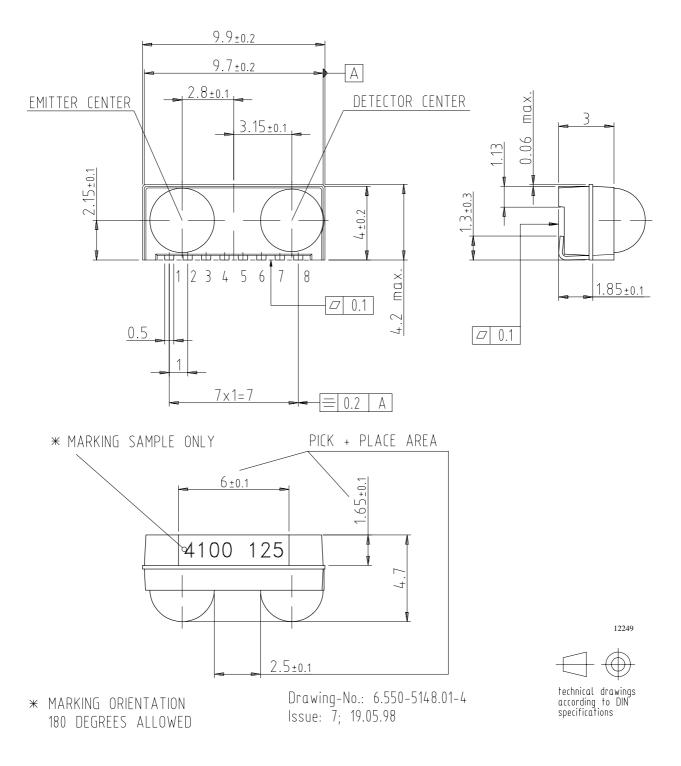


Figure 12. Current Derating Diagram

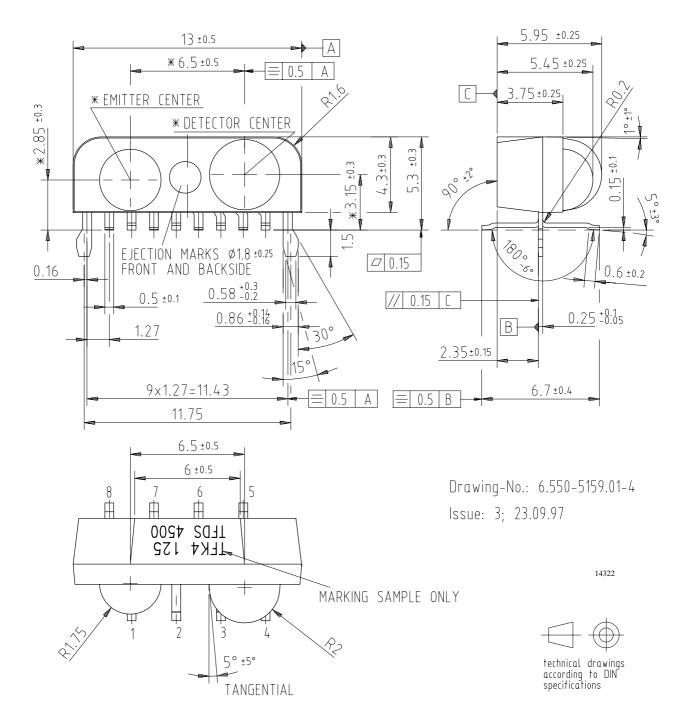


## TFDU4100 – BabyFace (Universal) Package (Mechanical Dimensions)



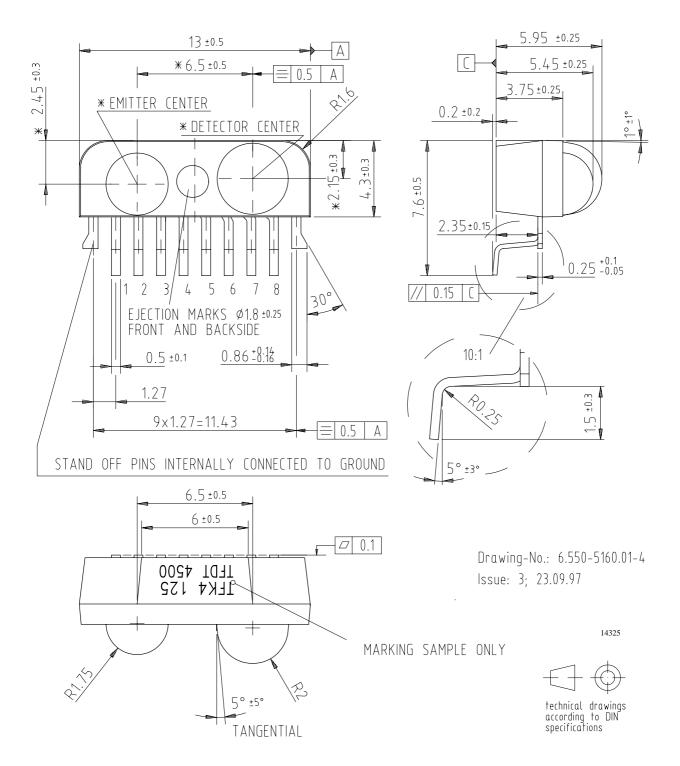








# **TFDT4500 – Top View Package (Mechanical Dimensions)**





### **Ozone Depleting Substances Policy Statement**

It is the policy of Vishay Semiconductor GmbH to

- 1. Meet all present and future national and international statutory requirements.
- 2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

- 1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
- 2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
- 3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice. Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Telefunken products for any unintended or unauthorized application, the buyer shall indemnify Vishay Telefunken against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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# TOIM3000/ 3232 Design Notes

# TOIM3xxx



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# IrDA Port and Serial Port Time Multiplexing

The TOIM3xxx is a low-cost device that allows the systems designer to integrate IrDA capability into a notebook computer using the UART NSC16550/16450 or equivalent. At one end, the TOIM3xxx interfaces directly with an IrDA port and a serial RS232 port, while at the other end, the 16550. Figure 2 provides an example of a how to time multiplex the 16550 to an IrDA port and a serial RS232 port:

The OUT1 signal from the NSC16550 plays the role of selecting either the IrDA port or the RS232 port. When RESET=0, the TOIM3xxx communicates with the IrDA port, while data communication from/to the RS232 port is blocked. On the other hand, when RESET=1, the TOIM3xxx communicates with the RS232 port while data communication from/to the IrDA port is blocked.

Please note that the TOIM3xxx always operates in half-duplex mode, as specified by the IrDA standard. That is, whenever the TOIM3xxx transmits, the receiver is blocked and is inactive, and vice versa.

# **Operation Description** Features only for TOIM3000

The TOIM3000 uses two clocks from the UART: the 1.8432 MHz clock and the Baud\_out clock for its internal timing. Both are connected to XIN and B\_CLK, respectively. The B\_CLK is used as a reference for pulse stretching whereas XIN is used as a time base for pulse shortening to 1.627 µs and noise filtering.

#### Single clock operation

TOIM3000 can be operated with only a single clock. In this case, the B\_CLK and XIN are tight together and connected to the Baudout pin of the UART. The pulse width is then shortened to 3/16 of the bit length and noise filtering is deactivated. S1 is to be connected to V<sub>CC</sub> and S0 to GND.

We strongly recommend not to use this mode in battery-operated systems because the 3/16pulse length at lower bit rates consumes more power than the shorter pulses. At a baud rate of 9600 bit/s, the ratio of power consumption of both modes is a factor of 12 (!).

The TOIM3000 interfaces to an RS232 level converter through two pins, RD\_232 and TD\_232. These two pins provide the extra function that a single TOIM3000 IC can time share with both an infrared IrDA port and an RS232 port. Whenever RESET = 0, the TOIM3000 links to the infrared transceiver TFDS3000 through RD\_IR and TD\_IR pins. On the other hand, when RESET = 1, the TOIM3000 links to the RS232 port through RD\_232 and TD\_232 pins.

# Features only for TOIM3232

The baud rate at which an RS232 serial port communicates with the external adapter is programmable inside the TOIM3232. This programmable baud rate should be used when the baud clock and the UART oscillator clock are not available. When BR/D = 0, the TOIM3232 inter-prets the signals at RD\_232 and RD\_IR pins as data to be transmitted and received data. On the other hand, whenever BR/D = 1, the TOIM3232 interprets the seven LSBs at the RD\_232 input as the control word. The operating baud rate will change to its supposedly new baud rate when the BR/D returns back to LOW ("0").

RS232 9-pin connector	Level converte	er	TOIN	M3232	TF	DS3000
Pin 4, DTR	<b>_</b>	→ R	ESET	VCC_S	SD-	VCC
Pin 7, RTS	▶	→ B]	$R/\overline{D}$	TD_	IR -	Txd
Pin 3, TXD	_►	→TI	D_UA	$RT \overline{RD}$	 IR ◀	Rxd
Pin 2, RXD	•		D_UA			
		L	X1	_  ■	$\Box_{X2}$	2
			3.	.6842 N	1Hz	

Figure 1. TOIM3232 – RS232 port interface (external infrared adapter)

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#### Control Byte (8 bit)

<first char=""></first>			<second char=""></second>				
Х	S2	<b>S</b> 1	<b>S</b> 0	B3	B2	B1	B0

where

X:	Don't care				
S1, S2:	User-programmable bit				
S0:	IrDA pulse select				
	= (1) 1.627 $\mu$ s output pulses				
	= (0) 3/16 bit time pulses *)				
B0 B3:	Baud rate selects, $B0 = LSB$				

\*) not recommended

#### **Baud Rate Select Words**

Note: IrDA standard only supports 2.4, 9.6, 19.2, 57.6, and 115.2 kbit/s.

B3	B2	B1	B0	Second	Baud Rate
				Char.	
0	0	0	0	0	115.2 k
0	0	0	1	1	57.6 k
0	0	1	0	2	38.4 k
0	0	1	1	3	19.2 k
0	1	0	0	4	14.4 k
0	1	0	1	5	12.8k
0	1	1	0	6	9.6k
0	1	1	1	7	7.2 k
1	0	0	0	8	4.8 k
1	0	0	1	9	3.6 k
1	0	1	0	А	2.4 k
1	0	1	1	В	1.8 k
1	1	0	0	С	1.2 k

# IrDA-Compliant 1.63 µs Pulse Hardwiring

The IrDA standard specifies the minimum pulse width as 1.41µs, regardless of the baud

rate, and nominal as 3/16 bit time. Setting the output pulse as 1.63 µs for all baud rates saves LED current for those baud rates below 115.2 Kb/s. For the baud rate = 115.2 Kb/s, the 1.63us pulse mode is equivalent to 3/16 bit time mode, so there is no power saving at this baud rate for either scheme. However, for those baud rates below 115.2 Kb/s, the 3/16 bit time pulses becomes larger as the baud rate decreases. At 9600 bit/s communication, the 3/16 bit time pulse is 19.5 µs, which is 12 times more consumption current than a 1.63 µs pulse per output pulse. For notebook applications, since power saving is critical, we therefore recommend setting the pulse width at 1.63 μs.

The 1.63 µs pulses are generated by counting 3 clocks from the 1.8632 MHz clock. It is assumed that the 1.8632 MHz clock is readily available as the input clock driving the NSC 16550 and or output thereof. The designer must make sure the clock output from the NSC 16550:XOUT is 1.8632 MHz. If the 1.8632 MHz clock is not available, the designer must use an extra crystal to generate this clock. The 1.8632 MHz clock does not have to be synchronized to the 16 x baud rate clock.

The additional and important advantage of using the 1.63  $\mu$ s mode is the digital filtering capability of the TOIM3000. The TOIM3000 uses the 1.8632 MHz clock to drive the digital filtering circuitry. Input infrared pulses of length less than one clock should then be filtered out. The following specifications must be set for this mode: S1=GND and S0=GND (see figure 3 for exact circuit connections).

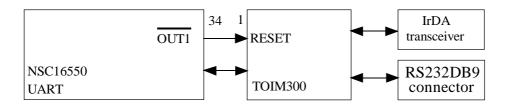


Figure 2. Using RESET to select communication port

# IrDA-Compliant 3/16 Bit Time Hardwiring

If a 1.8632 MHz clock isn't available, the 3/16 bit time pulse can be used. The TOIM3000 can be hardwire-configured to output 3/16 bit time pulses.

Mode 3/16 bit time consumes more current than the 1.63 µs mode at baud rates slower than 115.2 Kb/s. At 115.2 Kb/s, current consumption is identical regardless whether the 3/16 bit time or 1.63 µs mode is used. For notebook applications, we strongly recommend using the 1.63 µs mode as explained in "IrDA-Compliant 1.63 µs Pulse Hardwiring". There are two reasons for this:

- Power saving
- Infrared signal input noise digital filtering.

Mode 3/16 bit time DOES NOT have digital filtering. Therefore, the TOIM3000 is vulner-able to noise at the infrared signal input into the TOIM3000.

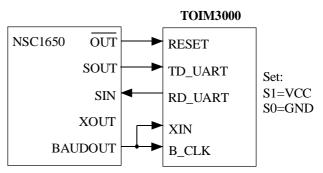
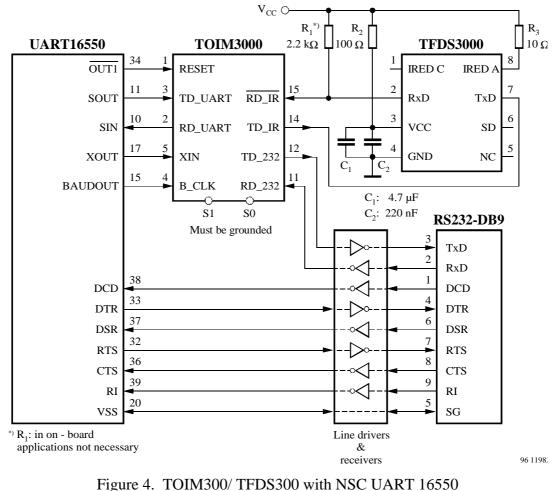


Figure 3. 3/16 bit time hardwiring



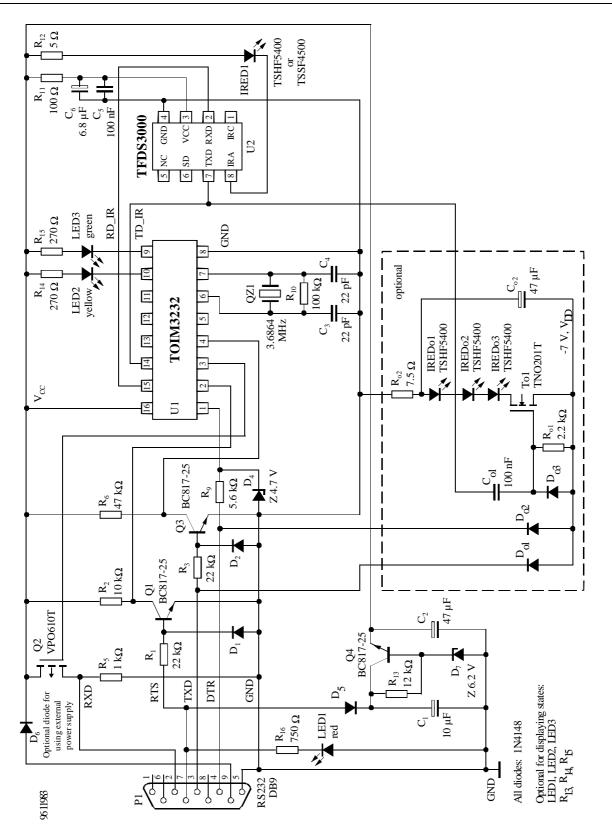


Figure 5. IrDA at RS232 port solution with discrete interface to RS232 port, PCB information, component placement, bill of material (see Appendix)

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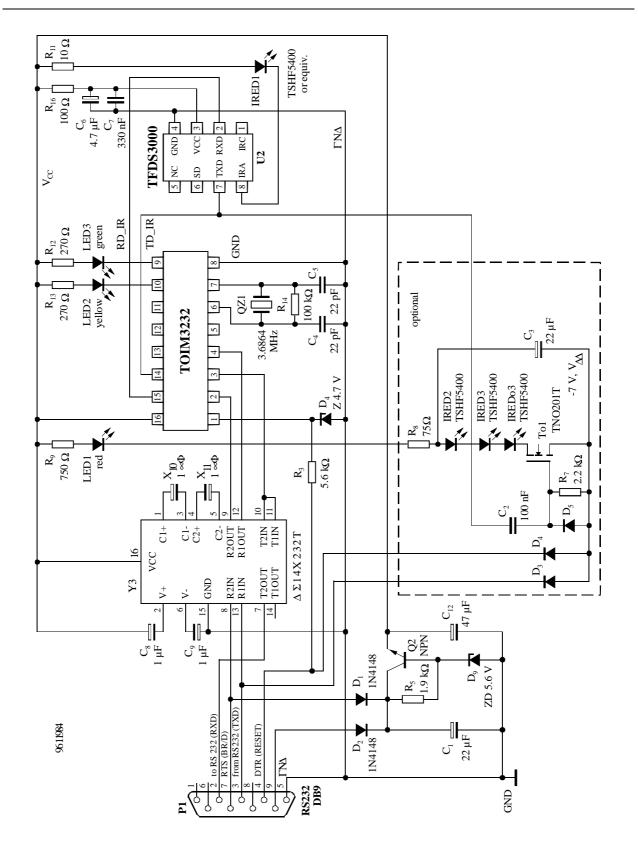


Figure 6. Solution with integrated interface to RS232 port

# TOIMxxx

# Appendix

# **Bill of Materials IrDA RS232 Adapter**

Item	Quantity	Reference	Part	
1	1	U1	TOIM3232	
2	1	U2	TFDS3000	
3	1	C1	10 µF, 16 V	
4	1	C <sub>2</sub>	47 μF, 10 V	
5	1	C3	22 pF	
6	1	C4	22 pF	
7	1	C5	100 nF	
8	1	C <sub>6</sub>	6.8 μF, 6.3 V Tantalum	
9	1	D1	1N4148	
10	1	D <sub>2</sub>	1N4148	
11	1	D3	Z4.7 V	
12	1	 D5	1N4148	
13	1	IRED1	TSHF5400	
14	1	D7	Z6.2 V	
15	1	, Р1	Connector, DB9	
16	1	Q1	BC817-25	
17		Q2	VP0610T	
18	1	Q3	BC817-25	
19	1	Q4	BC817-25	
20	1	QZ1	Quartz, 3.6864 MHz	
		X21	or ceram. resonator CSAC3.68MGC-TC,	
			Murata	
21	1	R1	22 k	
22	1	R2	10 k	
23	1	R3	22 k	
24	1	R4		
25	1	R5	1 k	
26	1	R <sub>6</sub>	47 k	
27	1	R7		
28	1	R8		
29	1	R9	5.6 k	
30	1	R <sub>10</sub>	100 k	
31	1	R <sub>11</sub>	100	
32	2	R <sub>12</sub>	$(2 \times 10 \text{ in parallel}) = 5$	
33	1	R <sub>13</sub>	12 k	
34	1	РСВ	TEMIC demo board	

Optional Display (recommended only with external power supply)				
35	1	LED1	LED, red, power on state display	
36	1	LED2	LED, yellow, status	
37	1	LED3	LED, green, status	
38	1	R <sub>16</sub>	750, power-on state display	
39	1	R <sub>14</sub>	270, status	
40	1	R <sub>15</sub>	270, status	

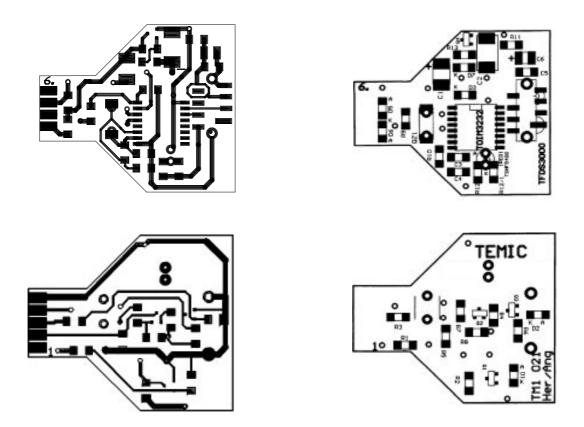
Optional Power Booster				
41	1	Ro <sub>1</sub>	2.2 k	
42	1	Ro <sub>2</sub>	7.5	
43	1	To <sub>1</sub>	TN0201T	
44	1	Co <sub>1</sub>	100 nF	
45	1	Co <sub>2</sub>	47 μF 16 V	
46	1	Do1	1N4148	
47	1	Do2	1N4148	
48	1	Do3	1N4148	
49	1	D <sub>6</sub>	1N4148 for external power supply	
50	1	IREDo1	TSHF5400	
51	1	IREDo2	TSHF5400	
52	1	IRED03	TSHF5400	

### (bold = TEMIC parts)



# **Board Layout and Component Placement**

Component placement, 9 Pin RS232 connector not shown.



# Software for the TOIM3232

The control word is composed of two characters, written in hexadecimal, in format: YZ

#### **UART Programming**

For proper operation, the RS232 must be programmed to send a START bit plus an 8 bit data word, YZ and no STOP bit for every word sent. The transfer rate for programming must be identical with the formerly programmed data rate, or after resetting the TOIM3232, the default rate of 9600 bit/s is used.

#### Software Algorithm

STEP	RESET	BR/D	RD_UART	TD_UART	RD_IR	TD_IR	COMMENTS
1	HIGH	Х	Х	Х	Х	Х	Resets all internal registers. Resets IrDA default baud rate of 9600 bit/s.
2	LOW	Х	Х	Х	Х	Х	Wait at least 7 µs.
3	LOW	HIGH	Х	Х	Х	Х	Wait at least 7 µs. The TOIM3232 now enters the control word (programming) mode.
4	LOW	HIGH	YZ with Y = 1 for $1.627 \ \mu s$ Y = 0 for $3/16 \ bit$ length	Х	Х	Х	Sending the control word YZ. Send '1Z' if 1.627 $\mu$ s pulses are used. Otherwise send '0Z' if 3/16 bit pulses are used. 'Y6' keeps the 9.6 kbit/s data rate, whereas the '0Z' selects the 3/16 bit time pulses. Z = 0 sets to 115.2 kbit/s. Then wait at least 1 $\mu$ s for hold–time.
5	LOW	LOW	DATA	DATA	DATA	DATA	Data communication between the TOIM3232 and the RS232 port has been established by BR/D LOW. The TOIM3232 now enters the data transmission mode. Both RESET and BR/D must be kept LOW ('0') during data mode. Software can re-program a new data rate by re-starting from step 3. The UART also must be set to the correct data rate ***).

\*\*\*) For programming the UART, refer to e.g., National Semiconductor's data sheet of PC 16550 UART



## **Examples for Programming the RS232 Port and TOIM3232**

#### **Demo Program for Transmitting ASCII Characters**

DECLARE SUB dtrreset () DECLARE SUB rtsbrdline () DECLARE SUB progtoim () **DECLARE SUB proguart ()** DECLARE SUB progtoimsh () DECLARE SUB dataout () DECLARE SUB proof () CLS DIM SHARED pro AS INTEGER DIM SHARED sig AS INTEGER **DIM SHARED asci AS INTEGER DIM SHARED rts**\$ DIM SHARED bdrate AS LONG 'Programmed for COM1, base address 3f8. ' In case of COM3 use 3e instead of 3f ' In case of COM2 use 2f instead of 3e ' In case of COM4 use 2e instead of 3e 'apply power supply voltage to dongle rts\$ = "LO" 'Vcc high, pin2 LOW CALL rtsbrdline 'sets rts=br/d - switch to  $V_{CC}$ 'Reset UART and PLD to default conditions CALL dtrreset 'In demo board the reset line is not(!) inverted 'Resets the TOIM3232 to 9600 bd bdrate = 9600CALL proguart 'sets the UART to 8,n,0,9600, default 'Read the speed from keyboard: datin: INPUT "BAUDRATE"; bdrate CALL proof IF pro = 0 THEN GOTO datin INPUT "ASCII character to be transmitted (0-255)"; asci IF asci < 0 OR asci > 255 THEN GOTO datin 'Send the control word to the TOIM3232 sig = 0PRINT "You can choose the different IrDA standards:" INPUT "1.6æs pulses (1) or 3/16 bit (0) length"; sig 'Set rts active rts\$ = "HI" pin2 = HighCALL rtsbrdline 'sets rts=br/d - switch to Vcc



```
'sets the toim to the given baudrate (3/16)
IF sig = 0 THEN CALL progtoim
IF sig = 1 THEN CALL programsh 'sets the toim to the given baudrate (1.6 \mu)
                      'some delay is necessary here
FOR n = 1 TO 100
NEXT n
rts = "LO"
                   'at PLD = GND
                     'sets rts=br/d - switch to GND
CALL rtsbrdline
                     'sets the baudrate to the right speed
CALL proguart
FOR i = 1 TO 1000
NEXT i
FOR n = 1 TO 10000
                          'PROGRAM DURATION
FOR m = 1 TO 11500
NEXT m
CALL dataout
NEXT n
CLS
END
SUB dataout
OUT &H3F8, asci
END SUB
SUB dtrreset
OUT &H3FC, (INP(&H3FC) AND &HFE)
OUT &H3FC, (INP(&H3FC) OR &H1)
OUT &H3FC, (INP(&H3FC) AND &HFE)
END SUB
SUB progtoim
OUT &H3FB, (INP(&H3FB) AND &H7F)
                                          'disable access to divisor latch bits
                      'enables data transfer to out/input register
IF bdrate = 115200 THEN OUT &H3F8, (&H0) 'LSB 0000
IF bdrate = 57600 THEN OUT &H3F8, (&H1) 'LSB 0001
IF bdrate = 38400 THEN OUT &H3F8, (&H2) 'LSB 0010
IF bdrate = 19200 THEN OUT &H3F8, (&H3) 'LSB
                                               0011
IF bdrate = 14400 THEN OUT &H3F8, (&H4) 'LSB 0100
IF bdrate = 12800 THEN OUT &H3F8, (&H5) 'LSB 0101
IF bdrate = 9600 THEN OUT &H3F8, (&H6) 'LSB
                                              0110
IF bdrate = 7200 THEN OUT &H3F8, (&H7) 'LSB
                                              0111
IF bdrate = 4800 THEN OUT &H3F8, (&H8) 'LSB
                                              1000
IF bdrate = 3600 THEN OUT &H3F8, (&H9) 'LSB
                                              1001
IF bdrate = 2400 THEN OUT &H3F8, (&HA) 'LSB
                                               1010
IF bdrate = 1800 THEN OUT &H3F8, (&HB) 'LSB
                                               1011
IF bdrate = 1200 THEN OUT &H3F8, (&HC) 'LSB
                                              1100
```



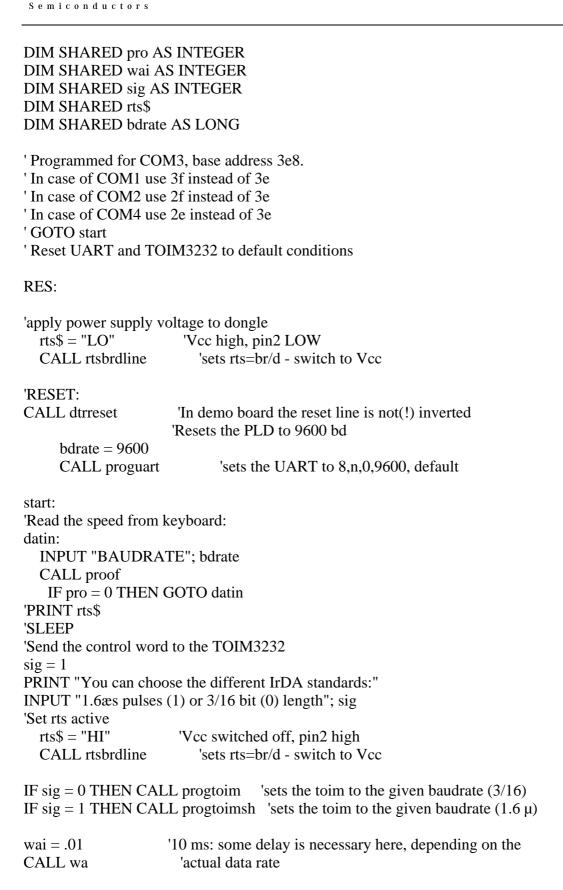
#### END SUB

SUB progtoimsh

OUT &H3FB, (INP(&H3FB) AND &H7F) 'disable access to divisor latch bits 'enables data transfer to out/input register IF bdrate = 115200 THEN OUT &H3F8, (&H10) 'LSB 0000 IF bdrate = 57600 THEN OUT &H3F8, (&H11) 'LSB 0001 IF bdrate = 38400 THEN OUT &H3F8, (&H12) 'LSB 0010 IF bdrate = 19200 THEN OUT &H3F8, (&H13) 'LSB 0011 IF bdrate = 14400 THEN OUT &H3F8, (&H14) 'LSB 0100 IF bdrate = 12800 THEN OUT &H3F8, (&H15) 'LSB 0101 IF bdrate = 9600 THEN OUT &H3F8, (&H16) 'LSB 0110 IF bdrate = 7200 THEN OUT &H3F8, (&H17) 'LSB 0111 IF bdrate = 4800 THEN OUT &H3F8, (&H18) 'LSB 1000 IF bdrate = 3600 THEN OUT &H3F8, (&H19) 'LSB 1001 IF bdrate = 2400 THEN OUT &H3F8, (&H1A) 'LSB 1010 IF bdrate = 1800 THEN OUT &H3F8, (&H1B) 'LSB 1011 IF bdrate = 1200 THEN OUT &H3F8, (&H1C) 'LSB 1100 **END SUB** SUB proguart OUT &H3FB, (&H3) '8bit, 1stop, no parity OUT &H3FB, (INP(&H3FB) OR &H80) 'Enable access to divisor latch register IF bdrate = 9600 THEN OUT &H3F8, (&HC) 'LSB send divisor: 12 for 9600 baud IF bdrate = 9600 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 19200 THEN OUT &H3F8, (&H6) 'LSB send divisor: 6 for 19.20 kbaud IF bdrate = 19200 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 38400 THEN OUT &H3F8, (&H3) 'LSB send divisor: 3 for 38.4 kbaud IF bdrate = 38400 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 57600 THEN OUT &H3F8, (&H2) 'LSB send divisor: 2 for 57.6 kbaud IF bdrate = 57600 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 115200 THEN OUT &H3F8, (&H1) 'LSB send divisor: 1 for 115.2 kbaud IF bdrate = 115200 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 7200 THEN OUT &H3F8, (&H10) 'LSB send divisor: 16 for 7.20 kbaud IF bdrate = 7200 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 4800 THEN OUT &H3F8, (&H18) 'LSB send divisor: 24 for 4800 baud IF bdrate = 4800 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 3600 THEN OUT &H3F8, (&H20) 'LSB send divisor: 32 for 3.6 kbaud IF bdrate = 3600 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 2400 THEN OUT &H3F8, (&H30) 'LSB send divisor: 48 for 2.4 kbaud IF bdrate = 2400 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 2000 THEN OUT &H3F8, (&H3A) 'LSB send divisor: 58 for 2 kbaud

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IF bdrate = 2000 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 1800 THEN OUT &H3F8, (&H40) 'LSB send divisor: 64 for 1.8 kbaud IF bdrate = 1800 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 1200 THEN OUT &H3F8, (&H60) 'LSB send divisor: 96 for 1.2 kbaud IF bdrate = 1200 THEN OUT &H3F9, (&H0) 'MSB = 0'PRINT INP(&H3f8), INP(&H3f9) 'PRINT INP(&H3fB) OUT &H3FB, (INP(&H3FB) AND &H7F) 'disable access to divisor latch bits 'PRINT INP(&H3fB) **END SUB** SUB proof pro = 0IF bdrate = 115200 THEN pro = 1IF bdrate = 57600 THEN pro = 1IF bdrate = 38400 THEN pro = 1IF bdrate = 19200 THEN pro = 1IF bdrate = 9600 THEN pro = 1IF bdrate = 7200 THEN pro = 1IF bdrate = 4800 THEN pro = 1IF bdrate = 3600 THEN pro = 1IF bdrate = 2400 THEN pro = 1IF bdrate = 1800 THEN pro = 1IF bdrate = 1200 THEN pro = 1IF bdrate = 14400 THEN pro = 1IF bdrate = 12800 THEN pro = 1**END SUB** SUB rtsbrdline 'Be aware: the signal is inverted by the MAX 232 IF rts\$ = "LO" THEN OUT &H3FC, (INP(&H3FC) OR &H2) 'IF rts\$ = "HI" then PRINT rts\$ IF rts\$ = "HI" THEN OUT &H3FC, (INP(&H3FC) AND &HFD) 'IF rts\$ = "LO" then PRINT rts\$ **END SUB** 'Demo program for receiving ASCII characters DECLARE SUB dtrreset () DECLARE SUB rtsbrdline () DECLARE SUB progtoim () **DECLARE SUB** proguart () DECLARE SUB progtoimsh () DECLARE SUB dataout () DECLARE SUB datain () DECLARE SUB proof () DECLARE SUB wa () CLS



# TOIMxxx

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rts\$ = "LO" 'at PLD = GNDCALL rtsbrdline 'sets rts=br/d - switch to GND 'PRINT rts\$ 'SLEEP CALL proguart 'sets the baudrate to the right speed wai = .01 CALL wa CALL datain **END** SUB datain beg: a = (INP(&H3FD) AND (&H1))IF a = 1 THEN b = INP(&H3F8)IF a = 1 THEN PRINT b; " "; GOTO beg **END SUB** SUB dataout OUT &H3F8, (&H0) **END SUB** SUB dtrreset 'OUT &H3fC, (INP(&H3fC) AND &HFE) FOR n = 1 TO 10 OUT &H3FC, (INP(&H3FC) OR &H1) OUT &H3FC, (INP(&H3FC) AND &HFE) NEXT n OUT &H3FC, (INP(&H3FC) AND &HFE) **END SUB** SUB progtoim OUT &H3FB, (INP(&H3FB) AND &H7F) 'disable access to divisor latch bits 'enables data transfer to out/input register IF bdrate = 115200 THEN OUT &H3F8, (&H0) 'LSB 0000 IF bdrate = 57600 THEN OUT &H3F8, (&H1) 'LSB 0001 IF bdrate = 38400 THEN OUT &H3F8, (&H2) 'LSB 0010 IF bdrate = 19200 THEN OUT &H3F8, (&H3) 'LSB 0011 IF bdrate = 14400 THEN OUT &H3F8, (&H4) 'LSB 0100 IF bdrate = 12800 THEN OUT &H3F8, (&H5) 'LSB 0101 IF bdrate = 9600 THEN OUT &H3F8, (&H6) 'LSB 0110 IF bdrate = 7200 THEN OUT &H3F8, (&H7) 'LSB 0111 IF bdrate = 4800 THEN OUT & H3F8, (&H8) 'LSB 1000 IF bdrate = 3600 THEN OUT &H3F8, (&H9) 'LSB 1001 IF bdrate = 2400 THEN OUT &H3F8, (&HA) 'LSB 1010

IF bdrate = 1800 THEN OUT &H3F8, (&HB) 'LSB 1011 IF bdrate = 1200 THEN OUT &H3F8, (&HC) 'LSB 1100 **END SUB** SUB progtoimsh OUT &H3FB, (INP(&H3FB) AND &H7F) 'disable access to divisor latch bits 'enables data transfer to out/input 'register IF bdrate = 115200 THEN OUT &H3F8, (&H10) 'LSB 0000 IF bdrate = 57600 THEN OUT &H3F8, (&H11) 'LSB 0001 IF bdrate = 38400 THEN OUT &H3F8, (&H12) 'LSB 0010 IF bdrate = 19200 THEN OUT &H3F8, (&H13) 'LSB 0011 IF bdrate = 14400 THEN OUT &H3F8, (&H14) 'LSB 0100 IF bdrate = 12800 THEN OUT &H3F8, (&H15) 'LSB 0101 IF bdrate = 9600 THEN OUT &H3F8, (&H16) 'LSB 0110 IF bdrate = 7200 THEN OUT &H3F8, (&H17) 'LSB 0111 IF bdrate = 4800 THEN OUT & H3F8, (& H18) 'LSB 1000 IF bdrate = 3600 THEN OUT &H3F8, (&H19) 'LSB 1001 IF bdrate = 2400 THEN OUT &H3F8, (&H1A) 'LSB 1010 IF bdrate = 1800 THEN OUT &H3F8, (&H1B) 'LSB 1011 IF bdrate = 1200 THEN OUT &H3F8, (&H1C) 'LSB 1100 **END SUB** SUB proguart OUT &H3FB. (&H3) '8bit, 1stop, no parity OUT &H3FB, (INP(&H3FB) OR &H80) 'Enable access to divisor latch register IF bdrate = 9600 THEN OUT &H3F8, (&HC) 'LSB send divisor: 12 for 9600 baud IF bdrate = 9600 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 14400 THEN OUT &H3F8, (&H8) 'LSB send divisor: 8 for 14400 baud IF bdrate = 14400 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 12800 THEN OUT &H3F8, (&H9) 'LSB send divisor: 9 for 12800 baud IF bdrate = 12800 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 19200 THEN OUT &H3F8, (&H6) 'LSB send divisor: 6 for 19.20 kbaud IF bdrate = 19200 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 38400 THEN OUT &H3F8, (&H3) 'LSB send divisor: 3 for 38.4 kbaud IF bdrate = 38400 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 57600 THEN OUT &H3F8, (&H2) 'LSB send divisor: 2 for 57.6 kbaud IF bdrate = 57600 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 115200 THEN OUT &H3F8, (&H1) 'LSB send divisor: 1 for 115.2 kbaud IF bdrate = 115200 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 7200 THEN OUT &H3F8, (&H10) 'LSB send divisor: 16 for 7.20 kbaud IF bdrate = 7200 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 4800 THEN OUT &H3F8, (&H18) 'LSB send divisor: 24 for 4800 baud IF bdrate = 4800 THEN OUT & H3F9, (&H0) 'MSB = 0

IF bdrate = 3600 THEN OUT &H3F8, (&H20) 'LSB send divisor: 32 for 3.6 kbaud IF bdrate = 3600 THEN OUT &H3F9, (&H0) 'MSB = 0 IF bdrate = 2400 THEN OUT &H3F8, (&H30) 'LSB send divisor: 48 for 2.4 kbaud IF bdrate = 2400 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 2000 THEN OUT &H3F8, (&H3A) 'LSB send divisor: 58 for 2 kbaud IF bdrate = 2000 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 1800 THEN OUT &H3F8, (&H40) 'LSB send divisor: 64 for 1.8 kbaud IF bdrate = 1800 THEN OUT &H3F9, (&H0) 'MSB = 0IF bdrate = 1200 THEN OUT &H3F8, (&H60) 'LSB send divisor: 96 for 1.2 kbaud IF bdrate = 1200 THEN OUT &H3F9, (&H0) 'MSB = 0 'PRINT INP(&H3f8), INP(&H3f9) 'PRINT INP(&H3fB) OUT &H3FB, (INP(&H3FB) AND &H7F) 'disable access to divisor latch bits 'PRINT INP(&H3fB) **END SUB** SUB proof pro = 0IF bdrate = 115200 THEN pro = 1IF bdrate = 57600 THEN pro = 1IF bdrate = 38400 THEN pro = 1IF bdrate = 19200 THEN pro = 1IF bdrate = 14400 THEN pro = 1IF bdrate = 12800 THEN pro = 1IF bdrate = 9600 THEN pro = 1IF bdrate = 7200 THEN pro = 1IF bdrate = 4800 THEN pro = 1IF bdrate = 3600 THEN pro = 1IF bdrate = 2400 THEN pro = 1IF bdrate = 1800 THEN pro = 1IF bdrate = 1200 THEN pro = 1**END SUB** SUB rtsbrdline 'Be aware: the signal is inverted by the MAX 232 IF rts\$ = "LO" THEN OUT &H3FC, (INP(&H3FC) OR &H2) 'IF rts\$ = "HI" then PRINT rts\$ IF rts\$ = "HI" THEN OUT &H3FC, (INP(&H3FC) AND &HFD) 'IF rts\$ = "LO" then PRINT rts\$ **END SUB** SUB wa t1 = TIMERDO UNTIL (t2 - t1) > wait2 = TIMERLOOP **END SUB**