Single Event Testing of the IS-705RH Microprocessor Supervisory Circuit

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Introduction

The intense heavy ion environment encountered in space applications can cause a variety of transient and destructive effects in analog circuits, including single-event latchup (SEL), single-event transient (SET) and single-event breakdown (SEB). These effects can lead to system-level failures including disruption and permanent damage. For predictable, reliable space system operation these components have to be formally designed and fabricated for SEE hardness, followed by detailed SEE testing to validate the design. This report discusses the results of SEE testing of the Intersil IS705RH microprocessor supervisory circuit.

Product Description

The Intersil IS705RH is a microprocessor supervisory circuit that monitors power supply voltage and battery functions in microprocessor systems. It provides the following functions:

- A reset output during power-up and power-down conditions.
- A precision 4.65V power supply voltage monitor
- A watchdog timer that switches to the LOW state if the timer input has not been toggled within 1.6 seconds.
- A 1.25V threshold detector to monitor power supply voltage.
- A manual reset input.

The IS705RH is fabricated using the CMOS option of the Intersil Corporation UHF-2 process. This is a sub-micron CMOS flow optimized for high-density logic applications. The IS705RH is total dose and SEE hardened by design, which enables the use of a dense non-hardened process to implement the part. This methodology uses special edgeless N-channel devices and guard rings to control N-channel leakage after total dose irradiation, and specific device sizing rules and logic redundancy to harden the part to SEE.

SEE Test Objectives

The objectives of SEE testing of the IS705RH were to evaluate the single-event latchup performance of the part and to determining its single-event upset cross section.

SEE Test Procedure

The part was tested for single event effects at the Cyclotron Institute at Texas A&M University using Au ions (LET=83.9) and Kr ions (LET=38.0)

The device under test was mounted in the beam line and irradiated with heavy ions of the appropriate species. The parts were assembled in dual in-line packages with the metal lid removed for beam exposure. The beam was directed on to the exposed die and the beam flux, beam fluence and errors in the device outputs were measured.

The tests were controlled remotely from the control room. All input power was supplied from portable power supplies connected via cable to the device under test (DUT). The supply currents were monitored along with the device outputs. All currents were measured with digital ammeters while all the output waveforms were monitored on a digital oscilloscope for ease of identifying the different types of SEE which the part displayed. Events were captured by triggering on changes in the output pulses in time such as changes in duty cycle or phase shifts.

Single Event Latchup and Burnout results

Unlike the other Star*Power components, the IS705RH is built in a junction-isolated process in which latchup is at least a theoretical possibility; other Intersil Star*Power parts use various dielectrically isolated (DI) processes in which latchup is not possible.

Accordingly, the first testing sequence looked at destructive effects. No burnout or latchup was observed using Au ions (LET = 83.9 MeV/mg/cm^2) at 60 degree incidence from perpendicular (representing an effective LET of 181.8 MeV/mg/cm^2 as compared to testing at normal incidence). Testing was performed on three parts at 25C and 125C at maximum voltage (Vcc=5.5V). All test runs were run to fluence of 1x10^7/ cm^2. The WDI and PFI inputs were toggled from 0.5V to 5V (with cable ringing, the device under test saw 0-5.5V) at 1Khz. The MR input was manually toggled using a pulse generator's single pulse capability. Functionality of all outputs was verified after exposure. Icc was recorded pre and post exposure, under continuous power; results are shown in Table 1. No destructive effects of any kind were encountered in these tests.

		Pre-Exposure	Post-Exposure
Serial number	Temperature	Icc, ua	Icc, ua
4	25C	433	432
5		443	442
6		420	419
4	125C	429	427
5		438	437
6		414	415

Table 1: IS705RH Icc Pre and Post SEB/SEL Testing

Single Event Upset Testing

Upsets of the Reset output were counted for various temperatures and ion angles (from the perpendicular) and the resultant error cross sections were calculated using the same test configuration as described above for SEB/Latchup testing, except the MR input was tied to Vcc. Reset should then be in the high state. This testing was performed to determine the sensitivity to temperature and ion angle. The upset goal was an LET of 40 MeV/mg/cm^2, hence upsets were expected when testing with Au at the higher LET of 83.9 MeV/mg/cm^2. Upsets were indeed measured and could be the result of either the Vcc Reset circuitry upsetting or the MR input logic upsetting. Table 2 gives the number of upsets vs fluence. From this table we see that the error cross section is about 25% higher at 125C (using "total" rows in table 2) and 9% higher for 0^o vs 60^o (based on one part, SN 6 results). All subsequent testing was then performed at 25C and with the ions normal to the chip surface. The next ion used was Kr at an LET of 38 MeV/mg/cm^2, with a predicted range in Si of 44 microns.

Reset Results:

The first test set Vcc at 4.5V and MR at Vcc; under these conditions, Reset should be low (as Vcc is below the nominal Vcc reset threshold of 4.65V). Using a fluence of 1x10^6/cm^2 , no upsets or transients were observed during this test. This was an encouraging result, as it means that during a low Vcc condition there would be no false signals sent from Reset indicating that Vcc is within tolerances.

The second test set Vcc at 4.75V and MR at Vcc, hence Reset should be high (as Vcc is above the nominal Vcc reset threshold of 4.65V). Two runs of fluence 1x10^6/cm^2 each were run and a total of 24 (10 + 14) HLH transients were observed for a transient cross section of 1.2x10^{-5} cm^2. Vcc was then raised to 5V, a more typical application, and the upsets were reduced to 4 (cross section 4x10^{6}cm^2). Vcc was then raised to 5.5V and no upsets were observed. Recall that the SEB/SEL testing with gold (LET= 84 MeV/mg/cm^2) was done at the maximum Vcc of 5.5V where an error cross section of 1.2x10^{5}cm^2 was found, hence 1.2x10^{5}cm^2 may be near the saturated cross section. If additional test time becomes available, testing with Au at Vcc=4.75 would verify this. Figure 1 shows scope traces for WDI (being clocked at 1Khz), WDO and Reset. Since we're triggering on WDON and the scope's persistence is set at infinity, the input clock looks like a blur as it is asynchronous with the upset events. Significantly, there are Reset upsets simultaneously with WDO. This implies upsets in the voltage reference or VccComp subcircuit which would affect both outputs. This upset lasts about 7us, as evidenced by the WDO output returning to the correct state in that time. This is long enough to reset the Reset Counter subcircuit, hence the Reset output width is expected to be the designed 200ms; it was only verified to be greater than 8ms as the trace ran off the screen at that point (see Fig 2).

Testing was next performed with different LET values to characterize cross section vs. LET. Kr ions were again used with their energy increased to obtain an LET of 26.8 MeV/mg/cm^2. The Reset cross section appeared to increase to 2.4x10^5 (71 upsets at a fluence of 3x10^6/cm^2 with Vcc=4.75V). Again, there were no LHL transients when

Vcc=4.5V. Testing with Ar at LET=17.5 MeV/mg/cm^2 yielded a cross section of 6x10^{-6} (30 upsets at a fluence of 5x10^6/cm^2) for the HLH upsets. No sure explanation exists why the error cross-section appears to have increased going from Kr at LET=38 to LET=27. Possibly the lower range in Si (44u vs 149u) for the lower energy/LET Kr ion has a contribution here. This was not expected, as both N-channel and P-channel MOS devices are shielded from the substrate by underlying N+ buried layers tied off to ground under the NMOS device and to Vcc under the PMOS one. If additional testing is done in the future, selecting 3200MeV Xe would provide an LET of 38 MeV/mg/cm^2 and a range of 285u and would possibly produce more upsets than the LET =38 Kr ion. If so, particle ranges should be kept above 100u for this technology to evaluate worst case effects. While no upsets would have been the preferred result for these tests, the Reset HLH transient cross section is so low that unnecessary resets of the uP would be extremely rare. With these LET and cross-section values, unnecessary resets would be hundreds to thousands of years apart.

When Reset was driven low by setting MR = 0V (Vcc was returned to 5V) there were no upsets with Kr or Ar with LET values ranging from 27 to 38 MeV/mg/cm^2. This test was not run with Au ions, as the IS705RH design goal was no upsets at LET<40 MeV/mg/cm^2. Observing no upsets was not a surprising result, as the SET would have to last longer than the 200ms Reset timer period to get a false transition to a "1" level. So, the manual reset function is SEU "immune".

Reset summary: The part has no Reset LHL transients when Vcc is less than 4.75V or is held low by MR input being held low. This means the system will not have any false Reset signal telling it that Vcc is within tolerance when it isn't, or that it can operate while the MR (manual reset) is being applied. When Vcc>4.75V and MR = "1" there are HLH upsets that would cause the system to go through an unnecessary reset cycle. However, the error crossection again is so small that this occurrence will be hundreds to thousands of years apart.

WDO SET/SEU Results: WDO has many modes of operation, depending on whether Vcc is below 4.5V or above 4.75V, on the state of MR and on whether WDI is toggling, DC low, DC high or floating. Table 3 shows these results. Again, we saw larger upset cross-sections with Kr ions at LET=27 MeV/mg/cm^2 than with Kr at LET=38 MeV/mg/cm^2. With Ar ions at LET=17.5 MeV/mg/cm^2 we saw much smaller cross sections, as expected. With the largest cross section observed in any WDO test being 2.2x10^{-5} cm^2, natural space upsets will be hundreds to thousands of years apart.

PFO SET/SEU Results: The PFI/PFO function is that of a comparator with the negative input tied to an on-chip 1.25V voltage reference. The PFI input is tied to the positive comparator input and PFO is the comparator output. The specifications allow a +/- 50mV offset over temperature and radiation. Hence input voltages below 1.2V set PFO low and voltages above 1.3V set PFO high. Table 4 lists PFO transients as a function of input voltage for several LET values. Again, results of Kr at LET=27 MeV/mg/cm^2 show higher upsets than Kr at LET=38. Upsets were seen with all ions when driving PFI to the minimum specs (1.2V or 1.3V). By increasing the comparator

overdrive, the upset cross section can be reduced or eliminated. For example, with Ar at LET=17.5 MeV/mg/cm^2, a reduction of PFI from 1.2Vto 1.15V will eliminate the LHL transients. Similarly, increasing the PFI input voltage from 1.3V to 1.5V will eliminate the HLH transients. Again, even at minimum overdrive conditions (input 1.2 or 1.3V), the upset cross-section is so small that the occurrence will be hundreds to thousands of years apart. For further reductions, an off-chip low pass filter could be used provided the load input impedance is high. Figures 3 and 4 show scope traces for PFO with PFI at 1.2 and 1.3V respectively. Note the LHL transient is 1.5-2.1us long and the HLH transient is 0.2-2.5us long. An external low-pass filter with a time constant of 20us would reduce the glitch to less that 10% of the rail to rail voltage. This would add delay in the system that the designer would need to evaluate.

Summary

The key objectives of burnout or latchup hardness to an LET in excess of 83 MeV/mg/cm^2 and no Reset LHL SEE transients to an LET of 38 MeV/mg/cm^2 have been demonstrated. Other functions have demonstrated cross sections so small as to not occur for hundreds to thousands of years. These characteristics must be evaluated by the system designer for the particular environment of interest and the usage of the available features of the IS-705RH. Feedback from potential customers will determine whether additional design enhancements are required.

Ion Angle, from normal	Temperature, ^{o}C	Serial number	Fluence, /cm^2	Reset HLH upsets	Error cross section, cm^2
60 ^{o}	25	5	1x10^7	125	1.25x10^{-5}
		6	1.07x10^7	116	1.08x10^{-5}
		total	2.07x10^7	241	1.16x10^{-5}
	125	4	1.01x10^7	131	1.30x10^{-5}
		5	1x10^7	150	1.5x10^{-5}
		6	1.04x10^7	161	1.55x10^{-5}
		total	3.05x10^7	442	1.45x10^{-5}
0 ^{o}	125	6	1.4x10^7	236	1.69x10^{-5}

Table 2: Reset HLH transients using Au ions at various angles and temperatures.

Ion/LET, MeV/mg/ cm^2	WDI	Vcc	Expected WDO State	LHL Transitions	HLH Transitions	Fluence, $/cm^2$	Cross section, cm^2
Kr, LET=38	toggle	4.5V	0	0	N.A.	$1x10^6$	0
	toggle MR=0	5V	1	N.A.	10	$2x10^6$	$5x10^{-6}$
	float	4.75V	1	N.A.	19	$2x10^6$	$9.5x10^{-6}$
	5V	5V	0	9	N.A.	$2x10^6$	$4.5x10^{-6}$
	0V	5V	0	10	N.A.	$2x10^6$	$5x10^{-6}$
Kr, LET=27	toggle	4.5V	0	6	N.A.	$1x10^6$	$6x10^{-6}$
	toggle MR=0	5V	1	N.A.	12	$1x10^6$	$1.2x10^{-5}$
	float	4.75V	1	N.A.	22	$1x10^6$	$2.2x10^{-5}$
	5V	5V	0	9	N.A.	$1x10^6$	$9x10^{-6}$
	0V	5V	0	11	N.A.	$1x10^6$	$1.1x10^{-5}$
Ar, LET=17.5	toggle	4.5V	0	0	N.A.	$5x10^6$	0
	toggle MR=0	5V	1	N.A.	11	$5x10^6$	$2.2x10^{-6}$
	float	4.75V	1	N.A.	32[1]	$5x10^6$	$6x10^{-6}$
	5V	5V	0	25	N.A.	$1x10^7$	$2.5x10^{-6}$
	0V	5V	0	66	N.A.	$2x10^7$	$3.3x10^{-6}$

Table 3: WDO Transients vs Ion species and mode of operation, MR = Vcc unless noted otherwise.

Note 1: Reduced to 12, if Vcc raised to 5V (fewer "VccLow" upsets driving WDO to 0).

Ion/LET, MeV/mg/ cm2	PFI Vin	Vcc	Expected PFO State	LHL Transitions	HLH Transitions	Fluence, /cm^2	Cross section, cm^2
Kr/38	1.2V	5V	0	3	N.A.	1x10^6	3x10^{-6}
	1.15V	5V	0	2	N.A.	1x10^6	2x10^{-6}
	1.1V	5V	0	0	N.A.	1x10^6	0
	1.3V	5V	1	N.A.	11	1x10^6	1.1x10^{-5}
	1.35V	5V	1	N.A.	8	1x10^6	8x10^{-6}
	1.4V	5V	1		2	1x10^6	2x10^{-6}
Kr/27	1.2V	5V	0	32	N.A.	4x10^6	8x10^{-6}
	1.3V	5V	1	N.A.	57	2x10^6	2.9x10^{-5}
	3.0V	5V	1	N.A.	0	1x10^6	0
Ar/17.5	1.2V	5V	0	9	N.A.	5x10^6	1.8x10^{-6}
	1.15V	5V	0	0	N.A.	5x10^6	0
	1.3V	5V	1	N.A.	27	5x10^6	5.4x10^{-6}
	1.35V	5V	1	N.A.	26	5x10^6	5.2x10^{-6}
	1.4V	5V	1	N.A.	11	5x10^6	2.2x10^{-6}
	1.5V	5V	1	N.A.	0	5x10^6	0

Table 4: PFO Transients vs Ion and PFI input voltage.

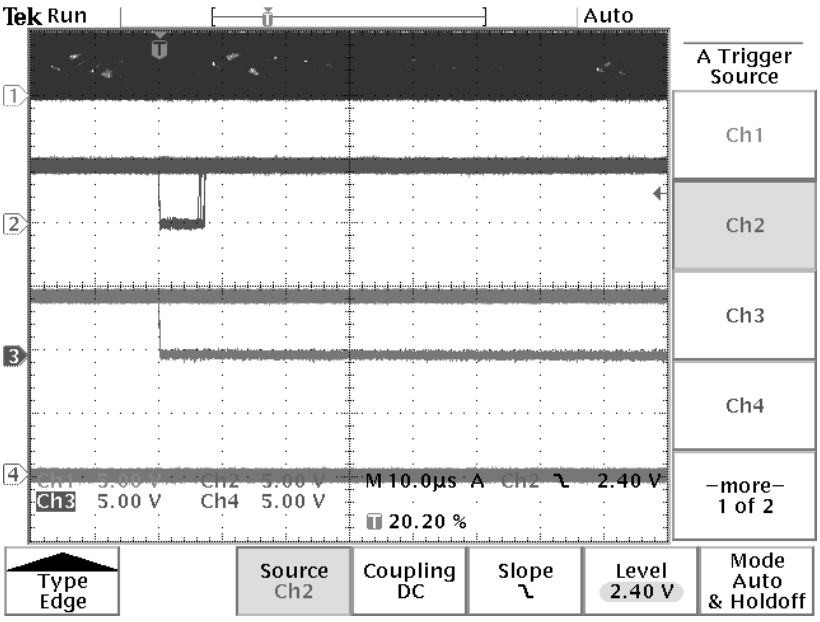

Figure 1. WDO and Reset single-event transients, Kr ions at LET=38 MeV/mg/cm^2.

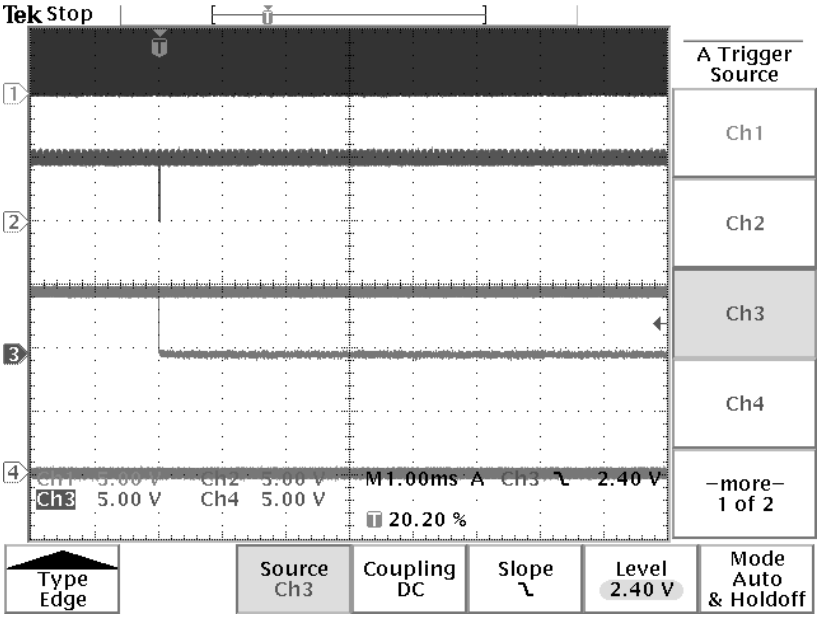

Figure 2. Same as Figure 1 except at 1ms/division.

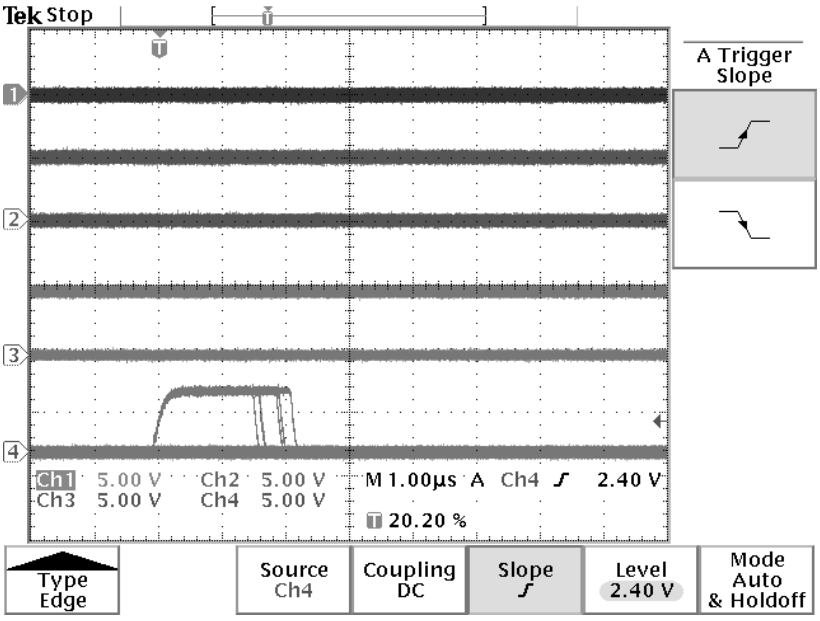

Figure 3. PFO LHL transients with PFI = 1.2V, Kr ions at LET=27 MeV/mg/cm^2.

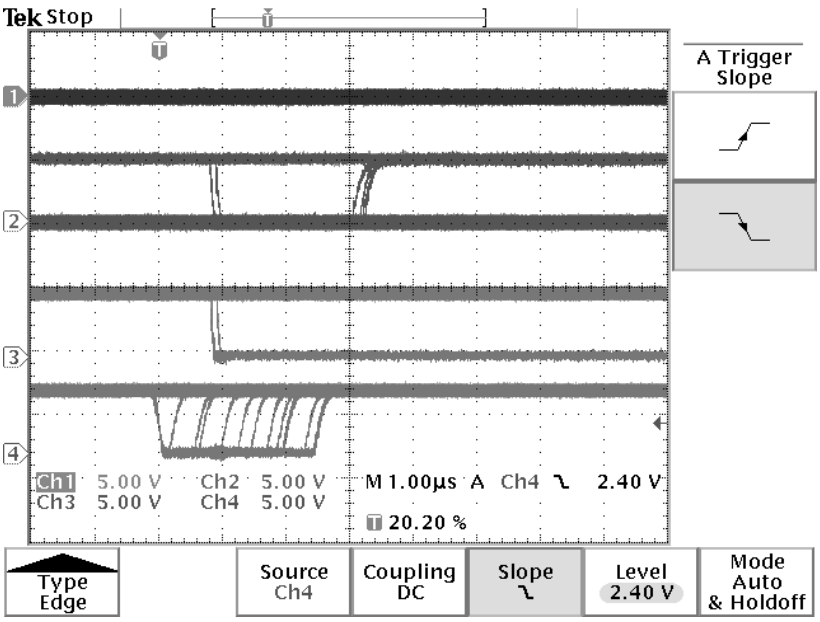

Figure 4. PFO HLH transients with PFI = 1.3V, Kr ions at LET=27 MeV/mg/cm^2.