SINGLE EVENT LATCHUP PROTECTION OF INTEGRATED CIRCUITS

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Abstract

Many commercially available advanced technology CMOS and bipolar integrated circuits are latchup susceptible to single event effects caused by heavy ions or protons from cosmic rays or solar flares making them unsuitable for satellite applications. Remanufacturing the integrated circuits on an inherently SEL immune process has been an expensive and technically difficult option as is the alternate option of incorporating latchup protection and recovery circuitry in the spacecraft system electronics. Space Electronics Inc. has developed several different circuits which provide protection and recovery of integrated circuits known to exhibit single event induced latchup. These circuits are integrated within the same package as the susceptible integrated circuit using MCM and modern packaging technology resulting in a device level solution providing minimum cost and minimum impact on the system. This paper will focus on test results from the development of single event latchup protection circuitry (referred to as Space Electronics Inc.'s (SEI's) LPT™ technology) for the ADS7805 16 bit analog to digital converter integrated circuit which is known to latchup at unacceptably low LET energies for space applications.

The LPT™ circuit was designed to provide the following features to protect and recover the susceptible integrated circuit device:

a. Provide current limiting to the device.
b. Detect the increase in current during the SEL event above a preset threshold.
c. Force a shutdown of the protected device when the threshold is exceeded.
d. Hold the device in the shut down mode for a preset time interval.
e. Return the device supply voltage to its original operating level.

Heavy ion characterization and validation of the ADS7805 with the LPT™ circuitry was performed using the Jet Propulsion Laboratories (JPL) Californium -252 source at Pasadena CA and also using the Texas A&M University Cyclotron facility. Latchup protection and recovery of the ADS7805 was demonstrated at both of these facilities.

The LPT™ circuitry (patent pending) has the potential to be applied to a wide variety of susceptible devices. The specific implementation details such as current latchup protection threshold and supply off time are determined by characterization of the susceptible devices at a heavy ion facility. The impact on a system using an LPT™ device is that an SEL is converted into a recoverable event. Using mission specific or orbit radiation data, recoverable event rates can be calculated. The rate and number of these recoverable events is dependent on the fluence, energy, and species of radiation encountered by the device during the mission.

ADS7805 Testing

Test results, as reported in JPL's radiation effects database[2] from a Brookhaven National Laboratory (BNL) heavy ion test conducted on 12/6/94, bounded SEL threshold for the ADS7805 below 38 MeV-cm^2/mg. This threshold level created a high probability of latchup in a space environment, making this device unsuitable for space applications. The latchup current level from the BNL test was not reported. Typical operating current of the ADS7805 is specified as 16.3 mA for both the analog and digital 5V supply. The maximum specified operating current[3] for the device is 20 mA.

An interesting characteristic of the ADS7805 die was that latchup could be induced with a high intensity light source. We were able to trigger latchup by exposing de-lidded devices to the flash from a 35mm camera flash bulb. Typical peak photoelectric currents were measured on the supply inputs at ~650 mA with a duration of 2 ms. After the flash induced current dissipated, the device latchup current was measured to be 110 mA. This latchup characteristic of the ADS7805 was used to electrically test and debug the LPT™ circuits during development and prior to radiation exposure.

LPT™ Circuit

The ADS7805 integrated circuit draws current from an analog and digital supply pin. The LPT™ circuit must sense the current into the supply pins and when the latchup current threshold is exceeded, remove the supply voltage from the latched device. During the time that the supply voltage is removed from the device, the supply current draw

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will come exclusively from the LPT™ circuit. After a set time interval required for the latchup to clear, the LPT™ circuit reapplies the supply voltage to the device and normal operation is restored. The LPT™ circuit will have a latchup current threshold, $I_{Threshold}$, an activation delay time, t_D, and recovery time, t_{REC}, as shown in figure 2 (b). This can be compared with the unprotected latchup supply current response shown in figure 2(a) where the normal operating current rises to the latchup current in response to a single event latchup.

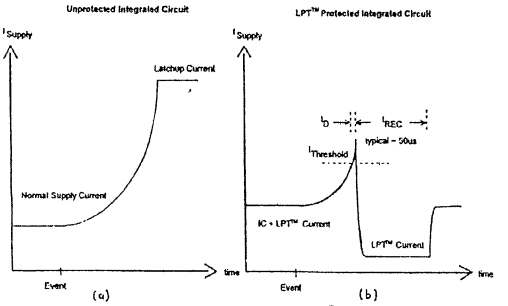

Figure 2. Supply Current Waveforms Showing LPT™ Latchup Protected Device

Two types of circuits were designed to protect and recover the ADS7805 from SEL. The primary components of the first circuit were a dual comparator and a logic level P channel MOSFET. One comparator was used to detect when the latchup current threshold was exceeded and provide a limited duration control pulse when this occurred. The second comparator provided a status output to indicate to the system that latchup had been detected and power was removed from the ADS7805. The logic level P channel MOSFET was used as a high side power switch to the ADS7805.

The second circuit used a specialized integrated circuit, the LTC1153 Auto Reset Electronic Circuit Breaker, available from Linear Technologies, Inc.[4] along with an N channel MOSFET. The LTC1153 provided latchup threshold detection, gate drive to the MOSFET including timed shutoff and status output to the system. The N-Channel MOSFET was operated as a high side power switch to the ADS7805.

In both LPT™ circuits, the analog and digital supply inputs to the device were tied together through a low value current sense resistor and powered by a single supply input.

Validation Test Results

Both LPT™ circuit types were tested at the JPL Californium-252 source. Additionally, two different comparators devices were tested in the comparator circuit. One comparator exhibited higher speed with higher power, while the second comparator exhibited lower speed and significantly lower power.

The test circuit consisted of a breadboard of each LPT™ circuit type, a de-lidded ADS7805 (the target of the radiation), and a 16 bit digital to analog converter which provided a composite monitor of the ADS7805 parallel data output. The status signal was used to trigger a digital storage scope set to capture the supply current response and the composite monitor response. A full scale sinusoidal input signal was provided to the ADS7805 during all testing, and the composite output was continuously monitored by a DMM for loss of functional operation.

The test results from the JPL Californium-252 test are shown in table 1. The fragments from the Californium source exhibit an LET of ~42 MeV-cm^2/mg. Latchup protection and recovery was demonstrated for both circuit types over a range of input conditions, LPT™ delay and recovery times.

Note that under one test condition latchup recovery did not occur. This was due to the applied voltages and related current limiting on the digital input pins to the ADS7805. The first condition occurred with the CS, R/C, and BYTE signals tied to +5V (chip not selected) each through a 91 Ohm series resistor. When the resistors were increased to 511 Ohms, latchup recovery occurred. Values between 91 and 511 Ohms were not tested. This result showed that not only does the supply voltage have to be removed, but the inputs must be carefully considered to assure that backdriving the supply through input pins does not sustain the latchup.

Subsequent testing of the LPT™ circuitry was performed at Texas A&M University cyclotron. The primary concern of this testing was to determine if there were any latchup modes that were not exhibited with the limited LET characterization available from the Californium-252 source. Since the main concern of this test was the SEL response of the ADS7805, only the LTC1153 based circuit was tested. The results of this testing are summarized in table 2. The LPT circuit successfully recovered the ADS7805 from all SELs over an LET range of 14 - 80 MeV-cm^2/mg. Additionally, this testing bounded the SEL threshold of the ADS7805 between 9.9 and 14 MeV-cm^2/mg.

Figure 3a shows the LPT™ operation in response to a single event latchup. The latchup

current occurs and the supply is cycled off then on. The current spike at turn-on is due to the high dV/dt driving the decoupling capacitance on the ADS7805 supply pins. Figure 3b shows the effect of the LPT protection and recovery on the ADS7805 output.

Figure 3
7805LP response to to Single Event Latchup
50 µs LPT recovery time

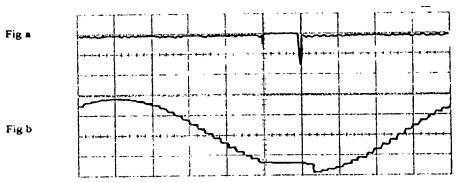

Figure a (channel 1), is I_{MON}, 500mV/Div

Figure b (channel 2) ,is V_{OUT}, 5 V/Div

all channels are 50 µs/Div

No destructive functional failures of any of the ADS7805 devices tested occurred during all radiation and flash testing.

Table 1: LPT™ Test Results at JPL Californium-252 Source

LPT Chk	Operation	Series Rs (Ohm)	tD (µs)	Latchup Current (mA)	Recovery ?	TREC	LET (Mev-cm²/mg)
LTC1153	Normal	132	19	159-133	Yes	2.5 ms	42
Slow Comparator	Normal	113	15	159-133	Yes	2.5 ms	42
Slow Comparator	All Inputs High	91	15	159-133	No		42
Slow Comparator	All Inputs High	1000	15	159-133	Yes	2.5 ms	42
Fast Comparator	All Inputs High	511	1.5	159-133	Yes	2.5 ms	42
Fast Comparator	Normal	511	1.5	159-133	Yes	2.5 ms	42
Fast Comparator	Normal	511	1.5	159-133	Yes	45 µs	42

Table 2: LPT™ Test Results at Texas A&M University Cyclotron

LPT Ckt	Operation	Series Rs (Ohm)	tD (µs)	Latchup Current (mA)	Recovery	tREC (ms)	LET Mev-cm²/mg
LTC1153	Normal	1k	19	None	n/a	2.5	7
LTC1153	Normal	1k	19	None	n/a	2.5	9.9
LTC1153	Normal	1k	19	267	Yes	2.5	14
LTC1153	Normal	1k	19	146 - 267	Yes	2.5	40
LTC1153	Normal	1k	19	146 - 267	Yes	2.5	56.6
LTC1153	Normal	1k	19	146 - 267	Yes	2.5	80

7805RPLP Design and Packaging

The ADS7805 LPT™ circuit has been developed into a multi-chip module referred to as the 7805RPLP. A pin diagram of the device is shown in figure 4. This device has the same footprint as the ADS7805 with some modification of the pin functions. The separate supplies are replaced by a single VS input. The ADS7805 common supply pin is made available for adding board level decoupling capacitance. The status output replaces the byte input which is internally grounded in the MCM. Care must be taken in the application not to backdrive the device when the status output is active. The latchup current threshold has been set typically at 80 mA with a recovery time of 50 microseconds.

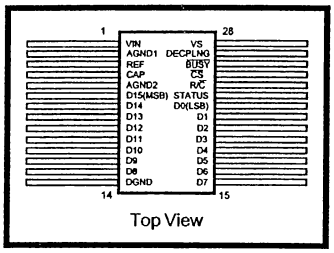

Figure 4. Pin Configuration for 7805LPRP

The 7805RPLP is packaged using SEI's RAD-PAK® packaging technology. This packaging provides shielding of the internal devices from total dose radiation thereby enhancing their total dose hardness. Total dose enhancement is required for both the ADS7805 and the LPT™ components. In particular, the power MOSFET's inherent total dose tolerance is well below most space application requirements.

Conclusions

The lessons learned for future Latchup protected devices are:

1) cycling power alone is not sufficient to return the device from a latched state,
2) the inputs need to be protected for the latchup protection circuit to work properly
3) each device needs to be validated at a heavy ion source to properly characterize the circuit, early latchup protection circuits developed at SEI had to be modified based on subsequent heavy ion data.

With proper characterization and design, devices without susceptibilities to microlatch can be protected at the package level from single event latchups.

SEI has developed and demonstrated a package level solution to allow single event latchup susceptible devices to be operated in space environments. This latchup protection technology has been demonstrated for the ADS7805 16 bit analog to digital converter device. The ADS7805 which was unsuitable for space applications based on its single event latchup threshold characteristics can now be used in a space environment using SEI's LPT™ technology.

SEI's latchup protected ADS7805 is available as the 7805RPLP multi-chip module. This technology can be applied to a wide range of devices in order to provide new options for the use of commercially developed, leading edge technology components in a space environment at a minimum cost.

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