ASIC for Single Event Latchup Protection of Commercial Integrated Circuits

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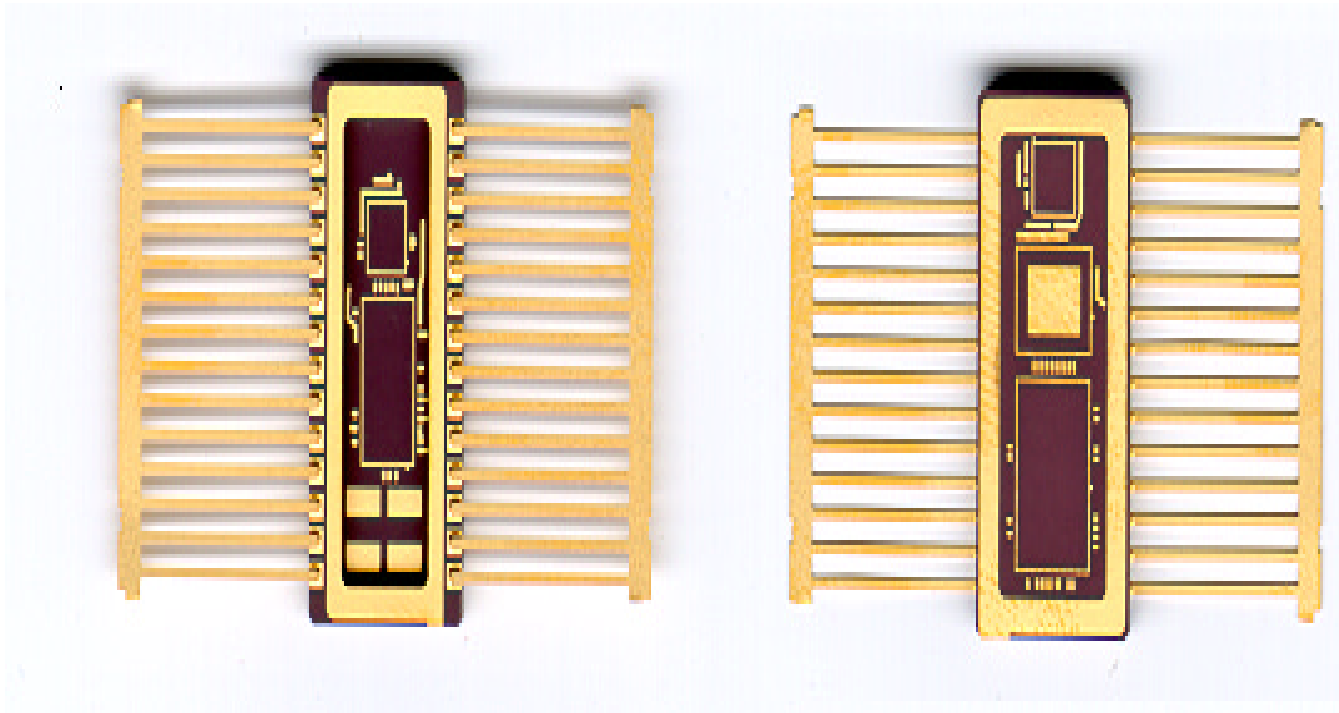
The LPT™ Circuit Method

- **Provide current limiting to the device.**
- **Detect the increase in current above a preset threshold level caused by a SEL event.**
- **Force a shutdown of the protected device when the threshold is exceeded.**
- **Leave the device in the shutdown mode for a preset time, to allow the latchup current to dissipate.**
- **Return the supply voltage to its original operating level.**

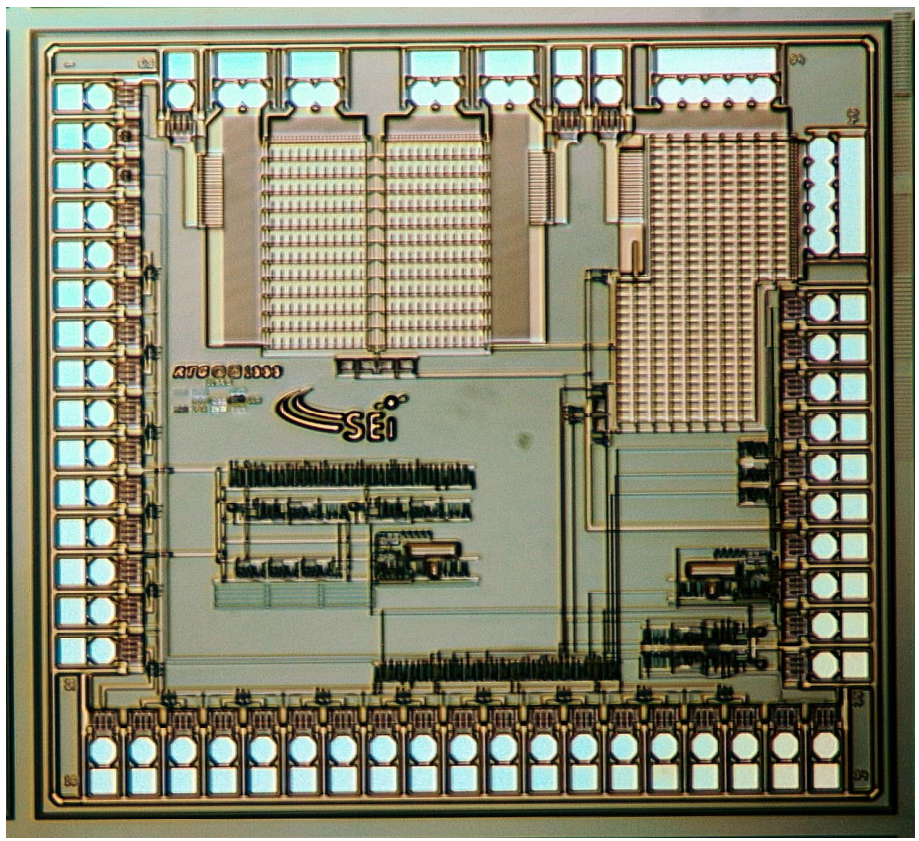
7805 MCM Substrate, Top and Bottom, Discrete MCM



Lessons Learned

- **Cycling power alone is not sufficient to return the device from a latched state.**
- **Each device type needs to be validated at a heavy ion source to properly characterize the circuit.**
- **Microlatching can prevent the application of latchup protection to a device.**
- **Total Ionizing Dose (TID) can increase the supply current, effecting the performance of the latchup protection circuit.**
- **Discrete MCM is a logistics pain!**

LPT ASIC Die



- small die size
  130 mils x 173 mils
- protects 14 inputs
- low leakage
- double pads (probe & bond)
- V_{cc} = 5 volts± 10%
- ESD > 2000 volts
- 0.6µ CMOS epi

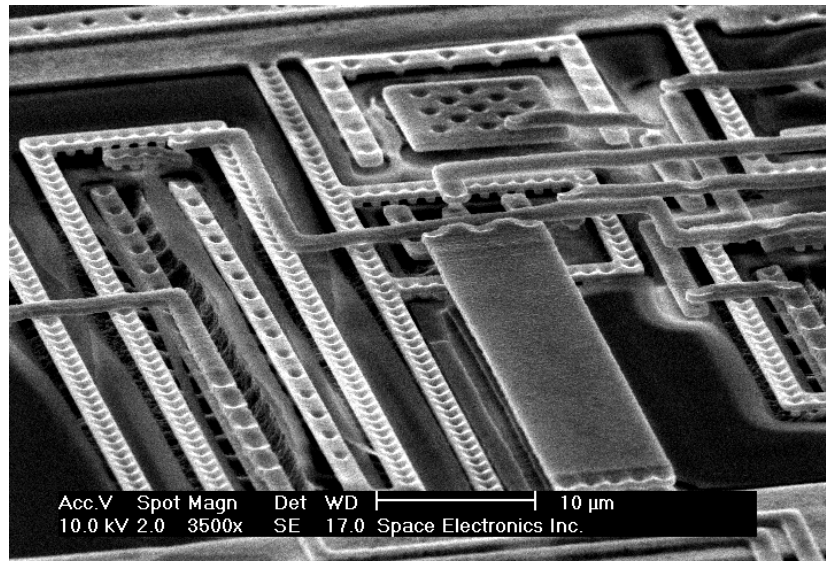
Wafer Lot Acceptance

DEVICE THICKNESS MEASUREMENTS

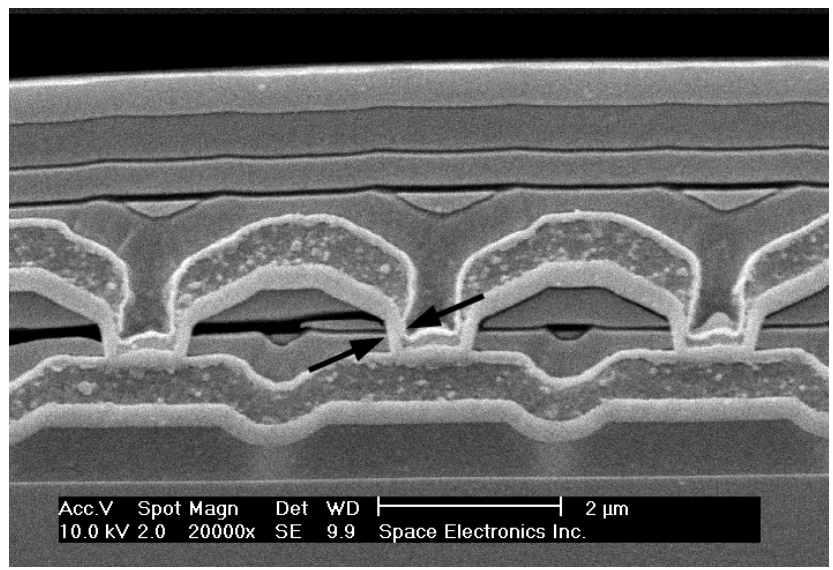
PROCESS LAYER	Minimums	Die #1
Glassivation (Si_3N_4)	2KÅ	4,780 Å
Glassivation (SiO_2)	6KÅ	11,960 Å
Barrier / Conduction Layer (Ti-W)		1,120 Å
Metal 2 (Aluminum)	8KÅ	4,500 Å
Barrier / Conduction Layer (Ti-W)		3,370 Å
Barrier / Conduction Layer (Ti-W)		1,270 Å
Metal 1 (Aluminum)	5KÅ	4,640 Å
Barrier / Conduction Layer (Ti-W)		2,870 Å
Epitaxial Layer (microns)		10 µ
Backside Metal		2.5 µ
Die Thickness	6.0mil	24.21 mil
Die Size (137.6 x 129.6 mils)		17,832.96 mil^2
Die Bond Pad Size		4 x 4 mil

SEM Analysis

- per MIL-STD-883 Method 2010
- Philips XL30 digital SEM @ 10kV
- Worst case step coverage ~20%



- Max current density 7 x 10^4 A/cm^2



Electrical Data

N = 44 units
Test platform: TMT Mixed Signal ATE
Ta = 25°C

	Power On Switch Vdrop			Sense Threshold			I/O switch closed leakages		I/O switch open leakages	
Parameter	dVin1	dVin2	dVin3	Vth_SNS1	Vth_SNS2	Vth_SNS3	IL_IO1_cL	IL_IO1_cH	IL_IO1_oL	IL_IO1_oH
Max Limit	0.21	0.15	0.15	2.51	2.51	2.51	1	1	1	1
Min Limit	0	0	0	2.49	2.49	2.49	-0.1	-0.1	-0.1	-0.1
Mean	0.0244	0.0283	0.0320	2.4993	2.4989	2.4997	-0.0022	-0.0034	-0.0033	-0.0015
Std Dev	0.0004	0.0004	0.0011	0.0026	0.0031	0.0029	0.0063	0.0055	0.0068	0.0077

ELECTRONIC COMPONENTS GROUP

MAXWELL TECHNOLOGIES

Radiation Data from BNL

	Ion	Energy	Range	LET(Si)	Tilt
# of Runs		MeV	um	MeV.cm2/mg	deg
4	Cl-35	210	63.5	11.4	0
2	Cl-35	210	44.9	16.2	45
12	Br-81	283	36.5	37.4	0
11	Br-81	283	25.8	52.9	45
8	Au-197	348	28.3	82.2	0
6	Au-197	348	20	116	45

No Latchup observed

LPT ASIC Total Dose

- **Foundry pre-qualified for > 50kRad (Si)**
- **Tested at Maxwell HDR Co-60**
- **Sample size = 5 units**
- **All units pass parametric spec at 50KRad (Si)**
- **Used in SEi RAD-PAK® MCM to extend space TID performance**

LPT™ Applications

- **Used in several SEi standard products**
  - 7809 LP 16 bit ADC
- **Future SEi products requiring Latchup protection**
- **Available as standalone part from SEi**
  - **packaged IC in 44QFP**
  - **probed die in waffle packs**