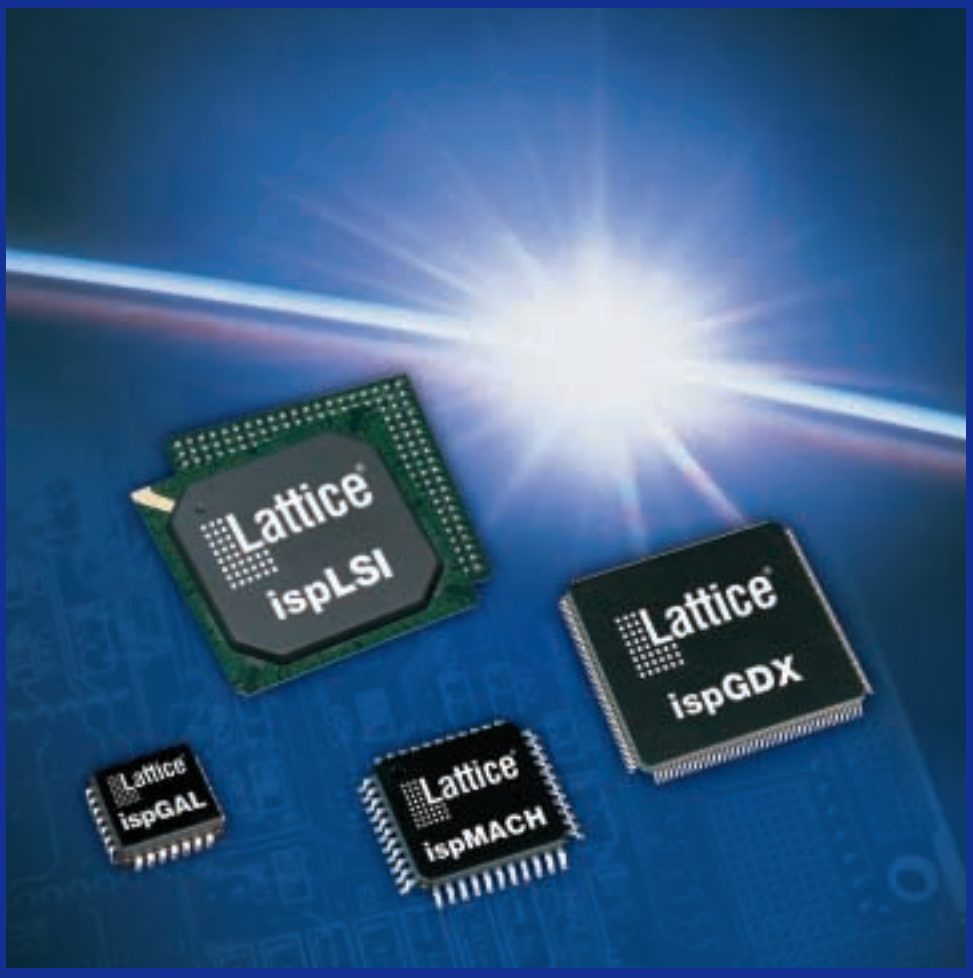
L A T T I C E  S E M I C O N D U C T O R

New Dimensions in ISP™

# Programmable Logic Devices




Lattice® Semiconductor Corporation

# Lattice: More than Programmable Logic

*"A vision of the ultimate system — analog, digital, and everything in between, instantly re-programmable."*

*Lattice provides solutions for the full array of electronic system design challenges. Analog, interconnect and logic applications are all covered by Lattice's high performance ISP™ (in-system programmable) products. With Lattice ISP devices, you can achieve faster time-to-market, lower overall cost, and in-field reconfiguration in all aspects of system design and operation.*

*Through the efforts of a worldwide development team, Lattice is working towards next generation ISP solutions in each of these areas and, in doing so, is laying the groundwork for building the integrated programmable chip of tomorrow. A global manufacturing network complements this development capability and provides the resources necessary to supply Lattice ISP solutions in high volume.*

*Lattice provides the tools and support necessary to utilize each of these building blocks. The ispDesignEXPERT™ package provides a comprehensive suite of tools ranging from HDL entry to device programming. The devices and design tools are coupled with a worldwide network of product support specialists to help you utilize ISP in your system.*

## A Global

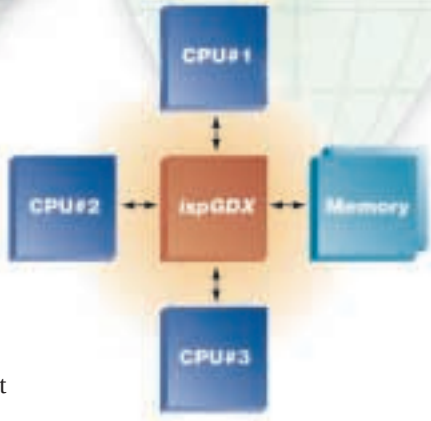
Sales & Support
- Finland
- France
- Germany
- Hong Kong
- Israel
- Italy
- Japan
- Korea
- Singapore
- Sweden
- Taiwan
- United Kingdom
- United States

R&D Centers
- Oregon
- California
- China
- Colorado
- Texas
- United Kingdom

## ISP Switching Solutions

**ISP Solutions for System-Level Signal Switching and Interface**

- Bus interface logic
- Multi-port memory interface
- Bus-width translation
- Electronic "Dip Switch" integration
- Provides boundary scan test support for critical system interfaces




## Lattice: A History of Innovation and Performance.

**1969** — MMI founded.

**1978** — MMI introduces the PAL device.

**1983** — Lattice founded.

**1984** — MMI introduces the 22V10 architecture.

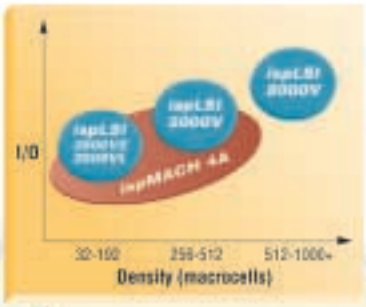
**1985** — Lattice invents GAL architecture. Lattice introduces E²CMOS PLDs.

**1987** — MMI acquired by AMD.

**1988** — Cyrus Tsui leaves AMD to become CEO of Lattice.

**1990** — MACH devices introduced with patented switch matrix architecture used today in all CPLDs.

## ISP CPLD Solutions




**The World's Best CPLD Portfolio**

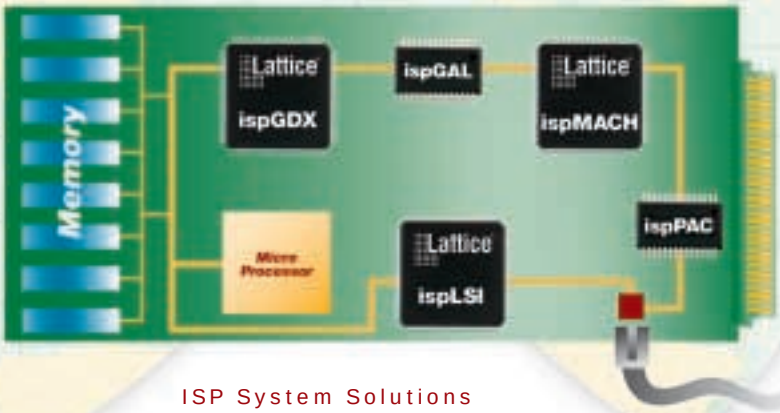
- ispLSI 5000V–delivers performance through architecture featuring 68-input logic blocks
- ispMACH 4A–industry's broadest, full featured CPLD family
- ispLSI 2000–industry's fastest CPLD families at 2.5V, 3.3V and 5V
- ispLSI 8000V–industry's highest density CPLDs


## ISP Analog Solutions

**A Revolution in Analog Design**

- Brings Benefits of ISP to Analog Circuit Design
- Precision Analog Performance
- Replaces Multiple Analog Components
- Fast and Easy Software Design Tools
- Extensive Technical Support

# Presence




## ISP System Solutions

**Lattice Delivers In-System Programmability for System Design**

- ispLSI®/ispMACH™ for Digital Logic
- ispPAC™ for Analog
- ispGDX™ for Board-Level Signal Switching and Interface

## Design Tools

**World-Class Development Tools**

- Complete Solutions for 3rd Party PC or Workstation EDA Environments
- Integrated Design Environment for all Lattice Products
- Optimized HDL Design Methodologies
- Industry's Broadest OEM Relationships

1992 — First ISP CPLDs.

1994 — First ispSTARTER Kit tools.

1995 — 3.5 ns CMOS GAL speed beats bipolar PAL.

1996 — VANTIS AMD spins off PLD division.

1997 — Lattice introduces ispGDX family

1998 — Industry-leading SuperBIG, SuperFAST, SuperWIDE ispCPLDs introduced by Lattice.

1999 — Lattice and Vantis merge. Lattice introduces ispPAC.

# ispMACH 4A

THE INDUSTRY'S

## Ease-of-Use Enables Fast Time-to-Market!

- **Broad I/O and Macrocell Options**
- **High-Performance, Low-Power CPLDs**

## The ispMACH 4A CPLD Family


***The ispMACH 4A CPLD*** *family provides programmable logic solutions that address designers' requirements for high performance, fast time-to-market and easy system integration.*

### Family Features

- 3.3V and 5V Versions
- 32 to 512 Macrocells; 1,250-20,000 PLD Gates
- 5.0 ns Pin-to-Pin Delay; 182 MHz System Performance
- SpeedLocking™ Performance
  - Guaranteed Fixed Timing
- Low Power Consumption
- Excellent Routability and Pin-Locking
- Hot-Socketing Capability
- Programmable Bus Friendly or Pull-up I/Os
- IEEE 1149.1 Boundary Scan Testable
- ispJTAG™ In-System Programmable

### Family Architecture

- Multiple Switch Matrices Support Routability and Pin-Locking
  - Input Switch Matrix (ISM)
  - Central Switch Matrix (CSM)
  - Output Switch Matrix (OSM)
- PAL Blocks Interconnected by CSM
- Up to 36 Inputs per PAL® Block
- 16 Macrocells per PAL Block
- Up to 20 Product Terms per Output

### Flexible Control Logic

ispMACH 4A Devices Provide Flexible Control Logic That Can Adapt to Designers' Needs. They Provide:

- Individual Product Term Initialization
- Individual Product Term Clock
- Individual Output Enable Control
- Dedicated Input Registers

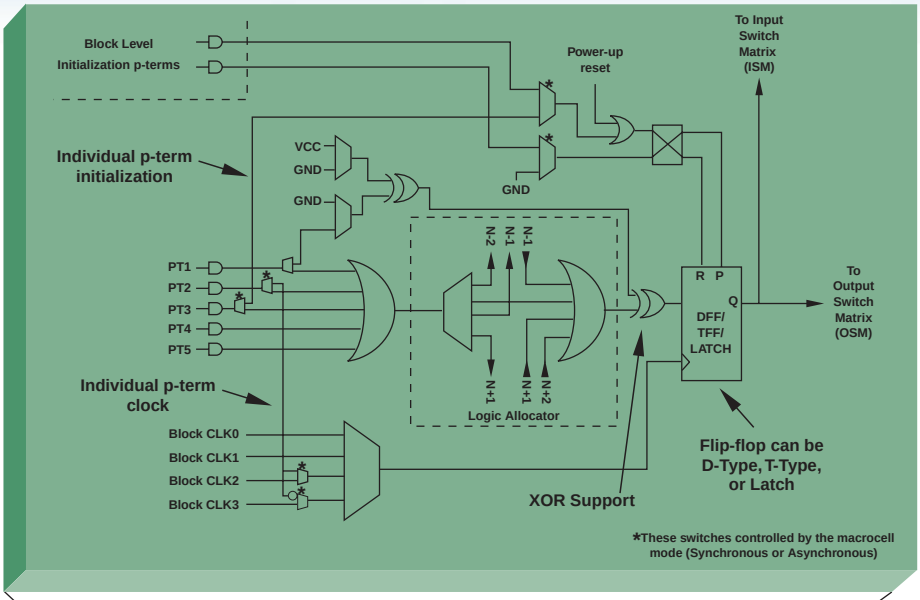
| ispMACH 4A Family | M4A3-32/ M4A5-32 | M4A3-64/ M4A5-64 | M4A3-96/ M4A5-96 | M4A3-128/ M4A5-128 | M4A3-192/ M4A5-192 | M4A3-256/ M4A5-256 | M4A3-256 | M4A3-384 | M4A3-512 |
|---|---|---|---|---|---|---|---|---|---|
| Density (PLD Gates) | 1250 | 2500 | 3750 | 5000 | 7500 | 10000 | 10000 | 15000 | 20000 |
| Macrocells | 32 | 64 | 96 | 128 | 192 | 256 | 256 | 384 | 512 |
| Speed - Tpd (ns) | 5.0 | 5.5 | 5.5 | 5.5 | 6.5 | 5.5 | 7.5 | 6.5 | 7.5 |
| Speed - Fmax (MHz) | 182 | 167 | 167 | 167 | 154 | 167 | 125 | 154 | 125 |
| Total Registers | 32 | 96 | 144 | 192 | 288 | 384 | 256 | 576 | 768 |
| I/Os + Inputs | 32+2 | 64+6 | 48+8 | 64+6 | 96+16 | 128+14 | 160*, 192* | 160*, 190* | 160*,192*, 256* |
| Vcc (Volts) | 3.3/5 | 3.3/5 | 3.3/5 | 3.3/5 | 3.3/5 | 3.3/5 | 3.3 | 3.3 | 3.3 |
| Pin/Package | 44-PLCC<br>44-TQFP<br>48-TQFP | 44-PLCC<br>44-TQFP<br>48-TQFP | 100-TQFP | 100-PQFP<br>100-TQFP<br>100-caBGA | 144-TQFP<br>144-fpBGA | 208-PQFP<br>256-BGA<br>256-fpBGA | 208-PQFP<br>256-fpBGA | 208-PQFP<br>256-BGA<br>256-fpBGA | 208-PQFP<br>256-BGA<br>388-fpBGA |

* I/O Options Shown. No Dedicated Inputs on These Devices.

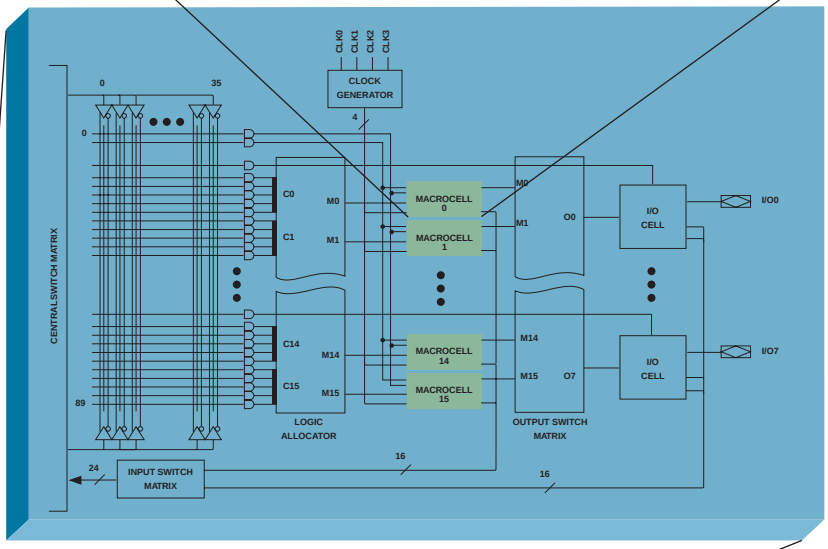
= Single Package, Density Migration

## System Integration

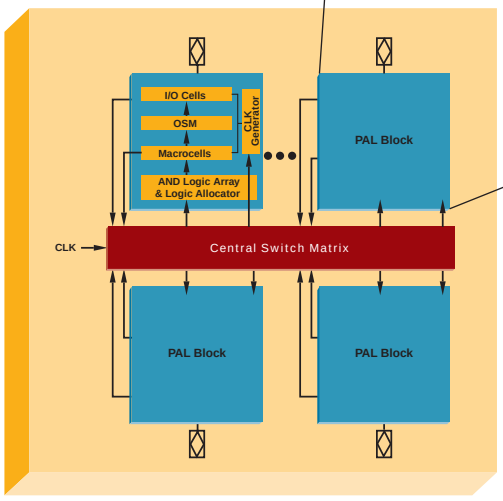
- Commercial and Industrial Temperature Ranges
- Slew Rate Control to Reduce Ground Bounce and Increase System Speed
- Power Management Mode




*ispMACH 4A Macrocell*




*ispMACH 4A PAL Block*



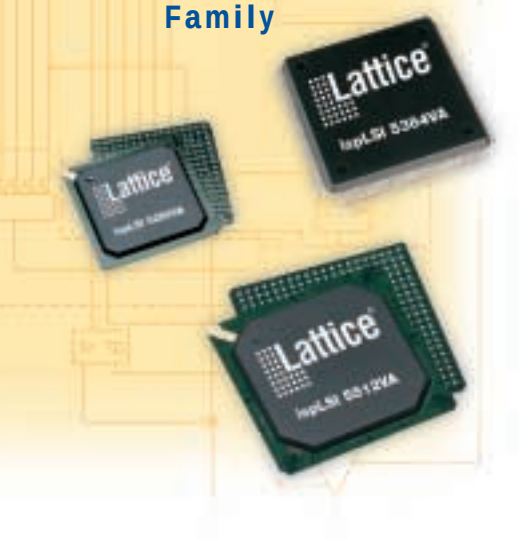

*ispMACH 4A Architecture*

# 5KV

THE INDUSTRY'S WIDEST CPLDS

## 68-Input/32 Macrocell Logic Blocks are the Industry's Widest!

## 3.3V SuperWIDE™ ISP CPLD Family




***Lattice's SuperWIDE ispLSI 5000V*** *Family incorporates a revolutionary new architecture, which provides unparalleled performance for today's 32- and 64-bit wide, logic functions. Wide input logic blocks provide unparalleled performance.*

### Family Features

- 256 to 512 Macrocells; 12,000-24,000 PLD Gates
- 68 Input SuperWIDE Logic Blocks
- 7.5 ns Pin-to-Pin Delay; 125 MHz System Performance
- User Selectable 3.3V/2.5V I/O
  - Pin-By-Pin
  - 5V Tolerant Inputs
- Very High Register and I/O Density
- 208-Ball to 388-Ball BGA Options
- IEEE 1149.1 Boundary Scan Testable
- ispJTAG In-System Programmable

### Family Architecture

- Enhanced Single-Level Global Routing Pool (GRP)
- Concurrent Combinatorial/ Register Outputs
- Enhanced Generic Logic Block (GLB)
  - SuperWIDE, 68-Input GLB Fan-In - Widest of any CPLD
  - 32 Macrocell Logic Block
  - Product Term Sharing Array (PTSA) Supports Very Wide Logic Functions
    - 160 Product Terms
    - Up to 35 Product Terms per Output
  - 5 Product Terms per GLB for Control Logic

| ispLSI 5000V Family | ispLSI 5256VA | ispLSI 5384VA | ispLSI 5512VA |
|---|---|---|---|
| Density (PLD Gates) | 12000 | 18000 | 24000 |
| Macrocells | 256 | 384 | 512 |
| Speed - Tpd (ns) | 7.5 | 7.5 | 8.5 |
| Speed - Fmax (MHz) | 125 | 125 | 110 |
| I/Os + Inputs* | 144, 192 | 144, 192, 288 | 144, 192, 288 |
| Pin/Package | 208-fpBGA | 208-fpBGA | |
| | 208-PQFP<br>272-BGA | 208-PQFP<br>272-BGA | 208-PQFP<br>272-BGA |
| | | 388-BGA | 388-BGA |

* I/O Options Shown, No Dedicated Inputs in the ispLSI 5000V Family

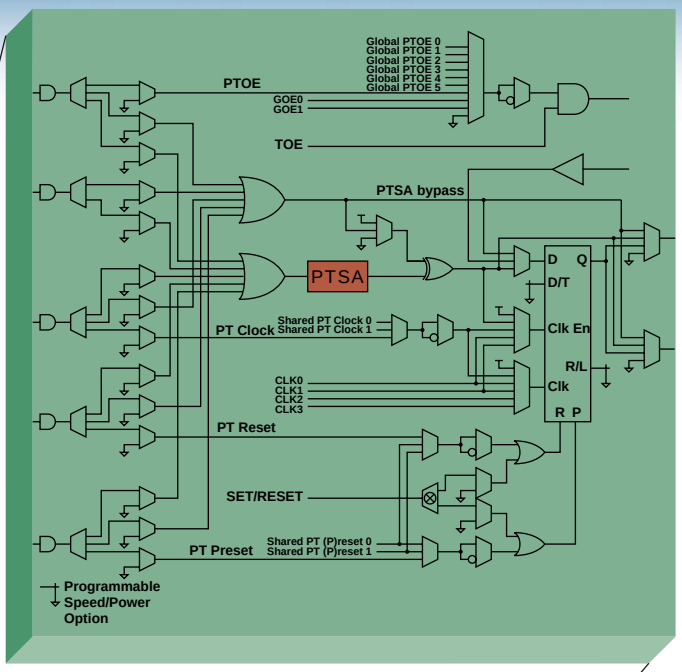
= Single Package, Density Migration

### Flexible Control Logic

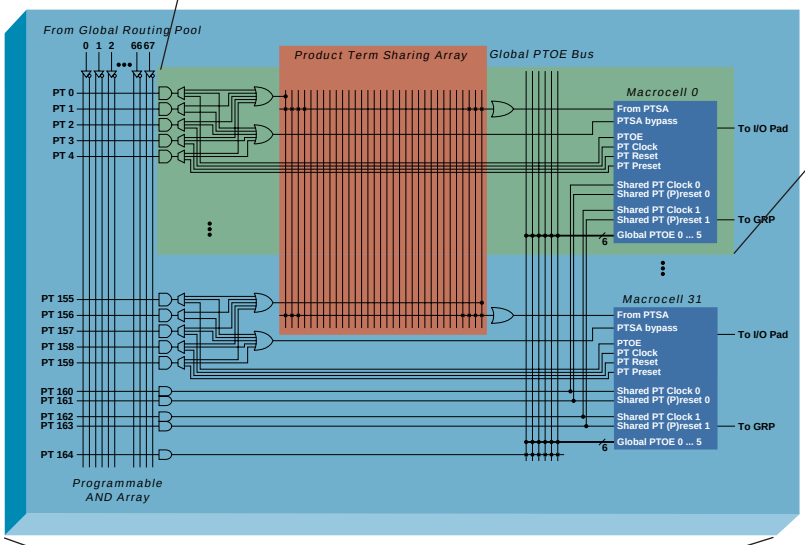
- Multiple Output Enable Options
  - 2 Global OE Pins
  - 6 Global Product Term OEs
  - 1 Product Term OE per I/O
- Multiple Clocks
  - 4 Global Clock Pins
  - 2 Shared Product Term Clocks/GLB
  - 1 Product Term Clock per Macrocell
  - Includes Register Clock Enables
- Individual and Shared Reset/Preset Controls

### System Integration

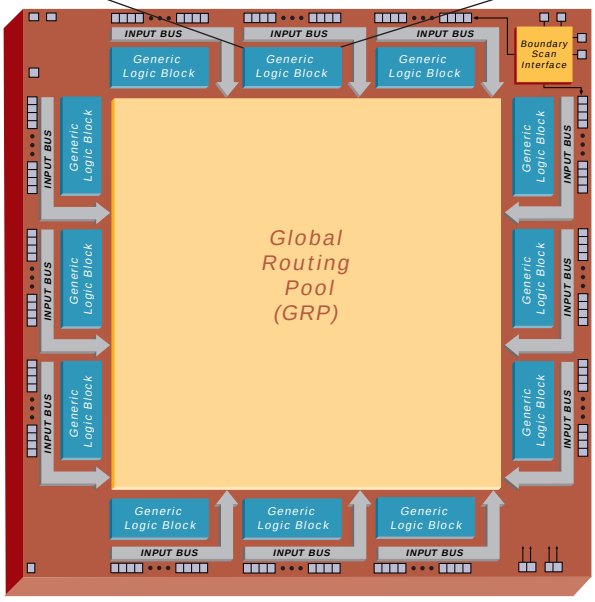
- Programmable Speed/Power Macrocell
  - 50% Power Reduction
- Programmable I/O Control
  - Bus Hold Latch
  - Open Drain Outputs
  - Pull-Up Resistors
  - Slew Rate Control




*ispLSI 5000V Macrocell*




*ispLSI 5000V Generic Logic Block*




*ispLSI 5000V Architecture*

# 2K

THE INDUSTRY'S FASTEST CPLDS

## SuperFAST™ ispLSI 2000 Family

## Unparalleled 3.5ns, 250 MHz Performance!
## ■ Available in 5V, 3.3V and 2.5V Operating Ranges

***Lattice SuperFAST ispLSI 2000*** *Families deliver the performance you need from your programmable logic devices. Designed specifically to perform in your most demanding applications, the ispLSI 2000E/VE/VL members are the fastest PLDs available in the universe! With families available in 5V, 3.3V, and 2.5V operating ranges, the ispLSI 2000 families have options to support your current designs as well as next-generation projects in the new millennium.*

### Family Features

**ispLSI 2000E Family**

- 5V Family with 4 Members Ranging from 32 to 128 Macrocells
- Industry's Fastest PLDs at 3.5ns!
- Supports 3.3V or 5V I/O
- JEDEC Compatible to ispLSI 2000 Family
- PCI Compatible
- ispJTAG In-System Programmable


**ispLSI 2000VE Family**

- 3.3V Family with 5 Members Ranging from 32 to 192 Macrocells
- JEDEC and Pin Compatible to Original ispLSI 2000V Family
- Density/Package Migration Paths
- Supports 3.3V or 5V I/O
- IEEE 1149.1 Boundary Scan Testable
- ispJTAG In-System Programmable

**ispLSI 2000VL Family**

- 2.5V Family with 5 Members Ranging from 32 to 192 Macrocells
- All Devices Shipping Today!
- Supports 2.5V or 3.3V I/O
- JEDEC and Pin Compatible to 2000VE Family
- Density/Package Migration Paths
- IEEE 1149.1 Boundary Scan Testable
- ispJTAG In-System Programmable

### Family Architecture

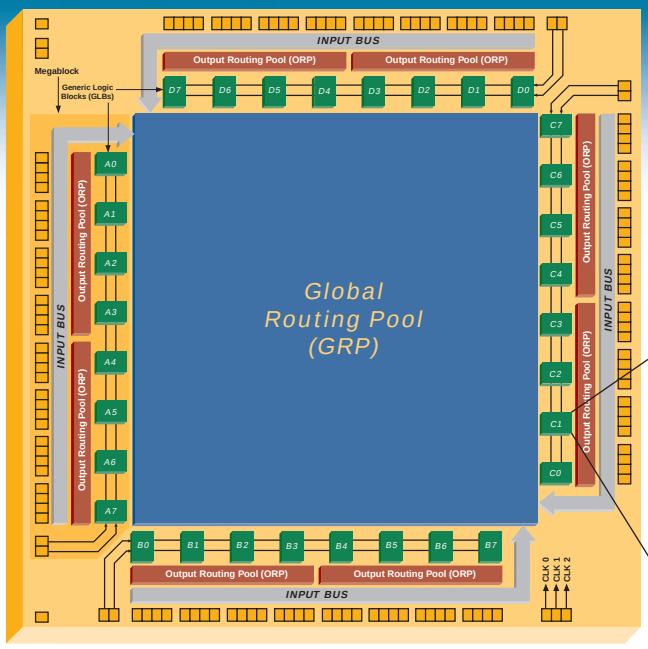
- Fine-Grained
  - 18 Input/4 Output GLB
- Enhanced Single-Level Global Routing Pool (GRP)
- Output Routing Pool for Enhanced Pin Locking
- Fast and Predictable GRP

### Flexible Control Logic

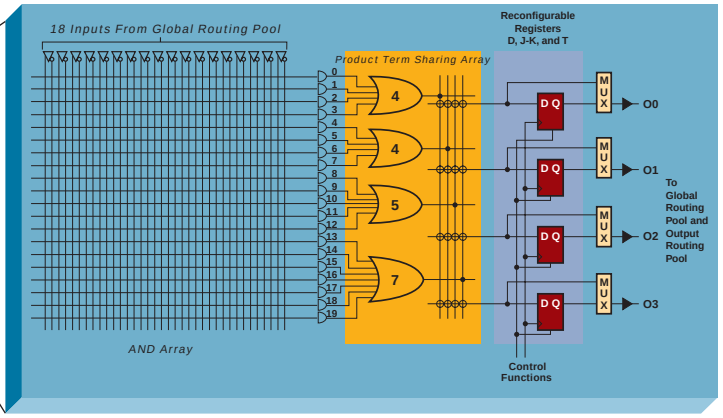
- Global Output Enables
- Flexible Clocking
- Megablock Output Enables

### System Integration

- Fast or Slow Output Slew Rate
- PCI Compatible (2000E)
- 3.3V (2000E/2000VE) or 2.5V (2000VL) Outputs




*ispLSI 2000 Architecture*




*ispLSI 2000 Generic Logic Block*

| ispLSI 2000E Family (5V) | ispLSI 2032E | ispLSI 2064E | ispLSI 2096E | ispLSI 2128E |
|---|---|---|---|---|
| Density (PLD Gates) | 1000 | 2000 | 4000 | 6000 |
| Macrocells | 32 | 64 | 96 | 128 |
| Speed - Tpd (ns) | 3.5 | 4.5 | 5 | 5 |
| Speed - Fmax (MHz) | 225 | 200 | 180 | 180 |
| I/Os + Inputs | 32+3 | 64+6 | 96+8 | 128+10 |
| Pin/Package | 44-PLCC<br>44-TQFP<br>48-TQFP | 100-TQFP | 128-PQFP<br>128-TQFP | 176-TQFP |

| ispLSI 2000VE Family (3.3V) | ispLSI 2032VE | ispLSI 2064VE | ispLSI 2096VE | ispLSI 2128VE | ispLSI 2192VE |
|---|---|---|---|---|---|
| Density (PLD Gates) | 1000 | 2000 | 4000 | 6000 | 8000 |
| Macrocells | 32 | 64 | 96 | 128 | 192 |
| Speed - Tpd (ns) | 4 | 4.5 | 4.5 | 4 | 4 |
| Speed - Fmax (MHz) | 225 | 200 | 200 | 250 | 225 |
| I/Os + Inputs | 32+3 | 32+5<br>64+6 | 96+8 | 64+10<br>128+10 | 96+11 |
| Pin/Package | 44-PLCC<br>44-TQFP<br>48-TQFP<br>49-caBGA | 44-PLCC<br>44-TQFP<br>100-TQFP<br>100-caBGA | 128-TQFP | 100-TQFP<br>100-caBGA<br>176-TQFP<br>160-PQFP<br>208-fpBGA | 128-TQFP<br>144-fpBGA |

| ispLSI 2000VL Family (2.5V) | ispLSI 2032VL | ispLSI 2064VL | ispLSI 2096VL | ispLSI 2128VL | ispLSI 2192VL |
|---|---|---|---|---|---|
| Density (PLD Gates) | 1000 | 2000 | 4000 | 6000 | 8000 |
| Macrocells | 32 | 64 | 96 | 128 | 192 |
| Speed - Tpd (ns) | 5 | 5.5 | 5.5 | 6 | 6 |
| Speed - Fmax (MHz) | 180 | 165 | 165 | 150 | 150 |
| I/Os + Inputs | 32+3 | 32+5<br>64+6 | 96+8 | 64+10<br>128+10 | 96+11 |
| Pin/Package | 44-PLCC<br>44-TQFP<br>48-TQFP<br>49-caBGA | 44-PLCC<br>44-TQFP<br>100-TQFP<br>100-caBGA | 128-TQFP | 100-TQFP<br>100-caBGA<br>176-TQFP<br>160-PQFP<br>208-fpBGA | 128-TQFP<br>144-fpBGA |

= Single Package, Density Migration

# 8K

THE HIGHEST DENSITY CPLDS IN THE INDUSTRY

## Up to 1,080 Macrocells and 1,440 Total Registers in a Single CPLD!

## The SuperBIG™ ispLSI 8000 Family


***The SuperBIG ispLSI 8000*** *Family provides the highest macrocell count and most register rich PLDs ever produced. The ispLSI 8000 Family available in both 5V and 3.3V versions offers a revolutionary hierarchical architecture, which is constructed with 120-macrocell Big Fast Megablocks, interconnected via a Global Routing Plane with Internal Tristate Busses.*

### Family Features

- 600 to 1,080 Macrocells; 32,000 to 60,000 PLD Gates!
- 864 to 1,440 Total Registers
- 5V and 3.3V Versions
- 8.5 ns Pin-to-Pin Delay; 125 MHz System Performance
- IEEE 1149.1 Boundary Scan Testable
- ispJTAG In-System Programmable

### Family Architecture

- First CPLDs with Internal Tristate Busses
- Programmable Speed/Power Macrocell
- Extra-Wide Generic Logic Block (GLB) (44 Inputs and 20 Macrocells)
- Dedicated I/O Registers

### System Integration

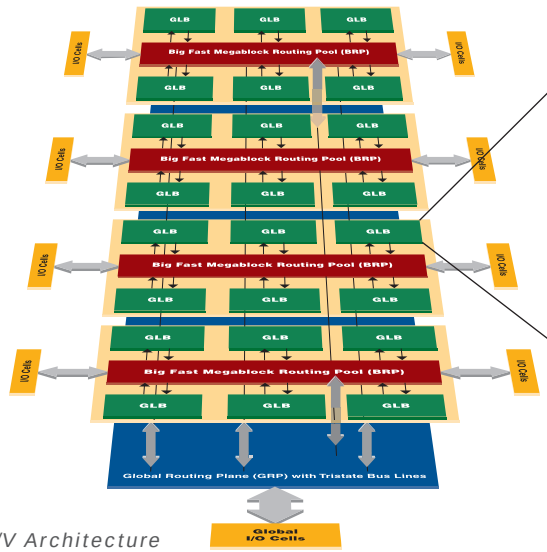
- User Selectable 5V/3.3V/2.5V I/O
- Open-Drain and Bus Hold Options
- Programmable Pull-up Resistors

| ispLSI 8000/V Family | ispLSI 8600V | ispLSI 8840V/8840 | ispLSI 81080V |
|---|---|---|---|
| Density (PLD Gates) | 32,000 | 45,000 | 60,000 |
| Macrocells | 600 | 840 | 1080 |
| Speed - Tpd (ns) | 8.5 | 8.5 | 8.5 |
| Speed - Fmax (MHz) | 125 | 125/110* | 125 |
| Total Registers | 864 | 1,152 | 1,440 |
| I/Os + Inputs** | 192, 264 | 192, 312 | 192, 360 |
| Vcc (Volts) | 3.3 | 3.3/5 | 3.3 |
| Pin/Package | 272-BGA<br>492-BGA | 272-BGA<br>492-BGA<br>432-BGA* | 272-BGA<br>492-BGA |

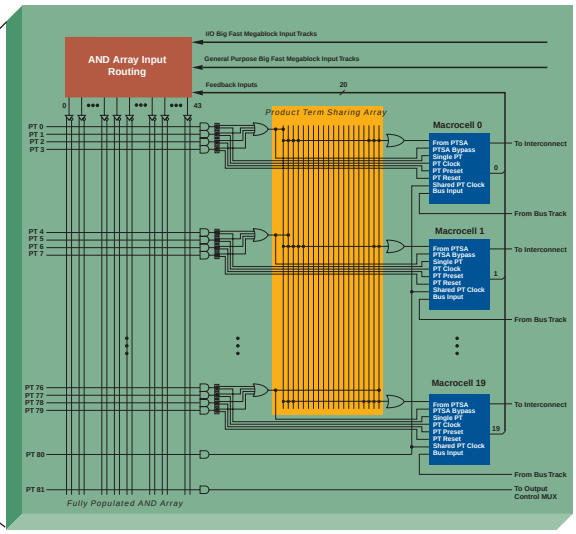
* Available for 5V 8840

** I/O Options Shown. No Dedicated Inputs in the ispLSI 8000/V Family

= Single Package, Density Migration




*ispLSI 8000/V Architecture*

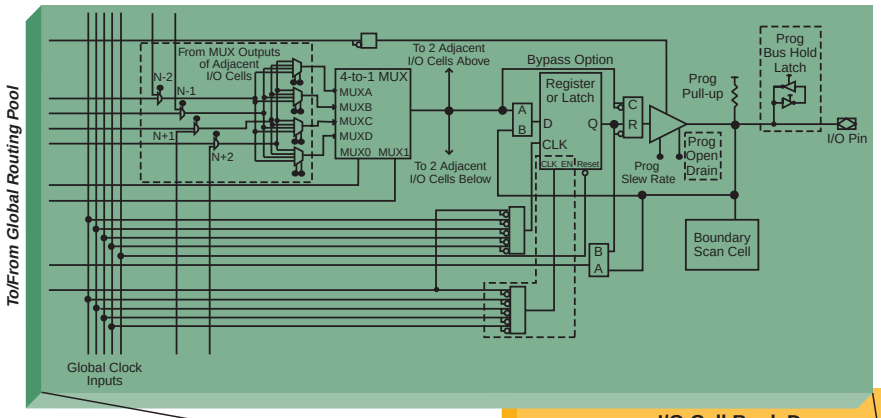



*ispLSI 8000/V Generic Logic Block*

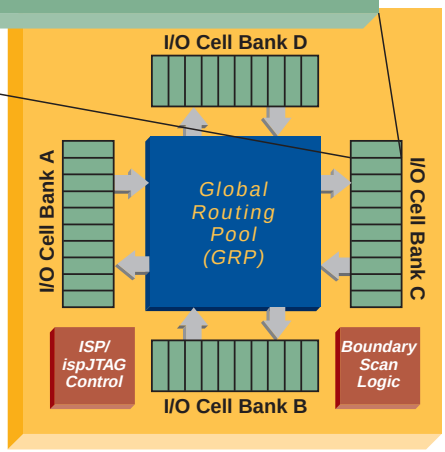
# ispGDX

## Industry's First Optimized ISP Signal Routing/Interface Architecture

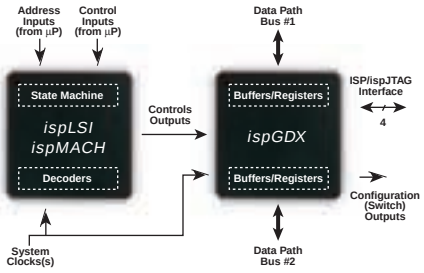
***The ispGDX*** *is an innovative architecture optimized for system-level signal routing and interface applications. Available in both 5V and 3.3V versions, the ispGDX Generic Digital Crosspoint Devices provide unprecedented performance and flexibility, supporting applications traditionally not addressed by CPLDs or FPGAs.*


ispGDXV Architecure Enhancements




### ispGDX/V: The Perfect Complement to CPLDs




- ispLSI/MACH for Fast Control Logic
- ispGDX for Fast Interface Logic and Signal Routing

### Family Features

- 5V and 3.3V Versions
- 3.5ns Pin-to-Pin Performance
- 80-240 I/O
- Any-Pin to Any-Pin Routing
- IEEE 1149.1 Boundary Scan Testable
- ispJTAG In-System Programmable

### Family Architecture

- Programmable I/O Features (Combinatorial/Register/Latch)
- Programmable Fast Wide MUX (4:1 up to 16:1* MUX)
- Abundance of I/O Control
- Bus Hold Latch*
- Clock Enable*

* Available in 3.3V ispGDXV version only

| ispGDX/V SuperSWITCHING Family | ispGDX 80A/VA | ispGDX 120A | ispGDX 160A/VA | ispGDX 240VA |
|---|---|---|---|---|
| Speed - Tpd (ns) | 5/3.5 | 5 | 5/3.5 | 4.5 |
| Speed - Fmax (MHz) | 143/250 | 143 | 143/250 | 167 |
| I/Os | 80 | 120 | 160 | 240 |
| Registers | 80 | 120 | 160 | 240 |
| Dedicated Clock Pins | 2 | 4 | 4 | 4 |
| Vcc (Volts) | 5/3.3 | 5 | 5/3.3 | 3.3 |
| Package | 100-TQFP | 176-TQFP<br>160-PQFP | 208-PQFP<br>208-fpBGA<br>272-BGA | 388-fpBGA |

# 1KEA

THE PREMIER ISP FAMILY

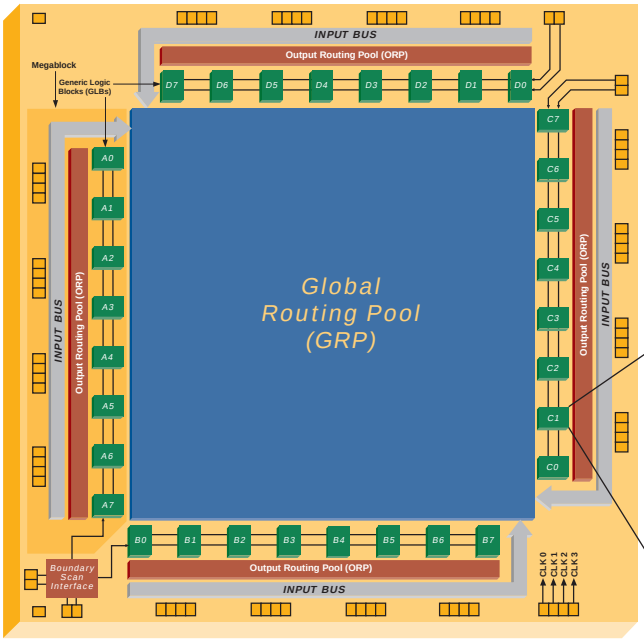
## The Industry Standard 5V ISP CPLD Family

***The ispLSI 1000EA Family*** *offers the industry's highest performance 5V CPLDs. With a winning combination of performance and density, the ispLSI 1000EA Family supports system designs requiring high speed and highly integrated logic.*

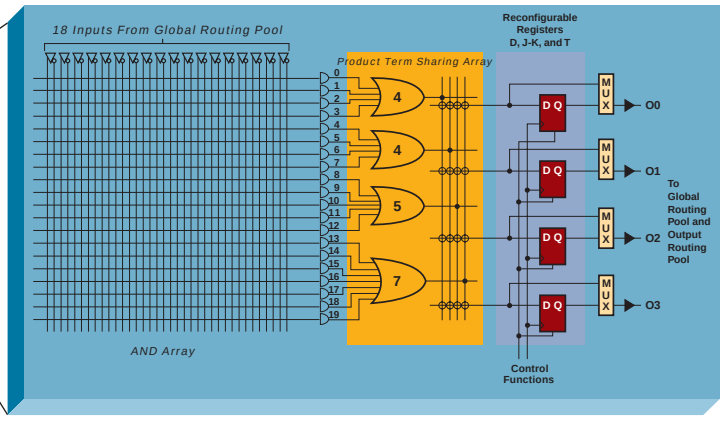
### ispLSI 1000EA Family

- 5V Power Supply
- User Selectable 5V/3.3V I/O
- IEEE 1149.1 Boundary Scan Testable
- ispJTAG In-System Programmable

| ispLSI 1000/EA Family | ispLSI 1016EA | ispLSI 1024EA | ispLSI 1032EA | ispLSI 1048EA |
|---|---|---|---|---|
| Density (PLD Gates) | 2000 | 4000 | 6000 | 8000 |
| Macrocells | 64 | 96 | 128 | 192 |
| Speed - Tpd (ns) | 4.5 | 4.5 | 4.5 | 5 |
| Speed - Fmax (MHz) | 200 | 200 | 200 | 170 |
| Total Registers | 96 | 144 | 192 | 288 |
| I/Os + Inputs | 32+1 | 48+2 | 64+4 | 96+8 |
| Pin/Package | 44-PLCC<br>44-TQFP | 100-TQFP | 100-TQFP | 128-PQFP<br>128-TQFP |




*ispLSI 1000EA Architecture*




*ispLSI 1000EA Generic Logic Block*

= Single Package, Density Migration

# MACH 5

GENERAL PURPOSE CPLDS

## A Wide Selection of Speed, Densities and Packages

***The MACH 5 Family*** *provides high performance solutions for medium to high-density CPLD applications. The MACH 5 Family features a high-speed hierarchical architecture for maximum system performance.*

### MACH 5 Families

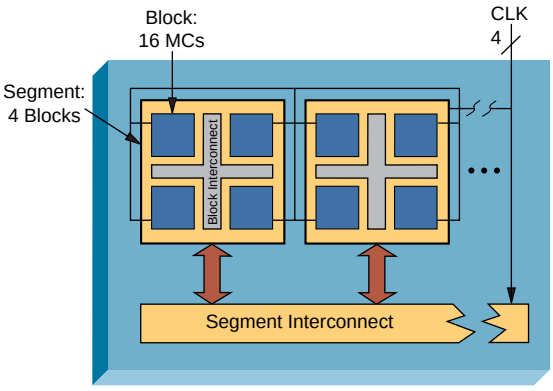
- 128 to 512 Macrocells
- Low Power Consumption
- User Selectable 5V/3.3V I/O
- ispJTAG In-System Programmable
- IEEE 1149.1 Boundary Scan Testable

| MACH 5LV Family (3.3V) | M5LV-128 | M5LV-256 | M5LV-320 | M5LV-384 | M5LV-512 |
|---|---|---|---|---|---|
| Density (PLD Gates) | 5000 | 10000 | 12500 | 15000 | 20000 |
| Macrocells | 128 | 256 | 320 | 384 | 512 |
| Speed - Tpd (ns) | 5.5 | 5.5 | 6.5 | 6.5 | 6.5 |
| Speed - Fmax (MHz) | 182 | 182 | 167 | 167 | 167 |
| I/Os + Inputs* | 68 - 120 | 74 - 160 | 120 - 160 | 120 - 160 | 120 - 256 |
| Vcc (Volts) | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V |
| Pin/Package | 100-TQFP<br>144-TQFP<br>160-PQFP | 100-TQFP<br>144-TQFP<br>160-PQFP<br>208-PQFP | 160-PQFP<br>208-PQFP | 160-PQFP<br>208-PQFP | 160-PQFP<br>208-PQFP<br>352-BGA |

* I/O Range Shown, All MACH 5 Devices Have 4 Dedicated Inputs

| MACH 5 Family (5V) | M5-128 | M5-192 | M5-256 | M5-320 | M5-384 | M5-512 |
|---|---|---|---|---|---|---|
| Density (PLD Gates) | 5000 | 7500 | 10000 | 12500 | 15000 | 20000 |
| Macrocells | 128 | 192 | 256 | 320 | 384 | 512 |
| Speed - Tpd (ns) | 5.5 | 5.5 | 5.5 | 6.5 | 6.5 | 6.5 |
| Speed - Fmax (MHz) | 182 | 182 | 182 | 167 | 167 | 167 |
| I/Os + Inputs* | 68 - 120 | 68 - 120 | 68 - 160 | 120 - 192 | 120 - 192 | 120 - 256 |
| Vcc (Volts) | 5 | 5 | 5 | 5 | 5 | 5 |
| Pin/Package | 100-PQFP<br>100-TQFP<br>144-PQFP<br>160-PQFP | 100-TQFP<br>160-PQFP<br>208-PQFP | 100-TQFP<br>160-PQFP<br>208-PQFP | 208-PQFP<br>256-BGA | 208-PQFP | 208-PQFP<br>352-BGA |

* I/O Range Shown, All MACH 5 Devices Have 4 Dedicated Inputs




*MACH 5 Architecture*

# ispGAL GAL/PAL

LOW-DENSITY PLDS

## The Industry's Premier Portfolio of Low-Density PLDs

### ispGAL - Get ISP for Free!

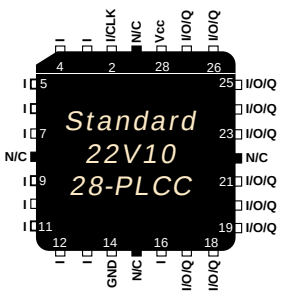
- The Only Low-Density ISP Solution
- Both 5V and 3.3V Versions
- Popular 22V10 Architecture
- Available in Space-Saving SSOP Package
- JEDEC Compatible with GAL22V10, GAL22LV10, PALCE22V10 and PALLV22V10

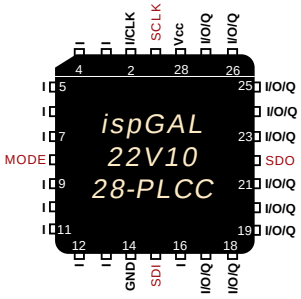
### The Undisputed Market Leader in Low-Density PLDs

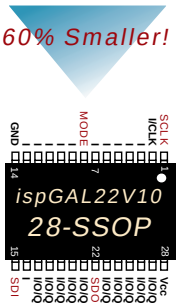
- World-Class Performance in All Industry Standard Architectures
- Broadest Offering of High Performance 3.3V Devices
- Comprehensive Product Portfolio
- Industry's Only Supplier of In-System Programmable Low-Density PLDs
- Military Grade Devices Available

| ispGAL Family | ispGAL 22LV10 | ispGAL 22V10 |
|---|---|---|
| Speed - Tpd (ns) | 4 | 7.5 |
| Speed - Fmax (MHz) | 182 | 111 |
| I/Os and Inputs | 12+10 | 12+10 |
| Vcc (Volts) | 3.3 | 5 |
| Pin/Package | 28-PLCC<br>28-SSOP | 28-PLCC<br>28-SSOP |

| GAL/PAL Families | DEVICE | Tpd (ns) | Max Icc (mA) |
|---|---|---|---|
| Industry Standard | 16V8<br>20V8<br>22V10 | 3.5 - 25<br>5 - 25<br>4 - 25 | 55 - 150 |
| 3.3 Volt | 16/20LV8<br>22LV10<br>26CLV12<br>16/20LV8ZD<br>22LV10Z/ZD | 3.5 - 15<br>4 - 15<br>5 - 7.5<br>15 - 25<br>15 - 25 | 70<br>75 - 130<br>130<br>55 (100µA Isb)<br>55 (100µA Isb) |
| In-System Programmable | ispGAL22LV10<br>ispGAL22V10 | 4 - 10<br>7.5 - 15 | 130<br>140 |
| High Output Drive | 16/20VP8 | 15 - 25 | 115 |
| Zero Power | 16/20V8Z/ZD<br>22V10Z | 12 - 15<br>15 - 25 | 55 (100µA Isb)<br>60 (30µA Isb) |
| Asynchronous Logic | 20RA10<br>29MA16<br>610 | 7.5 - 30<br>25<br>15 - 25 | 100<br>100<br>90 |
| XOR Logic | 20XV10 | 10 - 20 | 90 |
| FPLA | 6001/6002 | 15 - 30 | 135 - 150 |
| 22V10 Extensions | 26V12/26CV12<br>29M16<br>18V10<br>24V10 | 7.5 - 25<br>25<br>7.5 - 25<br>15 - 25 | 130<br>100<br>115<br>115 |




The four ISP control signals of the ispGAL22V10 utilize the "no connect" pins of the 28-pin PLCC standard 22V10 pin-out. The 28-pin SSOP package provides a board area savings of 60%.

# Packages

INDUSTRY'S MOST ADVANCED PACKAGES

## ISP and Advanced Package Technology Deliver System-Level Assembly and Test Optimization


***Lattice Semiconductor*** *offers an industry leading portfolio of innovative packaging solutions available today. Designers are able to choose from advanced high pin count TQFP and BGA packages as well as traditional QFPs and PLCCs. Quality and test problems once associated with these advanced packages are no longer an issue as the devices can be programmed in-system and tested via Boundary Scan test pins at the board level.*

### Advanced Packaging Features

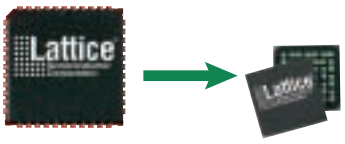
**BGAs**

- 49 to 492 Balls
- Up to 84% Board Area Savings
- Reduced Package Height (1.4mm)
- 1.27mm (BGA), 1.0mm (fpBGA) and 0.8mm (caBGA) Ball Pitch Options
- Greater Misalignment Tolerance, Less Susceptibility to Coplanarity and Easier PCB Routing

**TQFPs**

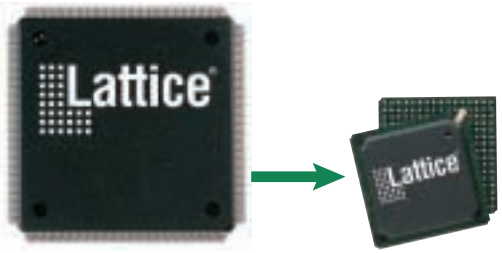
- 44 to 176 Pins
- Up to 75% Board Area Savings Over PLCC
- Reduced Package Height (1.4 mm)
- Reduced Handling with ISP
- No More Bent Leads!

### BGA Board Area Savings




84% smaller

44-PLCC 49-caBGA




70% smaller

208-PQFP 208-fpBGA 256-fpBGA

| Packages | PLCC Plastic Leaded Chip Carrier | QFP Quad Flat Pack (Plastic & Metal) | TQFP Thin Quad Flat Pack | BGA Ball Grid Array | fpBGA Fine Pitch Ball Grid Array | caBGA Chip Array Ball Grid Array |
|---|---|---|---|---|---|---|
| ispMACH 4A | 44 | 100, 208 | 44, 48, 100, 144 | 256 | 144, 256, 388 | 100 |
| ispLSI 5000V | - | 208 | - | 272, 388 | 208 | - |
| ispLSI 2000E | 44 | 128 | 44, 48, 100, 128, 176 | - | - | - |
| ispLSI 2000VE | 44 | 160 | 44, 48, 100, 128, 176 | - | 144, 208 | 49, 100 |
| ispLSI 2000VL | 44 | 160 | 44, 48, 100, 128, 176 | - | 144, 208 | 49, 100 |
| ispLSI 8000/V | - | - | - | 272, 432, 492 | - | - |
| ispGDX/V | - | 160, 208 | 100, 176 | 272 | 208, 388 | - |

# ispDesignEXPERT™

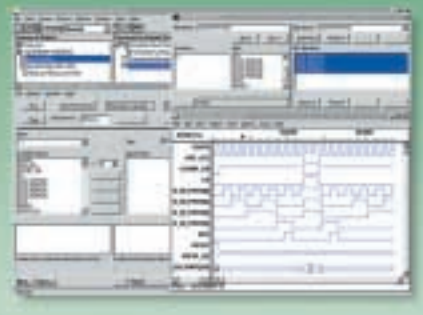
***Lattice's ispDesignEXPERT** is a fourth generation logic compiler supporting ispLSI, ispMACH, MACH, GAL, and PAL design. We have teamed with leaders in Third Party Synthesis and Simulation software, such as Exemplar Logic, Model Technology, Synopsys, Synplicity, and Innoveda (formerly Viewlogic Systems), to provide the very best in design entry, verification, and implementation tools, making design with Lattice programmable devices easy and efficient.*

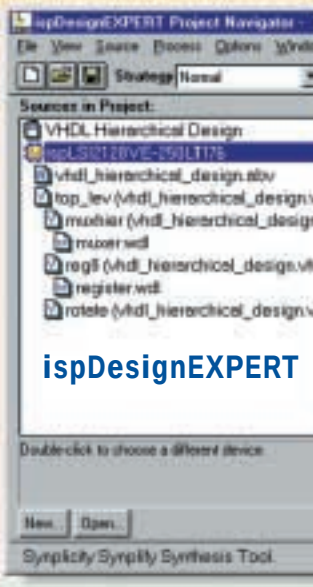
**HDL, Schematic, and ABEL Entry**

VHDL and Verilog Synthesis
- Exemplar Logic
- Synopsys
- Synplicity

**RTL & Timing Simulation**

RTL and Timing Simulation
- Model Technology
- Innoveda
- Lattice






## Complete Third Party Support

| | Synthesis | Schematic | Compiler | Simulation | PC | UNIX | ispLSI | ispMACH/MACH |
|---|---|---|---|---|---|---|---|---|
| Aldec | ● | ● | | ● | ● | | ● | |
| Cadence | ● | ● | | ● | | ● | ● | ● |
| Exemplar Logic | ● | | | | ● | ● | ● | ● |
| Mentor Graphics | ● | ● | | ● | | ● | ● | ● |
| Model Technology | | | | ● | ● | ● | ● | ● |
| OrCAD (Cadence) | ● | ● | ● | ● | ● | | ● | ● |
| Synopsys | ● | | | ● | | ● | ● | ● |
| Synplicity | ● | | | | ● | ● | ● | ● |
| Veribest (Mentor Graphics) | ● | ● | | ● | ● | | ● | |
| Innoveda | ● | ● | ● | ● | ● | ● | ● | ● |
| OVI Compliant Verilog | | | | ● | ● | ● | ● | ● |
| VITAL Compliant VHDL | | | | ● | ● | ● | ● | ● |

## ispDesignEXPERT Products

| | Macrocell | Support Level | Exemplar Leonardo Spectrum | Synplicity Synplify | Synopsys FPGA Express | Viewlogic Workview Office | Model Tech ModelSIM | License Type |
|---|---|---|---|---|---|---|---|---|
| **ispDesignEXPERT–HDL (Base)** | ≤600 | | ● | ● | | | ● | Node Locked |
| **ispDesignEXPERT–HDL (Advanced)** | ALL | | ● | ● | | | ● | Node Locked |
| **ispDesignEXPERT–Viewlogic (Base)** | ≤600 | | | | ● | ● | | Node Locked |
| **ispDesignEXPERT–Viewlogic (Advanced)** | ALL | | | | ● | ● | | Node Locked |
| **ispDesignEXPERT–Exemplar (Advanced)** | ALL | | ● | | | | ● | Floating |
| **ispDesignEXPERT (Starter)** | ≤600 | | | ● | | | | Node Locked |
| **ispDesignEXPERT (Advanced)** | ALL | | | | | | | Floating |
| **UNIX Design Tools** | ALL | | | | | | | Floating |

exemplar

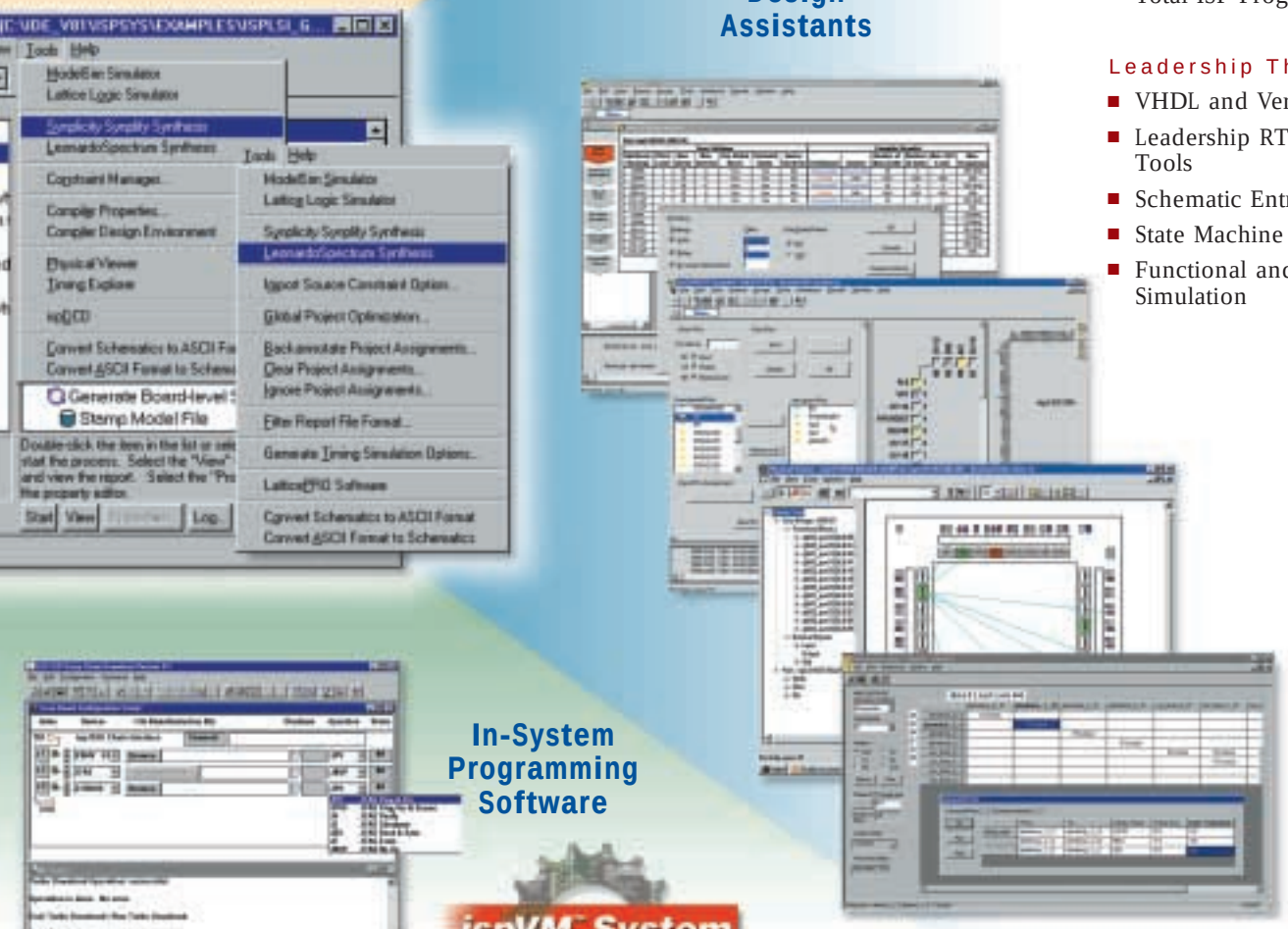
SYNOPSYS

INNOVEDA.

Model Technology

Synplicity


## Design Assistants



## In-System Programming Software




### ispDesignEXPERT Key Features

- Easy to Learn and Use
- Design Support for All Lattice Devices
- HDL Optimized Logic Compiler
- Lattice Schematic Tools
- ABEL-HDL Entry
- Advanced Design Assistant Tools
  - Performance Analyst™ and ispTA™
  - Explore Tool
  - Pin Editor
  - Physical Viewer
  - ispANALYZER™
- Lattice Functional and Timing Simulator
- Total ISP Programming Tools

### Leadership Third Party Tools

- VHDL and Verilog Synthesis
- Leadership RTL Simulation Tools
- Schematic Entry
- State Machine Entry
- Functional and Timing Simulation

# ispGDX Design & ISP Programming

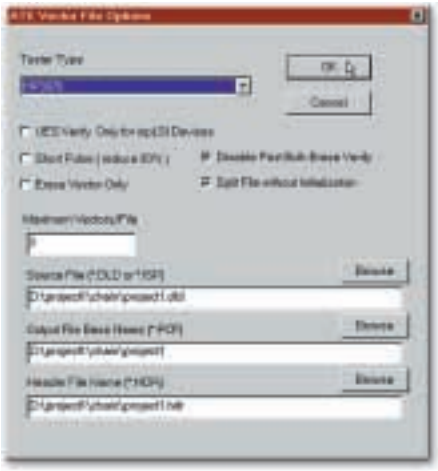
## ispGDX Development System

ispGDX Development System

***Lattice's ispGDX Development System*** *is a self contained design tool for ispGDX/V device design. Using a simple description language, designers can create complex interconnect designs quickly and easily.*

### Key Features

- Self Contained Design Tool Supporting ispGDX/V Device Design
- Simple Language-Based Design Entry with Syntax Checking
- Built-In Text Editor
- Detailed Timing Reports and On-line Help
- VHDL and Verilog Design and Synthesis from Leading CAE Vendors
- Interfaces to Industry Standard Simulators for Timing Verification
- Windows-based and Unix versions available



## ISP Programming Software

***Lattice*** *has the industry's only TOTAL ISP solution, providing a powerful variety of alternatives for in-system, embedded, ATE, parallel, and mixed-chain multi-vendor programming.*

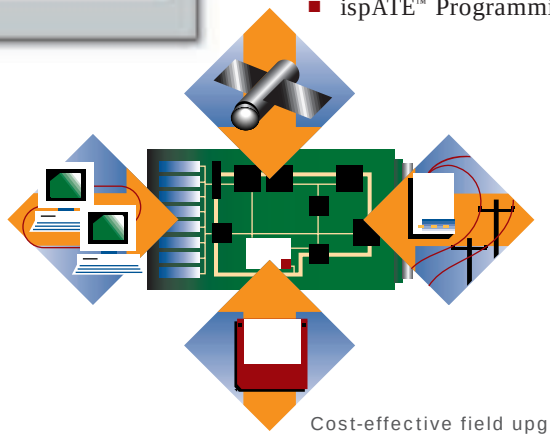
Teradyne's Z1890 Board Tester

### ispVM System

- LatticePRO™
- ISP Daisy Chain Download
- ispVM™ Download
- ispATE™ Programming

### Key Features

- Parallel/Turbo ispDOWNLOAD™
- Mixed Chain Programming
- Multi-Vendor Programming
- SVF File Translator
- User Electronic Signature (UES) Programming
- Programming Vector Support for Genrad, Teradyne, HP, Marconi and Other ATE Equipment Programming
- Embedded Programming Source Code



Cost-effective field upgrades are now possible with Lattice ISP products

# Lattice Delivers an Expanding Universe of In-System Programmable Solutions!

***Lattice*** *continues to redefine the concept of In-System Programmability with a unique portfolio of digital and analog products. Numerous vendors tout their product plans, but none can match the breadth of products and knowledge offered today by Lattice.*


- The Most Comprehensive ISP Product Portfolio Including Digital (ispLSI, ispMACH, ispGAL), Analog (ispPAC) and Signal Switching (ispGDX/V) Devices
  - Broadest Boundary Scan Testable and ISP Product Portfolio of Any PLD Vendor
- Industry's Broadest Portfolio of 3.3V ISP Devices
- Fastest Device Programming Times
  - Saves Time and Money
  - Turbo Programming - Dozens of CPLDs Programmed Simultaneously
- Broadest ISP Programming Tool Portfolio with ispVM System
- Embedded Programming
  - Source Code and Utilities to Embed ISP Within Their System

With Lattice's all-encompassing ISP solution, users are provided support throughout the lifecycle of their end-products. From product concept through field repairs and upgrades, Lattice ISP users are able to reduced costs and extend overall system lifetimes.

- Design
  - Faster Time-to-Market
  - Simplified System Prototyping
  - Improved Device and Board Level Testability
- Manufacturing
  - Streamlined Process Flows
  - Substantial Inventory Reduction
  - Lower Procurement Costs
  - Improved System Quality and Reliability
- Field Service
  - Easy Field Configuration or Customization
  - Cost Effective Remote Upgrade and Repair.

Lattice has been the ISP leader since its inception, by consistently providing the tools and devices necessary to meet every programmable logic need. When you think ISP, think Lattice. After all, ISP ***is*** Lattice!

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September 2000 Order #: I0107A