TN07001

USB design guideline

Rev. 01 — 09 May 2007 **Technical note**

1. Introduction

The layout on the PCB becomes more and more critical for a correct working of the High speed USB.
This document provides you a USB design checklist to help you to design a PCB with an optimal working USB interface with one of our microcontrollers
It does not provide you detailed information about each item. On the internet you find more information about the subject of designing a good working PCB.

2. Check list

3.1 USB design

Check	Item	Description
	1	Place the High-speed USB host controller and major components on the PCB first
	2	Rout high-speed signals (fi. clock) and high-speed USB differential pair first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB differential pair and any connector leaving the board
	3	Route high-speed USB signals on the bottom
	4	Route high-speed USB signals with a minimum of vias and corners to minimize reflection and impedance changes
	5	Use two 45 dgr. trance angles instead of one 90 dgr. angle
	6	Do not route USB traces under crystals, oscillators, magnetic devices or IC's that use or duplicate clocks
	7	Stubs on high speed USB traces (f.i. pull up resistors) should be avoided to minimize reflections and signal quality. When unavoidable they should not be grater than 200 mils.
	8	Routes all traces over continuous planes (VCC or GND) with no interruptions.
	9	Rout USB traces in pairs
	10	Keep high-speed USB signals away from external memory control signals.
	11	Keep the USB traces at least 20 times (height above the plane) from the edge of the pl

3.2 Trace spacing

Check	Item	Description
	1	Maintain parallelism between USB differential signals with trace distance needed for 90 ohm differential impedance. In general is the distance the same as the trace width.
	2	Verify the trace distance and the trace width on specific board . it should result in 90 ohms differential impedance
	3	Minimize the length that high-speed clock signals etc are in parallel with the USB signals. The minimum distance should be 50 mils.
	4	Use minimal 20 mil spacing between high-speed USB signal pairs and other signal traces.

3.3 High speed USB termination

Check	Item	Description
	1	The external termination resistors of the host controller should be in less than 200 mils from the HS output pins of the controller. (When controller is using external termination resistors)
	2	The pull down resistor should be between the termination resistor and the USB connector pins for downstream ports when pulldown is not integrated in the controller.
	3	Common mode choke should be placed close to the USB connector pins when EMI tests cannot be passed.

3.4 High speed USB trace length

Check	Item	Description
	1	The signal traces should be trace length matched.

3.5 Plane splits, voids and cut-outs (anti etches)

Check	Item	Description
	1	Traces should not cross Cut-outs. It increases the return path.
	2	No high-speed USB traces should be routed within 25 mils of any plane splits

3.6 Component placement

Check	Item	Description
	1	Locate high current devices near the source of power and away from any connector leaving the PCB. This reduces the length of return current travels and the coupling of traces that leave the PCB.
	2	Keep crystals, resonators, clock buffers away from high speed USB traces, I/O ports, PCB edges, power connectors, plane splits and mounting holes.
	3	Position crystals, resonators and oscillators so that they lie flat against the PCB. Add a ground pad with the same or larger footprint under the crystal etc connected with multiple vias to the ground plane.

3.7 High speed USB device

Check	Item	Description
	1	Place the Vbus bypass capacitance, CM choke and ESD suppression components as close as possible to the connector pins
	2	

3. Reference

- Internal USB course Nov 2006
- “High Speed USB Platform Design Guidelines” Rev.1.0 from Intel Corporation

4. History

Revision history

Rev	Date	Description
01	20070509	Final version