Reference Design for MIPS32® M14K™ Cores Application Note

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1 Introduction

The MIPS32® M14K™ Processor Core is cache-less and instead uses a SRAM-style bus that may be configured with either a Dual Memory Interface or a Unified Memory Interface. The Dual Memory Interface has separate instruction (ISRAM) and data (DSRAM) memory interfaces, and provides a redirection mechanism that permits D-side references to be handled by the I-side. The Unified Memory Interface has a single memory interface that shares both data and instructions.

This application note will introduce you to working with the higher performance Dual Memory Interface (ISRAM and DSRAM) with an optimized interface for flash memory and native AMBA®-3 AHB-Lite Bus Interface Unit. Source code and scripts accompany this application note that demonstrates how to build and debug an application in ISRAM/DSRAM. Target platforms include the CASim™ Cycle Accurate Simulator and the SEAD™-3/YAMON™ hardware platform.

2 Programming the m4k_sram_dual_switch*.v

This section discusses programming the `m4k_sram_dual_switch.v` (for SRAM interface) and `m4k_sram_dual_switch_ahb.v` (for `AHB-Lite` bus interface) customer example modules. These files are located in the `$MIPS_PROJECT/proc/design/rtl` directory of the M14K deliverable, and they may be modified by the customer to add application-specific functionality. All SEAD-3 hardware implementations include the deliverable version of the `m4k_sram_dual_switch_ahb.v` module. A block diagram of the system interface for the `m4k_sram_dual_switch.v` or `m4k_sram_dual_switch_ahb.v` modules is shown in Figure 1.

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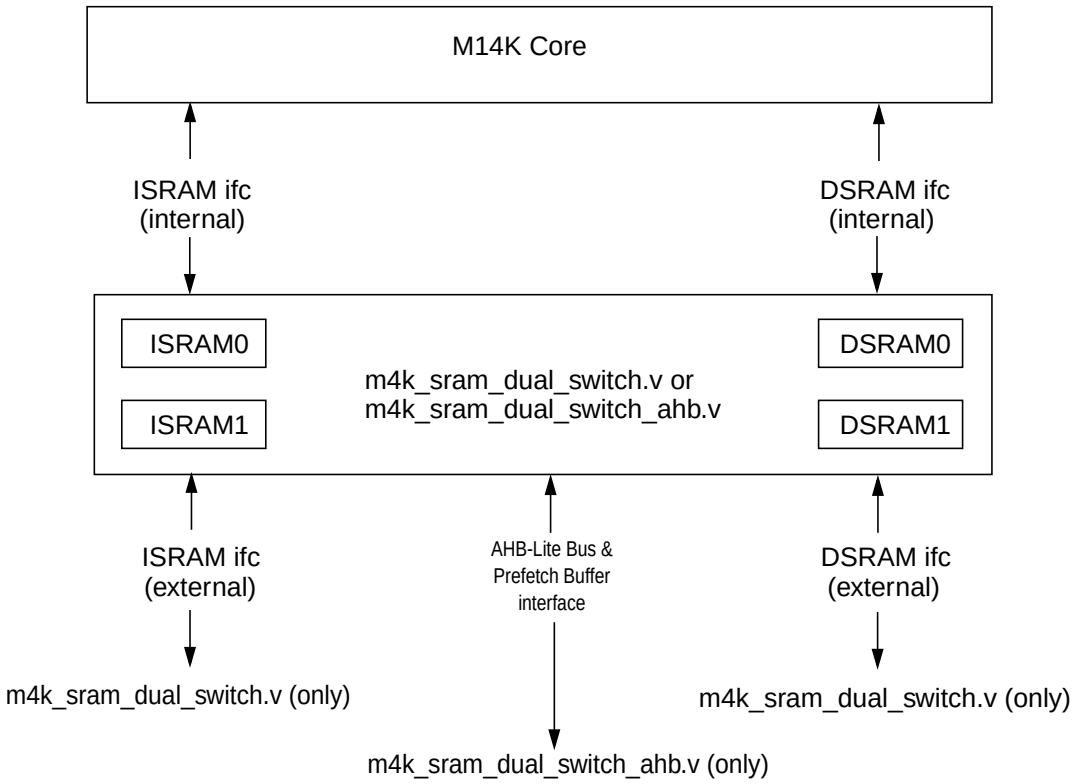
Figure 1 SRAM/DSRAM Interface Block Diagram



2.1 Theory of Operation

Following reset, the ISRAM and DSRAM in the `m4k_sram_dual_switch*.v` module are disabled, and therefore all memory operations from the core bypass the ISRAM, DSRAM, and FLASH interfaces and go through the AHB-lite interface. The `m4k_sram_dual_switch_ahb.v` module merges the separate (external) ISRAM & DSRAM and Flash interfaces into the AHB-lite interface bus that is connected to the system memory controller. Software can enable or disable the ISRAM & DSRAM & FLASH interface and configure their physical base address decoding. The base addresses of the ISRAM & DSRAM & FLASH interface may be initialized at any physical address as long as it's aligned with the physical size of the RAM, i.e., 16KB, 32KB, etc. When the DSRAM is enabled, all CPU loads and stores within its configured address range go to the DSRAM. When the ISRAM or FLASH interface is enabled, all CPU instruction fetches within its configured address range come from the ISRAM or FLASH interface respectively. Also, CPU loads and stores can go to the ISRAM or FLASH interface if REDIRECTION is enabled. Memory references outside the configured address ranges of ISRAM and DSRAM and FLASH interface will be forwarded to the system memory controller via the AHB-lite interface bus.

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2.2 Control Register Summary

Table 1 lists the control registers in order of physical address.

Table 1 Control Registers

Register Address (Physical)	Register Name	Function
0x1e000000	*ISRAM0 Configuration*	ISRAM0 Control
0x1e000010	*ISRAM0 Mask*	ISRAM0 Size and Alignment
0x1e000004	*ISRAM1 Configuration*	ISRAM1 Control
0x1e000014	*ISRAM1 Mask*	ISRAM1 Size and Alignment
0x1e000008	*Prefetch-Buffer Configuration*	Prefetch-Buffer Control
0x1e000018	*Prefetch-Buffer Mask*	Prefetch-Buffer Size and Alignment
0x1e000020	*DSRAM0 Configuration*	DSRAM0 Control
0x1e000030	*DSRAM0 Mask*	DSRAM0 Size and Alignment
0x1e000024	*DSRAM1 Configuration*	DSRAM1 Control
0x1e000034	*DSRAM1 Mask*	DSRAM1 Size and Alignment

2.3 ISRAM0 Configuration Register (0x1e000000)

The ISRAM0 is controlled by the *ISRAM0 Configuration* register located at physical address 0x1e000000. It contains a 22-bit field that sets the I-side physical base address. This is the physical starting address at which the ISRAM0 will be decoded, and it must be loaded with an address that is aligned with the block size of the ISRAM0. The *Enable* (*E*) bit enables the decoding of CPU fetches from ISRAM0. The *Redirection* (*r*) bit enables CPU loads and stores to ISRAM0, so instructions may be copied to it. Figure 2 shows the format of the *ISRAM0 Configuration* register; Table 2 describes the *ISRAM0 Configuration* register fields.

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Figure 2 ISRAM0 Configuration Register Format

Table 2 ISRAM0 Configuration Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
I-Side Base Address	31:10	I-side physical base address (must be aligned with block size).	R/W	0
0	9:2	Must be written with zero; returns zero on read.	0	0
R	1	Redirect D-side if hitting I-side address range (and not hitting D-side address range).	R/W	
E	0	Enable the ISRAM0.	R/W	0

2.4 ISRAM1 Configuration Register (0x1e000004)

The ISRAM1 is controlled by the *ISRAM1 Configuration* register located at physical address 0x1e000004. It contains a 22-bit field that sets the I-side physical base address. This is the physical starting address at which the ISRAM1 will be decoded, and it must be loaded with an address that is aligned with the block size of the ISRAM1. The *Enable* (*E*) bit enables the decoding of CPU fetches from ISRAM1. The *Redirection* (*r*) bit enables CPU loads and stores to ISRAM1, so instructions may be copied to it. Figure 2 shows the format of the *ISRAM1 Configuration* register; Table 2 describes the *ISRAM1 Configuration* register fields.

Figure 3 ISRAM1 Configuration Register Format

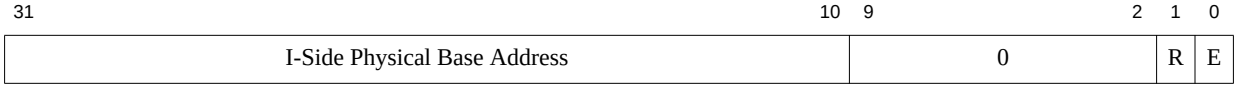

Table 3 ISRAM1 Configuration Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
I-Side Base Address	31:10	I-side physical base address (must be aligned with block size).	R/W	0
0	9:2	Must be written with zero; returns zero on read.	0	0
R	1	Redirect D-side if hitting I-side address range (and not hitting D-side address range).	R/W	
E	0	Enable the ISRAM1.	R/W	0

2.5 ISRAM0 Mask Register (0x1e000010)

The *ISRAM0 Mask* register is located at physical address 0x1e000010. It contains a 22-bit read-only mask used by software to mask and align the I-Side Address in the *ISRAM0 Configuration* register.

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Figure 4 shows the format of the *ISRAM0 Mask* register; Table 4 describes the *ISRAM0 Mask* register fields.

Figure 4 ISRAM0 Mask Register Format

Table 4 ISRAM0 Mask Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
I-Side Address Mask	31:10	I-side address mask 32K=0xffff8000, 64K=0xffff0000.	R	0
0	9:0	Returns zero on read.	0	0

2.6 ISRAM1 Mask Register (0x1e000010)

The *ISRAM1 Mask* register is located at physical address 0x1e000010. It contains a 22-bit read-only mask used by software to mask and align the I-Side Address in the *ISRAM1 Configuration* register.

Figure 4 shows the format of the *ISRAM1 Mask* register; Table 4 describes the *ISRAM1 Mask* register fields.

Figure 5 ISRAM1 Mask Register Format

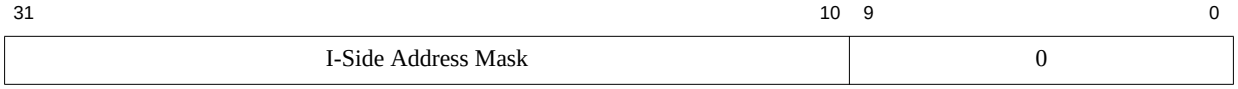

Table 5 ISRAM1 Mask Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
I-Side Address Mask	31:10	I-side address mask 32K=0xffff8000, 64K=0xffff0000.	R	0
0	9:0	Returns zero on read.	0	0

2.7 DSRAM0 Configuration Register (0x1e000020)

The DSRAM0 is controlled by the *DSRAM0 Configuration* register located at physical address 0x1e000020. It contains a 22-bit field for setting the D-side physical base address. This is the physical starting address at which the DSRAM0 will be decoded, and it must be loaded with an address that is aligned with the block size of the DSRAM0. The *Enable* (*E*) bit enables the decoding of CPU loads and stores to DSRAM0. The read-only *Redirection* (*R*) bit indicates a D-side access has been redirected to I-side.

Figure 6 shows the format of the *DSRAM0 Configuration* register; Table 6 describes the *DSRAM0 Configuration* register fields.

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Figure 6 DSRAM0 Configuration Register Format

Table 6 DSRAM0 Configuration Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
I-Side Base Address	31:10	I-side physical base address (must be aligned with block size),	R/W	0
0	9:2	Must be written with zero; returns zero on read.	0	0
R	1	Redirect D-side if NOT hitting D-side address range (if only access to external world from I-side).	R	0
E	0	Enable the DSRAM0.	R/W	0

2.8 DSRAM1 Configuration Register (0x1e000024)

The DSRAM1 is controlled by the *DSRAM1 Configuration* register located at physical address 0x1e000024. It contains a 22-bit field for setting the D-side physical base address. This is the physical starting address at which the DSRAM1 will be decoded, and it must be loaded with an address that is aligned with the block size of the DSRAM1. The *Enable* (*E*) bit enables the decoding of CPU loads and stores to DSRAM1. The read-only *Redirection* (*R*) bit indicates a D-side access has been redirected to I-side.

Figure 6 shows the format of the *DSRAM1 Configuration* register; Table 6 describes the *DSRAM1 Configuration* register fields.

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Figure 7 DSRAM1 Configuration Register Format

Table 7 DSRAM1 Configuration Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
I-Side Base Address	31:10	I-side physical base address (must be aligned with block size),	R/W	0
0	9:2	Must be written with zero; returns zero on read.	0	0
R	1	Redirect D-side if NOT hitting D-side address range (if only access to external world from I-side).	R	0
E	0	Enable the DSRAM1.	R/W	0

2.9 DSRAM0 Mask Register (0x1e000030)

The *DSRAM0 Mask* register is located at physical address 0x1e000030. It contains a 22-bit read-only mask used by software to mask and align the D-Side Address in the *DSRAM0 Configuration* register.

Figure 8 shows the format of the *DSRAM0 Mask* register; Table 8 describes the *DSRAM0 Mask* register fields.

Figure 8 DSRAM0 Mask Register Format

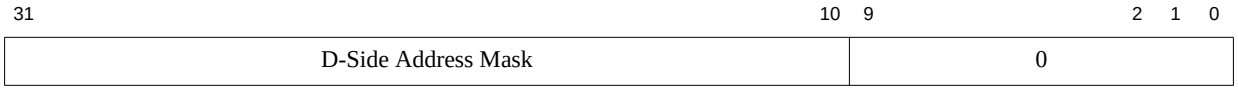

Table 8 DSRAM0 Mask Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
D-Side Address Mask	31:10	D-side address mask 32K=0xffff8000, 64K=0xffff0000.	R	0
0	9:0	Returns zero on read.	0	0

2.10 DSRAM1 Mask Register (0x1e000034)

The *DSRAM1 Mask* register is located at physical address 0x1e000034. It contains a 22-bit read-only mask used by software to mask and align the D-Side Address in the *DSRAM1 Configuration* register.

Figure 8 shows the format of the *DSRAM1 Mask* register; Table 8 describes the *DSRAM1 Mask* register fields.

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Figure 9 DSRAM1 Mask Register Format

Table 9 DSRAM1 Mask Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
D-Side Address Mask	31:10	D-side address mask 32K=0xffff8000, 64K=0xffff0000.	R	0
0	9:0	Returns zero on read.	0	0

2.11 Prefetch-Buffer Configuration Register (0x1e000008)

The Prefetch-Buffer is controlled by the *Prefetch-Buffer Configuration* register located at physical address 0x1e000008. It contains a 22-bit field for setting the I-side physical base address. This is the physical starting address at which the Prefetch-Buffer will be decoded, and it must be loaded with an address that is aligned with the block size of the Prefetch-Buffer. The *Enable* (*E*) bit enables the decoding of CPU fetches from Prefetch-Buffer. The *Redirection* (*r*) bit enables CPU loads and stores to Prefetch-Buffer so instructions may be copied to it. Figure 10 shows the format of the *Prefetch-Buffer Configuration* register; Table 10 describes the *Prefetch-Buffer Configuration* register fields.

Figure 10 IPrefetch-Buffer Configuration Register Format

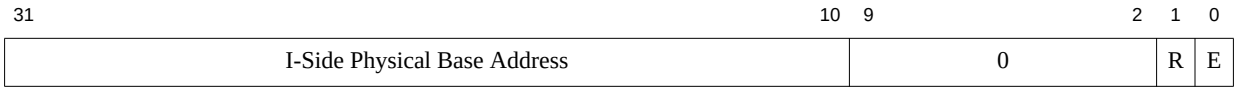

Table 10 Prefetch-Buffer Configuration Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
I-Side Base Address	31:10	I-side physical base address (must be aligned with block size).	R/W	0
0	9:2	Must be written with zero; returns zero on read.	0	0
R	1	Redirect D-side if hitting I-side address range (and not hitting D-side address range).	R/W	
E	0	Enable the Prefetch-Buffer.	R/W	0

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2.12 Prefetch-Buffer Mask Register (0x1e000018)

The *Prefetch-Buffer Mask* register is located at physical address 0x1e000018. It contains a 22-bit read-only mask used by software to mask and align the D-Side Address in the *Prefetch-Buffer Configuration* register.

Figure 11 shows the format of the *Prefetch-Buffer Mask* register; Table 11 describes the *Prefetch-Buffer Mask* register fields.

Figure 11 Prefetch-Buffer Mask Register Format

Table 11 Prefetch-Buffer Mask Register Field Descriptions

Fields		Description	Read / Write	Reset State
Name	Bits			
D-Side Address Mask	31:10	D-side address mask 32K=0xffff8000, 64K=0xffff0000.	R	0
0	9:0	Returns zero on read.	0	0

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3 References

This appendix lists other documents available from MIPS Technologies, Inc. that are referenced elsewhere in this document. These documents may be included in the `$MIPS_HOME/$MIPS_CORE/doc` area of a typical *Core-Name* soft or hard core release, or in some cases may be available on the MIPS web site, http://www.mips.com.

1. CASim™ Cycle Accurate Simulator for the MIPS32® M14K™ Core User's Guide
   MIPS Document: MD00697

1. CASim™ Cycle Accurate Simulator for the MIPS32® M14K™ Core Release Notes
   MIPS Document: MD00713

2. MIPS32® M14K™ Processor Core Datasheet
   MIPS Document: MD00666

3. MIPS32® M14K™ Processor Core Integrator’s Guide
   MIPS Document: MD00667

4. MIPS32® M14K™ Processor Core Software Users Manual
   MIPS Document: MD00668

5. SEAD™-3 Board Users Manual
   MIPS Document: MD00682

6. SEAD™-3 Board Getting Started
   MIPS Document: MD00687

7. YAMON™ Users Manual
   MIPS Document: MD00008

8. The GNU linker Manual “Using ld, version 2”

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4 Revision History

Change bars (vertical lines) in the margins of this document indicate significant changes in the document since its last release. Change bars are removed for changes that are more than one revision old.

This document may refer to Architecture specifications (for example, instruction set descriptions and EJTAG register definitions), and change bars in these sections indicate changes since the previous version of the relevant Architecture document.

Revision	Date	Description
1.00	March 25, 2010	Initial external release.

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