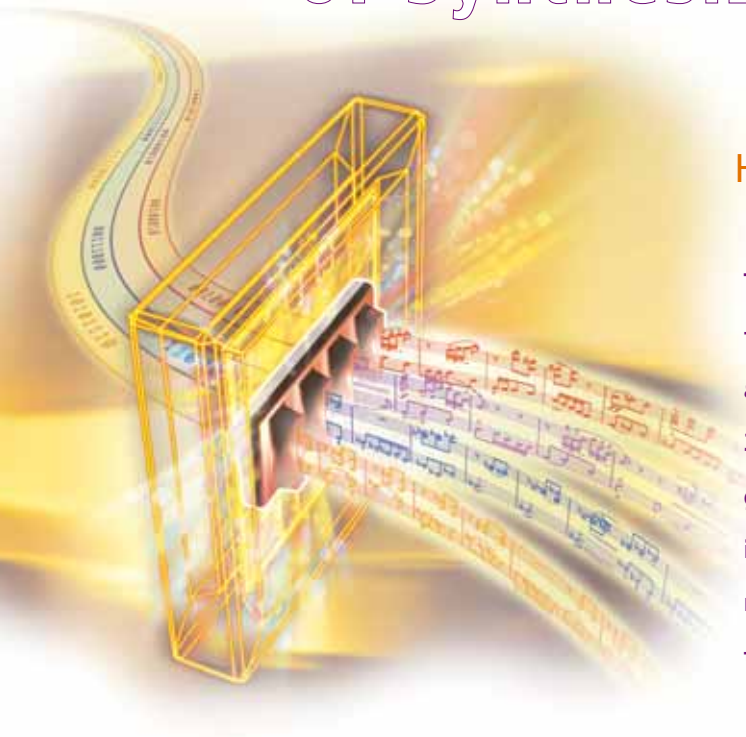
The MIPS32® 34K™ Family

of Synthesizable Processor Cores



The Multi-threading Solution for High-Performance, Cost-Sensitive Applications

The MIPS32® 34K™ core family is a revolutionary implementation of the MIPS® MT ASE designed to exploit multi-threading in embedded applications. Processing multiple software threads in parallel, 34K cores mask the effect of memory latency to deliver significant gains in system performance and cost savings, with a very modest increase in die size. The 34K core family also meets the real-time requirements of embedded applications by giving users the ability to allocate dedicated processing bandwidth to real-time tasks.

DOING MORE FOR LESS

Internal benchmarks indicate that the 34K™ core running two threads achieved a 60 percent speedup over a single-threaded processor with only a 14 percent increase in die size.

Lower System Costs

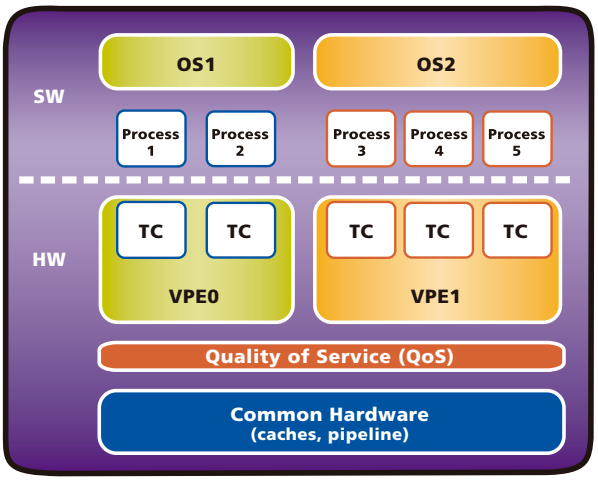
Higher application throughput enables several functions to be consolidated onto a single 34K core while preserving existing investments in software.

Design Flexibility

The 34K core can be configured with a maximum of two VPEs and five TCs for ultimate design flexibility. Depending on the application, the 34K core can implement symmetric multiprocessing across two VPEs. Alternatively, each VPE can run a separate operating system.

Faster Time-to-Market

A rich environment of third-party tools and software supports the 34K core family.



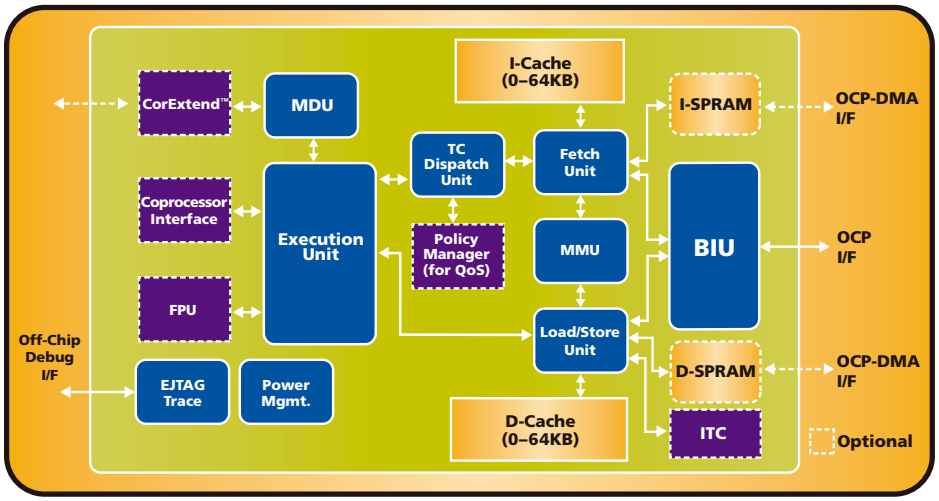
MIPS32® 34K™ Core — Simplified Overview

TC: Thread Context — represents the user-state of the MIPS32® architecture.

VPE: Virtual Processing Element — represents the OS-only visible state of the MIPS32 architecture.

MIPS32® 34K™ Core Family

The Synthesizable Multi-threading Solution for High-Performance, Cost-Sensitive Applications



- **34Kc™ Core:** The base core implementing the MIPS® MT and DSP ASEs.
- **34Kf™ Core:** Adds hardware floating-point support that is fully compliant with the IEEE 754 specification.
- **34K™ Pro Cores:** 34Kc Pro and 34Kf Pro cores feature the CorExtend™ capability.

SPECIFICATIONS

Product	34Kc™
Process	90nm G
Frequency	500 MHz (worst case)
Core Size	2.1 mm² (core only, extracted from full layout GDSII database)
Power Consumption	0.56 mW/MHz @ 1.0V (core only)

Note:
Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries.

Configuration: Two VPEs and four TCs, 32K/32K caches.

FEATURES

32-bit MIPS32® Architecture
- 9-stage pipeline
- 32-bit address paths
- 64-bit data paths to caches and external interface

MIPS® MT Application Specific Extension (ASE)
- Support for up to 2 VPEs and 5 TCs
- Policy Manager for QoS scheduling
- Inter-Thread Communication memory for efficient message and data transfer between TCs

MIPS DSP ASE
- 3 additional pairs of accumulator registers
- Fractional data types (Q15, Q31)
- Saturating arithmetic
- SIMD instructions operate on 2x16b or 4x8b simultaneously

Programmable Memory Management Unit
- 16/32/64 dual-entry JTLB per VPE
- JTLBs are sharable under software control
- 4–8 entry MT-optimized ITLB; 8-entry DTLB
- Optional simple Fixed Mapping Translation (FMT) mechanism

Programmable L1 Cache Sizes
- Individually configurable instruction and data caches, sizes of 0/8/16/32/64KB
- 4-way set associative
- Up to nine outstanding loads
- Write-back and write-through support
- Cache line locking support

Scratchpad RAM (SPRAM) support
- Separate RAMs for instruction and data
- Two 64-bit OCP interfaces for external DMA

Bus Interface Unit (BIU)
- OCP interface with 32-bit address and 64-bit data
- OCP interface runs at core/bus clock ratios of 1, 1.5, 2, 2.5, 3, 3.5, 4 or 5

Multiply/Divide Unit
- 32x32 multiply with a repeat rate of one per clock cycle

Coprocessor 2 Interface
- 64-bit interface to a user-designed coprocessor
- Optional thread support

CorExtend™
- Allows user to define and add instructions to the core at build time

Power Control
- Minimum frequency: 0 MHz
- Power-down mode (automatic and program-controlled)
- Software-controlled clock divider
- Extensive use of fine-grained clock gating

EJTAG Debug
- Support for single stepping
- Instruction address and data address/value breakpoints
- TAP controller is chainable for multi-CPU debug
- PC, data address and data value tracing with compression

MIPS16e™ Code Compression
- Reduces memory requirements by as much as 40 percent

MIPS TECHNOLOGIES

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MIPS Technologies, Inc.
1225 Charleston Road
Mountain View, CA 94043-1353
Phone: (650) 567-5000
Fax: (650) 567-5158

MIPS Technologies
Berghauser Strasse 62
42859 Remscheid
Germany
Phone: +49 2191 900 200
Fax: +49 2191 900 208

MIPS Technologies Japan
Landic Toranomon Building No.2
3-7-8 Toranomon, Minato-ku
Tokyo 105-0001 Japan
Phone: +81-3-5733-9541
Fax: +81-3-5733-9545

www.mips.com