# *Recommended JTAG Circuitry for Debug with Intel® Xscale™ Microarchitecture*

## Application Note

***June 2001***

Document Number: 273538-001

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# Revision History

| Date | Revision | Description |
|---|---|---|
| June 2001 | 001 | Initial release. |

# 1.0 Introduction

Certain restrictions exist in order to use JTAG based debuggers with the Intel® XScale™ microarchitecture (ARM* Architecture compliant). This is primarily due to the Tap Controller reset requirements of the Intel® 80200 processor with Intel® XScale™ microarchitecture and the reset requirements of specific JTAG debuggers. The following sections outline these requirements along with suggestions for circuitry to alleviate potential problems.

# 2.0 Requirements

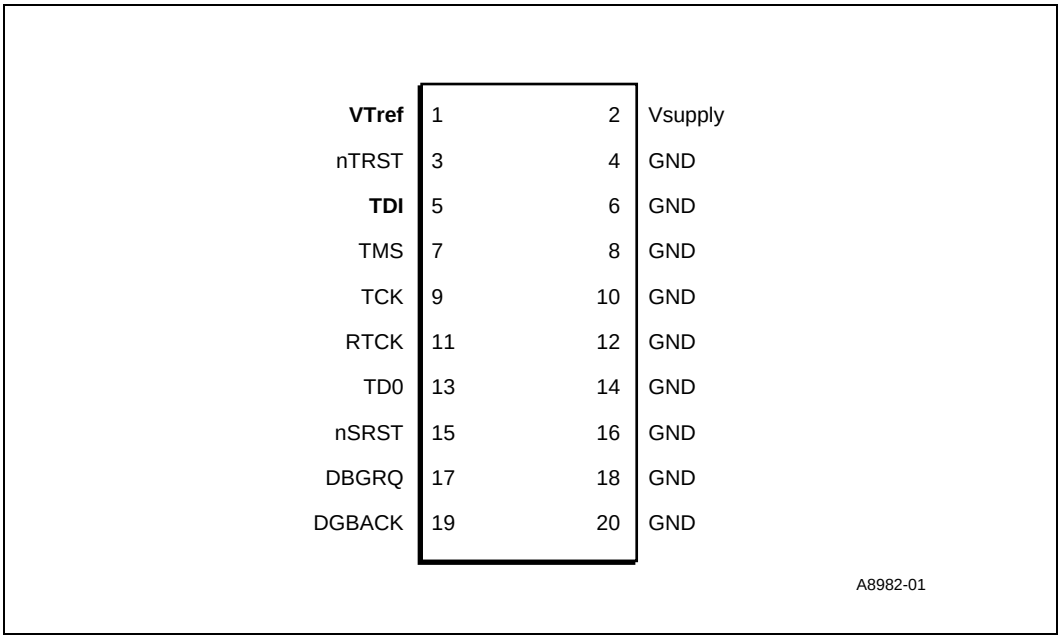
The Intel® 80200 processor with Intel® XScale™ microarchitecture, like many others, requires that nTRST (Tap Reset) is asserted low during power up for at least 32 core clock cycles. This is to ensure a fully initialized boundary scan chain. Failure to comply with this requirement may result in spurious behavior of the application.

The ARM∗ Multi-ICE∗ JTAG debugger requires that nTRST is always weakly pulled high. This requirement stems from the fact that the debugger can only assert nTRST (drive low). Both reset signals coming from the Multi-ICE (nTRST and nSRST) are open collector and must be weakly pulled high in order to avoid unintentional resets (System or TAP).

# 3.0 JTAG Signals / Header

Figure 1 is the pin definition (20-pin standard ARM connector) for JTAG (See specific Product Design Guide for part number information).

**Figure 1. JTAG Header**




The ARM Multi-ICE debugger along with the Macraigor Raven* and Wind River Systems* visionPROBE* / visionICE* utilize this connector. The main difference to be noted is the specific implementation of nTRST for each debugger. The Macraigor Raven implementation actively drives nTRST (high and low). The Wind River Systems visionPROBE / visionICE can configure nTRST active or open collector (only drive low). ARM Multi-ICE is configured as open collector only.

# 4.0 System Requirements

In order to successfully invoke a debug session, the JTAG debug unit must be able to control nTRST and nSRST independently. The nTRST signal allows the debugger to get the TAP controller in a known state. The nSRST signal allows the debugger to control system/processor reset in order to download the debug handler via the JTAG interface. See Figure 2, "Example JTAG Signals at Power-Up and Figure 3, "Example JTAG Signals at Debug Start-Up.

***Note:*** Figure 2 and Figure 3 are examples and do not reflect actual signal timings.

**Figure 2. Example JTAG Signals at Power-Up**

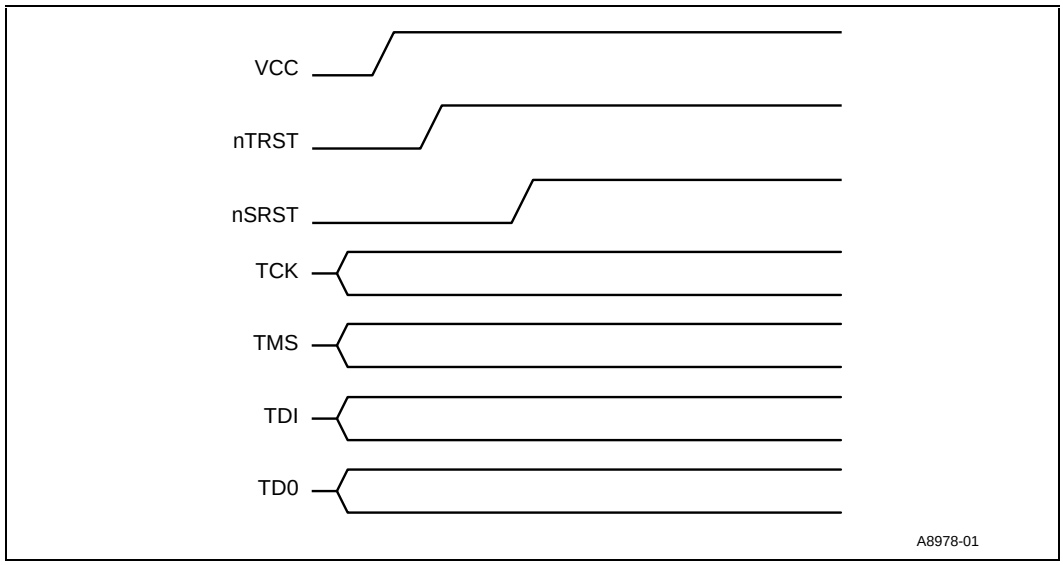
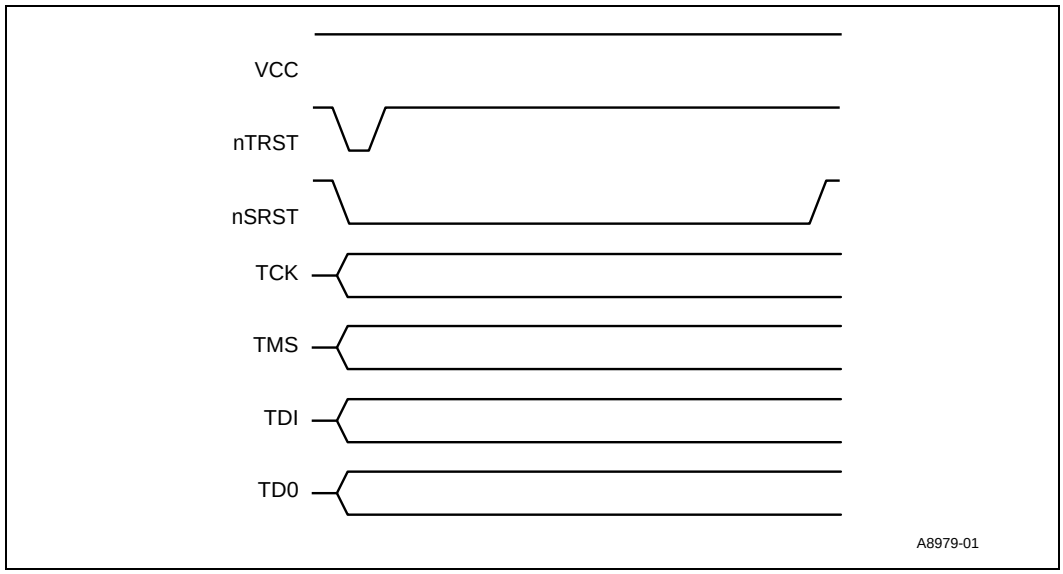



**Figure 3. Example JTAG Signals at Debug Start-Up**



# 5.0 Hardware Requirements

Due to the conflicting requirements of Multi-ICE and the Intel® 80200 processor, it is necessary to incorporate a circuit that can drive nTRST low at power up and weakly pull it high at all other times. This section details the circuits required for nTRST when using the Macraigor Raven, Wind River Systems visionPROBE / visionICE, and ARM Multi-ICE.

***Note:*** This section does not discuss circuitry needed for nSRST, due to varying system level requirements.

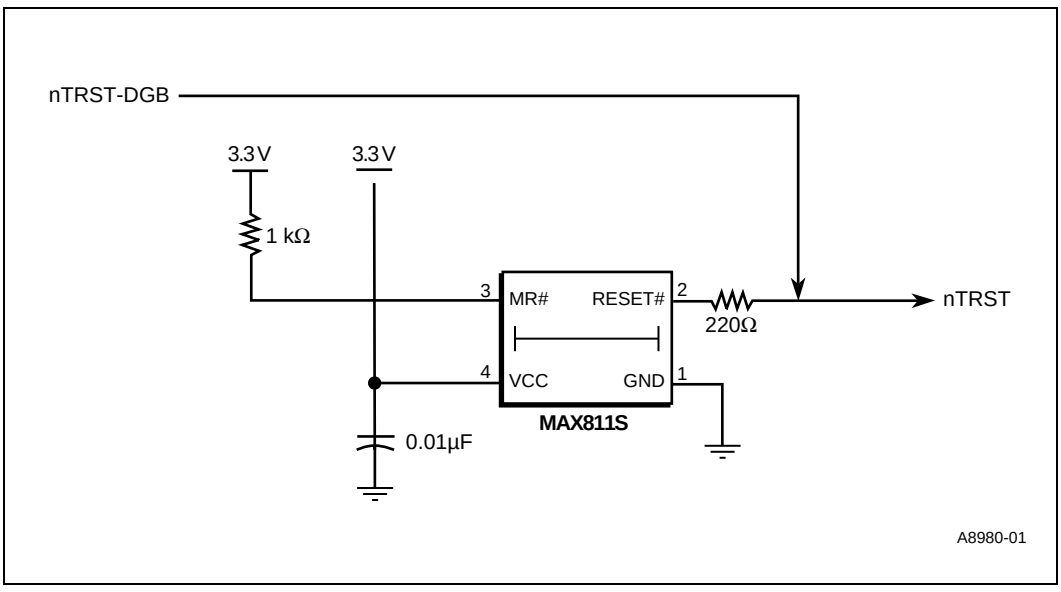
## 5.1 Macraigor Raven* and Wind River Systems visionPROBE* / visionICE*

Both the Macraigor Raven and Wind River Systems visionPROBE / visionICE (when configured as active) do not require any special power-up circuitry. Simply, the requirement is that nTRST is weakly pulled down at the processor. It is suggested that the value of the pull-down resistor is 10kΩ or greater. The value of this resistor should be confirmed with the JTAG debugger manufacturer to ensure optimal performance.

## 5.2 ARM* Multi-ICE*

The ARM Multi-ICE debugger requires special power-up circuitry due to the open collector implementation of the nTRST signal. This power-up circuit must ensure that nTRST is asserted (low) at power on and weakly pulled high thereafter. See Figure 4, “Example Power-Up Circuit for nTRST. This circuit is a universal solution and will work with other JTAG debug systems.

**Figure 4. Example Power-Up Circuit for nTRST**



# 6.0 References

1. *Multi-ICE System Design Considerations Application Note 72* (http://www.arm.com/)
2. *Intel® 80310 I/O Processor Chipset with Intel® XScale™ Microarchitecture Design Guide* (http://developer.intel.com/design/iio/docs/iop310.htm)
3. Intel® 80200 Processor Evaluation Platform Board Schematics (http://proto-cps.jf.intel.com/design/iio/docs/iop310.htm)
4. *Max811/812 Datasheet* (http://www.maxim-ic.com/)

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