# Fx™

## Fx™100100-5, Fx10050-5 Chipsets

### For DSLAMs, ONUs, OLTs, and Broadband Concentrators


### Target Markets

- Multi-tenant and Multi-Dwelling units (MxU)
- Fiber to the Basement/Building (FTTB)
- Fiber to the node (FTTN)
- Fiber to the Curb (FTTC)
- Fiber to the Premise (FTTP)
- Fiber to the Home (FTTH)

### Applications

- Fiber-fast Broadband, Peer to Peer Networking, Online Gaming/Hosting
- Triple play services
- IPTV (HDTV and SDTV)
- Voice over IP
- High-resolution Video Conferencing

### Features

- Eight-port BME – DSP Engine
- Four-port AFE
- Four-port IFE
- Two-port Line Driver with LNA
- iPOS – Firmware and API

### Development Tools

- Evaluation Systems
- Reference Designs
- Application Notes
- Complete Software Suite
- Bill of materials (BOM)

**The Fx™100100-5 and Fx10050-5 chipsets** are the industry's first IPTV-optimized multi-mode (VDSL2,VDSL, ADSL2+, ADSL2 and ADSL) solutions for central office (CO) equipment (DSLAMs,ONUs and other broadband concentrators). Both chipsets support all 8, 12 and 17 MHz profiles. The Fx100100-5 chipset additionally supports the 30 MHz profile. The chipsets also support the VDSL, ADSL2+, ADSL2 and ADSL standards.

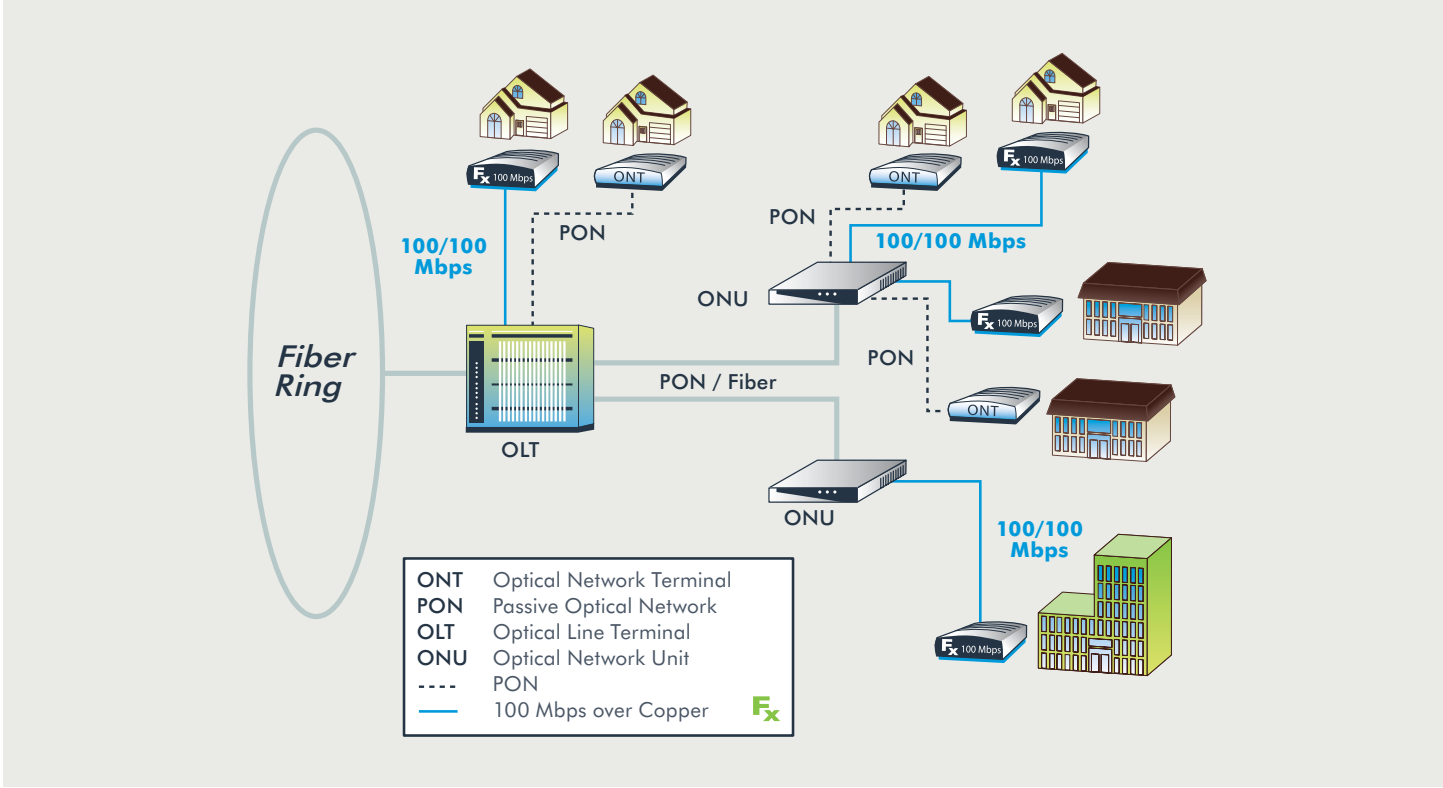
The rich set of features which were previously unavailable in such chipsets include: on-chip classification, queuing and scheduling for enhanced quality of service (QoS) in IPv4 and IPv6 networks, enhanced Impulse noise protection, and dual latency and dual interleaving over all network interfaces. Such features enable unsurpassed interactive broadband experience.

These high bandwidth, multi-port chipsets are powerful complements to fiber technology. Common attributes of both chipsets include: the industry's highest performance and density with the lowest power consumption, VDSL long range (VLR) capability with programmable U0, plug-and-play per-port multi-mode operation, integrated adaptive hybrid for best line impedance matching, full band plan configurability for worldwide applications and interoperability with deployed CPE. The Fx100100-5 and Fx10050-5 chipsets are 100% pin-compatible, which allows system vendors to develop a single platform for worldwide deployment and reduces their development costs and time to market.

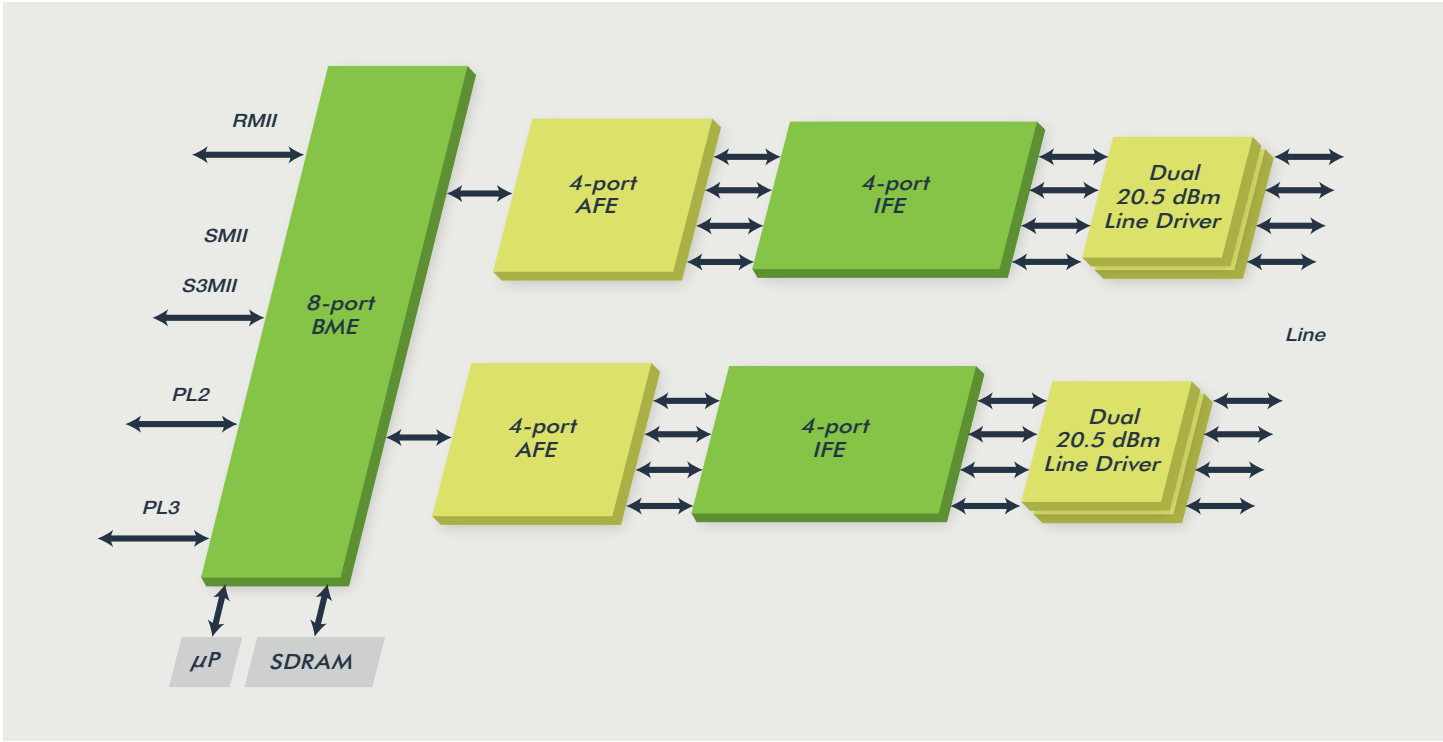
Both chipsets consist of an eight-port BME (DSP engine), a four-port analog front end (AFE), a four-port integrated front end (IFE), a two-port line driver with programmable 8.5 - 20.5 dBm drive and the Ikanos Programmable Operating System™ (iPOS).The iPOS consists of firmware and an OS-independent application programming interface (API) that enables easy integration into existing management software.

The Fx100100-5 and Fx10050-5 chipsets enable equipment vendors to develop a single system to deliver a full suite of revenue-generating interactive broadband services. The highly-integrated architecture enables the design of smaller, simpler, denser systems with fewer components. Carriers can now achieve their goal of delivering universal service at 100 Mbps while simultaneously future-proofing their networks.

## Central Office Equipment Diagram




## System Block Diagram

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## Key Features

- Supports mandatory and optional features of the VDSL2 standard
- Supports VDSL2 profiles
  - Fx100100-5 supports 8a/8b/8c/8d, 12a/12b, 17a and 30a
  - Fx10050-5 supports 8a/8b/8c/8d, 12a/12b and 17a
- Plug-and-play multi-mode (VDSL2,VDSL, ADSL2+, ADSL2 and ADSL) operation per port
- Feature set optimized for triple play and IPTV including:
  - Available on-chip classification, queuing and scheduling for enhanced quality of service
  - (QoS) for IPv4 and IPv6 networks
  - Support for dual latency, dual interleaving over xMII, PL2 and PL3 interfaces for interworking with low cost 10/100 Ethernet switch chips as well as high-performance network processors
  - Maximum interleaver and de-interleaver memory for impulse noise protection (INP)
  - Eraser detection and decoding for enhanced impulse noise protection
- Backward interoperable with deployed CPE
- Highly-integrated chipset consists of the following:
  - Eight-port BME (DSP Engine) – a single chip data pump that integrates a framer, deframer, FFT/IFFT engines, interleaver/ de-interleaver memory and network interfaces.
  - An embedded 200 MIPS processor performs control-plane and management functions for all ports. The BME is available in different versions to support different levels of QoS.
  - Four-port AFE integrates high performance converters (DAC and ADC)
  - Four-port IFE integrates the variable gain amplifier (VGA), programmable gain amplifier (PGA), and filters
  - Two-port line driver (HLD) with integrated low noise amplifier (LNA) enables adaptive hybrid for best line-impedance matching and supports programmable drive levels from 8.5 – 20.5 dBm
  - iPOS, which consists of firmware and OS-independent APIs that enable easy integration into existing management software
- Enhanced power savings modes: software can turn off quad ports in BME, and individual ports in the AFE, IFE, and HLD for maximum power savings
- Standards-compliant DMT line coding ensures spectral compatibility with POTS, ISDN, and DSL services per T1.417 standard
- Region-specific RFI notching
- IEEE 1149.1 compliant JTAG interface
- Industrial temperature range (-40 °C to +85 °C)



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