Fx™

Fx™100100S-5, Fx10050S-5 Chipsets

For Customer Premises Equipment

Target Markets

- Multi-tenant and Multi-dwelling units (MxU)
- Fiber to the Basement/Building (FTTB)
- Fiber to the Node (FTTN)
- Fiber to the Curb (FTTC)
- Fiber to the Premise (FTTP)
- Fiber to the Home (FTTH)

Applications

- Fiber-fast Broadband, Peer to Peer
- Networking,Online Gaming/Hosting
- Triple play services
- IPTV (HDTV and SDTV)
- Voice over IP
- High-resolution Video Conferencing

Solutions for High-Performance Modems, Routers, and Gateways

- Single-port data pump – DSP Engine
- Single-port IFE
- Single-port LD
- iPOS – firmware and API

Development Tools

- Evaluation Systems
- Reference Designs
- Application Notes
- Complete Software Suite
- Bill of Materials (BOM)

The Fx™100100S-5 and Fx10050S-5 chipsets are the industry's first IPTV-optimized VDSL2 and VDSL products for CPE modems and other subscriber located equipment. Both chipsets support all 8, 12 and 17 MHz profiles. The Fx100100S-5 chipset additionally supports the 30 MHz profile. The chipsets also support the VDSL standard.

The Fx100100S-5 and Fx10050S-5 chipsets have a rich feature set for IPTV and triple play. These include: on-chip classification, queuing and scheduling for enhanced Quality of service (QoS) in IPv4 and IPv6 networks, enhanced impulse noise protection, and dual latency and dual interleaving over all network interfaces.

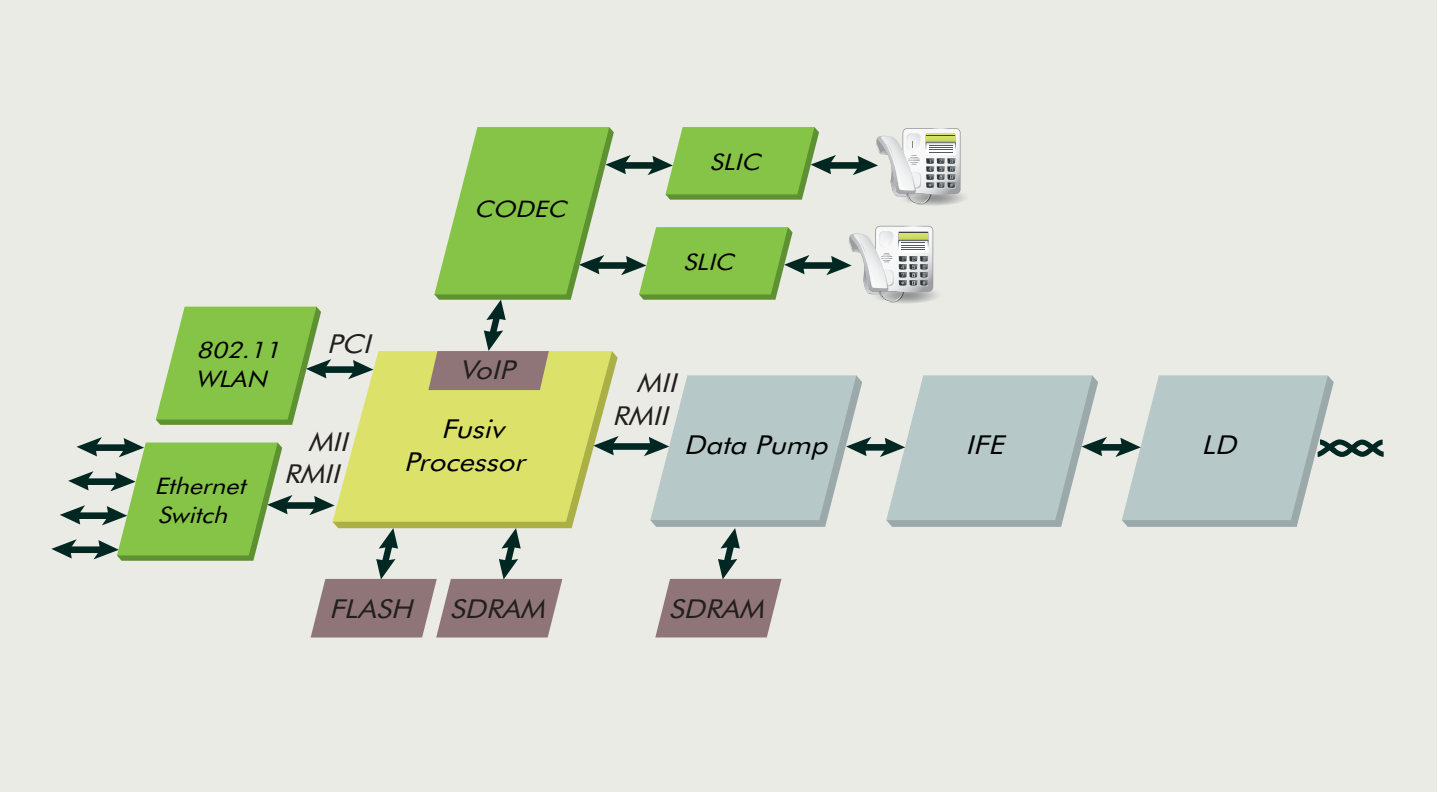
Common attributes of both chipsets include: the industry's highest performance, plug-and-play multi-mode operation, VDSL long range (VLR) capability with programmable U0, full band plan configurability for worldwide applications and interoperability with deployed central office (CO) equipment.The industry-standard xMII interfaces enable the chipsets to be used directly with external PHY chips for costeffective, standalone, host-less operation. In gateway and router applications, a communication processor can connect to the chipsets via the xMII or Utopia interfaces. Both chipsets are 100% pin compatible, which allows system vendors to develop a single CPE platform for worldwide deployment and reduces their development costs and time to market.

Both chipsets consist of a single-chip data pump (DSP engine) with the modem functionality and network interfaces, an Integrated Front End (IFE) with converters, amplifiers and filters, a line driver with programmable 8.5 - 14.5 dBm drive and the Ikanos Programmable Operating System™ (iPOS).

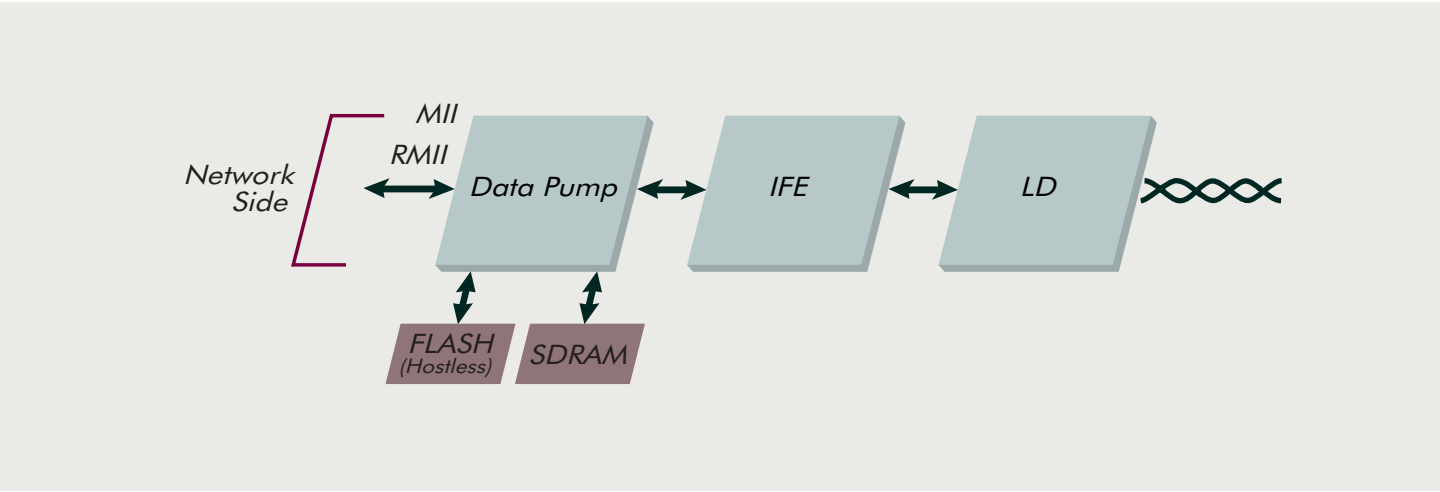
The iPOS consists of firmware and an OS-independent application programming interface (API) that enables easy integration into existing management software.

The Fx100100S-5 and Fx10050S-5 chipsets enable equipment vendors to develop a single system to deliver a full suite of revenue-generating interactive broadband services. The highly integrated architecture enables the design of smaller, simpler systems with fewer components and higher port density. Carriers can now achieve their goal of delivering universal service at 100 Mbps while simultaneously future-proofing their networks.

System Block Diagram – Residential Gateway



System Block Diagram – Hostless Modem



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Key Features

- Supports VDSL2 profiles
  - Fx100100S-5 supports 8a/8b/8c/8d, 12a/12b, 17a and 30a
  - Fx10050S-5 supports 8a/8b/8c/8d, 12a/12b and 17a
- Plug and play VDSL2 and VDSL operation
- Feature set optimized for triple play and
- IPTV including:
  - Available on-chip classification, queuing and scheduling for enhanced Quality of Service (QoS) for IPv4 and IPv6 networks
  - Support for Dual Latency, Dual Interleaving over xMII and Utopia interfaces for interworking with low cost 10/100 Ethernet PHY and high-performance communication processors
  - Maximum interleaver and de-interleaver memory for Impulse Noise Protection (INP)
  - Eraser detection and decoding for enhanced Impulse Noise Protection
- Universal CPE design for IP or ATM networks
  - Available integrated AAL5 SAR for ATM termination
  - Single worldwide platform for both short and long range applications
- Interoperable with deployed CO equipment
- Highly-integrated chipset consists of the following:
  - Data pump (DSP Engine) — a single chip data pump that integrates a framer, deframer, FFT/IFFT engines, interleaver/de-interleaver memory and network interfaces. An embedded 200 MIPS processor performs control-plane and management functions. The Data pump is available in different versions to support different levels of QoS
  - Integrated Front End (IFE) with on-chip ADC/DAC, amplifiers and filters
  - High-drive Line Driver (HLD) with integrated Low Noise Amplifier (LNA) supports programmable drive levels from 8.5 – 14.5 dBm
  - iPOS consists of firmware and OS-independent APIs that enable easy integration into existing management software
- Standards-compliant DMT line coding ensures spectral compatibility with POTS, ISDN, and DSL services per T1.417 standard
- Region-specific RFI notching
- IEEE 1149.1 compliant JTAG interface
- Industrial temperature range (-40 °C to +85 °C)

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