

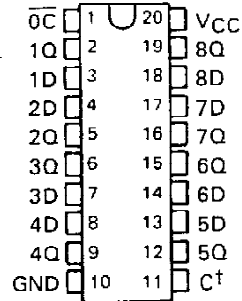
**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374**  
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1975—REVISED MARCH 1988

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)

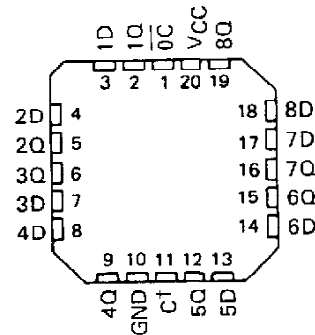
SN54LS373, SN54LS374, SN54S373,  
SN54S374 . . . J OR W PACKAGE  
SN74LS373, SN74LS374, SN74S373,  
SN74S374 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS373, SN54LS374, SN54S373,  
SN54S374 . . . FK PACKAGE

(TOP VIEW)



'LS373, 'S373  
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

'LS374, 'S374  
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

**description**

These 8-bit registers feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

Ct for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

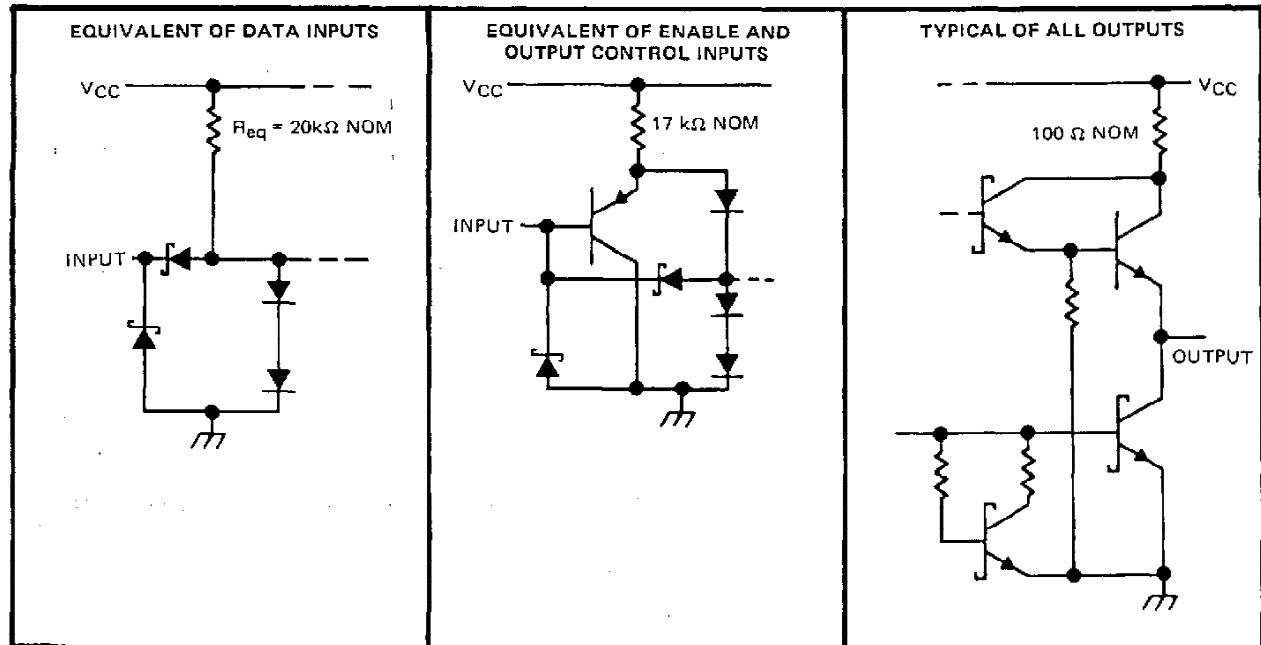


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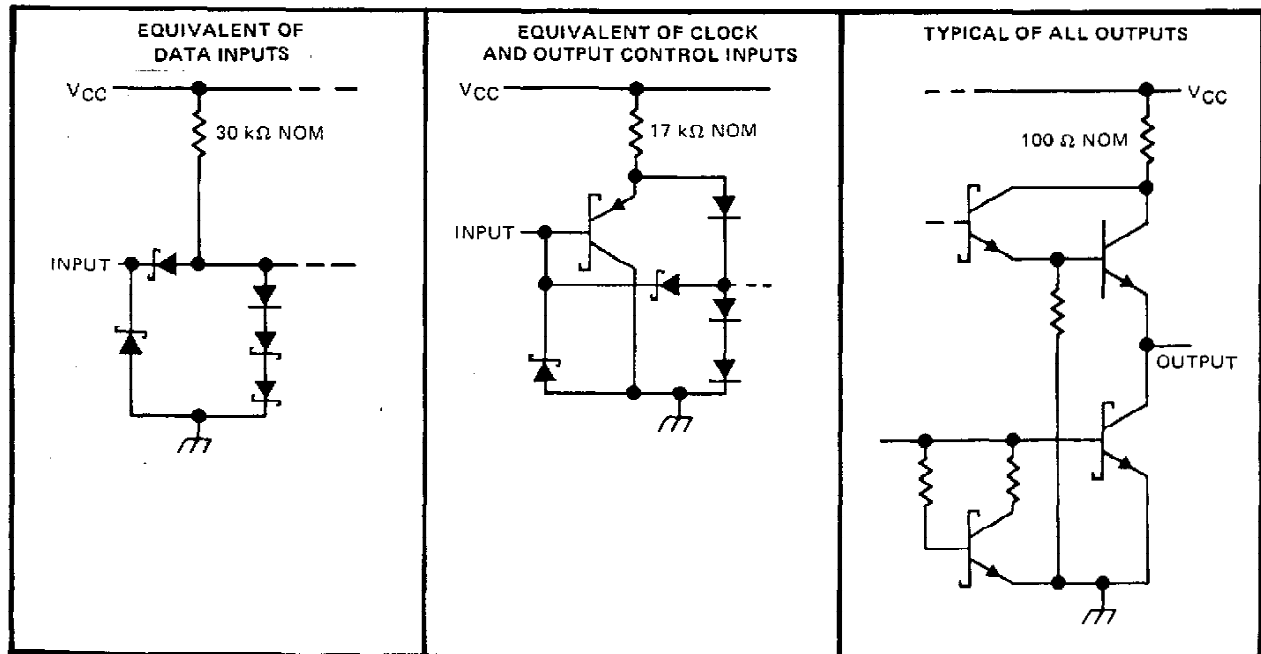
**SN54LS373, SN54LS374, SN74LS373, SN74LS374**  
**OCTAL D-TYPE TRANSPARENT LATCHES AND**  
**EDGE-TRIGGERED FLIP-FLOPS**

schematic of inputs and outputs

\*LS373



\*LS374



  
**TEXAS**  
**INSTRUMENTS**

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# SN54LS373, SN54LS374, SN74LS373, SN74LS374

## OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{OH}$	High-level output voltage			5.5			5.5	V
$I_{OH}$	High-level output current			-1			-2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$t_w$	Pulse duration	CLK high	15		15			ns
		CLK low	15		15			
$t_{su}$	Data setup time	'LS373	5↓		5↓			ns
		'LS374	20↑		20↑			
$t_h$	Data hold time	'LS373	20↓		20↓			ns
		'LS374†	5↑		0↑			
$T_A$	Operating free-air temperature	-55		125	0		70	°C

†The  $t_h$  specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns. (Commercial only)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}, I_{OH} = \text{MAX}$		2.4	3.4		2.4 3.1	V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}$		0.25	0.4		0.25 0.4	V
		$I_{OL} = 12 \text{ mA}$						
$I_{OZH}$	Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 2.7 \text{ V}$		20			20	μA
$I_{OZL}$	Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 0.4 \text{ V}$		-20			-20	μA
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20	μA
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4	mA
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}$		-30	-130		-30 -130	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX},$		24	40		24 40	mA
		Output control at 4.5 V						

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.



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**SN54LS373, SN54LS374, SN74LS373, SN74LS374**  
**OCTAL D-TYPE TRANSPARENT LATCHES AND**  
**EDGE-TRIGGERED FLIP-FLOPS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS373			'LS374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$f_{max}$			$C_L = 45\text{ pF}$ , $R_L = 667\ \Omega$ See Notes 2 and 3				35	50		MHz
$t_{PLH}$	Data	Any Q		12	18					ns
$t_{PHL}$				12	18					
$t_{PLH}$	Clock or enable	Any Q		20	30		15	28	ns	
$t_{PHL}$				18	30		19	28		
$t_{PZH}$	Output Control	Any Q		15	28		20	26	ns	
$t_{PZL}$			25	36		21	28			
$t_{PHZ}$	Output Control	Any Q	$C_L = 5\text{ pF}$ , $R_L = 667\ \Omega$ See Note 3	15	25		15	28	ns	
$t_{PLZ}$	Output Control	Any Q		12	20		12	20	ns	

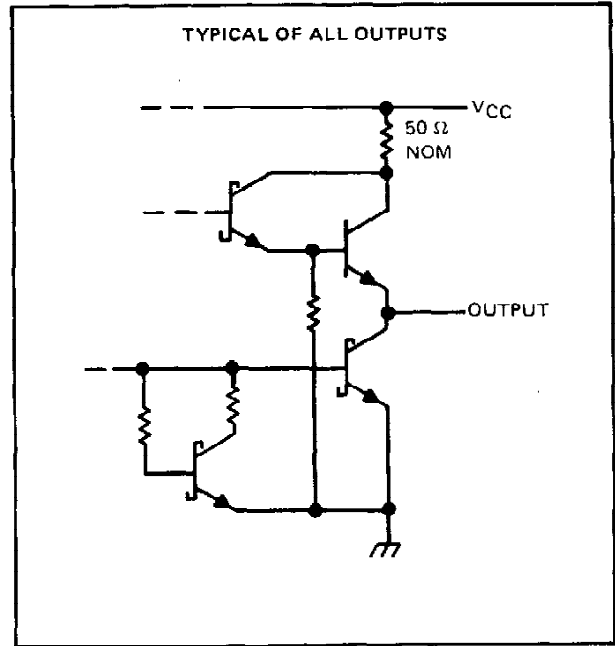
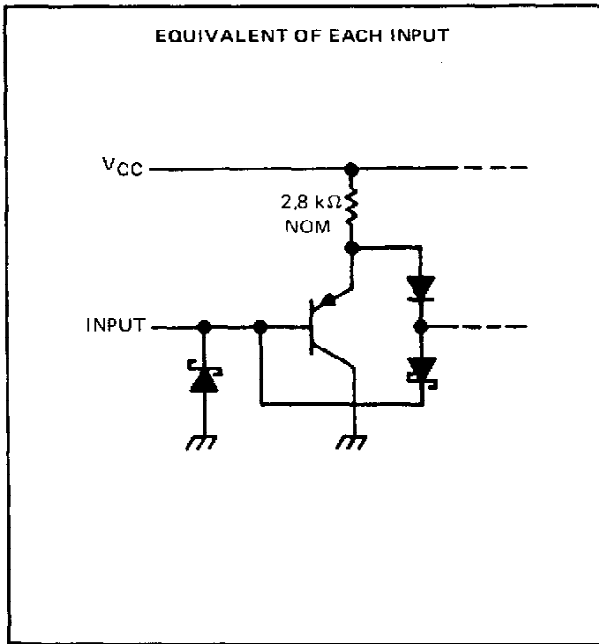
NOTES: 2. Maximum clock frequency is tested with all outputs loaded.  
3. Load circuits and voltage waveforms are shown in Section 1.

$f_{max}$  = maximum clock frequency  
 $t_{PLH}$  = propagation delay time, low-to-high-level output  
 $t_{PHL}$  = propagation delay time, high-to-low-level output  
 $t_{PZH}$  = output enable time to high level  
 $t_{PZL}$  = output enable time to low level  
 $t_{PHZ}$  = output disable time from high level  
 $t_{PLZ}$  = output disable time from low level

# SN54S373, SN54S374, SN74S373, SN74S374

## OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S'	-55°C to 125°C
SN74S'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, $V_{OH}$				5.5			5.5	V
High-level output current, $I_{OH}$				-2			-6.5	mA
Width of clock/enable pulse, $t_w$	High	6			6			ns
	Low	7.3			7.3			
Data setup time, $t_{su}$	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, $t_h$	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, $T_A$		-55		125	0		70	°C



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# SN54S373, SN54S374, SN74S373, SN74S374

## OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V <sub>IH</sub>					2			V
V <sub>IL</sub>							0.8	V
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA					-1.2	V
V <sub>OH</sub>	SN54S'	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX			2.4	3.4		V
	SN74S'				2.4	3.1		
V <sub>OL</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA					0.5	V
I <sub>OZH</sub>		V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 2.4 V					50	μA
I <sub>OZL</sub>		V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 0.5 V					-50	μA
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V					1	mA
I <sub>IH</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V					50	μA
I <sub>IL</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V					-250	μA
I <sub>OS</sub> §		V <sub>CC</sub> = MAX			-40		-100	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX	'S373		outputs high			160	mA
				outputs low			160	
				outputs disabled			190	
		'S374		outputs high			110	
				outputs low			140	
				outputs disabled			160	
CLK and OC at 4 V, D inputs at 0 V						180		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>			C <sub>L</sub> = 15 pF, R <sub>L</sub> = 280 Ω, See Notes 2 and 4				75	100		MHz
t <sub>PLH</sub>	Data	Any Q		7	12					ns
t <sub>PHL</sub>				7	12					
t <sub>PLH</sub>	Clock or enable	Any Q		7	14		8	15		ns
t <sub>PHL</sub>				12	18		11	17		
t <sub>PZH</sub>	Output Control	Any Q		8	15		8	15		ns
t <sub>PZL</sub>			11	18		11	18			
t <sub>PHZ</sub>	Output Control	Any Q	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 280 Ω, See Note 3	6	9		5	9	ns	
t <sub>PLZ</sub>				8	12		7	12		

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.

4. Load circuits and voltage waveforms are shown in Section 1.

f<sub>max</sub> = maximum clock frequency

t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

t<sub>PZH</sub> = output enable time to high level

t<sub>PZL</sub> = output enable time to low level

t<sub>PHZ</sub> = output disable time from high level

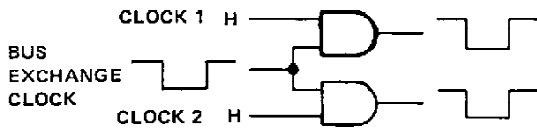
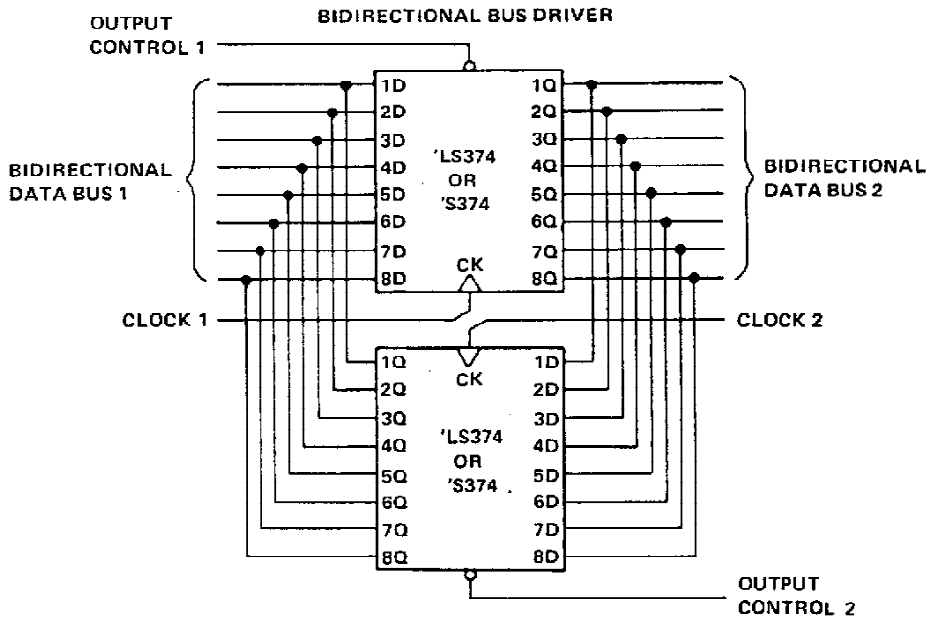
t<sub>PLZ</sub> = output disable time from low level

  
**TEXAS  
INSTRUMENTS**

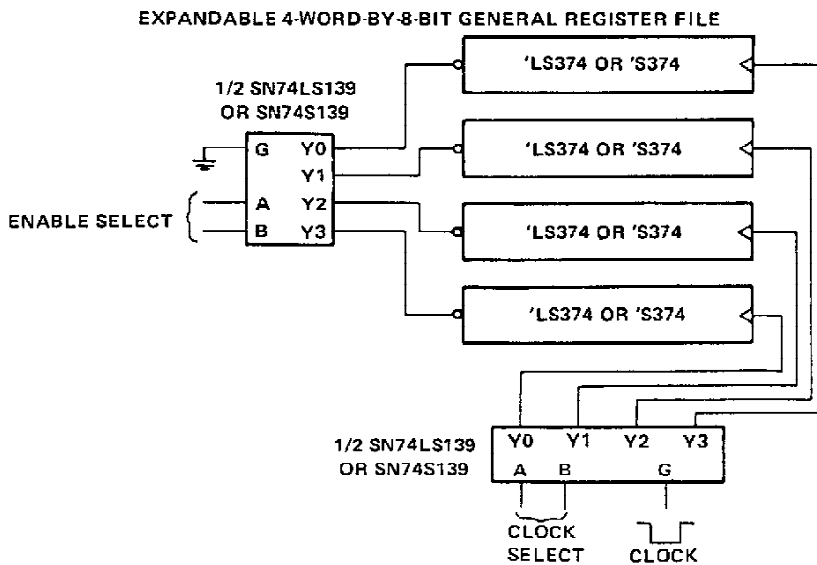
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**SN54LS373, SN54LS374, SN54S373, SN54S374,  
 SN74LS373, SN74LS374, SN74S373, SN74S374  
 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

**TYPICAL APPLICATION DATA**



**CLOCK CIRCUIT FOR BUS EXCHANGE**



**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374  
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

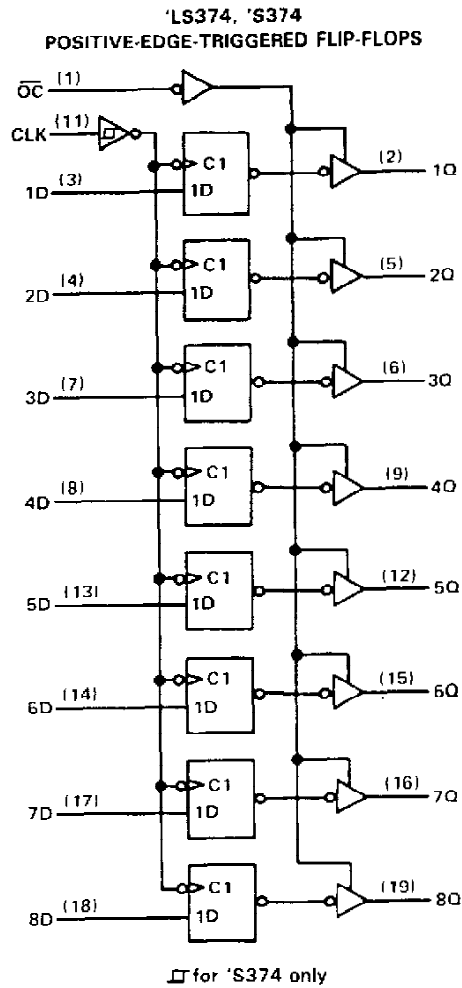
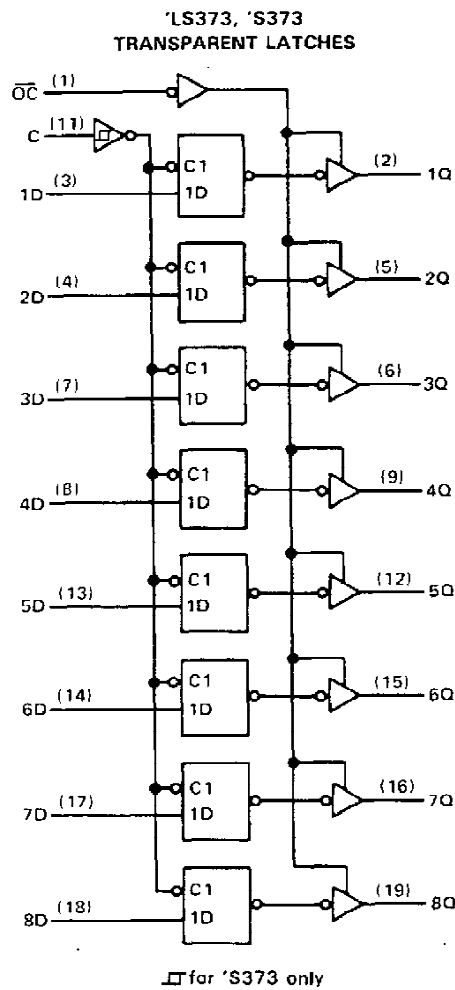
**description (continued)**

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices, simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

**logic diagrams (positive logic)**



Pin numbers shown are for DW, J, N, and W packages.



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