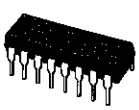
SGS-THOMSON MICROELECTRONICS

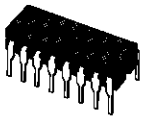
HCC/HCF40104B
HCC/HCF40194B

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

- MEDIUM-SPEED OPERATION : f_{CL} = 9MHz (typ.) @ V_{DD} = 10V
- FULLY STATIC OPERATION
- SYNCHRONOUS PARALLEL OR SERIAL OPERATION
- THREE-STATE OUTPUTS (**HCC/HCF40104B**)
- ASYNCHRONOUS MASTER RESET (**HCC/HCF40194B**)
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)



F
(Ceramic Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

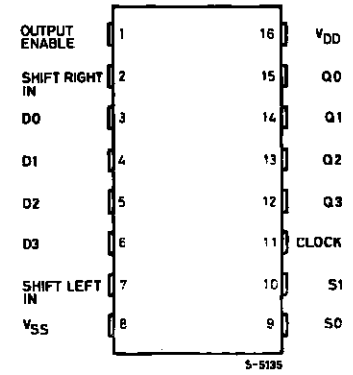
HCC401XXBF HCF401XXBEY
HCF401XXBC1

DESCRIPTION

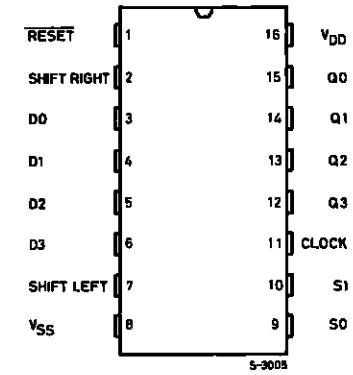
The **HCC40104B, HCC40194B**, (extended temperature range) and the **HCC40104B, HCF40194B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF 40104B** is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state. The **HCC/HCF40194B** is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and

PIN CONNECTIONS

40104B



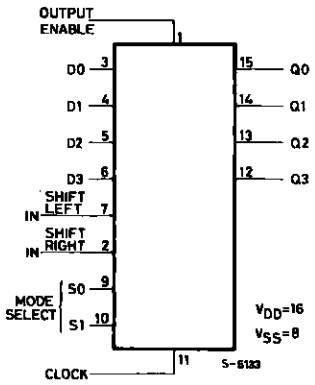
40194B



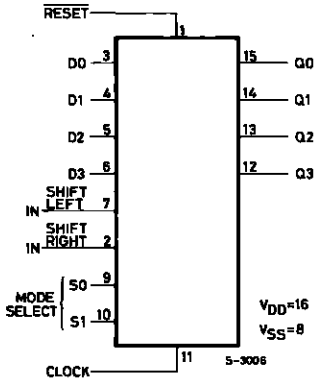
appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the RESET input resets all stages and forces all outputs low. The **HCC/HCF40194B** is similar to industry types 340194 and MC40194.

FUNCTIONAL DIAGRAMS

40104B



40194B



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : **HCC** Types **HCF** Types	– 0.5 to + 20 – 0.5 to + 18	V V
V_i	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

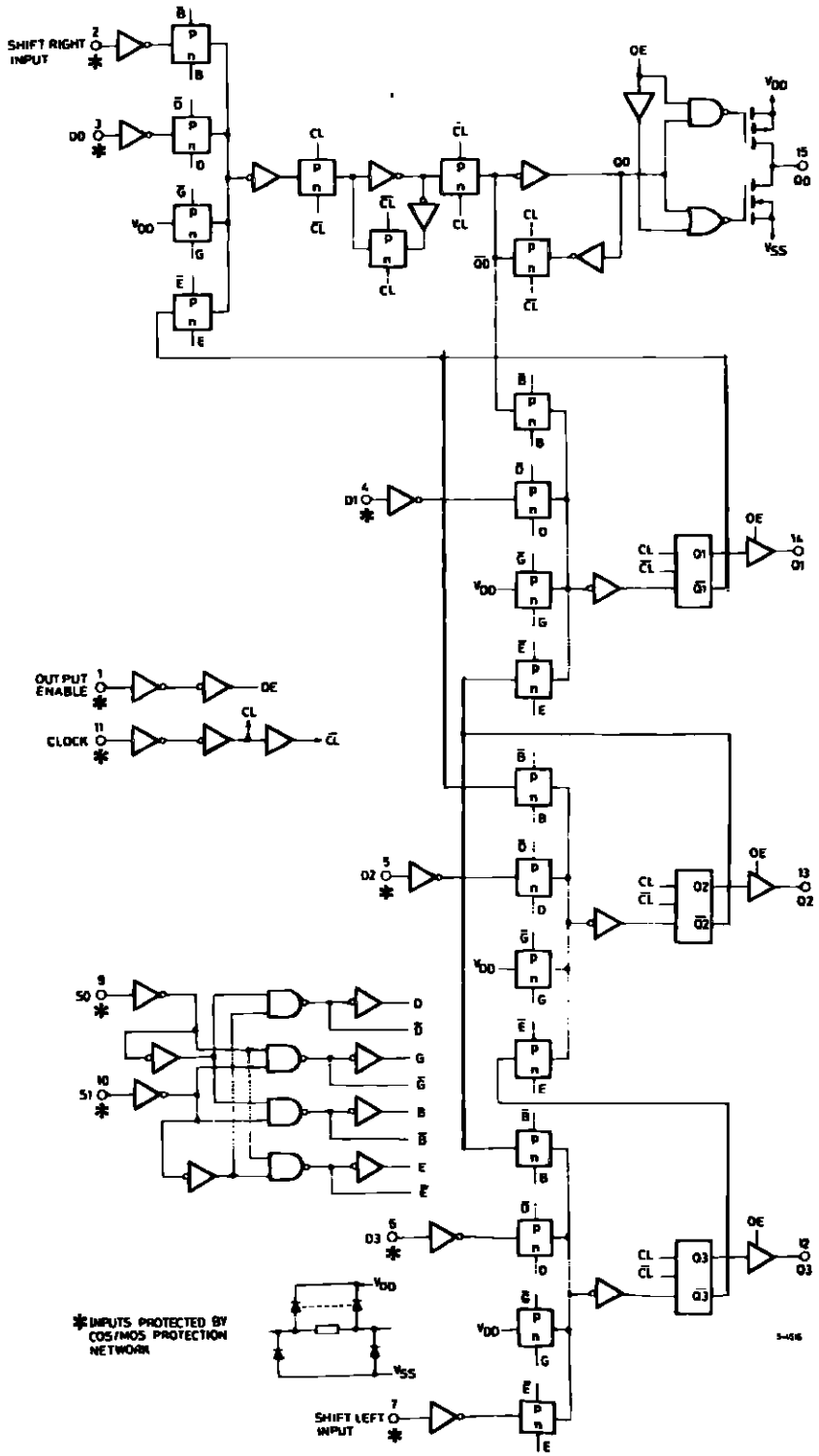
* All voltages values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : **HCC** Types **HCF** Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C

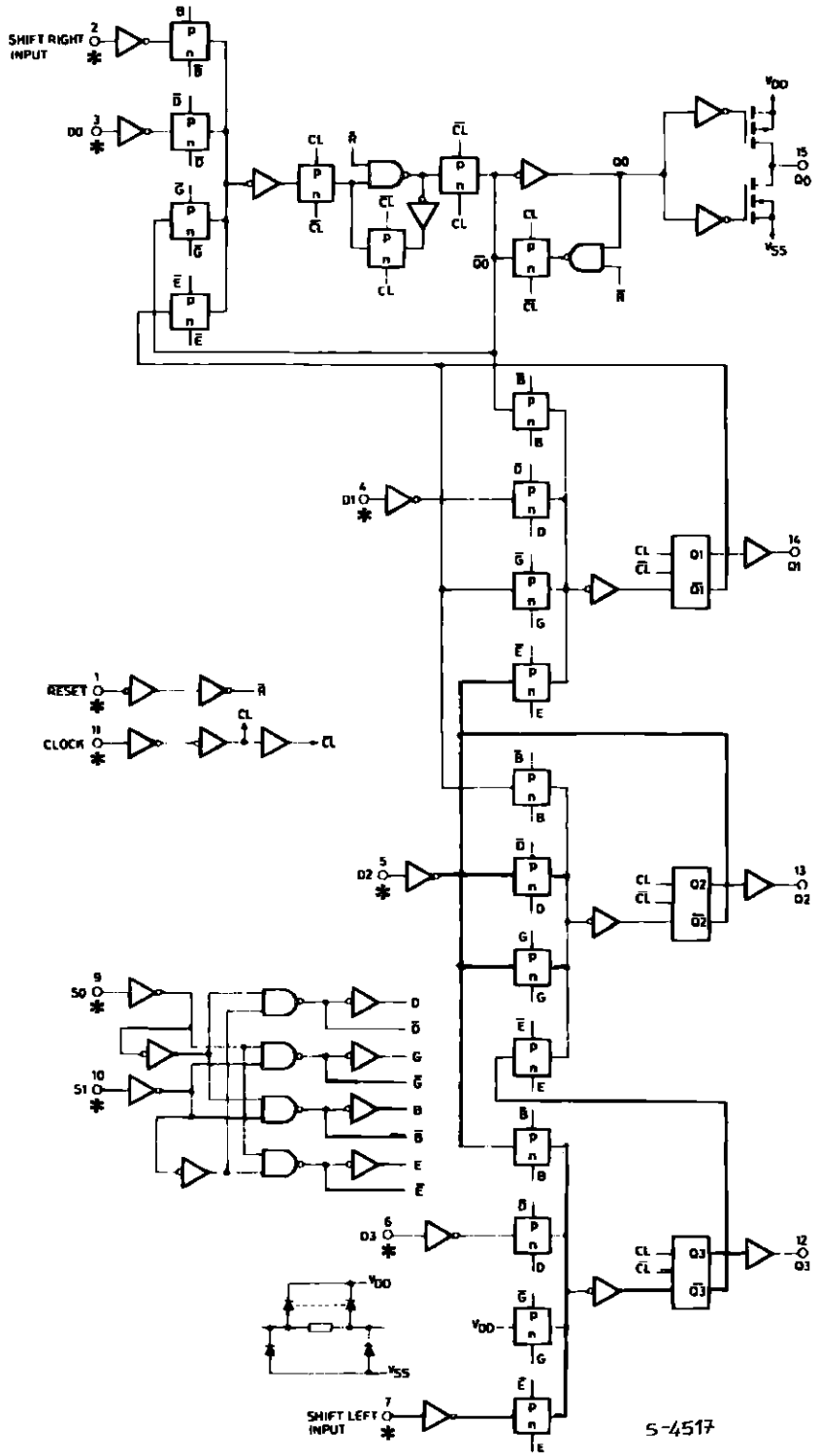
LOGIC DIAGRAMS

40104B



LOGIC DIAGRAMS

40194B



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
		HCF Types	0/ 5	2.5		5	– 1.53		– 1.36	– 3.2		– 1.1		
			0/ 5	4.6		5	– 0.52		– 0.44	– 1		– 0.36		
			0/10	9.5		10	– 1.3		– 1.1	– 2.6		– 0.9		
			0/15	13.5		15	– 3.6		– 3.0	– 6.8		– 2.4		
I_{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C_I	Input Capacitance			Any Input						5	7.5			pF

* T_{LOW}= – 55°C for **HCC** device : – 40°C for **HCF** device.
* T_{HIGH}= + 125°C for **HCC** device : + 85°C for **HCF** device.
The noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5 min. with V_{DD} = 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time Clock to Q		5		220	440	ns
			10		100	200	
			15		70	140	
t_{PZH}, t_{PZL}, t_{PLZ}	3-state Outputs ■ High Impedance		5		80	160	ns
			10		35	70	
			15		25	50	
t_{PHZ}			5		45	90	ns
			10		25	50	
			15		20	40	
t_{THL}, t_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_{setup}	Setup Time D0,D3,SR, SL to Clock		5		80	100	ns
			10		35	70	
			15		20	50	
	S0, S1 to Clock		5		200	400	ns
			10		110	220	
			15		65	130	
t_{hold}	Hold Time D0,D3,SR, SL to Clock		5		– 65	0	ns
			10		– 25	0	
			15		– 15	0	
	S0, S1 to Clock		5		– 170	0	ns
			10		– 95	0	
			15		– 55	0	
t_W	Clock Pulse Width		5		90	180	ns
			10		40	180	
			15		25	50	
f_{CL}	Clock Input Frequency		5	3	6		MHz
			10	6	12		
			15	8	15		
t_r, t_f	Clock Input Rise or Fall Time		5			1000	µs
			10			100	
			15			100	
t_W	Reset Pulse Width*		5		150	300	ns
			10		100	200	
			15		70	140	
t_{PRHL}	Propagation Delay Reset*		5		230	460	ns
			10		90	180	
			15		65	130	

■ For 40104B series only * For 40194B series only.

TRUTH TABLES

40104B

Clock▲	Mode Select		Output Enable	Action
	S0	S1		
_/‾	0	0	1	Reset
_/‾	1	0	1	Shift Right (Q0 toward Q3)
_/‾	0	1	1	Shift Left (Q3 toward Q0)
_/‾	1	1	1	Parallel Load
X	X	X	0	Operations occur as shown above, but outputs assume high impedance

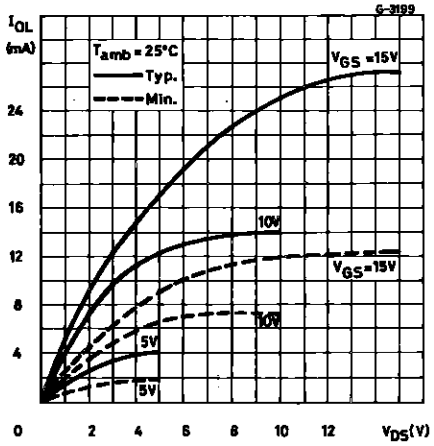
40194B

Clock	Mode Select		$\overline{\text{Reset}}$	Action
	S0	S1		
X	0	0	1	No Change
_/‾	1	0	1	Shift Right (Q0 toward Q3)
_/‾	0	1	1	Shift Left (Q3 toward Q0)
_/‾	1	1	1	Parallel Load
X	X	X	0	Reset

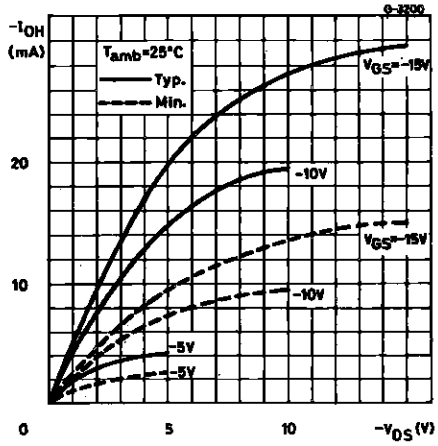
1=High level
0=Low level

X= Don't care
Δ = Level change

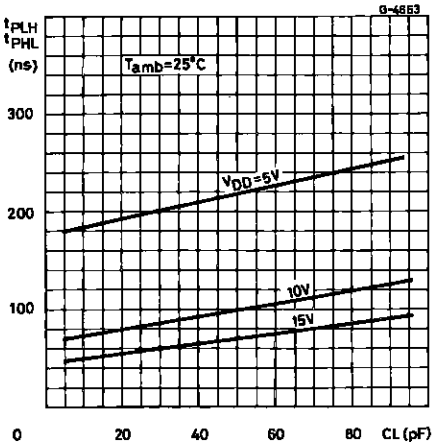
Output Low (sink) Current Characteristics.



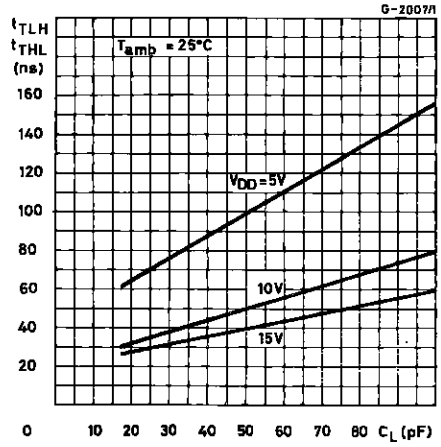
Output High (source) Current Characteristics.



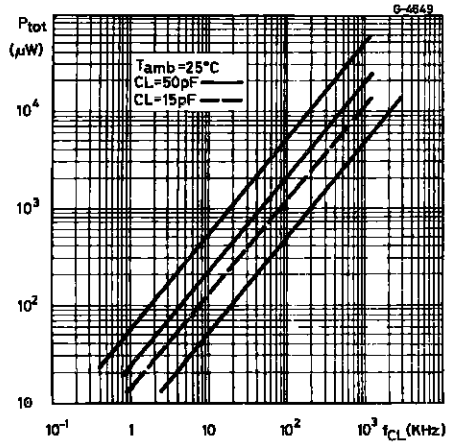
Typical Propagation Delay Time vs. Load Capacitance.



Typical Transition Time vs. Load Capacitance.

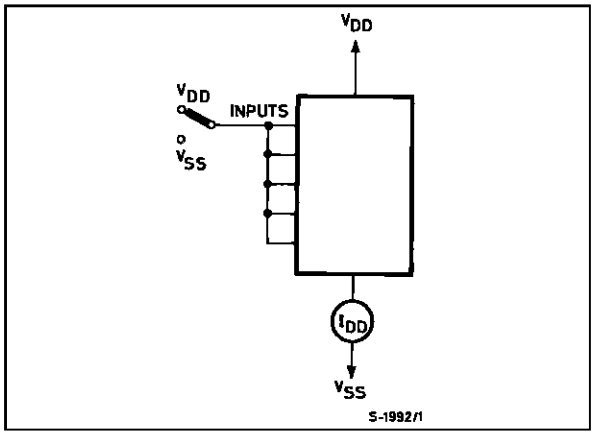


Typical Dynamic Power Dissipation vs. Frequency.

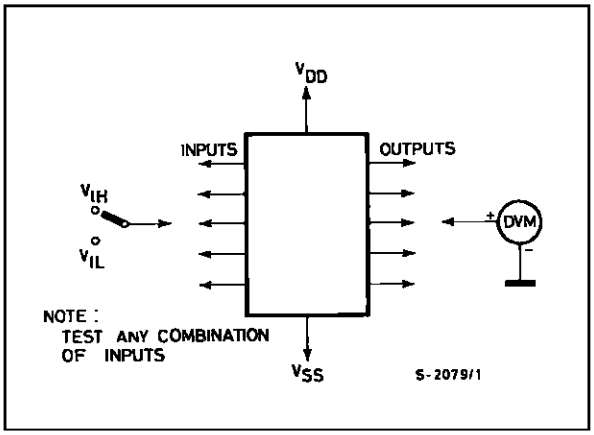


TEST CIRCUITS

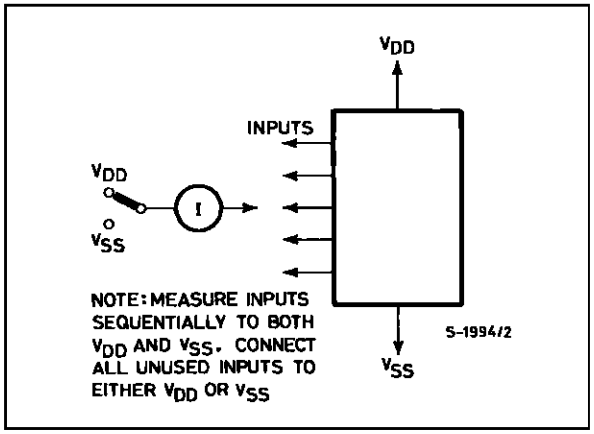
Quiescent Device Current.



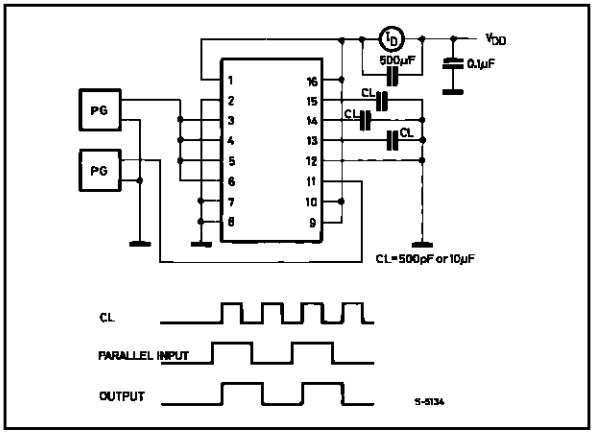
Input Voltage.



Input Leakage Current.

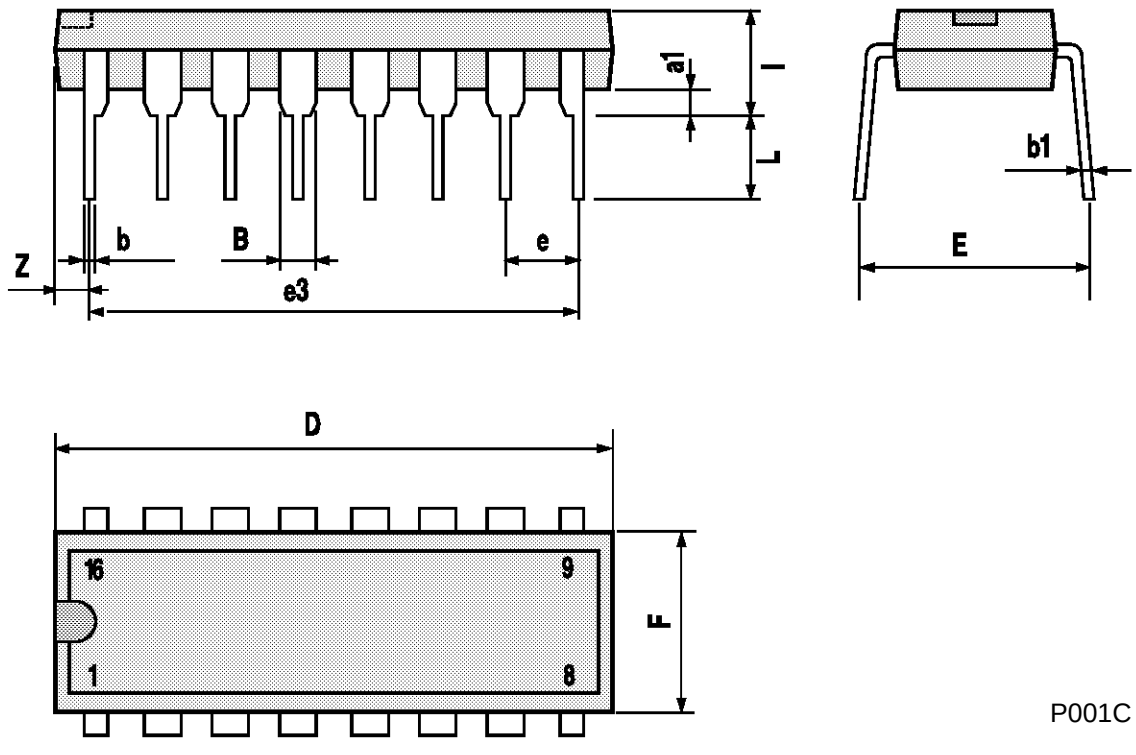


Dynamic Power Dissipation.



Plastic DIP16 (0.25) MECHANICAL DATA

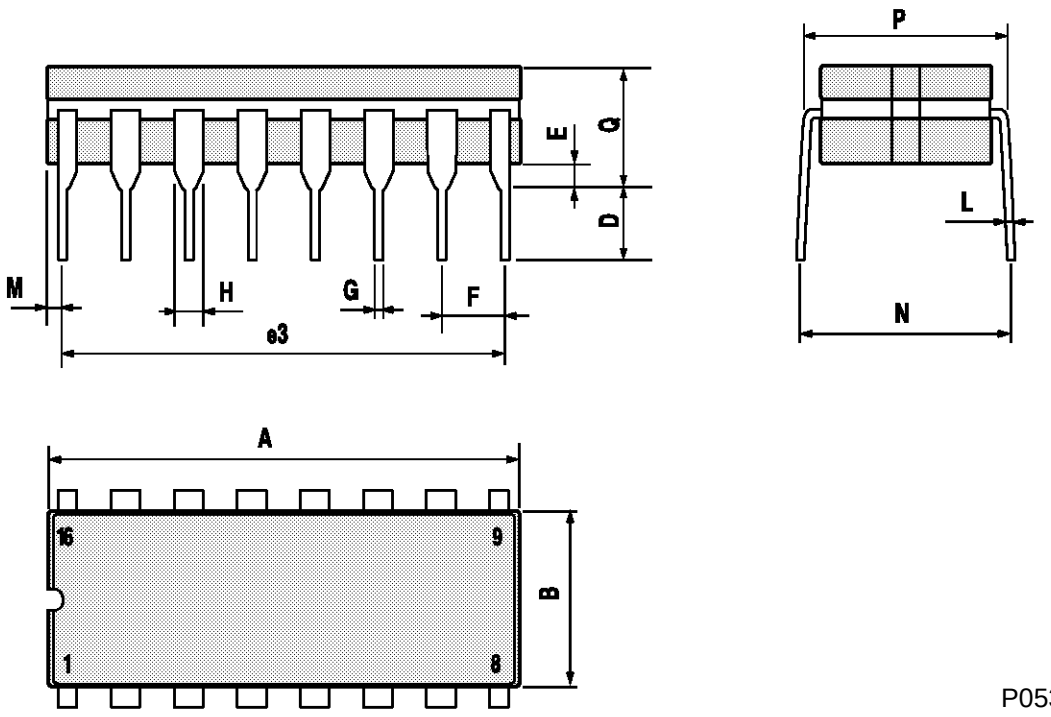
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

Ceramic DIP16/1 MECHANICAL DATA

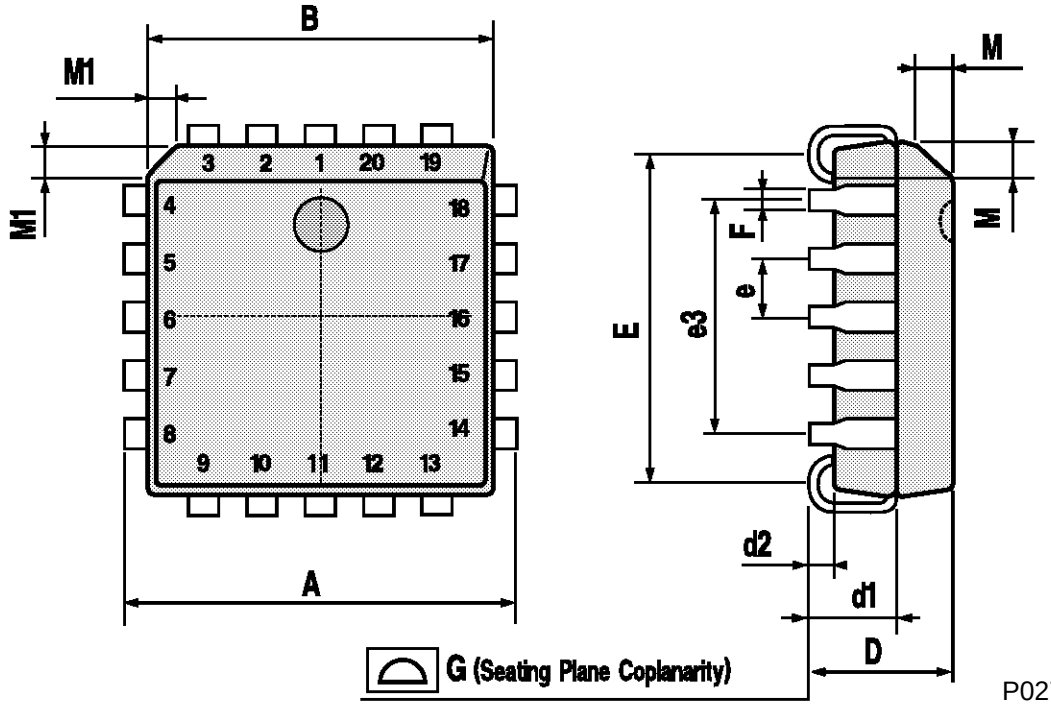
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053D

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



P027A

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