

INTRODUCTION

Dallas Semiconductor iButtons are designed to operate with a contact range exceeding 100 meters. The devices require a single bidirectional bus master for communication over the 1-Wire™ bus. The ideal connection between an iButton™ and its bus master is a short cable with low resistance and low capacitance. As the distance between the iButton and the bus master becomes longer, more care must be taken to ensure that the waveforms of the communication signals meet specification. The effects of cable length and lumped capacitance on two different bus master types are described as well as some guidelines for successful operation of iButton at extended cable lengths. The two bus master types are shown in Figure 1. The open drain type with a resistor pullup uses Port 0.3 of the Dallas Semiconductor DS5000 (8051-equivalent) microcontroller as an output and Port 0.4 as an input. The COM Port type uses a DS9097 COM Port Adaptor with a computer that has an Intel 8250-equivalent UART chip to drive the line. This COM Port Adaptor is the type provided in the DS9092K iButton Starter Kit. The cable used is 22 gauge, twisted-pair telephone wire with the characteristics shown in Table 1. A single twisted-pair of conductors out of the 30-pair bundle within the cable were used for bus master evaluation (see Figure 2). The lumped capacitance measurements were made using a capacitance decade box applied in parallel with the iButton (see Figure 3). Since many different wire types may be used for interconnect, the lumped capacitance data provides some ability to estimate operating distances for alternate wire if the characteristics of that alternate wire are known. The lumped capacitance data also allows estimation of total capacitive load capability for non-wire connections and contact surfaces for a particular bus master type. The test software for the DS1991, DS1992, DS1993 and DS1994 executed a Search ROM command and read ten bytes of RAM data

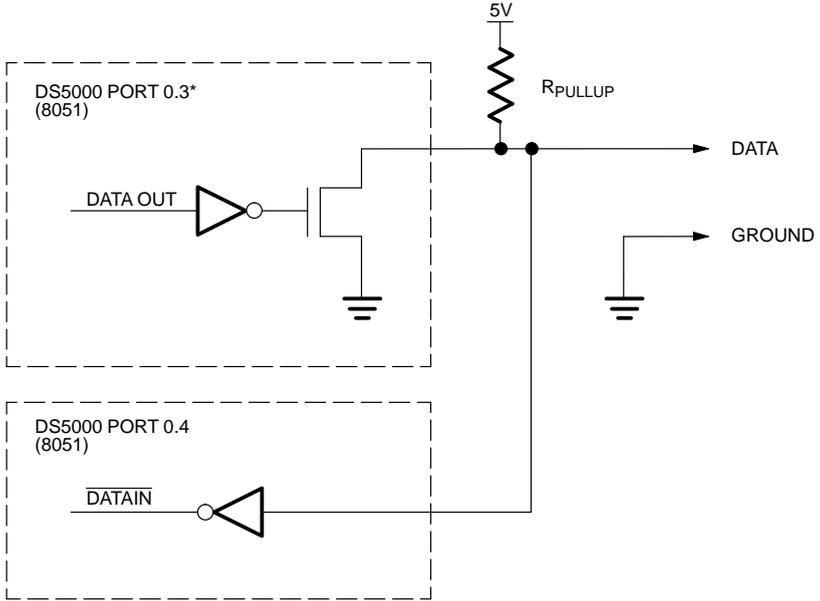
from each device present. The DS1990 was tested using the Read ROM command.

GENERAL GUIDELINES FOR OPERATION OVER EXTENDED DISTANCES

1-Wire Timing

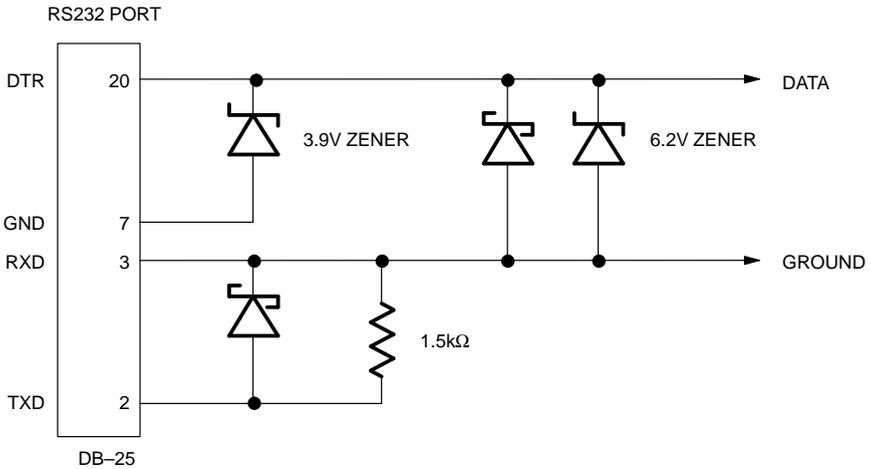
The bus master writes an iButton with a minimum low time of 60 μs for a Write 0 and a maximum low time of 15 μs for a Write 1 (see Figure 4a). The bus master reads an iButton by pulling the data line low then releasing and monitoring the condition of the data line. For the iButton to signal a Read 0 time slot, it continues to hold the data line low for a minimum of 15 μs from the initial falling edge. For the iButton to signal a Read 1 time slot, it allows the data line to return high via the pullup resistor. The pullup resistor must return the data line to a logic high level within 15 μs of the initial falling edge (see Figure 4b). The recovery time between time slots must be a minimum of 1 μs . These timing values result in the highest possible data rate. (For more details on 1-Wire timing, see the Dallas Semiconductor Automatic Identification Data Book or Book of DS19xx iButton Standards). For short cable lengths and small capacitive loads, this timing can be achieved with a pullup resistor in the 5k Ω to 10k Ω range. Using a resistor in this range maximizes design margin by providing a very small DC load to the iButton and therefore a strong logic low level to the input side of the bidirectional bus master. As cable length becomes longer, the capacitive load presented to the bus master increases and the RC time constant associated with the resistor pulling the line high after the active pulldown transistor releases begins to exceed the time slot conditions for correct operation. Using the lowest capacitance cable available will provide the greatest operating distances for a given pullup value. The twisted-pair cable that was used for testing is approximately 52 pF/m.

1-WIRE BUS MASTER TYPES Figure 1



*Substitution of other port pins that are not open drain but have active pull-ups that are aulsed on briefly may cause unreliable operation or nonfunctionality.

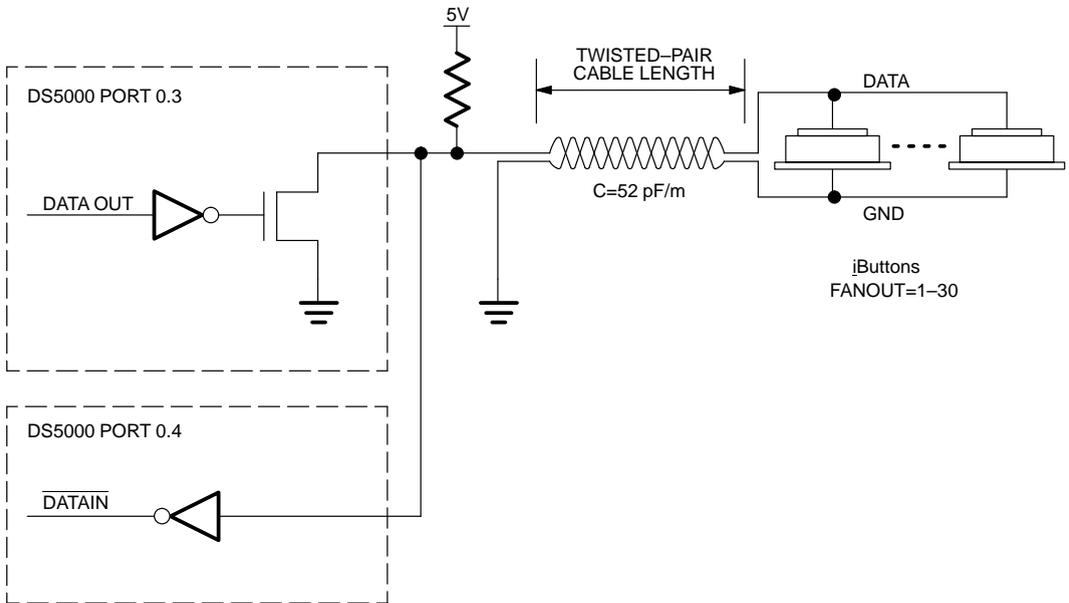
a) Open Drain Output with Resistor Pullup

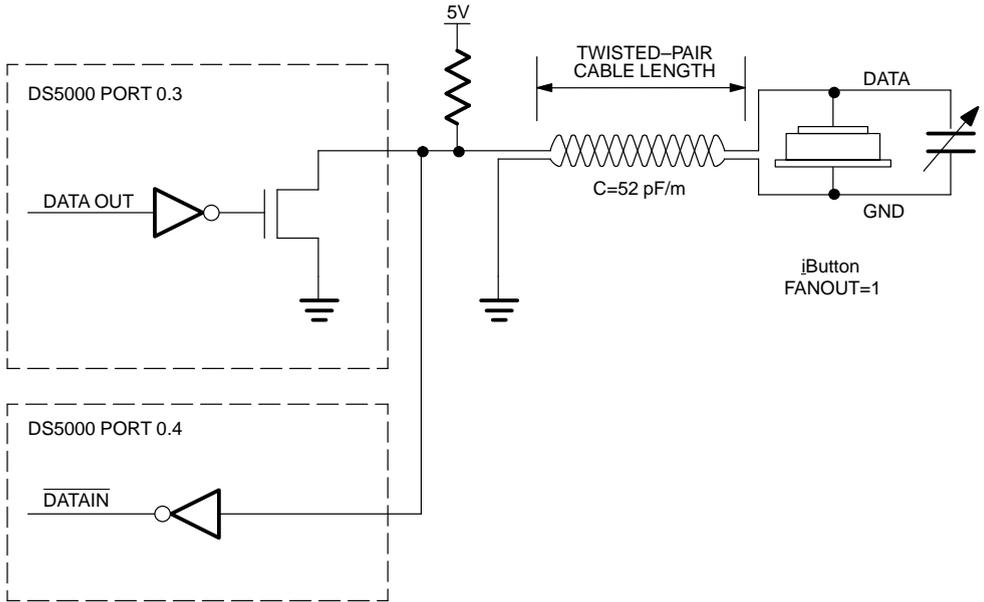


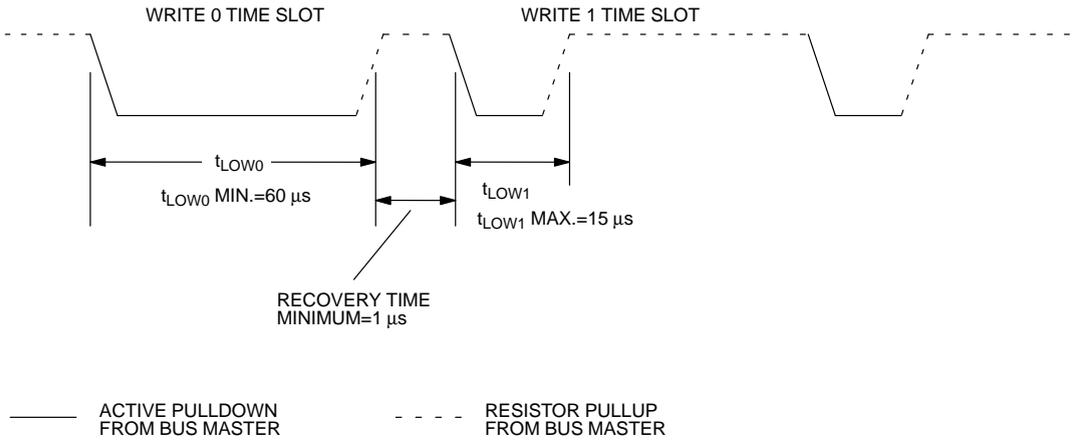
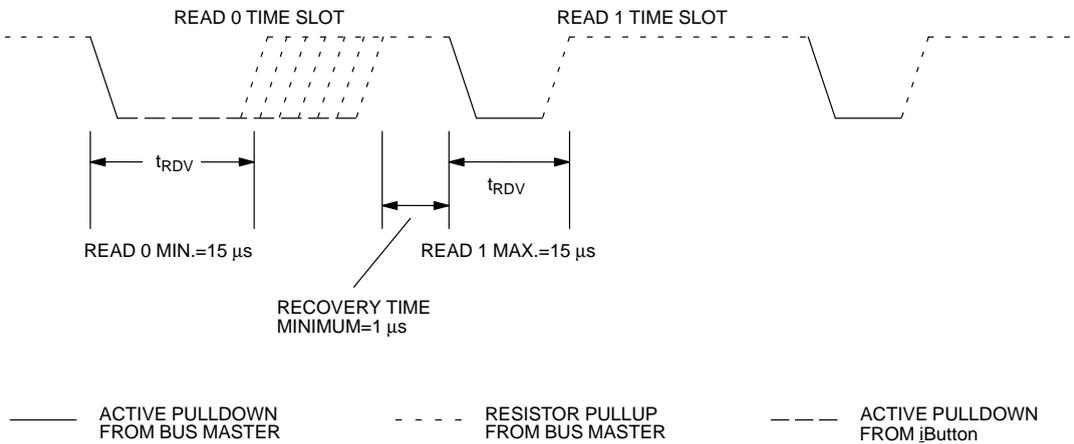
b) DS907 COM port Adaptor

CABLE CHARACTERISTICS – 22 GAUGE PLASTIC INSULATED CABLE AT 25°C Table 1

FREQ Hz	R ohm/km	L mH/km	G μ MHO/km	C μ F/km	Z_0 ohms		GAMMA	
							dB	deg/km
1	108	0.6128	0.000	0.052	12927	$-J^*12924$	0.037	0.24
100	108	0.6128	0.006	0.052	1295	$-J^*1290$	0.363	2.40
1k	108	0.6125	0.047	0.052	416	$-J^*402$	1.130	7.7
10k	109	0.6092	0.405	0.052	154	$-J^*109$	3.071	28.6
100k	134	0.5740	3.498	0.052	107	$-J^*19.3$	5.426	199
1M	362	0.4940	30.192	0.052	98	$-J^*5.70$	16.076	1820

FANOUT TEST SETUP (OPEN DRAIN W/RESISTOR BUS MASTER) Figure 2

LUMPED CAPACITANCE TEST SETUP (OPEN DRAIN W/RESISTOR BUS MASTER) Figure 3

MAXIMUM DATA RATE 1 – WIRE TIMING Figure 4**a) 1-Wire Timing – Write Time Slots****b) 1-Wire Timing – Read Time Slots**

Cable Length Effects on Read 1 Time Slots

The Read 1 time slot begins with an active device in the bus master pulling the line low and a resistor returning the line to a high level. A logic high level must be reached within 15 μ s of the falling edge in order to meet the 1–Wire timing specification for a logical 1. If the rise time becomes too slow due to loading, the desired logical 1 will be interpreted as being a logical 0 by the input stage of the bus master (see Figure 5). The pullup resistor value in the bus master can be reduced to improve the recovery time for large capacitive loads. The lower limit of the resistor should be approximately 1150 ohms. This value is derived from the *i*Button current sink capability of 4 mA at 0.4 volts. For a 5–volt system, the resistor will have 4.6 volts across it with 4 mA of current flowing through it resulting in a minimum value of 4.6/4 mA or 1150 ohms (see Figure 6). As this resistor value is further decreased the guaranteed noise margins for logic low levels are compromised. In general, the largest pullup resistor value that still provides sufficient operating margin at the desired distance should be used.

Additional improvement can be realized by releasing the active pulldown device in the bus master as quickly as possible after the data line is driven low. The minimum amount of time that the data line must be held low by the bus master is 1 μ s in order to meet the 1–Wire timing specifications. In practice the low time might be several microseconds due to the speed at which the port pin of the microcontroller or microprocessor can operate. The low time must also be sufficiently long to allow an *i*Button at the end of a long cable to interpret the low–going pulse correctly even though it may have been degraded significantly. For the data that is presented, the bus master pulldown was released 6.5 μ s after it was driven low for the open drain type.

Cable Length Effects on Write 0 Time Slots

The 60 μ s Write 0 time slot begins with an active device in the bus master pulling the data line low and a resistor returning the line to a high level. At least two consecutive Write 0 pulses (as in the case of the Search ROM command byte F0h) separated by the minimum 1 μ s recovery time can be degraded sufficiently over a long cable length that eventually the command byte is not interpreted correctly by the *i*Button and failure occurs. Figure 7 shows the filtering effect that the long cable can have on the recovery time. Increasing the amount of recovery time between time slots will extend the length of cable over which communication can occur. By increasing the recovery time from the 1 μ s minimum to

15 μ s, the worst case condition will always be determined by the Read 1 time slot and failure will occur there first. Increasing the recovery time to 15 μ s will reduce the data rate slightly, from 16.3kbits/s (60 μ s + 1 μ s) to 13.3kbits/s (60 μ s + 15 μ s).

OPEN DRAIN WITH RESISTOR PULLUP

The open drain port pin 0.3 of the DS5000 microcontroller was used with pullup resistor values ranging from 1k Ω to 10k Ω . The input stage of the bus master used port 0.4 of the DS5000, which is a TTL–compatible input that sampled the data line voltage level approximately 14 μ s after the line had been driven low. Each *i*Button device type was tested and the results show that a single device of any type can be read at cable lengths exceeding 300 m with a pullup resistor value of 1k Ω . Some reduction in distance occurs as *i*Button fanout increases, but the 1k Ω pullup can still read 30 devices at 240 m.

The lumped capacitive load that a particular resistor value can drive for a given cable length is also shown. The data indicates that the loading at long distances is directly proportional to the cable capacitance, as expected. For the DS1990 with a 1k Ω resistor, for example, the maximum 0 distance load is 16800 pF and the device also fails at just over 300 m of cable with a load of 1600 pF. The equivalent load at 300 m is (300 m) \times (52 pF/m) or 15600 pF for the cable and a lumped load of 1600 pF for a total of 17200 pF. Selecting the lowest capacitance cable available will increase the communication distance almost linearly for a given resistor value.

COM PORT BUS MASTER WITH DS9097 ADAPTOR

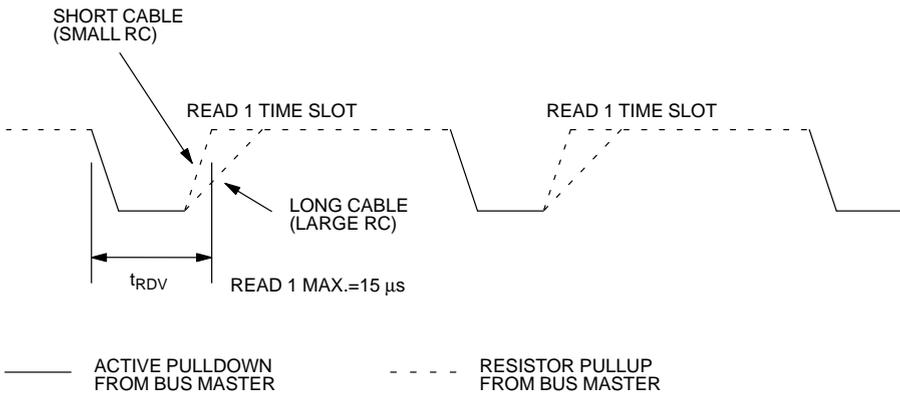
A second bus master type is examined which is created by attaching the DS9097 COM Port Adaptor to the RS–232 port of a 16Mhz 286–class PC that has an Intel 8250–equivalent UART chip. The DS9097 COM Port Adaptor is available as a standard product from Dallas Semiconductor. The resulting bus master has the approximate characteristics of a 5 mA current source. This provides operation that is roughly equivalent to the open drain bus master with a 1.5k Ω pullup. The data confirms that the performance of the COM port bus master falls between that of the open drain bus master with a 1.0k Ω pullup resistor and the open drain bus master with a 2.2k Ω pullup resistor.

The performance of the COM port bus master was very consistent for all types of *i*Button devices. One difference between the microcontroller-based open drain bus master and the PC-based COM port bus master was the recovery time. The timing constraints imposed by the UART coupled with the computational performance of the PC resulted in a time slot of approximately 118 μ s (8.5kbit/s data rate) which included a 58 μ s recovery time. This is significantly longer than the 75 μ s time slot which included a 15 μ s recovery time that the DS5000 microcontroller created. The fanout and capacitive loading results for the two bus masters were similar, however, because the limiting case for both bus master types was a Read 1 time slot appearing as a Read 0 time slot due to slow rise times.

ALTERNATE BUS MASTERS

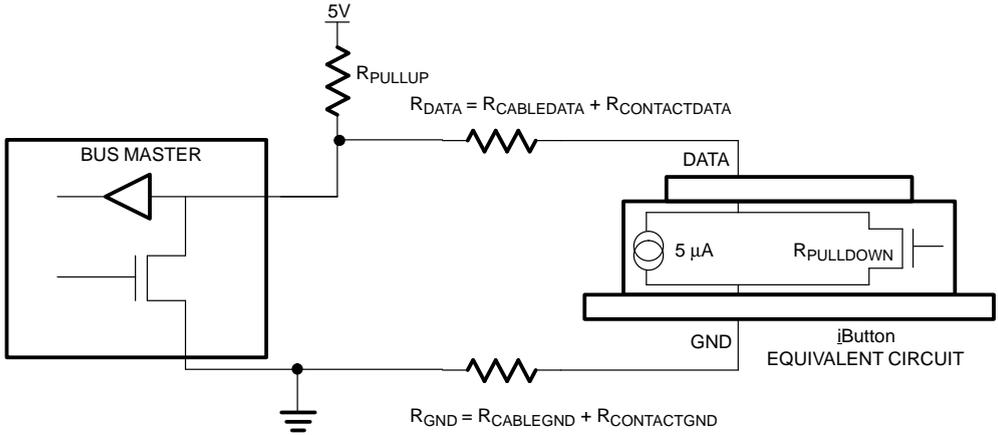
The simple open drain bus master or COM port bus master was quite adequate for driving several hundred meters of cable with relatively large capacitive loads and/or device fanout, but other bus masters could be developed for a specific application. The input stage of the resistor-pullup bus master is a port pin on the DS5000 which requires normal TTL input levels for correct operation. A more sophisticated non-TTL input stage may provide some additional improvement. A current source pullup or pulsed active pullup may reduce the time required to return the data line high for a Read 1 Time Slot. In general, however, active pull-ups should be scrutinized for excessive ringing caused by sharp signal transitions. Any new bus master design should be fully characterized before it is deployed into the field.

READ 1 TIME SLOT DEGRADATION FROM CABLE LOADING Figure 5



Failure Mode: Pullup at Bus Master is unable to recover data line quickly enough, Read 1 Time Slot rise time increases such that it is misinterpreted by input stage of Bus Master as a Read 0 Time Slot.

Solution: Decrease pullup resistor down to a minimum of 1 k Ω to provide fastest recovery but still maintain adequate logic levels for the Bus Master input. Also minimize time that active pull-down holds data line low to provide greatest amount of time for recovery within the 15 μ s Read 1 window.

DETERMINATION OF PULLUP RESISTOR VALUE Figure 6

$R_{PULLDOWN} \text{ Max.} = 0.4\text{V} / 4 \text{ mA} = 100 \text{ ohms}$ (from jButton data sheet)

$R_{PULLUP} \text{ Min.} = (5 - 0.4) / 4 \text{ mA} = 1150 \text{ ohms}$

Bus Master input stage is TTL equivalent: $V_{IL} = 0.8 / V_{IH} = 2.0$

$R_{CABLE} + R_{CONTACT}$ are interconnect resistances that will increase the minimum pullup resistance that will still allow correct operation. To calculate the value for R_{PULLUP} use the following equations:

$$0.4\text{V} = I_{MAX}(R_{DATA} + 100 + R_{GND})$$

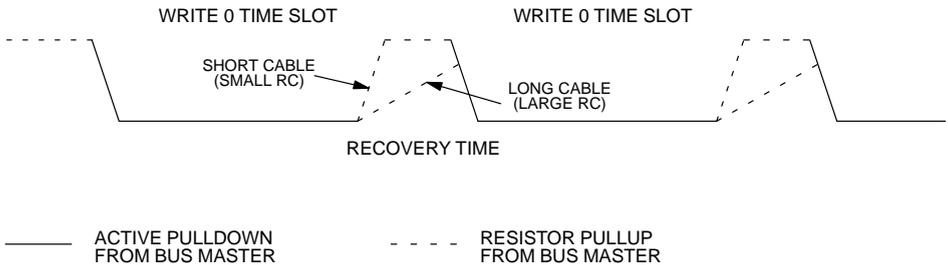
$$R_{PULLUP} = 4.6\text{V} / I_{MAX} = 4.6\text{V} / [0.4\text{V} / (R_{DATA} + 100 + R_{GND})]$$

Assume $R_{DATA} = R_{GND} = R_{INTERCONNECT}$

$$R_{PULLUP} = 11.5(2 * R_{INTERCONNECT} + 100) = 23(R_{INTERCONNECT}) + 1150$$

With negligible interconnect resistance, $R_{PULLUP} = 1150$ as above.

With $R_{PULLUP} = 4.7\text{k}\Omega$, $R_{INTERCONNECT}$ can be a maximum of 154 ohms.

CONSECUTIVE WRITE 0 TIME SLOT DEGRADATION FROM CABLE LOADING Figure 7

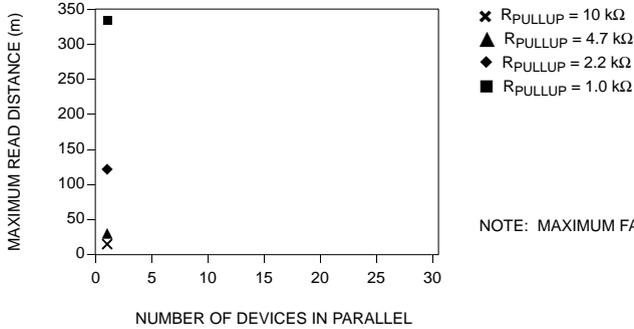
Failure Mode: jButton unable to recognize command byte with consecutive write 0 time slots (Search ROM=F0 hex, for example).

Solution: Increase recovery time from the 1 μs minimum to 15 μs to allow data line to recover completely. This will reduce data rate slightly, but allow operation over much longer distances.

Bus Master Type = Open Drain with Resistor
Cable is 22 gauge twisted-pair

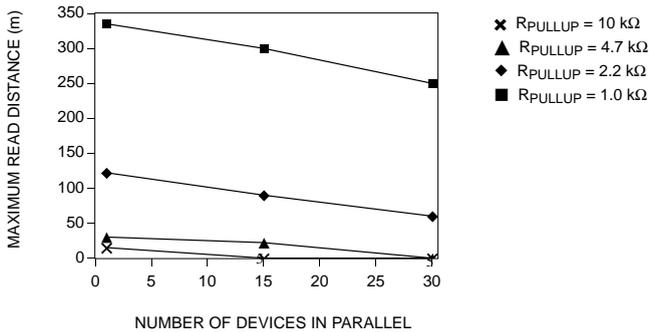
FANOUT vs. CABLE LENGTH vs. RESISTOR PULLUP

DS1990-R3*

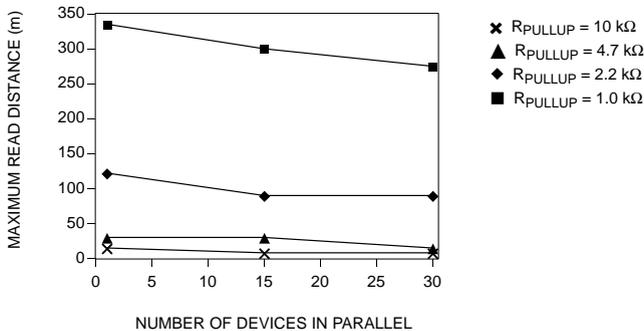


NOTE: MAXIMUM FANOUT FOR DS1990 IS ONE.*

DS1991L-F5



DS1992/3/4L-F5

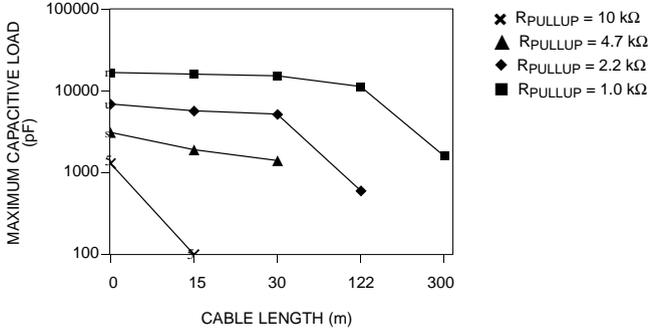


*THE DS1990-R3 HAS BEEN REPLACED BY THE DS1990A-F3. THE MAXIMUM FAN OUT OF THE DS1990A IS NOT LIMITED TO 1.

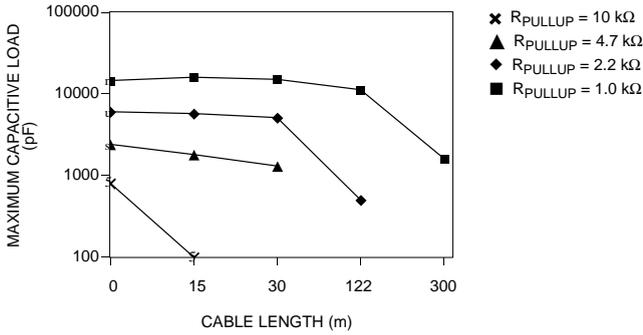
Bus Master Type = Open Drain with Resistor
Cable is 22 gauge twisted-pair
Reading One Device

CABLE LENGTH vs. CAPACITIVE LOAD vs. RESISTOR PULLUP

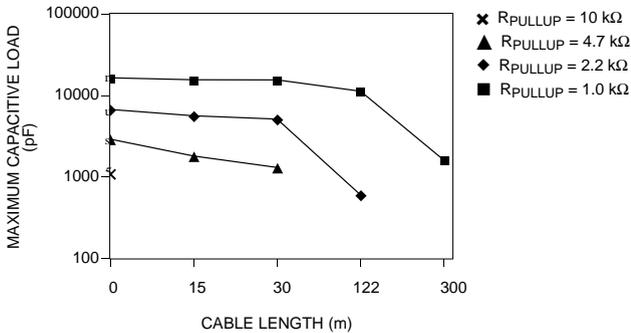
DS1990-R3*



DS1991L-F5



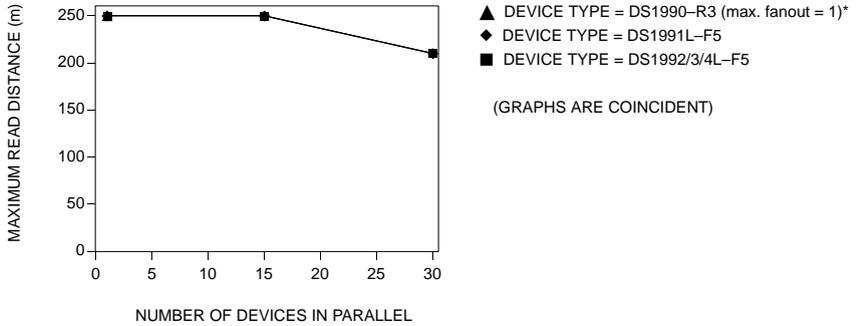
DS1992/3/4L-F5



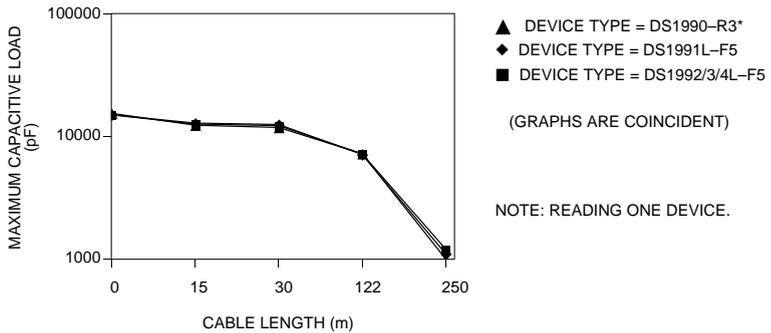
*THE DS1990-R3 HAS BEEN REPLACED BY THE DS1990A-F3.

Bus Master Type = COM Port w/ DS9097 Adapter
Cable is 22 gauge twisted-pair

FANOUT vs. CABLE LENGTH vs. DEVICE TYPE



CABLE LENGTH vs. CAPACITIVE LOAD vs. DEVICE TYPE



*THE DS1990-R3 HAS BEEN REPLACED BY THE DS1990A-F3. THE MAXIMUM FAN OUT OF THE DS1990A IS NOT LIMITED TO 1.