CASON Package Pad Landing Recommendations

DataFlash®

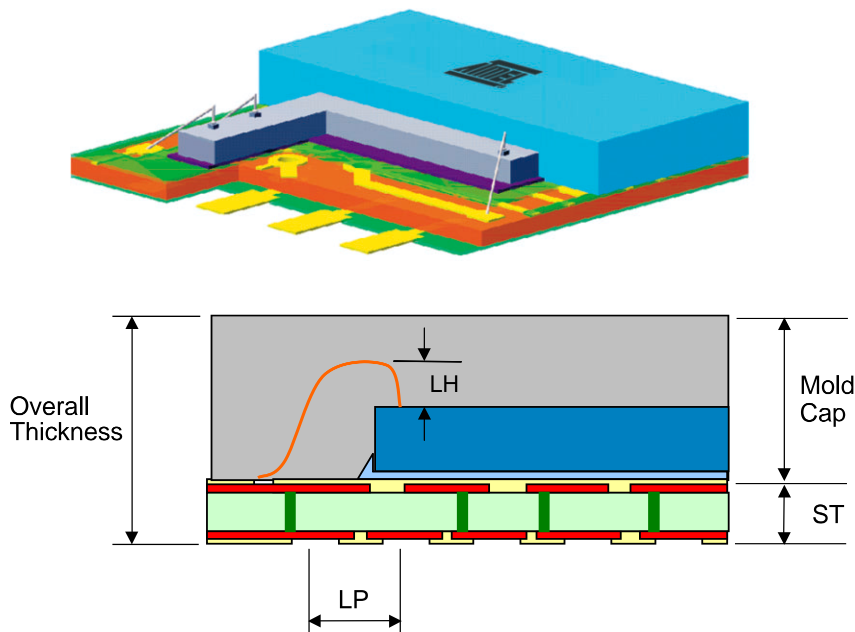
Application Note

Introduction

This application note provides PCB designers with a set of guidelines for successful board mounting of Atmel's DataFlash® memories housed in the Chip Array Small Outline No Lead (CASON) package. The 8-contact CASON package fits the same PCB footprint as the extremely popular 8-lead SOIC (EIAJ) package. The footprint compatibility of the CASON and SOIC packages provide an easy upgrade path for the DataFlash family of serial Flash memories. This allows system designers to migrate to higher densities without the need for PCB changes. Our next generation process technology will support the 8-contact CASON package for higher densities including the 128-Mbit DataFlash. The CASON package fills the need for low profile, space constrained and high-speed requirements of mobile phones, notebook and sub-notebook personal computers, global positioning systems (GPS), hard disk drives, DVD and CD-ROM drives, cordless phones and other wireless telecommunication systems.

This package has 8 contacts and is based on a cavity-up laminate-based substrate of 2 or 4 Cu layers. Figure 1 shows a typical cross section of a CASON package. The CASON package does not contain lead and is therefore ideal for Pb-free circuit board applications.

Figure 1. CASON Cross Section



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PC Board Design Guidelines

The IPC-SM-782 is an industry-standard specification for determining PCB land patterns. The standard provides the guidelines by which the PC Board (PCB) pattern should be designed. However, working with an Electronics Manufacturing Service provider and/or PCB design house with experience in designing and mounting this package type is recommended. The following guidelines are offered based on best known practice, research and evaluations by packaging design manufacturers.

PCB Land Pattern and Solder Mask Design

The CASON package is primarily composed of copper on a BT resin core. This adds stiffness to the package and uniform expansion during board mount and board level temperature cycling. A typical package outline and appropriate tolerances are shown in Figure 2. The solder lands on the package side are always Solder Mask Defined (SMD); i.e. the pad is slightly larger than the opening in the Solder Mask. The land pattern on the PCB should be designed to correspond with the land pattern on the package. The land on the PCB should be Non-Solder Mask Defined (NSMD) in order to realize the best board level reliability performance. The X & Y values of the solder land pad on the PCB should be equal to, or no more than 20% smaller than that of the package solder land. Refer to Figure 3 for the X and Y dimensions.

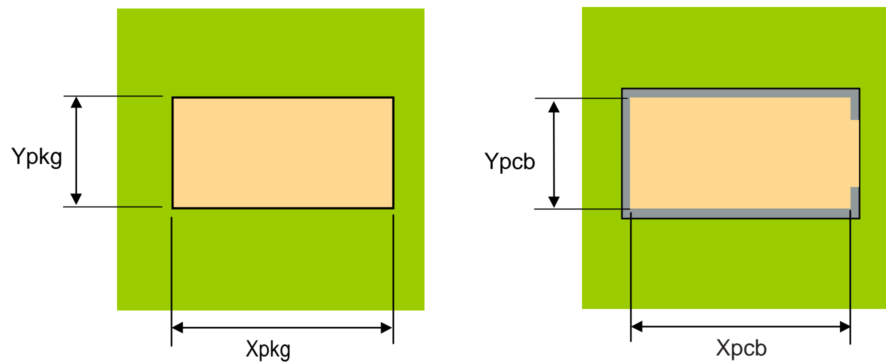
Designing the PCB land (X,Y) dimensions equal to the Solder Mask Opening of the package is quite common, however, making the NSMD land pad on the board a little smaller can increase the stand-off and board level reliability.

When the PCB lands are the exact same size as the package lands, board level temperature cycling will eventually cause a solder joint failure at the solder joint to package land interface. By slightly decreasing the PCB pad land, the failure point will not shift to the PCB to solder joint interface, and the number of temperature cycles achieved may see a positive impact.

The board traces leading into the CASON land pads (on the PCB) should not be wider than the minimum dimension of the land pad either X or Y. This is to avoid excessive solder paste wicking along the trace, away from the joint area and possibly impacting board level reliability.

Figure 2. Package Outline Drawing

Figure 3. PCB Land Pattern Design Guidelines (Rectangular NSMD)



Land Pitch (P) (mm)	Land Pad Length (X) Typ (mm)	Land Pad Width (Y) Typ (mm)	PCB Pad Length (X) (µm)		PCB Pad Width (Y) (µm)	
			Min	Max	Min	Max
1.27	1.27	0.63	1020	1270	450	630

Note: While rectangular pads are typically 50% of the pitch in width; it is not a rigid rule. Therefore, other formats are possible. Nonetheless, the PCB pad should be 80% to 100% of the Package Solder Mask opening in X & Y.

Board Assembly Guidelines

Most reputable Electronics Manufacturing Service providers have their own rules, guidelines, and standard practice regarding mounting surface mount packages in general. However, the following guidelines and principles have been characterized and proven to result in a reliable board assembly.

Stencil Design

- Laser cut stencil with electropolished walls is recommended.
- For NSMD pads aperture size to PCB pad size is typically 1:1 ratio with 0.125 to 0.150 mm thick stencil.

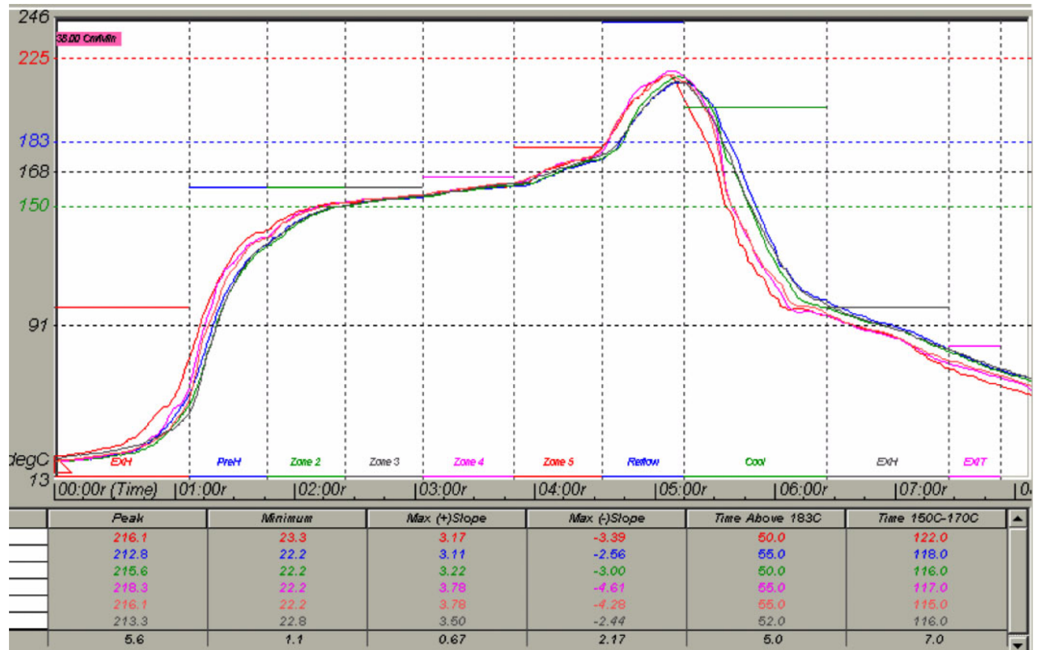
Paste and Reflow

- Water soluble or No-Clean paste can be used (Type 3).
  – 37%Pb-63%Sn eutectic paste
  – Sn-3%Ag-0.5%Cu lead free paste
- The reflow profile depends on the thermal mass of the other packages on the board. The CASON package will most likely be one of the lower mass packages on the board. Studies have shown good results when using the following reflow guidelines based on the solder paste used:
  – **For PbSn Paste**: The reflow peak temperature should be kept in the 215° C to 225° C range. An actual reflow profile used to produce good board level reliability result is shown in Figure 4 (no clean paste).
  – **For PbFree Paste**: The reflow peak temperature should be kept in the 225° C to 245° C range. An actual reflow profile used to produce good board level reliability result is shown in Figure 5 (no clean paste).

Note: For more detailed reflow information, refer to JEDEC-STD-020.

- No Clean pastes typically have shorter reflow profiles and dwells as the alcohol based solvent activates rapidly. Follow the paste manufacturers recommended profile and application notes. Also, no clean pastes have flux that is typically less active so reflow in Nitrogen environment (<75 ppm) may be advised.

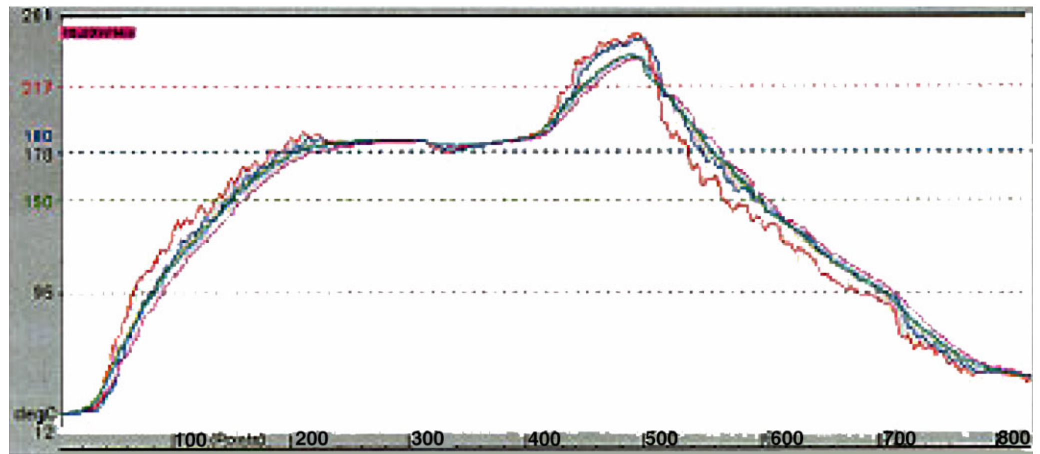
Figure 4. PbSn Reflow Profile



Peak	Minimum	Max (+)Slope	Max (-)Slope	Time Above 183C	Time 150C-170C
216.1	23.3	3.17	-3.39	50.0	122.0
212.8	22.2	3.11	-2.56	55.0	118.0
215.6	22.2	3.22	-3.00	50.0	116.0
218.3	22.2	3.78	-4.61	55.0	117.0
216.1	22.2	3.78	-4.28	55.0	115.0
213.3	22.8	3.50	-2.44	52.0	116.0
5.6	1.1	0.67	2.17	5.0	7.0

Note: Time between 150° C - 170° C: 120 sec
Time above 183° C: 50 sec
Peak Temp: 218° C

Figure 5. Pb-Free Reflow Profile



Note: Time between 130° C - 160° C: 120 sec
Time above 217° C: 60 - 70 sec
Peak Temp: 235.5°C

Rework

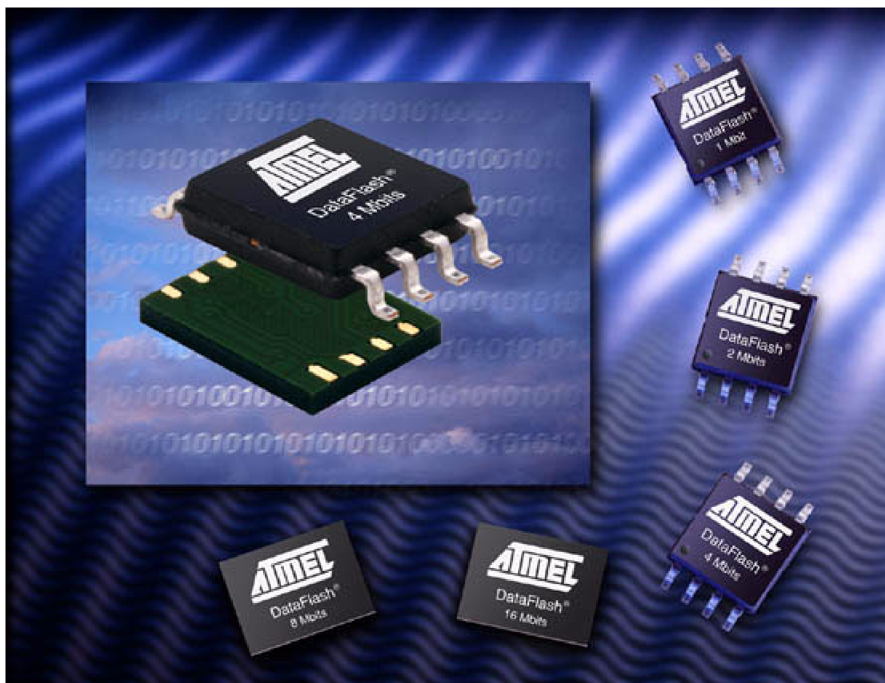
The CASON package is relatively easy to rework due to low thermal mass and high temperature stability.

- Bake board at 125° C at least 2 hours prior to part removal.
- Make sure board is flat to avoid tilting and improper removal that could cause bridging of solder.
- Under board heat is not normally required, if desired, maintain 120°C.
- Make sure hot gas nozzles are properly directed at part to be removed.
  - PbSn: Peak temperature should be 200°C.
  - PbFree: Do not exceed peak temperature of 225°C, if possible.
- Lift off part with integrated vacuum pick-up and clean the site properly with solder wick or alternative method.
- On rework printer/placer take care to properly align and print the same solder paste with a metal blade and a miniature stencil.
- Properly place the new package within 0.15 mm accuracy, if possible, and use the same reflow profile as used to initial mount package.

Footprint Compatibility

The 8-contact CASON package (8CN3) is footprint compatible to the EIAJ standard 8-lead SOIC (8S2). This 8-pin footprint allows easy density migration without board changes. Future die shrinks will enable densities up through 128 Mbits to fit into this footprint. Consult the current DataFlash datasheets for availability. Figure 6 demonstrates CASON and SOIC compatibility.

Figure 6. CASON and SOIC Compatibility



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