AVR001: Conditional Assembly and Portability Macros

8-bit AVR® Microcontroller

Application Note

Features

- **Increased Assembly Portability**
- **Easier Code Writing**
- **Simplified I/O Register Access**
- **Improved Assembly Status Feedback**

Introduction

This application note describes the Conditional Assembly feature present in the AVR Assembler version 1.71 and later. The AVR assembler can be downloaded seperately or together with AVR Studio 4.08 from the Atmel web site.

Examples of how to use Conditional Assembly are presented. One of the examples is a set of macros that will enable the software writer to write a generic code that will assemble to any AVR without other modifications than changing the device definition file.

Theory of Operation

Conditional Assembly (CA) was introduced in the AVR assembler (avrasm32.exe) in version 1.74. CA is based on a series of directives similar to the preprocessor directives available in C.

Two debugging directives are introduced in AVR assembler version 1.74; a message directive and an error directive.

Conditional Assembly

The assembler evaluates a CA directive expression at compile-time and determines if the code enclosed by the CA directive is to be included or not.

A list of CA directives are presented in Table 1 on page 2.

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Table 1. Conditional Assembly Directives

Directive	Description
.ifdef <symbol>	Includes the code present between the .ifdef and the corresponding .else or .endif if the symbol is defined. Only symbols declared by .EQU or .SET are evaluated by .ifdef; symbols defined by the .def directives are treated differently by the assembler and cannot be used with .ifdef.
.ifndef <symbol>	Includes the code present between the .ifndef and the corresponding .else or .endif if the symbol is not defined. Only symbols declared by .EQU or .SET are evaluated by .ifndef; symbols defined by the .def directives are treated differently by the assembler and cannot be used with .ifndef.
.if <expression>	Includes the code present between the .if and the corresponding .else, .elseif, or .endif if the expression evaluates to a value different from zero (true).
.elseif <expression>	A .elseif must be preceded by .if. It will include the code present between the .elseif and the corresponding .else, .elseif, or .endif if the expression evaluates to a value different from zero (true).
.else	A .else must be preceded by a .if or .elseif. Will include the code present between the .else and the corresponding .endif if the expression specified for the corresponding .if or .elseif evaluates to zero (false).
.endif	A .endif must be preceded by a .ifdef, .ifndef, .if, .else or .elseif. The .endif defines the end of scope for the corresponding .ifdef, .ifndef, .if, .else or .elseif.

The directives can be nested in up to 5 levels. CA directives can be combined with the .MACRO directive to make macros assemble differently depending on the enclosed CA directives. This is used in the example code for this application note.

Debugging Directives

When developing code it is useful with different types of feedback at assembly-time. For this purpose two new directives have been added: one that outputs a message to the message window if encountered and one that issues an error (accompanied with an error message). The debugging directives are described in Table 2.

Table 2. Debugging Directives

Directive	Description
.message "string”	If the .message directive is encountered when code is assembled the "string" is written to the message window.
.error "string”	If the .error directive is encountered when code is assembled an assembly error is issued and the "string" is written to the message window.

These directives can be combined with (e.g. AC) directives to provide information about the assembling status. The use of these directives is included in the code example for this application note.

Example 1: General usage of CA

The reuse of code modules from one project to the next can often be a great time saver. Reusage of code modules will, without pre-processor directives or in this case CA directives, easily result in several different versions of the code module as it needs to be taylored for the different targets used. Using CA one version can be used for several target devices.

As an example, consider the initilazation of the I/0 pins used for UART communication:

```
.EQU   ATmega128=1 ;Declares the symbol ATmega128
;EQU   ATmega16=1  ;Declares the symbol ATmega16
.EQU   UART= 0     ;UART0 or UART1

.ifdef ATmega128
  .message "UART Module assembled for ATmega128."
  .if UART == 0
    .message "UART0 used."
    sbi  DDRE, PE1    ;Config TxD as output
  .elseif UART == 1
    .message "UART0 used."
    sbi  DDRD, PD3    ;Config TxD as output
  .else
    .error "UART number not specified"
  .endif
.elseif ATmega16
  .message "UART Module assembled for ATmega128."
  .if UART == 0
    .message "UART0 used."
    sbi  DDRD, PD1    ;Config TxD as output
  .else
    .error "UART number not specified"
  .endif
.endif
```

As seen from the code example, a device specific initialization of (e.g. a UART) can be contained in one file. This allows for better control of the code modules reused.

Example 2: Conditional Assembly in Macros

The code example for this application note requires the AVR Assembler version 1.71 or later to assembled correctly. The AVR assembler version 1.71 is distributed seperately and with AVR Studio 4.08. The latest version of the AVR Assembler and AVR Studio can be downloaded from the AVR section on the Atmel web site.

The file "macros.h" includes a number of macros to ease bit and byte access in the I/0 and data space. The macros are listed with comments in Table 3.

Table 3. Macros Defined in the File “macros.inc”

Macro Name	Description
SETB [Address, Bit Mask, Register]	"Set Bit" - Set a bit in any location in the I/0 space. Registers that can be used are R16-R31.
CLRB [Address, Bit Mask, Register]	"Clear Bit" - Clear a bit in any location in the I/0 space. Registers that can be used are R16-R31.
SKBS [Address, Bit Mask, Register]	"Skip if Bit Set" - skip the instruction following the macro if the bit specified by Bit Mask in any location in the I/0 space is set.
SKBC [Address, Bit Mask, Register]	"Skip if Bit Cleared" - skip the instruction following the macro if the bit specified by Bit Mask in any location in the I/0 space is cleared.
STORE [Register, Address]	"Store register" - Stores the contents of a register in a location in any location in the I/0 space.
LOAD [Register, Address]	"Load register" - Load a register with the contents from any location in the I/0 space.

The reason for using these macros to access I/0 space (and extended I/0 space) is that the code writer need not consider where in the I/0 space the accessed registers are located. This would be required if the macros where not used as not all instructions reach all addresses in the I/0 space. The advantages are therefore numerous:

1. The author doesn't need to know the I/0 map, just the names of the registers.
2. The standard definition files for register and bit names can be used.
3. The most code size efficient instructions are used to access a register.
4. The assembly code can be ported to any device without modifying the code.

The Set-Bit Macro

As all the macros are similar in nature only the SETB are described in details.

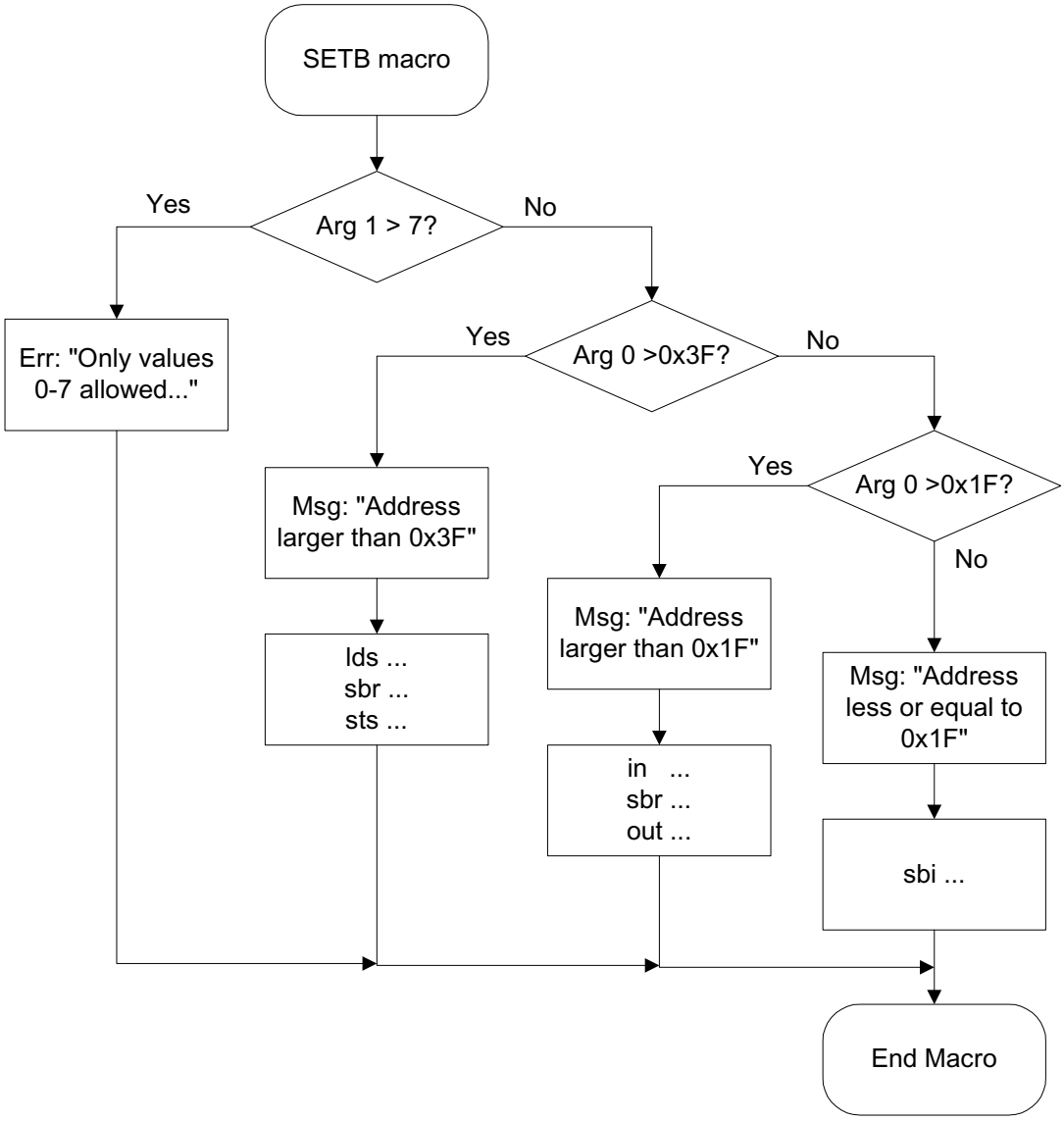
Three arguments are specified for the SETB macro: a destination address, a bit mask and a register. The register is only used if the address is higher than 0x001F, but it is recommended to specify it anyway to ensure correct assembly and best portability opportunities.

The range of the Bit mask is verified to be between 0 and 7, if this condition is violated an error is issued using the .error directive.

If the address is below 0x1F the SBI instruction is used to set the bit. If the Address is between 0x1F and 0x3F IN and OUT instruction is used to access the address. Finally, if the address is above 0x3F the LDS and STS instructions are used.

Figure 1 shows how the assembler handles the SETB macro using CA.

Figure 1. Assembling flow for CA inside SETB macro



Potential Improvements

At the expense of one of the registers Y or Z the LOAD and STORE macros could be improved to execute faster and be more code compact: If one of these registers are reserved for indirect access the STS and LDS instructions could be replaced by STD and LDD. As this is a constraint to the code writer this has not been added in the present implementation.

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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