Dual PLL Frequency Synthesizer

Preliminary Technical Data — ADF4216/ADF4217/ADF4218

FEATURES

ADF4216: 550MHz/1.2GHz
ADF4217: 550MHz/2.0GHz
ADF4218: 550MHz/2.5GHz
+2.7 V to +5.5 V Power Supply
Selectable Charge Pump Currents
Selectable Dual Modulus Prescaler
3-Wire Serial Interface
Power Down Mode

APPLICATIONS

Portable Wireless Communications (PCS/PCN, Cordless)
Cordless and Cellular Telephone Systems
Wireless Local Area Networks (WLANs)
Cable TV Tuners (CATV)
Pagers

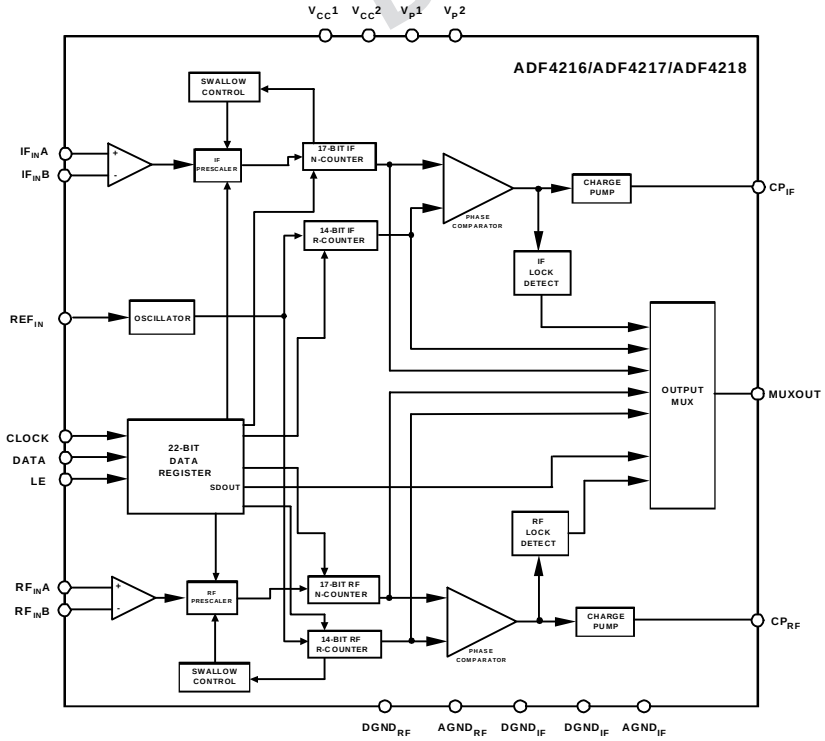
GENERAL DESCRIPTION

The ADF4216/ADF4217/ADF4218 is a dual frequency synthesizer which can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They can provide the LO for both the RF and IF sections. They consist of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (11-bit) counters, in conjunction with the dual modulus prescaler (P/P+1), implement an N divider (N= BP+A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizers are used with an external loop filter and VCO's (Voltage Controlled Oscillators)

Control of all the on-chip registers is via a simple 3-wire interface.

The devices operate with a 3V (± 10%) or 5V(± 10%) power supply and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



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ADF4216/17/18 – SPECIFICATIONS[1] (V_{CC} = +3 V ± 10%, +5 V ± 10%; V_P = V_{CC}, +5 V ± 10%; GND = 0 V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips	Units	Test Conditions/Comments
RF/IF CHARACTERISTICS				
RF Input Frequency (RF_{IN})				
ADF4216	0.1/1.2	0.1/1.2	GHz min/max	
ADF4217	0.1/2.0	0.1/2.0	GHz min/max	
ADF4218	0.1/2.5	0.1/2.5	GHz min/max	
IF Input Frequency (IF_{IN})	45/550	45/550	MHz min/max	
Reference Input Frequency	5/40	5/40	MHz min/max	
Phase Detector Frequency	10	10	MHz max	
RF Input Sensitivity	-15/0	-15/0	dBm min/max	3V Power Supply
	-10/0	-10/0	dBm min/max	5V Power Supply
IF Input Sensitivity	-15/0	-15/0	dBm min/max	3V Power Supply
	-10/0	-10/0	dBm min/max	5V Power Supply
Reference Input Sensitivity	-5	-5	dBm min	
CHARGE PUMP				
I_{CP} sink/source				
High Value	4	4	mA typ	
Low Value	1	1	mA typ	
I_{CP} Three State Current	1	1	nA max	
Sink and Source Current Matching	2	2	% typ	$0.5V < V_{CP} < V_P - 0.5$
I_{CP} vs. V_{CP}	2	2	% typ	$0.5V < V_{CP} < V_P - 0.5$
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	$0.8*V_{CC}$	$0.8*V_{CC}$	V min	
V_{INL}, Input Low Voltage	$0.2*V_{CC}$	$0.2*V_{CC}$	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Oscillator Input Current	±100	±100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	V_{CC} - 0.4	V_{CC} - 0.4	V min	I_{OH} = 1mA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 1mA
POWER SUPPLIES				
$V_{CC}1$	2.7/5.5	2.7/5.5	V min/V max	
$V_{CC}2$	$V_{CC}1$	$V_{CC}1$		
V_P	$V_{CC}1$/5.5	$V_{CC}1$/5.5	V min/V max	
I_{CC}				
ADF4216	4.0	4.0	mA max	
ADF4217	4.5	4.5	mA max	
ADF4218	5.0	5.0	mA max	
Low Power Sleep Mode	1	1	µA typ	

ADF4216/17/18 – SPECIFICATIONS[1] (V_{CC} = +3 V ± 10%, +5 V ± 10%; V_P = V_{CC}, +5 V ± 10%; GND = 0 V; R_{SET} = 4.7kΩ; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips	Units	Test Conditions/Comments
NOISE CHARACTERISTICS				
Phase Noise Floor	-173	-173	dBc/Hz typ	@ 25kHz PFD Frequency
	-165	-165	dBc/Hz typ	@ 200kHz PFD Frequency
Phase Noise Performance[2]				@ VCO Output
ADF4216, ADF4217, ADF4218 (IF)[3]	-97	-97	dBc/Hz typ	
ADF4216 (RF)[4]	-91	-91	dBc/Hz typ	
ADF4216 (RF)[5]	-82	-82	dBc/Hz typ	
ADF4217 (RF)[6]	-85	-85	dBc/Hz typ	
ADF4217 (RF)[7]	-65	-65	dBc/Hz typ	
ADF4218 (RF)[8]	-85	-85	dBc/Hz typ	
Spurious Signals				Measured at offset of f_{PFD}/2f_{PFD}
ADF4216, ADF4217, ADF4218 (IF)[3]	tbd/tbd	tbd/tbd	dB typ	
ADF4216 (RF)[4]	tbd/tbd	tbd/tbd	dB typ	
ADF4216 (RF)[5]	tbd/tbd	tbd/tbd	dB typ	
ADF4217 (RF)[6]	tbd/tbd	tbd/tbd	dB typ	
ADF4217 (RF)[7]	tbd/tbd	tbd/tbd	dB typ	
ADF4218 (RF)[8]	tbd/tbd	tbd/tbd	dB typ	

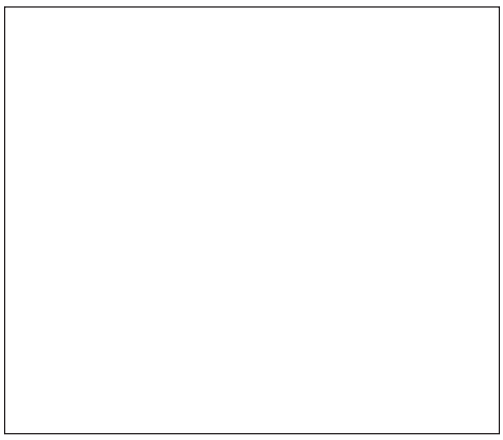
NOTES

1 Operating temperature range is as follows: B Version: –40°C to +85°C.

2 The phase noise is measured with the EVAL-ADF421XEB Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer. (f_{REFOUT} = 10MHz @ 0dBm)

3. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{IF} = 460MHz; N = 2300; Loop B/W = 20kHz;
4. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900MHz; N = 4500; Loop B/W = 12kHz
5. f_{REFIN} = 10 MHz; f_{PFD} = 30kHz; Offset frequency = 1 kHz; f_{RF} = 836MHz; N = 27867; Loop B/W = 3kHz
6. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1880MHz; N = 9400; Loop B/W = 20kHz
7. f_{REFIN} = 10 MHz; f_{PFD} = 10kHz; Offset frequency = 250Hz; f_{RF} = 1880MHz; N = 188000; Loop B/W = 1kHz
8. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1960MHz; N = 9800; Loop B/W = 20kHz

CHIP LAYOUT



TIMING CHARACTERISTICS (V_{CC} = +5 V 10%, +3 V ± 10%; GND = 0 V, unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	50	ns min	DATA to CLOCK Set Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	50	ns min	CLOCK High Duration
t_4	50	ns min	CLOCK Low Duration
t_5	50	ns min	CLOCK to LE Set Up Time
t_6	50	ns min	LE Pulse Width

NOTE
Guaranteed by Design but not Production Tested.

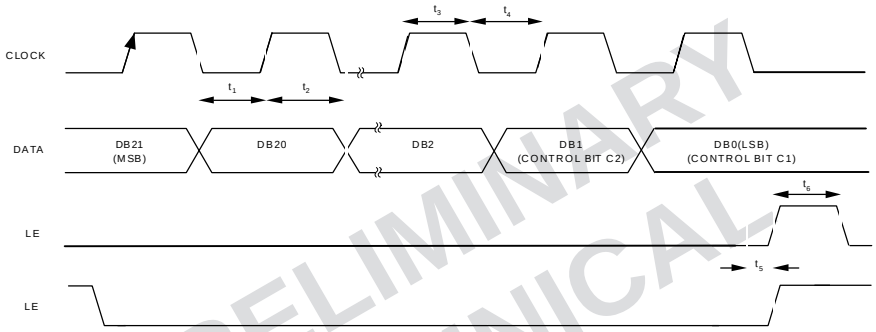


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{CC} to GND . . . . . –0.3 V to +7 V
V_P to GND . . . . . –0.3 V to +7 V
V_P to V_{DD} . . . . . –0.3 V to +3.5 V
Digital I/O Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . . –0.3 V to V_P + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . +150°C
TSSOP θ_{JA} Thermal Impedance . . . . . TBD°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device is a high-performance RF integrated circuit with an ESD rating of < 2kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

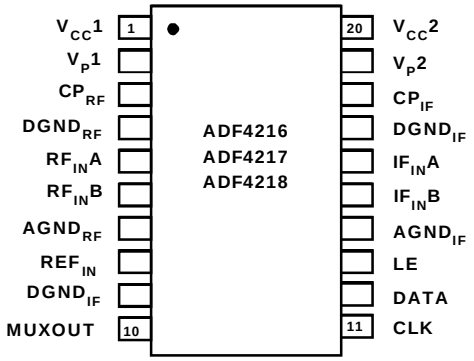
ORDERING GUIDE

Model	Temperature Range	Package Option*
ADF4216BRU	–40°C to +85°C	RU-20
ADF4216BCHIPS	–40°C to +85°C	
ADF4217BRU	–40°C to +85°C	RU-20
ADF4217BCHIPS	–40°C to +85°C	
ADF4218BRU	–40°C to +85°C	RU-20
ADF4218BCHIPS	–40°C to +85°C	

*RU = Thin Shrink Small Outline Package (TSSOP).

PIN DESCRIPTION

Mnemonic	Function
$V_{CC}1$	Positive power supply for the RF section. A 0.1µF capacitor should be connected between this pin and the RF ground pin, $DGND_{RF}$. $V_{CC}1$ should have a value of +5V ± 10% or +3V ± 10%. $V_{CC}1$ must have the same potential as $V_{CC}2$.
V_P1	Power supply for the RF charge pump. This should be greater than or equal to V_{DD}.
CP_{RF}	Output from the RF charge pump. This is normally connected to a loop filter which drives the input to an external VCO.
$DGND_{RF}$	Ground pin for the RF digital circuitry.
$RF_{IN}A$	Input to the RF Prescaler. This low-level input signal is normally taken from the RF VCO.
$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor. If this is not done then there will be some degradation in RF sensitivity.
$AGND_{RF}$	Ground pin for the RF analog circuitry.
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100kΩ. This input can be driven from a TTL or CMOS crystal oscillator.
$DGND_{IF}$	Ground pin for the IF digital, interface and control circuitry.
MUXOUT	This multiplexer output allows either the IF/RF Lock Detect, the scaled RF or the scaled Reference Frequency to be accessed externally.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
$AGND_{IF}$	Ground pin for the IF analog circuitry.
$IF_{IN}B$	Complementary Input to the IF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor. If this is not done then there will be some degradation in IF sensitivity.
$IF_{IN}A$	Input to the IF Prescaler. This low-level input signal is normally taken from the IF VCO.
$DGND_{IF}$	Ground pin for the IF digital, interface and control circuitry.
CP_{IF}	Output from the IF charge pump. This is normally connected to a loop filter which drives the input to an external VCO.
V_P2	Power supply for the IF charge pump. This should be greater than or equal to V_{CC}.
$V_{CC}2$	Positive power supply for the IF, interface and oscillator sections. A 0.1µF capacitor should be connected between this pin and the IF ground pin, $DGND_{IF}$. $V_{CC}2$ should have a value of +5V ± 10% or +3V ± 10%. $V_{CC}2$ must have the same potential as $V_{CC}1$.



CIRCUIT DESCRIPTION

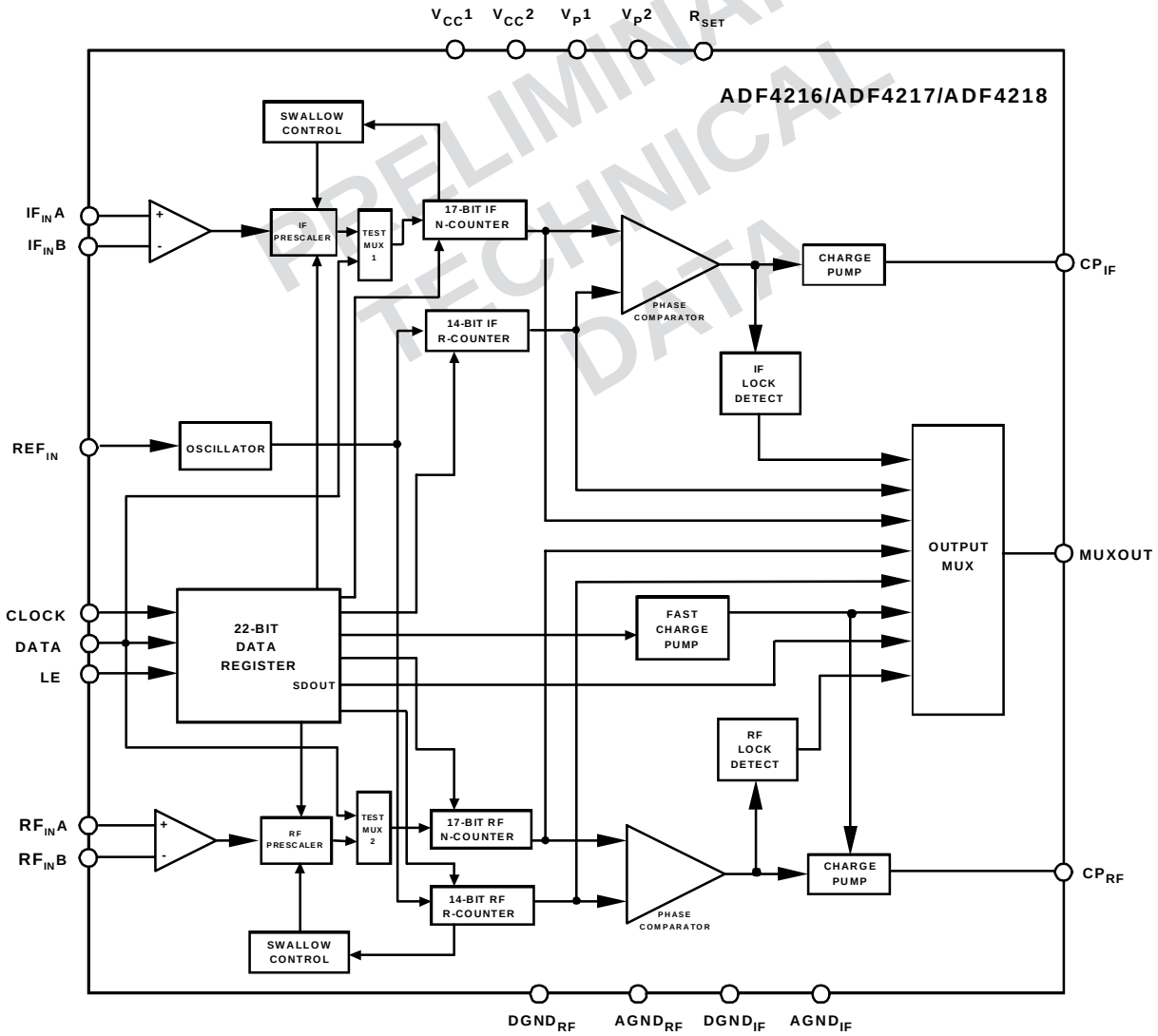
INPUT SHIFT REGISTER

The functional block diagram for the ADF4216 family is shown below. The main blocks include a 22-bit input shift register, a 14-bit R counter and an 17-bit N counter, comprising a 6-bit A counter and a 11-bit B counter. Data is clocked into the 22-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two lsb's DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table 1.

Table 1. C2, C1 Truth Table

Control Bits C2	Control Bits C1	Data Latch
0	0	IF R Counter
0	1	IF N Counter (A and B)
1	0	RF R Counter
1	1	RF N Counter (A and B)

FUNCTIONAL BLOCK DIAGRAM



IF REFERENCE (IF R) COUNTER

If control bits C2, C1 are 0,0 then the data is transferred from the input shift register to the IF R counter as shown in Table 2. Table 3 shows the divide ratios possible.

Table 2. Programming the Reference (R) Counter

DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2(0)	C1(0)
IF F_O	IF Lock Detect	3-State CP_{IF}	IF CP Gain	IF PD Polarity		14-Bit Reference Counter														Control Bits	

ADF4216 Family
ADF4206 Family

1. Data is shifted in MSB (DB23) first.

Table 3. R Counter Divide Ratios

Divide Ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0	0	0	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
16382	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES
1. Divide ratio: 1 to 16383

TABLE 4. Truth Table for Program Modes on ADF4216

P12 RFR20	P11 RFR19	P4 IFR20	P3 IFR19	Program Mode
0	0	0	0	Drive MUXOUT (F_OLD on LMX233X) to low logic state
0	0	0	1	IF Analog Lock Detect on MUXOUT
0	X	1	0	IF Reference Divider Output on MUXOUT
0	X	1	1	IF N Divider Output on MUXOUT
0	1	0	0	RF Analog Lock Detect on MUXOUT
0	1	0	1	RF/IF Analog Lock Detect on MUXOUT
1	X	0	0	RF Reference Divider on MUXOUT
1	X	0	1	RF N Divider MUXOUT
1	0	1	0	Fast Lock Output Switch On and connected to MUXOUT
1	0	1	1	IF Counter Reset
1	1	1	0	RF Counter Reset
1	1	1	1	IF and RF Counter Reset

Notes for Table 3

1. IF and RF Analog Lock Detect indicate when the PLL is in lock. When the loop is locked and either IF or RF Analog Lock Detect is selected, then the MUXOUT pin will show a logic high with narrow low-going pulses. When the IF/RF Analog Lock Detect is chosen then the locked condition is indicated only when both IF and RF loops are locked.
2. The digital lock detect modes also indicate when the loop is in lock. When the loop is locked and either IF or RF Digital Lock Detect is selected, then the MUXOUT pin will show a logic high. Internally, the device looks for 5 successive low-going pulses of less than 15ns at the output of the PFD and when it finds these it sets the Digital Lock Detect. When the IF/RF Analog Lock Detect is chosen then the locked condition is indicated only when both IF and RF loops are locked.
3. The IF Counter Reset mode resets the R and N counters in the IF section and also puts the IF charge pump into 3-state. The RF Counter Reset mode resets the R and N counters in the RF section and also puts the RF charge pump into 3-state. The IF and RF Counter Reset mode does both of the above. Upon removal of the reset bits, the N counter resumes counting in close alignment with the R counter (maximum error is one prescaler output cycle).
4. The Fastlock mode uses MUXOUT to switch a second loop filter damping resistor to ground during Fastlock operation. Activation of Fastlock occurs whenever RF CP Gain in the RF Reference counter is set to one.In the ADF4210, the Fastlock switch is brought out on a separate pin (FLO). However, its operation is the same as the other devices. Note, however, that the RF CP Gain bit which initiates Fastlock is contained in the RF N counter latch. This means that only one write is needed to both program a new output frequency and also initiate Fastlock.

R COUNTER FOR THE IF

R1 to R14 set the counter divide ratio. The divide range is 1 (00.....001) to 16383(111.....111).

IF PROGRAMMABLE MODES

PD POLARITY.

When the IF VCO characteristics are positive then this bit should be set to "1". When VCO characteristics are negative then this bit should be set to "0".

CHARGE PUMP 3-STATE

To put IF charge pump into 3-State, this bit (P2 for ADF4210, ADF4216, ADF4206 families) should be set to "1". For normal operation this bit should be set to zero.

IF LOCK DETECT / IF F_O

P3 and P4 on the ADF4216 family are used in conjunction with bits P11 and P12 of the RF R Latch to determine a programmable mode. Most but not all of these modes refer to the state of MUXOUT. Table 4 shows the full truth table for the ADF4216 Family Program Modes.

IF CHARGE PUMP CURRENT

On these devices, DB18 determines the level of IF Charge Pump Current. If DB18 is "1" then I_{CP} is High (4mA). If DB18 is "0", then I_{CP} is Low, (I_{CP} High)/4, or 1mA.

IF N COUNTER

If control bits C2, C1 are 0, 1 then the data in the input register is used to program the IF N (A + B) counter. The N counter consists of a 6-bit swallow counter (A counter) and 11-bit programmable counter (B counter). Table 5 shows the input register data format for programming these.

Table 5. Programming the IF A, B Counters

DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	0	A6	A5	A4	A3	A2	A1	C2(0)	C1(1)
IF Power Down	IF Prescaler	11-Bit B Counter												6-Bit A Counter						Control Bits	

ADF4216 Family
ADF4206 Family

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R . The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO}: Ouput Frequency of external voltage controlled oscillator (VCO).

P: Preset modulus of dual modulus prescaler.

B: Preset Divide Ratio of binary 13-bit counter (3 to 8191).

A: Preset Divide Ratio of binary 6-bit swallow counter.

f_{REFIN}: Ouput frequency of the external reference frequency oscillator.

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383).

A Counter Latch For The IF

In the ADF4216 family, A6 - A1 program the A counter. The divide range is 0 (000000) to 15 (001111).

B Counter Latch For the IF

In the ADF4216 family, B1 - B11 program the 11-bit B counter. The valid divide range is 3 (00....011) to 2047 (11...111).

Overall Divide Range

The upper limit of the divide range is defined by ((PxB) + A), where P is the prescaler value. To ensure a fully contiguous range, there is a lower limit of (P^2 -P).

IF Prescaler

In the ADF4216 family, DB20 determines the prescaler value. If DB20 is "0", then the prescaler value is 8/9. If it is "1", then the prescaler value is 16/17.

POWERDOWN FOR THE IF

In all the device families, the IF Power Down works as follows:

Synchronous Power Down.

Programming a “1” to P7 of the ADF4216 family will initiate a power down. If P2 of the ADF4216 family has been set to “0” (normal operation), then a synchronous power down is conducted. The device will automatically put the charge pump into 3-state and then complete the power down.

Asynchronous Power Down

If P2 of the ADF4216 families has been set to “1” (3-state the charge pump), then an asynchronous power down is conducted. The device will go into power down on the rising edge of LE which latches the “1” to the IF Power Down bit.

Activation of either synchronous or asynchronous power down forces the IF loop’s R and N dividers to their load state conditions and the IF_{IN} section is debiased to a high impedance state.

The REF_{IN} oscillator circuit is only disabled if both the IF and RF Power Downs are set.

The input register and latches remain active and are capable of loading and latching data during all the power down modes.

The IF section of the devices will return to normal powered-up operation immediately upon LE latching a “0” to the IF Power Down bit.

Table 6. Programming the RF Reference Counter

ADF4216 Family
ADF4206 Family

DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2(1)	C1(0)
RF F_O	RF Lock Detect	3-State CP_{RF}	RF I_{CP}	RF PD Polarity		14-Bit Reference Counter														Control Bits	

THE RF R COUNTER LATCH

With (C2, C1) = (1,0), the R Counter for RF is programmed.

R Counter For The RF

On the ADF4216 family, R1 to R14 set the counter divide ratio. The divide range is 1 (00.....001) to 16383(111.....111).

RF PROGRAMMABLE MODES

RF PD Polarity.

When the RF VCO characteristics are positive then this bit (P9) should be set to "1". When VCO characteristics are negative then this bit should be set to "0".

Charge Pump 3-State

To put RF charge pump into 3-State, this bit (P10) should be set to "1". For normal operation this bit should be set to zero.

RF Lock Detect /RF F_O

P11 and P12 on the ADF4216 family are used in conjunction with bits P3 and P4 of the IF R Latch to determine a programmable mode. Most but not all of these modes refer to the state of MUXOUT. Table 4 shows the truth table for the ADF4216 family.

RF Charge Pump Current

DB18 determines the level of RF Charge Pump Current. If DB18 is "1" then I_{CP} is High (4.0mA). If DB18 is "0", then I_{CP} is Low, (I_{CP} High)/4, or 1.0mA.

THE RF A,B COUNTER LATCH
With (C2, C1) = (1,1), the A, B Counters for the IF are programmed.

Table 7. Programming the RF N (A B) Counter

DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	0	A6	A5	A4	A3	A2	A1	C2(1)	C1(1)
RF Power Down	RF Prescaler	11-Bit B Counter												6-Bit A Counter						Control Bits	

ADF4216 Family
ADF4206 Family

A Counter Latch For The RF
In the ADF4216 family, A6 - A1 program the 6-bit A counter. The divide range is 0 (000000) to 63 (111111).

B Counter Latch For The RF
B1 - B11 program the 11-bit B counter. The valid divide range is 3 (00....011) to 2047 (11...111).

Overall Divide Range
The upper limit of the divide range is defined by ((PxB) + A), where P is the prescaler value. To ensure a fully contiguous range, there is a lower limit of (P^2 -P).

RF Prescaler
DB20 (P14) determines RF prescaler value.

For the ADF4216 and ADF4216, if P14 is "0", then the prescaler value is 64/65. If P14 is "1", then the prescaler value is 32/33.

For the ADF4218, if P14 is "0', then the prescaler value is 32/33. If P14 is "1", then the prescaler value is 64/65.